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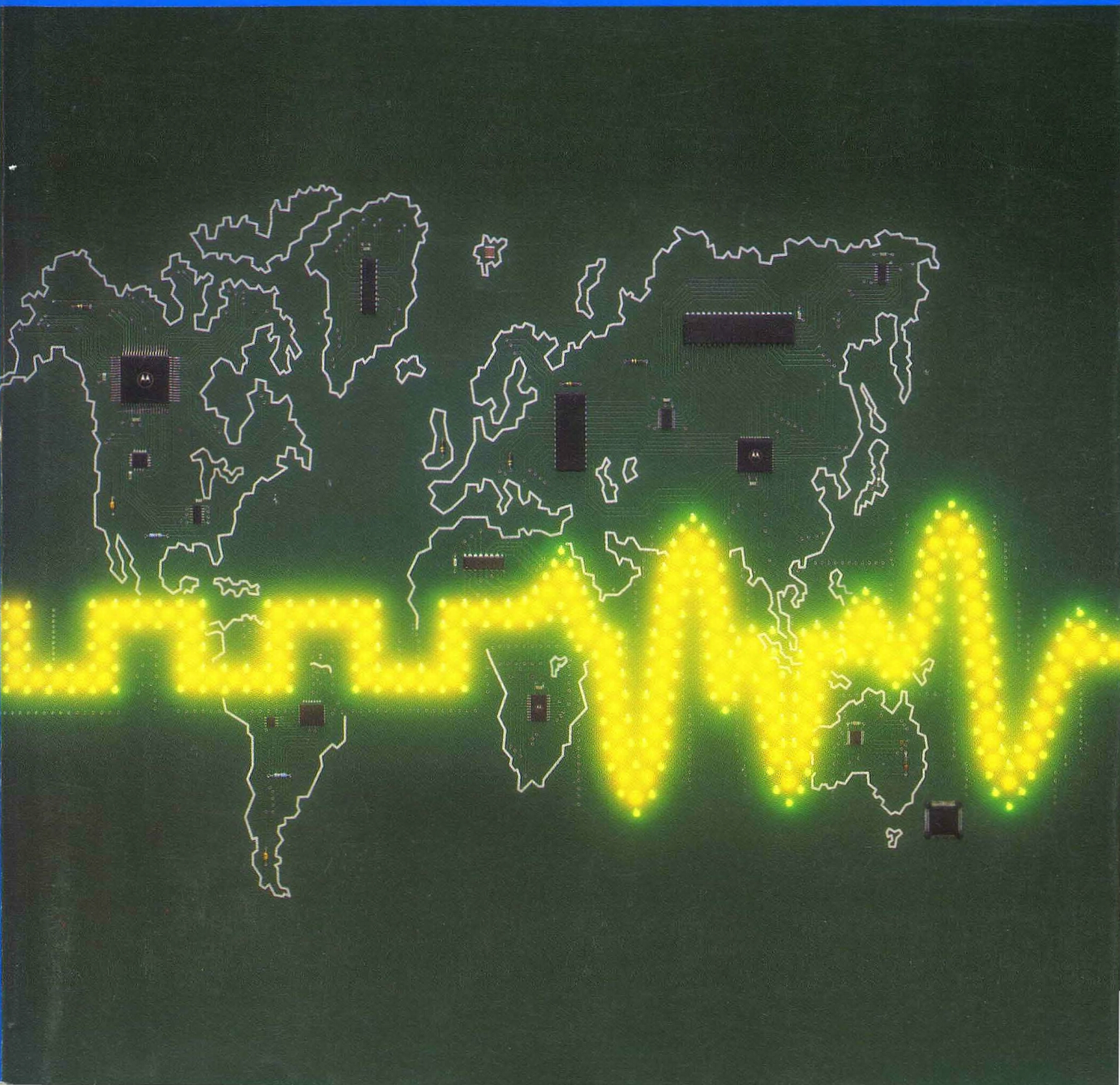
DL136/D
REV 3

Communications

Device Data



MOTOROLA

Communications
Device Data

Motorola offers a broad range of semiconductor communications products for a wide variety of applications. The *Motorola Communications Device Data Book* contains specifications on these parts as well as information on Evaluation Kits, a selection of Application Notes, Handling and Design Guidelines, and Reliability and Quality information. Functional and Technical Selection Guides are also included to help you select the appropriate part for your application.

The *Motorola Communications Device Data Book*, formerly *Motorola Telecommunications Device Data Book*, has been expanded to include additional Motorola devices for use in Communications applications. For instance, Phase-Locked Loop and Remote Control devices have been added from the former DL130/D *CMOS Application-Specific Standard IC Data Book*. Additionally, many new devices have been added since the last revision of this data book.

New Motorola communications devices are being introduced continually. For the latest releases, additional technical information, and pricing, please contact your nearest Motorola Semiconductor Sales Office or authorized distributor. A complete listing of sales offices and authorized distributors is included at the back of this book.

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*NRFND: The listed device is not recommended for new design.

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Selection Guides

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1

Functional Selection Guide

This selection guide includes all Motorola devices characterized in this book. Other devices also used in communications applications, but associated with other product families, appear in the following documents.

Document No.	Title
DL110/D	Volume 1 & 2, RF Device Data
DL111/D	Bipolar Power Transistor Data
DL118/D	Optoelectronics Device Data
DL122/D	MECL Device Data
DL126/D	Small-Signal Transistors/FETs/Diodes
DL128/D	Linear and Interface ICs Data
DL150/D	TVS/Zener Device Data
SG73/D	Master Selection Guide
SG96/D	Linear and Interface Integrated Circuits Selector Guide
SG127/D	Surface Mount Products Selector Guide
SG169/D	MOS Digital-Analog IC Quarterly Update
MC . . .	Data Sheets
DSP . . .	Data Sheets

AMPLIFIERS/COMPARATORS/REGULATORS

Device #	Function	Page #
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ANALOG TELEPHONE

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Device #	Function	Page #
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DSP56002	24-bit Digital Signal Processor	DSP56002/D
DSP56116	16-bit Digital Signal Processor	DSP56116/D
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DMA CONTROLLERS

Device #	Function	Page #
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Device #	Function	Page #
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FIBER DISTRIBUTED DATA INTERFACE (FDDI)

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MC68836	FDDI Clock Generator	MC68836UM/AD
MC68837	Elasticity Buffer and Link Manager	MC68837UM/AD
MC68838	Media Access Controller	MC68838UM/AD
MC68839	FDDI System Interface	
MC68840	Integrated FDDI	

INTEGRATED PROCESSORS

Device #	Function	Page #
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MC68340	Integrated Processor with DMA	MC68340UM/AD
MC68360	Quad Integrated Communication Controller (QUICC)	MC68360UM/AD

INTEGRATED SERVICES DIGITAL NETWORK (ISDN)

Device #	Function	Page #
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INTERFACE

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MC145706	5 V Only Driver/Receiver w/Integrated Standby Mode (3-Driver/2-Receiver)	2-929
MC145707	5 V Only Driver/Receiver w/Integrated Standby Mode (3-Driver/3-Receiver)	2-929

MODEMS

Device #	Function	Page #
MC145442	Single Chip 300 Baud Modem (CCITT V.21)	2-748
MC145443	Single Chip 300 Baud Modem (Bell 103)	2-748
MC145444	Single Chip 300 Baud Modem with DTMF Generator (CCITT V.21)	2-756
MC145447	Calling Line ID (CLID) Receiver with Ring Detector	2-765

NETWORK DEVICES

Device #	Function	Page #
MC68184	Broadband Interface Controller	MC68184UM/AD
MC68185	Twisted Pair Modem	MC68185UM/AD
MC68194	Carrierband Modem	MC68194UM/AD
MC68195	LocalTalk Adaptor	MC68195UM/AD
MC68605	X.25 Protocol Controller	MC68605UM/AD
MC68606	Multi-Link LAPD Controller CCITT Q.920/Q.921	MC68606UM/AD
MC68824	Token Bus Controller	MC68824UM/AD

PHASE-LOCKED LOOP (PLL) FREQUENCY SYNTHESIZERS

Device #	Function	Page #
MC145106	PLL Frequency Synthesizer	2-495
MC145145-2	4-Bit Data Bus Input PLL Frequency Synthesizer	2-502
MC145146-2	4-Bit Data Bus Input PLL Frequency Synthesizer	2-513
MC145149	Dual PLL Frequency Synthesizer	2-524
MC145151-2	Parallel-Input PLL Frequency Synthesizer (Single-Modulus Prescalers)	2-535
MC145152-2	Parallel-Input PLL Frequency Synthesizer (Dual-Modulus Prescalers)	2-538
MC145155-2	Serial-Input PLL Frequency Synthesizer (Single-Modulus Prescalers)	2-542
MC145156-2	Serial-Input PLL Frequency Synthesizer (Dual-Modulus Prescalers)	2-546
MC145157-2	Serial-Input PLL Frequency Synthesizer (Single-Modulus Prescalers)	2-550
MC145158-2	Serial-Input PLL Frequency Synthesizer (Dual-Modulus Prescalers)	2-553
MC145159-1	Serial-Input PLL Frequency Synthesizer with Analog Phase Detector	2-565
MC145160	4-Bit Parallel Dual PLL for 46/49 MHz Cordless Telephones	2-574
MC145161	Dual PLL for 30/39 MHz Cordless Telephones	2-581
MC145162	60 MHz Universal Programmable Dual PLL Frequency Synthesizer	2-587
MC145166	4-Bit Parallel Dual PLL for 46/49 MHz Cordless Telephones	2-574
MC145167	Serial-Input Dual PLL for 46/49 MHz Cordless Telephones	2-574
MC145168	4-Bit Input Dual PLL for 46/49 MHz Cordless Telephones	2-606
MC145169	Serial-Input Dual PLL for 46/49 MHz Cordless Telephones	2-606
MC145170	PLL Frequency Synthesizer with Serial Interface (160 MHz)	2-615
MC145173	Dual Band PLL Frequency Synthesizer	2-631
MC145190	1.1 GHz PLL Frequency Synthesizer (30/130 MHz)	2-632
MC145191	1.1 GHz PLL Frequency Synthesizer	2-632
MC145192	Low Voltage 1.1 GHz PLL Frequency Synthesizer	2-651
MC145200	2.0 GHz PLL Frequency Synthesizer	2-670
MC145201	2.0 GHz PLL Frequency Synthesizer	2-670

REMOTE CONTROL FUNCTIONS

Device #	Function	Page #
MC14469	Addressable Asynchronous Receiver/Transmitter	2-194
MC14497	PCM Remote Control Transmitter	2-202
MC145026	Encoder	2-461
MC145027	Decoder	2-461
MC145028	Decoder	2-461

RF COMMUNICATIONS

Device #	Function	Page #
MC2831A	Low Power FM Transmitter System	2-32
MC2833	Low Power FM Transmitter System	2-35
MC3356	Wideband FSK Receiver	2-38
MC3357	Low Power FM IF	2-44
MC3359	High Gain Low Power FM IF	2-48
MC3361B	Low Power FM IF	2-54
MC3362	Low Power Dual Conversion FM Receiver	2-60
MC3363	Low Power Dual Conversion FM Receiver	2-65
MC3367	Low Voltage Single Conversion FM Receiver	2-72
MC3371	Low Power Narrowband FM IF	2-78
MC3372	Low Power Narrowband FM IF	2-78
MC13055	Wideband FSK Receiver	2-135
MC13135	Dual Conversion Narrowband FM Receiver	2-142
MC13136	Dual Conversion Narrowband FM Receiver	2-142
MC13155	Wideband FSK Receiver	2-154
MC13156	Wideband FM IF System	2-169
MC13175	UHF FM/AM Transmitter	2-170
MC13176	UHF FM/AM Transmitter	2-170
MRFIC2001	900 MHz Downconverter LNA/Mixer	MRFIC2001/D
MRFIC2002	900 MHz Transmit Mixer	MRFIC2002/D
MRFIC2003	900 MHz GaAs Antenna Switch	MRFIC2003/D
MRFIC2004	900 MHz Driver and Ramp	MRFIC2004/D
MRFIC2006	900 MHz Two Stage Power Amplifier	MRFIC2006/D

SPEAKERPHONES

Device #	Function	Page #
MC33218	Voice Switched Speakerphone with Microprocessor Interface	2-302
MC34018	Voice Switched Speakerphone Circuit	2-370
MC34118	Voice Switched Speakerphone Circuit	2-417

SUBSCRIBER LOOP INTERFACE CIRCUITS (SLICs)

Device #	Function	Page #
MC3419-1L	Subscriber Loop Interface Circuit	2-119
MC33120	Subscriber Loop Interface Circuit	2-232
MC33121	Low Voltage Subscriber Loop Interface Circuit	2-262

VOICE CODING

Device #	Function	Page #
MC3417	CVSD Modulator/Demodulator (3-Bit Algorithm)	2-101
MC3418	CVSD Modulator/Demodulator (4-Bit Algorithm)	2-101
MC3517	CVSD Modulator/Demodulator (3-Bit Algorithm)	2-101
MC3518	CVSD Modulator/Demodulator (4-Bit Algorithm)	2-101
MC33110	Low Voltage Compander	2-220
MC34115	CVSD Modulator/Demodulators	2-402
MC145402	Serial 13-Bit Linear Codec (A/D and D/A)	2-689
MC145480	5 V PCM Codec-Filter	2-822
MC145500	Codec-Filter (Mono-Circuit; 16-Pin)	2-854
MC145501	Codec-Filter (Mono-Circuit; 18-Pin)	2-854
MC145502	Codec-Filter (Mono-Circuit; 22-Pin)	2-854
MC145503	Codec-Filter (Mono-Circuit; 16-Pin)	2-854
MC145505	Codec-Filter (Mono-Circuit; 16-Pin)	2-854
MC145532	ADPCM Transcoder	2-875
MC145540	ADPCM Codec	2-890
MC145542	CT2 Speech and Framing IC	2-906
MC145554	PCM Codec-Filter (16-Pin)	2-907
MC145557	PCM Codec-Filter (16-Pin)	2-907
MC145564	PCM Codec-Filter (20-Pin)	2-907
MC145567	PCM Codec-Filter (20-Pin)	2-907

OTHER FUNCTIONS

Device #	Function	Page #
MJD243	4-A Silicon Power Transistor	2-947
MJD253	4-A Silicon Power Transistor	2-947
MJE270	NPN Power Transistor	2-951
MJE271	PNP Power Transistor	2-951
MPS6717	NPN One Watt Amplifier Transistors	2-953
4N35/36/37	Optoisolators	2-954

DISCONTINUED/NOT RECOMMENDED FOR NEW DESIGN

Device #	Function
MC14400	Single-Chip Codec-Filter (Mono-Circuit)
MC14401	Single-Chip Codec-Filter (Mono-Circuit)
MC14402	Single-Chip Codec-Filter (Mono-Circuit)
MC14403	Single-Chip Codec-Filter (Mono-Circuit)
MC14405	Single-Chip Codec-Filter (Mono-Circuit)
MC14408	Binary to Pulse Dialer
MC14409	Binary to Pulse Dialer
MC14410	2-of-8 Tone Encoder/Dialer
MC14411	Bit Rate Generator
MC14412	Universal Low Speed Modem (0–600 bps)
MC14413-1, -2	PCM Band-Pass/Low-Pass Filter
MC14414-1, -2	PCM Dual Low-Pass Filter
MC14416	Time Slot Assigner Circuit
MC14417	Time Slot Assigner Circuit
MC14418	Time Slot Assigner Circuit
MC14419	2-of-8 Keypad-to-Binary Encoder
MC142100	4 × 4 Crosspoint Switch with Control Memory
MC142103	Encoder
MC143403	Quad Line Driver
MC143404	Quad Line Driver
MC145030	Encoder/Decoder
MC145031	Encoder
MC145032	Decoder
MC145033	Encoder/Decoder
MC145034	Encoder
MC145035	Decoder
MC145100	4 × 4 Crosspoint Switch with Control Memory
MC145411	Bit Rate Generator
MC145414	Dual Tunable Low-Pass Sampled Filter
MC145415	Dual Tunable Linear Phase Low-Pass Sampled Data Filter
MC145418	80 kbps Digital Loop Transceiver (Master)
MC145419	80 kbps Digital Loop Transceiver (Slave)
MC145421	Universal Digital Loop Transceiver II (UDLT II)
MC145422	Universal Digital Loop Transceiver (UDLT)
MC145425	Universal Digital Loop Transceiver II (UDLT II)
MC145426	Universal Digital Loop Transceiver (UDLT)
MC145428	Data Set Interface
MC145429	Teleset Audio Interface Circuit (TAIC)
MC145432	2600 Hz Signaling Filter
MC145433	Tunable Notch/Band-Pass Filter
MC145439	Encoder/Decoder
MC145440	300 Baud Modem Filter (Bell 103)
MC145441	300 Baud Modem Filter (CCITT V.21)
MC145445	300 Baud Modem (Bell 103/CCITT V.21)
MC145450	1200 Baud Modem (Bell 202/CCITT V.23)
MC145601	Time Slot Interchange Circuit (TSIC)
MC145610	Pulse Tone Dialer with Last Number Redial
MC145611	PCM 8-Channel Conference Circuit

Technical Selection Guide

RF COMMUNICATIONS

AM and Wideband FM Transmitters

Device	V_{CC}	I_{CC}	Output Power	Max RF Input Freq.	Max Mod. Freq.	Data Rate (Baud)	Notes	Suffix/ Case	Page
MC13175	2–5 V	40 mA	8.0 dBm	500 MHz	5 MHz	10 M	AM/FM Transmitter; Single Frequency PLL, $f_{OUT} = 8 \times f_{REF}$	P/648 D/751B	2-170
MC13176	2–5 V	40 mA	8.0 dBm	1 GHz	5 MHz	10 M	AM/FM Transmitter; Single Frequency PLL, $f_{OUT} = 32 \times f_{REF}$	P/648 D/751B	2-170

Wideband Single Conversion Receivers

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	Input RF Freq.	IF	Mute	RSSI	Data Rate (Baud)	Notes	Suffix/ Case	Page
MC3356	3–9 V	25 mA	30 µV	200 MHz	10.7 MHz	Yes	Yes	50k	Includes squelch and data shaper	P/738 DW/751D	2-38
MC13156	2–7 V	3 mA	2 µV	500 MHz	21.4 MHz	No	Yes	1 M	CT-2 FM demodulator split IF	DW/751E	2-169

Wideband IFs

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	IF	Mute	RSSI	Data Rate (Baud)	Notes	Suffix/ Case	Page
MC13055	3–12 V	25 mA	20 µV	40 MHz	Yes	Yes	2 M	Wideband, includes data shaper	P/648 D/751B	2-135
MC13155	3–6 V	10 mA	100 µV	250 MHz	No	Yes	10 M	Video speed	D/751B	2-154

Narrowband FM Transmitters

Device	V_{CC}	I_{CC}	Output Power	Max RF Input Freq.	Max Mod. Freq.	Data Rate (Baud)	Notes	Suffix/ Case	Page
MC2831A	3–8 V	5.0 mA	–30 dBm	50 MHz	50 kHz	4.8k	FM Transmitter — Includes low battery checker, tone oscillator	P/648 D/751B	2-32
MC2833	3–8 V	10 mA	–30 dBm to +10 dBm	150 MHz	50 kHz	4.8k	FM Transmitter — Includes two frequency multiplier/amplifier transistors	P/648 D/751B	2-35

Narrowband Single Conversion Receivers

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	Input RF Freq.	IF	Mute	RSSI	Data Rate (Baud)	Notes	Suffix/ Case	Page
MC3357	4–8 V	5 mA	5 µV	45 MHz	455 kHz	Yes	No	> 4.8k	Ceramic Quad Detector/Resonator	P/648	2-44
MC3359	4–9 V	7 mA	2 µV	45 MHz	455 kHz	Yes	No	> 4.8k	Scan Output Option	P/707 DW/751D	2-48
MC3361B	2–8 V	6 mA	2 µV	60 MHz	455 kHz	Yes	No	> 4.8k	Lowest Cost Receiver	P/648 D/751B	2-54
MC3367	1–5 V	1 mA	1 µV	75 MHz	455 kHz	Yes	No	> 4.8k	1 Cell Operation	DW/751F	2-72
MC3371	2–8 V	6 mA	2 µV	60 MHz	455 kHz	Yes	No	> 4.8k	RSSI	P/648 D/751B	2-78
MC3372	2–8 V	6 mA	2 µV	60 MHz	455 kHz	Yes	No	> 4.8k	RSSI, Ceramic Quad Detector/Resonator	P/648 D/751B	2-78

RF COMMUNICATIONS (continued)

Narrowband Dual Conversion Receivers

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	Input RF Freq.	IF1	IF2	Mute	RSSI	Data Rate (Baud)	Notes	Suffix/ Case	Page
MC3362	2–7 V	3 mA	0.7 µV	180 MHz	10.7 MHz	455 kHz	No	Yes	> 4.8k	Includes buffered VCO output	DW/751E	2-60
MC3363	2–7 V	4 mA	0.4 µV	180 MHz	10.7 MHz	455 kHz	Yes	Yes	> 4.8k	Includes RF Preamp and Mute	DW/751F	2-65
MC13135	2–7 V	4 mA	1 µV	180 MHz	10.7 MHz	455 kHz	No	Yes	> 4.8k	Voltage buffered RSSI, LC Quad Detector	DW/751E	2-142
MC13136	2–7 V	4 mA	1 µV	180 MHz	10.7 MHz	455 kHz	No	Yes	> 4.8k	Voltage buffered RSSI, Ceramic Quad Detector	DW/751E	2-142

LOW-POWER OPERATIONAL AMPLIFIER

Device	SR V/µs (Typ)	GBW MHz (Typ)	V_{IO} mV (Max)	I_{IB} µA (Max)	I_D mA (Max /amp)	I_{SC} mA (Typ)	e_n nV/√Hz (Typ)	Temp Range °C	Notes	Suffix/ Case	Page
MC33102 (Awake) (Sleep)	1.0 0.1	4.0 0.3	2.0 2.0	500 nA 50 nA		6.0 6.0	50 25	−40 to 85	Dual	P/626 D/751	2-208
MC33178/9	2.0	5.0	3.0	0.5	0.7	80	7.5	−40 to 85	Dual/Quad	P/626	2-292

REMOTE CONTROL

Function	Number of Address Lines	Maximum Number of Address Codes	Number of Data Bits	Operation	Device	Suffix/Case	Page
Encoder	Depends on Decoder(1)	Depends on Decoder(1)	Depends on Decoder(1)	Simplex	MC145026	P/648 D/751B	2-461
Decoder	5	243	4	Simplex	MC145027	P/648 DW/751G	
	9	19,683	0	Simplex	MC145028		

(1)See MC145027, MC145028

SWITCH MODE CONTROLLER

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Case	Page
1000 (Totem Pole MOSFET Driver Output)	4.2 to 12	Current	1.25 ± 2.0%	300	MC34129	0 to + 70	P/646 D/751A	2-446
					MC33129	−40 to + 85	P/646 D/751A	2-446

EIA-232/562/V.28 DRIVERS/RECEIVERS

Drivers	Receivers	Power Supplies (V)	Features	Device	Suffix/ Package	Page
—	4	+5.0	EIA-232/EIA-562 V.28	MC14C89B MC14C89AB	P/646, D/751A	2-9
—	4	+5.0	EIA-232/V.28	MC1489 MC1489A	P/646, D/751A	2-20
4	—	±7.0 to ±12	EIA-232/EIA-562 V.28	MC14C88B	P/646, D/751A	2-3
4	—	±9.0 to ±12	EIA-232/V.28	MC1488	P/646, D/751A	2-14
3	5	±5.0 to ±12	EIA-232/V.28	MC145403	P/738 DW/751D	2-700
4	4			MC145404		
5	3			MC145405		
3	3			MC145406	P/648, DW/751G	2-706
3	3	+5.0	EIA-232/V.28; Charge Pump	MC145407	P/738, DW/751D	2-714
5	5	±5.0 to ±12	EIA-232/V.28	MC145408	P/724, DW/751E	2-706
2	3	+3.3 to +5.0	EIA-232/V.28; Onboard ring monitor circuit	MC145583	DW/751F	2-926
2	3	+5.0	EIA-232/V.28; Charge Pump, Power Down	MC145705	P/738 DW/751D	2-929
3	2			MC145706		
3	3			MC145707	P/724, DW/751E	

EIA-422 DRIVERS/RECEIVERS

Drivers	Receivers	Power Supplies (V)	Features	Device	Suffix/ Package	Page
4	—	+5.0	Pin compatible with AM26LS31. Enable and disable common to all four drivers. Typical ESD protection of 2 KV.	MC26C31	P/648, D/751B	2-26
—	4	+5.0	Pin compatible with AM26LS32. Enable and disable common to all four receivers. Typical ESD protection of 2 KV.	MC26C32	P/648, D/751B	2-29
—	4	+5.0	Pin compatible with MC3486. Typical ESD protection of 2 KV.	MC34C86	P/648, D/751B	2-95
4	—	+5.0	Pin compatible with MC3487. Typical ESD protection of 2 KV.	MC34C87	P/648, D/751B	2-98

PHASE-LOCKED LOOP FREQUENCY SYNTHESIZERS

Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Standby	Interface	Device	Suffix/ Case	Page
4 @ 5 V	4.5 to 12	6 @ 5 V	Single-ended three-state	No	Parallel	MC145106	P/707 DW/751D FN/775	2-495
15 @ 5 V	3.0 to 9.0	—	Two single-ended three-state		Serial	MC145149	P/738 DW/751D	2-524
		7.5 @ 5 V	Analog			MC145159-1	P/738 DW/751D FN/775	2-565
20 @ 5 V	3.0 to 9.0	7.5 @ 5 V	Single-ended three-state, double-ended	No	4-Bit	MC145145-2	P/707 DW/751D	2-502
						MC145146-2	P/738 DW/751D	2-513
					Parallel	MC145151-2	P/710 DW/751F FN/776	2-535
			Double-ended			MC145152-2	P/710 DW/751F FN/776	2-538
			Single-ended three-state, double-ended		Serial	MC145155-2	P/707 DW/751D FN/775	2-542
						MC145156-2	P/707 DW/751D FN/775	2-546
						MC145157-2	P/648 DW/751G FN/775	2-550
						MC145158-2	P/648 DW/751G FN/775	2-553
60 @ 3 V	2.5 to 5.5	3.0 @ 3 V	Two single-ended three-state	Yes	Parallel	MC145160	P/707 DW/751D	2-574
					Serial	MC145161	P/648 DW/751G	2-581
						MC145162	P/648 DW/751G	2-587
					Parallel	MC145166	P/648 DW/751G	2-574
					Serial	MC145167	P/648 DW/751G	2-574
					Parallel	MC145168		2-606
					Serial	MC145169		2-606
100 @ 3 V 160 @ 5 V	2.5 to 6.0	3.0 @ 3 V 7.0 @ 5 V	Single-ended three-state, double-ended	No	Serial	MC145170	P/648 D/751B	2-615
30/130 @ 5 V	4.5 to 5.5	25 @ 5 V	Single-ended three-state, Current source/sink	Yes	Serial	MC145173	DW/751E	2-631
1100 @ 5 V	4.5 to 5.5	7.0 @ 5 V	Current source/sink, double-ended	Yes	Serial	MC145190	DW/751J	2-632
						MC145191	DW/751J	2-632
1100 @ 3 V	2.7 to 5.0	6.0 @ 2.7 V				MC145192	DW/751J	2-651
2000 @ 5 V	4.5 to 5.5	12 @ 5 V				MC145200	DW/751J	2-670
						MC145201	DW/751J	2-670

TELECOM CIRCUITS

Audio Amplifiers

Function	Features	Device	Suffix/Case	Page
Low Voltage Audio Amp	400 mW, 8.0 to 100 Ω, 2.0 to 16 V, differential outputs, chip-disable input pin.	MC34119	P/626 D/751	2-437

Complete Telephone Circuit

Function	Features	Device	Suffix/Case	Page
POTS circuit + MPU Dialing	Speech network, tone ringer, DC loop current interface, DTMF dialer with serial port control	MC34010	P/711 FN/777	2-313

Companders

Function	Features	Device	Suffix/Case	Page
Basic Compander	2.7 to 7 V, no precision externals, 80 dB range, −40 to +85°C, independent compressor and expander	MC33110	P/646 D/751A	2-220

Dialers

Function	Features	Device	Suffix/Case	Page
Pulse/Tone Repertory Dialer	10 number memory including LNR. Uses color burst XTAL. 3 × 4 or 4 × 4 keyboard compatibility. 32/68 make break ratio (MC145512 ONLY)	MC145412	P/707	2-721
		MC145413		
		MC145512		
Tone/Pulse Dialer	10 number memory including LNR plus 3 emergency numbers. Dial mode output pin. Uses color burst XTAL.	MC145416	P/738	2-730
Dual Tone Multiple Frequency Receiver	Pin compatible with SSI204. Single +5 V supply. Detects all 16 tones. Provides guard time controls for improved speech immunity. Output in 4-bit hexadecimal code.	MC145436	P/646 DW/751G	2-742

Integrated Services Digital Network (ISDN)

Function	Features	Device	Suffix/Case	Page
Line Cards, NT1s, Pair Gain, ISDN Compatible Bridge Routers, ISDN Terminals	ANSI T1.601 compliant, pin selectable LT or NT operation, industry standard IDL interface, slave-slave timing mode, control and status provided through four-wire serial control port.	MC145472	FE/847B	2-775
	500 mW die shrink version of the MC145472	MC1454LC72	FE/847B FU847	2-775
Network Termination (NT1), PC Based and Standalone ISDN Terminal Adaptors, ISDN Telephone, ISDN Video Phones	Conforms to CCITT I.430 and ANSI T1.605, pin selectable NT and TE modes, Interchip Digital Link (IDL), serial control port (SCP), full multiframing capabilities, NT1 star mode, S/T and IDL loopbacks.	MC145474	L/736B	2-801
		MC145475	DW/751D	2-801
Line Cards, NT1s, Pair Gain, ISDN Compatible Bridge Routers, ISDN Terminals	Enhanced version of the MC14LC5472, low power; 300 mW, ANSI T1.601 compliant, pin selectable LT or NT operation, IDL and GCI interfaces, timeslot assigner, parallel or serial control ports	MC145572	FN/777 FE/824A	2-922
Network Termination (NT1), PC Based and Standalone ISDN Terminal Adaptors, ISDN Telephone, ISDN Video Phones, PBX Applications, Combination Network Termination/Terminal Adaptor (NT1/TA)	Conforms to CCITT I.430 and ANSI T1.605, pin selectable NT and TE modes, Interchip Digital Link (IDL), serial control port (SCP), full multiframing capabilities, NT1 star mode, S/T and IDL loopbacks, backwards software compatible with the MC145474/75, low power consumption, general circuit interface (GCI), timeslot assigner, NT terminal mode, slave/slave mode.	MC145574	Not Available until 2Q94	2-924

TELECOM CIRCUITS (continued)

Modems

Function	Features	Device	Suffix/Case	Page
Single Chip 300 Baud Modem	CCITT V.21 compatible. Capable of driving –9 dBm into 600 Ω. Internal mid-supply generator. Uses color burst XTAL. Adjustable transmit level and CD delay timing.	MC145442	P/738 DW/751D	2-748
Single Chip 300 Baud Modem	Bell 103 compatible. Capable of driving –9 dBm into 600 Ω. Internal mid-supply generator. Uses color burst XTAL. Adjustable transmit level and CD delay timing.	MC145443	P/738 DW/751D	2-748
Single Chip 300 Baud Modem	CCITT V.21 compatible. Capable of driving 0 dBm into 600 Ω. Uses color burst XTAL. Adjustable transmit level and CD delay timing. On-chip DTMF generator and imprecise call progress detection. 3-wire serial interface.	MC145444	H/804 DW/751D	2-756
Adjust Box, Telephones, Fax Machines, Answering Machines, Key Systems, Transaction Terminals	Low-power mode, 3.5 V to 6.5 V operating range, high-performance Bell 202/V.23 demodulator, on chip ring detector, pin selectable oscillator frequencies: 3.68 MHz, 3.58 MHz, or 455 kHz	MC145447	P/648 DW/751G	2-765

Subscriber Loop Interface Circuits (SLICs)

Function	Features	Device	Suffix/Case	Page
PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 100 mA	MC3419-1L	L/726	2-119
Central Office, Remote Terminals, PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 50 mA, 58 dB Longitudinal Balance, –42 to –58 V	MC33120	P/738 FN/776	2-232
Central Office, Remote Terminals, PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 50 mA, 58 dB Longitudinal Balance, –21.6 to –42 V	MC33121	P/738 FN/776	2-262

Speakerphone Circuits

Function	Features	Device	Suffix/Case	Page
Complete Speakerphone with MPU Interface	All level detection, attenuators, and switching controls, mike amp, MPU interface for: volume control, mode selection, mike mute.	MC33218	P/724 DW/751E	2-302
Complete Speakerphone with Speaker Amplifier	All level detection (2 pt.), attenuators, and switching controls, mike and speaker amp	MC34018	P/710 DW/751F	2-370
Complete Speakerphone with Hybrid, Filter	All level detection (4 pt.), attenuators, and switching controls, mike amp with mute, hybrid, and filter	MC34118	P/710 DW/751F	2-417

Speech Networks

Function	Features	Device	Suffix/Case	Page
Basic Phone Line Interface	Loop current interface, speech network, line length compensation, speech/dialing modes, Bell system compliant.	MC34014	P/707 D/751D	2-345
Basic Phone Line Interface	Loop current interface, speech network, line length compensation, speech/dialing modes, Bell system and foreign countries.	MC34114	P/707 D/751D	2-384
European Speech Network	Loop current interface, speech network, line length compensation, speech/dialing modes, programmable masks for French, UK, low voltages, and PABX systems.	TCA 3388	DP/738 FP/751	2-943

Switching Regulator

Function	Features	Device	Suffix/Case	Page
Current Mode Regulator	For phone line power applications, soft start, current limiting, 2% accuracy	MC34129	P/646 D/751A	2-446

TELECOM CIRCUITS (continued)

Tone Ringers

Function	Features	Device	Suffix/Case	Page
Adjustable Tone Ringer	Single ended output, meets FCC requirements, adjustable REN, different warble rates	MC34012 -1, -2, -3	P/626 D/751	2-337
Adjustable Tone Ringer	Differential output, meets FCC requirements, adjustable REN, different warble rates	MC34017 -1, -2, -3	P/626 D/751	2-362
Adjustable Tone Ringer	Differential output, meets FCC requirements, adjustable REN, different warble rates	MC34217	P/626 D/751	2-362
Ring Signal Converter	Switching regulator to convert ringing voltage to regulated DC output. Provides ring detect output	TCA 3385	P/626 FP/751	2-935

Voice Coding

Function	Features	Device	Suffix/Case	Page
ISDN, PABX, DSP Interface, Cordless Telephone, Radio	5 V single power supply PCM codec-filter. Pin selectable Mu-Law or A-Law companding with serial PCM interface	MC145480	P/738 DW/751D	2-822
ISDN, Telephone Central Office, PABX, DSP Interface	PCM codec-filter with pin selectable Mu-Law or A-Law companding and serial PCM interface	MC145500	L/630	2-954
		MC145501	L/726	
		MC145502	L/736 P/708 FN/776	
		MC145503	L/620 P/648 DW/751G	
		MC145505		
Digital Cordless Telephone Base Station, T1 Multiplexer	5 V ADPCM transcoder that is CCITT G.721, G.723, and G.726 compliant for 24 and 32 kpbs with proprietary 16 kpbs mode. Mu-Law and A-Law compatible.	MC145532	L/620 DW/751G	2-875
Digital Cordless Telephone/ Base Station, Voice Storage	PCM codec-filter with ADPCM transcoder that operates at 2.7 V. CCITT G.721, G.723, and G.726 compliant at 16, 24, and 32 kpbs. Includes high-gain mic amp, receiver power driver, auxiliary driver, sidetone and gain controls.	MC145540	P/710 DW/751F	2-890
CT2 Digital Cordless Telephone and Base Station	2.7 V ADPCM codec with CT2 burst-mode control logic. This device is a complete voice coder with framing and system control features for CT2 applications.	MC145542	TBD	2-906
ISDN, Telephone Central Office, PABX, DSP Interface	Dual power supply PCM codec-filter. Industry standard pinout with serial PCM interface.	MC145554	P/648 L/620 DW/751G	2-907
		MC155557		
		MC145564	P/738 L/732 DW/751D	
		MC145567		

Voice Encoders/Decoders

Function	Features	Device	Suffix/Case	Page
Continuously Variable Slope Delta (CVSD) Modulator/Demodulator	Telephone quality voice encoding/decoding, variable clock rate, 3-bit coding, for secure communications, voice storage/ retrieval, answering machines, 0–70°C	MC34115	P/738 DW/751G	2-402
	Same as above, except 4-bit coding	MC3418	P/738 DW/751G	2-101
	Same as MC34115, but −55 to +125°C temp. range	MC3517	L/620	2-101
	Same as MC3418, but −55 to +125°C temp. range	MC3518	L/620	2-101

Data Sheets 2

2

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC14C88B

Advance Information

Quad Low Power Line Driver

The MC14C88B is a low power monolithic quad line driver, using BiMOS technology, which conforms to EIA-232-D, EIA-562, and CCITT V.28. The inputs feature TTL and CMOS compatibility with minimal loading. The outputs feature internally controlled slew rate limiting, eliminating the need for external capacitors. Power off output impedance exceeds 300 Ω, and current limiting protects the outputs in the event of short circuits.

Power supply current is less than 160 μA over the supply voltage range of ±4.5 to ±15 V. EIA-232-D performance is guaranteed with a minimum supply voltage of ±6.5 V.

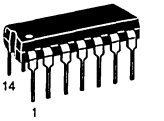
The MC14C88B is pin compatible with the MC1488, SN75188, SN75C188, DS1488, and DS14C88. This device is available in 14 pin plastic DIP, and surface mount packaging.

Features:

- BiMOS Technology for Low Power Operation (<5.0 mW)
- Meets Requirements of EIA-232-D, EIA-562, and CCITT V.28
- Quiescent Current Less Than 160 μA
- TTL/CMOS Compatible Inputs
- Minimum 300 Ω Output Impedance when Powered Off
- Supply Voltage Range: ±4.5 to ±15 V
- Pin Equivalent to MC1488
- Current Limited Output: 10 mA Minimum
- Operating Ambient Temperature: –40° to 85°C

QUAD LOW POWER LINE DRIVER

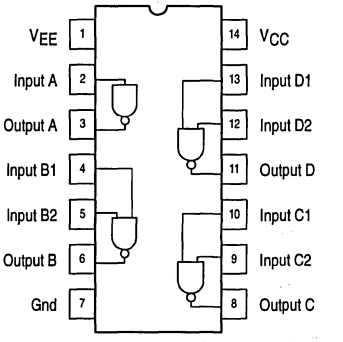
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646

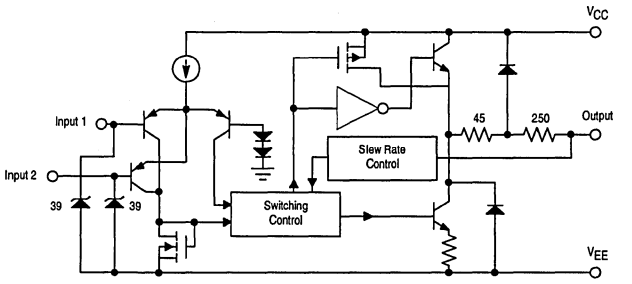
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram
(Each Driver)



ORDERING INFORMATION

Device	Temperature Range	Package
MC14C88BP	–40° to +85°C	Plastic DIP
MC14C88BD		SO-14

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage V_{CC}(max) V_{EE}(min) ($V_{CC} - V_{EE}$)max	 V_{CC} V_{EE} $V_{CC} - V_{EE}$	 +17 –17 34	Vdc
Input Voltage (All Inputs)	V_{in}	V_{EE}–0.3, V_{EE}+39	Vdc
Applied Output Voltage, when V_{CC}=V_{EE}≠0 V Applied Output Voltage, when V_{CC}=V_{EE}=0 V	V_X	V_{EE}–6.0 V, V_{CC}+6.0 V ±15	Vdc
Output Current	I_O	Self Limiting	mA
Operating Junction Temperature	T_J	–65, +150	°C

Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC} V_{EE}	+4.5 –15	— —	+15 –4.5	Vdc
Input Voltage (All Inputs)	V_{in}	0	—	V_{CC}	Vdc
Applied Output Voltage (V_{CC}=V_{EE}=0 V)	V_O	–2.0	0	+2.0	Vdc
Output DC Load	R_L	3.0	—	7.0	kΩ
Operating Ambient Temperature Range	T_A	–40	—	+85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +85°C, unless otherwise noted.)*

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (I_{out} = 0, see Figure 2) I_{CC} @ 4.75 V ≤ V_{CC}, –V_{EE} ≤ 15 V					µA
Outputs High	I_{CC} (OH)	—	—	160	
Outputs Low	I_{CC} (OL)	—	—	160	
I_{EE}					
Outputs High	I_{EE} (OH)	–160	—	—	
Outputs Low	I_{EE} (OL)	–160	—	—	
Output Voltage – High, V_{in} ≤ 0.8 V (R_L = 3.0 kΩ, see Figure 3)	V_{OH}				Vdc
V_{CC} = +4.75 V, V_{EE} = –4.75 V		3.7	3.8	—	
V_{CC} = +5.0 V, V_{EE} = –5.0 V		4.0	4.3	—	
V_{CC} = +6.5 V, V_{EE} = –6.5 V		5.0	6.1	—	
V_{CC} = +12 V, V_{EE} = –12 V		10	10.5	—	
V_{CC} = +13.2 V, V_{EE} = –13.2 V (R_L = ∞)		—	13.2	13.2	
Output Voltage – Low, V_{in} ≥ 2.0 V	V_{OL}				
V_{CC} = +4.75 V, V_{EE} = –4.75 V		—	–3.8	–3.7	
V_{CC} = +5.0 V, V_{EE} = –5.0 V		—	–4.2	–4.0	
V_{CC} = +6.5 V, V_{EE} = –6.5 V		—	–6.0	–5.0	
V_{CC} = +12 V, V_{EE} = –12 V		—	–10.5	–10	
V_{CC} = +13.2 V, V_{EE} = –13.2 V (R_L = ∞)		–13.2	–13.2	—	
Output Short Circuit Current** (see Figure 4) (V_{CC} = |V_{EE}| = 15 V)	I_{OS}				mA
Normally High Output, shorted to ground		–35	—	–10	
Normally Low Output, shorted to ground		+10	—	+35	
Output Source Resistance (V_{CC} = V_{EE} = 0 V, –2.0 V ≤ V_{out} ≤ +2.0 V)	R_O	300	—	—	Ω
Input Voltage					
Low Level	V_{IL}	0	—	0.8	Vdc
High Level	V_{IH}	2.0	—	V_{CC}	

* Typicals reflect performance @ T_A = 25°C
** Only one output shorted at a time, for not more than 1 second.

ELECTRICAL CHARACTERISTICS CONTINUED ($-40°C \le T_A \le +85°C$, unless otherwise noted.)*

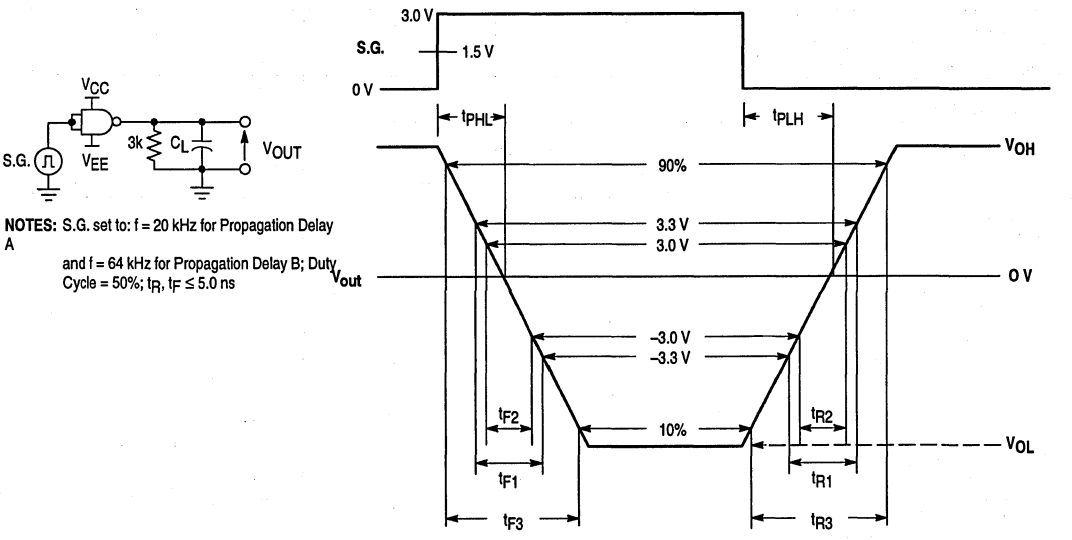
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current	I_{in}				μA
V_{in} = 0 V, V_{CC} = $\|V_{EE}\|$ = 4.75 V		–10	–0.1	0	
V_{in} = 0 V, V_{CC} = $\|V_{EE}\|$ = 15 V		–10	–0.1	0	
V_{in} = 4.5 V, V_{CC} = $\|V_{EE}\|$ = 4.75 V		0	+0.1	+10	
V_{in} = 4.5 V, V_{CC} = $\|V_{EE}\|$ = 15 V		0	+0.1	+10	

TIMING CHARACTERISTICS ($-40°C \le T_A \le +85°C$, unless otherwise noted.)*

Characteristic	Symbol	Min	Typ	Max	Unit
Output Rise Time					μs
V_{CC} = 4.75 V, V_{EE} = –4.75 V					
–3.3 V ≤ V_O ≤ 3.3 V	t_{R1}				
C_L = 15 pF		0.22	0.66	2.1	
C_L = 1000 pF		0.22	1.52	2.1	
–3.0 V ≤ V_O ≤ 3.0 V	t_{R2}				
C_L = 15 pF		0.20	0.51	1.5	
C_L = 1000 pF		0.20	1.16	1.5	
V_{CC} = 12.0 V, V_{EE} = –12.0 V					
–3.0 V ≤ V_O ≤ 3.0 V					
C_L = 15 pF		0.20	0.62	1.5	
C_L = 2500 pF		0.20	0.82	1.5	
10% ≤ V_O ≤ 90%	t_{R3}				
C_L = 15 pF		0.53	1.41	3.2	
Output Fall Time					μs
V_{CC} = 4.75 V, V_{EE} = –4.75 V					
3.3 V ≤ V_O ≤ –3.3 V	t_{F1}				
C_L = 15 pF		0.22	0.93	2.1	
C_L = 1000 pF		0.22	1.28	2.1	
3.0 V ≤ V_O ≤ –3.0 V	t_{F2}				
C_L = 15 pF		0.20	0.72	1.5	
C_L = 1000 pF		0.20	1.01	1.5	
V_{CC} = 12.0 V, V_{EE} = –12.0 V					
3.0 V ≤ V_O ≤ –3.0 V					
C_L = 15 pF		0.20	0.70	1.5	
C_L = 2500 pF		0.20	0.94	1.5	
90% ≤ V_O ≤ 10%	t_{F3}				
C_L = 15 pF		0.53	1.71	3.2	
Output Slew Rate, 3.0 kΩ < R_L < 7.0 kΩ, 15 pF < C_L < 2500 pF	S_R	4.0	—	30	V/μs
Propagation Delay A (C_L = 15 pF, see Figure 1)					μs
V_{CC} = 12.0 V, V_{EE} = –12.0 V					
Input to Output – Low to High	t_{PLH}	—	0.9	3.0	
Input to Output – High to Low	t_{PHL}	—	2.3	3.5	
Propagation Delay B (C_L = 15 pF, see Figure 1)					
V_{CC} = 4.75 V, V_{EE} = –4.75 V					
Input to Output – Low to High	t_{PLH}	—	0.4	2.0	
Input to Output – High to Low	t_{PHL}	—	1.5	2.5	

* Typicals reflect performance @ T_A = 25°C

Figure 1. Timing Diagram



STANDARDS COMPLIANCE

The MC14C88 is designed to comply with EIA-232-D (formerly RS-232), the newer EIA-562 (which is a higher speed version of the EIA-232), and CCITT's V.28. EIA-562 was written around modern integrated circuit technology, whereas EIA-232 retains many of the specs written around the electro-mechanical circuitry in use at the time of its creation. Yet the user will find enough similarities to allow a certain amount of compatibility among equipment built to the two standards. Following is a summary of the key specifications relating to the systems and the drivers.

Parameter	EIA-232-D	EIA-562
Maximum Data Rate	20 kbaud	38.4 kbaud Asynchronous 64 kbaud Synchronous
Maximum Cable Length	50 feet	Based on cable capacitance/data rate
Maximum Slew Rate	≤ 30 V/µs anywhere on the waveform	≤ 30 V/µs anywhere on the waveform ≥ 4.0 V/µs between +3.0 and –3.0 V
Transition Region	–3.0 to +3.0 V	–3.3 to +3.3 V
Transition Time	For UI ≥ 25 ms, t_R ≤ 1.0 ms For 25 ms > UI > 125 µs, t_R ≤ 4% UI For UI < 125 µs, t_R ≤ 5.0 µs	For UI ≥ 50 µs, 220 ns < t_R ≤ 3.1 µs For UI < 50 µs, 220 ns < t_R ≤ 2.1 µs (within the transition region)
MARK (one, off)	More negative than –3.0 V	More negative than –3.3 V
Space (zero, on)	More positive than +3.0 V	More positive than +3.3 V
Short Circuit Proof ?	Yes, to any system voltage	Yes, to ground
Short Circuit Current	≤ 500 mA to any system voltage	≤ 60 mA to ground
Open Circuit Voltage	$\|V_{OC}\|$ ≤ 25 V	$\|V_{OC}\|$ < 13.2 V
Loaded Output Voltage	5.0 V ≤ $\|V_O\|$ ≤ 15 V for loads between 3.0 kΩ and 7.0 kΩ	$\|V_O\|$ ≥ 3.7 V for a load of 3.0 kΩ
Power Off Input Source Impedance	≥ 300 Ω for $\|V_O\|$ ≤ 2.0 V	≥ 300 Ω for $\|V_O\|$ ≤ 2.0 V

NOTE: UI = Unit Interval, or bit time.
V.28 standard has the same specifications as EIA-232, with the exception of transition time which is listed as "less than 1.0 ms, or 3% of the UI, whichever is less".

Figure 2. Typical Supply Current versus Supply Voltage

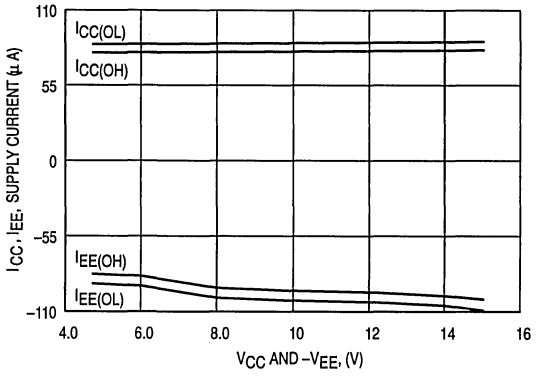


Figure 3. Typical Output Voltage versus Supply Voltage

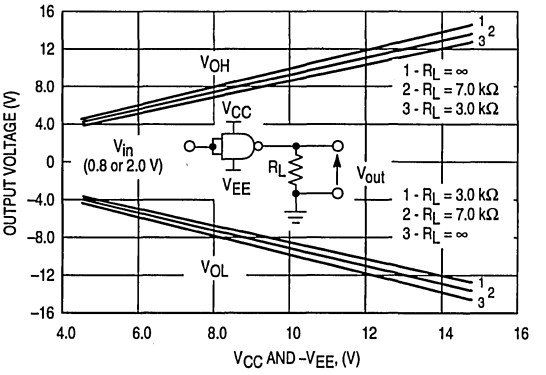


Figure 4. Typical Short Circuit Current versus Supply Voltage

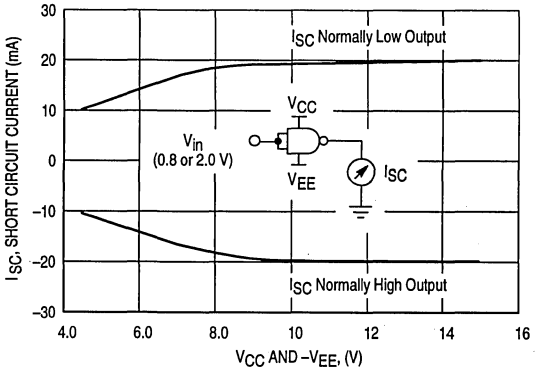
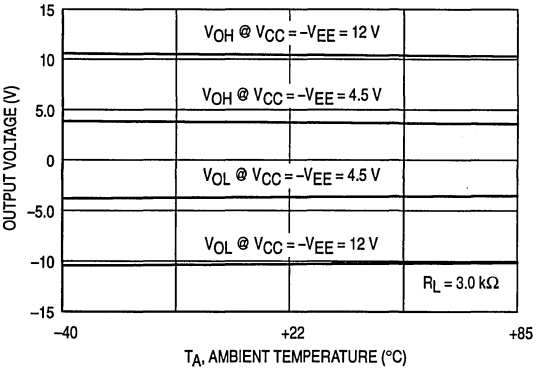


Figure 5. Typical Output Voltage versus Temperature



APPLICATIONS INFORMATION

Description

The MC14C88 was designed to be a direct replacement for the MC1488 in that it meets all EIA-232 specifications. However, use is extended as the MC14C88 also meets the faster EIA-562 and CCITT V.28 specifications. Slew rate limited outputs conform to the mentioned specifications and eliminate the need for external output capacitors. Low power consumption is made possible by BiMOS technology. Power supply current is limited to less than 160 μA, plus load currents over the supply voltage range of ±4.5 V to ±15 V (see Figure 2).

Outputs

The output low or high voltage depends on the state of the inputs, the load current, and the supply voltage (see Table 1 and Figure 3). The graphs apply to each driver regardless of how many other drivers within the package are supplying load current.

Table 1. Function Tables

Driver 1

Input A	Output A
H	L
L	H

Drivers 2 through 4

Input *1	Input *2	Output*
H	H	L
L	X	H
X	L	H

H = High level, L = Low level, X = Don't care.

Driver Inputs

The driver inputs determine the state of the outputs in accordance with Table 1. The nominal threshold voltage for the inputs is 1.4 Vdc, and for proper operation, the input voltages should be restricted to the range Gnd to V_{CC}. Should the input voltage drop below V_{EE} by more than 0.3 V or rise above V_{EE} by more than 39 V, excessive currents will flow at the input pin. Open input pins are equivalent to logic high, but good design practices dictate that inputs should never be left open.

Operating Temperature Range

The ambient operating temperature range is listed as –40° to +85°C and meets EIA-232-D, EIA-562 and CCITT V.28 specifications over this temperature range. The maximum ambient temperature is listed as +85°C. However, a lower ambient may be required depending on system use, i.e. specifically how many drivers within a package are used, and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

where: $R_{\theta JA}$ = the package thermal resistance (typically, 100°C/W for the DIP package, 125°C/W for the SOIC package);
T_{Jmax} = the maximum operating junction temperature (150°C); and
T_A = the ambient temperature.

$$P_D = \{ [(V_{CC} - V_{OH}) \bullet |I_{OH}|] \text{ or } [(V_{OL} - V_{EE}) \bullet |I_{OL}|] \}_{\text{each driver}} + (V_{CC} \bullet I_{CC}) + (V_{EE} \bullet I_{EE})$$

where: V_{CC} and V_{EE} are the positive and negative supply voltages;
V_{OH} and V_{OL} are measured or estimated from Figure 3;
I_{CC} and I_{EE} are the quiescent supply currents measured or estimated from Figure 2.

As indicated, the first term (in brackets) must be calculated and summed for each of the four drivers, while the last terms are common to the entire package.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC14C89B
MC14C89AB

Advance Information

Quad Low Power Line Receiver

QUAD LOW POWER LINE RECEIVER

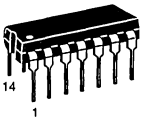
The MC14C89B and MC14C89AB are low power monolithic quad line receivers, using bipolar technology, which conform to the EIA-232-E, EIA-562 and CCITT V.28 Recommendations. The outputs feature LSTTL and CMOS compatibility for easy interface to +5.0 V digital systems. Internal time-domain filtering eliminates the need for external filter capacitors in most cases.

The MC14C89B has an input hysteresis of 0.35 V, while the MC14C89AB hysteresis is 0.95 V. The response control pins allow adjustment of the threshold level if desired. Additionally, an external capacitor may be added for additional noise filtering.

The MC14C89B and MC14C89AB are each available in a 14 pin dual-in-line plastic DIP and SOIC package.

Features:

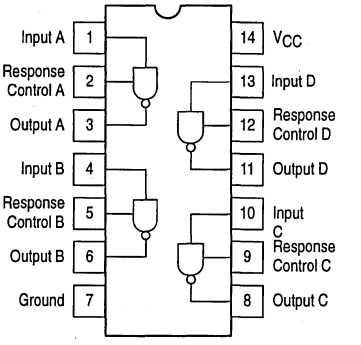
- Low Power Consumption
- Meets EIA-232-E, EIA-562, and CCITT V.28 Recommendations
- TTL/CMOS Compatible Outputs
- Standard Power Supply: + 5.0 V ± 10%
- Pin Equivalent to MC1489, MC1489A, TI's SN75C189/A, SN75189/A and National Semiconductor's DS14C89/A
- External Filtering Not Required in Most Cases
- Threshold Level Externally Adjustable
- Hysteresis: 0.35 V for MC14C89B, 0.95 V for MC14C89AB
- Available in Plastic DIP, and Surface Mount Packaging
- Operating Ambient Temperature: -40° to +85°C



P SUFFIX
PLASTIC PACKAGE
CASE 646

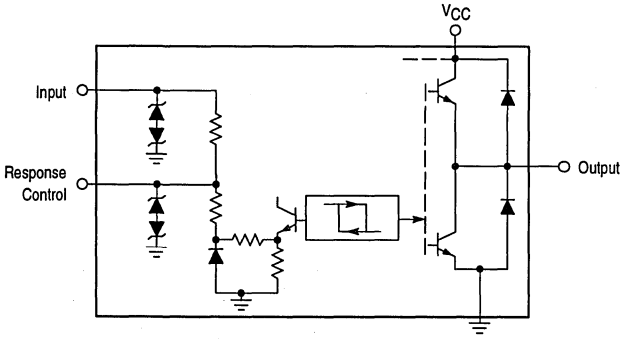
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram
(Each Receiver)



ORDERING INFORMATION

Device	Temperature Range	Package
MC14C89BP	–40° to +85°C	Plastic DIP
MC14C89BD		SO-14
MC14C89ABP		Plastic DIP
MC14C89ABD		SO-14

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage $V_{CC(max)}$ $V_{CC(min)}$	V_{CC}	 +7.0 −0.5	Vdc
Input Voltage	V_{in}	±30	Vdc
Output Load Current	I_O	Self-Limiting	—
Junction Temperature	T_J	−65, +150	°C

Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input Voltage	V_{in}	−25	—	25	Vdc
Output Current Capability	I_O	−7.5	—	6.0	mA
Operating Ambient Temperature	T_A	−40	—	85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS ($-40°C \le T_A \le 85°C$, unless otherwise noted.)*

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current ($I_{out} = 0$) I_{CC} @ $+4.5\ V \le V_{CC} \le +5.5\ V$	I_{CC}	 —	 330	 700	µA
Output Voltage — High, $V_{in} \le 0.4$ V (See Figures 2 and 3)	V_{OH}				Vdc
$I_{out} = -20$ µA $V_{CC} = 4.5$ V		3.5	3.8	—	
$V_{CC} = 5.5$ V		3.5	4.8	—	
$I_{out} = -3.2$ mA $V_{CC} = 4.5$ V		2.5	3.7	—	
$V_{CC} = 5.5$ V		2.5	4.7	—	
Output Voltage — Low, $V_{in} \ge 2.4$ V	V_{OL}				
$I_{out} = 3.2$ mA $V_{CC} = 4.5$ V		—	0.1	0.4	
$V_{CC} = 5.5$ V		—	0.1	0.4	
Output Short Circuit Current** ($V_{CC} = 5.5$ V, see Figure 4)	I_{OS}				mA
Normally High Output shorted to ground		−35	−13.9	—	
Normally Low Output shorted to V_{CC}		—	+10.3	35	
Input Threshold Voltage ($V_{CC} = 5.0$ V)					
(MC14C89AB, see Figure 5) Low Level	V_{IL}	0.75	0.95	1.25	Vdc
High Level	V_{IH}	1.6	1.90	2.25	
(MC14C89B, see Figure 6) Low Level	V_{IL}	0.75	0.95	1.25	
High Level	V_{IH}	1.0	1.3	1.5	
Input Impedance ($+4.5\ V < V_{CC} < +5.5\ V$ $-25\ V < V_{in} < +25\ V$)		3.0	5.5	7.0	kΩ

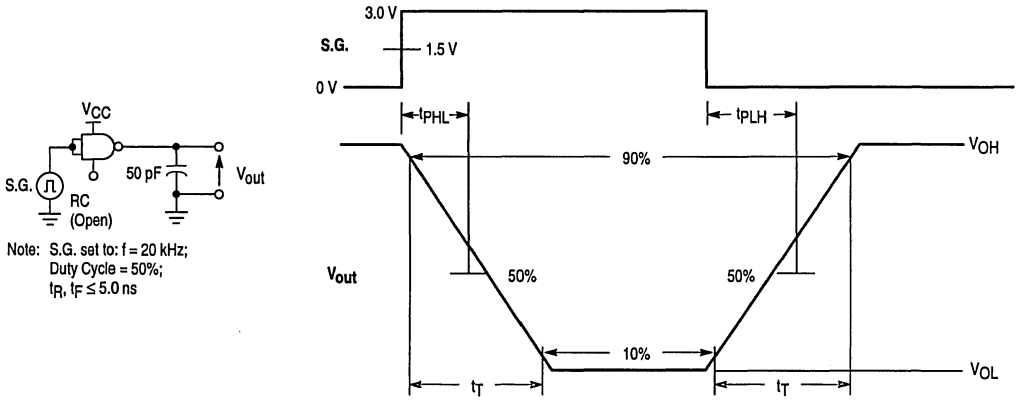
* Typicals reflect performance @ $T_A = 25°C$

** Only one output shorted at a time, for not more than 1.0 seconds.

TIMING CHARACTERISTICS ($T_A = +25°C$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Transition Time (10% to 90%) $4.5\ V \le V_{CC} \le 5.5\ V$	t_T	 —	 0.08	 0.30	µs
Propagation Delay Time $4.5\ V \le V_{CC} \le 5.5\ V$					
Output Low-to-High	t_{PLH}	—	3.35	6.0	µs
Output High-to-Low	t_{PHL}	—	2.55	6.0	
Input Noise Rejection (see Figure 9)		1.0	1.5	—	µs

Figure 1. Timing Diagram



STANDARDS COMPLIANCE

The MC14C89B and MC14C89AB are designed to comply with EIA-232-E (formerly RS-232), the newer EIA-562 (which is a higher speed version of the EIA-232), and CCITT V.28 Recommendations. EIA-562 was written around modern integrated circuit technology, whereas EIA-232 retains many of the specifications written around the electro-mechanical circuitry in use at the time of its creation. Yet the user will find enough similarities to allow a certain amount of compatibility among equipment built to the two standards. Following is a summary of the key specifications relating to the systems and the receivers.

Parameter	EIA-232-E	EIA-562
Max Data Rate	20 kBaud	38.4 kBaud Asynchronous 64 kBaud Synchronous
Max Cable Length	50 feet	Based on cable capacitance/data rate
Transition Region	–3.0 V to +3.0 V	–3.0 V to +3.0 V
MARK (one, off)	More negative than –3.0 V	More negative than –3.3 V
SPACE (zero, on)	More positive than +3.0 V	More positive than +3.3 V
Fail Safe	Output = Binary 1	Output = Binary 1
Open Circuit Input Voltage	< I2.0IV	Not Specified
Slew Rate (at the driver)	≤ 30 V/μs anywhere on the waveform	≤ 30 V/μs anywhere on the waveform, ≥ 4.0 V/μs between +3.0 V and –3.0 V
Loaded Output Voltage (at the driver)	5.0 V ≤ |VO| ≤ 15 V for loads between 3.0 kΩ and 7.0 kΩ	|VO| ≥ 3.7 V for a load of 3.0 kΩ

Figure 2. Typical Output versus Supply Voltage

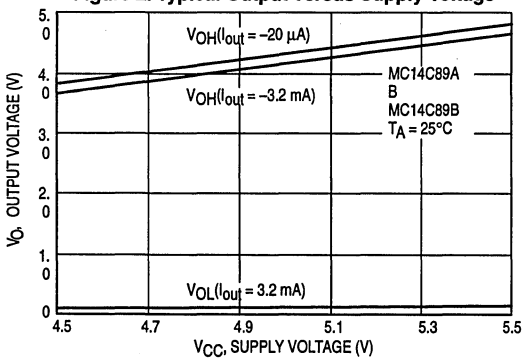


Figure 3. Typical Output Voltage versus Temperature

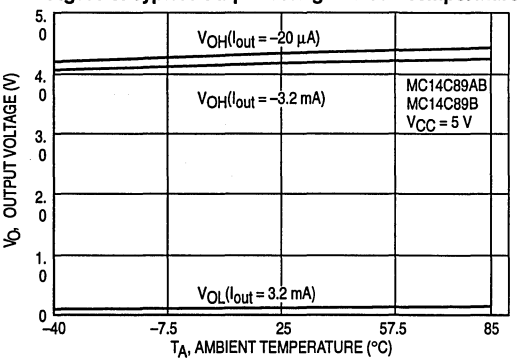


Figure 4. Typical Short Circuit Current versus Temperature

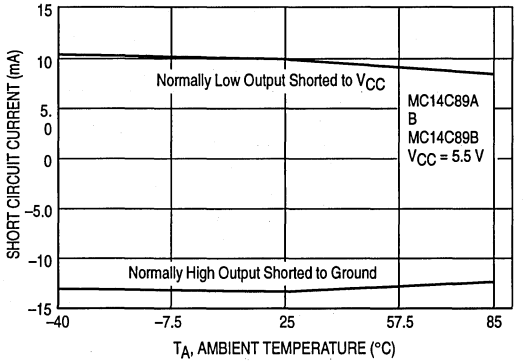


Figure 5. Typical Threshold Voltage versus Temperature

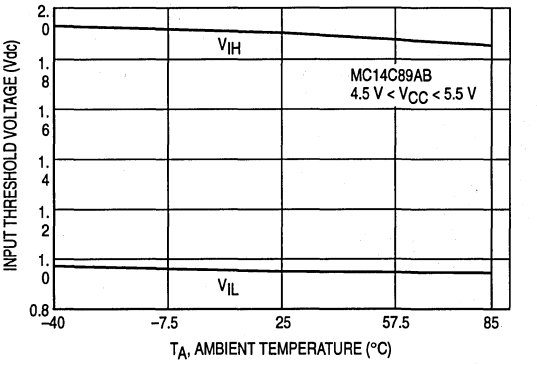


Figure 6. Typical Threshold Voltage versus Temperature

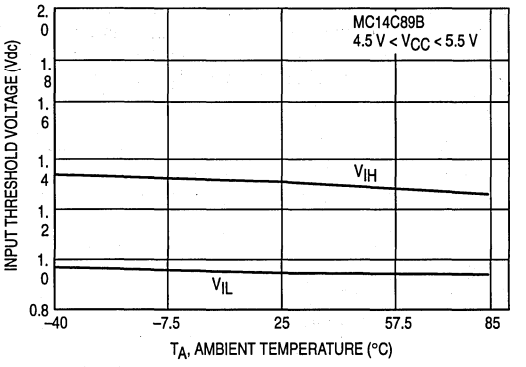


Figure 7. Typical Effect of Response Control Pin Bias

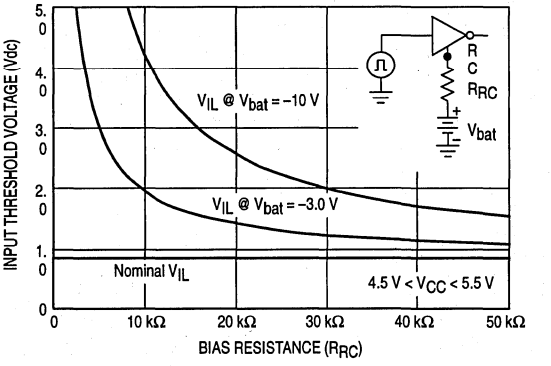
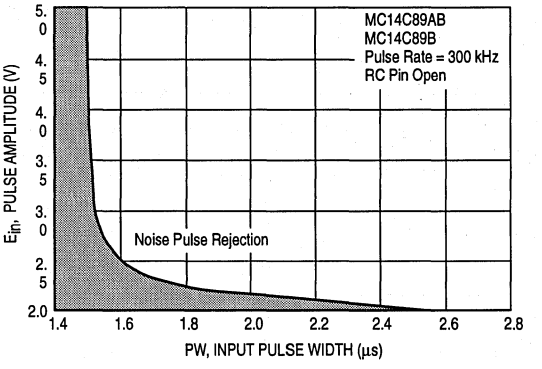


Figure 8. Typical Noise Pulse Rejection



APPLICATIONS INFORMATION

Description

The MC14C89AB and MC14C89B are designed to be direct replacements for the MC1489A and MC1489. Both devices meet all the EIA-232 specifications and also the faster EIA-562 and CCITT V.28 specifications. Noise pulse rejection circuitry eliminates the need for most response control filter capacitors but does not exclude the possibility as filtering is still possible at the Response Control (RC) pins. Also, the Response Control pins allow for a user defined selection of the threshold voltages. The MC14C89AB and MC14C89B are manufactured with a bipolar technology using low power techniques and consume at most 700 μA, plus load currents with a +5.0 V supply.

Outputs

The output low or high voltage depends on the state of the inputs, the load current, the bias of the Response Control pins, and the supply voltage. Table 1 applies to each receiver, regardless of how many other receivers within the package are supplying load current.

Table 1. Function Table

Receivers

Input *	Output *
H	L
L	H

*The asterisk denotes A, B, C, or D.

Receiver Inputs and Response Control

The receiver inputs determine the state of the outputs in accordance with Table 1. The nominal V_{IL} and V_{IH} thresholds are 0.95 V and 1.90 V respectively for the MC14C89AB. For the MC14C89B, the nominal V_{IL} and V_{IH} thresholds are 0.95 and 1.30, respectively. The inputs are able to withstand ± 30 V referenced to ground. Should the input voltage exceed ground by more than ± 30 V, excessive currents will flow at the input pin. Open input pins will generate a logic high output, but good design practices dictate that inputs should never be left open.

The Response Control (RC) pins are coupled to the inputs through a resistor string. The RC pins provide for adjustment of the threshold voltages of the IC while preserving the amount of hysteresis. Figure 10 shows a typical application to adjust the threshold voltages. The RC pins also provide access to an internal resistor string which permits low pass filtering of the input signal within the IC. Like the input pins, the RC pins should not be taken above or below ground by more than ± 30 V or excessive currents will flow at these pins. The dependence of the low level threshold voltage (V_{IL}) upon R_{RC} and V_{bat} can be described by the following equation,

$$V_{IL} \simeq \left\{V_{0.09} - V_{bat}\left[\frac{505\ \Omega}{R_{RC}\ (1.6) + 2.02\ k\Omega}\right]\right\} \left(\frac{5.32\ k\Omega + \frac{6.67 \times 10^6\ \Omega^2}{R_{RC}}}{505\ \Omega}\right) \quad (1)$$

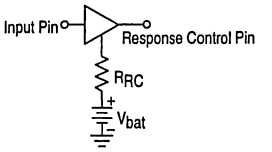
V_{IH} can be found by calculating for V_{IL} using equation (1) then adding the hysteresis for each device (0.35 for the MC14C89B or 0.95 V for the MC14C89AB). Figure 7 plots equation (1) for two values of V_{bat} and a range of R_{RC}.

If an RC pin is to be used for low pass filtering, the capacitor chosen can be calculated by the equation,

$$C_{RC} \simeq \frac{1}{2.02\ k\Omega\ 2\pi\ f_{-3\ dB}} \quad (2)$$

where $f_{-3\ dB}$ represents the desired –3 dB roll-off frequency of the low pass filter.

Figure 10. Application to Adjust Thresholds



Another feature of the MC14C89AB and MC14C89B is input noise rejection. The inputs have the ability to ignore pulses which exceed the V_{IH} and V_{IL} thresholds but are less than 1.0 μs in duration. As the duration of the pulse exceeds 1.0 μs, the noise pulse may still be ignored depending on its amplitude. Figure 8 is a graph showing typical input noise rejection as a function of pulse amplitude and pulse duration. Figure 8 reflects data taken for an input with an unconnected RC pin and applied to the MC14C89AB and MC14C89B.

Operating Temperature Range

The ambient operating temperature range is listed as –40°C to +85°C, and the devices are designed to meet the EIA-232-E, EIA-562 and CCITT V.28 specifications over this temperature range. The Timing Characteristics are guaranteed to meet the specifications at +25°C. The maximum ambient operating temperature is listed as +85°C. However, a lower ambient may be required depending on system use, (i.e., specifically how many receivers within a package are used) and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

where: $R_{\theta JA}$ = thermal resistance (typ., 100°C/W for the DIP and 125°C/W for the SOIC packages);
$T_{J(max)}$ = maximum operating junction temperature (150°C); and
T_A = ambient temperature.

P_D = {[(V_{CC} – V_{OH}) • $|I_{OH}|$] or [(V_{OL}) • $|I_{OL}|$]}each receiver +(V_{CC} • I_{CC})

where: V_{CC} = positive supply voltage;
V_{OH}, V_{OL} = measured or estimated from Figure 2 and 3;
I_{CC} = measured quiescent supply current.

As indicated, the first term (in brackets) must be calculated and summed for each of the four receivers, while the last term is common to the entire package.

MC1488

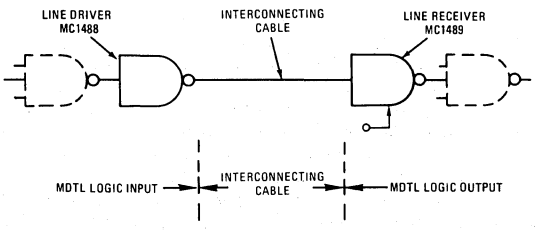
QUAD LINE DRIVER

The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

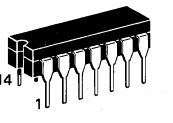
Features:

- Current Limited Output
  ±10 mA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

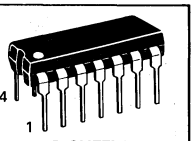
TYPICAL APPLICATION



QUAD MDTL LINE DRIVER
RS-232C
SILICON MONOLITHIC
INTEGRATED CIRCUIT

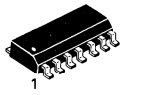


L SUFFIX
CERAMIC PACKAGE
CASE 632

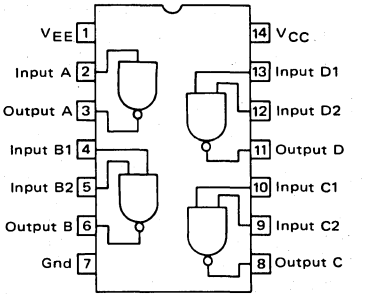


P SUFFIX
PLASTIC PACKAGE
CASE 646

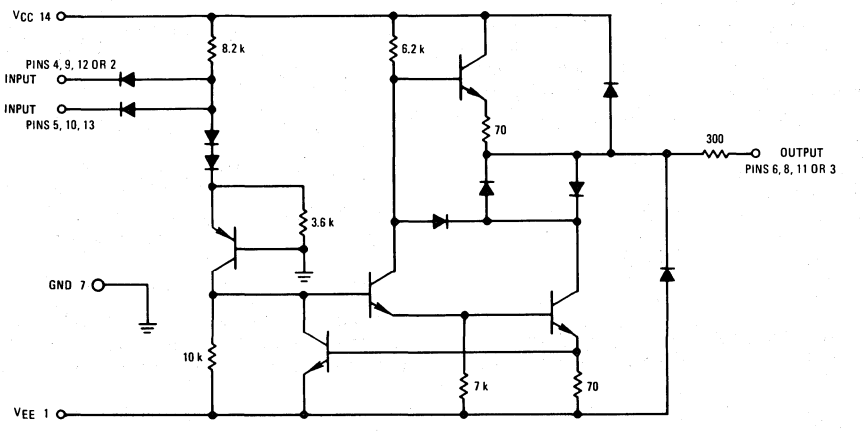
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



PIN CONNECTIONS



CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



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MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 −15	Vdc
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	Vdc
Output Signal Voltage	V_O	±15	Vdc
Power Derating (Package Limitation, Ceramic and Plastic Dual-In-Line Package) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +9.0 ±1% Vdc, V_{EE} = −9.0 ±1% Vdc, T_A = 0 to 75°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State (V_{IL} = 0)	1	I_{IL}	—	1.0	1.6	mA
Input Current — High Logic State (V_{IH} = 5.0 V)	1	I_{IH}	—	—	10	μA
Output Voltage — High Logic State (V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = −9.0 Vdc) (V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = −13.2 Vdc)	2	V_{OH}	 +6.0 +9.0	 +7.0 +10.5	 — —	Vdc
Output Voltage — Low Logic State (V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = −9.0 Vdc) (V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = −13.2 Vdc)	2	V_{OL}	 −6.0 −9.0	 −7.0 −10.5	 — —	Vdc
Positive Output Short-Circuit Current (1)	3	I_{OS+}	+6.0	+10	+12	mA
Negative Output Short-Circuit Current (1)	3	I_{OS-}	−6.0	−10	−12	mA
Output Resistance (V_{CC} = V_{EE} = 0, $\|V_O\|$ = ±2.0 V)	4	r_o	300	—	—	Ohms
Positive Supply Current (R_l = ∞) (V_{IH} = 1.9 Vdc, V_{CC} = +9.0 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = +9.0 Vdc) (V_{IH} = 1.9 Vdc, V_{CC} = +12 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = +12 Vdc) (V_{IH} = 1.9 Vdc, V_{CC} = +15 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = +15 Vdc)	5	I_{CC}	 — — — — — —	 +15 +4.5 +19 +5.5 — —	 +20 +6.0 +25 +7.0 +34 +12	mA
Negative Supply Current (R_L = ∞) (V_{IH} = 1.9 Vdc, V_{EE} = −9.0 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = −9.0 Vdc) (V_{IH} = 1.9 Vdc, V_{EE} = −12 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = −12 Vdc) (V_{IH} = 1.9 Vdc, V_{EE} = −15 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = −15 Vdc)	5	I_{EE}	 — — — — — —	 −13 — −18 — — —	 −17 −500 −23 −500 −34 −2.5	 mA μA mA μA mA mA
Power Consumption (V_{CC} = 9.0 Vdc, V_{EE} = −9.0 Vdc) (V_{CC} = 12 Vdc, V_{EE} = −12 Vdc)		P_C	 — —	 — —	 333 576	mW

SWITCHING CHARACTERISTICS (V_{CC} = +9.0 ±1% Vdc, V_{EE} = −9.0 ±1% Vdc, T_A = +25°C.)

Propagation Delay Time	(z_l = 3.0 k and 15 pF)	6	t_{PLH}	—	275	350	ns
Fall Time	(z_l = 3.0 k and 15 pF)	6	t_{THL}	—	45	75	ns
Propagation Delay Time	(z_l = 3.0 k and 15 pF)	6	t_{PHL}	—	110	175	ns
Rise Time	(z_l = 3.0 k and 15 pF)	6	t_{TLH}	—	55	100	ns

(1) Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

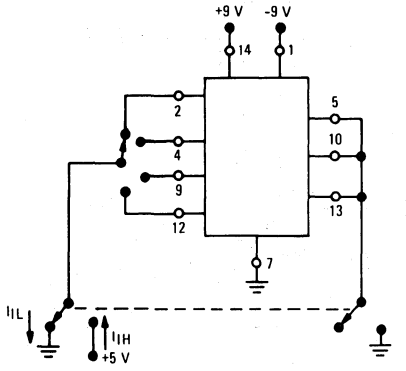


FIGURE 2 – OUTPUT VOLTAGE

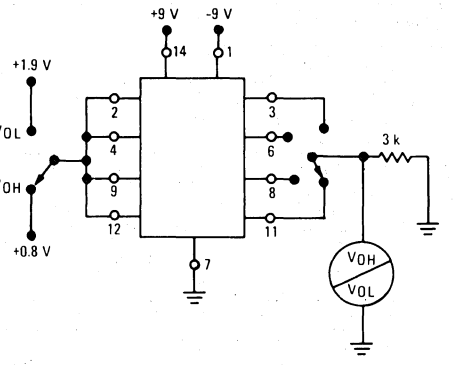


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

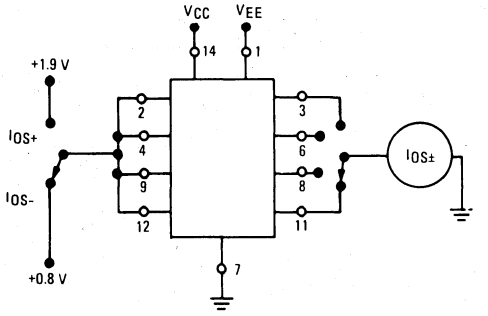


FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

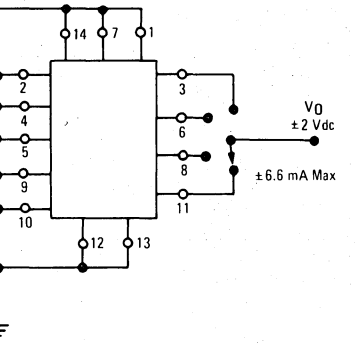


FIGURE 5 – POWER-SUPPLY CURRENTS

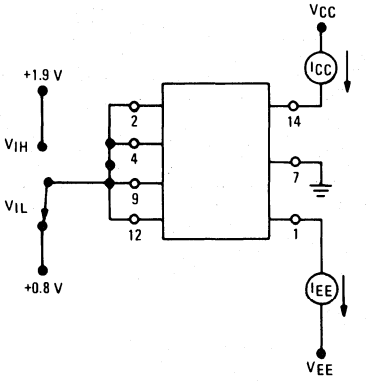
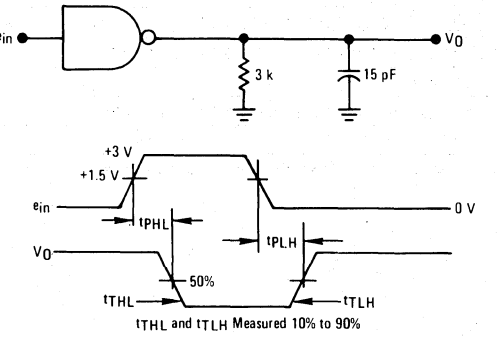


FIGURE 6 – SWITCHING RESPONSE



TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 7 — TRANSFER CHARACTERISTICS versus POWER-SUPPLY VOLTAGE

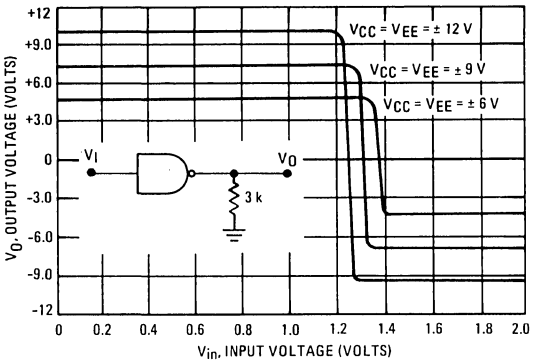


FIGURE 8 — SHORT-CIRCUIT OUTPUT CURRENT versus TEMPERATURE

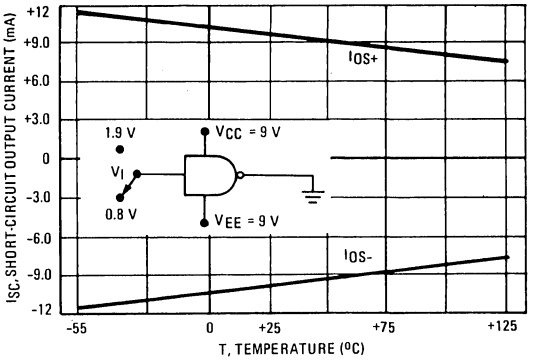


FIGURE 9 — OUTPUT SLEW RATE versus LOAD CAPACITANCE

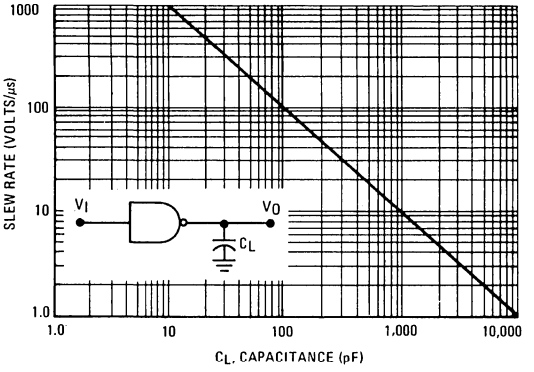


FIGURE 10 — OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

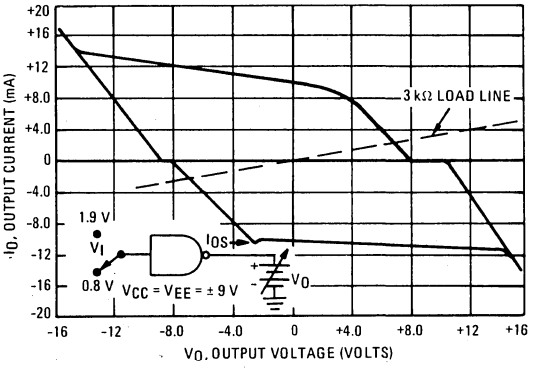
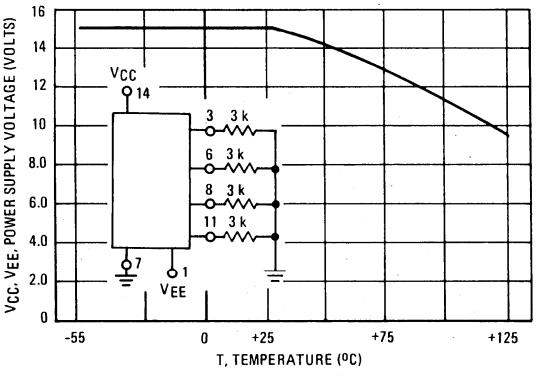


FIGURE 11 — MAXIMUM OPERATING TEMPERATURE versus POWER-SUPPLY VOLTAGE



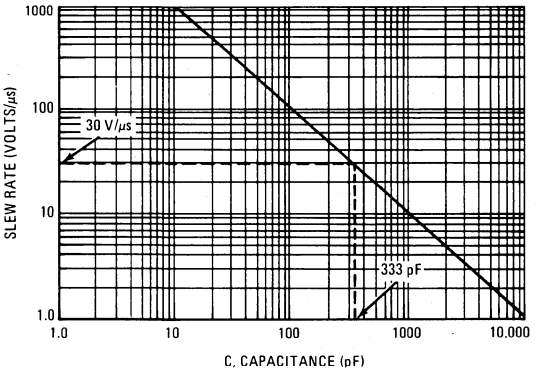
APPLICATIONS INFORMATION

The Electronic Industries Association (EIA) RS232C specification detail the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined levels. The RS232C requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a logic "0" and negative for a logic "1". These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into RS232C levels with one stage of inversion.

The RS232C specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488 is much too

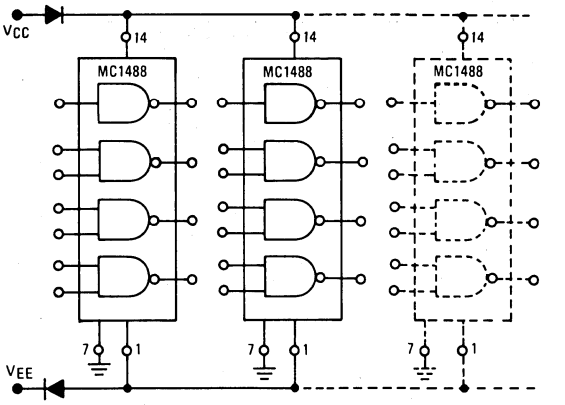
FIGURE 12 – SLEW RATE versus CAPACITANCE FOR I_{SC} = 10 mA



fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330-pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15-volt, 500-mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geqslant 9.0$ V; $V_{EE} \leqslant -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300-ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors

FIGURE 13 – POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25-volt limits specified in the earlier Standard RS232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting – this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high-level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power-Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately -2.5 volts to the minimum specified -15 volts. The MC1488 will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving RS232C lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

FIGURE 14 – MDTL/MTTL-TO-MOS TRANSLATOR

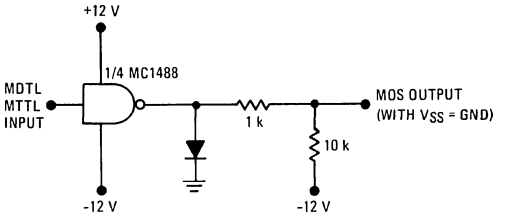
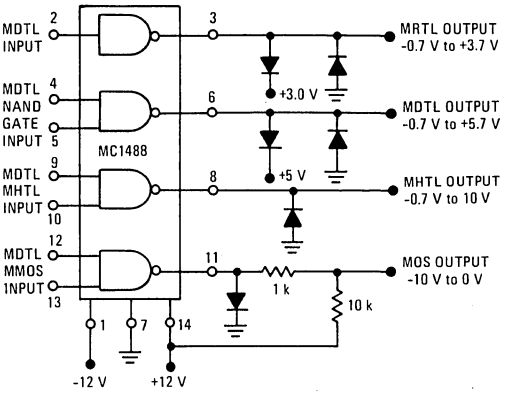


FIGURE 15 – LOGIC TRANSLATOR APPLICATIONS



MC1489
MC1489A

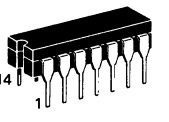
QUAD LINE RECEIVERS

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS-232C.

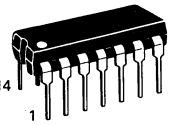
- Input Resistance — 3.0 k to 7.0 kilohms
- Input Signal Range — ± 30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  a) Logic Threshold Shifting
  b) Input Noise Filtering

QUAD MDTL LINE RECEIVERS RS-232C

SILICON MONOLITHIC INTEGRATED CIRCUIT

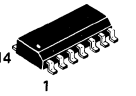


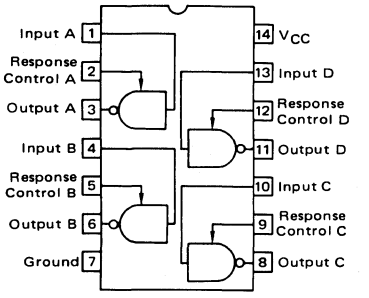
L SUFFIX
CERAMIC PACKAGE
CASE 632



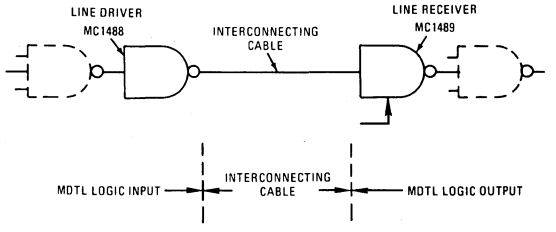
P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

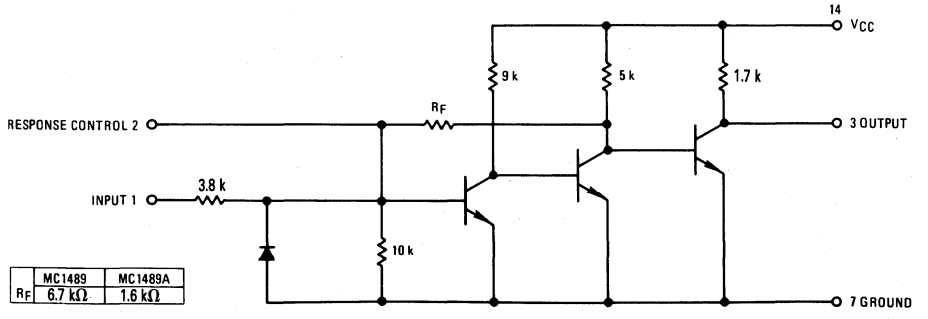




TYPICAL APPLICATION



EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



	MC1489	MC1489A
RF	6.7 kΩ	1.6 kΩ

MDTL and MTTL are trademarks of Motorola Inc.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Voltage Range	V_{IR}	±30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, Ceramic and Plastic Dual In-Line Package) Derate above T_A = +25°C	P_D $1/\theta JA$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = +5.0 Vdc ±10%, T_A = 0 to +75°C unless otherwise noted)

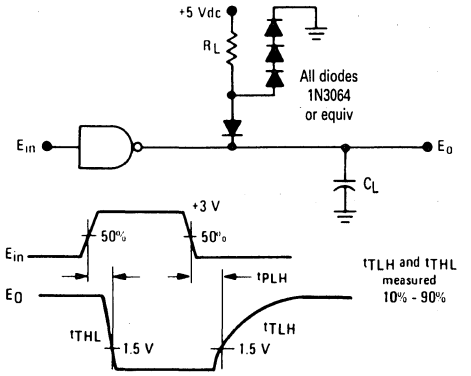
Characteristics		Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{IH} = +25 Vdc) (V_{IH} = +3.0 Vdc)	I_{IH}	3.6 0.43	— —	8.3 —	mA
Negative Input Current	(V_{IL} = −25 Vdc) (V_{IL} = −3.0 Vdc)	I_{IL}	−3.6 −0.43	— —	−8.3 —	mA
Input Turn-On Threshold Voltage (T_A = +25°C, V_{OL} ≤ 0.45 V)	MC1489 MC1489A	V_{IH}	1.0 1.75	— 1.95	1.5 2.25	Vdc
Input Turn-Off Threshold Voltage (T_A = +25°C, V_{OH} ≥ 2.5 V, I_L = −0.5 mA)	MC1489 MC1489A	V_{IL}	0.75 0.75	— 0.8	1.25 1.25	Vdc
Output Voltage High	(V_{IH} = 0.75 V, I_L = −0.5 mA) (Input Open Circuit, I_L = −0.5 mA)	V_{OH}	2.5 2.5	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low	(V_{IL} = 3.0 V, I_L = 10 mA)	V_{OL}	—	0.2	0.45	Vdc
Output Short-Circuit Current		I_{OS}	—	−3.0	−4.0	mA
Power Supply Current (All Gates "on," I_{out} = 0 mA, V_{IH} = +5.0 Vdc)		I_{CC}	—	16	26	mA
Power Consumption	(V_{IH} = +5.0 Vdc)	P_C	—	80	130	mW

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ±1%, T_A = +25°C, See Figure 1.)

Propagation Delay Time	(R_L = 3.9 kΩ)	t_{PLH}	—	25	85	ns
Rise Time	(R_L = 3.9 kΩ)	t_{TLH}	—	120	175	ns
Propagation Delay Time	(R_L = 390 kΩ)	t_{PHL}	—	25	50	ns
Fall Time	(R_L = 390 kΩ)	t_{THL}	—	10	20	ns

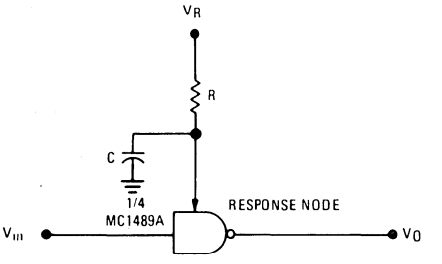
TEST CIRCUITS

FIGURE 1 — SWITCHING RESPONSE



C_L = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances

FIGURE 2 — RESPONSE CONTROL NODE



C, capacitor is for noise filtering.
R, resistor is for threshold shifting.

TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 — INPUT CURRENT

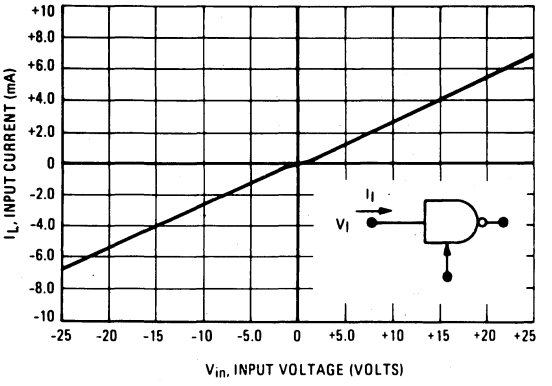


FIGURE 4 — MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

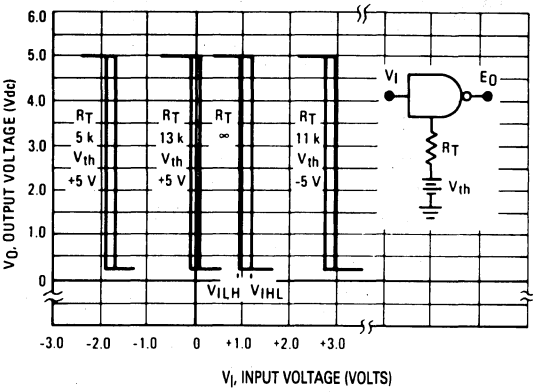


FIGURE 5 — MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

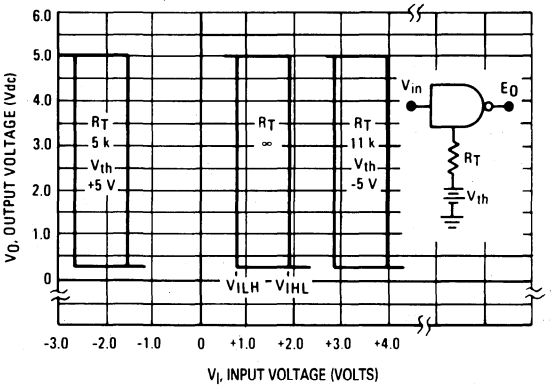


FIGURE 6 — INPUT THRESHOLD VOLTAGE versus TEMPERATURE

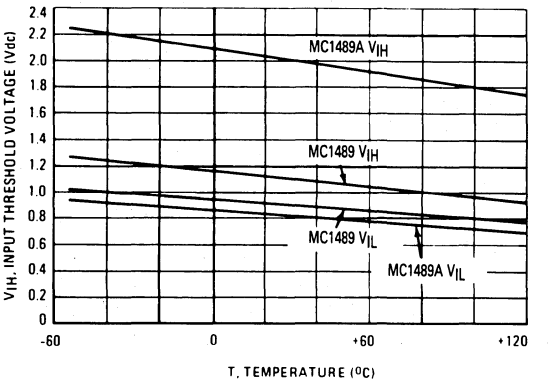
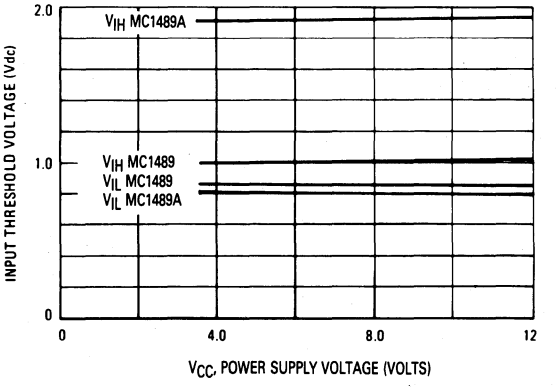


FIGURE 7 — INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the RS-232C specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232C defined levels. The RS-232C requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between −3.0 and −25 volts as a Logic "1" and inputs between +3.0 and +25 volts as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power-supply. Figures 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high-energy noise pulses. Figures 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the RS-232C impedance requirement.

FIGURE 8 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

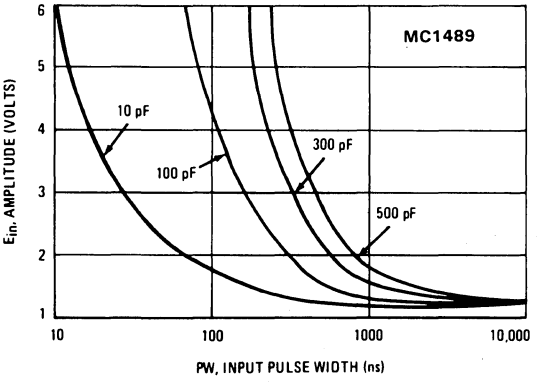


FIGURE 9 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

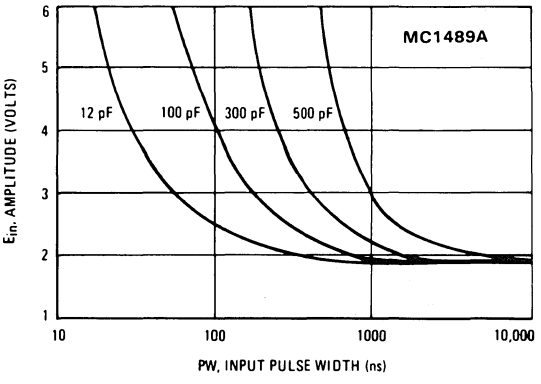


FIGURE 10 — TYPICAL TRANSLATOR APPLICATION — MOS TO DTL OR TTL

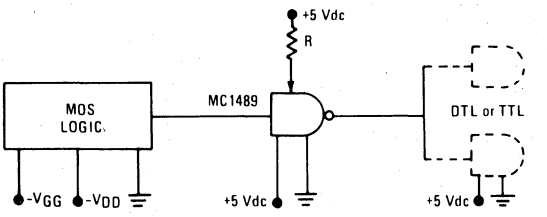
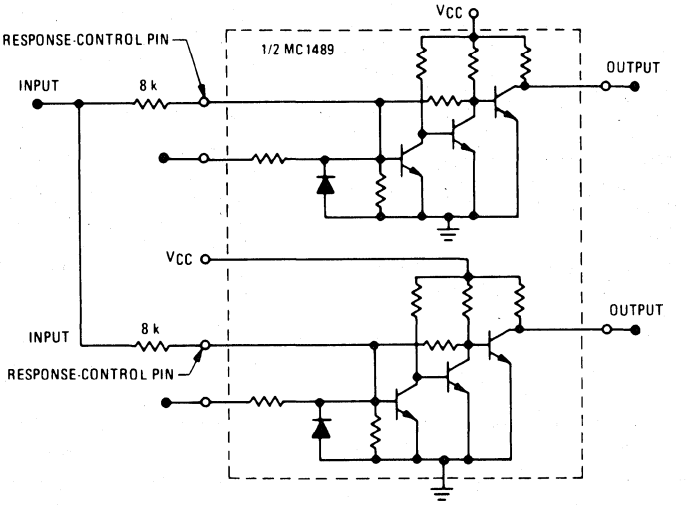
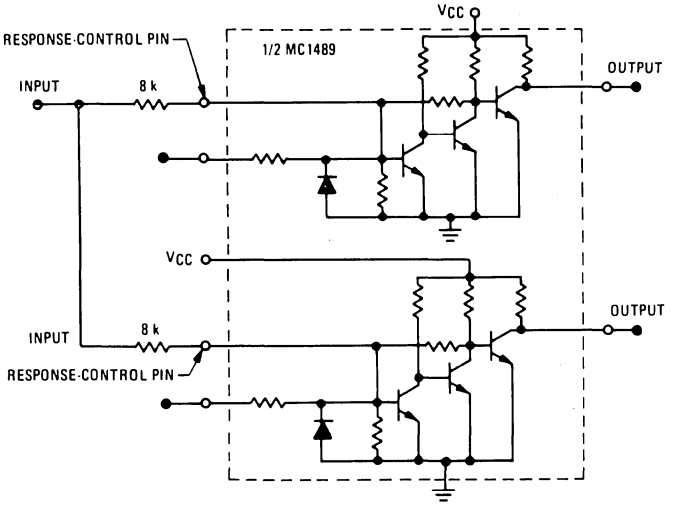


FIGURE 11 — TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET RS-232C



APPLICATIONS INFORMATION (continued)

FIGURE 11 — TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET RS-232C

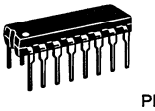


MC26C31

Product Preview

Quad EIA-422-A Line Driver

CMOS



P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC26C31P	Plastic DIP
MC26C31D	SOG Package

The MC26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The MC26C31 meets all the requirements of standard EIA-422-A while retaining the low-power characteristics of CMOS.

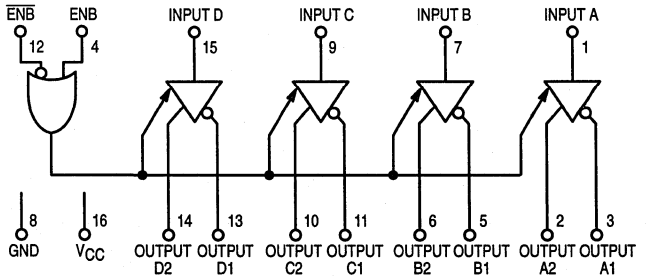
The MC26C31 accepts TTL or CMOS input levels and translates these to EIA-422-A output level. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. The MC26C31 also includes special circuitry which will set the outputs to a high impedance mode during power up or down, preventing spurious glitches. This device has enable and disable circuitry common for all four drivers.

The MC26C31 is pin compatible with the AM26LS31.

All pins are protected against damage due to electrostatic discharges.

- Maximum Supply Current: 3 mA
- 2000-V ESD Protection on the Inputs and Outputs
- TTL/CMOS Input Compatible
- Typical Propagation Delay: 6 ns
- Typical Output Skew: 1 ns
- Meets V_O = 6.0 V (and V_O = 0.25 V), V_{CC} = 0 V, I_O < 100 μA Requirement
- Meets the Requirements of Standard EIA-422-A
- Operation from single 5-V Supply
- High-Impedance Mode for Outputs Connected to System Buses

BLOCK DIAGRAM



This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV. 3

TRUTH TABLE

Control Inputs E/$\overline{E}$	Input	Non-Inverting Output	Inverting Output
L/H	X	Z	Z
All other combinations of enable inputs	H	H	L
	L	L	H

X = Don't Care
Z = High Impedance
H = High Logic State
L = Low Logic State

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
DC Input Voltage	V_{in}	−1.5 to V_{CC} +1.5	V
DC Output Voltage*	V_{out}	−0.5 to V_{CC} +0.5	V
DC Output Current, per Pin	I_{out}	150	mA
DC V_{CC} or GND Current, per Pin	I_{DD}	150	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	500	mW
ESD (Human Body model)		2000	V

* Power-on conditions.

OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
DC Input Voltage	V_{in}	0	V_{CC}	V
Operating Temperature Range	T_A	−40	+ 85	°C
Input Rise and Fall Time	t_r, t_f	—	500	ns

DC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = − 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage (Low Logic State)	V_{IL}	—	—	0.8	V
Input Voltage (High Logic State)	V_{IH}	2.0	—	—	V
Output Voltage (Low Logic State) I_{sink} = 20 mA	V_{OL}	—	0.3	0.5	V
Output Voltage (High Logic State) I_{source} = 20 mA	V_{OH}	2.5	2.8	—	V
Output Differential Voltage R_L = 100 Ω (Note 1)	V_{OD}	2.0	—	—	V
Output Differential Voltage Difference R_L = 100 Ω (Note 1)	$D(V_{OD})$	—	—	±0.4	V
Output Offset Voltage R_L = 100 Ω (Note 1)	V_{OS}	—	—	3.0	V
Output Offset Voltage Difference R_L = 100 Ω (Note 1)	$D(V_{OS})$	—	—	±0.4	V
Input Current V_{IH} = V_{CC}, GND, V_{IH} or V_{IL}	I_{in}	—	—	±1.0	µA
Quiescent Supply Current I_{out} = 0 µA	I_{CC}	—	—	3.0	mA
Output Short Circuit Current (Note 2)	I_{OS}	−30	−100	−150	mA
Output Leakage Current (Hi-Z State) V_{out} = V_{CC} or GND	$I_{O(Z)}$	—	—	±1.0	µA
Input Leakage Current (Power Off) V_{out} = 6 V	I_{oxh}	—	—	100	µA
V_{out} = − 0.25 V	I_{oxl}	—	—	−100	

NOTES:
1. See EIA specifications EIA-422-A for exact test conditions.
2. Only one output may be shorted at a time.

AC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay Input to Output (S1 Open)	t_{PLH} t_{PHL}	—	6	12	ns
Output Skew (S1 Open)*	Skew	—	1.0	4	ns
Differential Output Rise Time Fall Time (S1 Open)	$t_{(TLH)}$ $t_{(THL)}$	—	4	8	ns
Output Enable Time (S1 Closed)	t_{PZH} t_{PZL}	— —	16 15	— —	ns
Output Disable Time (S1 Closed)	t_{PHZ} t_{PLZ}	— —	6 9	— —	ns

* Skew: difference in propagation delays between complementary outputs.

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

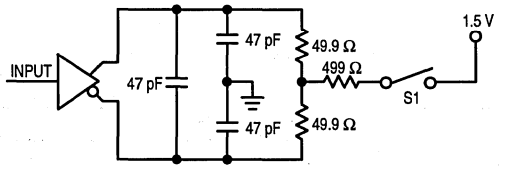


Figure 1. AC Test Circuit

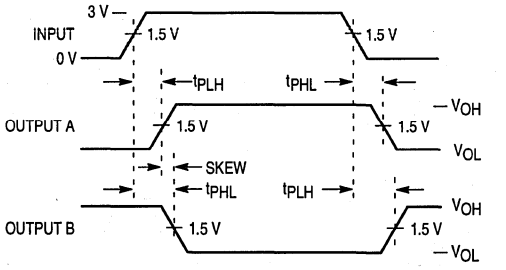


Figure 2. Propagation Delays and Skew Waveforms

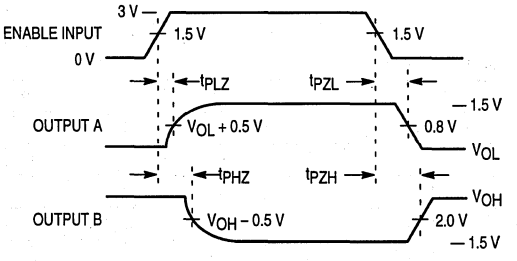


Figure 3. Enable and Disable Times

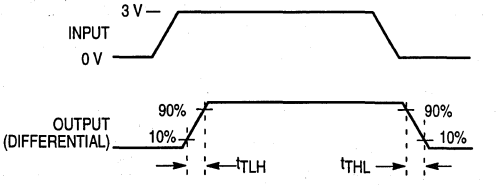


Figure 4. Differential Rise and Fall Times

TYPICAL APPLICATIONS

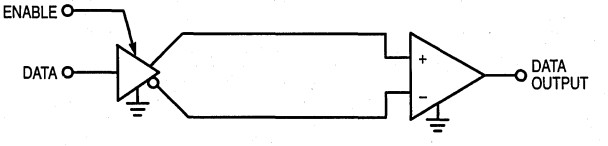


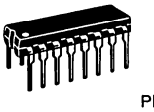
Figure 5. Two-Wire Balanced Systems (EIA-422-A)

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC26C32

Product Preview

Quad EIA-422-A Line Receiver
CMOS



P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC26C32P	Plastic DIP
MC26C32D	SOG Package

The MC26C32 is a quad differential line receiver designed for digital data transmission over balanced lines. The MC26C32 meets all the requirements of standard EIA-422-A while retaining the low-power characteristics of CMOS.

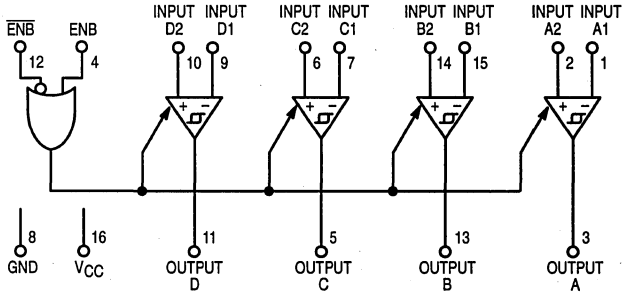
The MC26C32 has an input sensitivity of 200 mV over the common mode input voltage range of ± 7 V. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

The MC26C32 is pin compatible with the AM26LS32.

All pins are protected against damage due to electrostatic discharges.

- Typical Power Supply Current: 6 mA
- 2000-V ESD Protection on the Inputs and Outputs
- Typical Propagation Delay: 18 ns
- Typical Input Hysteresis: 75 mV
- Meets the Requirements of Standard EIA-422-A
- Operation from single 5-V Supply
- High-Impedance Mode for Outputs Connected to System Buses
- TTL/CMOS Compatible Outputs

BLOCK DIAGRAM



This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV. 3

TRUTH TABLE

Control Inputs E/$\overline{E}$	Input	Output
L/H	X	Z
All other combinations of enable inputs	$V_{ID} \geq V_{TH}$ (max)	1
	$V_{ID} \geq V_{TH}$ (min)	0
	Open	1

X = Don't Care
Z = High Impedance
H = High Logic State
L = Low Logic State

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
Input Voltage	V_I	±12	V
Input Differential Voltage	V_{ID}	±14	V
Enable Control Input Voltage	V_{in}	V_{CC} + 0.5	V
Storage Temperature	T_{stg}	−65 to +150	°C
Maximum Current per Output	I_O	±25	mA
ESD (Human Body model)		2000	V

OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
Operating Temperature Range	T_A	−40	+85	°C
Input Rise and Fall Time	t_r, t_f	—	500	ns

DC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = −40 to +85°C, unless otherwise stated) (See Note 1)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current, $V_{CC} \geq$ Max		I_{CC}	—	6	12	mA
Enable Input Current, $V_{in} = V_{CC}$ or GND		I_I	—	—	±1.0	µA
Input Voltage — Low Logic State (Enable Control)		V_{IL}	—	—	0.8	V
Input Voltage — High Logic State (Enable Control)		V_{IH}	2	—	—	V
Differential Input Voltage, −7 V < V_{LCM} < 7 V	$V_{out} = V_{OH}$ $V_{out} = V_{OL}$	V_{TH}	0.2 —	— —	— −0.2	V
Input Hysteresis, V_{LCM} = 0 V		V_{hys}	—	75	—	mV
Comparator Input Current	V_{in} = +10 V, Other Input = GND V_{in} = −10 V, Other Input = GND	I_{in}	— —	1.4 −2.5	— —	mA
Comparator Input Resistance, −12 V < V_{LCM} < +12 V		R_{in}	4	4.8	—	kΩ
Output Voltage (Low Logic State) V_{ID} = −1 V, I_{out} = 6 mA (Note 2)		V_{OL}	—	0.13	0.33	V
Output Voltage (High Logic State) V_{ID} = +1 V, I_{out} = −6 mA (Note 2)		V_{OH}	3.8	4.8	—	V
Output Leakage Current (High Logic State) $V_{out} = V_{CC}$ or GND		I_{OZ}	−5	—	5	µA

NOTES:
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. See EIA specifications EIA-422-A for exact test conditions.

AC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay Input to Output, C_L = 50 pF, V_{DIFF} = 2.5 V	t_{PLH} t_{PHL}	—	18	30	ns
Skew = $\lvert t_{PHL} - t_{PLH} \rvert$	Skew	—	1	—	ns
Propagation Delay Enable to Output C_L = 50 pF, R_L = 1000 Ω, V_{DIFF} = 2.5 V	t_{PLZ} t_{PHZ}	—	12	—	ns
Propagation Delay Enable to Output C_L = 50 pF, R_L = 1000 Ω, V_{DIFF} = 2.5 V	t_{PZL} t_{PZH}	—	14	—	ns

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

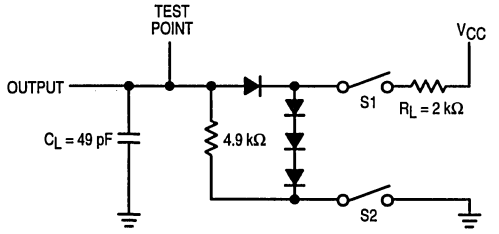


Figure 6. Test Circuit

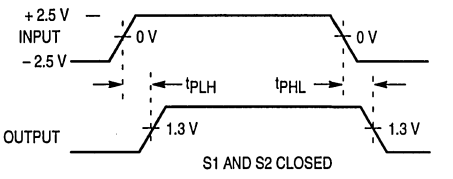


Figure 7. Propagation Delays

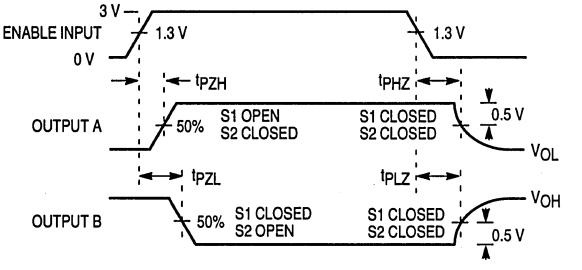


Figure 8. Enable and Disable Times

TYPICAL APPLICATIONS

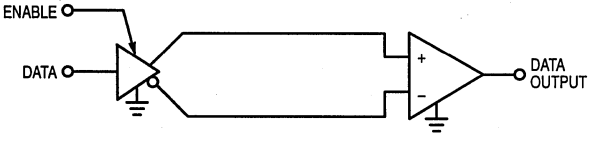


Figure 9. Two-Wire Balanced Systems (EIA-422-A)

MC2831A

LOW POWER FM TRANSMITTER SYSTEM

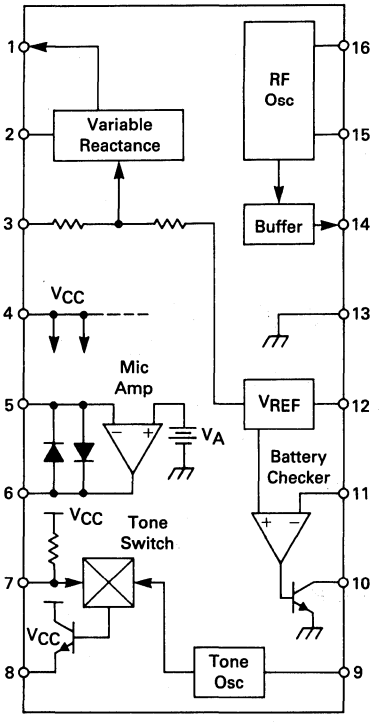
The MC2831A is a one-chip FM transmitter subsystem designed for cordless telephone and FM communication equipment. It includes a Microphone Amplifier, Pilot Tone Oscillator, Voltage Controlled Oscillator and Battery Monitor.

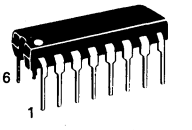
- Wide Range of Operating Supply Voltage (3.0 V–8.0 V)
- Low Drain Current (4.0 mA Typ Full Operation at V_{CC} = 4.0 V)
- Battery Checker (290 μA Typ at V_{CC} = 4.0 V)
- Low Number of External Parts Required

LOW POWER FM TRANSMITTER SYSTEM

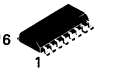
SILICON MONOLITHIC INTEGRATED CIRCUIT

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



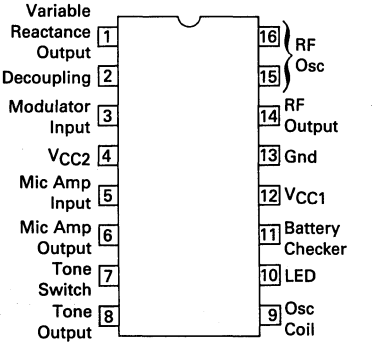


P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
SO-16

PIN ASSIGNMENTS



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 12	V_{CC}	10	Vdc
Operating Supply Voltage Range	4, 12	V_{CC}	3.0 to 8.0	Vdc
Battery Checker Output Sink Current	10	I_{LED}	25	mA
Junction Temperature	—	T_J	+150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +75	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC1} = 4.0 Vdc, V_{CC2} = 4.0 Vdc, T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
Drain Current	I_{CC1}	12	150	290	420	μA
Drain Current	I_{CC2}	4	2.2	3.6	6.5	mA
BATTERY CHECKER						
Threshold Voltage (LED Off → On)	V_{TB}	11	1.0	1.2	1.4	Vdc
Output Saturation Voltage (Pin 11 = 0 V, Pin 10 Sink Current = 5.0 mA)	V_{OSAT}	10	—	0.15	0.5	Vdc
MIC AMPLIFIER						
Voltage Gain, Closed Loop (V_{in} = 1.0 mV_{rms}, f_{in} = 1.0 kHz)	—	5, 6	27	30	33	dB
Output dc Voltage	—	6	1.1	1.4	1.7	Vdc
Output Swing (V_{in} = 30 mV_{rms}, f_{in} = 1.0 kHz)	—	6	0.8	1.2	1.6	Vp-p
Total Harmonic Distortion (V_O = 31 mV_{rms}, f_{in} = 1.0 kHz)	THD	6	—	0.7	—	%
PILOT TONE OSCILLATOR (250 Ω LOADING)						
Output AF Voltage (f_o = 5.0 kHz)	—	8	—	50	—	mV_{rms}
Output dc Voltage	—	8	—	1.4	—	Vdc
Total Harmonic Distortion (f_o = 5.0 kHz, V_{AF} = 150 mV_{rms})	—	8	—	1.8	5.0	%
Tone Switch Threshold	—	7	1.1	1.4	1.7	Vdc
FM MODULATOR (120 Ω LOADING)						
Output RF Voltage (f_o = 16.6 MHz)	VRFO	14	—	40	—	mV_{rms}
Output dc Voltage	—	14	—	1.3	—	Vdc
Modulation Sensitivity (Note 1) (V_{in} = 1.0 V ± 0.2 V)	—	3, 14	6.0	10	18	Hz/mVdc
Maximum Deviation (Note 1) (V_{in} = 0 V to +2.0 V)	—	3, 14	±2.5	±5.0	±12.5	kHz
RF Frequency Range	—	14	—	—	60	MHz

Note 1. Modulation sensitivity and maximum deviation are measured at 49.815 MHz, which is the third harmonic of the crystal frequency.

FIGURE 2 — TEST CIRCUIT

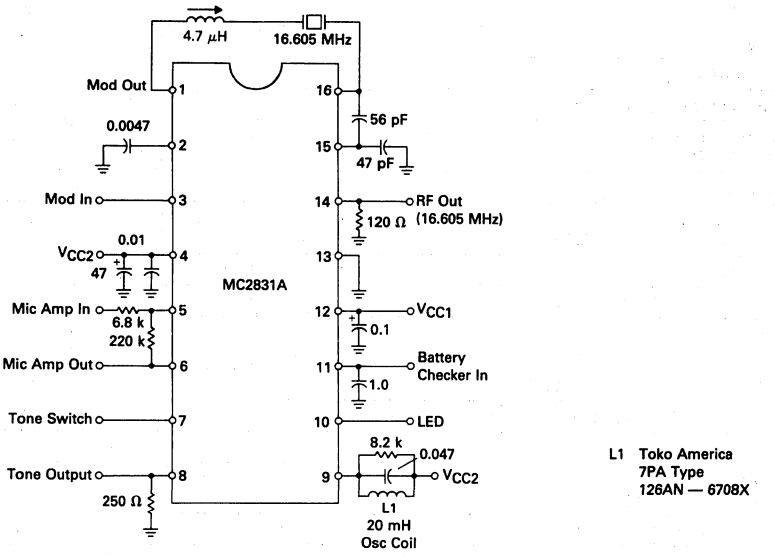
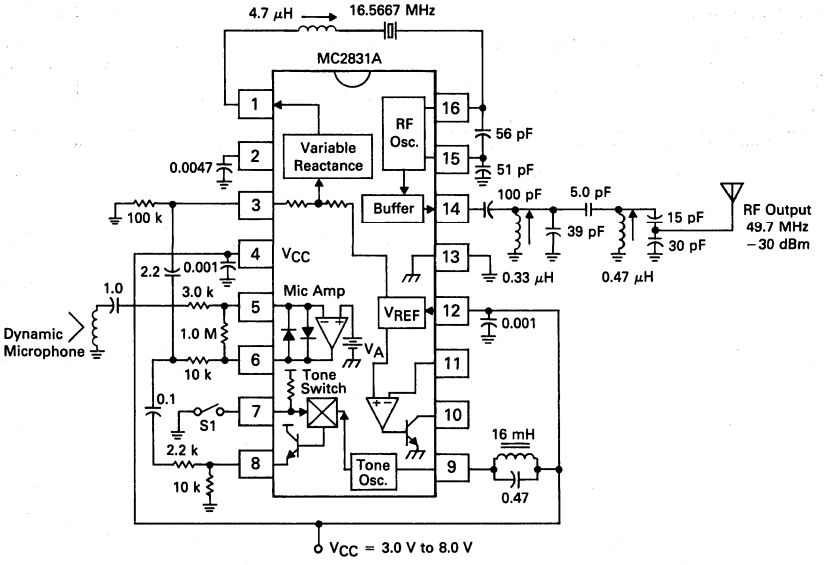


FIGURE 3 — SINGLE CHIP FM VHF TRANSMITTER AT 49.7 MHz



NOTES:

S1 is a normally closed push button type switch.

The crystal used is fundamental mode, calibrated for parallel resonance with a 32 pF load. The 49.7 MHz output is generated in the output buffer, which generates useful harmonics to 60 MHz.

The network on the output at Pin 14 provides output tuning and impedance matching to 50 Ω at 49.7 MHz. Harmonics are suppressed by more than 25 dB.

Battery checker circuit (Pins 10, 11) is not used in this application.

All capacitors in microfarads, inductors in Henries and resistors in Ohms, unless otherwise specified.

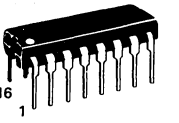
MC2833

LOW POWER FM TRANSMITTER SYSTEM

MC2833 is a one-chip FM transmitter subsystem designed for cordless telephone and FM communication equipment. It includes a microphone amplifier, voltage controlled oscillator and two auxiliary transistors.

- Wide Range of Operating Supply Voltage (2.8–9.0 V)
- Low Drain Current (I_{CC} = 2.9 mA Typ)
- Low Number of External Parts Required
- −30 dBm Power Output to 60 MHz Using Direct RF Output
- +10 dBm Power Output Attainable Using On-Chip Transistor Amplifiers

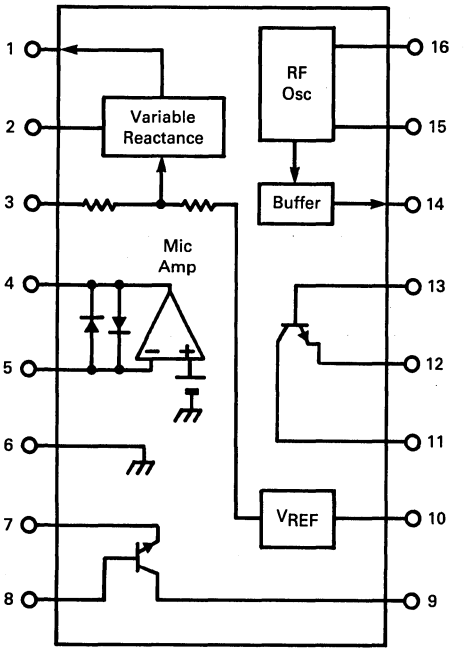
LOW POWER FM TRANSMITTER SYSTEM



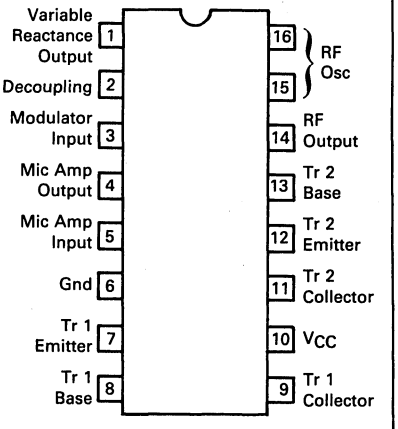
P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
SO-16

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS



MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10 (max)	V
Operating Supply Voltage Range	V_{CC}	2.8–9.0	V
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	−30 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 V, T_A = 25°C, unless otherwise noted)

Characteristics	Symbol	Pin	Min	Typ	Max	Unit
Drain Current (No input signal)	I_{CC}	10	1.7	2.9	4.3	mA
FM MODULATOR						
Output RF Voltage (f_o = 16.6 MHz)	V_{out} RF	14	60	90	130	mVrms
Output DC Voltage (No input signal)	Vdc	14	2.2	2.5	2.8	V
Modulation Sensitivity (f_o = 16.6 MHz) (V_{in} = 0.8 V to 1.2 V)	SEN	3.0 14	7.0 —	10 —	15 —	Hz/mVdc
Maximum Deviation (f_o = 16.6 MHz) (V_{in} = 0 V to 2.0 V)	Fdev	3.0 14	3.0 —	5.0 —	10 —	kHz
MIC AMPLIFIER						
Closed Loop Voltage Gain (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	A_V	4.0 5.0	27 —	30 —	33 —	dB
Output DC Voltage (No input signal)	V_{out} dc	4.0	1.1	1.4	1.7	V
Output Swing Voltage (V_{in} = 30 mVrms) (f_{in} = 1.0 kHz)	V_{out} p-p	4.0	0.8	1.2	1.6	Vp-p
Total Harmonic Distortion (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	THD	4.0	—	0.15	2.0	%

AUXILIARY TRANSISTOR STATIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Collector Base Breakdown Voltage (I_C = 5.0 μA)	$V_{(BR)CBO}$	15	45	—	V
Collector Emitter Breakdown Voltage (I_C = 200 μA)	$V_{(BR)CEO}$	10	15	—	V
Collector Substrate Breakdown Voltage (I_C = 50 μA)	$V_{(BR)CSO}$	—	70	—	V
Emitter Base Breakdown Voltage (I_E = 50 μA)	$V_{(BR)EBO}$	—	6.2	—	V
Collector Base Cut Off Current (V_{CB} = 10 V) (I_E = 0)	I_{CBO}	—	—	200	nA
DC Current Gain (I_C = 3.0 mA) (V_{CE} = 3.0 V)	h_{FE}	40	150	—	—

AUXILIARY TRANSISTOR DYNAMIC CHARACTERISTICS

Current Gain Bandwidth Product (V_{CE} = 3.0 V) (I_C = 3.0 mA)	f_T	—	500	—	MHz
Collector Base Capacitance (V_{CE} = 3.0 V) (I_C = 0)	C_{CB}	—	2.0	—	pF
Collector Substrate Capacitance (V_{CS} = 3.0 V) (I_C = 0)	C_{CS}	—	3.3	—	pF

FIGURE 1 — TEST CIRCUIT

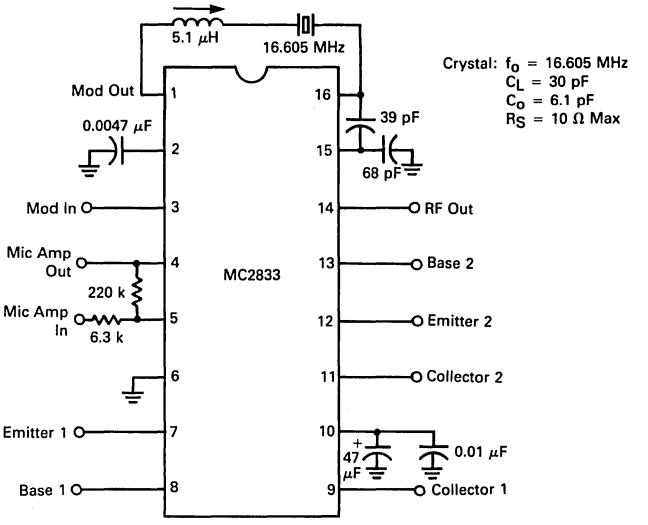
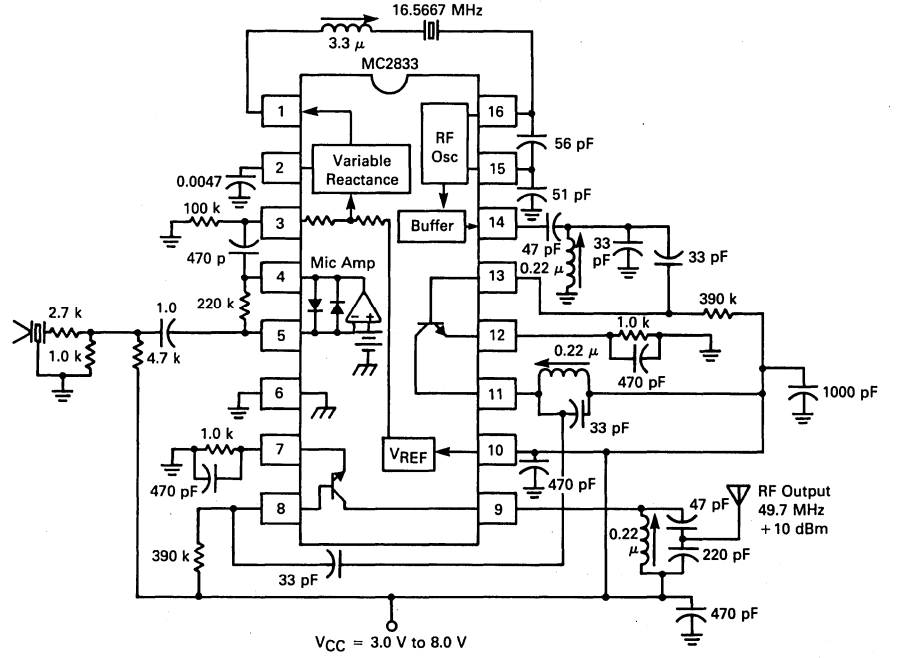


FIGURE 2 — SINGLE CHIP FM VHF TRANSMITTER AT 49.7 MHz



NOTES: The crystal used is fundamental mode, calibrated for parallel resonance with a 32 pF load. The 49.7 MHz output is generated in the output buffer, which is being used as a frequency tripler in this application.
The networks in the output stages provide frequency selectivity and impedance matching at 49.7 MHz.
The RF output is +10 dBm (10 mW into 50 Ω load) at 49.7 MHz, with all harmonics reduced by more than 50 dB.
All capacitors in microfarads, inductors in Henries and resistors in Ohms unless otherwise specified.
0.22 μH inductors are Toko B199SN-T1048Z
3.3 μH inductor is Toko B199KN-T1055Z

MC3356

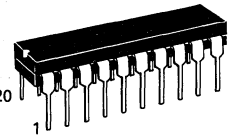
WIDEBAND FSK RECEIVER

. . . includes Oscillator, Mixer, Limiting IF Amplifier, Quadrature Detector, Audio Buffer, Squelch, Meter Drive, Squelch Status output, and Data Shaper comparator. The MC3356 is designed for use in digital data communications equipment.

- Data Rates up to 500 kilobaud
- Excellent Sensitivity: −3 dB Limiting Sensitivity
  30 μVrms @ 100 MHz
- Highly versatile, full-function device, yet few external parts are required

WIDEBAND FSK RECEIVER

MONOLITHIC SILICON INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 738

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM

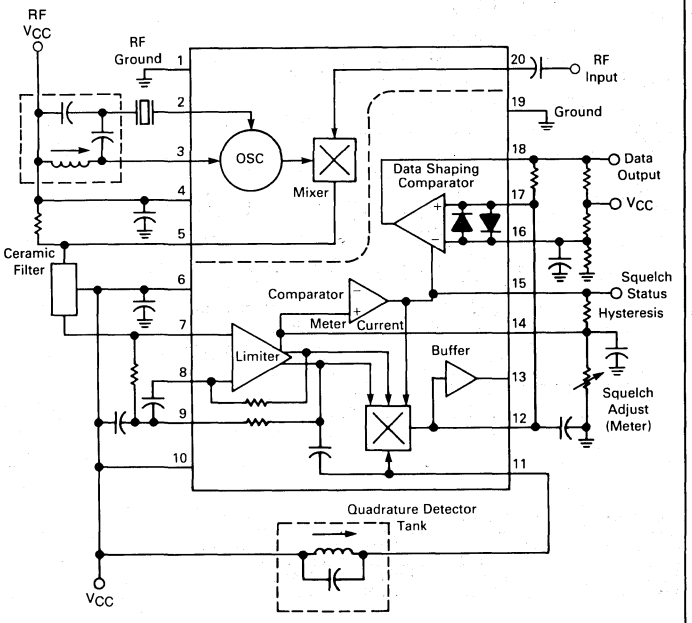
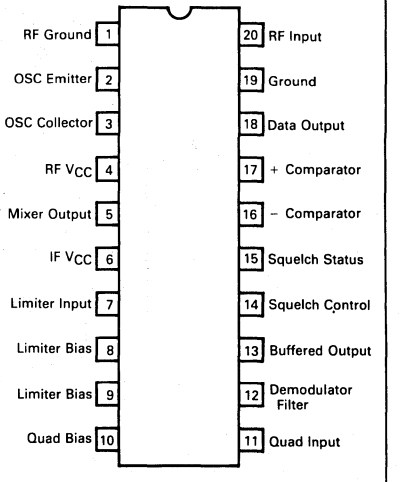


FIGURE 2 — PIN CONNECTIONS



MAXIMUM RATINGS

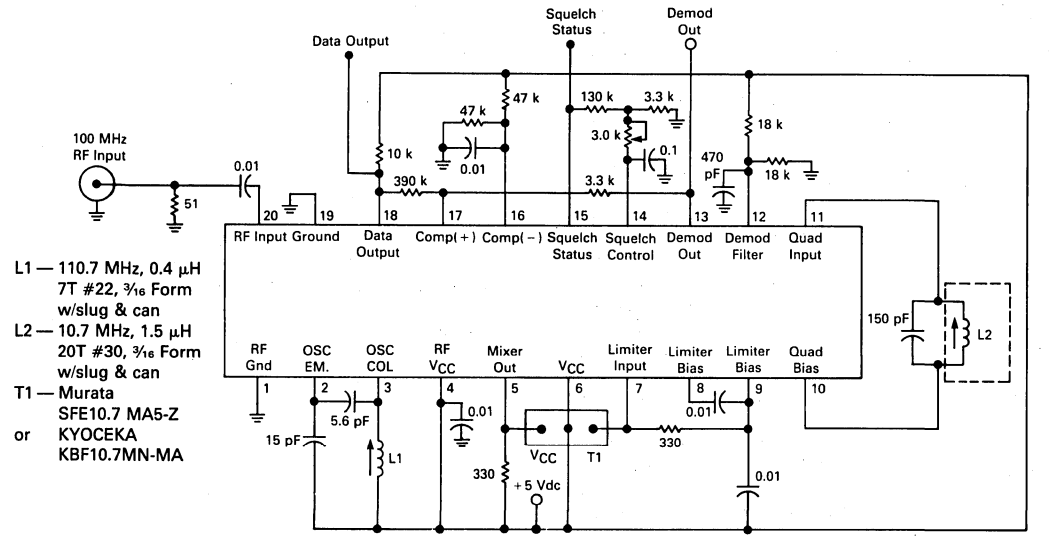
Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Power Supply Voltage Range (Pins 6, 10)	V_{CC}	3.0 to 9.0	Vdc
Operating R.F. Supply Voltage Range (Pin 4)	R.F. V_{CC}	3.0 to 12.0	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 100 MHz, f_{osc} = 110.7 MHz, Δf = ±75 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C, test circuit of Figure 3, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
Drain Current Total, RF V_{CC} and V_{CC}	—	20	25	mAdc
Input for −3 dB limiting	—	30	—	μVrms
Input for 50 dB quieting $\left(\frac{S+N}{N}\right)$	—	60	—	μVrms
Mixer Voltage Gain, Pin 20 to Pin 5	—	2.0	3.0	
Mixer Input Resistance, 100 MHz	—	260	—	Ω
Mixer Input Capacitance, 100 MHz	—	5.0	—	pF
Mixer/Oscillator Frequency Range (Note 1)	—	—	200	MHz
IF/Quadrature Detector Frequency Range (Note 1)	0.2	—	50	MHz
AM Rejection (30% AM, RF V_{in} = 1.0 mVrms)	—	50	—	dB
Demodulator Output, Pin 13	—	0.5	—	Vrms
Meter Drive	—	7.0	—	μA/dB
Squelch Threshold	—	0.8	—	Vdc

Note 1: Not taken in Test Circuit of Figure 3; new component values required.

FIGURE 3 — TEST CIRCUIT



L1 — 110.7 MHz, 0.4 μH
7T #22, 3/16 Form
w/slug & can
L2 — 10.7 MHz, 1.5 μH
20T #30, 3/16 Form
w/slug & can
T1 — Murata
SFE10.7 MA5-Z
or KYOCEKA
KBF10.7MN-MA

FIGURE 4 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

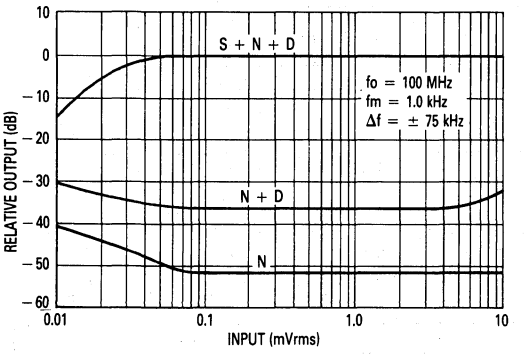
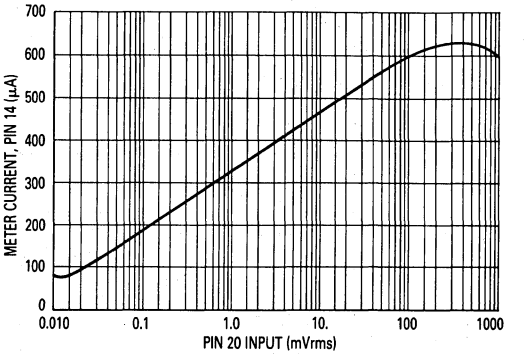


FIGURE 5 — METER CURRENT versus SIGNAL INPUT



General Description

This device is intended for single and double conversion VHF receiver systems, primarily for FSK data transmission up to 500 K baud (250 kHz). It contains an oscillator, mixer, limiting IF, quadrature detector, signal strength meter drive, and data shaping amplifier.

The oscillator is a common base Colpitts type which can be crystal controlled, as shown in Figure 1, or L-C controlled as shown in the other figures. At higher V_{CC}, it has been operated as high as 400 MHz. A mixer/oscillator voltage gain of 2 up to approximately 200 MHz, is readily achievable.

The mixer functions well from an input signal of 10 μVrms, below which the squelch is unpredictable, up to about 10 mVrms, before any evidence of overload. Operation up to 1.0 Vrms input is permitted, but nonlinearity of the meter output is incurred, and some oscillator pulling is suspected. The AM rejection above 10 mVrms is degraded.

The limiting IF is a high frequency type, capable of being operated up to 50 MHz. It is expected to be used at 10.7 MHz in most cases, due to the availability of standard ceramic resonators. The quadrature detector is internally coupled to the IF, and a 5.0 pF quadrature capacitor is internally provided. The −3dB limiting sensitivity of the IF itself is approximately 50 μV (at Pin 7), and the IF can accept signals up to 1.0 Vrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 state limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 10 μV to 100 mVrms. (See Figure 5.)

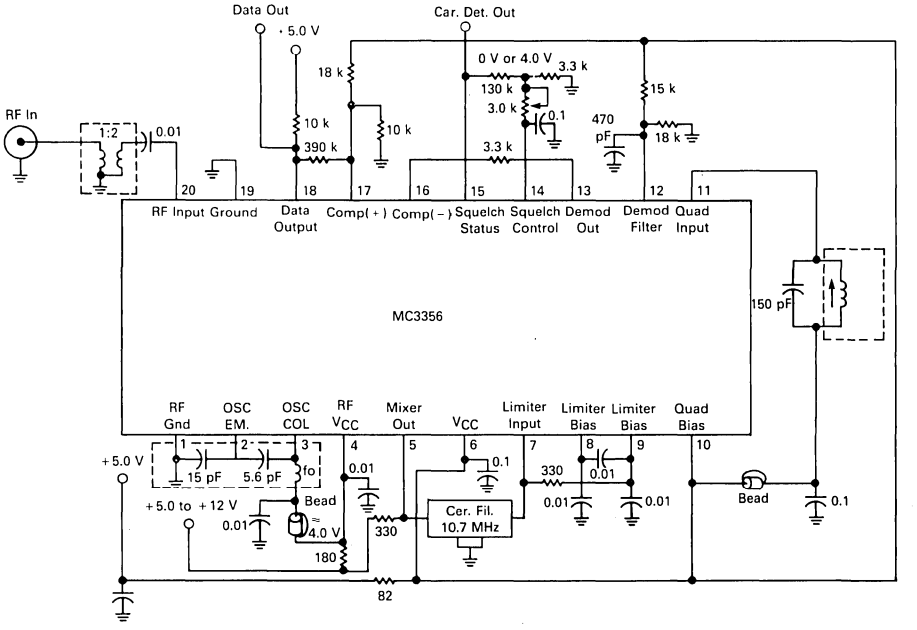
A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator(+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 30 μVrms. The 130 kΩ resistor shown in the test circuit provides a small amount of hysteresis. Its connection between the 3.3 k resistor to ground and the 3.0 k pot, permits adjustment of squelch level without changing the amount of hysteresis.

The squelch is internally connected to both the quadrature detector and the data shaper. The quadrature detector output, when squelched, goes to a dc level approximately equal to the zero signal level, unsquelched. The squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete "floating" comparator, with back to back diodes across its inputs. The output of the quadrature detector can be fed directly to either input of this amplifier to produce an output that is either at V_{CC} or V_{EE}, depending upon the received frequency. The impedance of the biasing can be varied to produce an amplifier which "follows" frequency detuning to some degree, to prevent data pulse width changes.

When the data shaper is driven directly from the demodulator output, Pin 13, there may be distortion at Pin 13 due to the diodes, but this is not important in the data application. A useful note in relating high/low input frequency to logic state: low IF frequency corresponds to low demodulator output. If the oscillator is above the incoming RF frequency, then high RF frequency will produce a logic low. (Input to (+)input of Data Shaper as shown in figures 1 and 3.)

FIGURE 6 — APPLICATION WITH FIXED BIAS ON DATA SHAPER



Application Notes

The MC3356 is a high frequency/high gain receiver that requires following certain layout techniques in designing a stable circuit configuration. The objective is to minimize or eliminate, if possible, any unwanted feedback.

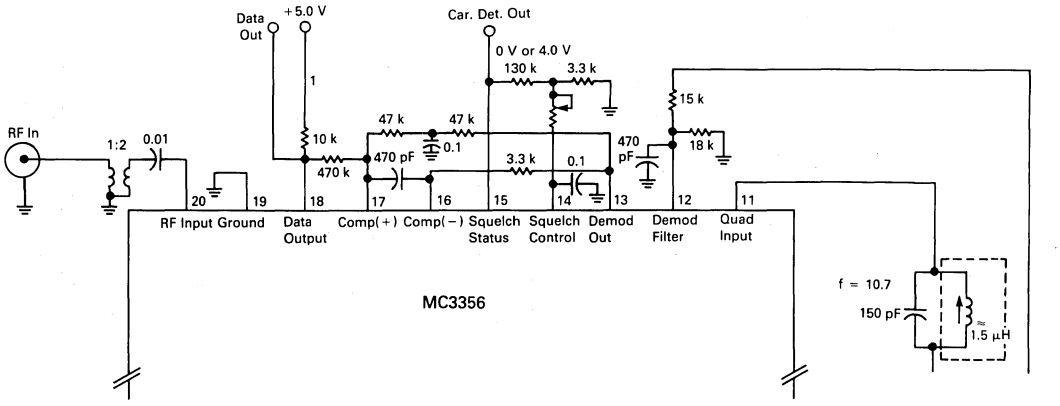
Shielding, which includes the placement of input and output components, is important in minimizing electrostatic or electromagnetic coupling. The MC3356 has its pin connections such that the circuit designer can place the critical input and output circuits on opposite ends of the chip. Shielding is normally required for inductors in tuned circuits.

The MC3356 has separate V_{CC}'s and grounds for the RF and IF sections which allows good external circuit isolation by minimizing common ground paths.

Note that the circuits of figures 1 and 3 have RF, oscillator, and IF circuits predominantly referenced to the plus supply rails. Figure 6, on the other hand, shows a suitable means of ground referencing. The two methods produce identical results when carefully executed. It is important to treat Pin 19 as a ground node for either approach. The RF input should be "grounded" to Pin 1 and then the input and the mixer/oscillator grounds (or RF V_{CC} bypasses) should be connected by a low inductance path to Pin 19. IF and detector sections should also have their bypasses returned by a *separate* path to Pin 19. V_{CC} and RF V_{CC} can be decoupled to minimize feedback, although the configuration of Figure 3 shows a successful implementation on a common 5.0 supply. Once again, the message is: define a supply node and a ground node and return each section to those nodes by separate, low impedance paths.

The test circuit of Figure 3 has a 3 db limiting level of 30 μV which can be lowered 6 db by a 1:2 untuned transformer at the input as shown in figures 6 and 7. For applications that require additional sensitivity, an RF amplifier can be added, but with no greater than 20 db gain. This will give a 2.0 to 2.5 μV sensitivity and any additional gain will reduce receiver dynamic range without improving its sensitivity. Although the test circuit operates at +5.0 V, the mixer/oscillator optimum performance is at +8.0 V to 12 V. A minimum of +8.0 V is recommended in high frequency applications (above 150 MHz), or in PLL applications where the oscillator drives a prescaler.

FIGURE 7 — APPLICATION WITH SELF-ADJUSTING BIAS ON DATA SHAPER

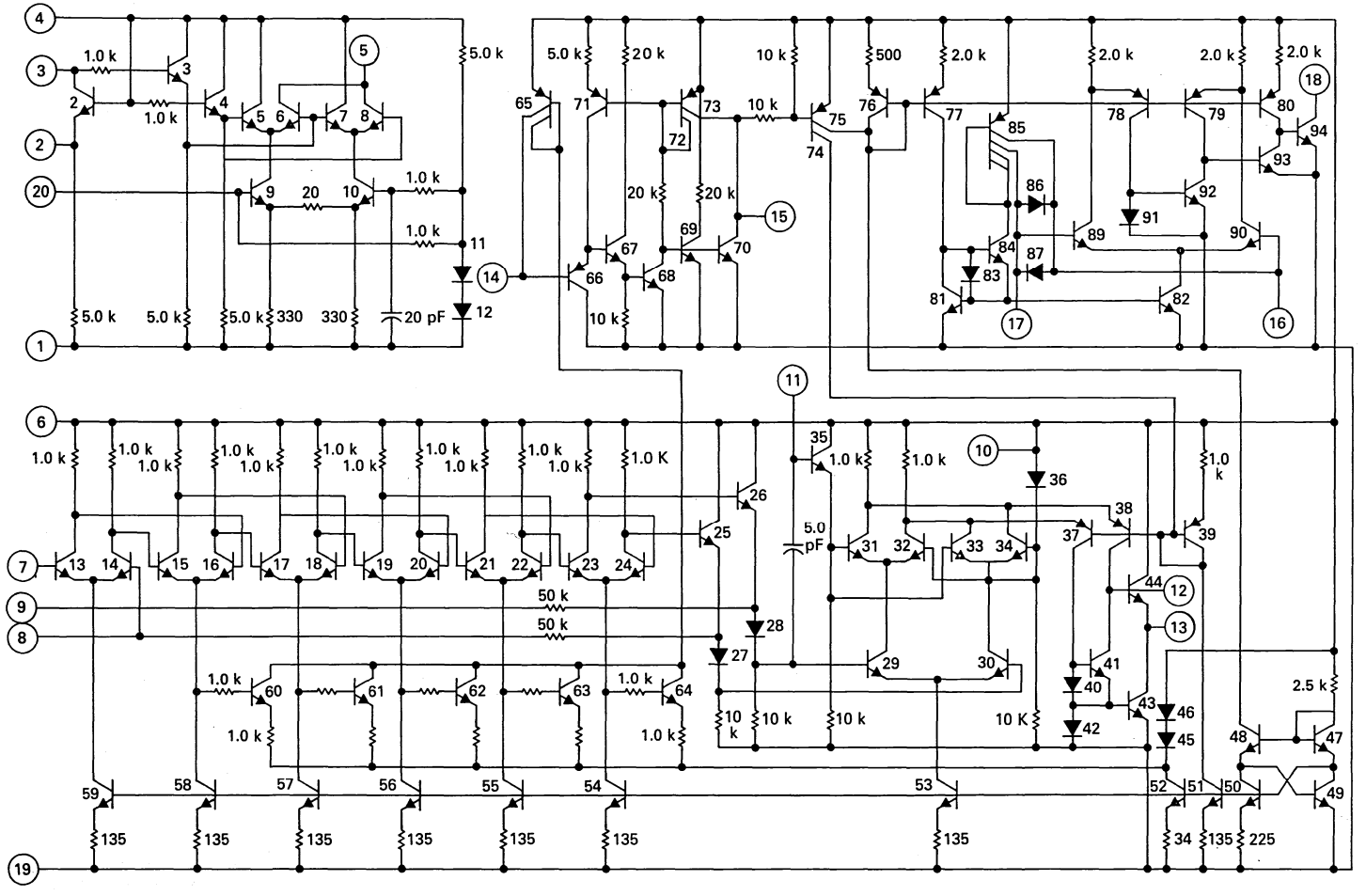


APPLICATION NOTES, continued

Depending on the external circuit, inverted or non-inverted data is available at Pin 18. Inverted data makes the higher frequency in the FSK signal a 'one' when the local oscillator is above the incoming RF. Figure 6 schematic shows the comparator with hysteresis. In this circuit the dc reference voltage at Pin 17 is about the same as the demodulated output voltage (Pin 13) when no signal is present. This type circuit is preferred for systems where the data rates can drop to zero. Some systems have a low frequency limit on the data rate, such as systems using the MC3850 ACIA that has a start or stop bit. This defines the low frequency limit that can appear in the data stream. Figure 6 circuit can then be changed to a circuit configuration as shown in Figure 7. In Figure 7 the reference voltage for the comparator is derived from the demodulator output through a low pass circuit where τ is much lower than the lowest frequency data rate. This and similar circuits will compensate for small tuning changes (or drift) in the quadrature detector.

Squelch status (Pin 15) goes high (squelch off) when the input signal becomes greater than some preset level set by the resistance between Pin 14 and ground. Hysteresis is added to the circuit externally by the resistance from Pin 14 to Pin 15.

FIGURE 8 — INTERNAL SCHEMATIC



MC3357

LOW POWER NARROW BAND FM IF

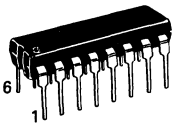
. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typ) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage — (-3.0 dB) = 5.0 μV (Typ)
- Low Number of External Parts Required

NOT RECOMMENDED FOR NEW DESIGNS

LOW POWER FM IF

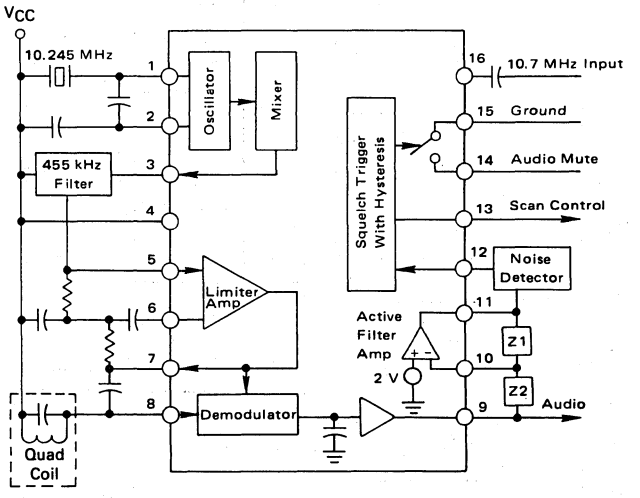
SILICON MONOLITHIC INTEGRATED CIRCUIT



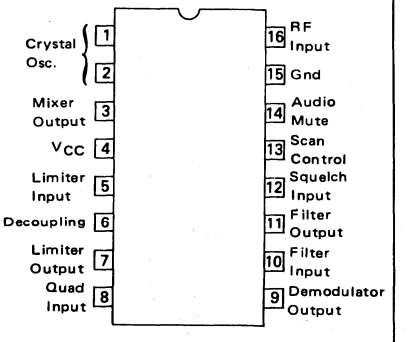
P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
SO-16

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



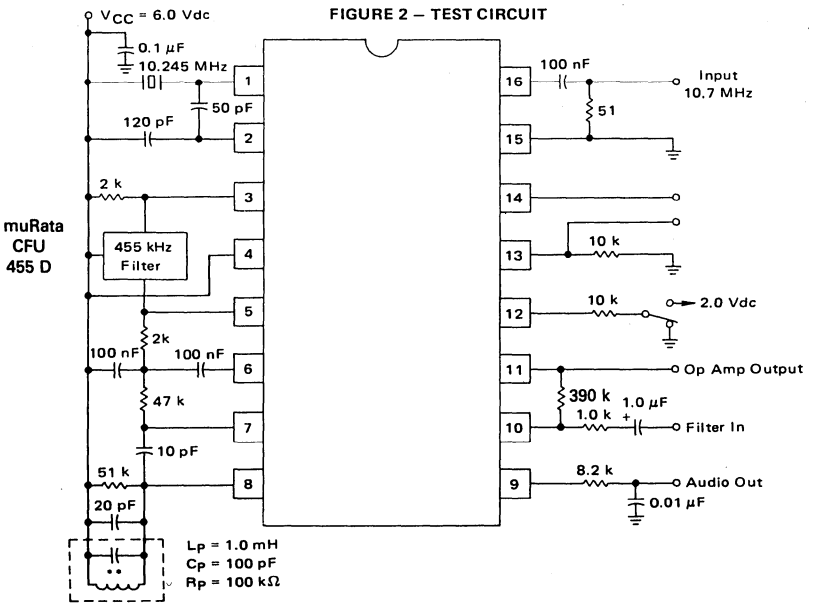
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 8	Vdc
Detector Input Voltage	8	–	1.0	Vp-p
Input Voltage (V_{CC} ≥ 6.0 Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	-0.5 to 5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	-30 to +70	°C
Storage Temperature Range	–	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, f_o = 10.7 MHz, Δf = ± 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current	4				mA
Squelch Off		–	2.0	–	
Squelch On		–	3.0	5.0	
Input Limiting Voltage (-3 dB Limiting)	16	–	5.0	10	μV
Detector Output Voltage	9	–	3.0	–	Vdc
Detector Output Impedance	–	–	400	–	Ω
Recovered Audio Output Voltage (V_{in} = 10 mV)	9	200	350	–	mVrms
Filter Gain (10 kHz) (V_{in} = 5 mV)	–	40	46	–	dB
Filter Output Voltage	11	1.8	2.0	2.5	Vdc
Trigger Hysteresis	–	–	100	–	mV
Mute Function Low	14	–	15	50	Ω
Mute Function High	14	1.0	10	–	MΩ
Scan Function Low (Mute Off) (V_{12} = 2 Vdc)	13	–	0	0.5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	5.0	–	–	Vdc
Mixer Conversion Gain	3	–	20	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	2.2	–	pF

FIGURE 2 – TEST CIRCUIT



CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer-oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly-balanced to reduce spurious responses. The input impedance at Pin 16 is set by a 3.0 kΩ internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at Pin 3 must be dc connected to B+, below which it can swing 0.5 V.

After suitable bandpass filtering (ceramic or LC) the signal goes to the input of a five-stage limiter at Pin 5. The output of the limiter at Pin 7 drives a multiplier, both internally directly, and externally through a quadrature coil, to detect the FM. The output at Pin 7 is also used to supply dc feedback to Pin 5. The other side of the first limiter stage is decoupled at Pin 6.

The recovered audio is partially filtered, then buffered giving an impedance of around 400 Ω at Pin 9. The signal still requires de-emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at Pin 11 providing dc bias (externally) to the input at Pin 10 which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that Pin 13 is low at an impedance level of around 60 kΩ, and the audio mute (Pin 14) is open circuit. If Pin 12 is pulled down to 0.7 V by the noise or tone detector, Pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 μA and Pin 14 is internally short-circuited to ground. There is 100 mV of hysteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to a high-impedance ground-reference point in the audio path between Pin 9 and the audio amplifier.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

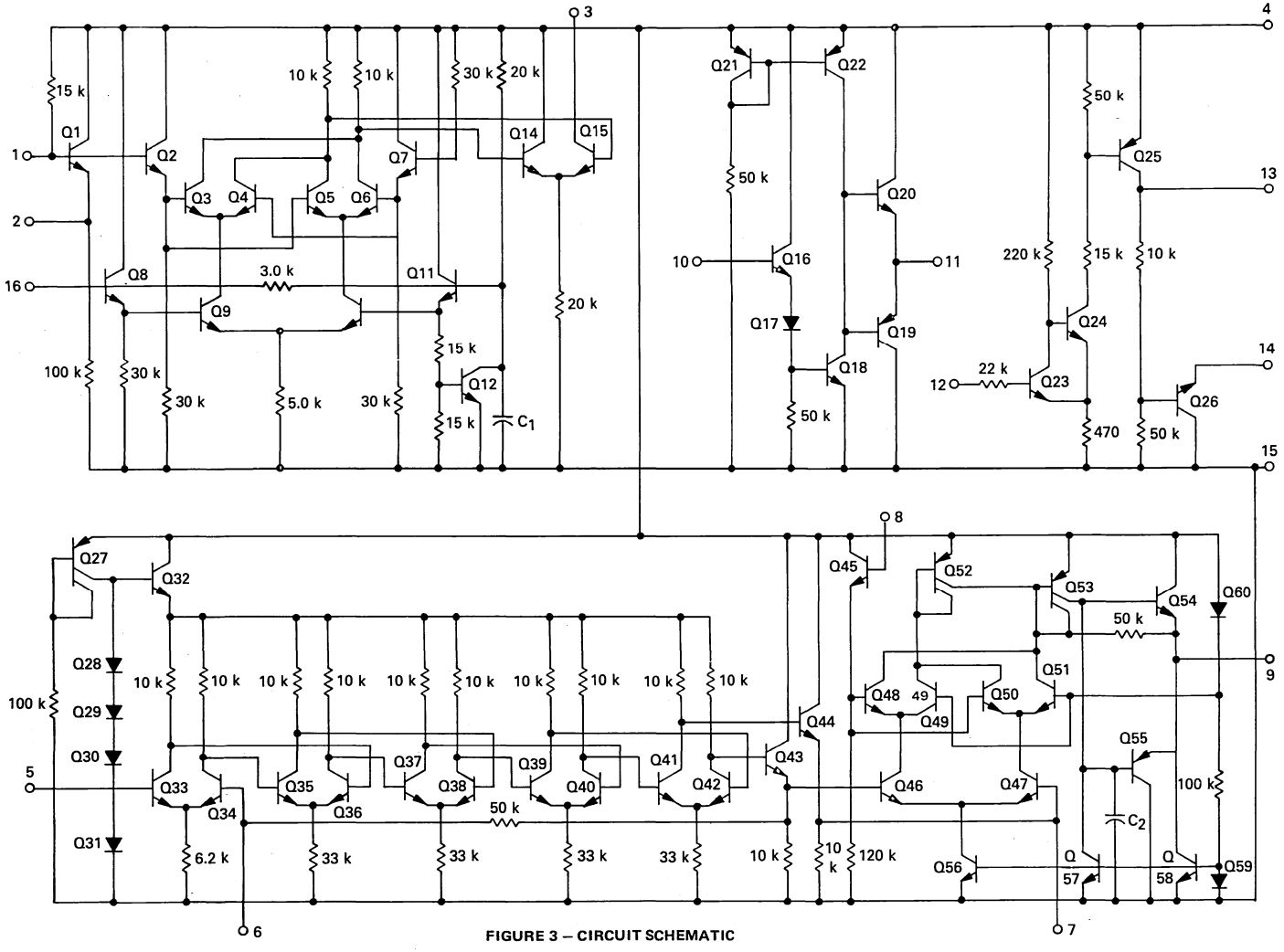


FIGURE 3 – CIRCUIT SCHEMATIC

MC3359

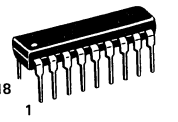
HIGH GAIN LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

LOW POWER NARROWBAND FM IF

. . . includes oscillator, mixer, limiting amplifier, AFC, quadrature discriminator, op/amp, squelch, scan control, and mute switch. The MC3359 is designed to detect narrowband FM signals using a 455 kHz ceramic filter for use in FM dual conversion communications equipment. The MC3359 is similar to the MC3357 except that the MC3359 has an additional limiting IF stage, an AFC output, and an opposite polarity Broadcast Detector. The MC3359 also requires fewer external parts.

- Low Drain Current: 3.6 mA (Typ) @ V_{CC} = 6.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage — −3.0 dB = 2.0 μV (Typ)
- Low Number of External Parts Required



P SUFFIX
PLASTIC PACKAGE
CASE 707

DW SUFFIX
PLASTIC PACKAGE
CASE 751D

FIGURE 1 — TYPICAL APPLICATION IN A SCANNER RECEIVER

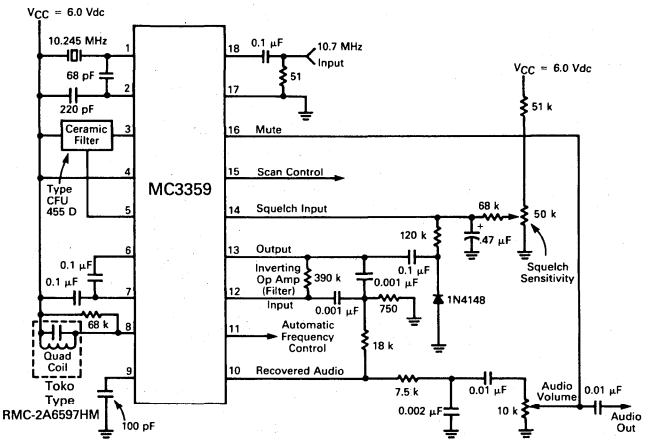
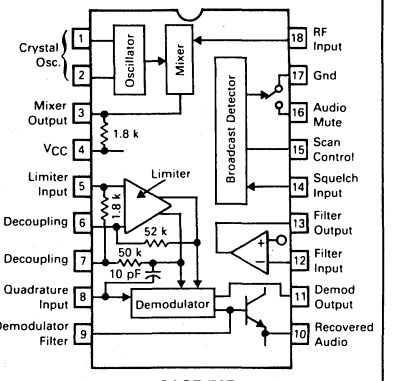
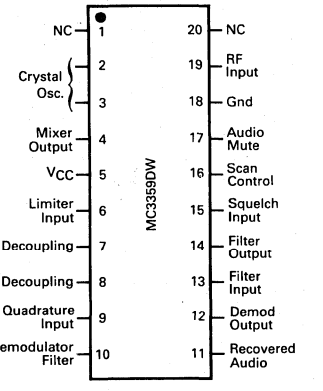


FIGURE 2 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



CASE 707



CASE 751D

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 9	Vdc
Input Voltage (V_{CC}≥ 6.0 Volts)	18	V_{18}	1.0	V_{rms}
Mute Function	16	V_{16}	−0.7 to 12	V_{pk}
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +70	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, f_o = 10.7 MHz, Δf = ±3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C test circuit of Figure 3, unless otherwise noted)

Characteristics		Min	Typ	Max	Units
Drain Current (Pins 4 and 8)	Squelch Off Squelch On	— —	3.6 5.4	6.0 7.0	mA
Input for 20 dB Quieting		—	8.0	—	μVrms
Input for −3.0 dB Limiting		—	2.0	—	μVrms
Mixer Voltage Gain (Pin 18 to Pin 3, Open)		—	46	—	
Mixer Third Order Intercept, 50 Ω Input		—	−1.0	—	dBm
Mixer Input Resistance		—	3.6	—	kΩ
Mixer Input Capacitance		—	2.2	—	pF
Recovered Audio, Pin 10 (Input Signal 1.0 mVrms)		450	700	—	mVrms
Detector Center Frequency Slope, Pin 10		—	0.3	—	V/kHz
AFC Center Slope, Pin 11, Unloaded		—	12	—	V/kHz
Filter Gain (test circuit of Figure 3)		40	51	—	dB
Squelch Threshold, Through 10K to Pin 14		—	0.62	—	Vdc
Scan Control Current, Pin 15	Pin 14 — High — Low	— 2.0	0.01 2.4	1.0 —	μA mA
Mute Switch Impedance Pin 16 to Ground	Pin 14 — High — Low	—	5.0 1.5	10 —	Ω MΩ

FIGURE 3 — TEST CIRCUIT

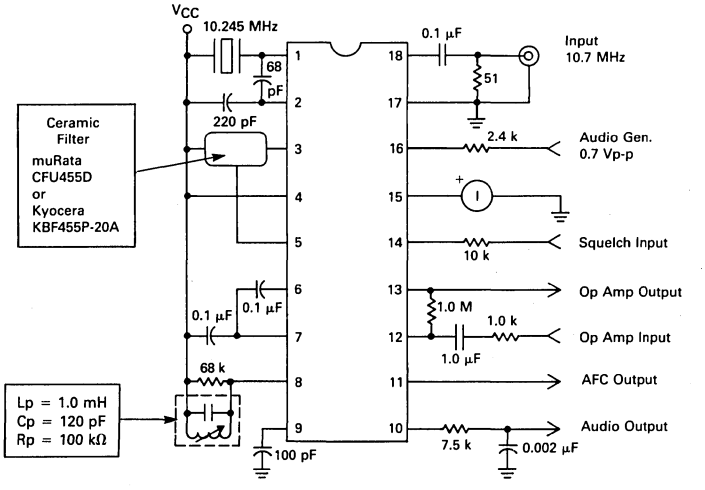


FIGURE 4 — MIXER VOLTAGE GAIN

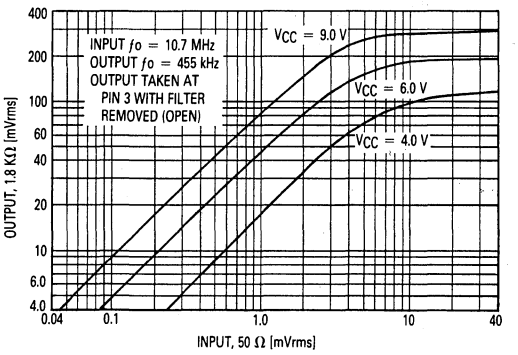


FIGURE 5 — LIMITING I.F. FREQUENCY RESPONSE

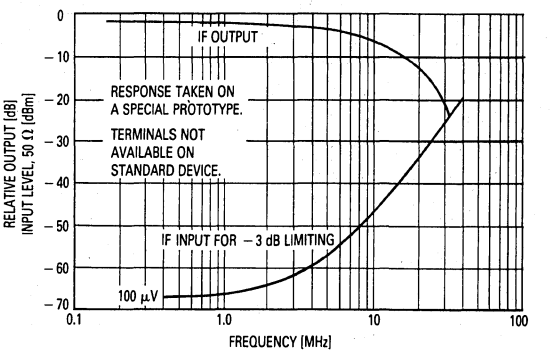


FIGURE 6 — MIXER THIRD ORDER INTERMODULATION PERFORMANCE

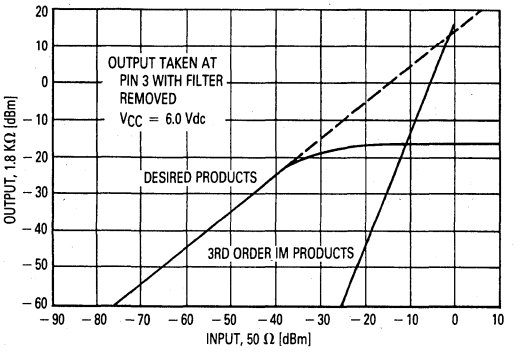


FIGURE 7 — DETECTOR AND AFC RESPONSES

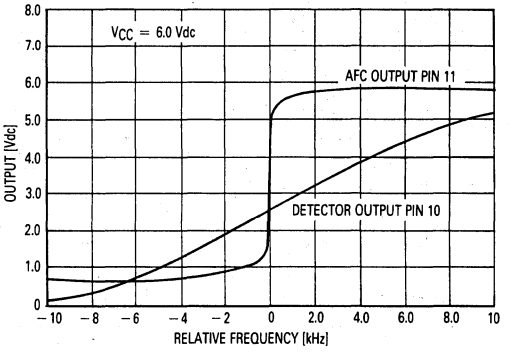


FIGURE 8 — RELATIVE MIXER GAIN

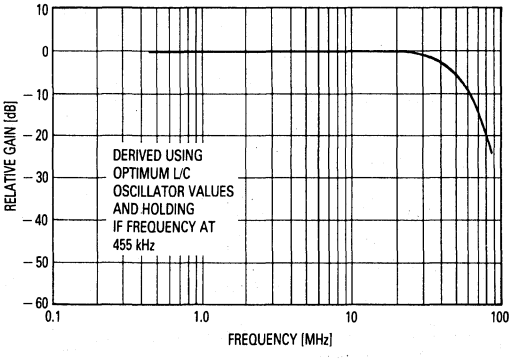


FIGURE 9 — OVERALL GAIN, NOISE, AND A.M. REJECTION

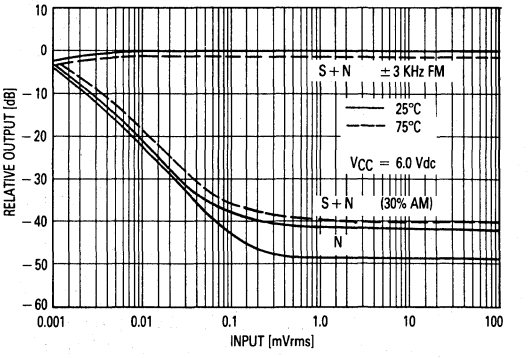


FIGURE 10 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

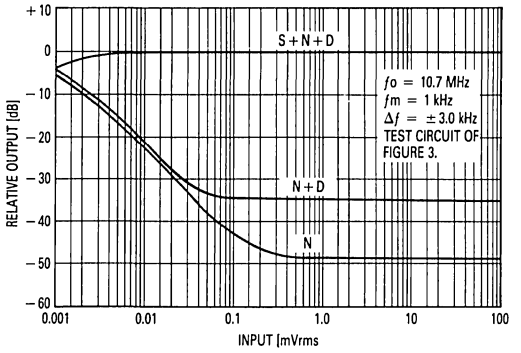


FIGURE 11 — AUDIO OUTPUT AND TOTAL CURRENT DRAIN versus SUPPLY VOLTAGE

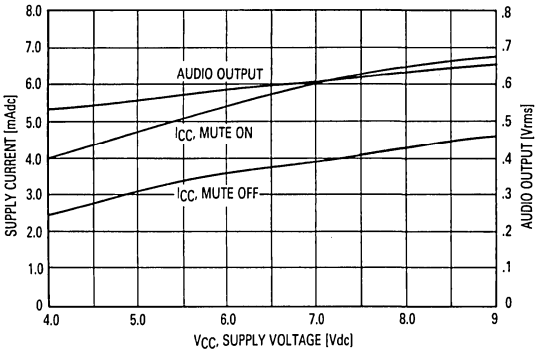


FIGURE 12 — L/C OSCILLATOR, TEMPERATURE AND POWER SUPPLY SENSITIVITY

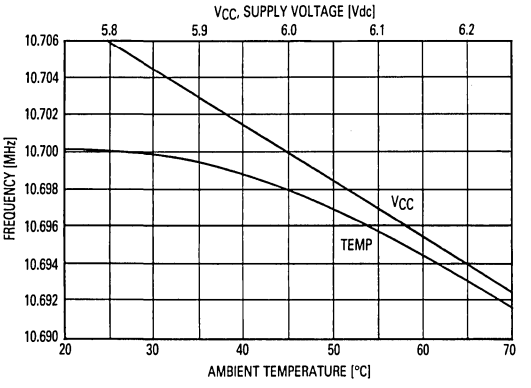


FIGURE 13 — OP AMP GAIN AND PHASE RESPONSE

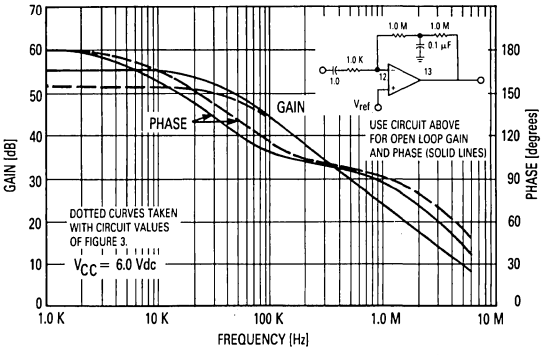


FIGURE 14 — L/C OSCILLATOR RECOMMENDED COMPONENT VALUES

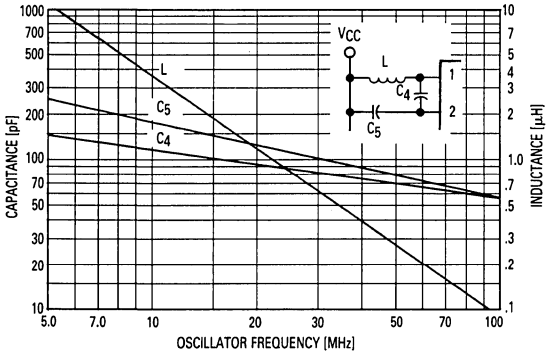
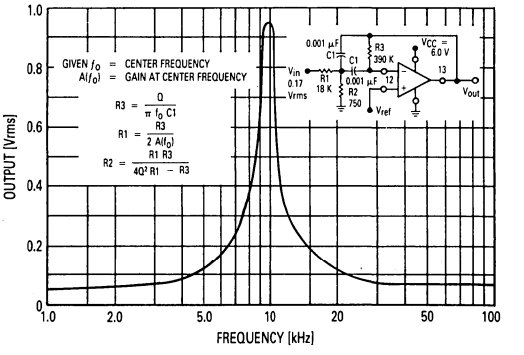


FIGURE 15 — THE OP AMP AS A BANDPASS FILTER



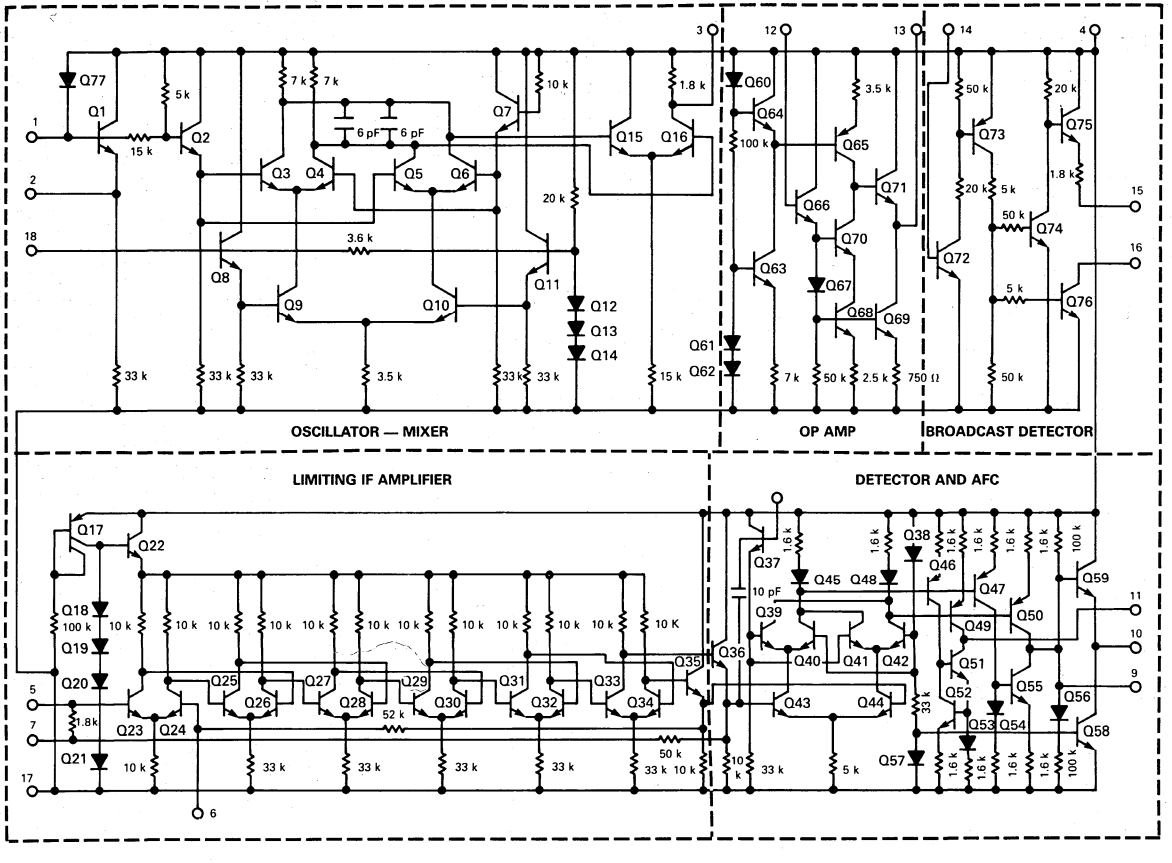


FIGURE 16 — CIRCUIT SCHEMATIC

CIRCUIT DESCRIPTION

The MC3359 is a low-power FM IF circuit designed primarily for use in voice-communication scanning receivers. It is also finding a place in narrowband data links.

In the typical application (Figure 1), the mixer-oscillator combination converts the input frequency (10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch-trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

APPLICATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pin 4, 1, and 2, respectively. The crystal is used in fundamental mode, calibrated for parallel resonance at 32 pF load capacitance. In theory this means that the two capacitors in series should be 32 pF, but in fact much larger values do not significantly affect the oscillator frequency, and provide higher oscillator output.

The oscillator can also be used in the conventional L/C Colpitts configuration without loss of mixer conversion gain. This oscillator is, of course, much more sensitive to voltage and temperature as shown in Figure 12. Guidelines for choosing L and C values are given in Figure 14.

The mixer is doubly balanced to reduce spurious responses. The mixer measurements of Figure 4 and 6 were made using an external 50 Ω source and the internal 1.8 k at Pin 3. Voltage gain curves at several V_{CC} voltages are shown in Figure 4. The Third Order Intercept curves of Figure 6 are shown using the conventional dBm scales. Measured power gain (with the 50 Ω input) is approximately 18 dB but the useful gain is much higher because the mixer input impedance is over 3 kΩ. Most applications will use a 330 Ω 10.7 MHz crystal filter ahead of the mixer. For higher frequencies, the relative mixer gain is given in Figure 8.

Following the mixer, a ceramic bandpass filter is recommended. The 455 kHz types come in bandwidths from ±2 kHz to ±15 kHz and have input and output impedances of 1.5 k to 2.0 k. For this reason, the Pin 5 input to the 6 stage limiting IF has an internal 1.8 k resistor. The IF has a 3 dB limiting sensitivity of approximately 100 μV at Pin 5 and a useful frequency range of about 5 MHz as shown in Figure 5. The frequency limitation is due to the high resistance values in the IF, which were necessary to meet the low power requirement. The output of the limiter is internally connected to the quadrature detector, including the 10 pF quadrature capacitor. Only a parallel L/C is needed externally from Pin 8 to V_{CC}. A shunt resistance can be added to widen the peak separation of the quadrature detector.

The detector output is amplified and buffered to the audio output, Pin 10, which has an output impedance of approximatley 300 Ω. Pin 9 provides a high impedance (50 k) point in the output amplifier for application of a filter or de-emphasis capacitor. Pin 11 is the AFC output, with high gain and high output impedance (1 M). If not needed, it should be grounded, or it can be connected to Pin 9 to double the recovered audio. The detector and AFC responses are shown in Figure 7.

Overall performance of the MC3359 from mixer input to audio output is shown in Figure 9 and 10. The MC3359 can also be operated in "single conversion" equipment; i.e., the mixer can be used as a 455 kHz amplifier. The oscillator is disabled by connecting Pin 1 to Pin 2. In this mode the overall performance is identical to the 10.7 MHz results of Figure 9.

A simple inverting op amp is provided with an output at Pin 13 providing dc bias (externally) to the input at Pin 12, which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of either noise above the normal audio, or a tone signal.

The open loop response of this op amp is given in Figure 13. Bandpass filter design information is provided in Figure 15.

A low bias to Pin 14 sets up the squelch-trigger circuit such that Pin 15 is high, a source of at least 2.0 mA, and the audio mute (Pin 16) is open-circuit. If Pin 14 is raised to 0.7 V by the noise or tone detector, Pin 15 becomes open circuit and Pin 16 is internally short circuited to ground. There is no hysteresis. Audio muting is accomplished by connecting Pin 16 to a high-impedance ground-reference point in the audio path between Pin 10 and the audio amplifier. No dc voltage is needed, in fact it is not desirable because audio "thump" would result during the muting function. Signal swing greater than 0.7 V below ground on Pin 16 should be avoided.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3361B

Advance Information

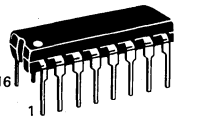
LOW POWER NARROWBAND FM IF

The MC3361B includes an Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. This device is designed for use in FM dual conversion communications equipment.

- Operates From 2.0 V to 8.0 V Supply
- Low Drain Current 3.9 mA Typ @ V_{CC} = 4.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage — −3.0 dB = 2.6 μV Typ
- Low Number of External Parts Required
- Operating Frequency Up to 60 MHz

LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

PIN CONNECTIONS

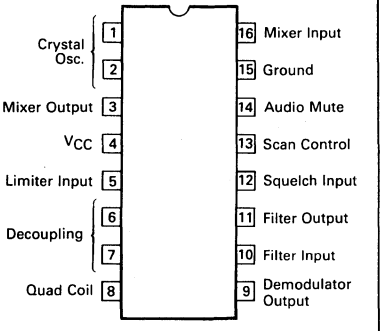
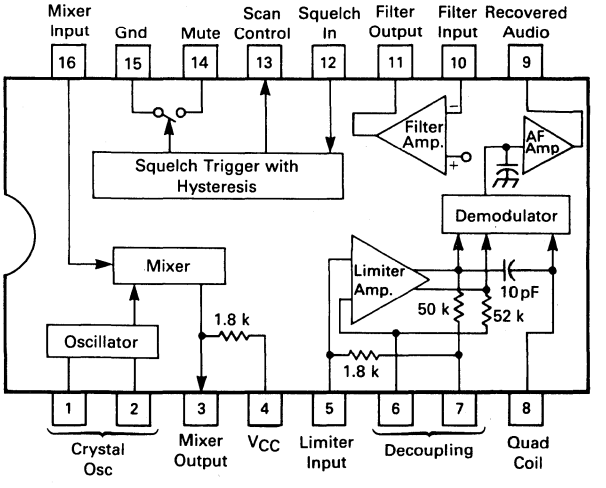


FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

MC3361BD	−30° to +70°C	SO-16
MC3361BP		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

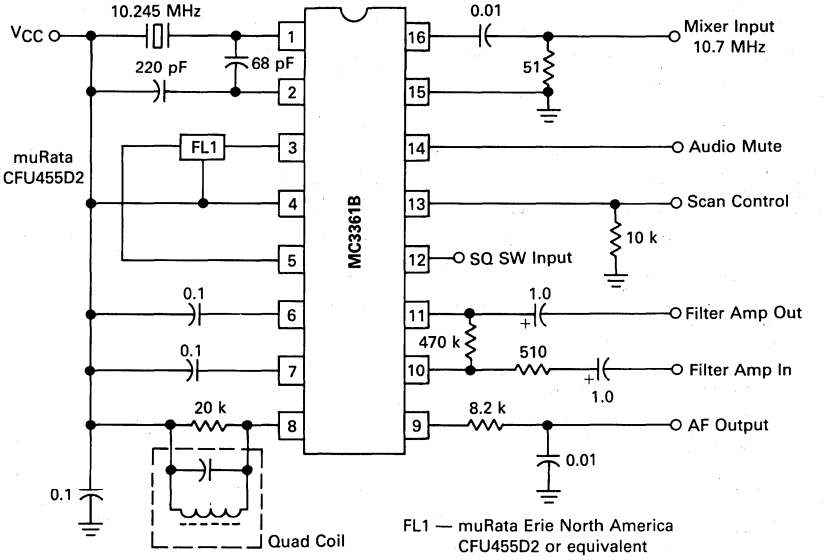
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
Operating Supply Voltage Range	4	V_{CC}	2.0 to 8.0	Vdc
Detector Input Voltage	8	—	1.0	Vp-p
Input Voltage ($V_{CC} \geq$ 4.0 Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	−0.5 to +5.0	V_{pk}
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +70	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 10.7 MHz, Δf = ±3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current (No Signal)	4				mA
Squelch Off		2.9	3.9	4.9	
Squelch On		4.4	5.4	6.4	
Recovered Audio Output Voltage (V_{in} = 10 mV_{RMS})	9	130	160	200	mV_{RMS}
Input Limiting Voltage (−3.0 dB Limiting)	16	—	2.6	6.0	μV
Total Harmonic Distortion	9	—	0.86	—	%
Recovered Output Voltage (No Input Signal)	9	60	120	250	mV_{RMS}
Drop Voltage AF Gain Loss	9	−3.0	−0.6	—	dB
Detector Output Impedance	—	—	450	—	Ω
Filter Gain (10 kHz) (V_{in} = 0.3 mV_{RMS})	—	40	50	—	dB
Filter Output Voltage	11	1.0	1.3	1.6	Vdc
Mute Function Low	14	—	30	50	Ω
Mute Function High	14	1.0	11	—	MΩ
Scan Function Low (Mute Off) (V_{12} = 1.0 Vdc)	13	—	0	0.4	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	3.0	3.5	—	Vdc
Trigger Hysteresis	—	—	45	100	mV
Mixer Conversion Gain	3	—	28	—	dB
Mixer Input Resistance	16	—	3.3	—	kΩ
Mixer Input Capacitance	16	—	2.2	—	pF

FIGURE 2 — TEST CIRCUIT



FL1 — muRata Erie North America CFU455D2 or equivalent

Quadrature Coil — Toko America Type 7MC-8128Z or equivalent

C — μF, unless noted

FIGURE 3 — AUDIO OUTPUT, DISTORTION versus SUPPLY VOLTAGE

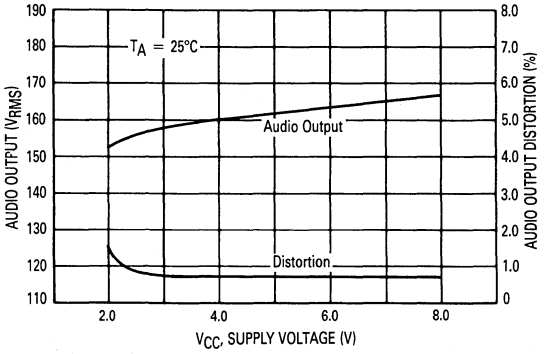
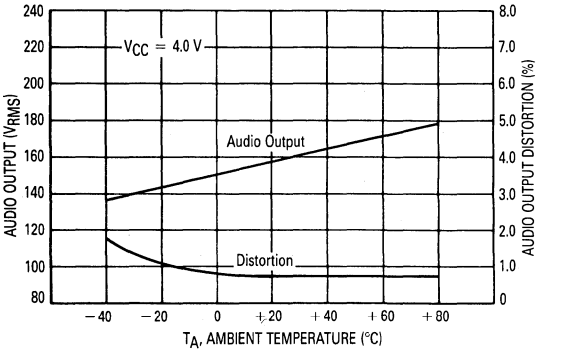


FIGURE 4 — AUDIO OUTPUT, DISTORTION versus TEMPERATURE



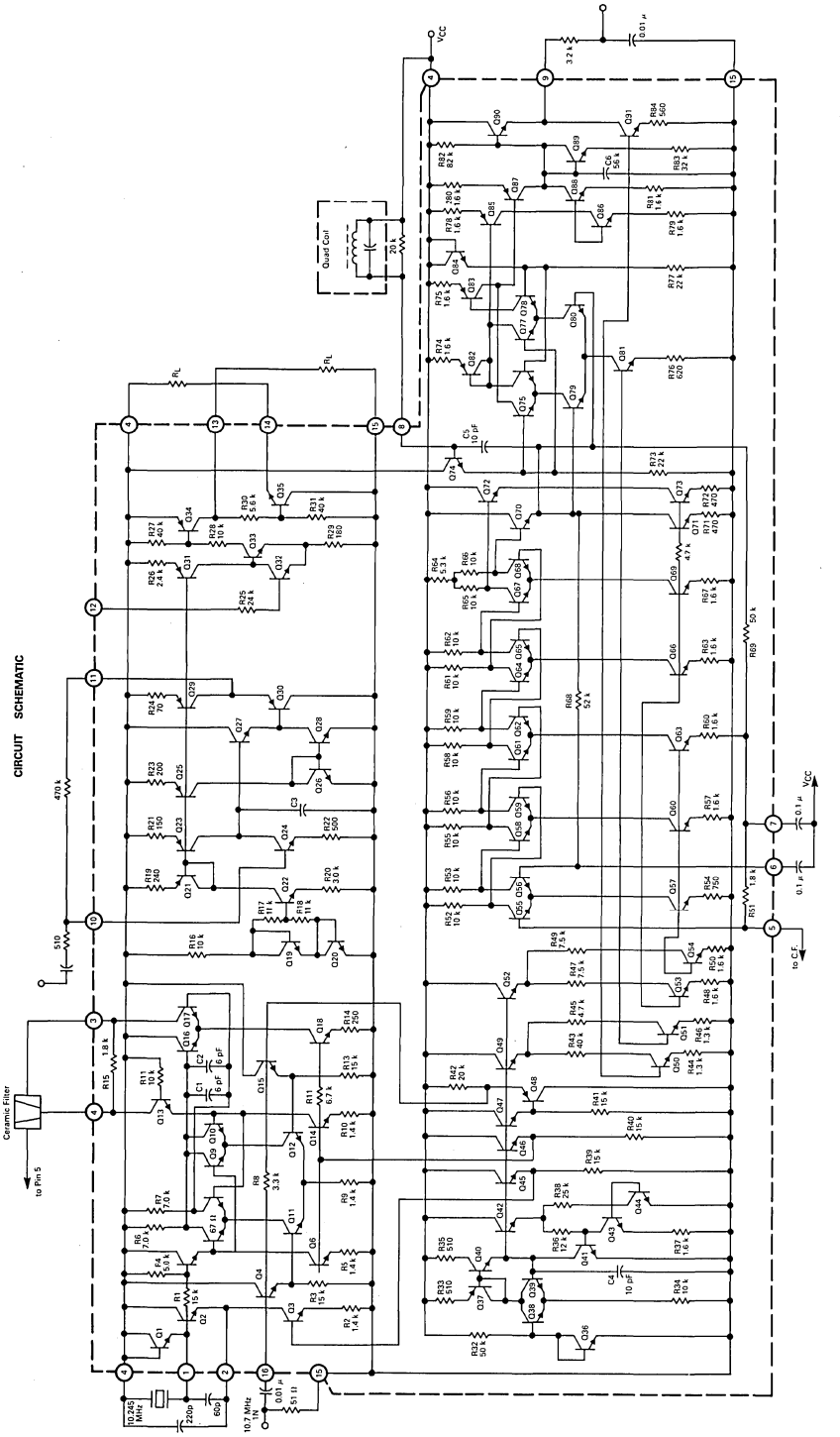


FIGURE 5 — LOW VOLTAGE LOW POWER NARROW BAND FM IF

FIGURE 6 — INPUT LIMITING VOLTAGE

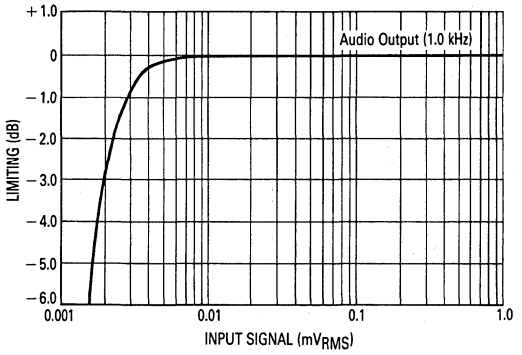


FIGURE 7 — OVERALL GAIN, NOISE, AND AM REJECTION

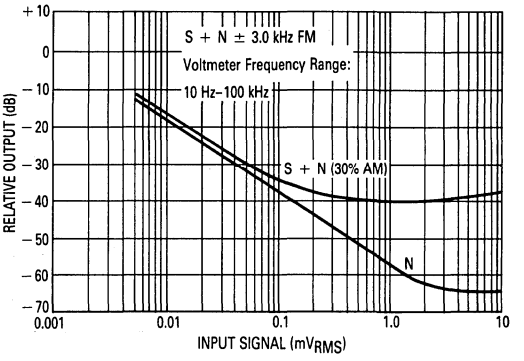


FIGURE 8 — FILTER AMP RESPONSE

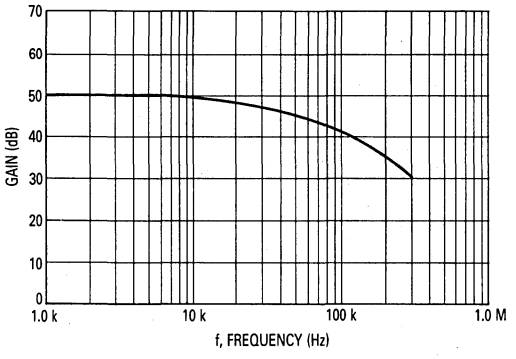


FIGURE 9 — FILTER AMP GAIN

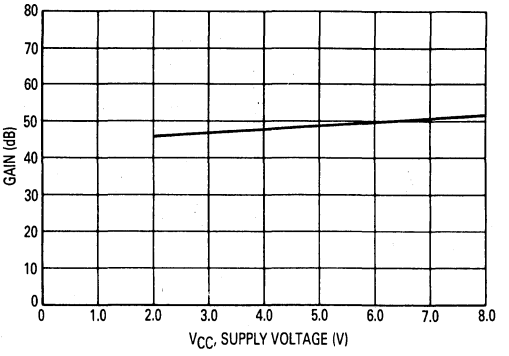


FIGURE 10 — SUPPLY CURRENT

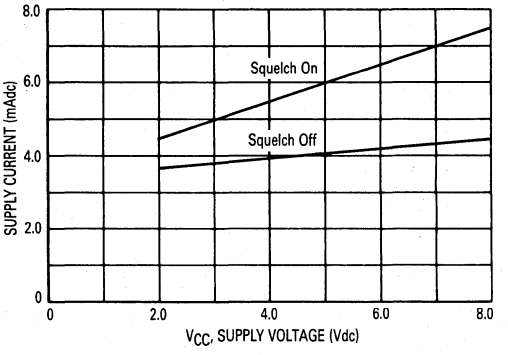
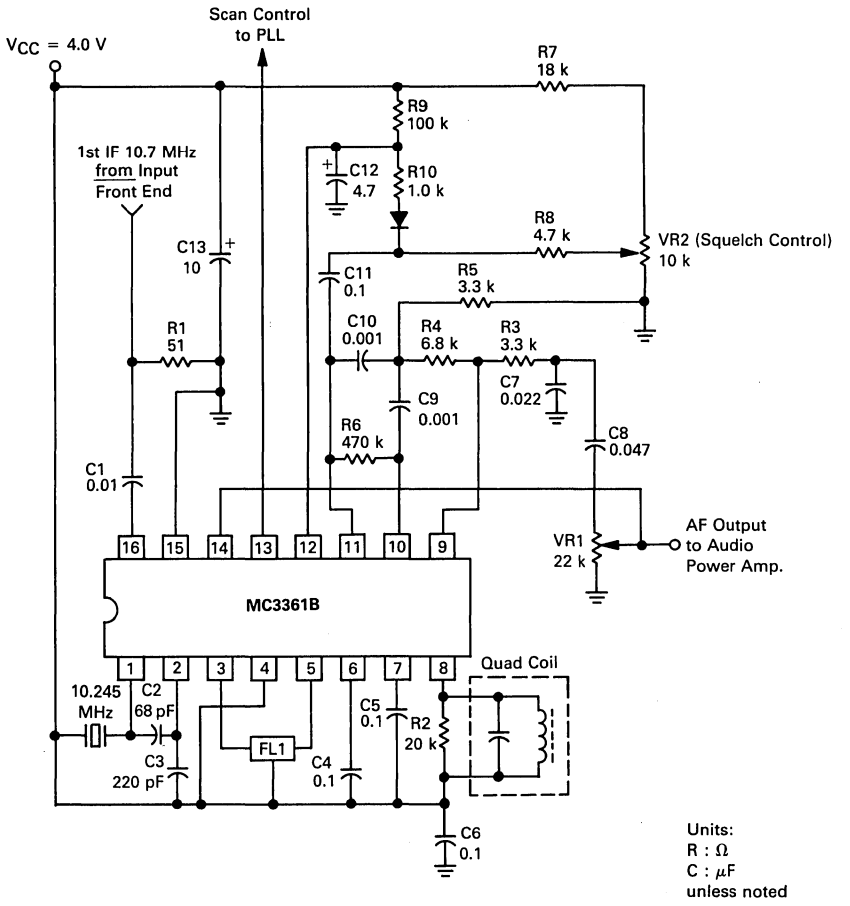


FIGURE 11 — TYPICAL APPLICATION



FL1 — muRata Erie North America
Type CFU455D2 or equivalent

Quadrature Coil — Toko America
Type 7MC-8128Z or equivalent

MC3362

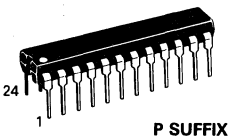
LOW POWER NARROWBAND FM RECEIVER

. . . includes dual FM conversion with oscillators, mixers, quadrature detector, and meter drive/carrier detect circuitry. The MC3362 also has buffered first and second local oscillator outputs and a comparator circuit for FSK detection.

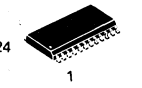
- Wide Input Bandwidth:
  - — 200 MHz using Internal Local Oscillator
  - — 450 MHz using External Local Oscillator
- Complete Dual Conversion Circuitry
- Low Voltage: V_{CC} = 2.0 to 7.0 Vdc
- Low Drain Current (3.6 mA (Typ) @ V_{CC} = 3.0 Vdc)
- Excellent Sensitivity: Input 0.7 μV (Typ) for 12 dB SINAD
- Data Shaping Comparator
- Received Signal Strength Indicator (RSSI) with 60 dB Dynamic Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC Process Technology

LOW-POWER DUAL CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 724



DW SUFFIX
PLASTIC PACKAGE
CASE 751E
SO-24

FIGURE 1 — TYPICAL APPLICATION IN A PLL FREQUENCY SYNTHESIZED RECEIVER

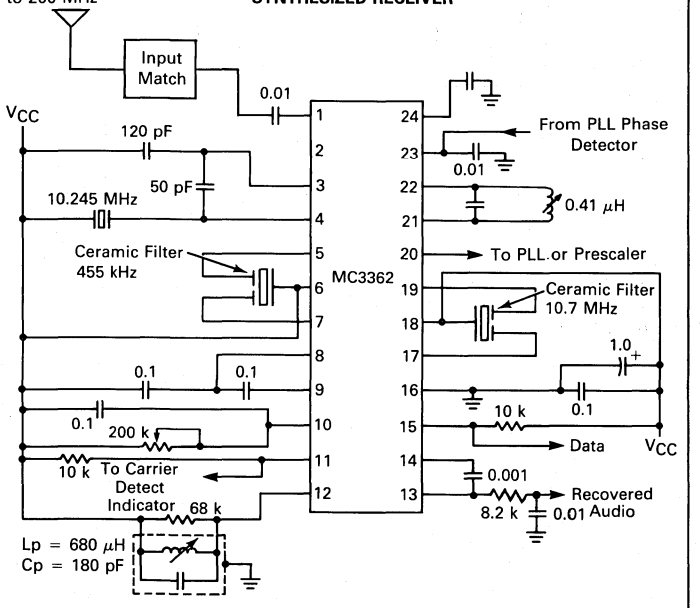
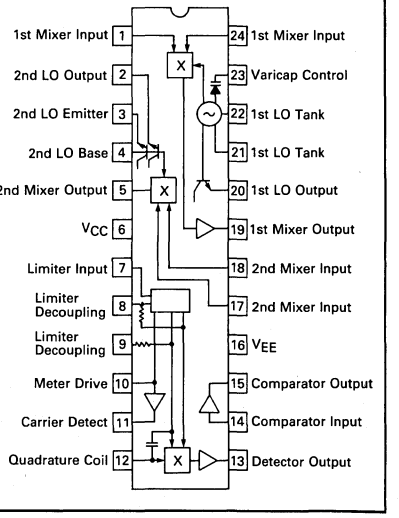


FIGURE 2 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	6	$V_{CC(max)}$	8.0	Vdc
Operating Supply Voltage Range (Recommended)	6	V_{CC}	2.0 to 7.0	Vdc
Input Voltage ($V_{CC} \geq$ 5.0 Vdc)	1, 24	V_{1-24}	1.0	Vrms
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−40 to +85	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 3 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
Drain Current (Carrier Detect Low — See Figure 5)	6	—	4.5	7.0	mA
Input for −3.0 dB Limiting	—	—	0.7	2.0	μVrms
Recovered Audio (RF signal level = 10 mV)	13	—	350	—	mVrms
Noise Output (RF signal level = 0 mV)	13	—	250	—	mVrms
Carrier Detect Threshold (below V_{CC})	10	—	0.64	—	Vdc
Meter Drive Slope	10	—	100	—	nA/dB
Input for 20 dB (S+N)/N (See Figure 7)	—	—	0.7	—	μVrms
First Mixer 3rd Order Intercept (Input)	—	—	−22	—	dBm
First Mixer Input Resistance (Rp)	—	—	690	—	Ω
First Mixer Input Capacitance (Cp)	—	—	7.2	—	pF
First Mixer Conversion Voltage Gain	—	—	18	—	dB
Second Mixer Conversion Voltage Gain	—	—	21	—	dB
Detector Output Resistance	13	—	1.4	—	kΩ

FIGURE 3 — TEST CIRCUIT

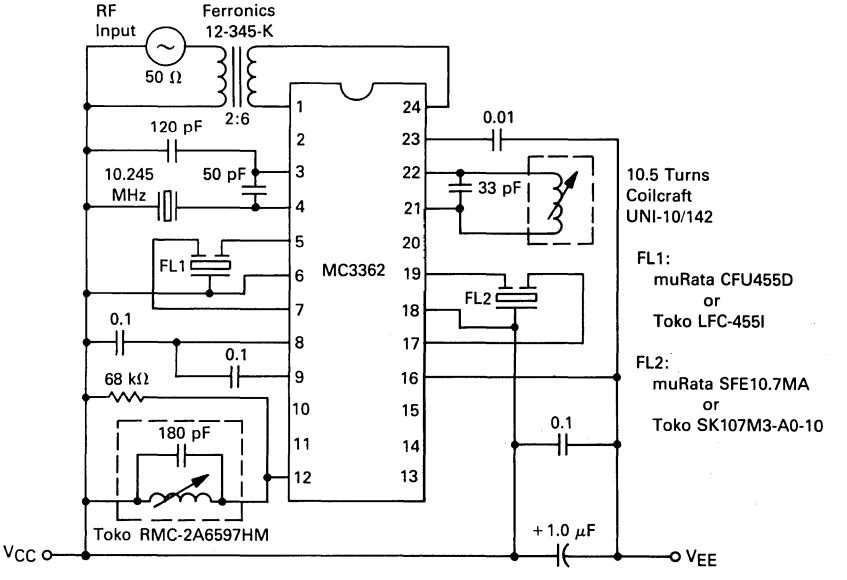


FIGURE 4 — I_{METER} versus INPUT

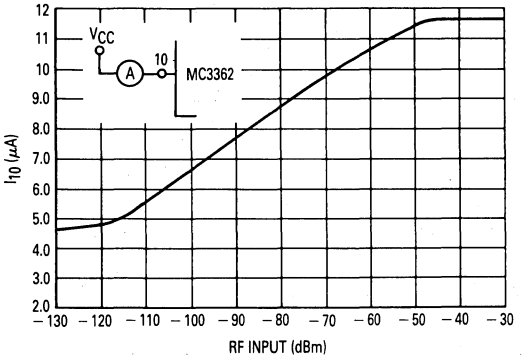


FIGURE 5 — DRAIN CURRENT, RECOVERED AUDIO versus SUPPLY

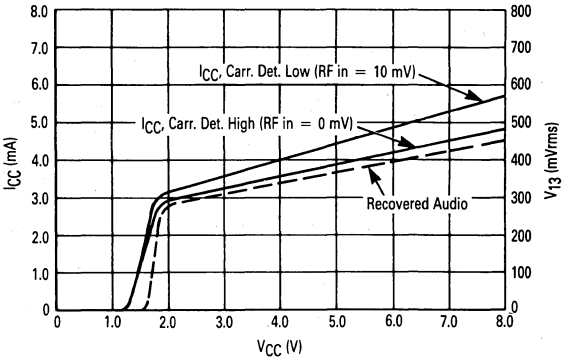


FIGURE 6 — SIGNAL LEVELS

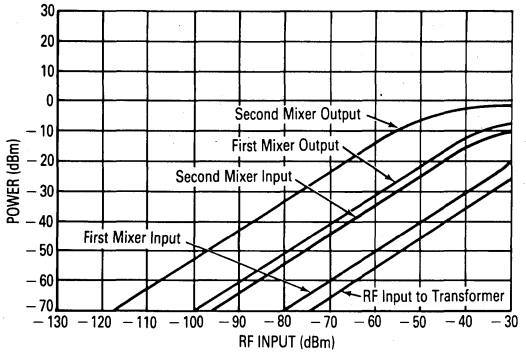


FIGURE 7 — S+N, N, AMR versus INPUT

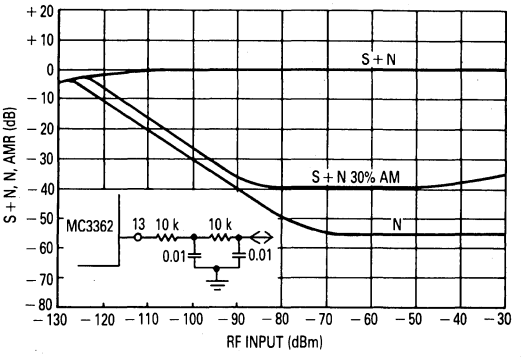


FIGURE 8 — 1ST MIXER 3RD ORDER INTERMODULATION

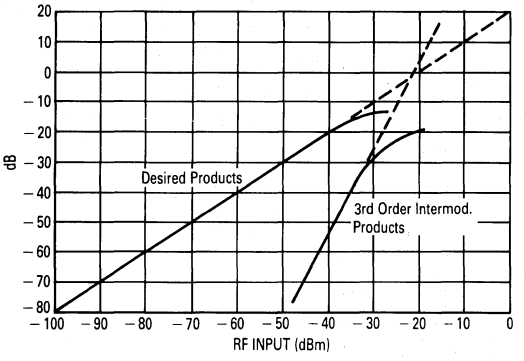
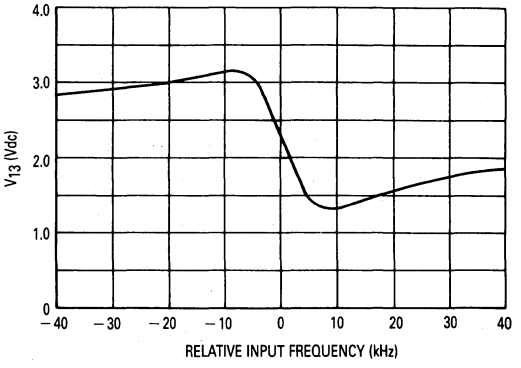


FIGURE 9 — DETECTOR OUTPUT versus FREQUENCY



CIRCUIT DESCRIPTION

The MC3362 is a complete FM narrowband receiver from antenna input to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application (Figure 1), the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATION

The first local oscillator can be run using a free-running LC tank, as a VCO using PLL synthesis, or driven from an external crystal oscillator. It has been run to 190 MHz.* A buffered output is available at Pin 20. The second local oscillator is a common base Colpitts type which is typically run at 10.245 MHz under crystal control. A buffered output is available at Pin 2. Pins 2 and 3 are interchangeable.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 22 dB (typical), respectively, as seen in Figure 6. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters. Overall sensitivity and AM rejection are shown in Figure 7. The input level for 20 dB (S+N)/N is 0.7 μV using the two-pole post-detection filter pictured.

*If the first local oscillator (Pins 21 and/or 22) is driven from a strong external source (100 mVrms), the mixer can be used to over 450 MHz.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into one second mixer input pin, the other input pin being connected to V_{CC}.

The 455 kHz IF is typically filtered using a ceramic bandpass filter then fed into the limiter input pin. The limiter has 10 μV sensitivity for -3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 12 to V_{CC}. A 68 kΩ shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will increase the spacing and linearity but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 13. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of 2000 to 35000 baud are detectable using the circuit of Figure 1. Hysteresis is available by connecting a high-valued resistor from Pin 15 to Pin 14. Values below 120 kΩ are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 4 shows the unloaded current at Pin 10 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power. To do this, pick an RF trip level in dBm. Read the corresponding current from Figure 4 and pick a resistor such that:

$$R_{10} \simeq 0.64\ \text{Vdc} / I_{10}$$

Hysteresis is available by connecting a high-valued resistor R_H between Pins 10 and 11. The formula is:

$$\text{Hyst.} = V_{CC}/(R_H \times 10^{-7})\ \text{dB}$$

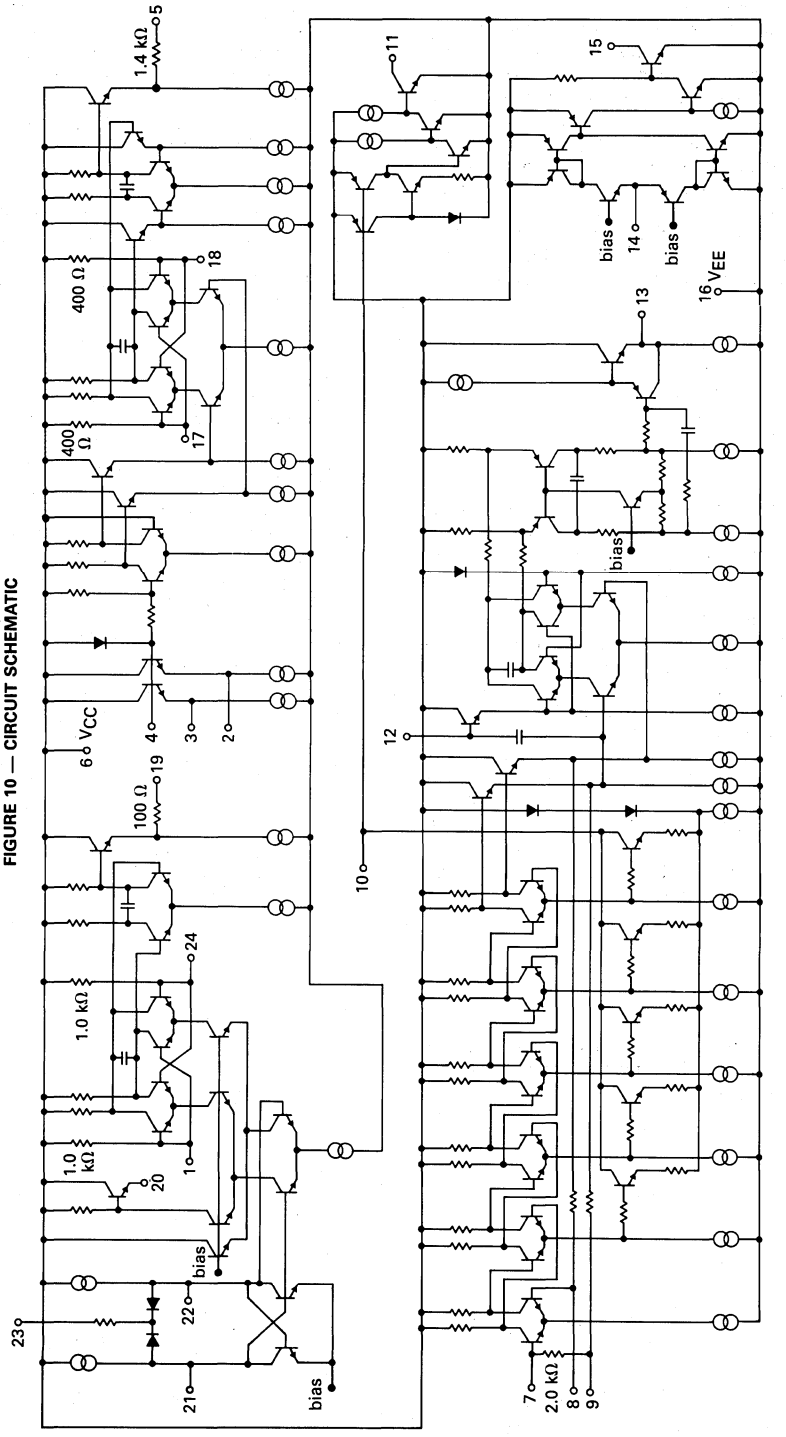


FIGURE 10 — CIRCUIT SCHEMATIC

MC3363

LOW POWER DUAL CONVERSION FM RECEIVER

The MC3363 is a single chip narrowband VHF FM radio receiver. It is a dual conversion receiver with RF amplifier transistor, oscillators, mixers, quadrature detector, meter drive/carrier detect and mute circuitry. The MC3363 also has a buffered first local oscillator output for use with frequency synthesizers, and a data slicing comparator for FSK detection.

- Wide Input Bandwidth — 200 MHz Using Internal Local Oscillator
  — 450 MHz Using External Local Oscillator
- RF Amplifier Transistor
- Muting Operational Amplifier
- Complete Dual Conversion
- Low Voltage: V_{CC} = 2.0 V to 7.0 V
- Low Drain Current: I_{CC} = 3.6 mA (Typ) at V_{CC} = 3.0 V, Excluding RF Amplifier Transistor
- Excellent Sensitivity: Input 0.3 μV (Typ) for 12 dB SINAD Using Internal RF Amplifier Transistor
- Data Shaping Comparator
- Received Signal Strength Indicator (RSSI) with 60 dB Dynamic Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC Process Technology
- See AN980 For Additional Design Information

LOW POWER DUAL CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

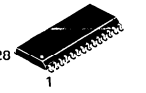


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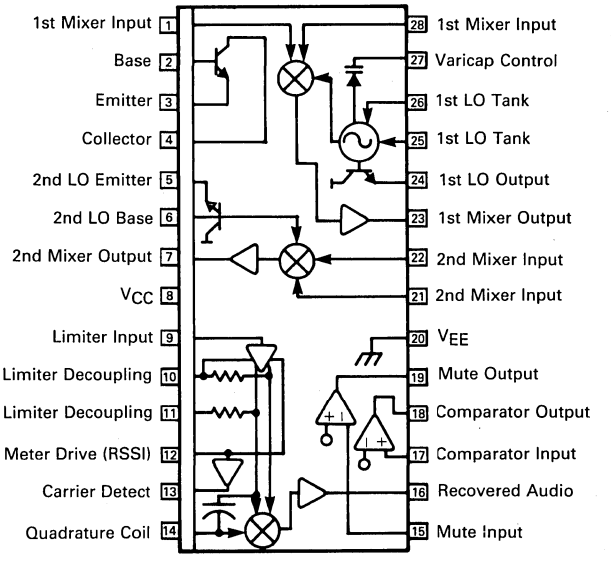
FIGURE 1 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



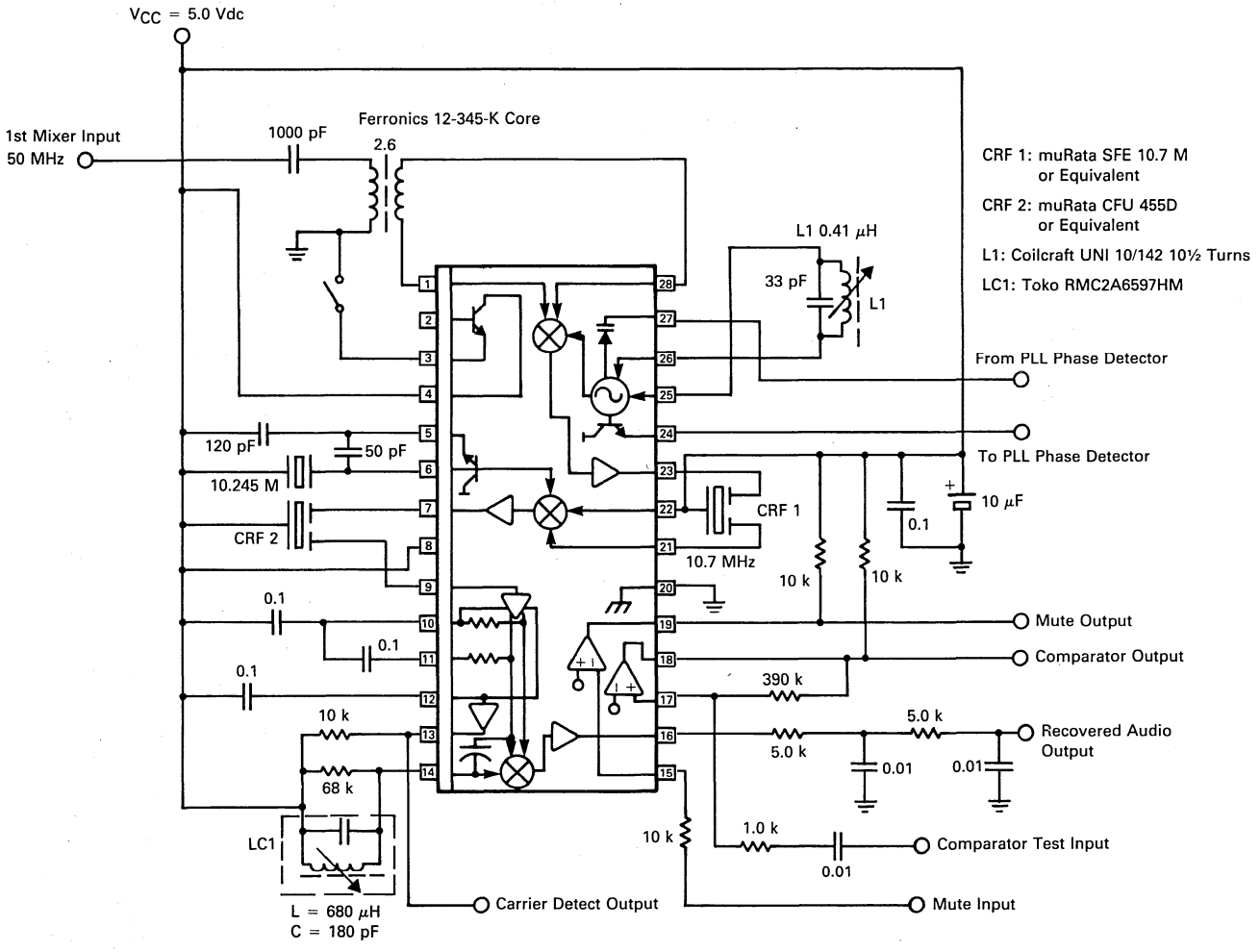
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	8	$V_{CC(max)}$	8.0	Vdc
Operating Supply Voltage Range (Recommended)	8	V_{CC}	2.0 to 7.0	Vdc
Input Voltage (V_{CC} = 5.0 Vdc)	1, 28	V_{1-28}	1.0	Vrms
Mute Output Voltage	19	V_{19}	−0.7 to 8.0	Vpk
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−40 to +85	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = ±3.0 kHz, T_A = 25°C, Mod 1.0 kHz, Test Circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current (Carrier Detect Low)	8	—	4.5	8.0	mA
−3.0 dB Limiting Sensitivity (RF Amplifier Not Used)	—	—	0.7	2.0	μVrms
20 dB S/N Sensitivity (RF Amplifier Not Used)	—	—	1.0	—	μVrms
1st Mixer Input Resistance (Parallel — Rp)	1, 28	—	690	—	Ohm
1st Mixer Input Capacitance (Parallel — Cp)	1, 28	—	7.2	—	pF
1st Mixer Conversion Voltage Gain (A_{vc1}, Open Circuit)	—	—	18	—	dB
2nd Mixer Conversion Voltage Gain (A_{vc2}, Open Circuit)	—	—	21	—	dB
2nd Mixer Input Sensitivity (20 dB S/N) (10.7 MHz i/p)	21	—	10	—	μVrms
Limiter Input Sensitivity (20 dB S/N) (455 kHz i/p)	9	—	100	—	μVrms
RF Transistor DC Current Drain	4	1.0	1.5	2.5	mAdc
Recovered Audio (RF Signal Level = 1.0 mV)	16	120	200	—	mVrms
Noise Output Level (RF Signal = 0 mV)	16	—	70	—	mVrms
THD of Recovered Audio (RF Signal = 1.0 mV)	16	—	2%	—	%
Detector Output Impedance	16	—	400	—	Ohm
Data (Comparator) Output Voltage — High — Low	18 18	— 0.1	— 0.1	V_{CC} —	Vdc Vdc
Data (Comparator) Threshold Voltage Difference	17	70	110	150	mV
Meter Drive Slope	12	70	100	135	nA/dB
Carrier Detect Threshold (Below V_{CC})	12	0.53	0.64	0.77	Vdc
Mute Output Impedance — High — Low	19 19	— —	10 25	— —	Mohm Ohm

FIGURE 2 — TEST CIRCUIT



CIRCUIT DESCRIPTION

The MC3363 is a complete FM narrowband receiver from RF amplifier to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application, the input RF signal is amplified by the RF transistor and then the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATION

The first local oscillator is designed to serve as the VCO in a PLL frequency synthesized receiver. The MC3363 can operate together with the MC145166/7 to provide a two-chip ten channel frequency synthesized receiver in the 46/49 cordless telephone band. The MC3363 can also be used with the MC14515X series of CMOS PLL synthesizers and MC120XX series of ECL prescalers in VHF frequency synthesized applications to 200 MHz.

For single channel applications the first local oscillator can be crystal controlled. The circuit of Figure 4 has been used successfully up to 60 MHz. For higher frequencies an external oscillator signal can be injected into Pins 25 and/or 26 — a level of approximately 100 mVrms is recommended. The first mixer's transfer characteristic is essentially flat to 450 MHz when this approach is used (keeping a constant 10.7 MHz IF frequency). The second local oscillator is a Colpitts type which is typically run at 10.245 MHz under crystal control.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 21 dB (typical), respectively. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into the second mixer input Pin 21, the other input Pin 22 being connected to V_{CC}.

The 455 kHz IF is filtered by a ceramic narrow bandpass filter then fed into the limiter input Pin 9. The limiter has 10 μV sensitivity for −3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 14 to V_{CC}. A 68 kOhm shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will lower the Q and expand the deviation range and linearity, but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 16. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of 2000 to 35000 baud are detectable using the comparator. Best sensitivity is obtained when data rates are limited to 1200 baud maximum. Hysteresis is available by connecting a high-valued resistor from Pin 17 to Pin 18. Values below 120 kOhm are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 5 shows the unloaded current at Pin 12 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power.

A muting op amp is provided and can be triggered by the carrier detect output (Pin 13). This provides a carrier level triggered squelch circuit which is activated when the RF input at the desired input frequency falls below a preset level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 12) and V_{CC}. Values between 80–130 kOhms are recommended. This type of squelch is pictured in Figures 3 and 4.

Hysteresis is available by connecting a high-valued resistor Rh between Pins 12 and 13. The formula is:

$$\text{Hyst} = V_{CC}/(\text{Rh} \times 10^{-7})\ \text{dB}$$

The meter drive can also be used directly to drive a meter or to provide AGC. A current to voltage converter or other linear buffer will be needed for this application.

A second possible application of the op amp would be in a noise triggered squelch circuit, similar to that used with the MC3357/MC3359/MC3361 FM I.F.'s. In this case the op amp would serve as an active noise filter, the output of which would be rectified and compared to a reference on a squelch gate. The MC3363 does not have a dedicated squelch gate, but the NPN RF input stage or data shaping comparator might be used to provide this function if available. The op amp is a basic type with the inverting input and the output available. This application frees the meter drive to allow it to be used as a linear signal strength monitor.

The circuit of Figure 4 is a complete 50 MHz receiver from antenna input to audio preamp output. It uses few components and has good performance. The receiver operates on a single channel and has input sensitivity of <0.3 μV for 12 dB SINAD.

FIGURE 3 — TYPICAL APPLICATION IN A PLL FREQUENCY SYNTHESIZED RECEIVER

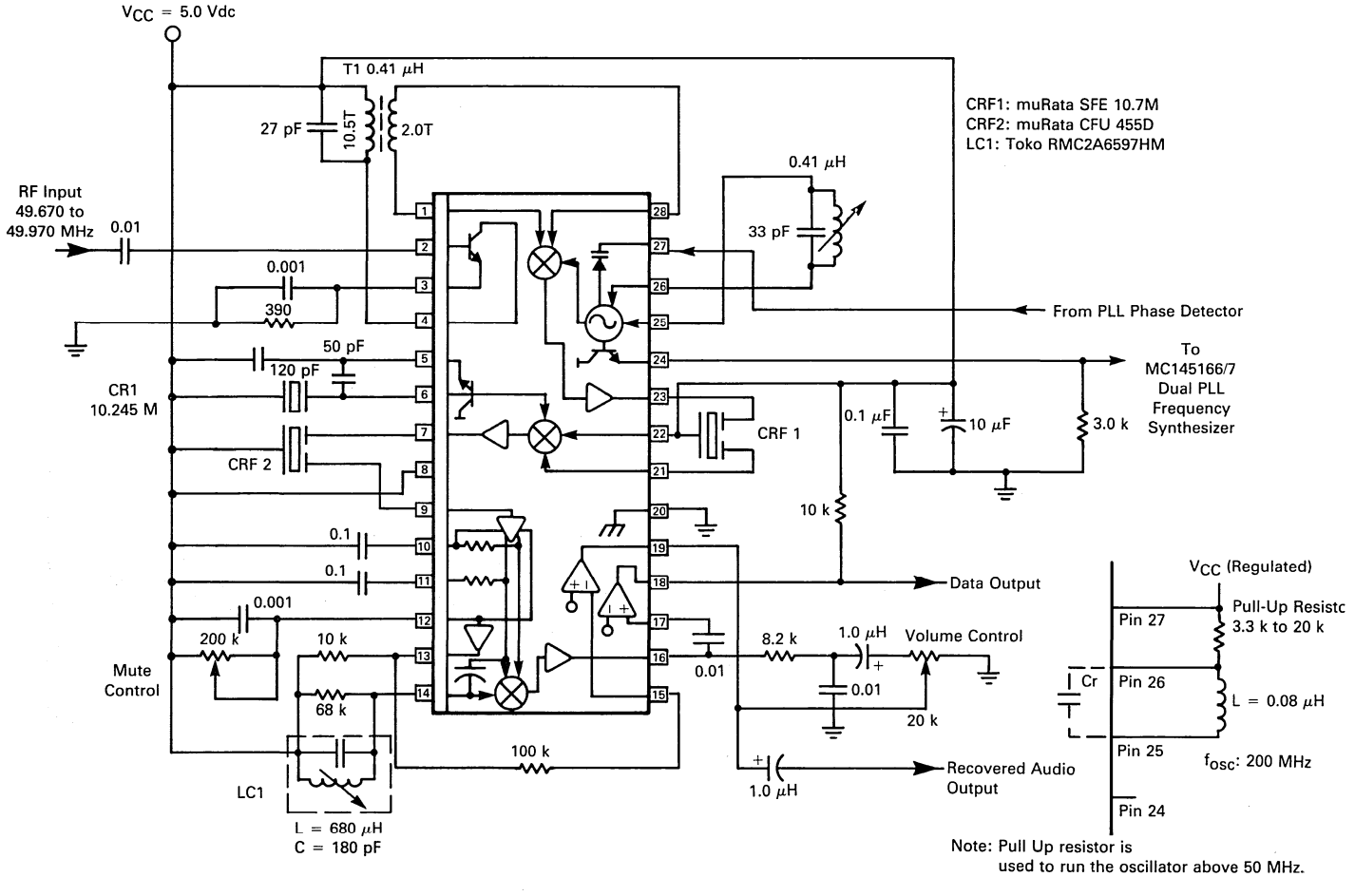


FIGURE 4 — SINGLE CHANNEL CRYSTAL CONTROLLED FM RECEIVER

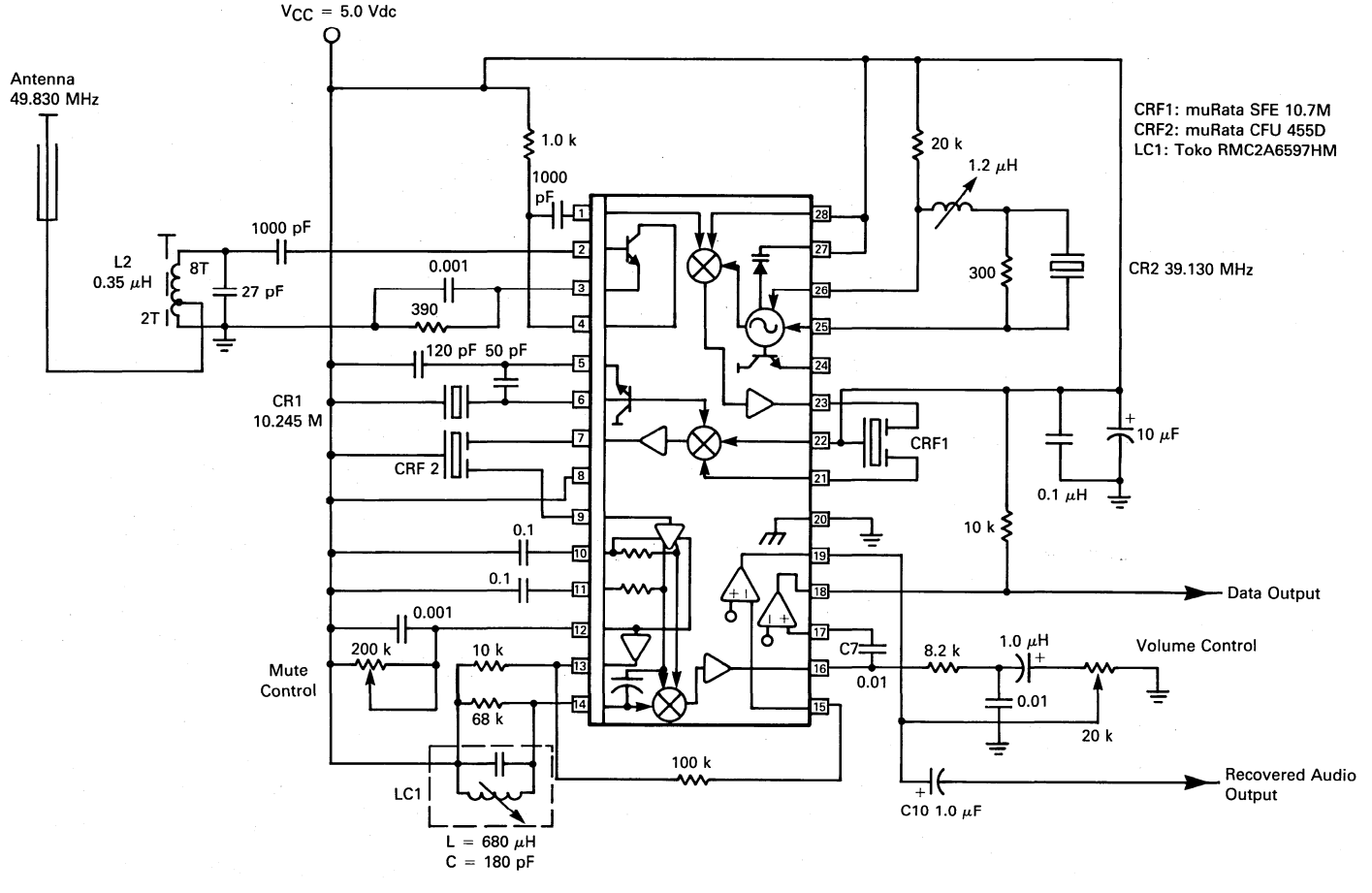
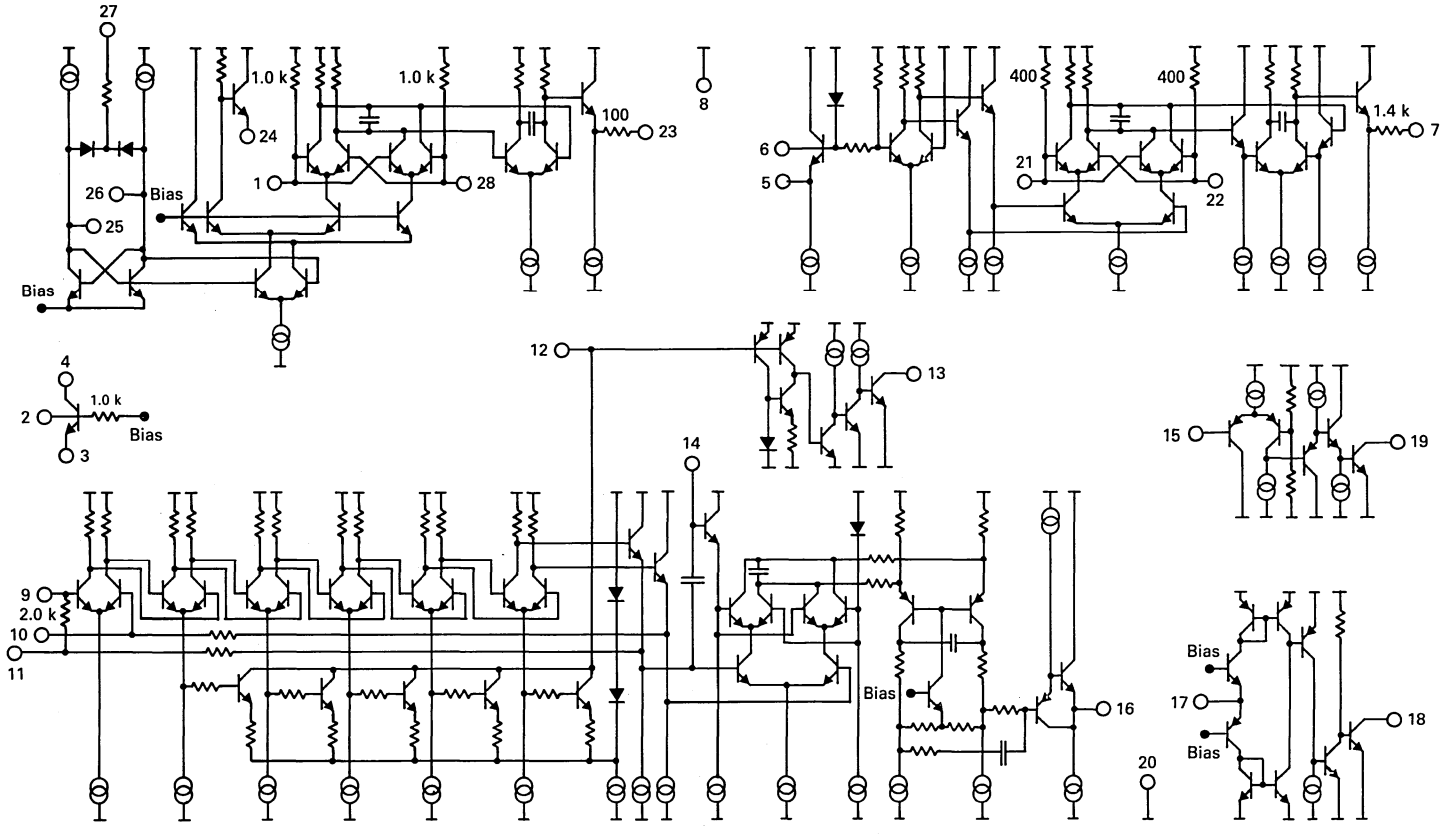


FIGURE 5 — CIRCUIT SCHEMATIC



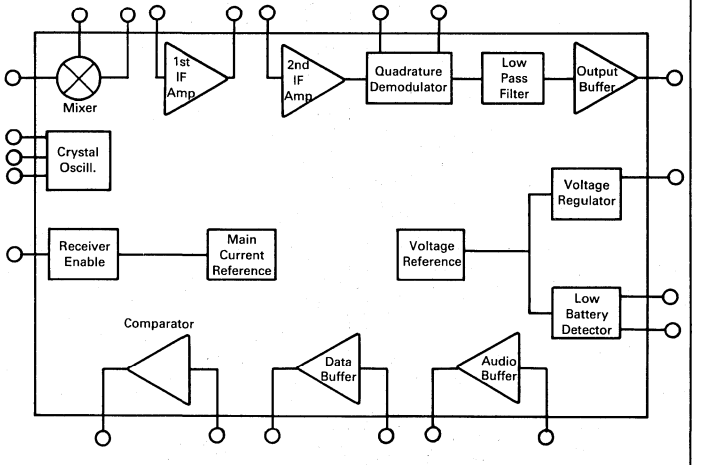
MC3367

LOW VOLTAGE FM NARROWBAND RECEIVER

. . . with single conversion circuitry including oscillator, mixer, IF amplifiers, limiting IF circuitry, and quadrature discriminator. The MC3367 is perfect for narrowband audio and data applications up to 75 MHz which require extremely low power consumption. Battery powered applications down to V_{CC} = 1.1 V are possible. The MC3367 also includes an on-board voltage regulator, low battery detection circuitry, a receiver enable allowing a power down "sleep mode," two undedicated buffer amplifiers to allow simultaneous audio and data reception, and a comparator for enhancing FSK (Frequency Shift Keyed) data reception.

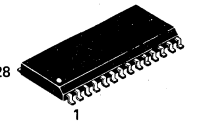
- Low Supply Voltage: V_{CC} = 1.1 to 3.0 Vdc
- Low Power Consumption: P_D = 1.5 to 5.0 mW
- Input Bandwidth 75 MHz
- Excellent Sensitivity: Input Limiting Voltage (−3.0 dB) = 0.2 μVrms
- Voltage Regulator Available (Source Capability 3.0 mA)
- Receiver Enable to Allow Active/Standby Operation
- Low Battery Detection Circuitry
- Self Biasing Audio Buffer with Nominal Gain A_V = 4.0
- Data Buffer with Nominal Gain A_V = 3.2
- Comparator with > 25 kHz (50 kbaud) Capability
- Standard 28-Lead Surface Mount (SOIC) Package

FIGURE 1 — BLOCK DIAGRAM



LOW VOLTAGE SINGLE CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



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PIN CONNECTIONS

Mixer Dcpl.	1	28	2nd IF Amp In
Mixer Out	2	27	Data Buffer Out
Mixer In	3	26	Data Buffer In
Osc. Dcpl.	4	25	1st IF Amp Out
Osc. Base	5	24	V_{CC3}
Osc. Emit.	6	23	1st IF Amp In
Isrc Dcpl.	7	22	Audio Buffer Out
IF Gnd	8	21	Audio Buffer In
V_{CC2}	9	20	Low Battery Det.
Rec. Audio	10	19	1.2 V Select
Quad Tank	11	18	V_{CC}
Quad Tank	12	17	V_{reg}
Demod. Gnd	13	16	Receiver Enable
Comparator I/P	14	15	Comparator O/P

ABSOLUTE MAXIMUM RATINGS (Voltages referred to Pin 12; T_A = 25°C)

Parameter	Pin	Value	Units
Supply Voltage	18	5.0	Vdc
RF Input Signal	3	1.0	Vrms
Audio Buffer Input	21	1.0	Vrms
Data Buffer Input	26	1.0	Vrms
Comparator Input	14	1.0	Vrms
Junction Temperature	—	150	°C
Storage Temperature	—	−65 to +150	°C

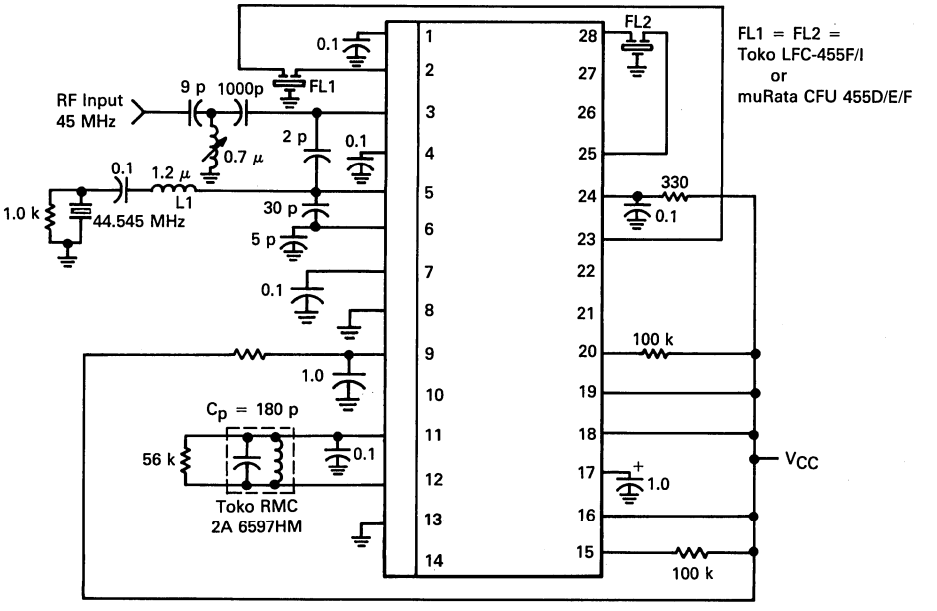
Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin	Value	Units
Supply Voltage	18	1.1 to 3.0	Vdc
Receiver Enable Voltage	16	0 or V_{CC}	Vdc
1.2 V Select Voltage	19	V_{CC}	Vdc
RF Input Signal	3	0.001 to 100	mVrms
RF Input Frequency	3	0 to 75	MHz
Intermediate Frequency (IF)	—	455	kHz
Audio Buffer Input	21	0 to 75	mVrms
Data Buffer Input	26	0 to 75	mVrms
Comparator Input	14	10 to 300	mVrms
Ambient Temperature	—	0 to 70	°C

FIGURE 2 — TEST CIRCUIT

(All capacitors in μF unless otherwise stated. Resistors in ohms. Inductors in Henries.)



ELECTRICAL CHARACTERISTICS (V_{CC} = 1.3 V, f_o = 45 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
OVERALL MC3367 PERFORMANCE					
Drain Current — Pin 15 = V_{CC} — Pin 15 = 0 Vdc	— —	— —	1.4 0.5	3.0 —	mA μA
Recovered Audio (RF Input = 10 mV)	10	—	13	—	mVrms
Noise Output (RF Input = 0 mV)	10	—	4.5	—	mVrms
Input for −3.0 dB Limiting	3	—	0.2	—	μVrms
MIXER					
Mixer Input Resistance (Rp)	3	—	3.0	—	kΩ
Mixer Input Capacitance (Cp)	3	—	9.0	—	pF
FIRST IF AMPLIFIER					
First IF Amp Voltage Gain	—	—	25	—	dB
AUDIO BUFFER					
Voltage Gain	—	—	4.0	—	V/V
Input Resistance	21	—	125	—	kΩ
Maximum Input for Undistorted Output	21	—	70	—	mVrms
Maximum Output Swing	22	—	800	—	mVpp
Output Resistance	22	—	680	—	Ω
DATA BUFFER					
Voltage Gain	—	—	3.2	—	V/V
Input Resistance	26	—	8.0	—	MΩ
Maximum Input for Undistorted Output	26	—	70	—	mVrms
Maximum Output Swing	27	—	600	—	mVpp
Output Resistance	27	—	1.5	—	kΩ
COMPARATOR					
Minimum Input for Triggering	14	—	7.0	—	mVrms
Maximum Input Frequency (R_L = 100 kΩ)	14	—	25	—	kHZ
Rise Time (10–90%; R_L = 100 kΩ)	15	—	5.0	—	μs
Fall Time (90–10%; R_L = 100 kΩ)	15	—	0.4	—	μs
LOW BATTERY DETECTOR					
Low Battery Trip Point	18	—	1.09	—	Vdc
Low Battery Output — V_{CC} = 0.9 V — V_{CC} = 1.3 V	20 20	— —	0.2 V_{CC}	— —	Vdc Vdc
VOLTAGE REGULATOR					
Regulated Output (see Figure 6)	17	—	0.95	—	Vdc
Source Capability	17	—	—	3.0	mA

FIGURE 3 — RECOVERED AUDIO versus SUPPLY

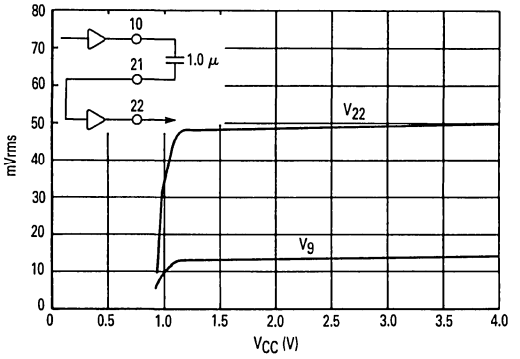


FIGURE 4 — DRAIN versus SUPPLY

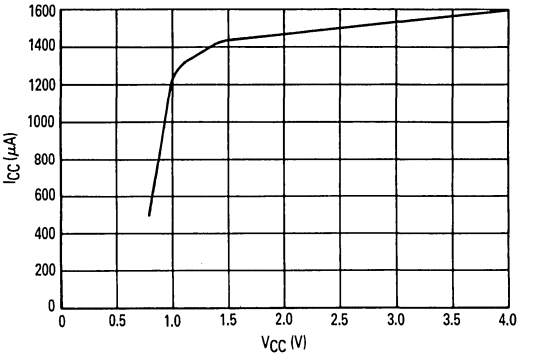


FIGURE 5 — S+N, N versus INPUT

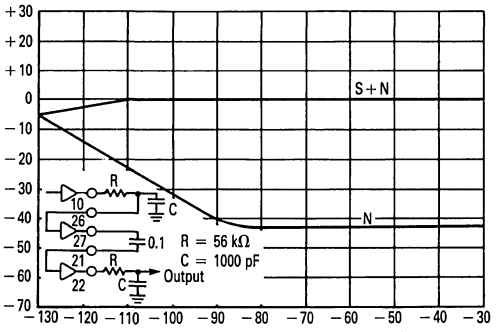
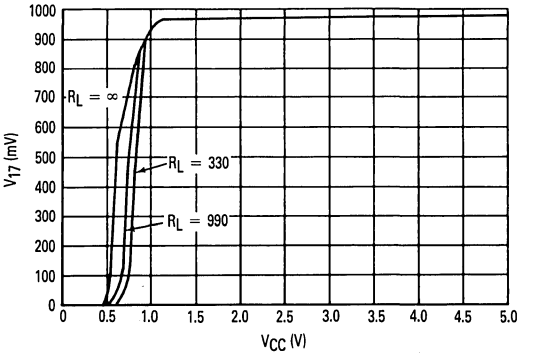


FIGURE 6 — V_{REG} versus SUPPLY



CIRCUIT DESCRIPTION

The MC3367 is an FM narrowband receiver capable of operation to 75 MHz. The low voltage design yields low power drain and excellent sensitivity in narrowband voice and data link applications. In the typical application the mixer amplifies the incoming RF or IF signal and converts the RF or IF frequency to 455 kHz. This signal is then filtered by a 455 ceramic filter and applied to the first intermediate frequency (IF) amplifier input. This amplifier amplifies the 455 kHz IF before it is filtered by a second ceramic filter. The modulated IF signal is then applied to the limiting IF amplifier and detector circuitry. Audio is recovered by a conventional quadrature detector.

Features available include buffers for audio/data amplification and active filtering, on board voltage regulator, low battery detection circuitry with programmable level, and receiver disable circuitry. The MC3367 is an FM utility receiver to be used for voice and/or narrowband data reception, especially suitable where extremely low power consumption and high design flexibility are required.

APPLICATION

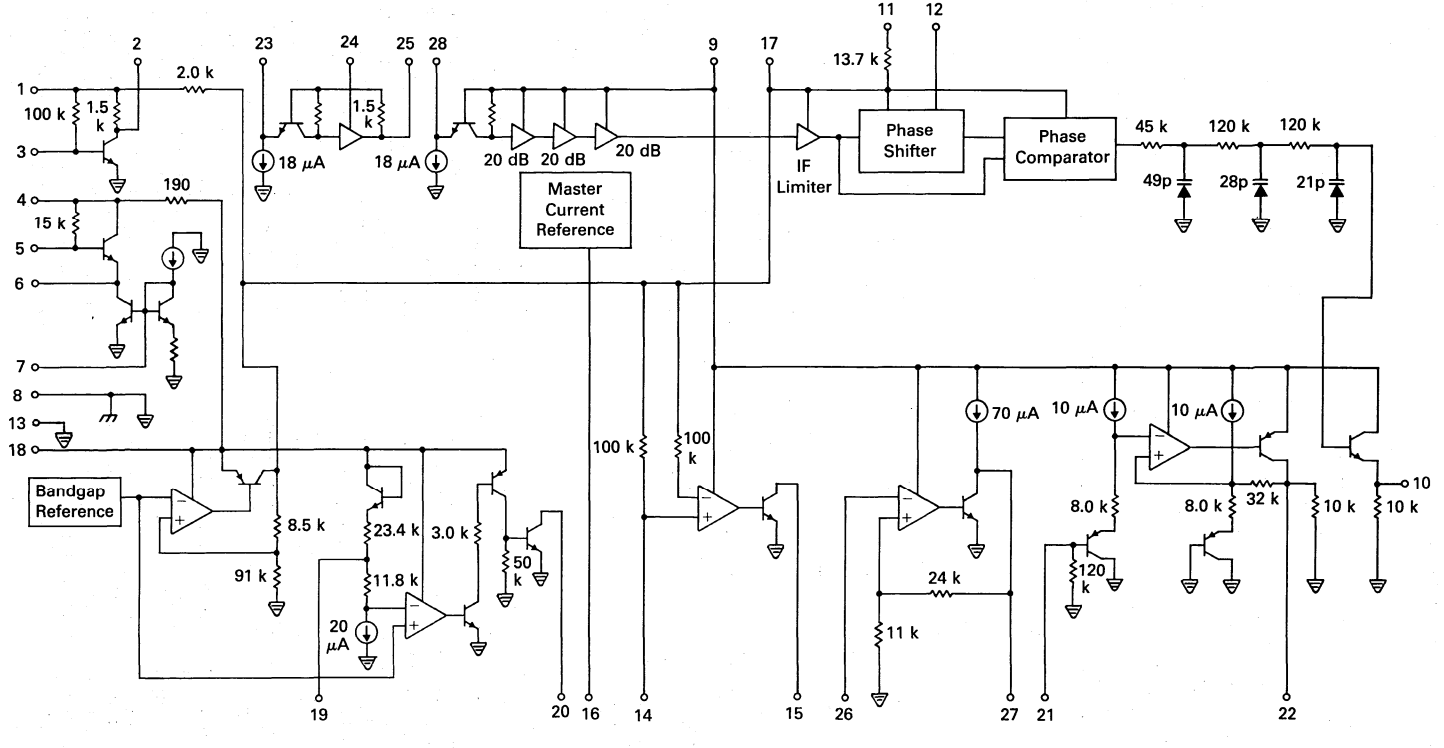
The MC3367 can be used as a high performance FM IF for use in low power dual conversion receivers. Because of the MC3367's extremely good sensitivity (0.6 μV for 20 dB (S+N)/N, see Figure 5), it can also be used as a stand alone single conversion narrowband receiver to 75 MHz for applications not sensitive to image frequency interference.

The oscillator is a Colpitts type which can be run as an LC oscillator or under crystal control. The crystal in Figure 2 is a 3rd overtone series mode type, and the 1.2 μH coil (L1) and 1.0 kΩ resistor are needed to ensure proper operation. For fundamental mode crystals, the inductor L1 can be omitted.

The best adjacent channel and sensitivity response occur when two 455 kHz ceramic filters are used, as shown in Figure 2. Either can be replaced by a 0.1 μF coupling capacitor to reduce cost, but some degradation in sensitivity and/or stability is suspected.

The detector is a quadrature type, with the connection from the limiter output to the detector input provided internally as with the MC3359 and the MC3361.

FIGURE 7 — CIRCUIT SCHEMATIC



A 455 kHz LC tank circuit must be provided externally. One of the tank pins (Pin 11) must be decoupled using a 0.1 μF capacitor. The 56 kΩ damping resistor shown in Figure 2 determines the peak separation (and thus the detector bandwidth) of the detector. Smaller values will increase the separation and bandwidth but decrease recovered audio and sensitivity.

The data buffer is a non-inverting amplifier with a nominal voltage gain of 3.2 V/V. This buffer needs its dc bias (approx. 250 mV) provided externally or else debiasing will occur. A single-pole RC filter as shown in Figure 5 connecting the recovered audio output to the data buffer input provides the necessary dc bias and some post-detection filtering. The buffer can also be used as an active filter.

The audio buffer is a non-inverting amplifier with a nominal voltage gain of 4.0 V/V. This buffer is self-biasing so its input should be ac coupled. The two buffers, when used as active filters, can be used together to allow simultaneous audio and very low-speed data reception. Another possible configuration is to receive audio only and include a noise-triggered squelch.

The comparator is a non-inverting type with an open collector output. Typically the pull-up resistor used between Pin 15 and V_{CC} is 100 kΩ. With R_L = 100 kΩ the comparator is capable of operation up to 25 kHz. This circuit is self-biasing, so its input should be ac coupled.

The regulator is a 0.95 V reference capable of sourcing 3.0 mA. This pin (Pin 17) needs to be decoupled using a 1.0–10 μF capacitor to maintain stability of the MC3367.

All three V_{CC}'s on the MC3367 (V_{CC}, V_{CC2}, V_{CC3}) run on the same supply voltage. V_{CC} is typically decoupled using capacitors only. V_{CC2} and V_{CC3} should be bypassed using the RC bypasses shown in Figure 2. Eliminating the resistors on the V_{CC2} and V_{CC3} bypasses may be possible in some applications, but a reduction in sensitivity and quieting will likely occur.

The low battery detection circuit gives an NPN open collector output at Pin 20 which drops low when the MC3367 supply voltage drops below 1.1 V. Typically it would be pulled up via a 100 kΩ resistor to supply.

The 1.2 V Select pin, when connected to the MC3367 supply, programs the low battery detector to trip at V_{CC} < 1.1 V. Leaving this pin open raises the trip voltage on the low battery detector.

Pin 16 is a receiver enable, which is connected to V_{CC} for normal operation. Connecting this pin to ground shuts off receiver and reduces current drain to I_{CC} < 0.5 μA.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3371
MC3372

Advance Information

Low Power Narrowband FM IF

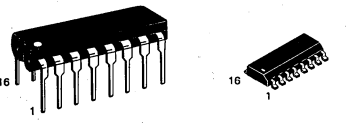
LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC3371 and MC3372 perform single conversion FM reception and consist of an oscillator, mixer, limiting IF amplifier, quadrature discriminator, active filter, squelch switch, and meter drive circuitry. These devices are designed for use in FM dual conversion communication equipment. The MC3371/MC3372 are similar to the MC3361/MC3357 FM IFs, except that a signal strength indicator replaces the scan function controlling driver which is in the MC3361/MC3357. The MC3371 is designed for the use of parallel LC components, while the MC3372 is designed for use with either a 455 kHz ceramic discriminator, or parallel LC components.

These devices also require fewer external parts than earlier products. The MC3371 and MC3372 are available in dual-in-line and surface mount packaging.

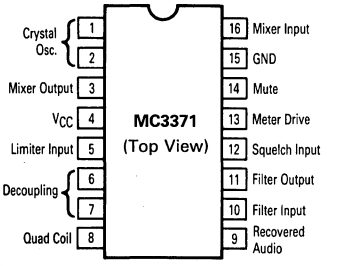
- Wide Operating Supply Voltage Range: V_{CC} = 2.0 to 9.0 V
- Input Limiting Voltage Sensitivity of −3.0 dB
- Low Drain Current: I_{CC} = 3.2 mA, @ V_{CC} = 4.0 V, Squelch Off
- Minimal Drain Current Increase When Squelched
- Signal Strength Indicator: 60 dB Dynamic Range
- Mixer Operating Frequency Up to 100 MHz
- Fewer External Parts Required than Earlier Devices

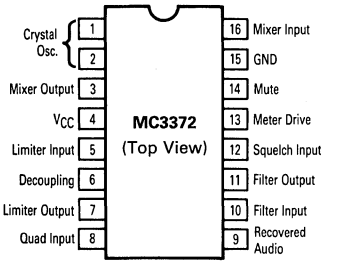


P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

PIN CONNECTIONS





MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
RF Input Voltage (V_{CC} ≥ 4.0 Vdc)	16	V_{16}	1.0	Vrms
Detector Input Voltage	8	V_8	1.0	V_{p-p}
Squelch Input Voltage (V_{CC} ≥ 4.0 Vdc)	12	V_{12}	6.0	Vdc
Mute Function	14	V_{14}	−0.7 to 10	V_{pk}
Mute Sink Current	14	I_{14}	50	mA
Junction Temperature	—	T_J	150	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Supply Voltage (@ T_A = 25°C) (−30°C ≤ T_A ≤ +75°C)	4	V_{CC}	2.0 to 9.0 2.4 to 9.0	Vdc
RF Input Voltage	16	V_{rf}	0.0005 to 10	mVrms
RF Input Frequency	16	f_{rf}	0.1 to 100	MHz
Oscillator Input Voltage	1	V_{local}	80 to 400	mVrms
Intermediate Frequency	—	f_{if}	455	kHz
Limiter Amp Input Voltage	5	V_{if}	0 to 400	mVrms
Filter Amp Input Voltage	10	V_{fa}	0.1 to 300	mVrms
Squelch Input Voltage	12	V_{sq}	0 or 2	Vdc
Mute Sink Current	14	I_{sq}	0.1 to 30	mA
Ambient Temperature Range	—	T_A	−30 to +70	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

Device	Temperature Range	Package
MC3371D	−30° to +70°C	SO-16
MC3371P		Plastic DIP
MC3372D		SO-16
MC3372P		Plastic DIP

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 58.1125 MHz, df = ±3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, f_{local} = 57.6575 MHz, V_{local} = 0 dBm, T_A = 25°C unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Input for 12 dB SINAD	—	V_{SIN}				μVrms
Matched Input — (See Figures 10, 11 & 12)			—	1.0	—	
Unmatched Input — (See Figures 7A & 7B)			—	5.0	15	
Input for 20 dB NQS	—	V_{NQS}	—	3.5	—	μVrms
Recovered Audio Output Voltage	—	AF_O				mVrms
V_{rf} = −30 dBm			120	200	320	
Recovered Audio Drop Voltage Loss	—	AF_{loss}				dB
V_{rf} = −30 dBm, V_{CC} = 4.0 V to 2.0 V			−8.0	−1.5	—	
Meter Drive Output Voltage (No Modulation)	13	M_{Drv}				Vdc
V_{rf} = −100 dBm		MV1	—	0.3	0.5	
V_{rf} = −70 dBm		MV2	1.1	1.5	1.9	
V_{rf} = −40 dBm		MV3	2.0	2.5	3.1	
Filter Amp Gain	—	$A_{V(Amp)}$				dB
R_S = 600 Ω, f_S = 10 kHz, V_{fa} = 1.0 mVrms			47	50	—	
Mixer Conversion Gain	—	$A_{V(Mix)}$				dB
V_{rf} = −40 dBm, R_L = 1.8 kΩ			14	20	—	
Signal to Noise Ratio	—	s/n				dB
V_{rf} = −30 dBm			36	67	—	
Total Harmonic Distortion	—	THD				%
V_{rf} = −30 dBm, BW = 400 Hz to 30 kHz			—	0.6	3.4	
Detector Output Impedance	9	Z_O	—	450	—	Ω
Detector Output Voltage (No Modulation)	9	DV_O				Vdc
V_{rf} = −30 dBm			—	1.45	—	
Meter Drive	13	M_O				μA/dB
V_{rf} = −100 to −40 dBm			—	0.8	—	
Meter Drive Dynamic Range	13	MVD				dB
RF_{In}			—	60	—	
IF_{In} (455 kHz)			—	80	—	
Mixer Third Order Input Intercept Point	—	ITO_{Mix}				dBm
f1 = 58.125 MHz						
f2 = 58.1375 MHz			—	−22	—	
Mixer Input Resistance	16	R_{in}	—	3.3	—	kΩ
Mixer Input Capacitance	16	C_{in}	—	2.2	—	pF

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, T_A = 25°C, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Drain Current (No Input Signal)	4					mA
Squelch Off, V_{sq} = 2.0 Vdc		Icc1	—	3.2	4.2	
Squelch On, V_{sq} = 0 Vdc		Icc2	—	3.6	4.8	
Squelch Off, V_{CC} = 2.0 to 9.0 V		dIcc1	—	1.0	2.0	
Detector Output (No Input Signal)	9	V_9				Vdc
DC Voltage, V8 = V_{CC}			0.9	1.6	2.3	
Filter Output (No Input Signal)	11					Vdc
DC Voltage		V_{11}	1.5	2.5	3.5	
Voltage Change, V_{CC} = 2.0 to 9.0 V		dV_{11}	2.0	5.0	8.0	
Trigger Hysteresis	—	Hys	34	57	80	mV

TYPICAL CURVES (UNMATCHED INPUT)

FIGURE 1 — TOTAL HARMONIC DISTORTION versus TEMPERATURE

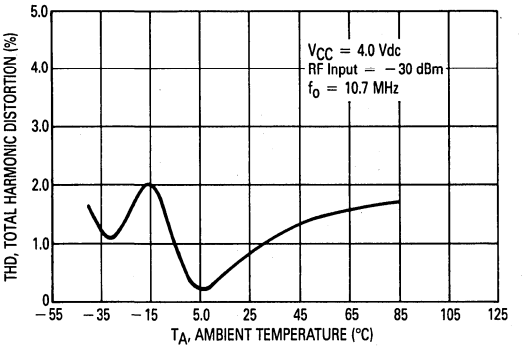


FIGURE 2 — RSSI versus RF INPUT

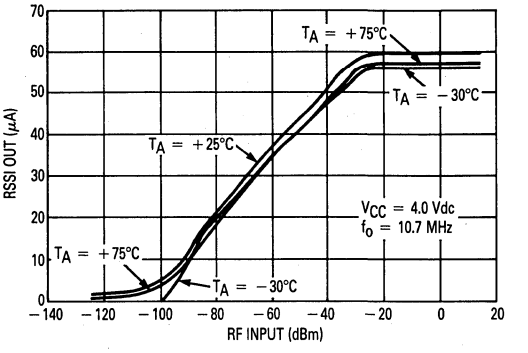


FIGURE 3 — RSSI OUTPUT versus TEMPERATURE

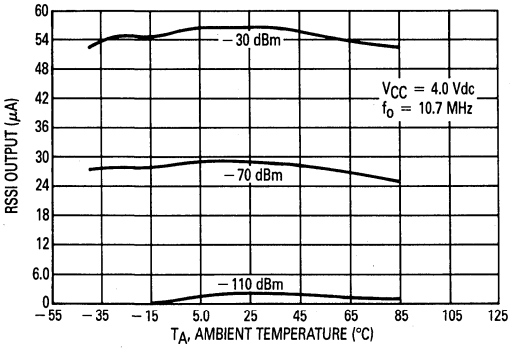


FIGURE 4 — MIXER OUTPUT versus RF INPUT

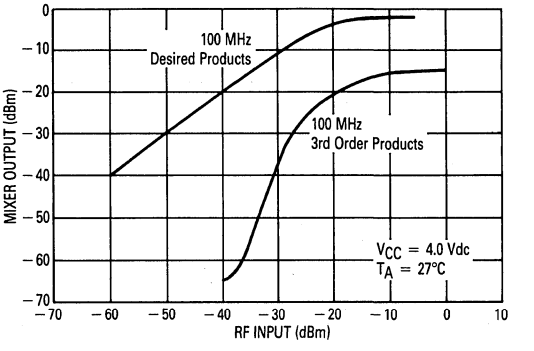


FIGURE 5 — MIXER GAIN versus SUPPLY VOLTAGE

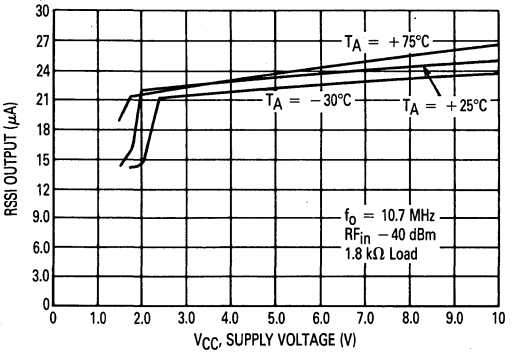


FIGURE 6 — MIXER GAIN versus FREQUENCY

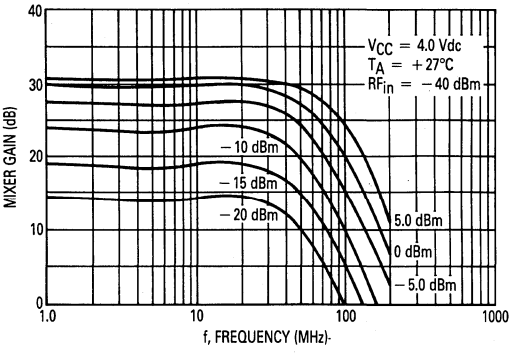


FIGURE 7A — MC3371 FUNCTIONAL BLOCK DIAGRAM AND TEST FIXTURE SCHEMATIC

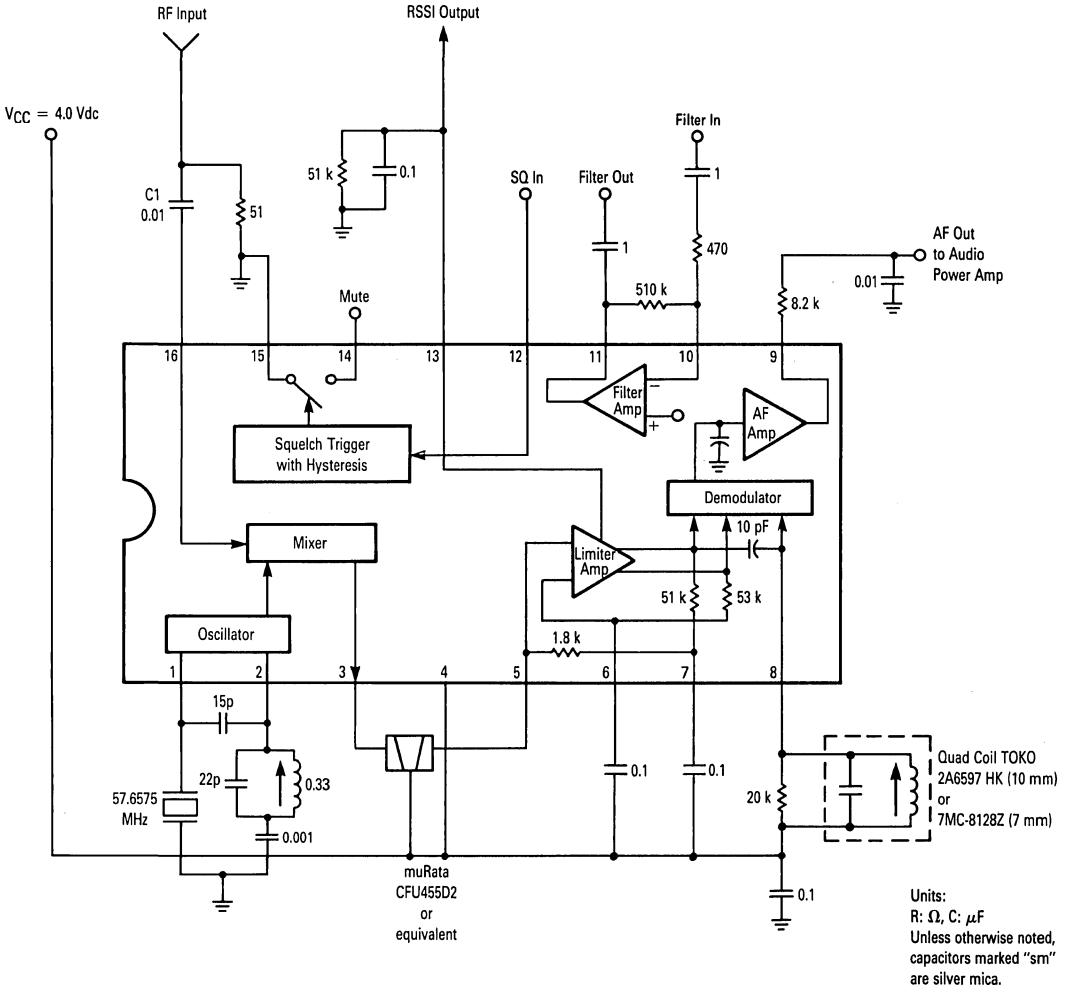
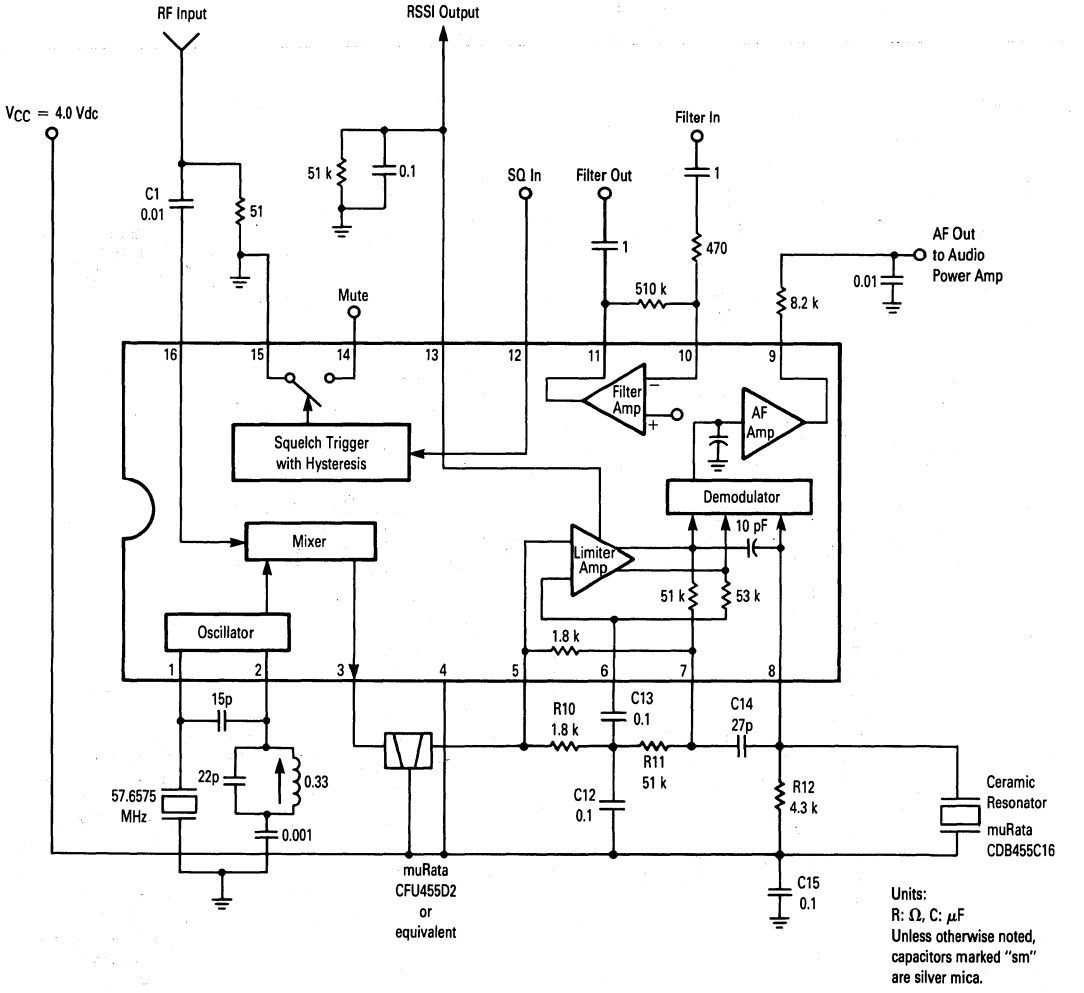
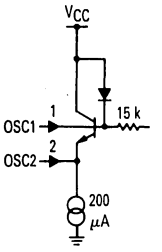
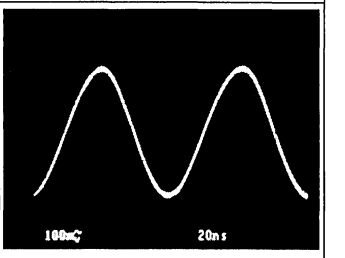
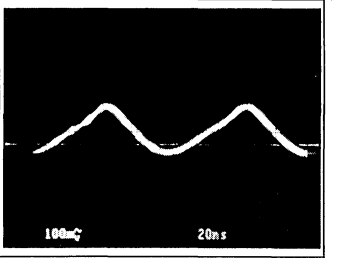
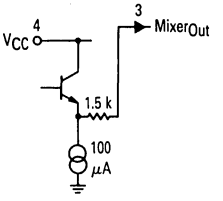
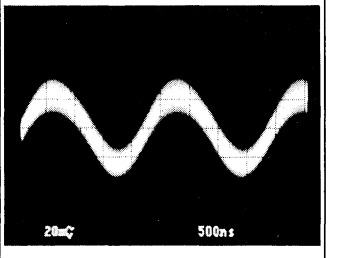
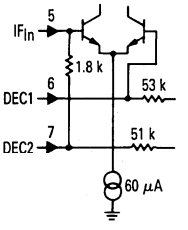
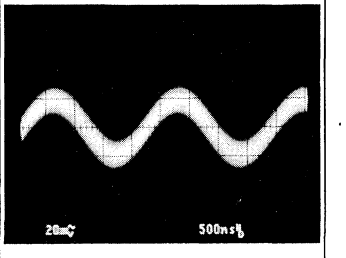


FIGURE 7B — MC3372 FUNCTIONAL BLOCK DIAGRAM AND TEST FIXTURE SCHEMATIC



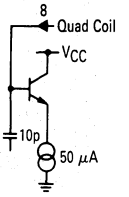
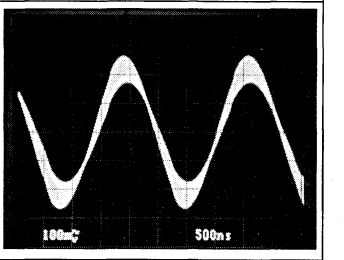
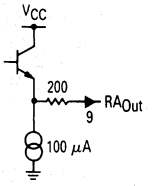
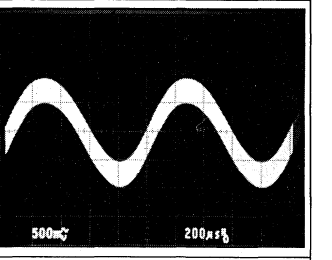
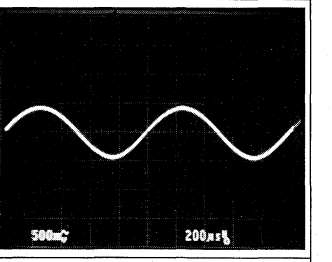
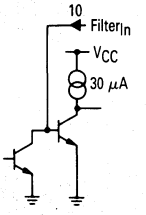
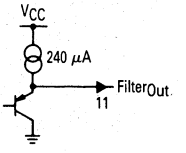
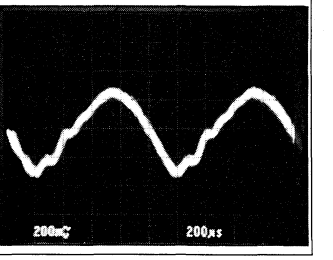
PIN DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 μV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 10).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
1	OSC1		The base of the Colpitts oscillator. Use a high impedance and low capacitance probe or a "sniffer" to view the waveform without altering the frequency. Typical level is 450 mVp-p.	
2	OSC2		The emitter of the Colpitts oscillator. Typical signal level is 200 mVp-p. Note that the signal is somewhat distorted compared to that on pin 1.	
3	MX_{Out}		Output of the Mixer. Riding on the 455 kHz is the RF carrier component. The typical level is approximately 60 mVp-p.	
4	V_{CC}		Supply Voltage — 2.0 to 9.0 Vdc is the operating range. V_{CC} is decoupled to ground.	
5	IF_{In}		Input to the IF amplifier after passing through the 455 kHz ceramic filter. The signal is attenuated by the filter. The typical level is approximately 50 mVp-p.	
6 7	DEC1 DEC2		IF Decoupling. External 0.1 μF capacitors connected to V_{CC}.	

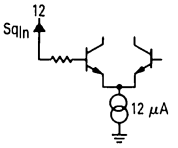
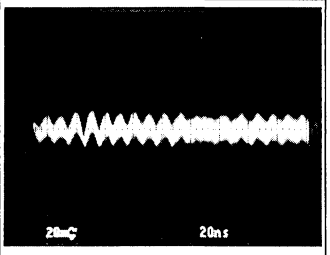
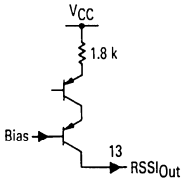
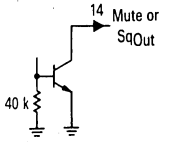
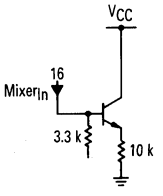
PIN DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 μV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 10).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
8	Quad Coil		Quadrature Tuning Coil. Composite (not yet demodulated) 455 kHz IF signal is present. The typical level is 500 mVp-p.	
9	RA		Recovered Audio. This is a composite FM demodulated output having signal and carrier component. The typical level is 1.4 Vp-p.	
			The filtered recovered audio has the carrier component removed and is typically 800 mVp-p.	
10	Fil_{In}		Filter Amplifier Input	
11	Fil_{Out}		Filter Amplifier Output. The typical signal level is 400 mVp-p.	

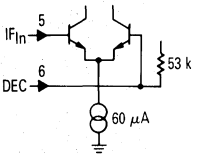
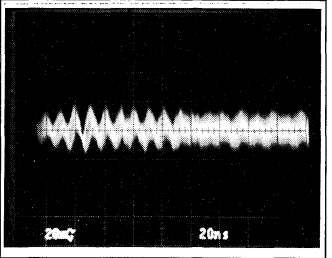
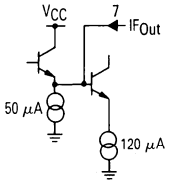
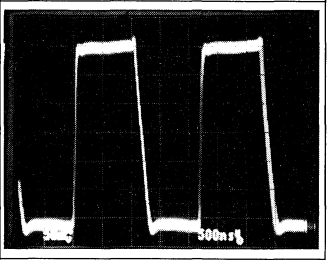
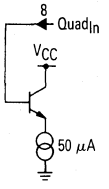
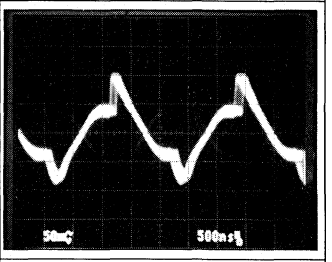
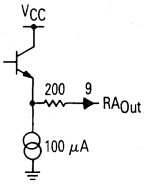
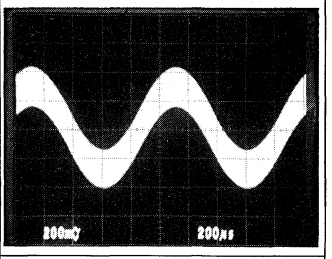
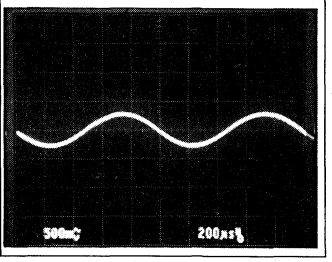
PIN DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 μV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 10).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
12	Sq_{In}		Squelch Input. See discussion in application text.	
13	RSSI		RSSI Output. Referred to as the Received Signal Strength Indicator or RSSI. The chip sources up to 60 μA over the linear 60 dB range. This pin may be used many ways, such as: AGC, meter drive and carrier triggered squelch circuit.	
14	MUTE		Mute Output. See discussion in application text.	
15	GND		Ground. The ground area should be continuous and unbroken. In a two-sided layout, the component side has the ground plane. In a one-sided layout, the ground plane fills around the traces on the circuit side of the board and is not interrupted.	
16	MIX_{In}		Mixer Input — Series Input Impedance: @ 10 MHz: 309 − j33 Ω @ 45 MHz: 200 − j13 Ω	

PIN DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 μV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3372 at f_{RF} = 45 MHz (see Figure 12).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
5	IF_{In}		IF Amplifier Input	
6	DEC1		IF Decoupling. External 0.1 μF capacitors connected to V_{CC}.	
7	IF_{Out}		IF Amplifier Output Signal level is typically 300 mVp-p.	
8	$Quad_{In}$		Quadrature Detector Input. Signal level is typically 150 mVp-p.	
9	RA		Recovered Audio. This is a composite FM demodulated output having signal and carrier components. Typical level is 800 mVp-p.	
			The filtered recovered audio has the carrier signal removed and is typically 500 mVp-p.	

*Other pins are the same as pins in MC3371.

FIGURE 8 — MC3371 CIRCUIT SCHEMATIC

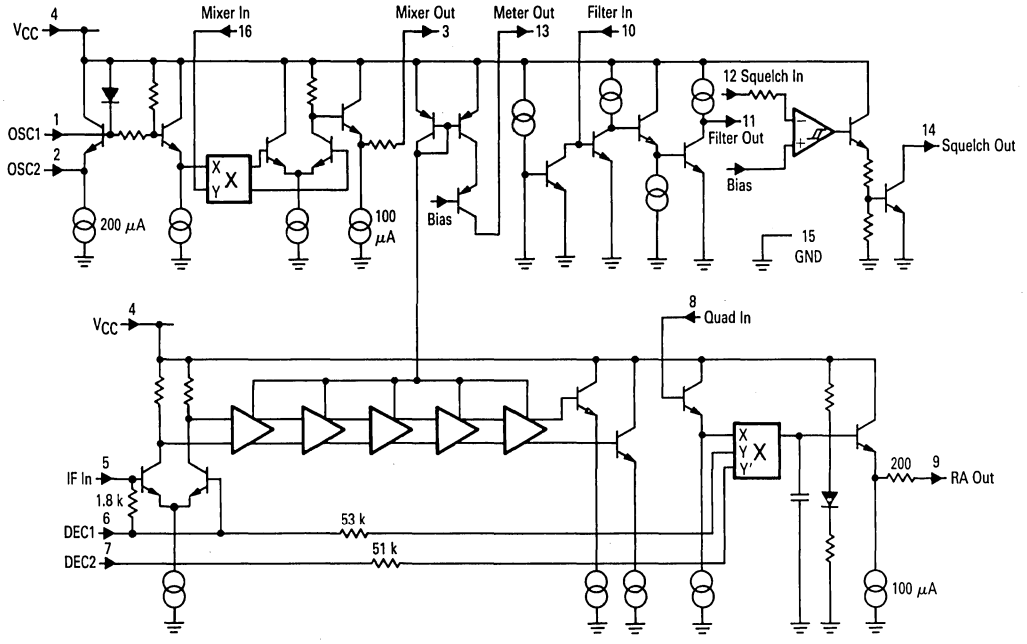
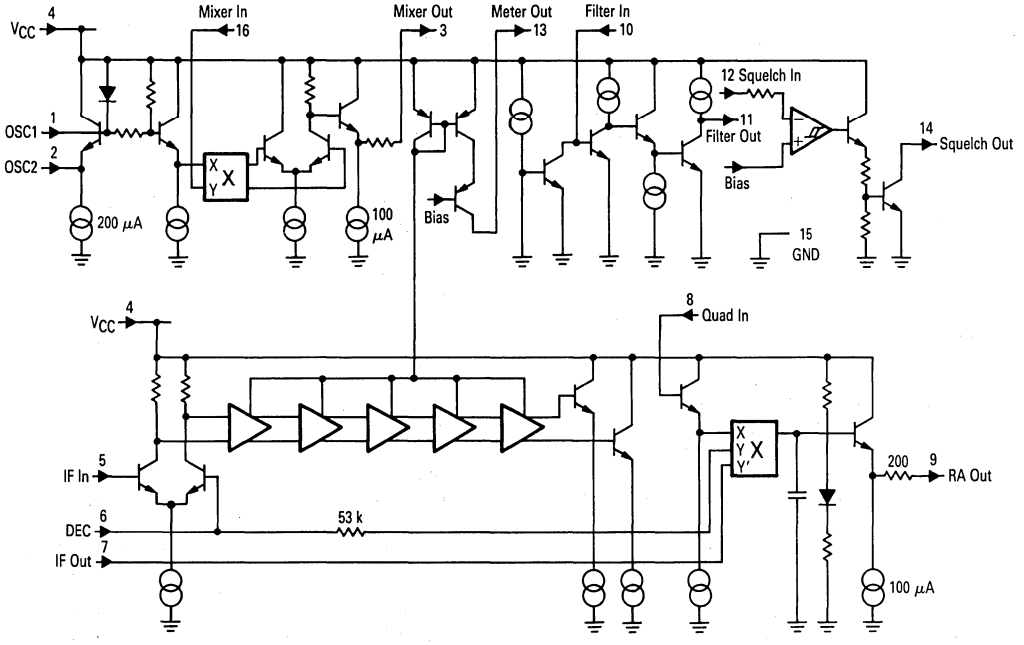


FIGURE 9 — MC3372 CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC3371 and MC3372 are low power narrowband FM receivers with an operating frequency of up to 60 MHz. Its low voltage design provides low power drain, excellent sensitivity, and good image rejection in narrowband voice and data link applications.

This part combines a mixer, an IF (intermediate frequency) limiter with a logarithmic response signal strength indicator, a quadrature detector, an active filter and a squelch trigger circuit. In a typical application, the mixer amplifier converts an RF input signal to a 455 kHz IF signal. Passing through an external bandpass filter, the IF signal is fed into a limiting amplifier and detection circuit where the audio signal is recovered. A conventional quadrature detector is used.

The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch switch is used to mute the audio when noise or a tone is present. The input signal level is monitored by a meter drive circuit which detects the amount of IF signal in the limiting amplifier.

APPLICATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1 and 2 respectively. This oscillator can be run under crystal control. For fundamental mode crystals use crystal characterized parallel resonant for 32 pF load. For higher frequencies, use 3rd overtone series mode type crystals. The coil (L2) and resistor RD (R13) are needed to ensure proper and stable operation at the LO frequency (see Figure 12, 45 MHz application circuit).

The mixer is doubly balanced to reduce spurious radiation. Conversion gain stated in the AC Electrical Characteristics table is typically 20 dB. This power gain measurement was made under stable conditions using a 50 Ω source at the input and an external load provided by a 455 kHz ceramic filter at the mixer output which is connected to the V_{CC} (Pin 4) and IF input (Pin 5). The filter impedance closely matches the 1.8 kΩ internal load resistance at Pin 3 (mixer output). Since the input impedance at Pin 16 is strongly influenced by a 3.3 kΩ internal biasing resistor and has a low capacitance, the useful gain is actually much higher than shown by the standard power gain measurement. The Smith Chart plot in Figure 16 shows the measured mixer input impedance versus input frequency with the mixer input matched to a 50 Ω source impedance at the given frequencies. In order to assure stable operation under matched conditions, it is necessary to provide a shunt resistor to ground. Figures 10, 11 and 12 show the input networks used to derive the mixer input impedance data.

Following the mixer, a ceramic bandpass filter is recommended for IF filtering (i.e. 455 kHz types having a bandwidth of ±2.0 kHz to ±15 kHz with an input and output impedance from 1.5 kΩ to 2.0 kΩ). The 6 stage limiting IF amplifier has approximately 92 dB of gain. The MC3371 and MC3372 are different in the limiter and quadrature detector circuits. The MC3371 has a 1.8 kΩ and a 51 kΩ resistor providing internal DC biasing and the output of the limiter is internally connected, both directly and through a 10 pF capacitor to the quadrature detector; whereas, in the MC3372 these components are not provided internally. Thus, in the MC3371, no external components are necessary to match the 455 kHz ceramic filter, while in the MC3372, external 1.8 kΩ and 51 kΩ biasing resistors are needed between Pins 5 and 7, respectively (see Figures 11 and 12).

In the MC3371, a parallel LCR quadrature tank circuit is connected externally from Pin 8 to V_{CC} (similar to the MC3361). In the MC3372, a quadrature capacitor is needed externally from Pin 7 to Pin 8 and a parallel LC or a ceramic discriminator with a damping resistor is also needed from Pin 8 to V_{CC} (similar to the MC3357). The above external quadrature circuitry provides 90° phase shift at the IF center frequency and enables recovered audio.

The damping resistor determines the peak separation of the detector and is somewhat critical. As the resistor is decreased, the separation and the bandwidth is increased but the recovered audio is decreased. Receiver sensitivity is dependent on the value of this resistor and the bandwidth of the 455 kHz ceramic filter.

On the chip the composite recovered audio, consisting of carrier component and modulating signal, is passed through a low pass filter amplifier to reduce the carrier component and then is fed to Pin 9 which has an output impedance of 450 Ω. The signal still requires further filtering to eliminate the carrier component, deemphasis, volume control, and further amplification before driving a loudspeaker. The relative level of the composite recovered audio signal at Pin 9 should be considered for proper interaction with an audio post amplifier and a given load element. The MC13060 is recommended as a low power audio amplifier.

The meter output indicates the strength of the IF level and the output current is proportional to the logarithm of the IF input signal amplitude. A maximum source current of 60 μA is available and can be used to drive a meter and to detect a carrier presence. This is referred to as a Received Strength Signal Indicator (RSSI). The output at Pin 13 provides a current source. Thus, a resistor to ground yields a voltage proportional to the input carrier signal level. The value of this resistor is estimated by $(V_{CC}(Vdc) - 1.0\ V)/60\ \mu A$; so for V_{CC} = 4.0 Vdc, the resistor is approximately 50 kΩ and provides a maximum voltage swing of about 3.0 V.

A simple inverting op amp has an output at Pin 11 and the inverting input at Pin 10. The noninverting input is connected to 2.5 V. The op amp may be used as a noise triggered squelch or as an active noise filter. The bandpass filter is designed with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal is checked for a tone signal or for the presence of noise above the normal audio band. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that the audio mute (Pin 14) is open or connected to ground. If Pin 12 is pulled down to 0.9 V or below by the noise or tone detector, Pin 14 is internally shorted to ground. There is about 57 mV of hyteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to the appropriate point in the audio

path between Pin 9 and an audio amplifier. The voltage at Pin 14 should not be lower than −0.7 V; this can be assured by connecting Pin 14 to the point that has no dc component.

Another possible application of the squelch switch may be as a carrier level triggered squelch circuit, similar to the MC3362/MC3363 FM receivers. In this case the meter output can be used directly to trigger the squelch switch when the RF input at the input frequency falls below the desired level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 13) and ground (Pin 15).

FIGURE 10 — TYPICAL APPLICATION FOR MC3371 AT 10.7 MHz

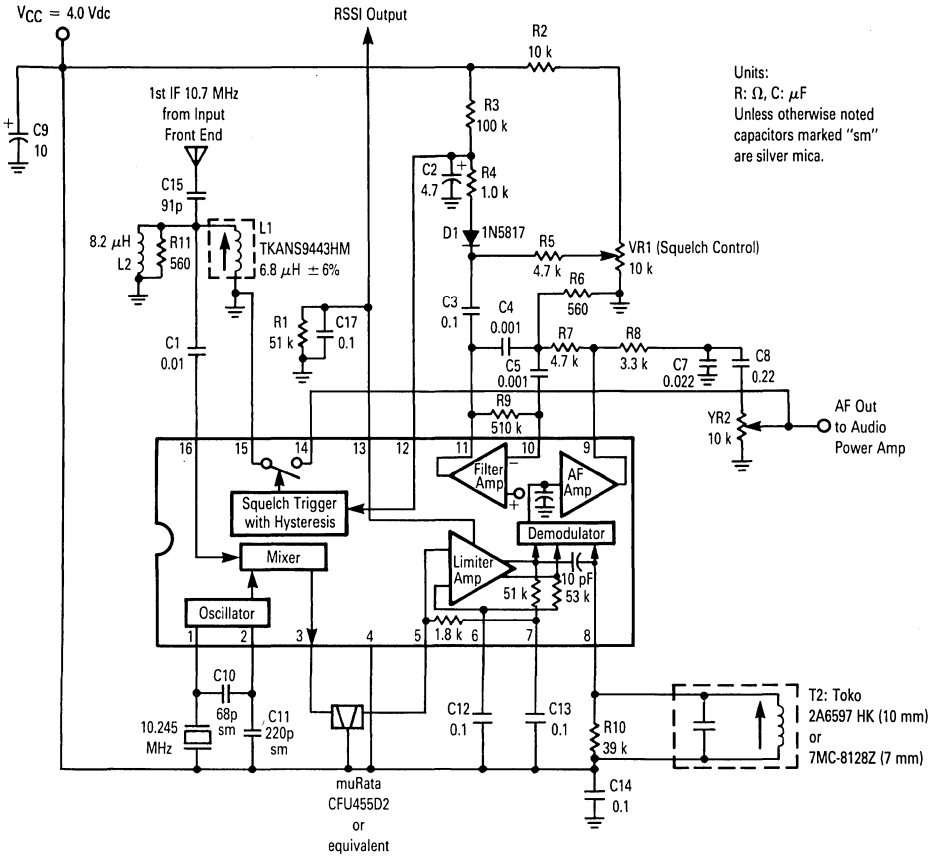


FIGURE 11 — TYPICAL APPLICATION FOR MC3372 AT 10.7 MHz

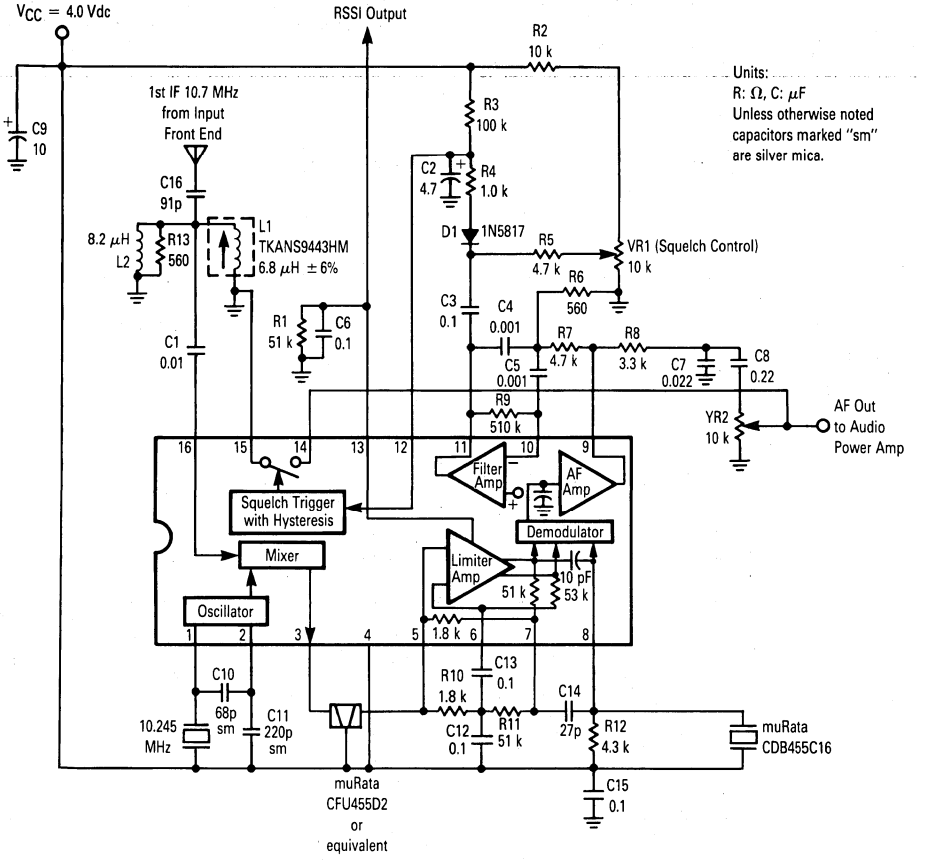


FIGURE 12 — TYPICAL APPLICATION FOR MC3372 AT 45 MHz

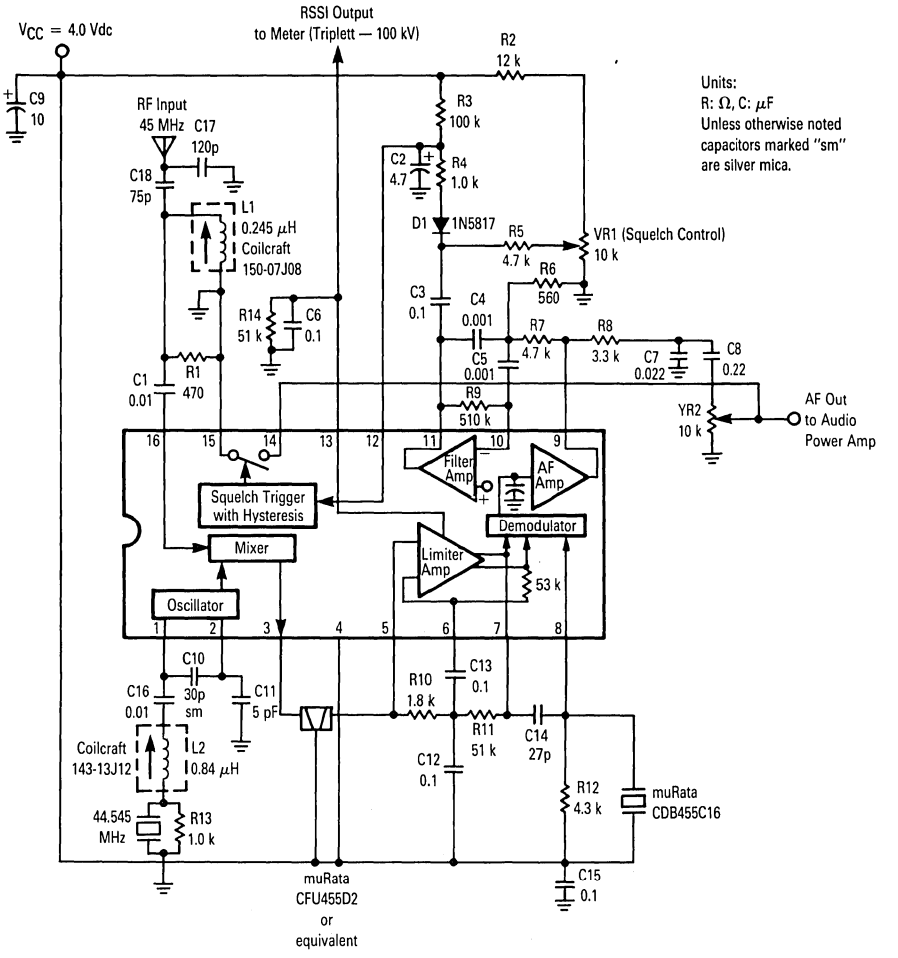


FIGURE 13 — RSSI OUTPUT versus RF INPUT

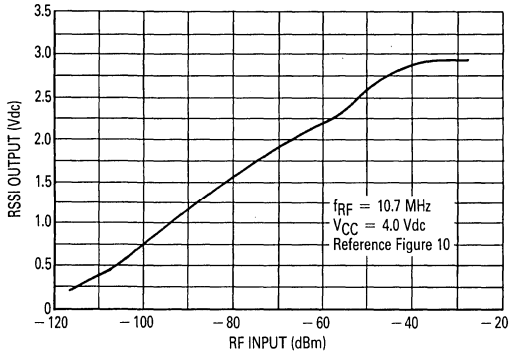


FIGURE 14 — RSSI OUTPUT versus RF INPUT

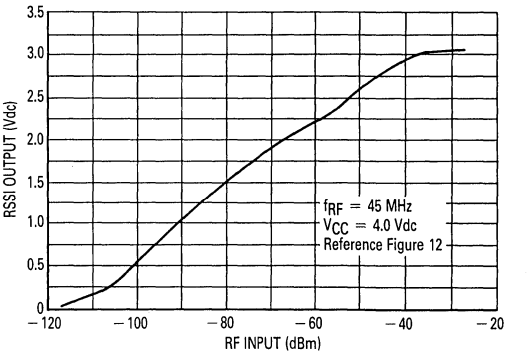
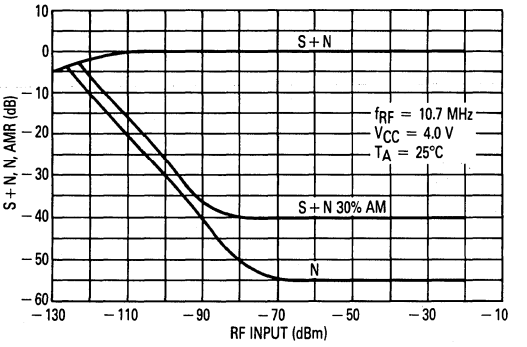


FIGURE 15 — S+N, N, AMR versus INPUT



*REFERENCE FIGURES 10, 11 & 12

FIGURE 16 — MIXER INPUT IMPEDANCE versus FREQUENCY

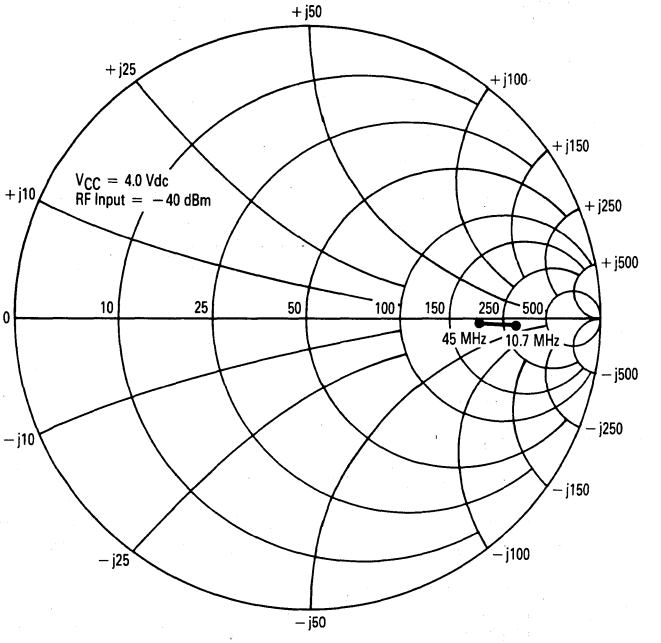


FIGURE 17 — MC3371P PC BOARD COMPONENT VIEW WITH MATCHED INPUT AT 10.7 MHz

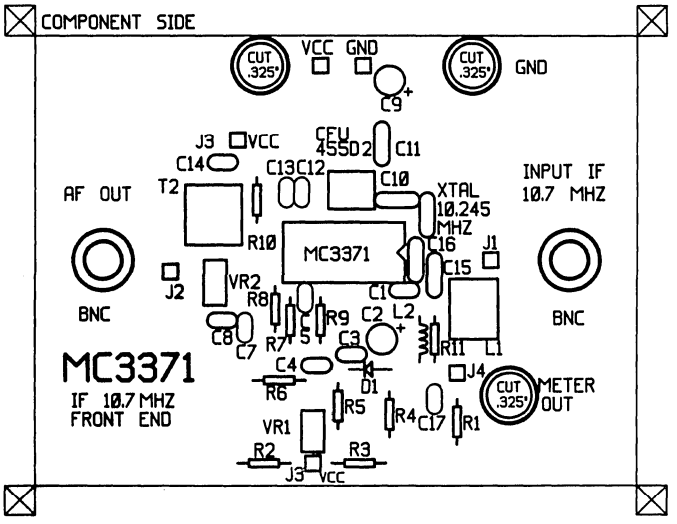
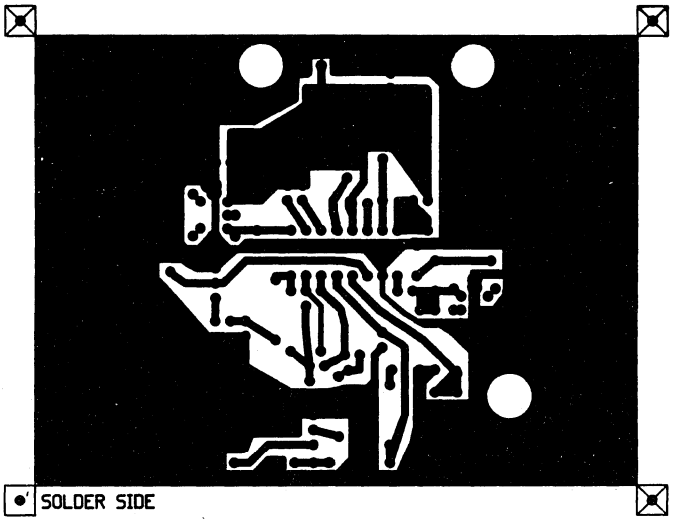


FIGURE 18 — MC3371P PC BOARD CIRCUIT OR SOLDER SIDE AS VIEWED THRU COMPONENT SIDE



Above PC Board is laid out for the circuit in Figure 10.

FIGURE 19 — MC3372P PC BOARD COMPONENT VIEW WITH MATCHED INPUT AT 10.7 MHz

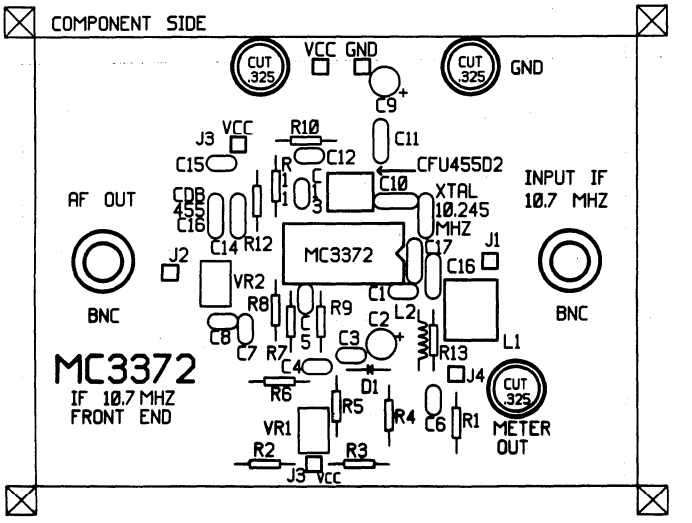
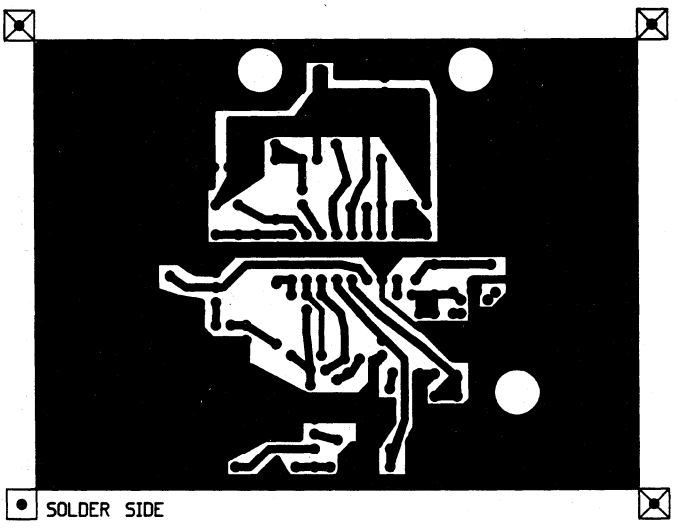


FIGURE 20 — MC3372P PC BOARD CIRCUIT OR SOLDER SIDE AS VIEWED THRU COMPONENT SIDE



Above PC Board is laid out for the circuit in Figure 11.

MC34C86

Product Preview

Quad EIA-422-A Line Receiver
CMOS

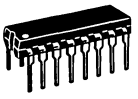
The MC34C86 is a quad differential line receiver designed for digital data transmission over balanced lines. The MC34C86 meets all the requirements of standard EIA-422-A while retaining the low-power characteristics of CMOS.

The MC34C86 has an input sensitivity of 200 mV over the common mode input voltage range of ± 7 V. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

The MC34C86 is pin compatible with the MC3486.

All pins are protected against damage due to electrostatic discharges.

- Typical Power Supply Current: 6 mA
- 2000-V ESD Protection on the Inputs and Outputs
- Typical Propagation Delay: 18 ns
- Typical Input Hysteresis: 75 mV
- Meets the Requirements of Standard EIA-422-A
- Operation from Single 5-V Supply
- High-Impedance Mode for Outputs Connected to System Buses
- TTL/CMOS Compatible Outputs



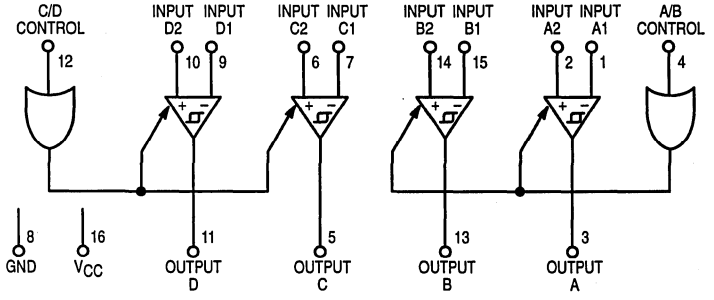
P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC34C86P	Plastic DIP
MC34C86D	SOG Package

BLOCK DIAGRAM



This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV. 3

TRUTH TABLE

Control Input	Input	Output
L	X	Z
H	$V_{ID} \geq V_{TH}$ (Max)	1
H	$V_{ID} \leq V_{TH}$ (Min)	0
H	Open	1

X = Don't Care
Z = High Impedance
H = High Logic State
L = Low Logic State

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
Input Voltage	V_I	±12	V
Input Differential Voltage	V_{ID}	±14	V
Enable Control Input Voltage	V_{in}	V_{CC} + 0.5	V
Storage Temperature	T_{stg}	−65 to +150	°C
Maximum Current per Output	I_O	±25	mA
ESD (Human Body model)		2000	V

OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
Operating Temperature Range	T_A	− 40	+ 85	°C
Input Rise and Fall Time	t_r, t_f	—	500	ns

DC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = − 40 to + 85°C, unless otherwise stated) (See Note 1)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supply Current, V_{CC} = Max		I_{CC}	—	6	12	mA
Enable Input Current, V_{in} = V_{CC} or GND		I_L	—	—	±1.0	µA
Input Voltage — Low Logic State (Enable Control)		V_{IL}	—	—	0.8	V
Input Voltage — High Logic State (Enable Control)		V_{IH}	2	—	—	V
Differential Input Voltage, − 7 V < V_{LCM} < 7 V	V_{out} = V_{OH} V_{out} = V_{OL}	V_{TH}	0.2 —	— —	— − 0.2	V
Input Hysteresis, V_{LCM} = 0 V		V_{hys}	—	75	—	mV
Comparator Input Current	V_{in} = + 10 V, Other Input = GND V_{in} = − 10 V, Other Input = GND	I_{in}	— —	1.4 − 2.5	— —	mA
Comparator Input Resistance, − 12 V < V_{LCM} < + 12 V		R_{in}	4	4.8	—	kΩ
Output Voltage (Low Logic State) V_{ID} = − 1 V, I_{out} = 6 mA (Note 2)		V_{OL}	—	0.13	0.33	V
Output Voltage (High Logic State) V_{ID} = + 1 V, I_{out} = − 6 mA (Note 2)		V_{OH}	3.8	4.8	—	V
Output Leakage Current (High Logic State) V_{out} = V_{CC} or GND		I_{OZ}	− 5	—	5	µA

NOTES:
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. See EIA specifications EIA-422-A for exact test conditions.

AC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay Input to Output, C_L = 50 pF, V_{DIFF} = 2.5 V	t_{PLH} t_{PHL}	—	18	30	ns
Skew = $\lvert t_{PHL} - t_{PLH} \rvert$	Skew	—	1	—	ns
Propagation Delay Enable to Output C_L = 50 pF, R_L = 1000 Ω, V_{DIFF} = 2.5 V	t_{PLZ} t_{PHZ}	—	12	—	ns
Propagation Delay Enable to Output C_L = 50 pF, R_L = 1000 Ω, V_{DIFF} = 2.5 V	t_{PZL} t_{PZH}	—	14	—	ns

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

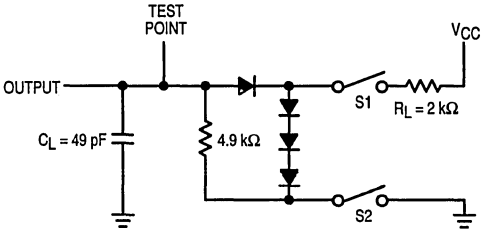


Figure 1. Test Circuit

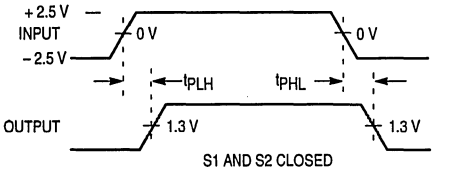


Figure 2. Propagation Delays

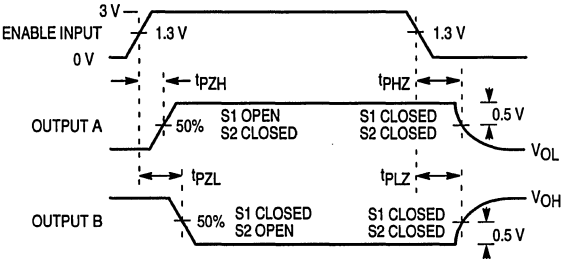


Figure 3. Enable and Disable Times

TYPICAL APPLICATIONS

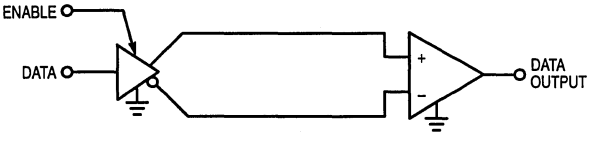


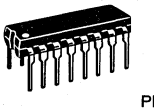
Figure 4. Two-Wire Balanced Systems (EIA-422-A)

MC34C87

Product Preview

Quad EIA-422-A Line Driver

CMOS



P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
SOG PACKAGE
CASE 751B

ORDERING INFORMATION

MC34C87P	Plastic DIP
MC34C87D	SOG Package

The MC34C87 is a quad differential line driver designed for digital data transmission over balanced lines. The MC34C87 meets all the requirements of standard EIA-422-A while retaining the low-power characteristics of CMOS.

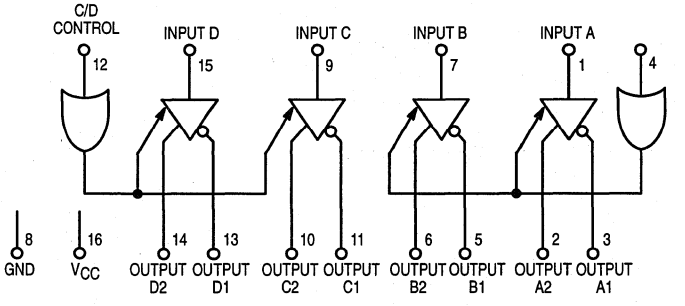
The MC34C87 accepts TTL or CMOS input levels and translates these to EIA-422-A output level. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. The MC34C87 also includes special circuitry which will set the outputs to a high impedance mode during power up or down, preventing spurious glitches. Each enable pin controls 2 drivers.

The MC34C87 is pin compatible with the MC3487.

All pins are protected against damage due to electrostatic discharges.

- Maximum Power Supply Current: 3 mA
- 2000-V ESD Protection on the Inputs and the Outputs
- TTL/CMOS Input Compatible
- Typical Propagation Delay: 6 ns
- Typical Output Skew: 1 ns
- Meets V_O = 6.0 V (and V_O = – 0.25 V), V_{CC} = 0 V, I_O < 100 µA Requirement
- Operation from Single 5-V Supply
- High-Impedance Mode for Outputs Connected to System Buses

BLOCK DIAGRAM



This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV. 3

TRUTH TABLE

Control Input	Input	Non-Inverting Output	Inverting Output
L	X	Z	Z
H	H	H	L
H	L	L	H

X = Don't Care
Z = High Impedance
H = High Logic State
L = Low Logic State

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
DC Input Voltage	V_{in}	-1.5 to $V_{CC}+1.5$	V
DC Output Voltage*	V_{out}	-0.5 to $V_{CC}+0.5$	V
DC Output Current, per Pin	I_{out}	150	mA
DC V_{CC} or GND Current, per Pin	I_{DD}	150	mA
Storage Temperature	T_{stg}	-65 to $+150$	°C
Power Dissipation	P_D	500	mW
ESD (Human Body model)		2000	V

* Power-on conditions.

OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.5	V
DC Input Voltage	V_{in}	0	V_{CC}	V
Operating Temperature Range	T_A	-40	$+85$	°C
Input Rise and Fall Time	t_r, t_f	—	500	ns

DC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, $T_A = -40$ to $+85$°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage (Low Logic State)	V_{IL}	—	—	0.8	V
Input Voltage (High Logic State)	V_{IH}	2.0	—	—	V
Output Voltage (Low Logic State) I_{sink} = 20 mA	V_{OL}	—	0.3	0.5	V
Output Voltage (High Logic State) $I_{source} = -20$ mA	V_{OH}	2.5	2.8	—	V
Output Differential Voltage R_L = 100 Ω (Note 1)	V_{OD}	2.0	—	—	V
Output Differential Voltage Difference R_L = 100 Ω (Note 1)	$D(V_{OD})$	—	—	±0.4	V
Output Offset Voltage R_L = 100 Ω (Note 1)	V_{OS}	—	—	3.0	V
Output Offset Voltage Difference R_L = 100 Ω (Note 1)	$D(V_{OS})$	—	—	±0.4	V
Input Current $V_{in} = V_{CC}$, GND, V_{IH} or V_{IL}	I_{in}	—	—	±1.0	µA
Quiescent Supply Current I_{out} = 0 µA	I_{CC}	—	—	3.0	mA
Output Short Circuit Current (Note 2)	I_{OS}	-30	-100	-150	mA
Output Leakage Current (Hi-Z State) $V_{out} = V_{CC}$ or GND	$I_{O(Z)}$	—	—	±1.0	µA
Output Leakage Current (Power Off) V_{out} = 6 V	I_{oxh}	—	—	100	µA
$V_{out} = -0.25$ V	I_{oxl}	—	—	-100	

NOTES:
1. See EIA specifications EIA-422-A for exact test conditions.
2. Only one output may be shorted at a time.

AC CHARACTERISTICS (V_{CC} = 4.5 to 5.5 V, T_A = – 40 to + 85°C, unless otherwise stated)

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay Input to Output (S1 Open)	t_{PLH} t_{PHL}	—	6	12	ns
Output Skew (S1 Open)*	Skew	—	1.0	4	ns
Differential Output Rise Time Fall Time (S1 Open)	t_{TLH} t_{THL}	—	4	8	ns
Output Enable Time (S1 Closed)	t_{PZH} t_{PZL}	— —	16 15	— —	ns
Output Disable Time (S1 Closed)	t_{PHZ} t_{PLZ}	— —	6 9	— —	ns

* Skew: difference in propagation delays between complementary outputs.

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS

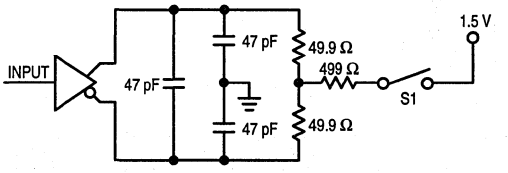


Figure 5. AC Test Circuit

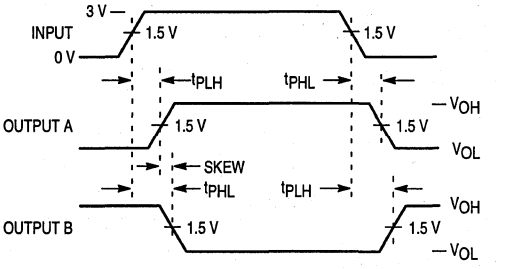


Figure 6. Propagation Delays and Skew Waveforms

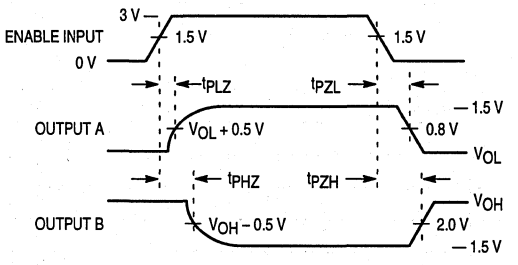


Figure 7. Enable and Disable Times

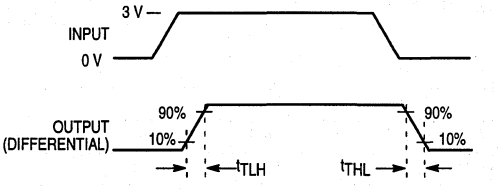


Figure 8. Differential Rise and Fall Times

TYPICAL APPLICATIONS

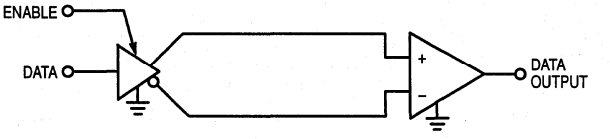


Figure 9. Two-Wire Balanced Systems (EIA-422-A)

MC3417, MC3517
MC3418, MC3518

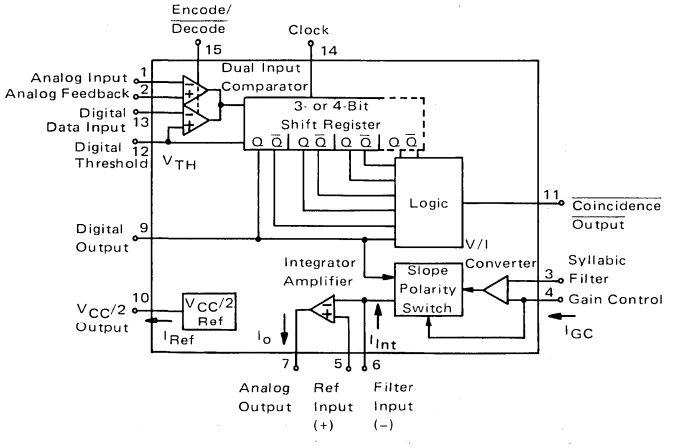
Specifications and Applications Information

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

Providing a simplified approach to digital speech encoding/decoding, the MC3517/18 series of CVSDs is designed for military secure communication and commercial telephone applications. A single IC provides both encoding and decoding functions.

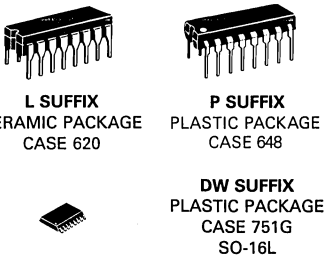
- Encode and Decode Functions on the Same Chip with a Digital Input for Selection
- Utilization of Compatible I^2L – Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- MC3417/MC3517 has a 3-Bit Algorithm (General Communications)
- MC3418/MC3518 has a 4-Bit Algorithm (Commercial Telephone)

CVSD BLOCK DIAGRAM



CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

LASER-TRIMMED INTEGRATED CIRCUIT

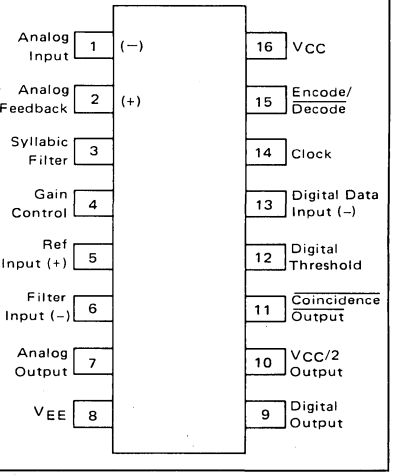


L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

DW SUFFIX
PLASTIC PACKAGE
CASE 751G
SO-16L

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Temperature Range
MC3417L	Ceramic DIP	0°C to +70°C
MC3418DW	Plastic SOIC	0°C to +70°C
MC3418L	Ceramic DIP	0°C to +70°C
MC3418P	Plastic DIP	0°C to +70°C
MC3517L	Ceramic DIP	−55°C to +125°C
MC3518L	Ceramic DIP	−55°C to +125°C

MAXIMUM RATINGS

(All voltages referenced to V_{EE}, T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{TH}	−0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	−0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	−0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(SyI)}$	−0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	−0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	$V_{CC}/2$ − 1.0 to V_{CC}	Vdc
$V_{CC}/2$ Output Current	I_{Ref}	−25	mA

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0°C to +70°C for MC3417/18, T_A = −55°C to +125°C for MC3517/18 unless otherwise noted.)

Characteristic	Symbol	MC3417/MC3517			MC3418/MC3518			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage Range (Figure 1)	V_{CCR}	4.75	12	16.5	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) (@ Idle Channel)	I_{CC}							mA
(V_{CC} = 5.0 V, All except MC3418P,DW)		—	3.7	5.0	—	3.7	5.0	
(V_{CC} = 5.0 V, MC3418P,DW)		—	—	—	—	3.7	5.5	
(V_{CC} = 15 V, All except MC3418P,DW)		—	6.0	10	—	6.0	10	
(V_{CC} = 15 V, MC3418P,DW)		—	—	—	—	6.0	11	
Gain Control Current Range (Figure 2)	I_{GCR}	0.002	—	3.0	0.002	—	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) (4.75 V ≤ V_{CC} ≤ 16.5 V)	V_I	1.3	—	V_{CC} − 1.3	1.3	—	V_{CC} − 1.3	Vdc
Analog Output Range (Pin 7) (4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ±5.0 mA)	V_O	1.3	—	V_{CC} − 1.3	1.3	—	V_{CC} − 1.3	Vdc
Input Bias Currents (Figure 3) (Comparator in Active Region)	I_{IB}							μA
Analog Input (I1)		—	0.5	1.5	—	0.25	1.0	
Analog Feedback (I2)		—	0.5	1.5	—	0.25	1.0	
Syllabic Filter Input (I3)		—	0.06	0.5	—	0.06	0.3	
Reference Input (I5)		—	−0.06	−0.5	—	−0.06	−0.3	
Input Offset Current (Comparator in Active Region)	I_{IO}							μA
Analog Input/Analog Feedback |I1 − I2| — Figure 3		—	0.15	0.6	—	0.05	0.4	
Integrator Amplifier |I5 − I6| — Figure 4		—	0.02	0.2	—	0.01	0.1	
Input Offset Voltage V/I Converter (Pins 3 and 4) — Figure 5	V_{IO}	—	2.0	6.0	—	2.0	6.0	mV
Transconductance	gm							mA/mV
V/I Converter, 0 to 3.0 mA		0.1	0.3	—	0.1	0.3	—	
Integrator Amplifier, 0 to ±5.0 mA Load		1.0	10	—	1.0	10	—	
Propagation Delay Times (Note 1)								μs
Clock Trigger to Digital Output	t_{PLH}	—	1.0	2.5	—	1.0	2.5	
(C_L = 25 pF to Gnd)	t_{PHL}	—	0.8	2.5	—	0.8	2.5	
Clock Trigger to Coincidence Output	t_{PLH}	—	1.0	3.0	—	1.0	3.0	
(C_L = 25 pF to Gnd) (R_L = 4.0 kΩ to V_{CC})	t_{PHL}	—	0.8	2.0	—	0.8	2.0	
Coincidence Output Voltage — Low Logic State ($I_{OL(Con)}$ = 3.0 mA)	$V_{OL(Con)}$	—	0.12	0.25	—	0.12	0.25	Vdc
Coincidence Output Leakage Current — High Logic State (V_{OH} = 15 V, 0°C ≤ T_A ≤ 70°C)	$I_{OH(Con)}$	—	0.01	0.5	—	0.01	0.5	μA

NOTE 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	MC3417/MC3517 Min	MC3417/MC3517 Typ	MC3417/MC3517 Max	MC3418/MC3518 Min	MC3418/MC3518 Typ	MC3418/MC3518 Max	Unit
Applied Digital Threshold Voltage Range (Pin 12)	V_{TH}	+1.2	—	$V_{CC}-2.0$	+1.2	—	$V_{CC}-2.0$	Vdc
Digital Threshold Input Current ($1.2\ V \leq V_{th} \leq V_{CC} - 2.0\ V$)	$I_{I(th)}$							μA
(V_{IL} applied to Pins 13, 14 and 15)		—	—	5.0	—	—	5.0	
(V_{IH} applied to Pins 13, 14 and 15)		—	−10	−50	—	−10	−50	
Maximum Integrator Amplifier Output Current	I_O	±5.0	—	—	±5.0	—	—	mA
$V_{CC}/2$ Generator Maximum Output Current (Source only)	I_{Ref}	+10	—	—	+10	—	—	mA
$V_{CC}/2$ Generator Output Impedance (0 to +10 mA)	z_{Ref}	—	3.0	6.0	—	3.0	6.0	Ω
$V_{CC}/2$ Generator Tolerance ($4.75\ V \leq V_{CC} \leq 16.5\ V$)	ϵ_r	—	—	±3.5	—	—	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15)								Vdc
Low Logic State	V_{IL}	Gnd	—	$V_{th}-0.4$	Gnd	—	$V_{th}-0.4$	
High Logic State	V_{IH}	$V_{th}+0.4$	—	18	$V_{th}+0.4$	—	18	
Dynamic Total Loop Offset Voltage (Note 2) — Figures 3, 4 and 5	ΣV_{offset}							mV
I_{GC} = 12 μA, V_{CC} = 12 V								
T_A = 25°C (All except 3418P,DW)		—	—	—	—	±0.5	±1.5	
(MC3418P,DW)		—	—	—	—	±0.5	±3.0	
$0°C \leq T_A \leq +70°C$ (MC3417/18L)		—	—	—	—	±0.75	±2.3	
(MC3418P,DW)		—	—	—	—	±0.75	±3.8	
$-55°C \leq T_A \leq +125°C$ (MC3517/18)		—	—	—	—	±1.5	±4.0	
I_{GC} = 33 μA, V_{CC} = 12 V								
T_A = 25°C		—	±2.5	±5.0	—	—	—	
$0°C \leq T_A \leq +70°C$ (MC3417/18)		—	±3.0	±7.5	—	—	—	
$-55°C \leq T_A \leq +125°C$ (MC3517/18)		—	±4.5	±10	—	—	—	
I_{GC} = 12 μA, V_{CC} = 5.0 V								
T_A = 25°C (All except MC3418P,DW)		—	—	—	—	±1.0	±2.0	
(MC3418P,DW)		—	—	—	—	±1.0	±3.5	
$0°C \leq T_A \leq +70°C$ (MC3417/18L)		—	—	—	—	±1.3	±2.8	
(MC3418P,DW)		—	—	—	—	±1.3	±4.3	
$-55°C \leq T_A \leq +125°C$ (MC3517/18)		—	—	—	—	±2.5	±5.0	
I_{GC} = 33 μA, V_{CC} = 5.0 V								
T_A = 25°C		—	±4.0	±6.0	—	—	—	
$0°C \leq T_A \leq +70°C$ (MC3417/18)		—	±4.5	±8.0	—	—	—	
$-55°C \leq T_A \leq +125°C$ (MC3517/18)		—	±5.5	±10	—	—	—	
Digital Output Voltage								Vdc
(I_{OL} = 3.6 mA)	V_{OL}	—	0.1	0.4	—	0.1	0.4	
(I_{OH} = −0.35 mA)	V_{OH}	$V_{CC}-1.0$	$V_{CC}-0.2$	—	$V_{CC}-1.0$	$V_{CC}-0.2$	—	
Syllabic Filter Applied Voltage (Pin 3) (Figure 2)	$V_{I(Syl)}$	+3.2	—	V_{CC}	+3.2	—	V_{CC}	Vdc
Integrating Current (Figure 2)	$\lvert I_{Int}\rvert$							
(I_{GC} = 12 μA)		8.0	10	12	8.0	10	12	μA
(I_{GC} = 1.5 mA) (All except 3418P,DW)		1.45	1.5	1.55	1.45	1.5	1.55	mA
(MC3418P,DW)		—	—	—	1.42	1.5	1.58	mA
(I_{GC} = 3.0 mA)		2.75	3.0	3.25	2.75	3.0	3.25	mA
Dynamic Integrating Current Match (I_{GC} = 1.5 mA) Figure 6	$V_{O(Ave)}$							mV
(All except MC3418P,DW)		—	±100	±250	—	±100	±250	
(MC3418P,DW)		—	—	—	—	±100	±280	
Input Current — High Logic State (V_{IH} = 18 V)	I_{IH}							μA
Digital Data Input		—	—	+5.0	—	—	+5.0	
Clock Input		—	—	+5.0	—	—	+5.0	
Encode/Decode Input		—	—	+5.0	—	—	+5.0	
Input Current — Low Logic State (V_{IL} = 0 V)	I_{IL}							μA
Digital Data Input		—	—	−10	—	—	−10	
Clock Input		—	—	−360	—	—	−360	
Encode/Decode Input		—	—	−36	—	—	−36	
Clock Input, V_{IL} = 0.4 V		—	—	−72	—	—	−72	

NOTE 2. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. For the MC3417/MC3517, the clock frequency is 16 kHz. For the MC3418/MC3518, the clock frequency is 32 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size). Laser trimming is used to insure good idle channel performance.

DEFINITIONS AND FUNCTION OF PINS

Pin 1 — Analog Input

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between Pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

Pin 2 — Analog Feedback

This is the noninverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be Pin 7 or a low pass filter output connected to Pin 7. In a decode circuit Pin 2 is not used and may be tied to $V_{CC}/2$ on Pin 10, ground or left open.

The analog input comparator has bias currents of 1.5 μA max, thus the driving impedances of Pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 — Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between Pins 11 and 3. Typical time constant values of 6.0 ms to 50 ms are used in voice codecs.

Pin 4 — Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and Pin 3. The active voltage to current (V−I) converter drives Pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into Pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_X resistance. Figure 7 shows the relationship between I_{GC} (x-axis) and the integrating current, I_{Int} (y-axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The R_X resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 — Reference Input

This pin is the noninverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as Pin 1 and is tied to Pin 10.

Pin 6 — Filter Input

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into Pin 6 when the analog input (Pin 1) is high with respect to the analog feedback (Pin 2) in the encode mode or when the digital data input (Pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between Pins 6 and 7. Multipole configurations will have different circuitry. The resistance between Pins 6 and 7 should always be between 8.0 kΩ and 13 kΩ to maintain good idle channel characteristics.

Pin 7 — Analog Output

This is the integrator op amp output. It is capable of driving a 600-ohm load referenced to $V_{CC}/2$ to +6.0 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

Pin 8 — V_{EE}

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

Pin 9 — Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to Pin 1 and non-inverting with respect to Pin 2. It is clocked on the falling edge of Pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

Pin 10 — $V_{CC}/2$ Output

An internal low impedance mid-supply reference is provided for use of the MC3417/18 in single supply applications. The internal regulator is a current source and must be loaded with a resistor to insure its sinking capability. If a +6.0 dBmo signal is expected across a 600 ohm input bias resistor, then Pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is only possible if Pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from Pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 — $\overline{\text{Coincidence Output}}$

The duty cycle of this pin is proportional to the voltage across C_S. The coincidence output will be low whenever the content of the internal shift register is all 1s or all 0s. In the MC3417 the register is 3 bits long while the MC3418 contains a 4 bit register. Pin 11 is an open collector of an NPN device and requires a pull-up resistor.

If the syllabic filter is to have equal charge and discharge time constants, the value of R_P should be much less than R_S. In systems requiring different charge and discharge constants, the charging constant is $R_S C_S$ while the decaying constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3.0 mA in any configuration. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for $R_L = 4.0\ k\Omega$ to $+12$ V and $C_L = 25$ pF to ground.

Pin 12 — Digital Threshold

This input sets the switching threshold for Pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Often it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 — Digital Data Input

In a decode application, the digital data stream is applied to Pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of Pin 15. It is an inverting input with respect to Pin 9. When Pins 9 and 13 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 μs before and after the clock trigger for proper clocking.

Pin 14 — Clock Input

The clock input determines the data rate of the codec circuit. A 32K bit rate requires a 32 kHz clock. The switching threshold of the clock input is set by Pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum width for a positive-going pulse on the clock input is 300 ns, whereas for a negative-going pulse, it is 900 ns.

Pin 15 — Encode/$\overline{\text{Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at Pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through Pin 13 in an encoder.

Pin 16 — V_{CC}

The power supply range is from 4.75 to 16.5 volts between Pin V_{CC} and V_{EE}.

FIGURE 1 – POWER SUPPLY CURRENT

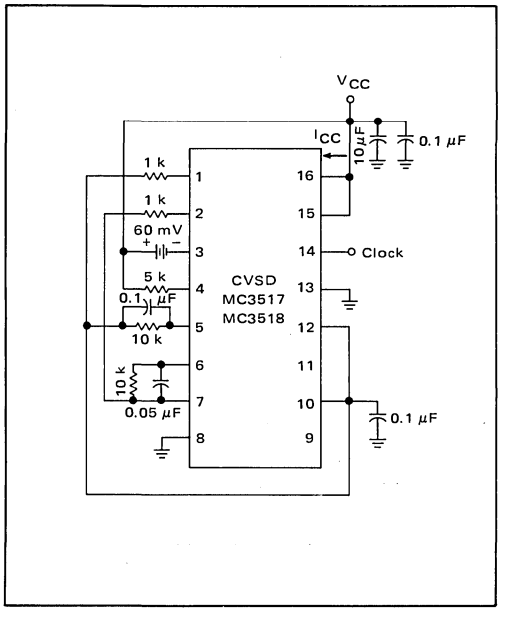
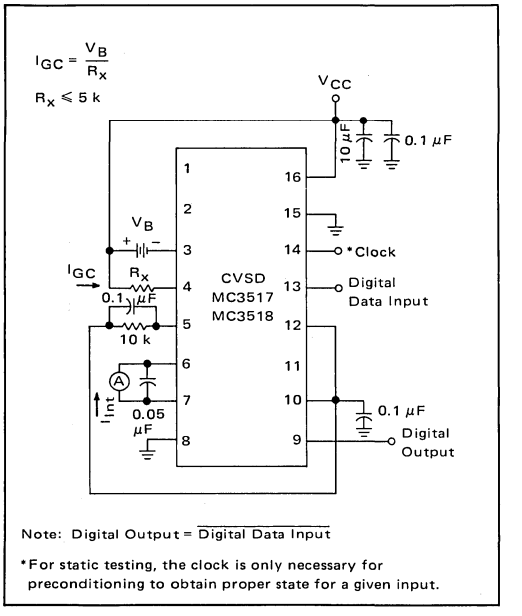


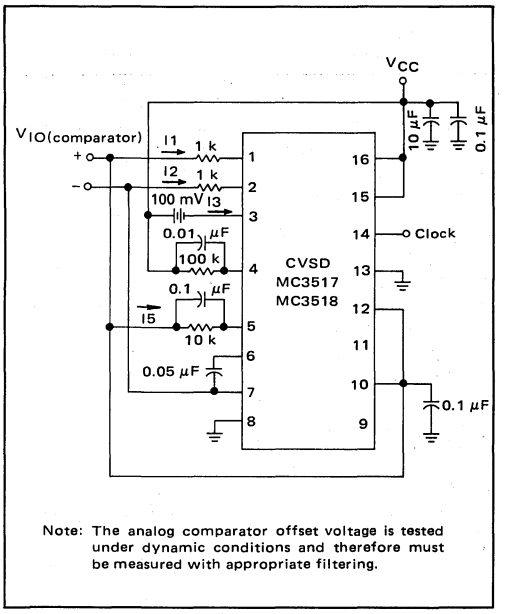
FIGURE 2 – I_{GCR}, GAIN CONTROL RANGE and I_{Int} – INTEGRATING CURRENT



Note: Digital Output = $\overline{\text{Digital Data Input}}$

*For static testing, the clock is only necessary for preconditioning to obtain proper state for a given input.

FIGURE 3 – INPUT BIAS CURRENTS, ANALOG COMPARATOR OFFSET VOLTAGE AND CURRENT



Note: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

FIGURE 4 – INTEGRATOR AMPLIFIER OFFSET VOLTAGE AND CURRENT

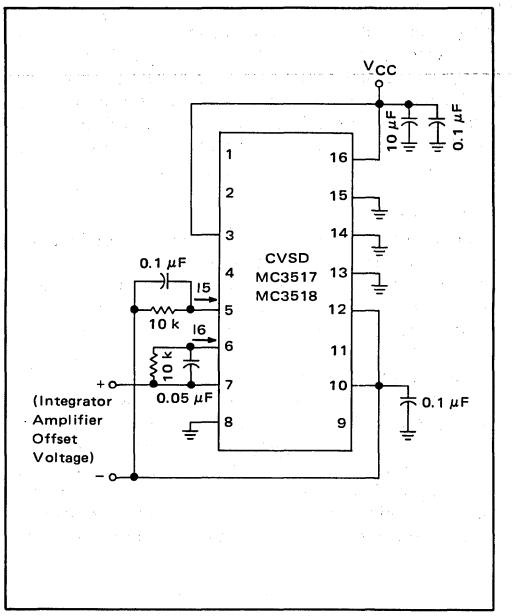
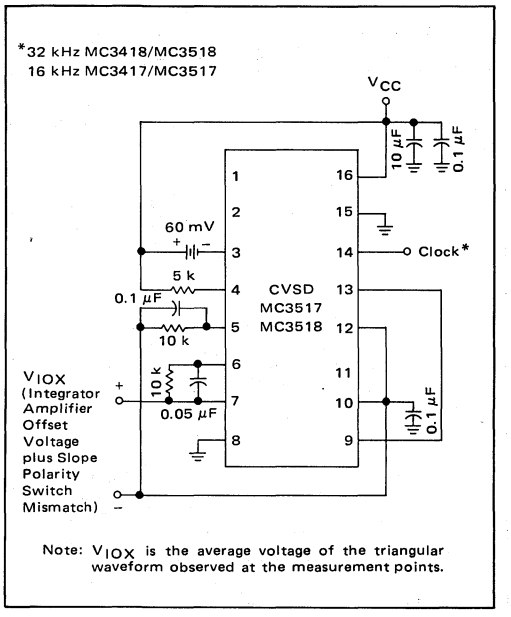
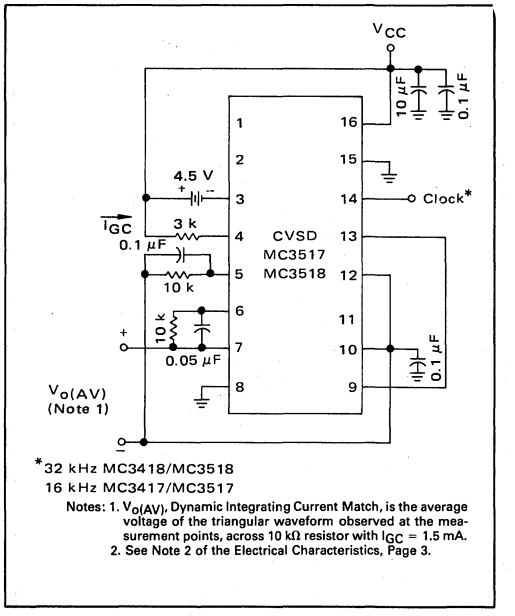


FIGURE 5 – V/I CONVERTER OFFSET VOLTAGE, V_{IO} and V_{IOX}



Note: V_{IOX} is the average voltage of the triangular waveform observed at the measurement points.

FIGURE 6 – DYNAMIC INTEGRATING CURRENT MATCH



*32 kHz MC3418/MC3518
16 kHz MC3417/MC3517

Notes: 1. $V_{o(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.
2. See Note 2 of the Electrical Characteristics, Page 3.

TYPICAL PERFORMANCE CURVES

FIGURE 7 – TYPICAL I_{Int} versus I_{GC} (Mean ± 2σ)

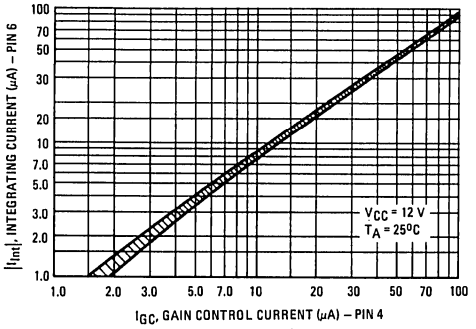


FIGURE 8 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus V_{CC}

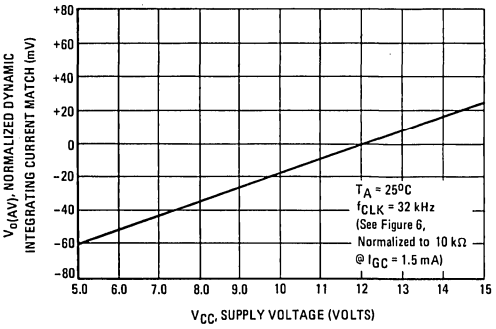


FIGURE 9 – NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus CLOCK FREQUENCY

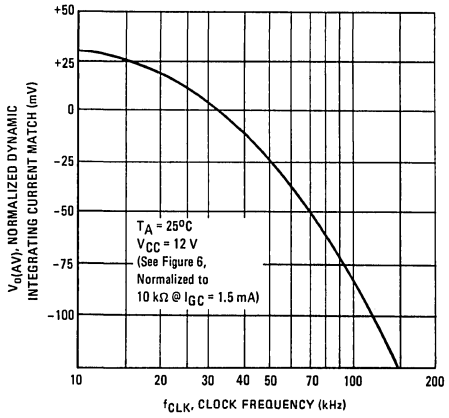


FIGURE 10 – DYNAMIC TOTAL LOOP OFFSET versus CLOCK FREQUENCY

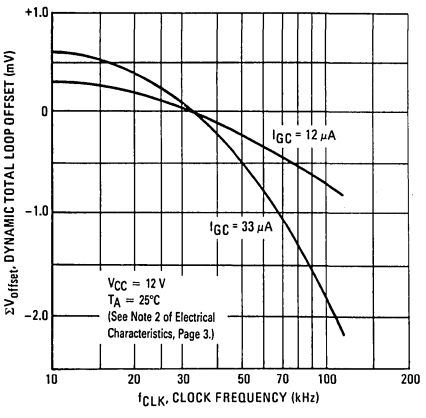


FIGURE 11 – BLOCK DIAGRAM OF THE CVSD ENCODER

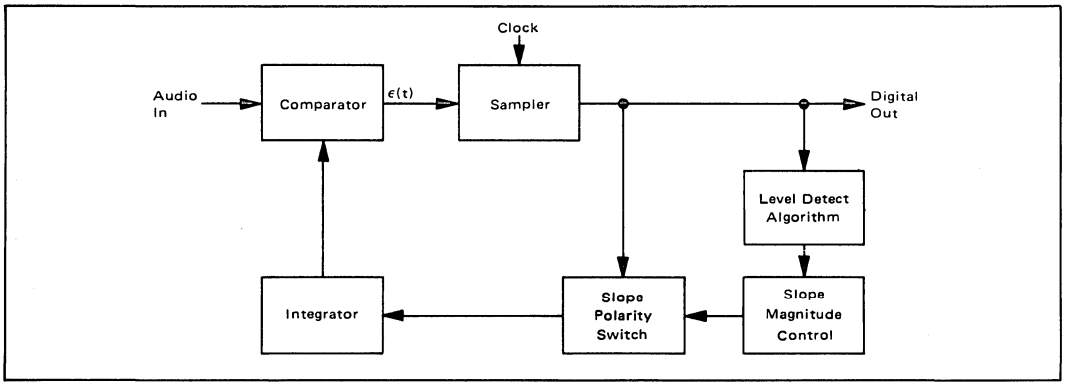


FIGURE 12 – CVSD WAVEFORMS

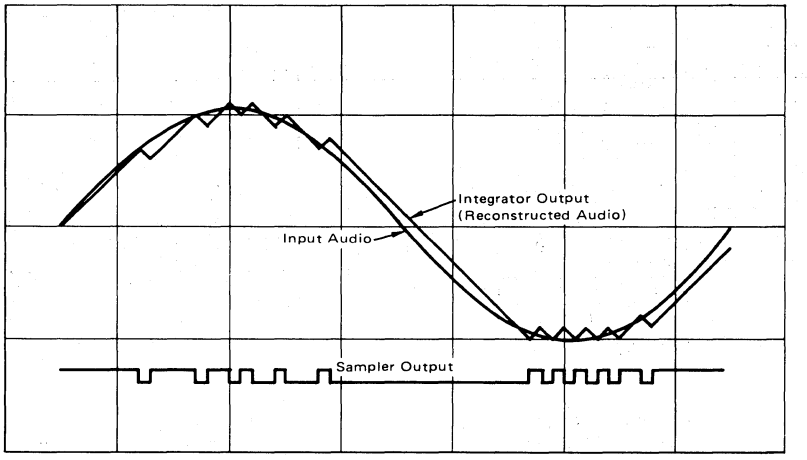


FIGURE 13 – BLOCK DIAGRAM OF THE CVSD DECODER

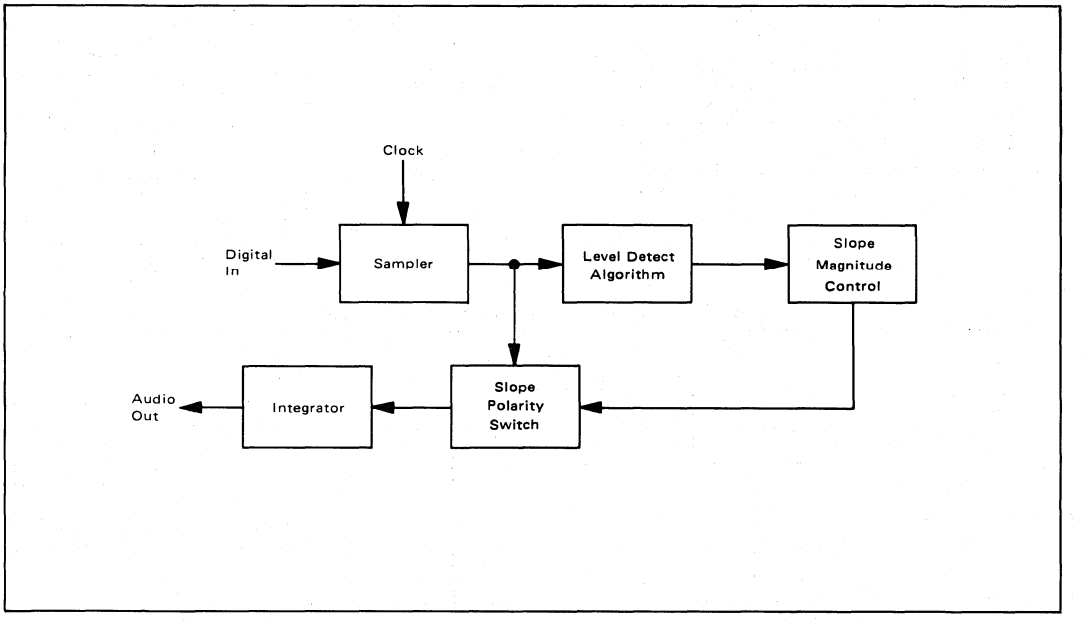
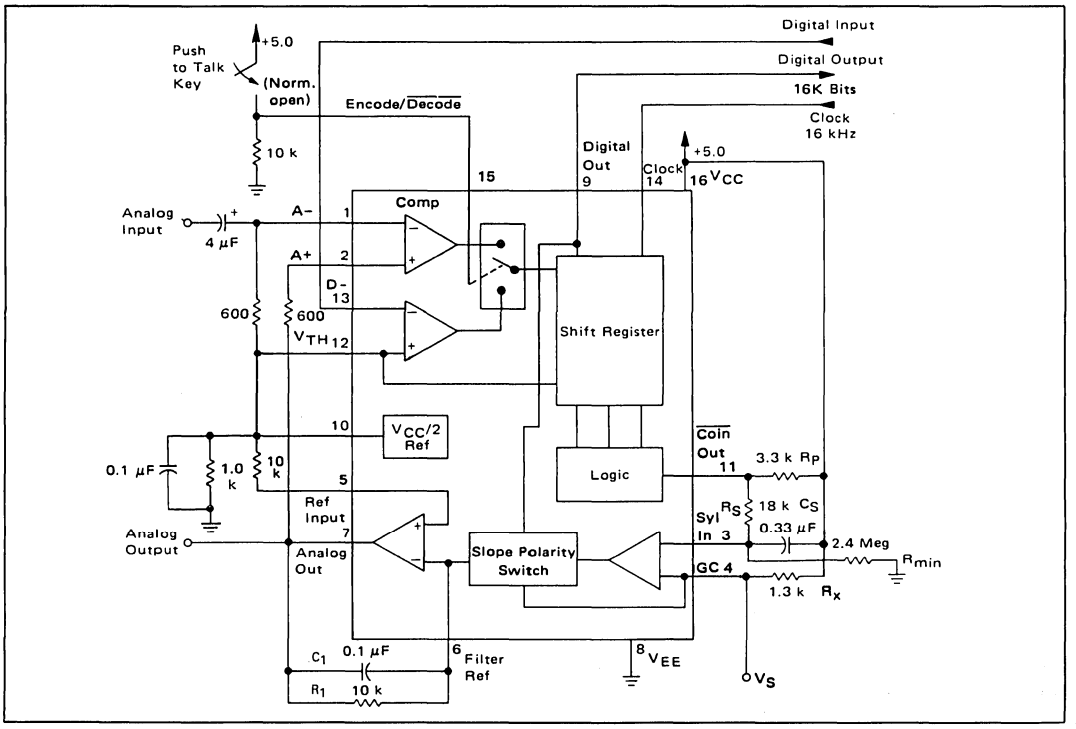


FIGURE 14 – 16 kHz SIMPLEX VOICE CODEC
(Using MC3417, Single Pole Companding and Single Integration)



CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to

zero and receive restart begins without framing when the receiver reacquires. Similarly a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 or 4 bits long depending on the application. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communciations requirements.

APPLICATIONS INFORMATION

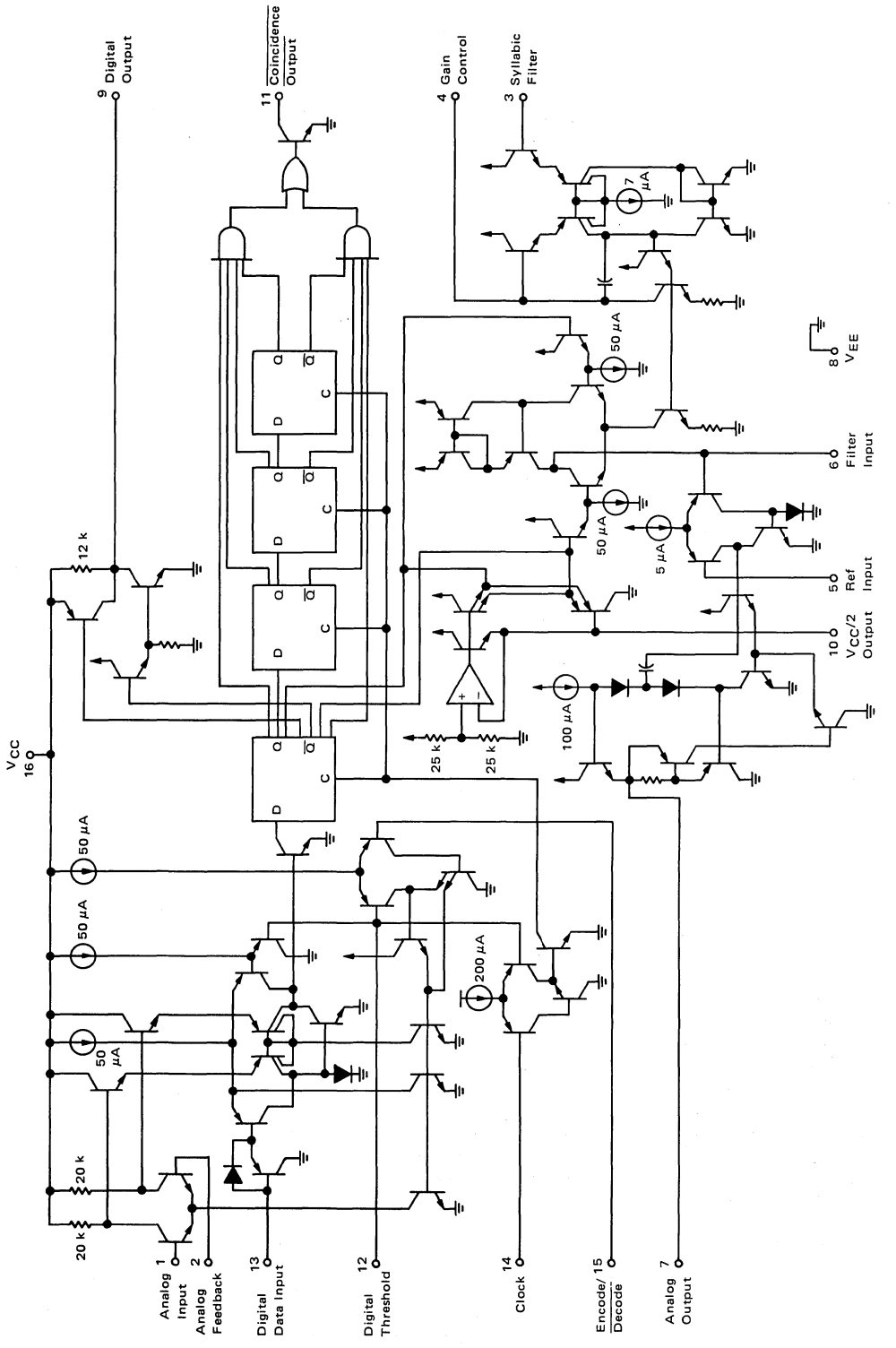
CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC3417 or MC3418 is shown in Figure 14. These ICs are general purpose CVSD building blocks which allow the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC3417 and MC3418. There are seven design considerations involved in designing these basic CVSD building blocks into a specific codec application, and they are as follows:

1. Selection of clock rate
2. Required number of shift register bits
3. Selection of loop gain
4. Selection of minimum step size
5. Design of integration filter transfer function
6. Design of syllabic filter transfer function
7. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 5 and 6 are reduced to their simplest form. The syllabic and integration filters are both single pole networks. The selection of items 1 through 4 govern the codec performance.

CVSD CIRCUIT SCHEMATIC



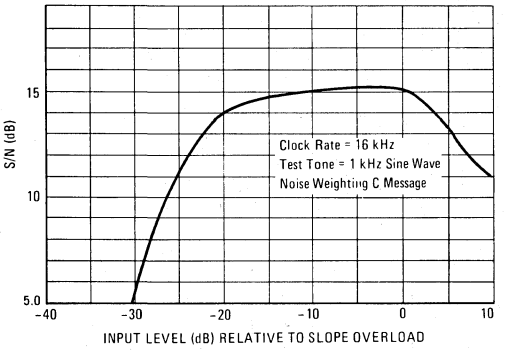
Layout Considerations

Care should be exercised to isolate all digital signal paths (Pins 9, 11, 13, and 14) from analog signal paths (Pins 1–7 and 10) in order to achieve proper idle channel performance.

Clock Rate

With minor modifications the circuit in Figure 14 may be operated anywhere from 9.6 kHz to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 15. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4-wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32K bits and above. Other codecs may use bit rates up to 200K bits/sec.

FIGURE 15 – SIGNAL-TO-NOISE PERFORMANCE OF MC3417 WITH SINGLE INTEGRATION, SINGLE-POLE AND COMPANDING AT 16K BITS – TYPICAL



Shift Register Length (Algorithm)

The MC3417 has a three-bit algorithm and the MC3418 has a four-bit algorithm. For clock rates of 16 kHz and below, the 3-bit algorithm is well suited. For 32 kHz and higher clock rates, the 4-bit system is preferred. Since the algorithm records a fixed past history of the input signal, a longer shift register is required to obtain the same internal hsitory. At 16 bits and below, the 4-bit algorithm will produce a slightly wider dynamic range at the expense of level change response. Basically the MC3417 is designed for low bit rate systems and the MC3418 is intended for high performance, high bit rate system. At bit rates above 64K bits either part will work well.

Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor R_X. R_X must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on Pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single pole of 160 Hz is used.

$$R_1 = 10\ k\Omega,\ C_1 = 0.1\ \mu F$$

$$\frac{V_o}{I_i} = \frac{1}{C(S + 1/RC)} \equiv \frac{K}{S + \omega_o}$$

$$\omega_o = 2\pi f$$

$$10^3 = \omega_o = 2\pi f$$

$$f = 159.2\ Hz$$

Note that the integration filter produces a single-pole response from 300 to 3 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_o}{R_1} + \left(C_1 \times \frac{dV_o}{dt}\right)$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1 kHz sine wave is:

$$I_i = \frac{1.1\ V}{*2(10\ k\Omega)} + \frac{0.1\ \mu F(1.1)}{0.125\ ms} = 0.935\ mA$$

*The maximum voltage across R_1 when maximum slew is required is:

$$\frac{1.1\ V}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_x = 0.25(V_{CC})\ \frac{1}{0.935\ mA}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

Minimum Step Size

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one-zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC3417 is tested to ensure that a 20 mVp-p minimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one-zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1-0 pattern.

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_o}{R_1} + C\frac{dV_o}{dt}$$

For values of V_o near $V_{CC}/2$ the V_o/R term is negligible; thus

$$I_i = C_S\frac{\Delta V_o}{\Delta T}$$

where ΔT is the clock period and ΔV_o is the desired peak-to-peak value of the idle output. For a 16K-bit system using the circuit in Figure 14

$$I_i = \frac{0.1\,\mu F\ \ 20\ mV}{62.5\,\mu s} = 33\,\mu A$$

The voltage on C_S which produces a 33 μA current is determined by the value of R_X.

$$I_i R_X = V_S min;\ \text{for } 33\,\mu A,\ V_S min = 41.6\ mV$$

In Figure 14 R_S is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of R_S and R_{min} must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_S min \qquad R_{min} \simeq 2.4\ M\Omega$$

Having established these four parameters — clock rate, number of shift register bits, loop gain and minimum step size — the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

INCREASING CVSD PERFORMANCE

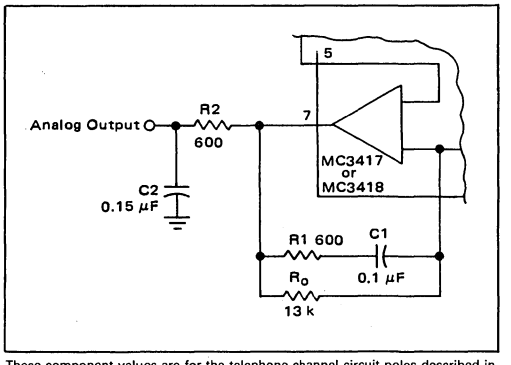
Integration Filter Design

The circuit in Figure 14 uses a single-pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1 or 2 dB by using a two-pole integration network. The improved circuit is shown.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low-pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2 kHz and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low-pass filter which breaks at about 2.5 kHz.) The two-pole network in Figure 16 has a transfer function of:

$$\frac{V_o}{I_i} = \frac{R_0R_1\left(S + \frac{1}{R_1C_1}\right)}{R_2C_2(R_0 + R_1)\left(S + \frac{1}{(R_0 + R_1)C_1}\right)S + \left(\frac{1}{R_2C_2}\right)}$$

FIGURE 16 — IMPROVED FILTER CONFIGURATION



These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on Pin 1.

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two-pole filter network effects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_o}{R_0} + \left(\frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\right)\frac{\Delta V_o}{\Delta T} + \left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\right)\frac{\Delta V_o{}^2}{\Delta T^2}.$$

The calculation of desired gain resistor R_X then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single-pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

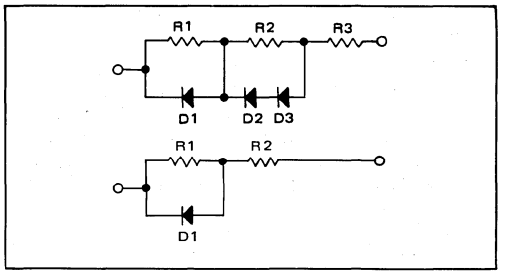
The S/N performance may be improved by modifying the voltage to current transformation produced by R_X. If different portions of the total R_X are shunted by diodes, the integrator current can be other than $(V_{CC}-V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to Pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_X in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor-diode networks are shown in Figure 17.

FIGURE 17 – RESISTOR-DIODE NETWORKS



If the performance of more complex diode networks is desired, the circuit in Figure 18 should be used. It simulates the companding characteristics of nonlinear R_X elements in a different manner.

Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 20 provides excellent performance for 12 kHz to 40 kHz systems.

TELEPHONE CARRIER QUALITY CODEC USING MC3418

Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5 mV minimum step size and a typical 1% current match from 15 μA to 3 mA. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the four-bit algorithm currently used in subscriber loop telephone systems. With these specifications and the circuit of Figure 18, a telephone quality codec can be mass produced.

The circuit in Figure 18 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1 kHz test tone at a 37.7K bit rate. At 37.7K bits, 40 voice channels may be multiplexed on a standard 1.544 megabit T1 facility. This codec has also been tested for 10^{-7} error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators and small PABX installations.

The Active Companding Network

The unique feature of the codec in Figure 18 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C_S divided by the voltage swing of the coincidence output. In Figure 18, the voltage swing of Pin 11 is 6.0 volts. The operating companding ratio is analoged by the voltage between Pins 10 and 4 by means of the virtual short across Pins 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 volts below $V_{CC}/2$, then the positive input of A1 is ($V_{CC}/2$ − 0.7). The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6.0 V).

The present step size of the operating codec is directly related to the voltage across R_X, which established the integrator current. In Figure 18, the voltage across R_X is amplified by the differential amplifier A2 whose output is single ended with respect to Pin 10 of the IC.

For large signal inputs, the step size is large and the output of A2 is lower than 0.7 volts. Thus D1 is fully on. The present step size is not a factor in the step size control. However, the difference between 12% companding ratio and the instantaneous companding ratio at Pin 4 is amplified by A1. The output of A1 changes the voltage across R_X in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at Pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on R_X, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on Pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across R_X and the gain of A2 and A1. The gain of A2 is also experimentally determined, but once determined, the circuitry is easily

FIGURE 18 – TELEPHONE QUALITY DELTAMOD CODER

(Both double integration and active companding control are used to obtain improved CVSD performance. Laser trimming of the integrated circuit provides reliable idle channel and step size range characteristics.)

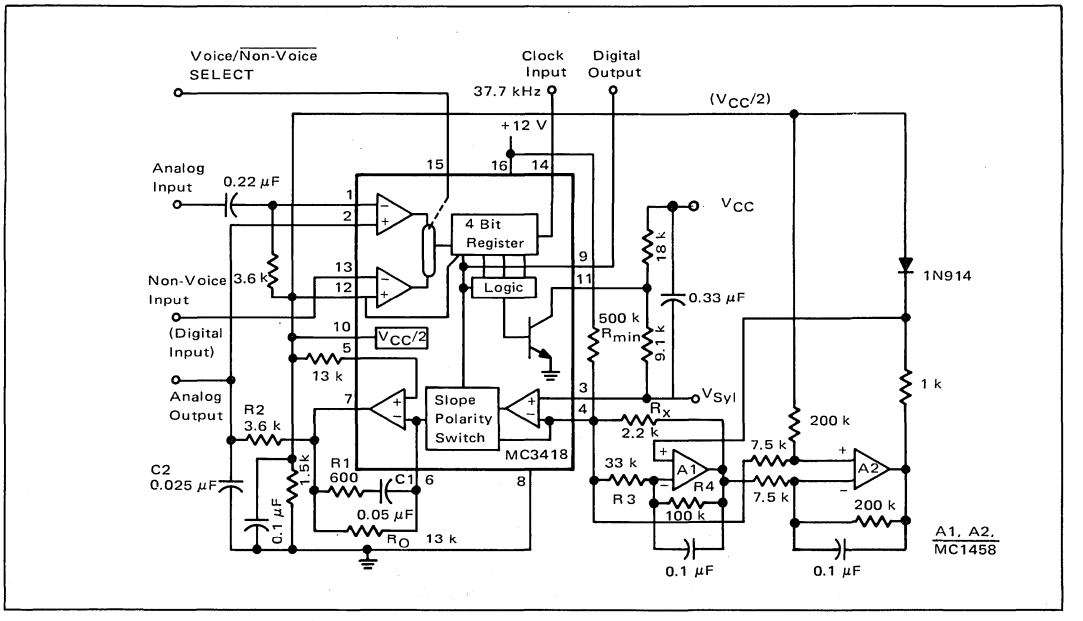
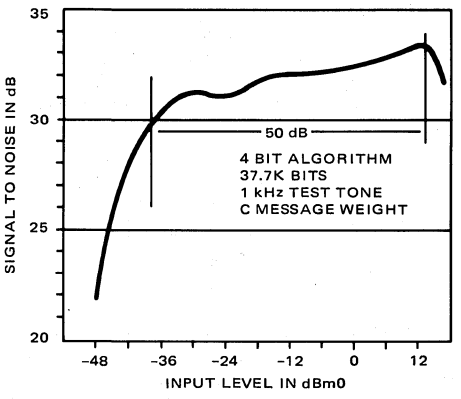
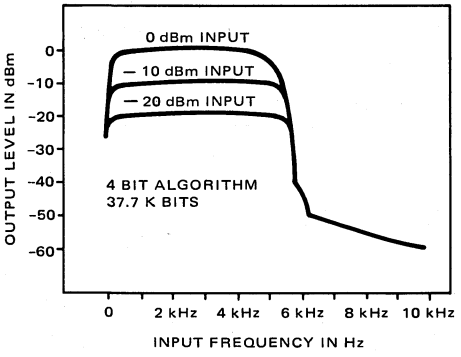


FIGURE 19 – SIGNAL-TO-NOISE PERFORMANCE AND FREQUENCY RESPONSE
(Showing the improvement realized with the circuit in Figure 18.)

a. SIGNAL-TO-NOISE PERFORMANCE OF TELEPHONY QUALITY DELTAMODULATOR



b. FREQUENCY RESPONSE versus INPUT LEVEL (SLOPE OVERLOAD CHARACTERISTIC)



repeated.

With no input signal, the companding ratio at Pin 4 goes to zero and the voltage across R_X goes to zero. The voltage at the output of A2 becomes zero since there is no drop across R_X. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between V_{CC} and $V_{CC}/2$ and is therefore independently selectable.

The signal to noise results of the active companding network are shown in Figure 19. A smooth 2 dB drop is realized from +12 dBm to –24 under the control of A1. At –24 dBm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm.

The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across R_X. The curves demonstrate that the level linearity has been maintained or improved.*

The codec in Figure 18 is designed specifically for 37.7K bit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 18 represents a significant step forward in the art and cost of CVSD codec designs.

*A larger value for C2 is required in the decoder circuit than in the encoder to adjust the level linearity with frequency. In Figure 18, 0.050 μF would work well.

FIGURE 20 – HIGH PERFORMANCE ELLIPTIC FILTER FOR CVSD OUTPUT

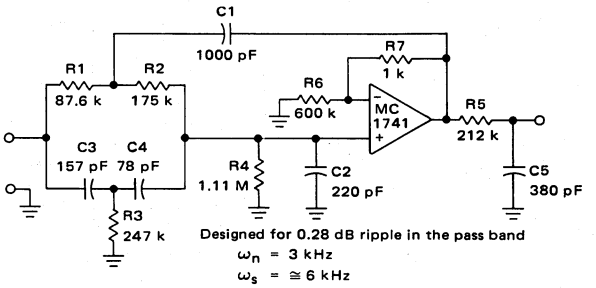
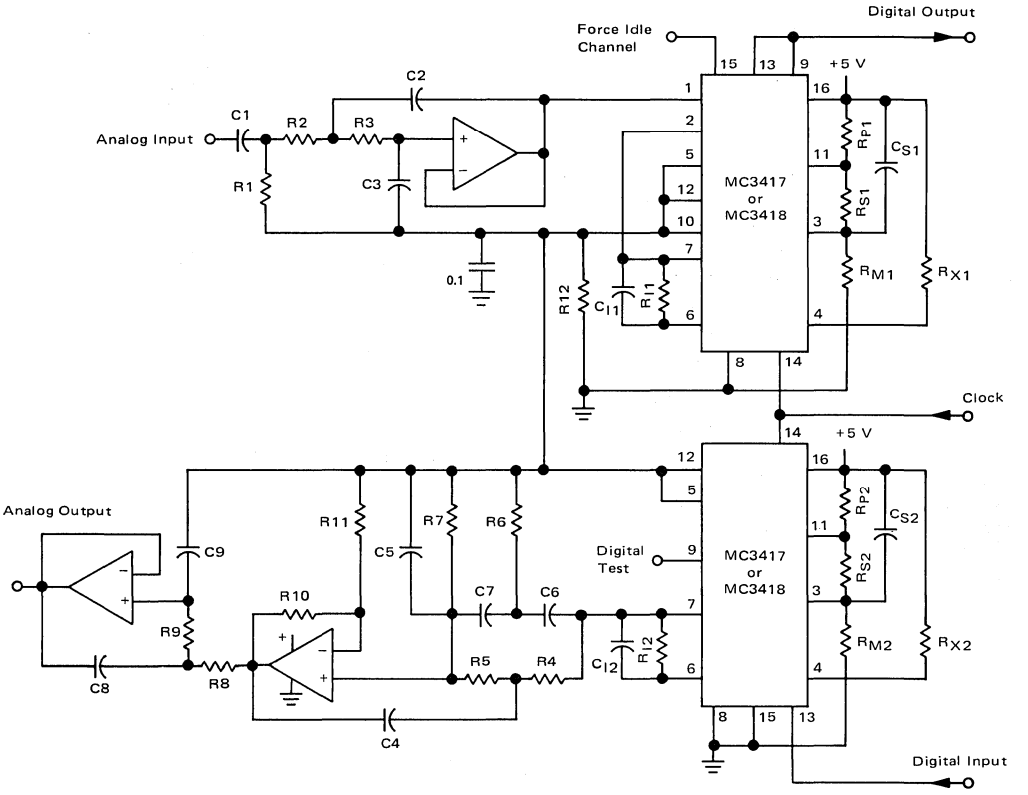


FIGURE 21 – FULL DUPLEX/32K BIT CVSD VOICE CODEC USING MC3517/18 AND MC3503/6 OP AMP



Codec Components

R_{X1}, R_{X2} – 3.3 kΩ
R_{P1}, R_{P2} – 3.3 kΩ
R_{S1}, R_{S2} – 100 kΩ
R_{I1}, R_{I2} – 20 kΩ
R_{12} – 1 kΩ
R_{M1}, R_{M2} –5 MΩ (MC3417)
Minimum step size = 20 mV
R_{M1}, R_{M2} – 15 MΩ (MC3418)
Minimum step size = 6 mV

C_{S1}, C_{S2} – 0.05 μF
C_{I1}, C_{I2} – 0.05 μF

2 MC3417 (or MC3418)
1 MC3403 (or MC3406)

Note: All Res. 5%
All Cap. 5%

Input Filter Specifications

12 dB/Octave Rolloff above 3.3 kHz
6 dB/Octave Rolloff below 50 Hz

Output Filter Specifications

Break Frequency – 3.3 kHz
Stop Band – 9 kHz
Stop Band Atten. – 50 dB
Rolloff – > 40 dB/Octave

Filter Components

R1 – 965 Ω
R2 – 72 kΩ
R3 – 72 kΩ
R4 – 63.46 kΩ
R5 – 127 kΩ
R6 – 365.5 kΩ
R7 – 1.645 MΩ
R8 – 72 kΩ
R9 – 72 kΩ
R10 – 29.5 kΩ
R11 – 72 kΩ

C1 – 3.3 μF
C2 – 837 pF
C3 – 536 pF
C4 – 1000 pF
C5 – 222 pF
C6 – 77 pF
C7 – 38 pF
C8 – 837 pF
C9 – 536 pF

Note: All Res. 0.1% to 1%.
All Cap. 1.0%

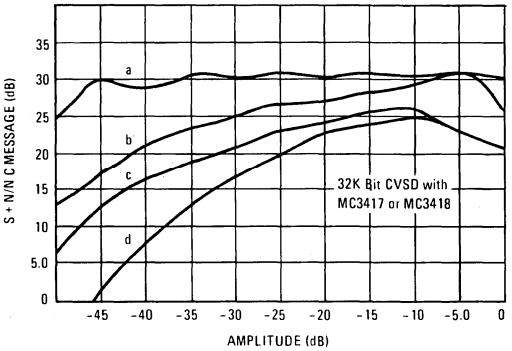
COMPARATIVE CODEC PERFORMANCE

The salient feature of CVSD codecs using the MC3517 and MC3518 family is versatility. The range of codec complexity tradeoffs and bit rate is so wide that one cannot grasp the interdependency of parameters for voice applications in a few pages.

Design of a specific codec must be tailored to the digital channel bandwidth, the analog bandwidth, the quality of signal transmission required and the cost objectives. To illustrate the choices available, the data in Figure 22 compares the signal-to-noise ratios and dynamic range of various codec design options at 32K bits. Generally, the relative merits of each design feature will remain intact in any application. Lowering the bit rate will reduce the dynamic range and noise performance of all techniques. As the bit rate is increased, the overall performance of each technique will improve and the need for more complex designs diminishes.

Non-voice applications of the MC3517 and MC3518 are also possible. In those cases, the signal bandwidth and amplitude characteristics must be defined before the specification of codec parameters can begin. However, in general, the design can proceed along the lines of the voice applications shown here, taking into account the different signal bandwidth requirements.

FIGURE 22 – COMPARATIVE CODEC PERFORMANCE – SIGNAL-TO-NOISE RATIO FOR 1 kHz TEST TONE



These curves demonstrate the improved performance obtained with several codec designs of varying complexity.

Curve a — Complex companding and double integration (Figure 18 — MC3418)
Curve b — Double integration (Figure 14 using Figure 16 — MC3418)
Curve c — Single integration (Figure 14 — MC3418) with 6.0 mV step size
Curve d — Single integration (Figure 14 — MC3417) with 25 mV step size

MC3419-1L

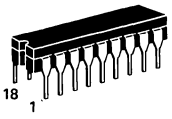
SUBSCRIBER LOOP INTERFACE CIRCUIT

. . . designed as the heart of a circuit to provide BORSHT functions for telephone service in Central Office, PABX, and Subscriber Carrier equipment. This circuit provides dc power for the telephone (Battery), Overvoltage protection, Supervision features such as hook status and dial pulsing, two-wire differential to four-wire single-ended conversions and suppression of longitudinal signals at the two-wire input (Hybrid), and facilitates ringing insertion, Ring trip detection and Testing.

- Totally Upward Compatible with the MC3419
- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of Both Tip and Ring Leads for Auxiliary Functions such as: Ground Key, Ring Trip, Message Waiting Lamp, etc.
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Powerdown Input
- Ground Fault Protection
- Operates from Single −20 V to −56 V Power Source
- Size and Weight Reduction Over Conventional Approaches
- The sale of this product is licensed under Patent No. 4,004,109. All royalties related to this patent are included in the unit price.

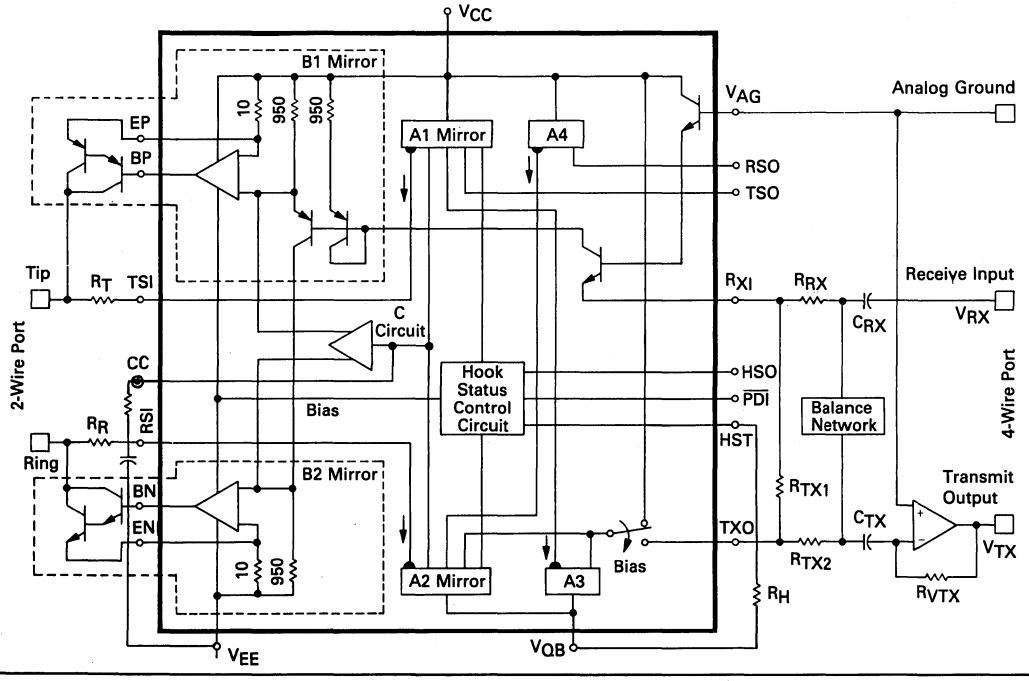
SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

BIPOLAR LASER-TRIMMED INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 726

FUNCTIONAL BLOCK DIAGRAM



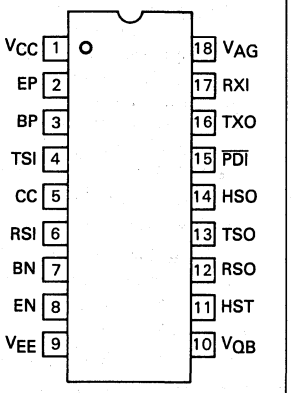
MAXIMUM RATINGS (Voltages Referenced to V_{CC}.)

Rating	Symbol	Value	Unit
Voltage	V_{EE} V_{QB}	−60 V_{EE} −1.0 V	Vdc
Powerdown Input Voltage Range	$V_{\overline{PDI}}$	+15 to −15	Vdc
Sense Current Steady State Pulse — Figure 4	I_{TSI}, I_{RSI}	 100 200	mAdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature (θ_{JA} = 100°C/W Typ)	T_J	150	°C

OPERATING CONDITIONS (Voltages Referenced to V_{CC}.)

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70	°C
Loop Current	I_L	10 to 120	mA
Voltage	V_{EE} V_{QB}	−20 to −56 −20 to V_{EE}	Vdc
Analog Ground (I_L = 0 to 60 mA) (I_L = 0 to 120 mA)	V_{AG}	 0 to −12 −2.5 to −12	Vdc
Supervisory Output Voltage Compliance Range	V_{RSO}, V_{TSO}	−2.0 to −20	Vdc
Hook Status Output	V_{HSO}	+15 to −20	Vdc
Loop Resistance	R_L	0 to 2500	Ω

PIN CONNECTIONS



TRANSMISSION CHARACTERISTICS (R_L = 600 Ω unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Transmit and Receive Gain Variation (Insertion Loss) (1.0 kHz @ 0 dBm Input)	1	V_{TX}/V_L, V_L/V_{RX}	−0.3	0	+0.3	dB
Transhybrid Rejection (Input — 1.0 kHz @ 0 dBm) Fixed (1%) Resistor Balance Network Trimmed Balance Network All Types	1	V_{TX}/V_{RX}	 −23 —	 −35 −55	 — —	dB
Level Linearity (−48 to +3.0 dBm, referenced to 0 dBm @ 1.0 kHz) Transmission Reception	1	 V_{TX}/V_L V_L/V_{RX}	 −0.1 −0.1	 0 0	 +0.1 +0.1	dB
Frequency Response (200–3400 Hz referenced to 1.0 kHz @ 0 dBm) Transmission Reception	1	 V_{TX}/V_L V_L/V_{RX}	 −0.1 −0.1	 0 0	 +0.1 +0.1	dB
Total Distortion @ 1.0 kHz, 0 dBm (C-Message Filtered)	1	V_L/V_{RX} V_{TX}/V_L	— —	−60 −60	— —	dB

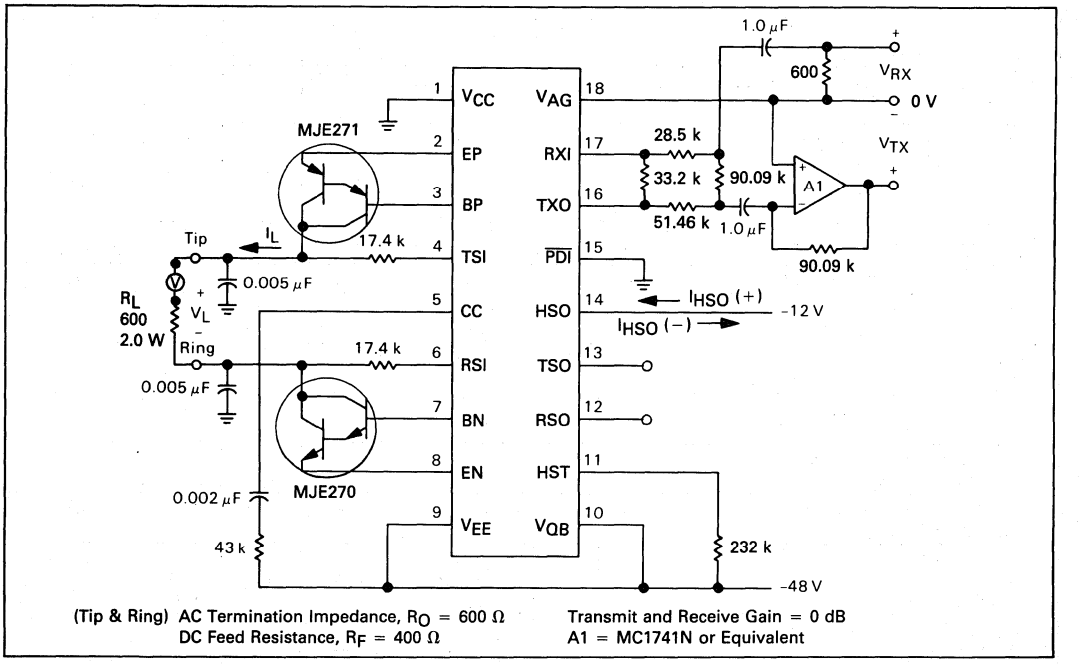
TRANSMISSION CHARACTERISTICS (continued) (R_L = 600 Ω unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Idle Channel Noise (V_{RX} = 0 V)	1	V_{TX}, V_L	—	3.0	10	dBrnC
Return Loss (referenced to 600 ohms) @ 1.0 kHz, 0 dBm	1	$20 \text{ Log } \left\lvert \frac{R_0 - 600}{R_0 + 600} \right\rvert$	30	—	—	dB
Longitudinal Induction (60 Hz) (I_{LON} = 35 mA RMS)	2	V_{TX}	—	5.0	—	dBrnC
Longitudinal Balance (200–3000 Hz)	2	V_{TX}/V_{LON}, V_L/V_{LON}	−45	—	—	dB

ELECTRICAL CHARACTERISTICS (V_{EE} = −48 V, V_{QB} = V_{EE}, V_{AG} = 0 V, R_L = 600 Ω, T_A = 25°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Propagation Delay	1	T_P, V_{RX} to V_L	—	750	—	ns
		V_{RX} to I_{TX}	—	1.2	—	μs
Supply Current — On-Hook (V_{EE} = V_{QB} = 56 V, R_L > 100 MΩ)	3	I_{VCC}	—	40	200	μA
On-Hook Power Dissipation (R_L > 100 MΩ)	3	P_D	—	1.0	—	mW
Power Supply Noise Rejection (1.0 kHz @ 1.0 V_{RMS})	3	V_{TX}/V_{ee}	−40	—	—	dB
Quiet Battery Noise Rejection (1.0 kHz @ 1.0 V_{RMS})	3	V_{TX}/V_{qb}	—	−6.0	—	dB
Sense Current	4					mA/mA
Tip		I_{TSO}/I_{TSI}	0.15	0.17	0.19	
Ring		I_{RSO}/I_{RSI}	0.15	0.17	0.19	
Fault Currents	1					mA
Tip to V_{CC}		I_{Tip}	—	0	—	
Ring to V_{CC}		I_{Ring}	—	2.5	—	
Tip to Ring		I_{Loop}	—	120	—	
Tip and Ring to V_{CC}		I_{Tip} and I_{Ring}	—	2.5	—	
Analog Ground Current	1	I_{VAG}	—	0.1	2.0	μA
Powerdown Logic Levels		$I_{\overline{PDI}}$	—	−1.0	−10	μA
		V_{IH}	−1.2	—	—	Vdc
		V_{IL}	—	—	−4.0	Vdc
Hook Status Output Current	1	I_{HSO}				
(R_L < 2.5 kΩ, V_{HSO} = +0.4 Vdc)			+1.0	+3.0	—	mA
V_{HSO} = −0.4 Vdc)			−0.4	−1.5	—	mA
(R_L > 10 kΩ, V_{HSO} = +12 Vdc)			—	0	+50	μA
V_{HSO} = −12 Vdc)			—	0	−2.0	μA

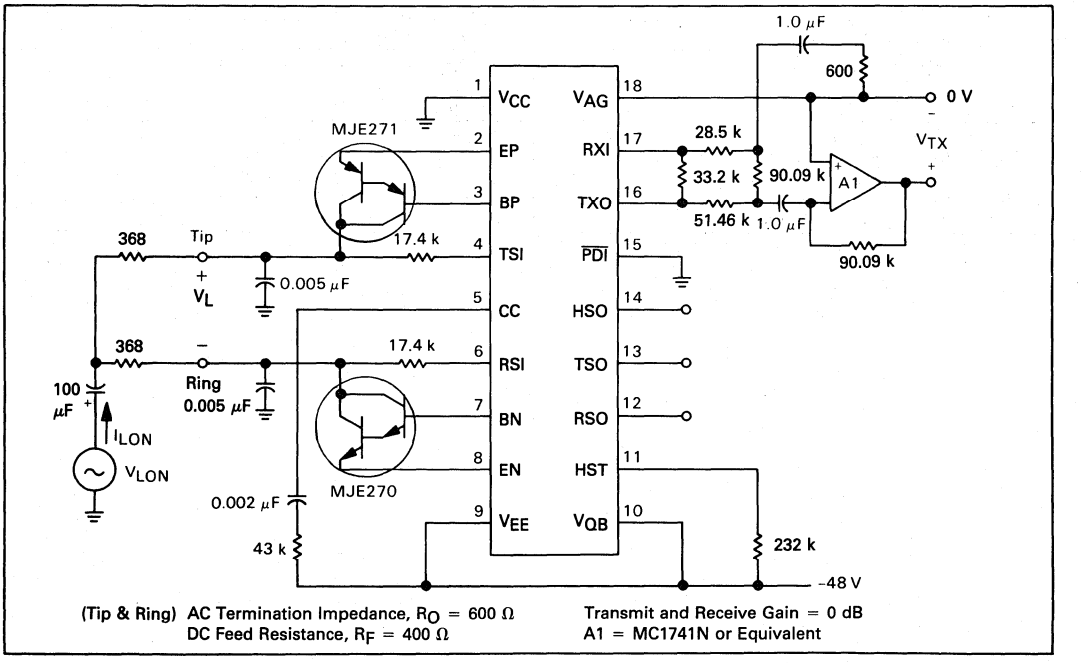
FIGURE 1 — AC TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

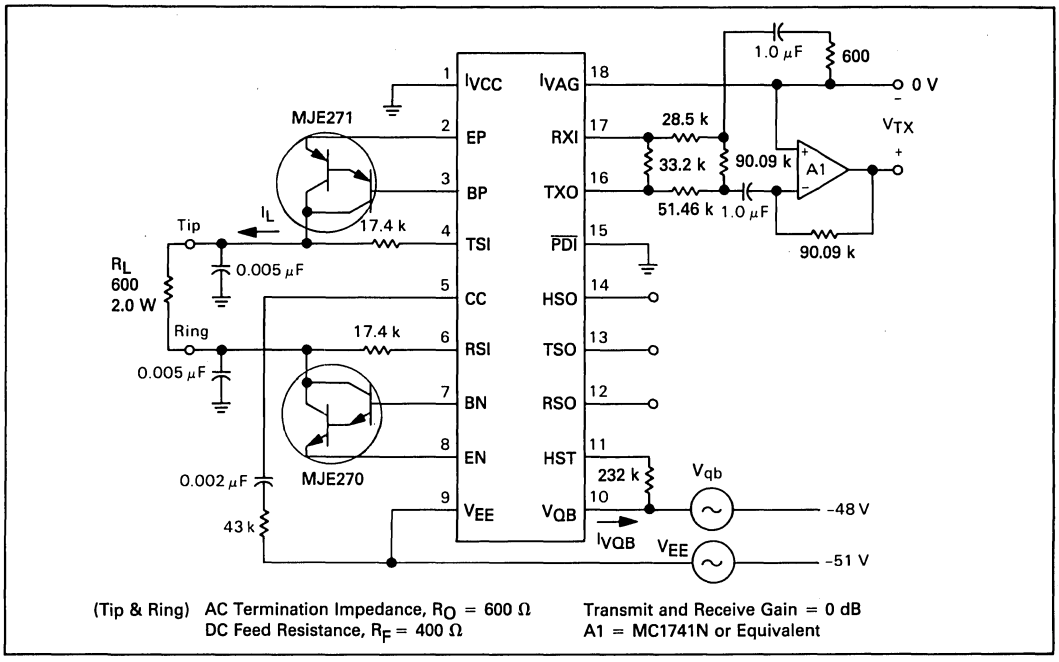
FIGURE 2 — LONGITUDINAL BALANCE TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

FIGURE 3 — SUPPLY NOISE REJECTION TEST CIRCUIT



(Tip & Ring) AC Termination Impedance, R_O = 600 Ω
DC Feed Resistance, R_F = 400 Ω

Transmit and Receive Gain = 0 dB
A1 = MC1741N or Equivalent

FIGURE 4 — TSO AND RSO SUPERVISORY OUTPUT TEST CIRCUIT

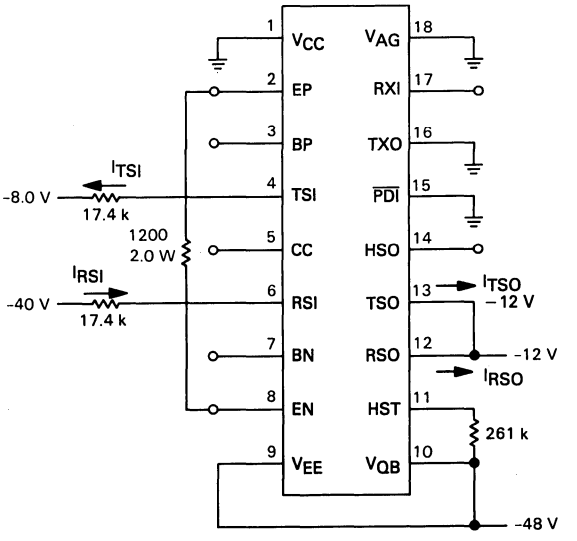


FIGURE 5 — QUIET BATTERY CURRENT I_{VQB} versus LOOP CURRENT I_L

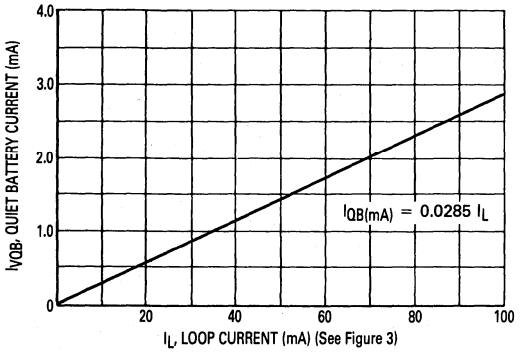
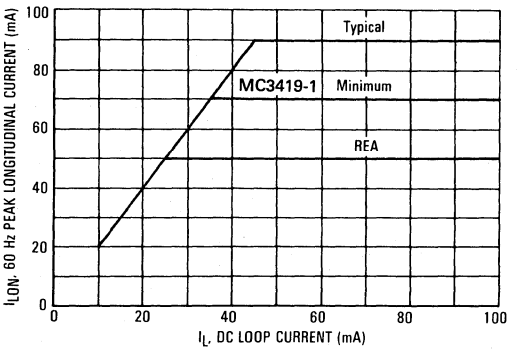


FIGURE 6 — LONGITUDINAL CAPACITY



PIN DESCRIPTIONS

Pin	Name	Function
1	V_{CC}	The positive supply voltage. This point is ground in typical applications.
2, 8	EP & EN	Loop current sensing inputs. These are connected to the emitters of the PNP and NPN Darlington transistors. They are tied through 10 Ω resistors to V_{CC} and V_{EE}, respectively. The maximum continuous current through these inputs is 240 mA.
3, 7	BP & BN	Base drive outputs. These pins drive the bases of the PNP and NPN transistors and are able to sink or source, respectively, up to 5.0 mA.
4, 6	TSI & RSI	Tip and Ring voltage Sensing Inputs. They are low impedance inputs (approximately 600 Ω each i.e., 400 Ω + 3 diodes) that translate the voltages on Tip and Ring to a current through resistors R_T and R_R. TSI is referenced to V_{CC} and RSI is referenced to V_{QB}. These pins have 6.0 V zener diodes (to their respective reference) for protection against overvoltage line surges.
5	CC	Compensation Capacitor pin. This pin is used to stabilize the longitudinal or common mode circuitry.
9	V_{EE}	Negative supply voltage. This pin ties to the chip substrate. Its operating voltage range is −20 V to −56 V. It can withstand −60 V without damage and can sustain a voltage surge to −75 V for less than 4.0 ms without significant degradation of performance. Most of the loop current and bias currents flow through this pin.
10	V_{QB}	Quiet Battery Voltage reference. This is the voltage reference for the RSI pin. Its voltage must not go more negative than V_{EE}. The current through this pin, while powered up, is proportional to the loop current, allowing it to be used for loop current limiting. The voltage on this pin, less 4 volts, is the "effective battery feed voltage for the 2-wire lines even though most of the power comes from the V_{EE} supply.
11	HST	Hook Status Threshold programming resistor input. R_H determines the value of loop resistance at which on-hook and off-hook status is switched.
12	RSO	Ring Sense current Output. This output reflects the voltage status of the Ring terminal for voltages more positive than V_{QB}. The current is sourced from this output, it is one-sixth I_{RSI}, its voltage range is 0 to −20 V and its saturation voltage is approximately −2.0 V.
13	TSO	Tip Sense current Output. This output reflects the voltage status of the Tip terminal for voltages more negative than V_{CC}. The current is sourced from this output, it is one-sixth I_{TSI}, its voltage range is 0 V to −20 V and its saturation voltage is approximately −2.0 V.
14	HSO/$\overline{\text{HSO}}$	Hook Status Output. This is a digital output that reflects the condition of the loop resistance. If loop resistance is less than a predetermined value established by R_H, usually $R_L < 2.5$ kΩ, the HSO pin will be active, i.e., with positive voltage logic (a resistor tied from a +5.0 V or +12 V supply to HSO), this pin will sink current to V_{CC} ($V_{HSO} \cong 0$ V); with negative voltage logic (a resistor tied from a −12 V supply to HSO), this pin will source current from V_{CC} ($V_{HSO} \cong 0$ V). If loop resistance is greater than a predetermined value again established by the same resistor R_H, usually $R_L > 10$ kΩ, the HSO pin is inactive, i.e., V_{HSO} = logic supply voltage.
15	$\overline{\text{PDI}}$	Powerdown Input pin. This pin is used to deny service to the subscriber. A logic level "O" ($V_{IL} <$ −4.0 V) powers down the MC3419-1 except for HSO, TSO and RSO. The voltage range of this high impedance input pin is ±15 V.
16	TXO	Transmit current Output. This output sinks current to V_{QB} and is proportional to $I_{TSI} + I_{RSI}$ by a ratio of K1 where: K1 = 0.51. Its saturation voltage is V_{QB} + 2.5 V typ. (+3.5 V over the temperature range). This pin is only active during the off-hook power-up condition.
17	RXI	Receive Input. This input sums ac currents from TXO and the receive voltage input (V_{RX}) and sources all the dc current to TXO. It has a low input impedance (15 Ω) typically biased 4.5 V below the V_{AG} pin voltage during off-hook power-up conditions. During powerdown conditions, the voltages on RXI and TXO can drift up to V_{AG}.
18	V_{AG}	Analog Ground Voltage reference input. The input impedance of this pin is much greater than 1.0 MΩ. It should be ac coupled to system ground and could be direct coupled if system ground is between 0 V and −12 V. AC coupling requires 300 kΩ to V_{CC} and 0.1 μF to system ground. If V_{CC} and system ground are common, tie V_{AG} directly to V_{CC}. If dc loop currents are allowed to go higher than 60 mA, V_{AG} should be biased from −2.5 V to −12 V to avoid problems at high ambient temperatures.

FUNCTIONAL DESCRIPTION

Referring to the functional block diagram on page 1, line sensing resistors (R_R and R_T) at the TSI and RSI pins convert voltages at the Tip and Ring terminals into currents which are fed into current mirrors* A1 and A2. An output of A1 is mirrored by A3 and summed together with an output of A2 at the TXO terminal. Thus, a differential to single-ended conversion is performed from the ac line signals to the TXO output.

All the dc current at the TXO output is fed back through the RXI terminals to the B1 mirror input. The inputs to B1 and B2 are made equal by mirroring the B1 input current to the B2 input through a unity gain output of the B1 mirror. Both B1 and B2 mirrors have high gain outputs (x95) which drive the subscriber lines with balanced currents that are equal in amplitude and 180° out of phase. The feedback from the TXO output, through the B-Circuit mirrors, to the subscriber line produces a dc feed resistance significantly less, but proportional to the loop sensing resistors.

In most line-interface systems, the ac termination impedance is desired to be greater than the dc feed impedance. A differential ac generator on the subscriber loop would be terminated by the dc feed impedance if the total ac current at the TXO output were returned to the B1 input along with the dc current. Instead, the MC3419-1 system diverts part of the ac current from the B-Circuit mirrors. This decreases the ac feedback current, causing the ac termination impedance at the line interface to be greater than the dc feed impedance.

The ac current that is diverted from the B1 mirror input is coupled to a current-to-voltage converter circuit that has a low input impedance. This circuit consists of an op amp (external to the MC3419-1) and a feedback resistor which produces the transmit output voltage (V_{TX}) at the 4-wire interface. Transmission gain is programmed by the op amp feedback resistor (R_{VTX}).

Reception gain is realized by converting the ac coupled receive input voltage (V_{RX}) to a current through an external resistor (R_{RX}) at the low impedance RXI terminal. This current is summed at RXI with the dc and ac feedback current from the A-Circuit mirrors and drives the B1 mirror input. The B-Circuit mirror outputs drive the 2-wire port with balanced ac current proportional to the receive input voltage. Reception gain is programmed by the R_{RX} resistor.

Since receive input signals are transmitted through the MC3419-1 to the 2-wire port, and the 2-wire port signals are returned to the 4-wire transmit output, a means of cancellation must be provided to maintain 4-wire signal separation (transhybrid rejection). Cancellation is complicated because the gain from the receive port to the transmit port depends on the impedance of the subscriber loop. A passive "balance network" is used to achieve transhybrid rejection by cancelling, at the low impedance input to the transmit op amp, the current reflected by the loop impedance to the 4-wire transmit output. For a resistive loop impedance, a single resistor provides the cancellation. For reactive loops, the balance network should be reactive.

Longitudinal (common-mode) currents that may be present on the subscriber lines are suppressed in the MC3419-1 by two methods. The first is inherent in the mirror configuration. Positive-going longitudinal currents into Tip and Ring create common-mode voltages that cause a decreasing current through the Tip Sensing resistor and an increasing current through the Ring Sensing resistor. When these equal and opposite signal currents are reflected through the A-Circuit mirrors and summed together at TXO, the total current at TXO remains unchanged. Therefore, the ac currents due to the common-mode signal are cancelled before reaching the transmit output.

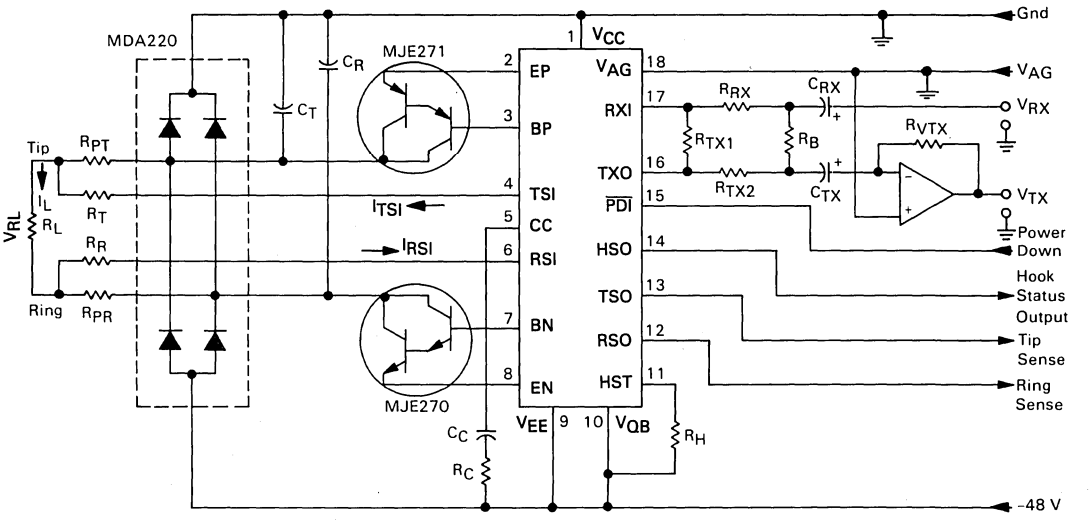
The second longitudinal suppression method is more dominant, since it limits the amplitude of common-mode voltages that appear at the Tip and Ring terminals.

A common-mode suppression circuit detects common-mode inputs and drives the loop with balanced currents to reduce the input amplitude. Subtracting currents from outputs of the A1 and A2 mirrors produces a signal current at the CC terminal in response to the common-mode voltage at Tip and Ring. A transconductance amplifier (C-Circuit) generates a current proportional to the CC terminal voltage which is summed with the current from the RXI terminal at the inputs of current mirrors B1 and B2. The weighting and polarity of the summing networks produce common-mode B1 and B2 mirror output currents at the 2-wire port. The common-mode input impedance is inversely proportional to the gain of the longitudinal suppression circuit. R_C and C_C compensate the common-mode feedback loop. At 60 Hz with typical component values, the 2-wire common-mode impedance is less than 5 Ω.

The longitudinal suppression circuit output currents are generated by modulating dc current fed to the loop by the B1 and B2 current mirrors. This configuration avoids the increased power dissipation attributed to current mode loop drive because dc and longitudinal currents are not cumulatively sourced to the loop. However, driving common-mode currents through the B-circuit current mirrors in this manner limits the longitudinal suppression capability. The suppression circuit is unable to reverse 2-wire current polarities to maintain a low-impedance termination when longitudinal currents exceed the dc loop current. At low dc loop currents, the common-mode signal capability, known as longitudinal capacity, is limited by the loop current (Figure 6). At high-loop currents, longitudinal capacity is limited by the maximum voltage swing of the CC terminal and is therefore independent of dc loop current.

*A current mirror is a circuit which behaves as a current controlled current source. It has a single low-impedance input terminal with respect to a reference point and one or more high impedance outputs.

FIGURE 7 — BASIC SLIC CIRCUIT



The hook status control circuit supplies the bias currents to activate the B-Circuit op amps and other sections of the MC3419-1. To activate the bias currents, the control circuit compares the current through the sense resistors, R_R and R_T, and the load resistance R_L with the current through the hook status threshold programming resistor, R_H, by using outputs from both A1 and A2 mirrors. The A1 mirror output sources current to the R_H resistor. (This reduces all internal currents to near zero during the on-hook state in order to eliminate unnecessary power consumption.) If this current is large enough the voltage on the HST pin will trip an internal comparator, then another circuit compares the current from the A1 output with that of an A2 output. These currents must match within ±15%. If so, HSO will be activated and the bias circuits will turn on provided the voltage on $\overline{PDI}$ is greater than −1.2 V. The HSO pin can have either a pull-up resistor or a pull-down resistor and when activated it will switch to V_{CC} (0 volts).

Once the MC3419-1 is powered up, a circuit with a gain of 20 feeds current to the R_H resistor in order to keep the bias circuitry active. (The sense resistors are paralleled with the Darlington transistors which reduces the sense input currents.) Should the sense input currents drop below one-twentieth of the required power-up current, the bias currents will be removed, forcing a power-down condition.

Current mode analog signal processing is critically dependent on voltage to current conversion at the 2-wire and 4-wire inputs. Precise, low-noise voltage sensing through resistors R_T, R_R and R_{RX} requires quiet, low impedance terminations at terminals TSI, RSI and RXI respectively. For 2-wire signals, terminal V_{QB} isolates the loop-sensing resistors and current mirrors from noise at the high-current V_{EE} terminal. External filtering from V_{CC} to V_{QB} ("quiet battery" terminal) ensures loop voltages are sensed without interference from system supply noise. V_{EE} noise rejection at audio frequencies is typically 60 dB or greater.

Receive input terminal RXI is referenced to the V_{AG} terminal which references the 4-wire input to the "analog ground" of the 4-wire signal source, thus isolating the input from power ground voltage transients. This isolation offers 70 dB of noise rejection at audio frequencies.

SYSTEM EQUATIONS

K1 — The current gain from $I_{TSI} + I_{RSI}$ to TXO only during an off-hook power-up condition. K1 = 0.51 ± 1%.

K2 — The current gain from RXI to the collectors of the off-chip Darlington transistors only during an off-hook power-up condition. K2 = 95 ± 1%.

For simplicity, the following equations do not use K1 or K2. Instead the actual numerical value is used, for instance (1 + [2]K1K2) = 1 + 1.02 x 95 = 97.9 is approximately 98.

R_L — Loop resistance. This is a load resistance from Tip to Ring and can be either ac or dc depending on context.

LOOP CURRENT REGULATIONS

FIGURE 8(a)

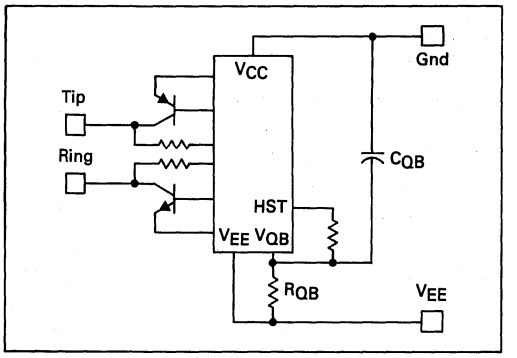


FIGURE 9(a)

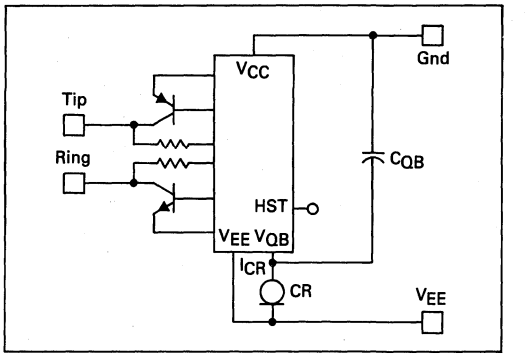


FIGURE 8(b)

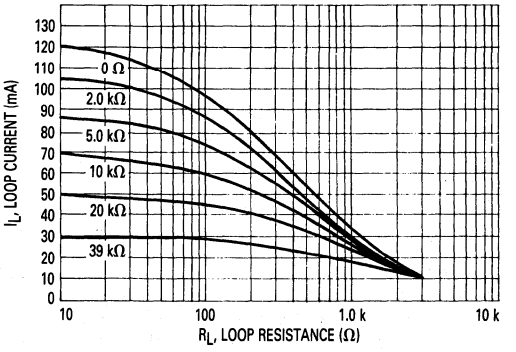
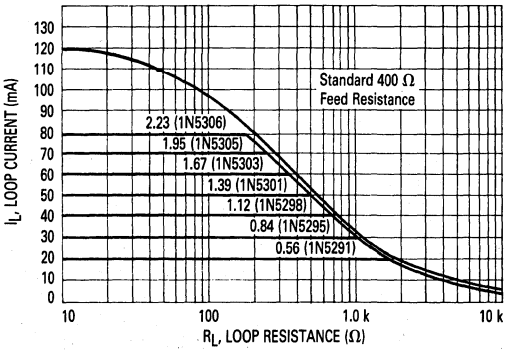


FIGURE 9(b)



SYSTEM EQUATIONS (continued)

Z_L — Loop impedance. This is used only to connote a complex impedance loading on Tip and Ring.

I_L — Loop current. The dc current flow through R_L.

R_F — Dc feed resistance. The synthesized resistance from which battery (V_{CC} and V_{EE}) current is fed to R_L. The battery feed resistance is balanced differential feed. See Figure 7. (This assumes $V_{QB} = V_{EE}$.) The first order equation is:

$$R_F = \frac{R_R + R_T + 1200\ \Omega}{98} \quad (1)$$

Because of the diode voltage drops on TSI and RSI, the actual dc feed resistance is higher. The second order equation is:

$$R_F = \frac{|V_{QB}|(98\ R_L + R_R + R_T + 1200\ \Omega)}{98\ (|V_{QB}| - 4.0\ V)} - R_L \quad (2)$$

ignoring the effects of R_L

$$R_F = \frac{|V_{QB}|(R_R + R_T + 1200\ \Omega)}{98\ (|V_{QB}| - 4.0\ V)} \quad (3)$$

So:

$$R_R = R_T = \frac{49R_F\ (|V_{QB}| - 4.0\ V)}{|V_{QB}|} - 600 \quad (4)$$

The minimum value for R_R and R_T is 5.0 kΩ.

The first order value of R_F can not be greater than the desired value of the termination impedance (usually 600 Ω or 900 Ω). To achieve dc feed resistances that are greater, a resistor can be placed between V_{QB} and V_{EE} along with a filter capacitor C_{QB} which restores the desired termination impedance and filters power supply noise. A diode should also be placed between V_{QB} and V_{EE} to prevent damage in case a catastrophic power supply failure occurs.

I_{VQB} — This is the current that is sourced from the V_{QB} pin and is proportional to the currents into and out of RSI and TSI. When the SLIC is in the off-hook power-up mode, I_{VQB} is also proportional to I_L.

$$I_{VQB} = 2.15\ I_{RSI} + 0.7\ I_{TSI} \quad (5)$$

$$I_{VQB} = 0.029\ I_L \quad (6)$$

R_{FQ} — Dc feed resistance. The synthesized resistance from which battery current is fed to R_L, see Figure 8. (This assumes V_{QB} is tied to V_{EE} through a resistor R_{QB}.) R_{QB} synthesizes additional dc feed resistance to the R_F value previously stated.

When using R_{QB}, the dc feed is effectively balance fed from V_{CC} and V_{QB} instead of V_{EE}. The sense resistors (R_R and R_T) should be selected to make R_F (first order) less than the termination impedance.

$$R_{FQ} = \frac{|V_{EE}|(98R_L + R_R + R_T + 1200 + 2.85R_{QB})}{98(|V_{EE}| - 4.0\ V)} - R_L \quad (7)$$

Ignoring R_L, this simplifies to:

$$R_{FQ} = \frac{|V_{EE}|(R_R + R_T + 1200 + 2.85R_{QB})}{98(|V_{EE}| - 4.0\ V)} \quad (8)$$

Therefore:

$$R_{QB} = \frac{98R_{FQ}(|V_{EE}| - 4.0\ V) - |V_{EE}|(R_R + R_T + 1200\ \Omega)}{2.85|V_{EE}|} \quad (9)$$

C_{QB} — Power supply noise filter capacitor.

$$C_{QB} = \frac{2.85\ R_{QB} + R_R + R_T + 1200\ \Omega}{2\pi f\ R_{QB}\ (R_R + R_T + 1200\ \Omega)} \quad (10)$$

Figure 9B shows R_{QB} replaced with a current regulating device such as Motorola's 1N5283 family.

I_{CRQB} — The current that is sourced to a current regulating device from the V_{QB} pin. When this current reaches the regulated value, the voltage differential between V_{EE} and V_{QB} increases causing the effective battery voltage to decrease which limits I_L to a maximum value as determined below:

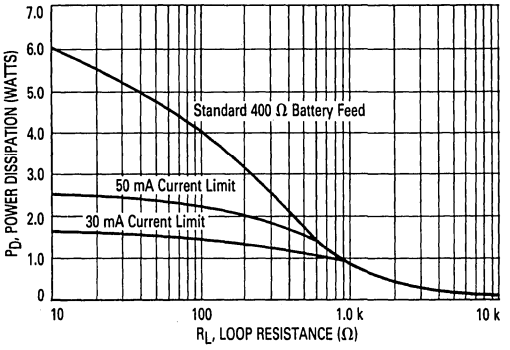
$$I_L = 34.5\ I_{CRQB} \quad (11)$$

The graph, Figure 9B, shows loop current versus loop resistance using several values of I_{CRQB}. The closest current regulating diode part number to that value is also shown. A typical value for C_{QB} in this case is 10 μF, 60 Vdc.

Figure 10 shows how power can be conserved on the shorter loop lengths by utilizing current limiting techniques.

Overvoltage protection on the 2-wire port is achieved with the MDA220 diode bridge and the protection resistors R_{PR} and R_{PT}. Whenever the voltage on the 2-wire port exceeds the power supply rails (V_{CC} and V_{EE}), the MDA220 diodes will forward bias and "clamp" to the rail voltage. The current is limited by the protection resistors. These resistors should be as large in value as possible. However, if they are too large, they will interfere with the performance of the SLIC under worst case conditions.

FIGURE 10 — TOTAL SLIC POWER DISSIPATION versus LOOP RESISTANCE



$$R_{PT} < R_T/196 - 15 \quad (12)$$

Using the voltage of V_{QB} when I_L is at its minimum off-hook value (Typ. 20 mA):

$$R_{PR} < R_R/196 + 25|V_{EE} - V_{QB}| - 15 \quad (13)$$

The tolerance of these resistors is not critical due to placement inside a closed loop. Positive temperature co-efficient resistors (PTC) may be considered here. Consult resistor manufacturers for component selections that will meet the surge current and peak voltage requirements.

Because the MC3419-1 is a broadband device it requires compensation components to keep its circuits stable.

C_R & C_T — Compensates the longitudinal gain of the A and the B circuit mirrors. Their values range from 2000 pF to 5000 pF.

R_C & C_C — Compensates the longitudinal "C" circuitry. Their values can be ratioed according to:

$$R_C \times C_C = R_T \times C_T. \quad (14)$$

Two off-chip power Darlington transistors are used with the MC3419-1. These transistors reduce any temperature gradiant problems with the precision matched devices on-chip and they alleviate thermal stress conditions that could occur for every on-hook and off-hook transition. The power dissipation in these devices is:

$$P_{QT} = I_L{}^2(R_T/98 - R_{PT} - 4) + (2.0\ V)I_L \quad (15)$$

$$P_{QR} = I_L\,[|V_{EE}| - 2 - I_L(R_T/98 + R_L + R_{PR} + 16)] \quad (16)$$

where $I_L = |V_{EE}|/R_{FQ}$ or I_L(max) in current limited designs.

SYSTEM EQUATIONS (continued)

R_H — The resistor that determines the hook status threshold values of R_L. R_H is selected from a graph of the following two equations:

Off-hook threshold

$$R_H = 6(R_L + R_R + R_T) \quad (17)$$

On-hook threshold

$$R_H = 27.25\,[R_L + 0.01(R_R + R_T)] \quad (18)$$

FIGURE 11 — HOOK STATUS DETECTION

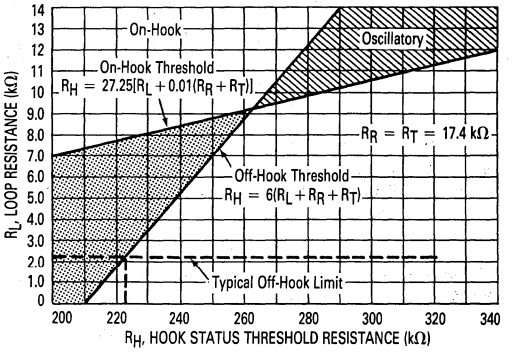


Figure 11 shows such a graph using 17.4 kΩ as the values for R_R and R_T. Note the oscillatory condition to the right of the crossing point. Selection of R_H in this region is usually not a problem since the majority of telephone lines do not fall into this resistance range. R_H always ties to V_{QB} and HST and will give reliable hook status information regardless of power supply voltages and $\overline{PDI}$.

R_O — Termination impedance of the 2-wire port. This impedance is greater than the dc feed resistance R_F because of a current splitting network in the feedback loop, R_{TX1} and R_{TX2}.

K3 — A constant, formed by R_{TX1} and R_{TX2}, between 0 and 1, which determines the ratio of the first order value of R_F to R_O.

$$R_O = \frac{R_R + R_T + 1200\ \Omega}{1 + 97K3} \quad (19)$$

So:

$$K3 = \frac{R_R + R_T + 1200\ \Omega - R_O}{97R_O} \quad (20)$$

and

$$K3 = \frac{R_{TX2} + Z_{in}}{R_{TX1} + R_{TX2} + Z_{in}} \quad (21)$$

Z_{in} — The input impedance of the current to voltage converter op amp. This impedance is usually negligible, it can be used to sway the selection of a 1% component value.

$$Z_{in} = \frac{(R_R + R_T + 1200\ \Omega)\,G_{TX}}{1020\,(1 - K3)} = \frac{R_{VTX}}{1000} \quad (22)$$

R_{TX1} — Feeds most of the TXO dc current to the RXI pin. To keep TXO from saturation the maximum value of R_{TX1} is as follows:

$$R_{TX1} < \frac{(R_R + R_T + 1200\ \Omega)\,(|V_{QB}|min - |V_{AG}|max - 6.5\ V)}{|V_{QB}|min - 5.4\ V} \quad (23)$$

Where:

$$|V_{QB}|min = \frac{(R_R + R_T + 1200\ \Omega)\,(|V_{EE}|min - 4)}{(R_R + R_T + 1200\ \Omega + 2.8\,R_{QB})} \quad (24)$$

or if a current regulator diode is used:

$$R_{TX1} < \frac{0.01\ I_L(max)\,(R_R + R_T + 600\ \Omega) - |V_{AG}|max - 3.9\ V}{0.01\ I_L(max)} \quad (25)$$

It is beneficial to make R_{TX1} as large as possible. Typical values range from 15 k to 24 kΩ.

$$R_{TX2} = \frac{K3\,R_{TX1}}{1 - K3} - Z_{in} \quad (26)$$

$$C_{TX} = \frac{R_R + R_T + 1200\ \Omega}{7R_{TX2}} \quad \text{The result is in } \mu F. \quad (27)$$

G_{TX} — The voltage gain from the 2-wire port to V_{TX} which is adjustable by R_{VTX}.

$$G_{TX} = \frac{1.02\,(1 - K3)\,R_{VTX}}{R_R + R_T + 1200\ \Omega} \quad (28)$$

$$R_{VTX} = \frac{G_{TX}(R_R + R_T + 1200\ \Omega)}{1.02\,(1 - K3)} \quad (29)$$

G_{RX} — The voltage gain from the V_{RX} input to the 2-wire port which is adjustable by R_{RX}.

$$G_{RX} = \frac{-95\,R_L\,(R_R + R_T + 1200\ \Omega)}{R_{RX}\,[(R_R + R_T + 1200\ \Omega) + R_L(1 + 97K3)]} \quad (30)$$

$$G_{RX} = \frac{-95\,R_L\,R_O}{R_{RX}(R_L + R_O)} \quad (31)$$

$$R_{RX} = \frac{95\,R_L\,R_O}{G_{RX}(R_L + R_O)} \quad (32)$$

$$C_{RX} > \frac{R_{RX} + R_B}{2\pi\,f\,R_{RX}R_B} \quad (33)$$

Where f is the minimum passband frequency, usually 200 Hz.

Transhybrid Rejection — The voltage gain from V_{RX} to V_{TX}. It is expressed in dB, the number should be negative and the larger the value the better. Transhybrid rejection is achieved by summing a current from the V_{RX} input (R_B) with the TXO current that flows to the current to voltage converter. R_B balances a resistive load, R_L.

$$R_B = \frac{R_{RX}(1 + 97K3)\,(R_O + R_L)}{97R_L\,(1 - K3)} \quad (34)$$

FIGURE 12 — BALANCE NETWORK FOR CAPACITIVE LINES

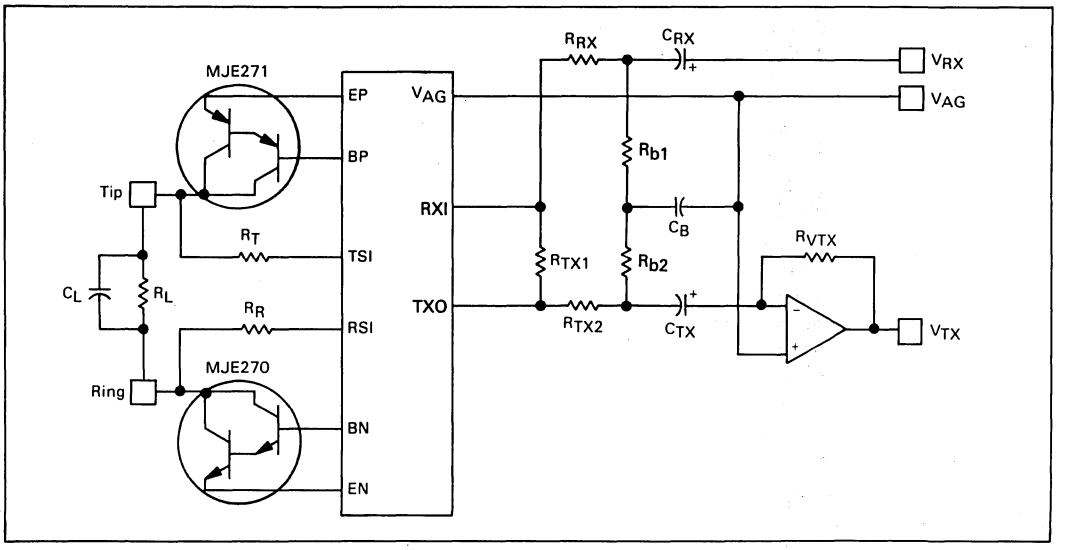
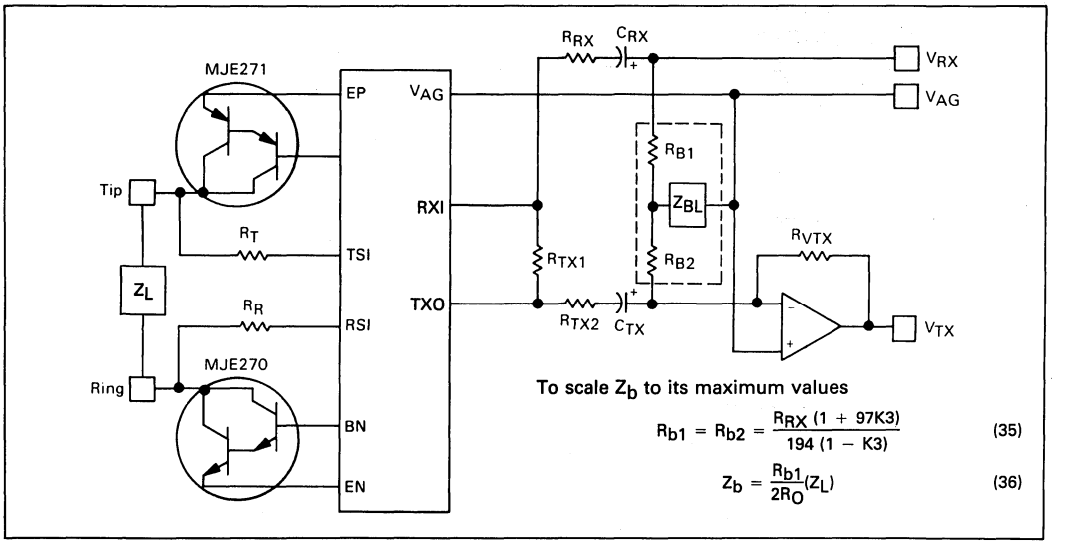


FIGURE 13 — BALANCE NETWORK FOR COMPLEX LOAD IMPEDANCES



To scale Z_b to its maximum values

$$R_{b1} = R_{b2} = \frac{R_{RX}\,(1 + 97K3)}{194\,(1 - K3)} \quad (35)$$

$$Z_b = \frac{R_{b1}}{2R_O}(Z_L) \quad (36)$$

When the 2-wire port has a parallel R and C load, then (see Figure 12):

$$R_{b1} = \frac{R_{RX}(R_R + R_T + 1200\ \Omega)}{97R_L\,(1 - K3)} \quad (37)$$

$$R_{b2} = \frac{R_{RX}(R_R + R_T + 1200\ \Omega)}{97R_O(1 - K3)} \quad (38)$$

$$C_b = \frac{R_L C_L}{R_{b2}} \quad (39)$$

When it is desirable to balance complex load impedances using component values that are equal to the load values (see Figure 13) then:

$$R_{b1} = \frac{R_{RX}(1 + 97K3)}{194(1 - K3)} + \sqrt{\left[\frac{R_{RX}(1 + 97K3)}{194(1 - K3)}\right]^2 - \frac{R_O R_{RX}(1 + 97K3)}{97(1 - K3)}} \quad (40)$$

$$R_{b2} = \frac{R_{RX}(1 + 97K3)}{97(1 - K3)} - R_{b1} \quad (41)$$

$$Z_b = Z_L \quad (42)$$

R_{b1} and R_{b2} values are interchangeable.

SYSTEM EQUATIONS (continued)

The Tip and Ring Sense Output currents are proportional to the currents out of and into TSI and RSI, respectively.

$$I_{TSO} = \frac{I_{TSI}}{6} \quad (43)$$

$$I_{RSO} = \frac{I_{RSI}}{6} \quad (44)$$

$$I_{TSO} = \frac{|V_{Tip} - V_{CC}| - 2.0\ V}{6\ (R_T + 600\ \Omega)} \text{ for } V_{Tip} < V_{CC} \quad (45)$$

$$I_{RSO} = \frac{|V_{Ring} - V_{QB}| - 2.0\ V}{6(R_R + 600\ \Omega)} \text{ for } V_{Ring} > V_{QB} \quad (46)$$

Digital interfacing to the MC3419-1 $\overline{PDI}$ pin and the HSO pin is shown in Figures 14a, 14b and 14c. If the $\overline{PDI}$ pin is not used it should be terminated to V_{CC} and if HSO is not used, it can be left open.

Figure 15 is an application circuit showing solid state ringing insertion using an MOC3030 zero-crossing detector optocoupled triac to replace the conventional electromechanical relay. This device inserts the ringing signal on a zero voltage crossing which eliminates noise in adjacent cable pairs and removes the signal on a zero current crossing which eliminates inductive voltage spikes that commonly destroy relay contacts. The ringing generator provides a continuous 40 V to 120 V RMS signal from 15 to 66 Hz superimposed upon −48 Vdc. Ringing cadencing is inserted with the Ring Enable Input. The 2N6558 and MPSA42 replace the MJE270 for systems that use ringing generator voltages greater than 70 V_{RMS}. The MDA220 diode bridge is replaced with a series 1N4007 on the Tip lead and a shunting 1N4004 to V_{EE} and to allow ringing voltage

FIGURE 14 — INTERFACE-TO-DIGITAL LOGIC

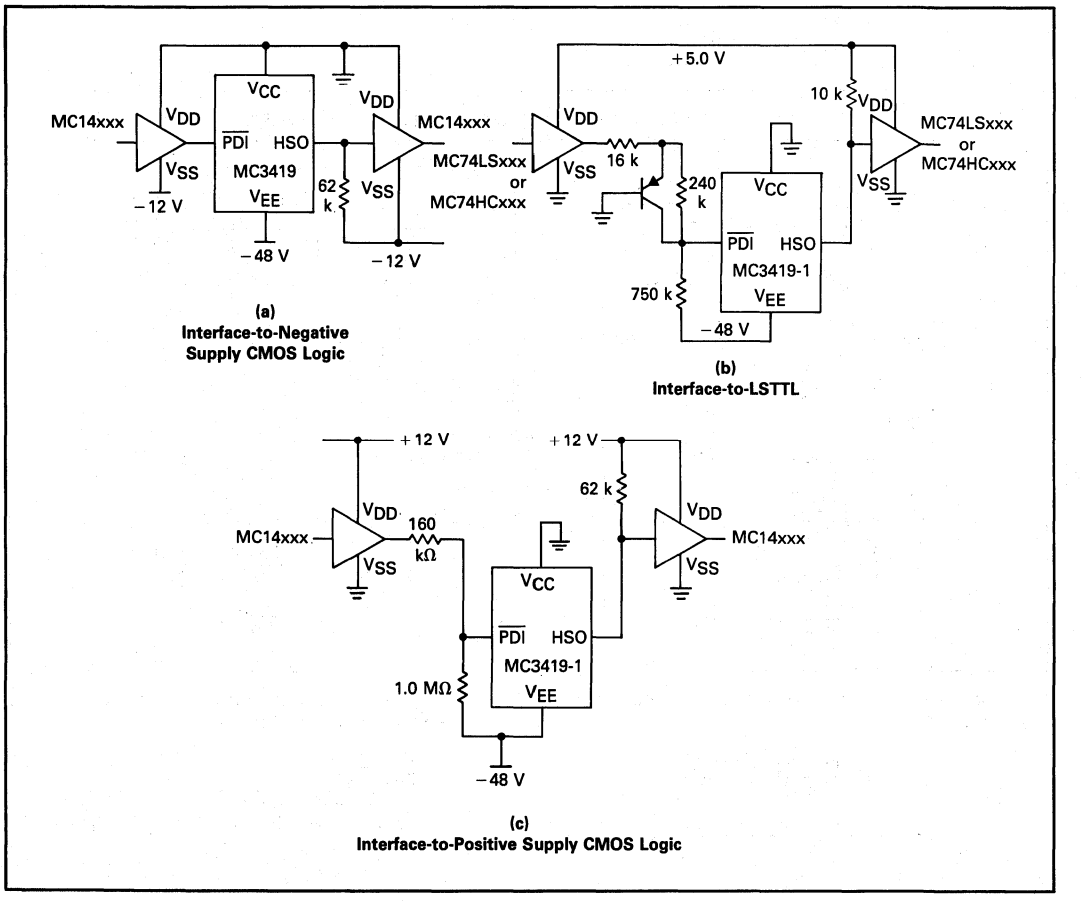
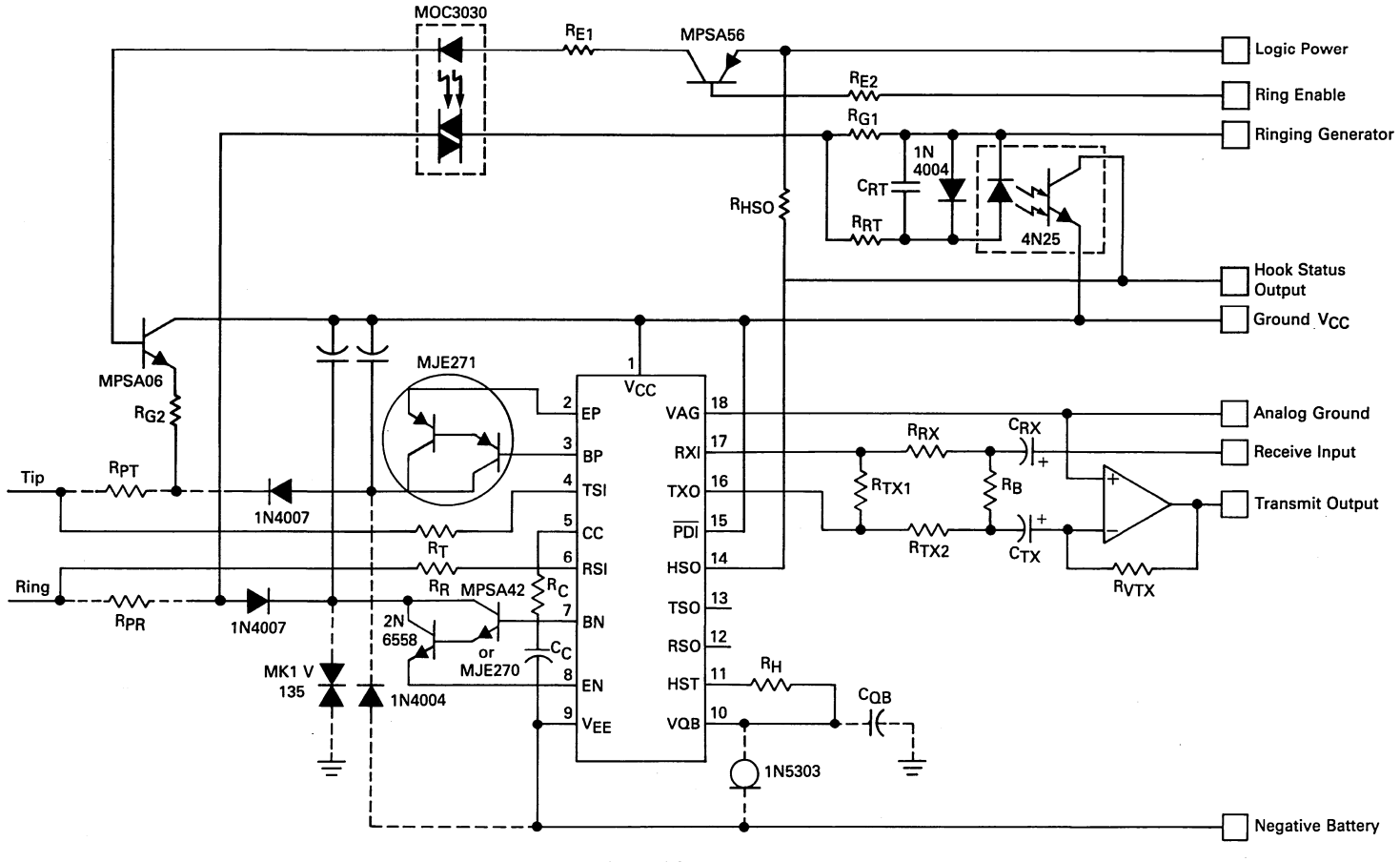


FIGURE 15 — PBX LINE CIRCUIT



SYSTEM EQUATIONS (continued)

on the Ring lead to exceed the power supply voltages, a 1N4007 and an MK1V-135 (Sidac) are used for protection. The forward voltage drop across the 1N4007, during normal operation, will not affect the parametric characteristics of the MC3419-1 since it is "inside" a feedback circuit. If the MJE270 is used, the MK1V-135 should be replaced with a lower voltage Sidac or MOsorb transient suppressor.

An optocoupled transistor circuit is used for ring trip detection on long lines. It samples only the ac and dc ringing signal current and uses a simple one pole filter to eliminate the low level ac signal. Under worst case conditions this circuit will ring trip in 1½ to 4 cycles. In systems serving only short loops (<700 Ω), if R_{G1} and R_{G2} are 620 Ω or greater, the optotransistor circuit is not needed, the Hook Status Output will perform ring trip on a Zero Crossing. The Ring Enable input and the Hook Status Output interface with standard CMOS and TTL logic.

The op amp in this circuit is an integral part of the following codecs, filters or combos:

MC3417/8 — MC145414
MC14404/6/7 — MC14413/4
MC14401/2/3/5

LONG LINES OFF-PREMISE LINES

Specifications

R_F	— 200 Ω	R_O	— 600 Ω
I_L(max)	— 60 mA	R_X Gain	— 0 dB 200–3400 Hz
R_L(max)	— 1900 Ω	T_X Gain	— 0 dB 200–3400 Hz
Off-Hook	— <2500 Ω	V_{Logic}	— +5.0 V
On-Hook	— >10 kΩ	V_{EE}	— −42 to −56 Volts
Protection	— 1000 V	$V_{Ringing}$	— (40 V to 120 V_{RMS}) + V_{EE}
Ringer Equivalent	— 5		

Parts List

MPSA56	R_R	—	9.09 k	1%	Matched
2N3905	R_T	—	9.09 k	1%	if desired
2N6558	R_{PT}	—	47 Ω	5%	
MPSA42	R_{PR}	—	75 Ω	5%	
MJE271	R_{G1}	—	620 Ω	5%	
1N4007	R_{G2}	—	100 Ω	5%	
MK1V135	R_{E1}	—	91 Ω	5%	
1N4007	R_{E2}	—	3.0 k	5%	
1N4007	R_{RT}	—	20 k	5%	
1N5303	R_C	—	24 k	5%	
1N4004	R_H	—	127 k	1–3%	
MC3419-1	R_{HSO}	—	10 k	5%	

MOC3030	R_{TX1}	—	12.1 k	1%	
4N25	R_{TS2}	—	5.76 k	1%	
	R_{RX}	—	28.7 k	1%	
	R_B	—	28.0 k	1%	
	R_{VTX}	—	28.6 k	1%	
	C_T		0.004 μF		
	C_R	—	0.004 μF		
	C_C	—	0.001 μF		
	C_{RX}	—	1.0 μF/20 V		
	C_{TX}	—	2.0 μF/40 V		
	C_{RT}	—	20 μF/5.0 V		
	C_{QB}	—	10 μF/60 V		

SHORT LINES ON-PREMISE LINES

Specifications

R_F	—	500 Ω
R_L(max)	—	700 Ω
Ring Trip	—	<50 ms
Ringer Equivalent	—	2.5
R_O	—	600 Ω
R_X Gain	—	−5.0 dB
T_X Gain	—	0 dB
V_{Logic}	—	+5.0 Volts
V_{EE}	—	−20 to −56 Volts
$V_{Ringing}$	—	(40 V to 70 V_{RMS}) + V_{EE}

Parts List

MJE271	R_R	—	19.6 k	1%	
MJE270	R_T	—	19.6 k	1%	
MPSA56	R_{G1}	—	620 Ω	5%	
2N3905	R_{G2}	—	620 Ω	5%	
1N4007	R_{E1}	—	91 Ω	5%	
1N4007	R_{E2}	—	3.0 k	5%	

MOC3030				R_{HSO}	— 10 k 5%
				R_{TX1}	— 19.6 k 1%
C_T	—	0.004 μF		R_{TX2}	— 42.2 k 1%
C_R	—	0.004 μF		R_{RX}	— 69.8 k 1%
C_C	—	0.004 μF		R_B	— 301 k 1%
C_{RX}	—	0.1 μF		R_{VTX}	— 127 k 1%
C_{TX}	—	0.5 μF		R_C	— 56 k 5%

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13055

Advance Information

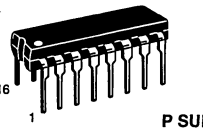
Wideband FSK Receiver

WIDEBAND FSK RECEIVER

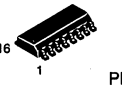
MONOLITHIC SILICON INTEGRATED CIRCUIT

The MC13055 is intended fo RF data link systems using carrier frequencies up to 40 MHz and FSK (frequency shift keying) data rates up to 2.0 M Baud (1.0 MHz). This design is similar to the MC3356, except that it does not include the oscillator/mixer. The IF bandwidth has been increased and the detector output has been revised to a balanced configuration. The received signal strength metering circuit has been retained, as has the versatile data slicer/comparator.

- Input Sensitivity 20 μV @ 40 MHz
- Signal Strength Indicator Linear Over 3 Decades
- Available in Surface Mount Package
- Easy Application, Few Peripheral Components

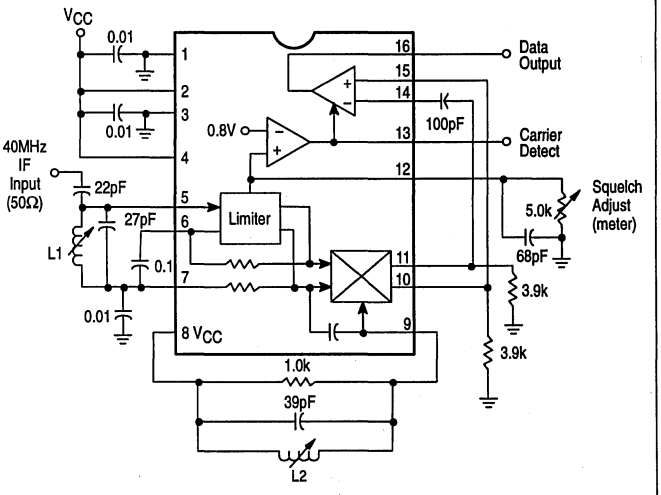


P SUFFIX
PLASTIC PACKAGE
CASE 648

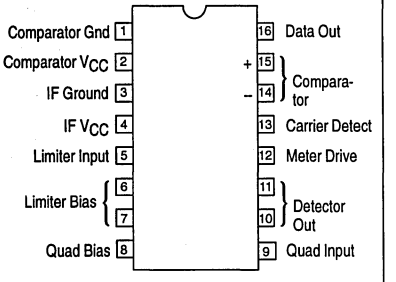


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

Figure 1. Block Diagram and Application Circuit



PIN CONNECTIONS



This document contains information on a new product. Specifications and information herein are subject to change without notice.

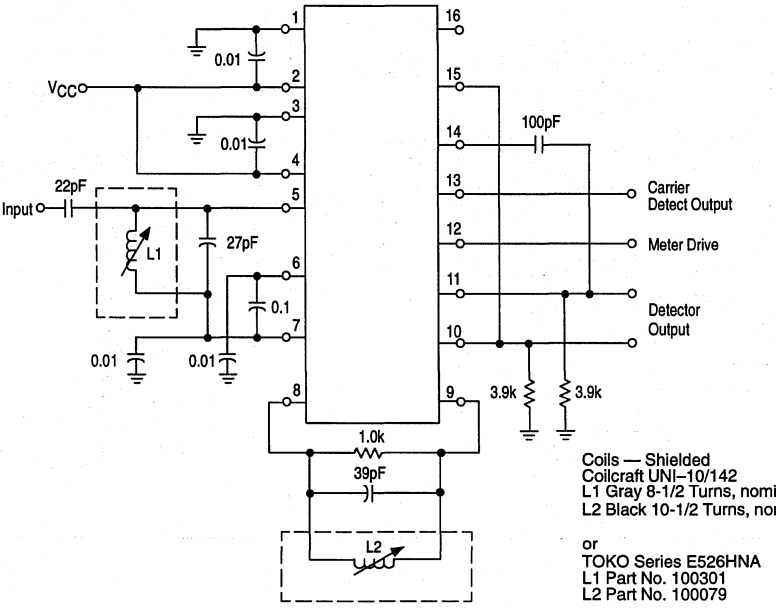
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Supply Voltage Range	V2, V4	3.0 to 12	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 40 MHz, f_{mod} = 1.0 MHz, Δf = ±1.0 MHz, T_A = 25°C, test circuit of Figure 2.)

Characteristics		Measure	Min	Typ	Max	Unit
Total Drain Current		12 + 14	—	20	25	mA
Data Comparator Pull-Down Current		I16	—	10	—	mA
Meter Drive Slope versus Input		I12	4.5	7.0	9.0	µA/dB
Carrier Detect Pull-Down Current		I13	—	1.3	—	mA
Carrier Detect Pull-Up Current		I13	—	500	—	µA
Carrier Detect Threshold Voltage		V12	700	800	900	mV
DC Output Current		I10, I11	—	430	—	µA
Recovered Signal		V10 – V11	—	350	—	mVrms
Sensitivity for 20 dB S + N/N, BW = 5.0 MHz		VIN	—	20	—	µVrms
S + N/N at V_{in} = 50 µV		V10 – V11	—	30	—	dB
Input Impedance @ 40 MHz	R_{in}	Pin 5, Ground	—	4.2	—	kΩ
	C_{in}		—	4.5	—	pF
Quadrature Coil Loading	R_{in}	Pin 9 to 8	—	7.6	—	kΩ
	C_{in}		—	5.2	—	pF

Figure 2. Test Circuit



Coils — Shielded
Coilcraft UNI–10/142
L1 Gray 8-1/2 Turns, nominal 300 nH
L2 Black 10-1/2 Turns, nominal 380 nH

or
TOKO Series E526HNA
L1 Part No. 100301
L2 Part No. 100079

Figure 3. Overall Gain, Noise, AM Rejection

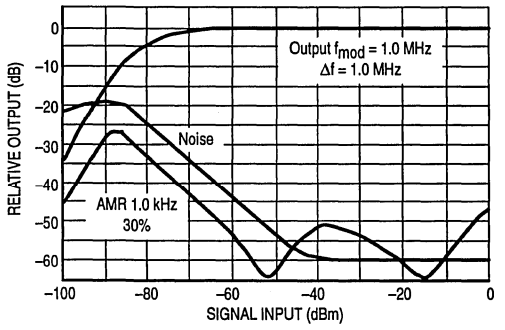


Figure 4. Meter Current versus Signal

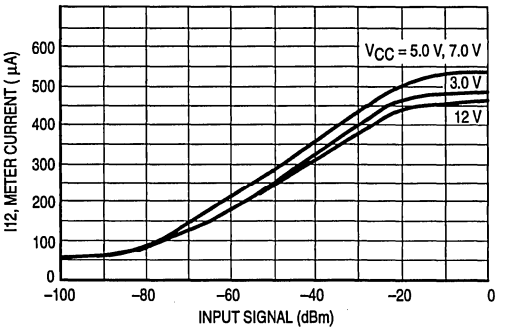


Figure 5. Untuned Input: Limiting Sensitivity versus Frequency

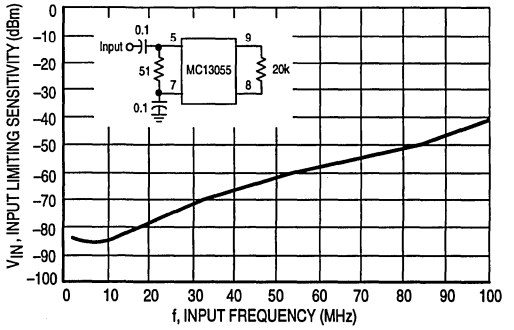


Figure 6. Untuned Input: Meter Current versus Frequency

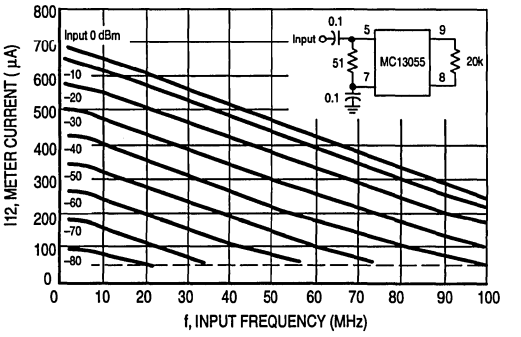


Figure 7. Limiting Sensitivity and Detuning versus Supply Voltage

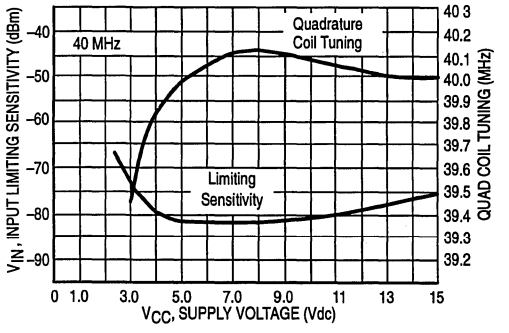


Figure 8. Detector Current and Power Supply Current versus Supply Voltage

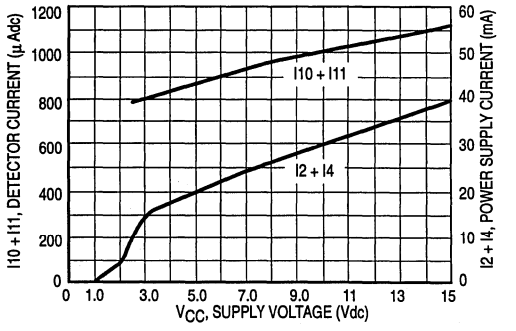


Figure 9. Recovered Audio versus Temperature

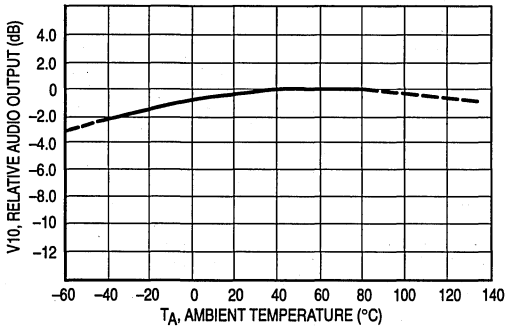


Figure 10. Carrier Detect Threshold versus Temperature

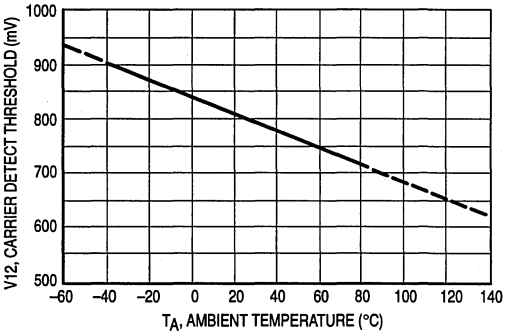


Figure 11. Meter Current versus Temperature

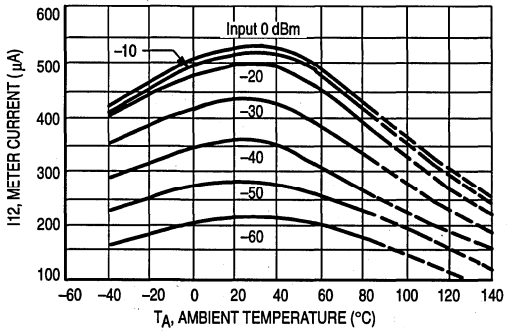


Figure 12. Input Limiting versus Temperature

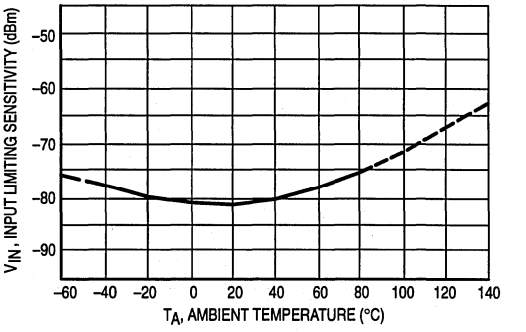


Figure 13. Input Impedance, Pin 5

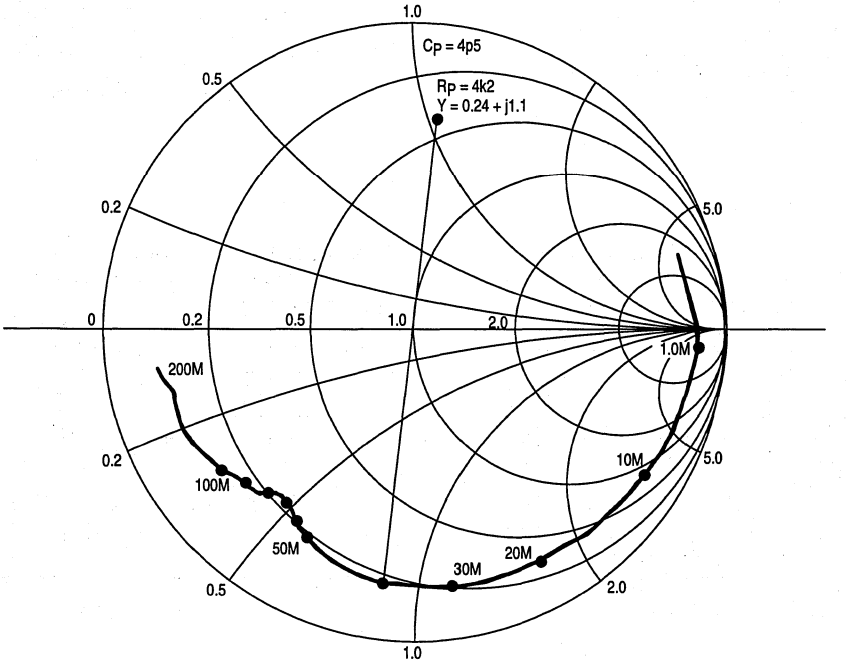
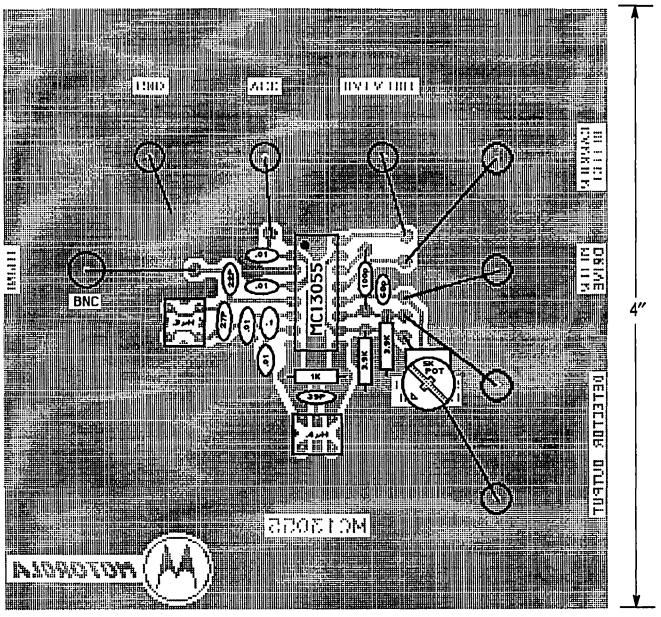


Figure 14. Test Fixture (Component Layout)



(Circuit Side View)

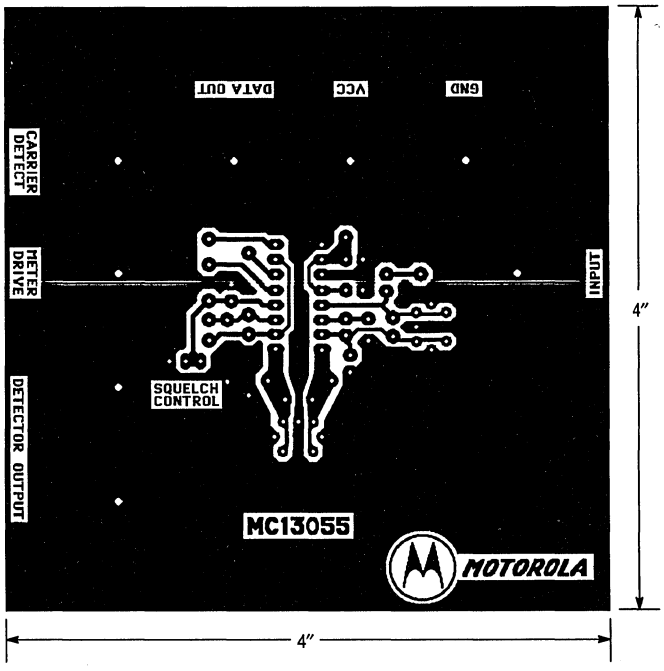
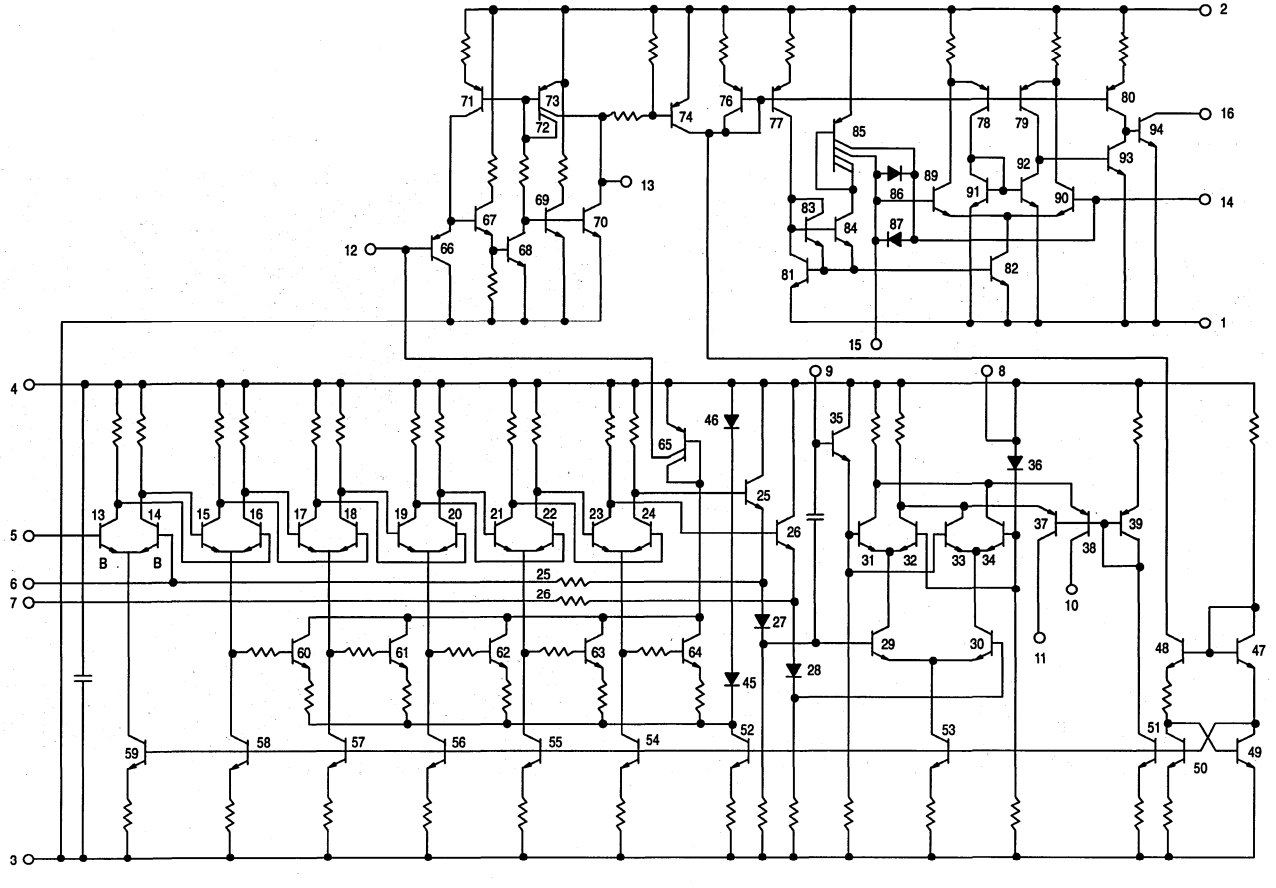


Figure 15. Internal Schematic



GENERAL DESCRIPTION

The MC13055 is an extended frequency range FM IF, quadrature detector, signal strength detector and data shaper. It is intended primarily for FSK data systems. The design is very similar to MC3356 except that the oscillator/mixer has been removed, and the frequency capability of the IF has been raised about 2:1. The detector output configuration has been changed to a balanced, open-collector type to permit symmetrical drive of the data shaper (comparator). Meter drive and squelch features have been retained.

The limiting IF is a high frequency type, capable of being operated up to 100 MHz. It is expected to be used at 40 MHz in most cases. The quadrature detector is internally coupled to the IF, and a 2.0 pF quadrature capacitor is internally provided. The 20 dB quieting sensitivity is approximately 20 μV, tuned input, and the IF can accept signals up to 220 mVrms without distortion or change of detector quiescent DC level.

The IF is unusual in that each of the last 5 stages of the 6 stage limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 20 μV to 20 mVrms. (See Figure 4.)

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator (+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 20 μVrms. A resistor (R) from Pin 13 to Pin 12 will provide V_{CC}/R of feedback current. This current can be correlated to an amount of signal strength hysteresis by using Figure 4.

The squelch is internally connected to the data shaper. Squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete "floating" comparator, with diodes across its inputs. The outputs of the quadrature detector can be fed directly to either or preferably both inputs of the comparator to produce a squared output swinging from V_{CC} to ground in inverted or noninverted form.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13135
MC13136

DUAL CONVERSION NARROWBAND FM RECEIVERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

Advance Information

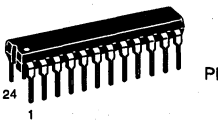
FM Communications Receivers

The MC13135/MC13136 are the second generation of single chip, dual conversion FM communications receivers developed by Motorola. Major improvements in signal handling, RSSI and first oscillator operation have been made. In addition, recovered audio distortion and audio drive have improved. Using Motorola's MOSAIC™ 1.5 process, these receivers offer low noise, high gain and stability over a wide operating voltage range.

Both the MC13135 and MC13136 include a Colpitts oscillator, VCO tuning diode, low noise first and second mixer and LO, high gain limiting IF, and RSSI. The MC13135 is designed for use with an LC quadrature detector and has an uncommitted op amp that can be used either for an RSSI buffer or as a data comparator. The MC13136 can be used with either a ceramic discriminator or an LC quad coil and the op amp is internally connected for a voltage buffered RSSI output.

These devices can be used as stand-alone VHF receivers or as the lower IF of a triple conversion system. Applications include cordless telephones, short range data links, walkie-talkies, low cost land mobile, amateur radio receivers, baby monitors and scanners.

- Complete Dual Conversion FM Receiver – Antenna Input to Audio Output
- Voltage Buffered RSSI with 70 dB of Usable Range
- Low Voltage Operation – 2.0 to 6.0 Vdc (2 Cell NiCad Supply)
- Low Current Drain – 3.5 mA Typ
- Low Impedance Audio Output < 25 Ω
- VHF Colpitts First LO for Crystal or VCO Operation
- Isolated Tuning Diode
- Buffered First LO Output to Drive CMOS PLL Synthesizer



P SUFFIX
PLASTIC PACKAGE
CASE 724

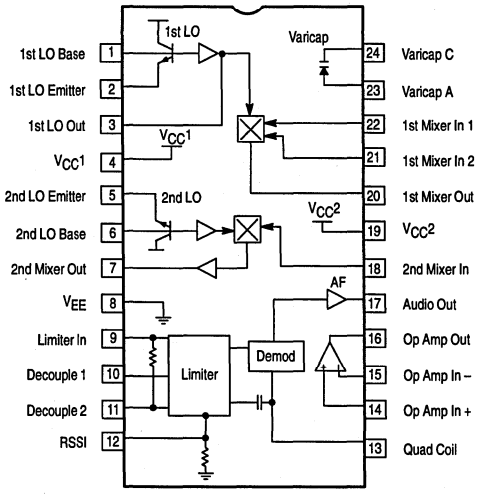
DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO-24L)

ORDERING INFORMATION

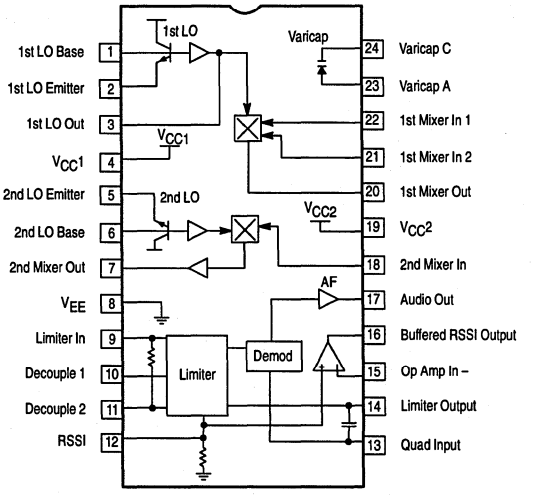
Device	Temperature Range	Package
MC13135P	– 40° to +85°C	Plastic DIP
MC13135DW		SO-24L
MC13136P		Plastic DIP
MC13136DW		SO-24L

PIN CONNECTIONS

MC13135



MC13136



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 19	V_{CC} (max)	6.5	Vdc
RF Input Voltage	22	RF_{in}	1.0	Vrms
Junction Temperature	—	T_J	+150	°C
Storage Temperature Range	—	T_{stg}	– 65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 19	V_{CC}	2.0 to 6.0	Vdc
Maximum 1st IF	—	f_{IF1}	21	MHz
Maximum 2nd IF	—	f_{IF2}	3.0	MHz
Ambient Temperature Range	—	T_A	– 40 to + 85	°C

ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{CC}=4.0 Vdc, f_o=49.7 MHz, f_{MOD}=1.0 kHz, Deviation=±3.0 kHz, f_{1stLO}=39 MHz, $f_{2nd\ LO}$=10.245 MHz, IF1=10.7 MHz, IF2=455 kHz, unless otherwise noted. All measurements performed in the test circuit of Figure 1.)

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Total Drain Current	No Input Signal	I_{CC}	—	4.0	6.0	mAdc
Sensitivity (Input for 12 dB SINAD)	Matched Input	V_{SIN}	—	1.0	—	µVrms
Recovered Audio MC13135 MC13136	V_{RF} = 1.0 mV	AF_O	 170 215	 220 265	 270 315	mVrms
Limiter Output Level (Pin 14, MC13136)		V_{LIM}	—	130	—	mVrms
1st Mixer Conversion Gain	V_{RF} = – 40 dBm	MX_{gain1}	—	12	—	dB
2nd Mixer Conversion Gain	V_{RF} = – 40 dBm	MX_{gain2}	—	13	—	dB
First LO Buffered Output	—	V_{LO}	—	100	—	mVrms
Total Harmonic Distortion	V_{RF} = – 30 dBm	THD	—	1.2	3.0	%
Demodulator Bandwidth	—	BW	—	50	—	kHz
RSSI Dynamic Range	—	RSSI	—	70	—	dB
First Mixer 3rd Order Intercept (Input)	 Matched Unmatched	TOI_{Mix1}	 — —	 –17 –11	 — —	dBm
Second Mixer 3rd Order Intercept (RF Input)	Matched Input	TOI_{Mix2}	—	– 27	—	dBm
First LO Buffer Output Resistance	—	R_{LO}	—	—	—	Ω
First Mixer Parallel Input Resistance	—	R	—	722	—	Ω
First Mixer Parallel Input Capacitance	—	C	—	3.3	—	pF
First Mixer Output Impedance	—	ZO	—	330	—	Ω
Second Mixer Input Impedance	—	Z_I	—	40	—	kΩ
Second Mixer Output Impedance	—	ZO	—	1.8	—	kΩ
Detector Output Impedance	—	ZO	—	25	—	Ω

TEST CIRCUIT INFORMATION

Although the MC13136 can be operated with a ceramic discriminator, the recovered audio measurements for both the MC13135 and MC13136 are made with an LC quadrature detector. The typical recovered audio will depend on the external circuit; either the Q of the quad coil, or the RC matching network for the ceramic discriminator. On the MC13136, an external capacitor between Pins 13 and 14 can be used with a quad coil for slightly higher recovered audio. See Figures 10 through 13 for additional information.

Since adding a matching circuit to the RF input increases the signal level to the mixer, the third order intercept (TOI) point is better with an unmatched input (50 Ω from Pin 21 to Pin 22). Typical values for both have been included in the Electrical Characterization Table. TOI measurements were taken at the pins with a high impedance probe/spectrum analyzer system. The first mixer input impedance was measured at the pin with a network analyzer.

Figure 1a. MC13135 Test Circuit

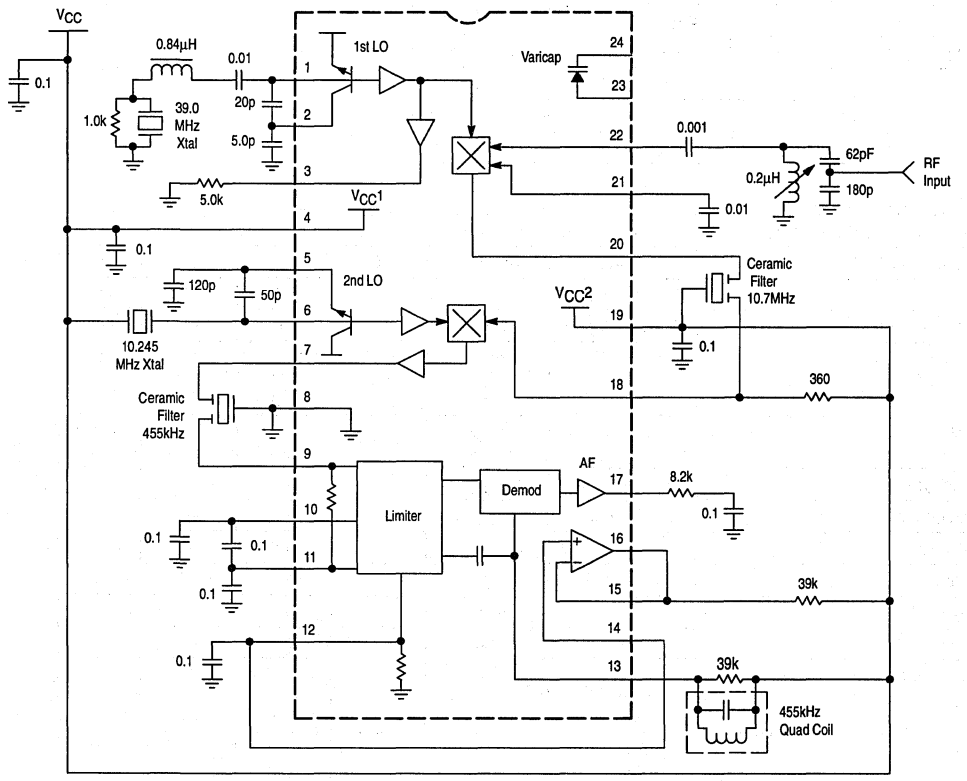


Figure 1b. MC13136 Quad Detector Test Circuit

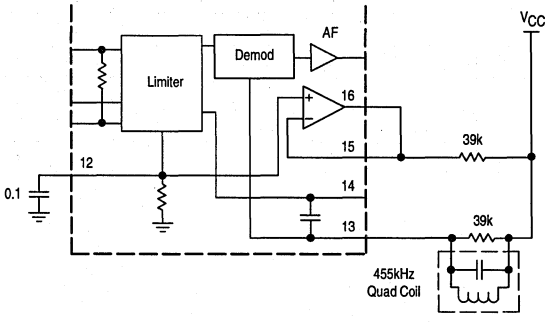


Figure 2. Supply Current versus Supply Voltage

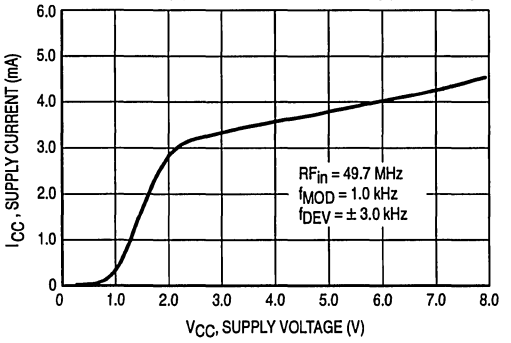


Figure 3. RSSI Output versus RF Input

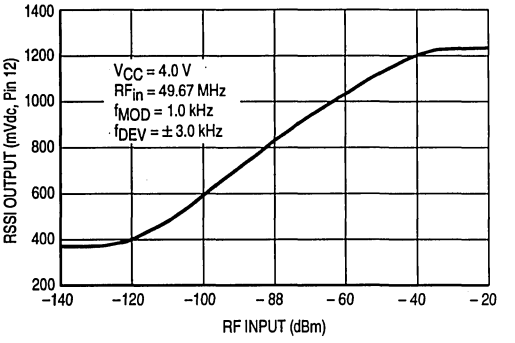


Figure 4. Varactor Capacitance, Resistance versus Bias Voltage

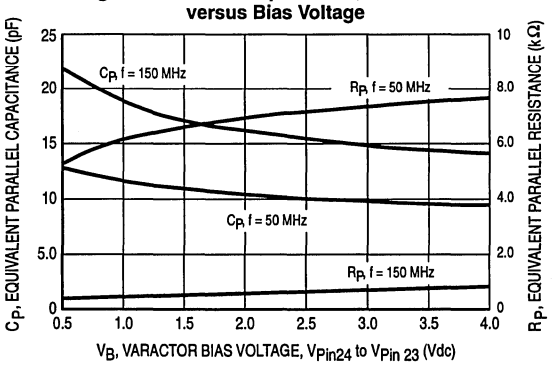


Figure 5. Oscillator Frequency versus Varactor Bias

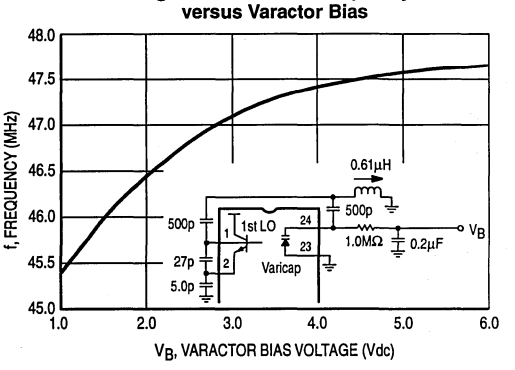


Figure 6. Signal Levels versus RF Input

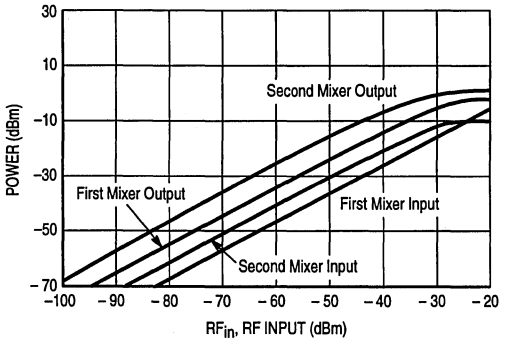


Figure 7. Signal + Noise, Noise, and AM Rejection versus Input Power

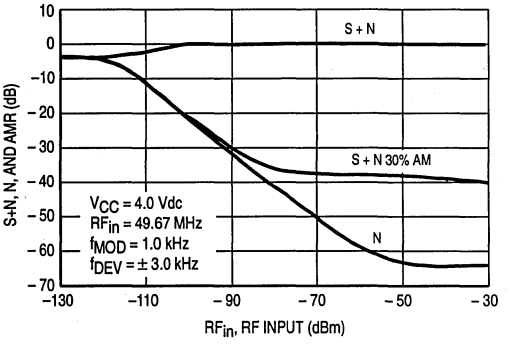


Figure 8. Op Amp Gain and Phase versus Frequency

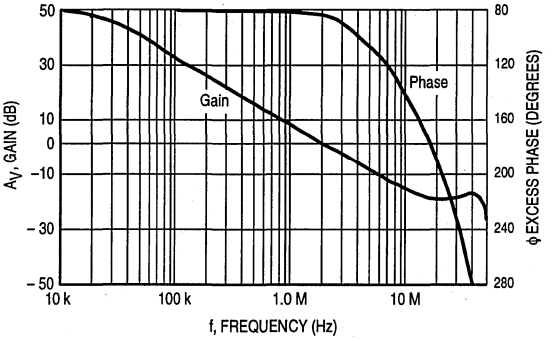


Figure 9. First Mixer Third Order Intermodulation (Unmatched Input)

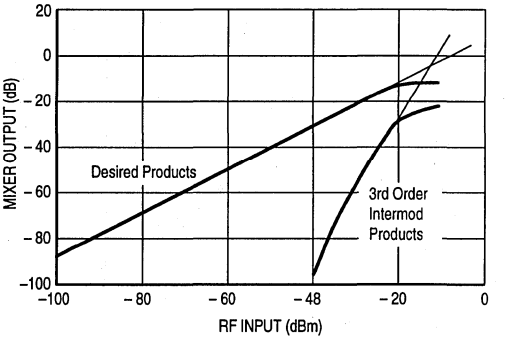


Figure 10. Recovered Audio versus Deviation for MC13135

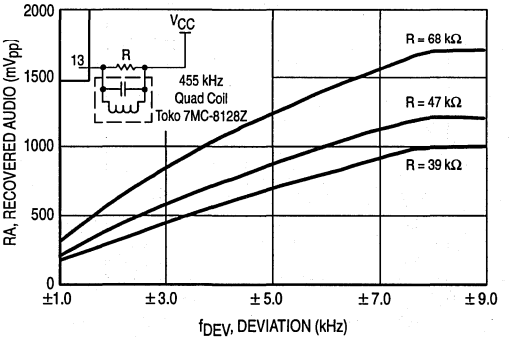


Figure 11. Distortion versus Deviation for MC13135

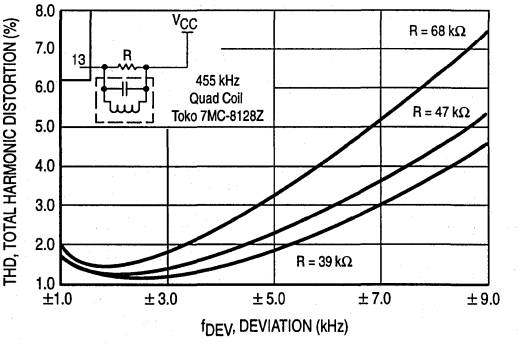


Figure 12. Recovered Audio versus Deviation for MC13136

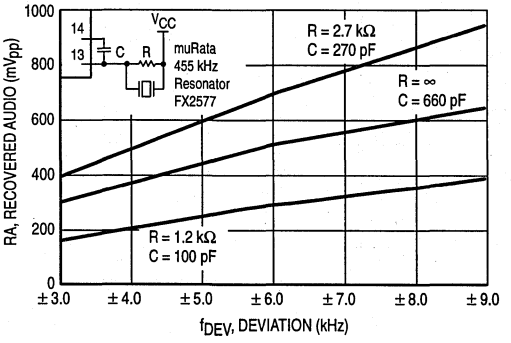
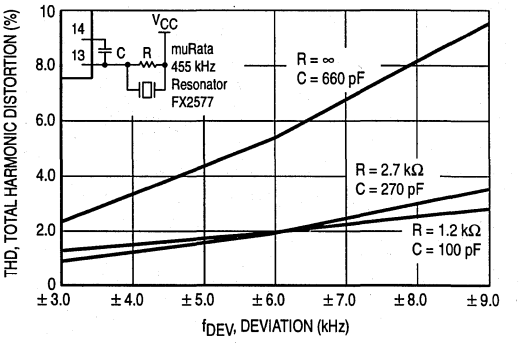


Figure 13. Distortion versus Deviation for MC13136



CIRCUIT DESCRIPTION

The MC13135/13136 are complete dual conversion receivers. They include two local oscillators, two mixers, a limiting IF amplifier and detector, and an op amp. Both provide a voltage buffered RSSI with 70 dB of usable range, isolated tuning diode and buffered LO output for PLL operation, and a separate V_{CC} pin for the first mixer and LO. Improvements have been made in the temperature performance of both the recovered audio and the RSSI.

V_{CC}

Two separate V_{CC} lines enable the first LO and mixer to continue running while the rest of the circuit is powered down. They also isolate the RF from the rest of the internal circuit.

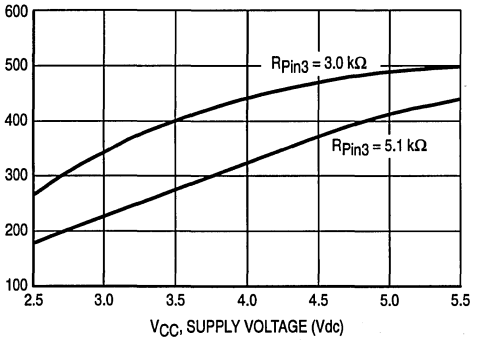
Local Oscillators

The local oscillators are grounded collector Colpitts, which can be easily crystal-controlled or VCO controlled with the on-board varactor and external PLL. The first LO transistor is internally biased, but the emitter is pinned-out and I_Q can be increased for high frequency or VCO operation. The collector is not pinned out, so for crystal operation, the LO is generally limited to 3rd overtone crystal frequencies; typically around 60 MHz. For higher frequency operation, the LO can be provided externally as shown in Figure 16.

Buffer

The buffer on the 1st LO output converts the single-ended LO output to a differential signal to drive the mixer. Capacitive coupling between the LO and buffer minimizes the effects of the change in oscillator current on the mixer. The buffered LO output is pinned-out for use with a PLL, with a typical output voltage of 320 mVp-p at V_{CC} = 4.0 V and with a 5.1 k resistor from Pin 3 to ground. As seen in Figure 14, the buffered LO output varies with the supply voltage and a smaller external resistor may be needed for low voltage operation. The LO buffer operates up to 60 MHz, typically.

Figure 14. Buffered LO Output Voltage versus Supply Voltage



Mixers

The first and second mixer are of similar design. Both are double balanced to suppress the LO and input frequencies to give only the sum and difference frequencies out. This configuration typically provides 40 to 60 dB of LO suppression. New design techniques provide improved mixer linearity and third order intercept without increased noise. The gain on the output of the 1st mixer starts to roll off at about 20 MHz, so this receiver could be used with a 21 MHz first IF. It is designed for use with a ceramic filter, with an output impedance of 330 Ω. A series resistor can be used to raise the impedance for use with a crystal filter, which typically has an input impedance of 4.0 kΩ. The second mixer input impedance is approximately 4.0 kΩ; it requires an external 360 Ω parallel resistor for use with a standard ceramic filter.

Limiting IF Amplifier and Detector

The limiter has approximately 110 dB of gain, which starts rolling off at 2.0 MHz. Although not designed for wideband operation, the bandwidth of the audio frequency amplifier has been widened to 50 kHz, which gives less phase shift and enables the receiver to run at higher data rates. However, care should be taken not to exceed the bandwidth allowed by local regulations.

The MC13135 is designed for use with an LC quadrature detector, and does not have sufficient drive to be used with a ceramic discriminator. The MC13136 was designed to use a ceramic discriminator, but can also be run with an LC quad coil, as mentioned in the Test Circuit Information section. The data shown in Figures 12 and 13 was taken using a muRata FX2577 ceramic discriminator which has been specially matched to the MC13136. Both the choice of discriminators and the external matching circuit will affect the distortion and recovered audio.

RSSI/Op Amp

The Received Signal Strength Indicator (RSSI) on the MC13135/13136 has about 70 dB of range. The resistor needed to translate the RSSI current to a voltage output has been included on the internal circuit, which gives it a tighter tolerance. A temperature compensated reference current also improves the RSSI accuracy over temperature. On the MC13136, the op amp on board is connected to the output to provide a voltage buffered RSSI. On the MC13135, the op amp is not connected internally and can be used for the RSSI or as a data slicer (see Figures 17c and 20b).

Figure 15. PLL Controlled Narrowband FM Receiver at 46/49 MHz

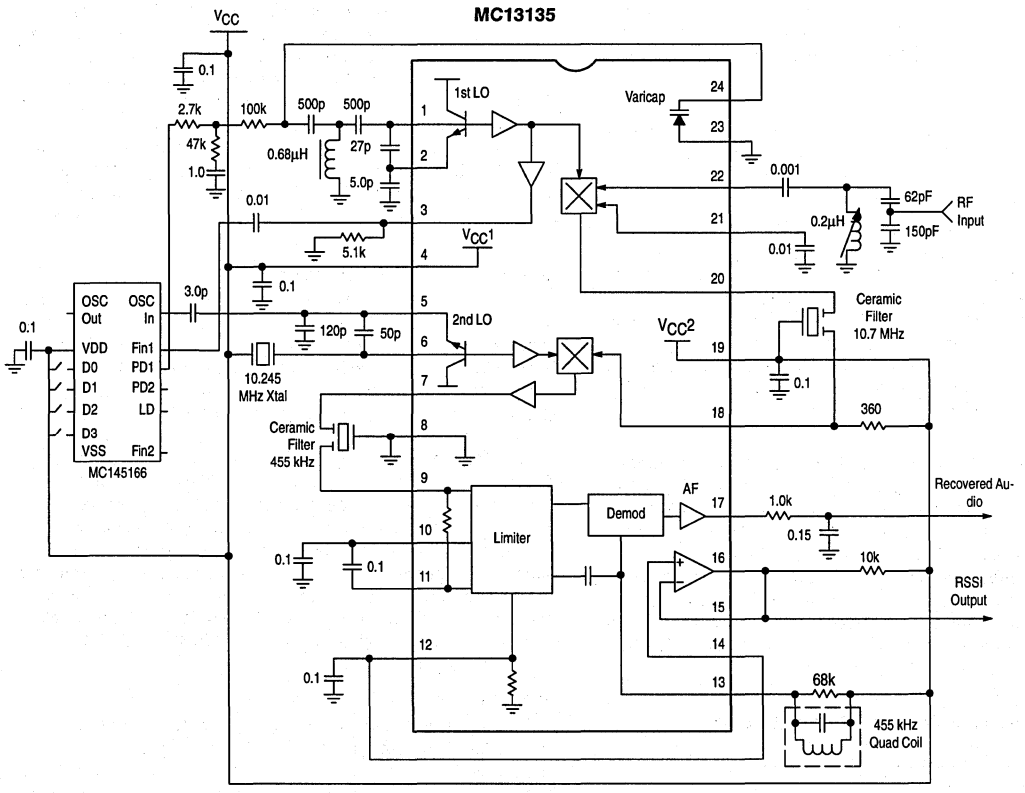
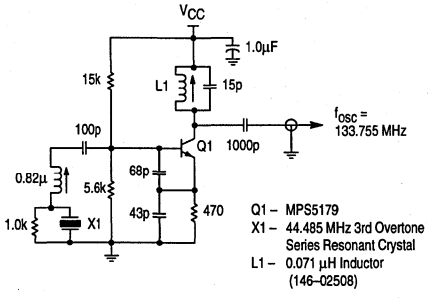


Figure 16. 144 MHz Single Channel Application Circuit

1st LO External Oscillator Circuit



Preamp for MC13135 at 144.455 MHz

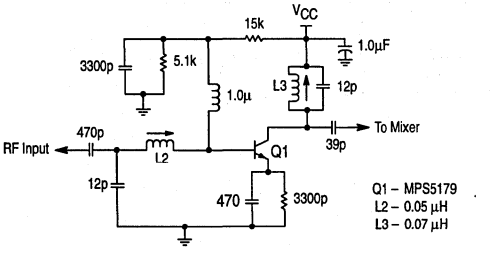


Figure 17a. Single Channel Narrowband FM Receiver at 49.7 MHz

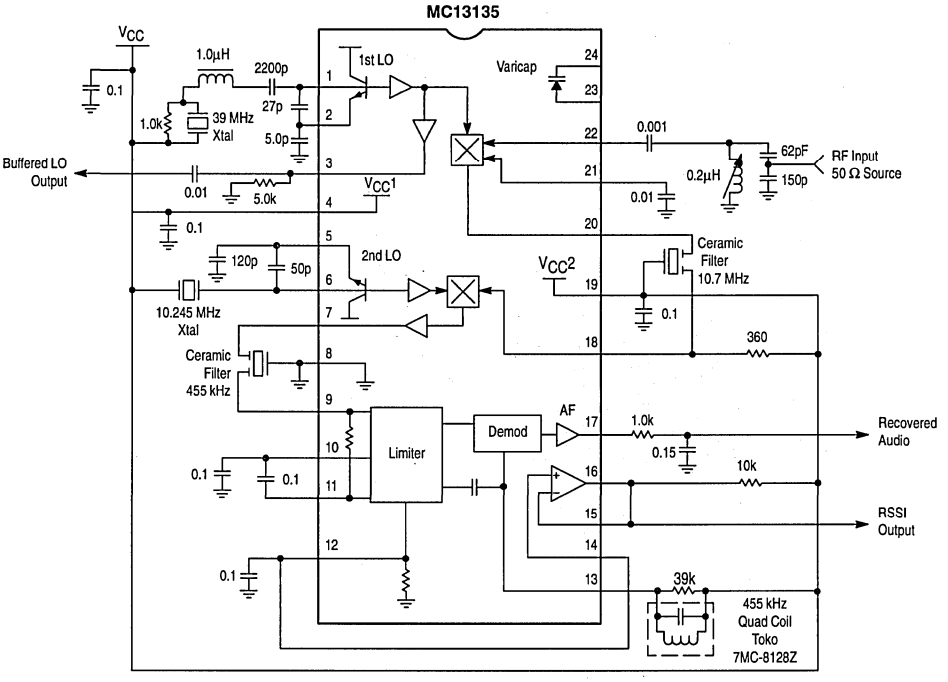
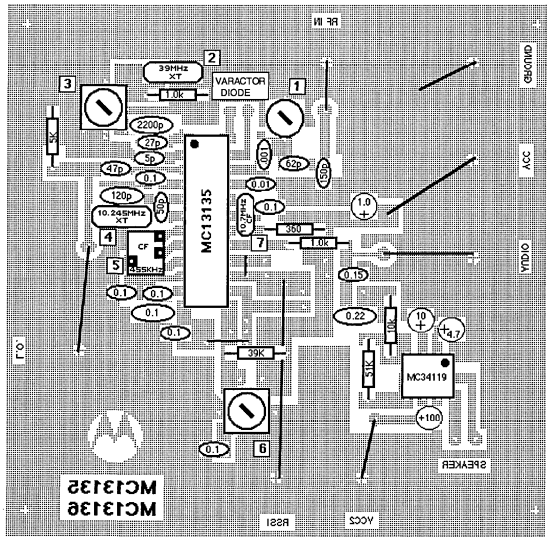


Figure 17b. PC Board Component View



NOTES:
1. 0.2 µH tunable (unshielded) inductor
2. 39 MHz Series mode resonant 3rd Overtone Crystal
3. 1.5 µH tunable (shielded) inductor
4. 10.245 MHz Fundamental mode crystal, 32 pF load
5. 455 kHz ceramic filter, muRata CFU 455B or equivalent
6. Quadrature coil, Toko 7MC-8128Z (7mm) or Toko RMC-2A6597HM (10mm)
7. 10.7 MHz ceramic filter, muRata SFE10.7MJ-A or equivalent

Figure 17c. Optional Data Slicer Circuit
(Using Internal Op Amp)

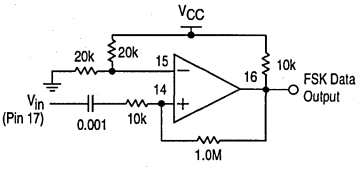
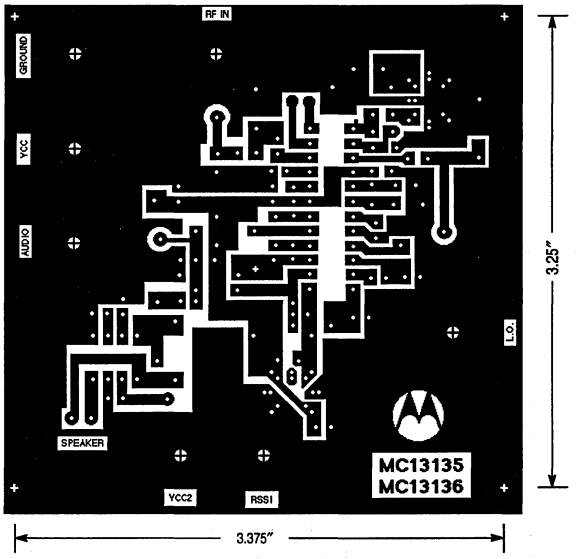
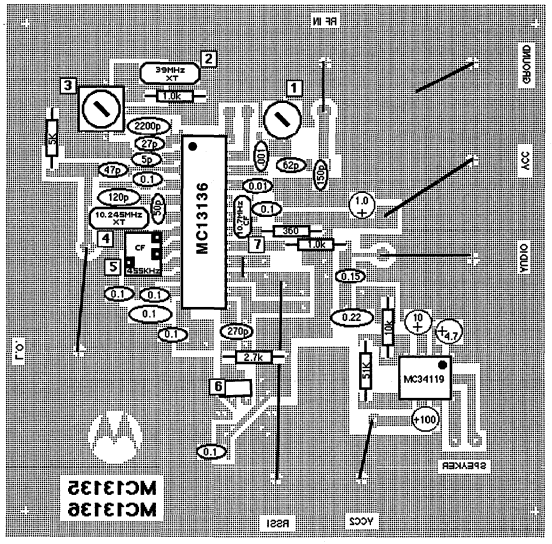


Figure 18. PC Board Solder Side View



(Circuit Side View)

Figure 19. PC Board Component View



NOTES:
1. 0.2 µH tunable (unshielded) inductor
2. 39 MHz Series mode resonant 3rd Overtone Crystal
3. 1.5 µH tunable (shielded) inductor
4. 10.245 MHz Fundamental mode crystal, 32 pF load
5. 455 kHz ceramic filter, muRata CFU 455B or equivalent
6. Ceramic discriminator, muRata FX2577 or equivalent
7. 10.7 MHz ceramic filter, muRata SFE10.7MJ-A or equivalent

Figure 20a. Single Channel Narrowband FM Receiver at 49.7 MHz

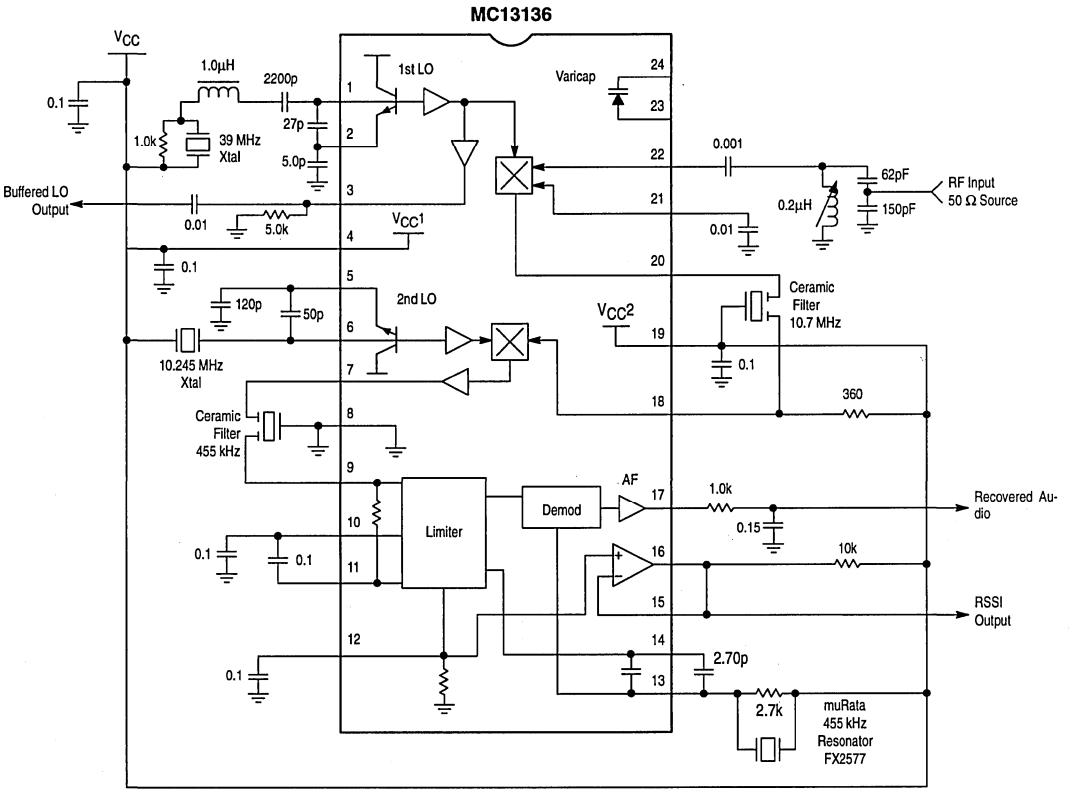


Figure 20b. Optional Audio Amplifier Circuit

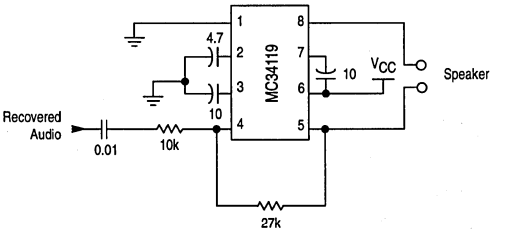


Figure 21. MC13135 Internal Schematic

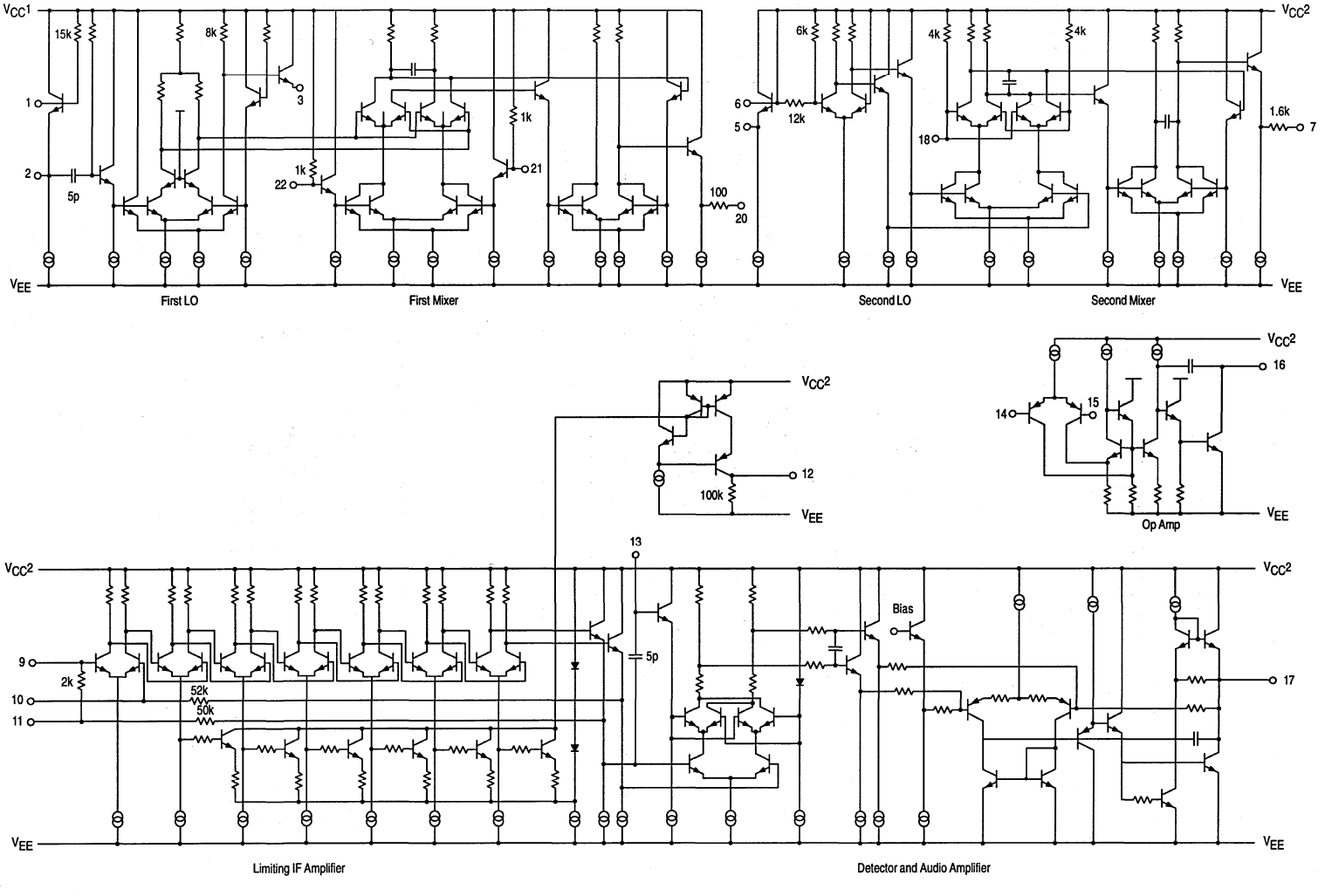
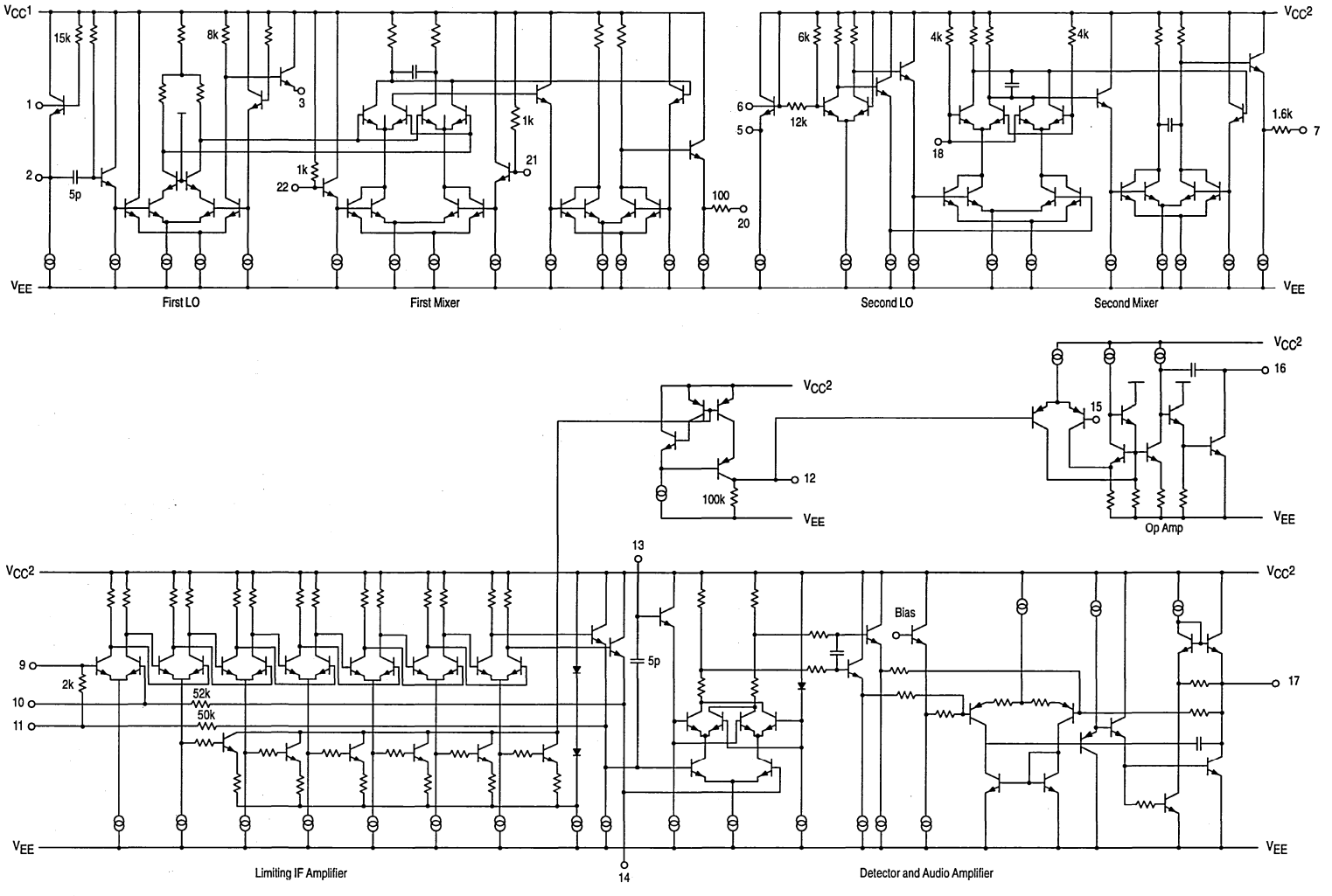


Figure 22. MC13136 Internal Schematic



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13155

Advance Information

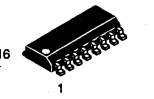
Wideband FM IF

The MC13155 is a complete wideband FM detector designed for satellite TV and other wideband data and analog FM applications. This device may be cascaded for higher IF gain and extended Receive Signal Strength Indicator (RSSI) range.

- 12 MHz Video/Baseband Demodulator
- Ideal for Wideband Data and Analog FM Systems
- Limiter Output for Cascade Operation
- Low Drain Current: 7.0 mA
- Low Supply Voltage: 3.0 to 6.0 V
- Operates to 300 MHz

WIDEBAND FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT



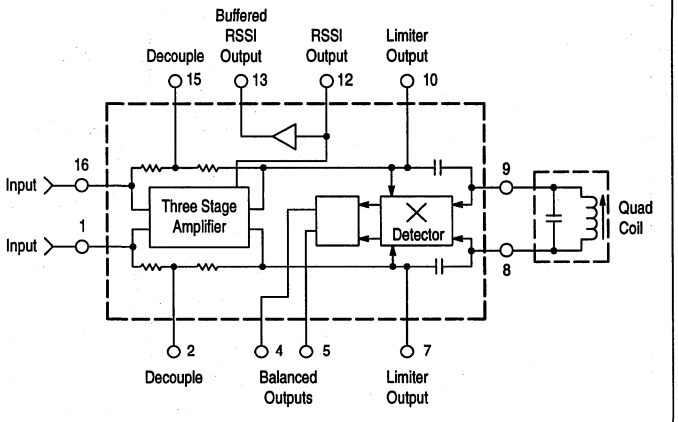
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	11, 14	V_{EE} (max)	6.5	Vdc
Input Voltage	1, 16	V_{in}	1.0	Vrms
Junction Temperature	—	T_J	+150	°C
Storage Temperature Range	—	T_{stg}	– 65 to +150	°C

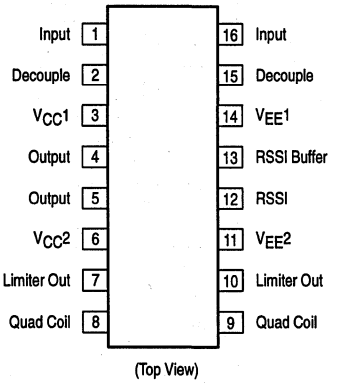
NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.

Simplified Block Diagram



NOTE: This device requires careful layout and decoupling to ensure stable operation.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC13155D	– 40° to + 85°C	SO-16

This document contains information on a new product. Specifications and information herein are subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage (T_A= 25°C) – 40°C ≤ T_A ≤ 85°C	11, 14 3, 6	V_{EE} V_{CC}	– 3.0 to – 6.0 Grounded	Vdc
Maximum Input Frequency	1, 16	f_{in}	300	MHz
Ambient Temperature Range	—	T_J	– 40 to + 85	°C

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, no input signal.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Drain Current	11	I_{11}	2.0	2.8	4.0	mA
(V_{EE} = – 5.0 Vdc)	14	I_{14}	3.0	4.3	6.0	
(V_{EE} = – 5.0 Vdc)	14	I_{14}	3.0	4.3	6.0	
Drain Current Total (see Figure 3)	11, 14	I_{Total}	5.0	7.1	10	mA
(V_{EE} = – 5.0 Vdc)			5.0	7.5	10.5	
(V_{EE} = – 6.0 Vdc)			5.0	7.5	10.5	
(V_{EE} = – 3.0 Vdc)			4.7	6.6	9.5	

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, f_{IF} = 70 MHz, V_{EE} = – 5.0 Vdc Figure 2, unless otherwise noted.)

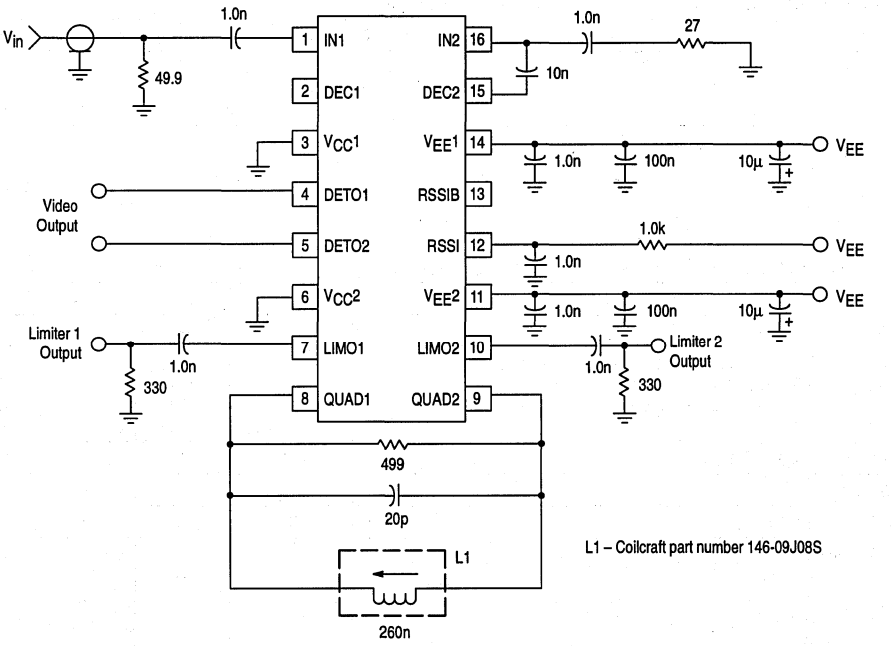
Characteristic	Pin	Min	Typ	Max	Unit
Input for - 3 dB Limiting Sensitivity	1, 16	—	1.0	2.0	mVrms
Differential Detector Output Voltage (V_{in} = 10 mVrms)	4, 5				mV_{p-p}
(f_{dev} = ± 3.0 MHz) (V_{EE} = – 6.0 Vdc)		470	590	700	
(V_{EE} = – 5.0 Vdc)		450	570	680	
(V_{EE} = – 3.0 Vdc)		380	500	620	
Detector DC Offset Voltage	4, 5	– 250	—	250	mVdc
RSSI Slope	13	1.4	2.1	2.8	µA/dB
RSSI Dynamic Range	13	31	35	39	dB
RSSI Output	12				µA
(V_{in} = 100 µVrms)		—	2.1	—	
(V_{in} = 1.0 mVrms)		—	2.4	—	
(V_{in} = 10 mVrms)		16	24	36	
(V_{in} = 100 mVrms)		—	65	—	
(V_{in} = 500 mVrms)		—	75	—	
RSSI Buffer Maximum Output Current (V_{in} = 10 mVrms)	13	—	2.3	—	mAdc
Differential Limiter Output					mVrms
(V_{in} = 1.0 mVrms)	7, 10	100	140	—	
(V_{in} = 10 mVrms)		—	180	—	
Demodulator Video 3.0 dB Bandwidth	4, 5	—	12	—	MHz
Input Impedance (Figure 14)	1, 16				
@ 70 MHz Rp (V_{EE} = – 5.0 Vdc)		—	450	—	Ω
Cp (C_2=C_{15} = 100 p)		—	4.8	—	pF
Differential IF Power Gain	1, 7, 10, 16	—	46	—	dB

NOTE: Positive currents are out of the pins of the device.

CIRCUIT DESCRIPTION

The MC13155 consists of a wideband three-stage limiting amplifier, a wideband quadrature detector which may be operated up to 200 MHz, and a received signal strength indicator (RSSI) circuit which provides a current output linearly proportional to the IF input signal level for approximately 35 dB range of input level.

Figure 2. Test Circuit



APPLICATION INFORMATION

Evaluation PC Board

The evaluation PCB shown in Figures 19 and 20 is very versatile and is designed to cascade two ICs. The center section of the board provides an area for attaching all surface mount components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 17 and 18). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Limiting Amplifier

Differential input and output ports interfacing the three stage limiting amplifier provide a differential power gain of typically 46 dB and useable frequency range of 300 MHz. The IF gain flatness may be controlled by decoupling of the internal feedback network at Pins 2 and 15.

Scattering parameter (S-parameter) characterization of the IF as a two port linear amplifier is useful to implement maximum stable power gain, input matching, and stability over a desired bandpass response and to ensure stable operation outside the bandpass as well. The MC13155 is unconditionally stable over most of its useful operating frequency range; however, it can be made unconditionally stable over its entire operating range with the proper decoupling of Pins 2 and 15. Relatively small decoupling capacitors of about 100 pF have a significant effect on the wideband response and stability. This is shown in the scattering parameter tables where S-parameters are shown for various values of C2 and C15 and at V_{EE} of – 3.0 and – 5.0 Vdc.

TYPICAL PERFORMANCE AT TEMPERATURE
(See Figure 2. Test Circuit)

Figure 3. Drain Current versus Supply Voltage

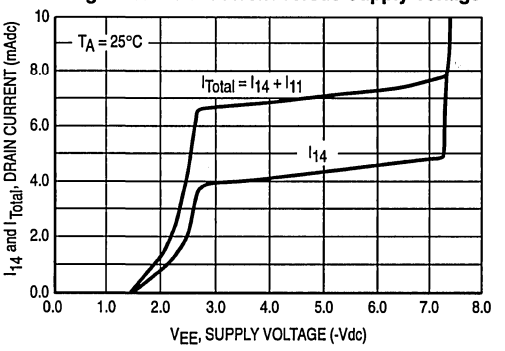


Figure 4. RSSI Output versus Frequency and Input Signal Level

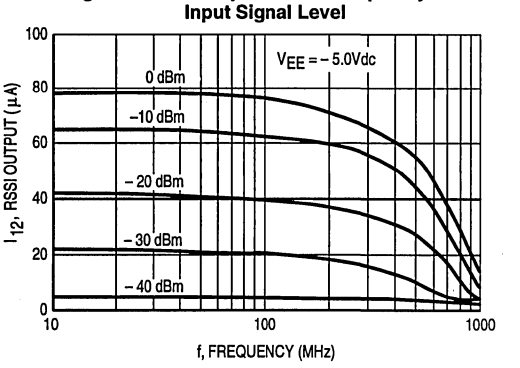


Figure 5. Total Drain Current versus Ambient Temperature and Supply Voltage

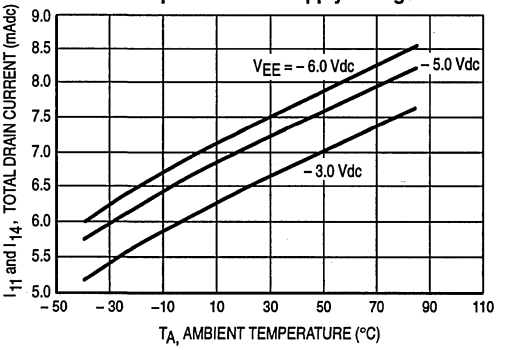


Figure 6. Detector Drain Current and Limiter Drain Current versus Ambient Temperature

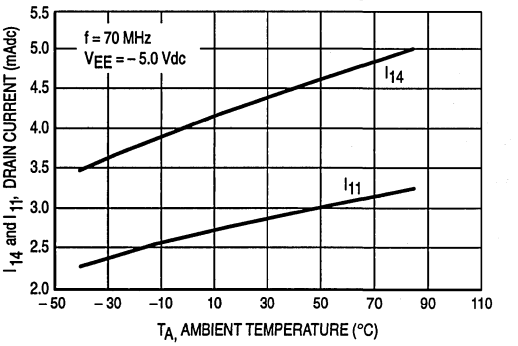


Figure 7. RSSI Output versus Ambient Temperature and Supply Voltage

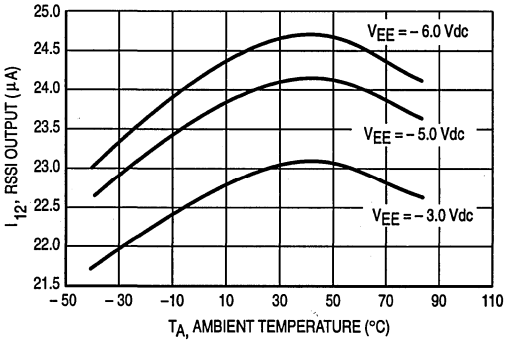


Figure 8. RSSI Output versus Input Signal Voltage (V_{in} at Temperature)

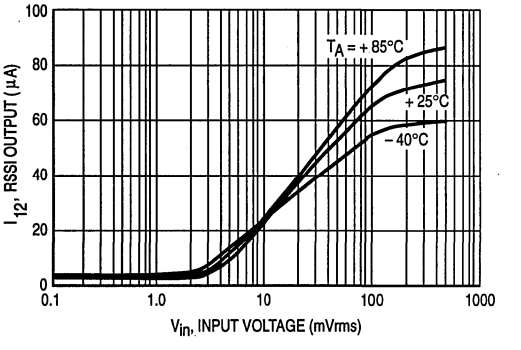


Figure 9. Differential Detector Output Voltage versus Ambient Temperature and Supply Voltage

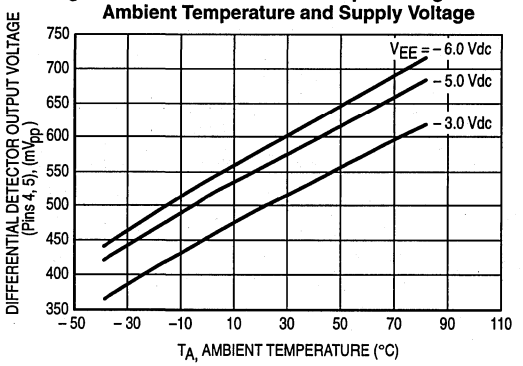


Figure 10. Differential Limiter Output Voltage versus Ambient Temperature (V_{in} = 1 and 10 mVrms)

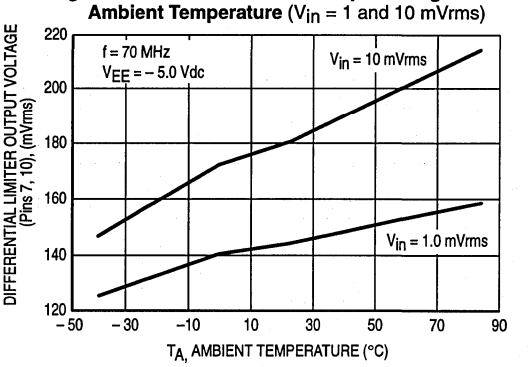


Figure 11A. Differential Detector Output Voltage versus Q of Quadrature LC Tank

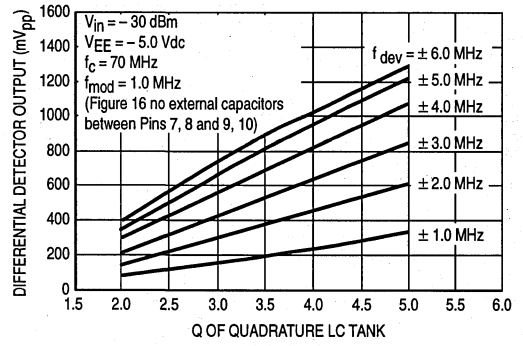


Figure 11B. Differential Detector Output Voltage versus Q of Quadrature LC Tank

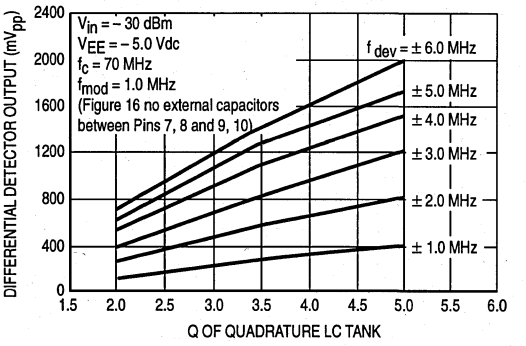


Figure 12. RSSI Output Voltage versus IF Input

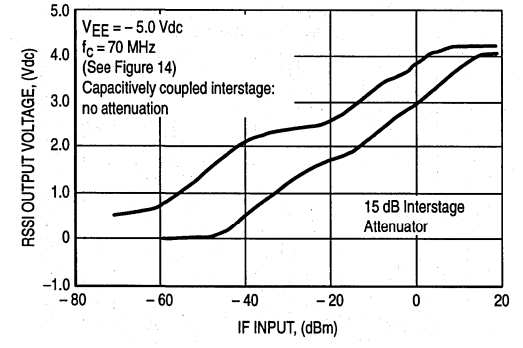
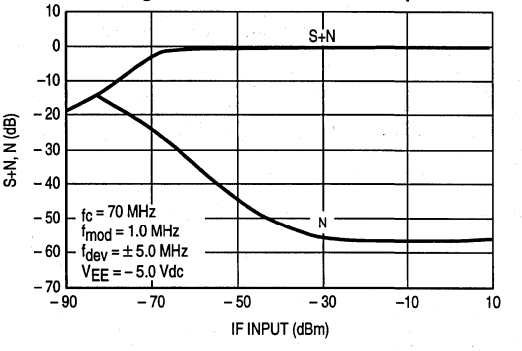


Figure 13. – S+N, N versus IF Input



In the S-parameters measurements, the IF is treated as a two-port linear class A amplifier. The IF amplifier is measured with a single-ended input and output configuration in which the Pins 16 and 7 are terminated in the series combination of a 47 Ω resistor and a 10 nF capacitor to V_{CC} ground (see Figure 11– S-Parameter Test Circuit).

The S-parameters are in polar form as the magnitude (MAG) and angle (ANG). Also listed in the tables are the calculated values for the stability factor (K) and the Maximum Available Gain (MAG). These terms are related in the following equations:

$$K = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2) / (2 |S_{12} S_{21}|)$$

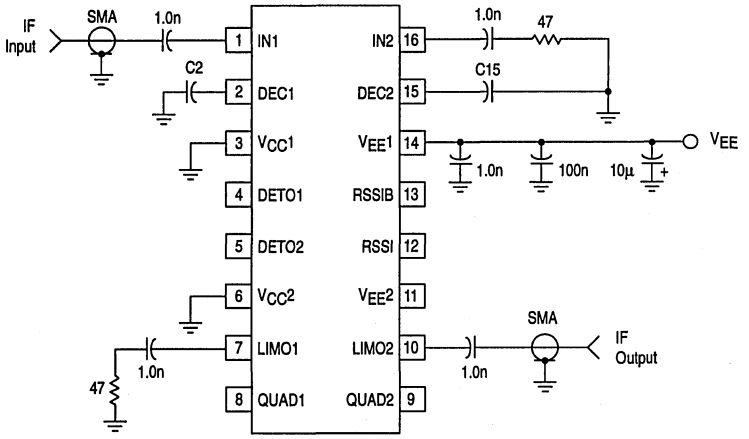
where: $|\Delta| = |S_{11} S_{22} - S_{12} S_{21}|$.

$$MAG = 10 \log |S_{21}| / |S_{12}| + 10 \log |K - (K^2 - 1)^{1/2}|$$

where: K > 1. The necessary and sufficient conditions for unconditional stability are given as K > 1:

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0$$

Figure 14. S-Parameter Test Circuit



S-Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 0 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.94	–13	8.2	143	0.001	7.0	0.87	– 22	2.2	32
2.0	0.78	– 23	23.5	109	0.001	– 40	0.64	– 31	4.2	33.5
5.0	0.48	1.0	39.2	51	0.001	– 97	0.34	–17	8.7	33.7
7.0	0.59	15	40.3	34	0.001	– 41	0.33	–13	10.6	34.6
10	0.75	17	40.9	19	0.001	– 82	0.41	–1.0	5.7	36.7
20	0.95	7.0	42.9	– 6.0	0.001	– 42	0.45	0	1.05	46.4
50	0.98	–10	42.2	– 48	0.001	– 9.0	0.52	– 3.0	0.29	—
70	0.95	–16	39.8	– 68	0.001	112	0.54	–16	1.05	46.4
100	0.93	– 23	44.2	– 93	0.001	80	0.53	– 22	0.76	—
150	0.91	– 34	39.5	–139	0.001	106	0.50	– 34	0.94	—
200	0.87	– 47	34.9	–179	0.002	77	0.42	– 44	0.97	—
500	0.89	–103	11.1	– 58	0.022	57	0.40	–117	0.75	—
700	0.61	–156	3.5	–164	0.03	0	0.52	179	2.6	13.7
900	0.56	162	1.2	92	0.048	- 44	0.47	112	4.7	4.5
1000	0.54	131	0.8	42	0.072	- 48	0.44	76	5.1	0.4

S-Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 100 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.98	–15	11.7	174	0.001	–14	0.84	– 27	1.2	37.4
2.0	0.50	– 2.0	39.2	85.5	0.001	–108	0.62	– 35	6.0	35.5
5.0	0.87	8.0	39.9	19	0.001	100	0.47	– 9.0	4.2	39.2
7.0	0.90	5.0	40.4	9.0	0.001	– 40	0.45	– 8.0	3.1	40.3
10	0.92	3.0	41	1.0	0.001	– 40	0.44	– 5.0	2.4	41.8
20	0.92	– 2.0	42.4	–14	0.001	– 87	0.49	– 6.0	2.4	41.9
50	0.91	– 8.0	41.2	– 45	0.001	85	0.50	– 5.0	2.3	42
70	0.91	–11	39.1	– 63	0.001	76	0.52	– 4.0	2.2	41.6
100	0.91	–15	43.4	– 84	0.001	85	0.50	–11	1.3	43.6
150	0.90	– 22	38.2	–126	0.001	96	0.43	– 22	1.4	41.8
200	0.86	– 33	35.5	–160	0.002	78	0.43	– 21	1.3	39.4
500	0.80	– 66	8.3	– 9.0	0.012	75	0.57	– 63	1.7	23.5
700	0.62	– 96	2.9	– 95	0.013	50	0.49	–111	6.3	12.5
900	0.56	–120	1.0	–171	0.020	53	0.44	–150	13.3	2.8
1000	0.54	–136	0.69	154	0.034	65	0.44	–179	12.5	– 0.8

S-Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 680 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.74	4.0	53.6	110	0.001	101	0.97	– 35	0.58	—
2.0	0.90	3.0	70.8	55	0.001	60	0.68	– 34	1.4	45.6
5.0	0.91	0	87.1	21	0.001	–121	0.33	– 60	1.1	49
7.0	0.91	0	90.3	11	0.001	–18	0.25	– 67	1.2	48.4
10	0.91	– 2.0	92.4	2.0	0.001	33	0.14	– 67	1.5	47.5
20	0.91	– 4.0	95.5	–16	0.001	63	0.12	–15	1.3	48.2
50	0.90	– 8.0	89.7	– 50	0.001	– 43	0.24	26	1.8	46.5
70	0.90	–10	82.6	–70	0.001	92	0.33	21	1.4	47.4
100	0.91	–14	77.12	–93	0.001	23	0.42	–1.0	1.05	49
150	0.94	– 20	62.0	–122	0.001	96	0.42	– 22	0.54	—
200	0.95	– 33	56.9	–148	0.003	146	0.33	– 62	0.75	—
500	0.82	– 63	12.3	–12	0.007	79	0.44	– 67	1.8	26.9
700	0.66	– 98	3.8	–107	0.014	84	0.40	–115	4.8	14.6
900	0.56	–122	1.3	177	0.028	78	0.39	–166	8.0	4.7
1000	0.54	–139	0.87	141	0.048	76	0.41	165	7.4	0.96

S-Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 0 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.89	–14	9.3	136	0.001	2.0	0.84	– 27	3.2	30.7
2.0	0.76	– 22	24.2	105	0.001	– 90	0.67	– 37	3.5	34.3
5.0	0.52	5.0	35.7	46	0.001	– 32	0.40	–13	10.6	33.3
7.0	0.59	12	38.1	34	0.001	– 41	0.40	–10	9.1	34.6
10	0.78	15	37.2	16	0.001	– 92	0.40	–1.0	5.7	36.3
20	0.95	5.0	38.2	– 9.0	0.001	47	0.51	– 4.0	0.94	—
50	0.96	–11	39.1	– 50	0.001	–103	0.48	– 6.0	1.4	43.7
70	0.93	–17	36.8	– 71	0.001	– 76	0.52	–13	2.2	41.4
100	0.91	– 25	34.7	– 99	0.001	–152	0.51	–19	3.0	39.0
150	0.86	– 37	33.8	–143	0.001	53	0.49	– 34	1.7	39.1
200	0.81	– 49	27.8	86	0.003	76	0.55	– 56	2.4	35.1
500	0.70	– 93	6.2	– 41	0.015	93	0.40	–110	2.4	19.5
700	0.62	–144	1.9	–133	0.049	56	0.40	–150	3.0	8.25
900	0.39	–176	0.72	125	0.11	–18	0.25	163	5.1	–1.9
1000	0.44	166	0.49	80	0.10	– 52	0.33	127	7.5	– 4.8

S-Parameters (V_{EE} = - 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 100 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.97	–15	11.7	171	0.001	– 4.0	0.84	– 27	1.4	36.8
2.0	0.53	2.0	37.1	80	0.001	– 91	0.57	– 31	6.0	34.8
5.0	0.88	7.0	37.7	18	0.001	– 9.0	0.48	– 7.0	3.4	39.7
7.0	0.90	5.0	37.7	8.0	0.001	–11	0.49	– 7.0	2.3	41
10	0.92	2.0	38.3	1.0	0.001	– 59	0.51	– 9.0	2.0	41.8
20	0.92	– 2.0	39.6	–15	0.001	29	0.48	– 3.0	1.9	42.5
50	0.91	– 8.0	38.5	– 46	0.001	– 21	0.51	– 7.0	2.3	41.4
70	0.91	–11	36.1	– 64	0.001	49	0.50	– 8.0	2.3	40.8
100	0.91	–15	39.6	– 85	0.001	114	0.52	–13	1.7	37.8
150	0.89	– 22	34.4	–128	0.001	120	0.48	– 23	1.6	40.1
200	0.86	– 33	32	–163	0.002	86	0.40	– 26	1.7	37.8
500	0.78	– 64	7.6	–12	0.013	94	0.46	– 71	1.9	22.1
700	0.64	– 98	2.3	–102	0.027	58	0.42	–109	4.1	10.1
900	0.54	–122	0.78	179	0.040	38.6	0.35	–147	10.0	– 0.14
1000	0.53	–136	0.47	144	0.043	23	0.38	–171	15.4	– 4.52

S-Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 680 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.81	3.0	37	101	0.001	–19	0.90	– 32	1.1	43.5
2.0	0.90	2.0	47.8	52.7	0.001	– 82	0.66	– 39	0.72	—
5.0	0.91	0	58.9	20	0.001	104	0.37	– 56	2.3	44
7.0	0.90	–1	60.3	11	0.001	– 76	0.26	– 55	2.04	44
10	0.91	– 2.0	61.8	3.0	0.001	105	0.18	– 52	2.2	43.9
20	0.91	– 4.0	63.8	– 15	0.001	59	0.11	–13	2.0	44.1
50	0.90	– 8.0	60.0	– 48	0.001	96	0.22	33	2.3	43.7
70	0.90	–11	56.5	– 67	0.001	113	0.29	15	2.3	43.2
100	0.91	–14	52.7	– 91	0.001	177	0.36	5.0	2.0	43
150	0.93	– 21	44.5	–126	0.001	155	0.35	–17	1.8	42.7
200	0.90	– 43	41.2	–162	0.003	144	0.17	– 31	1.6	34.1
500	0.79	– 65	7.3	–13	0.008	80	0.44	– 75	3.0	22
700	0.65	– 97	2.3	–107	0.016	86	0.38	–124	7.1	10.2
900	0.56	–122	0.80	174	0.031	73	0.38	–174	12	0.37
1000	0.55	–139	0.52	137	0.50	71	0.41	157	11.3	– 3.4

DC Biasing Considerations

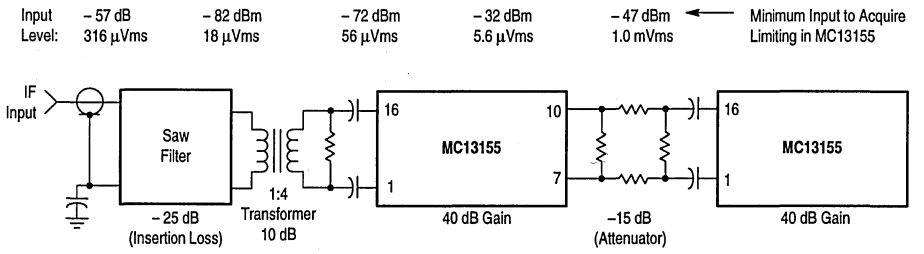
The DC biasing scheme utilizes two V_{CC} connections (Pins 3 and 6) and two V_{EE} connections (Pins 14 and 11). $V_{EE}1$ (Pin 14) is connected internally to the IF and RSSI circuits' negative supply bus while $V_{EE}2$ (Pin 11) is connected internally to the quadrature detector's negative bus. Under positive ground operation, this unique configuration offers the ability to bias the RSSI and IF separately from the quadrature detector. When two ICs are cascaded as shown in the 70 MHz application circuit and provided by the PCB (see Figures 17 and 18), the first MC13155 is used without biasing its quadrature detector, thereby saving approximately 3.0 mA. A total current of 7.0 mA is used to fully bias each IC, thus the total current in the application circuit is approximately 11 mA. Both V_{CC} pins are biased by the same supply. $V_{CC}1$ (Pin 3) is connected internally to the positive bus of the first half of the IF limiting amplifier, while $V_{CC}2$ is internally connected to the positive bus of the RSSI, the quadrature detector circuit, and the second half of the IF limiting amplifier (see Figure 15). This distribution of the V_{CC} enhances the stability of the IC.

RSSI Circuitry

The RSSI circuitry provides typically 35 dB of linear dynamic range and its output voltage swing is adjusted by selection of the resistor from pin 12 to V_{EE}. The RSSI slope is typically 2.1 μA/dB ; thus, for a dynamic range of 35 dB, the current output is approximately 74 μA. A 47 k resistor will yield a RSSI output voltage swing of 3.5 Vdc. The RSSI buffer output at Pin 13 is an emitter-follower and needs an external emitter resistor of 10 k to V_{EE}.

In a cascaded configuration (see circuit application in Figure 16), only one of the RSSI Buffer outputs (Pin 13) is used; the RSSI outputs (Pin 12 of each IC) are tied together and the one closest to the V_{EE} supply trace is decoupled to V_{CC} ground. The two pins are connected to V_{EE} through a 47 k resistor. This resistor sources a RSSI current which is proportional to the signal level at the IF input; typically, 1.0 mVrms (– 47 dBm) is required to place the MC13155 into limiting. The measured RSSI output voltage response of the application circuit is shown in Figure 12. Since the RSSI current output is dependent upon the input signal level at the IF input, a careful accounting of filter losses, matching and other losses and gains must be made in the entire receiver system. In the block diagram of the application circuit shown below, an accounting of the signal levels at points throughout the system shows how the RSSI response in Figure 12 is justified.

Block Diagram of 70 MHz Video Receiver Application Circuit

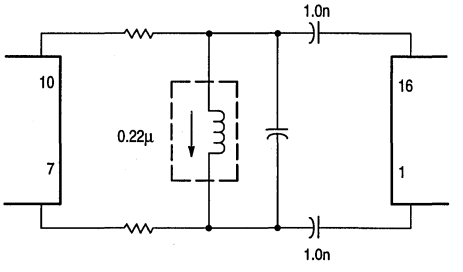


Cascading Stages

The limiting IF output is pinned-out differentially, cascading is easily achieved by AC coupling stage to stage. In the evaluation PCB, AC coupling is shown, however, interstage filtering may be desirable in some applications. In which case, the S-parameters provide a means to implement a low loss interstage match and better receiver sensitivity.

Where a linear response of the RSSI output is desired when cascading the ICs, it is necessary to provide at least 10 dB of interstage loss. Figure 12 shows the RSSI response with and without interstage loss. A 15 dB resistive attenuator is an inexpensive way to linearize the RSSI response. This has its drawbacks since it is a wideband noise source that is dependent upon the source and load impedance and the amount of attenuation that it provides. A better, although more costly, solution would be a bandpass filter designed to the desired center frequency and bandpass response while carefully selecting the insertion loss. A network topology shown below may be used to provide a bandpass response with the desired insertion loss.

Network Topology



Quadrature Detector

The quadrature detector is coupled to the IF with internal 2.0 pF capacitors between Pins 7 and 8 and Pins 9 and 10. For wideband data applications, such as FM video and satellite receivers, the drive to the detector can be increased with additional external capacitors between these pins, thus, the recovered video signal level output is increased for a given bandwidth (see Figure 11A and Figure 11B).

The wideband performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit's bandwidth:

$$Q = R_T/X_L \quad (1)$$

where: R_T is the equivalent shunt resistance across the LC Tank and X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

The inductor and capacitor are chosen to form a resonant LC Tank with the PCB and parasitic device capacitance at the desired IF center frequency as predicted by:

$$fc = (2\pi \sqrt{(LC_p)})^{-1} \quad (2)$$

where: L is the parallel tank inductor and C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a wideband detector at 70 MHz and a loaded Q of 5. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 70 MHz and an IF bandpass of 10.9 MHz, the IF bandpass Q is approximately 6.4.

Example:

Let the external Cext = 20 pF. (The minimum value here should be greater than 15 pF making it greater than the internal device and PCB parasitic capacitance, Cint ≈ 3.0 pF).

$$C_p = Cint + Cext = 23\ pF$$

Rewrite Equation 2 and solve for L:

$L = (0.159)^2 /(C_p\ fc^2)$

L = 198 nH, thus, a standard value is chosen.

L = 0.22 μH (tunable shielded inductor).

The value of the total damping resistor to obtain the required loaded Q of 5 can be calculated by rearranging Equation 1:

$$R_T = Q(2\pi fL)$$

$R_T = 5\ (2\pi)(70)(0.22) = 483.8\ \Omega$.

The internal resistance, Rint between the quadrature tank Pins 8 and 9 is approximately 3200 Ω and is considered in determining the external resistance, Rext which is calculated from:

$Rext = ((R_T)(Rint))/\ (Rint - R_T)$

Rext = 570, thus, choose the standard value.

Rext =560 Ω.

SAW Filter

In wideband video data applications, the IF occupied bandwidth may be several MHz wide. A good rule of thumb is to choose the IF frequency about 10 or more times greater than the IF occupied bandwidth. The IF bandpass filter is a SAW filter in video data applications where a very selective response is needed (i.e., very sharp bandpass response). The evaluation PCB is laid out to accommodate two SAW filter package types: 1) A five-leaded plastic SIP package. Recommended part numbers are Siemens X6950M which operates at 70 MHz; 10.4 MHz 3 dB passband, X6951M (X252.8) which operates at 70 MHz; 9.2 MHz 3 dB passband; and X6958M which operates at 70 MHz, 6.3 MHz 3 dB passband, and 2) A four-leaded TO-39 metal can package. Typical insertion loss in a wide bandpass SAW filter is 25 dB.

The above SAW filters require source and load impedances of 50 Ω to assure stable operation. On the PC board layout, space is provided to add a matching network, such as a 1:4 surface mount transformer between the SAW filter output and the input to the MC13155. A 1:4 transformer, made by Coilcraft and Mini Circuits, provides a suitable interface (see Figures 16, 17 and 18). In the circuit and layout, the SAW filter and the MC13155 are differentially configured with interconnect traces which are equal in length and symmetrical. This balanced feed enhances RF stability, phase linearity, and noise performance.

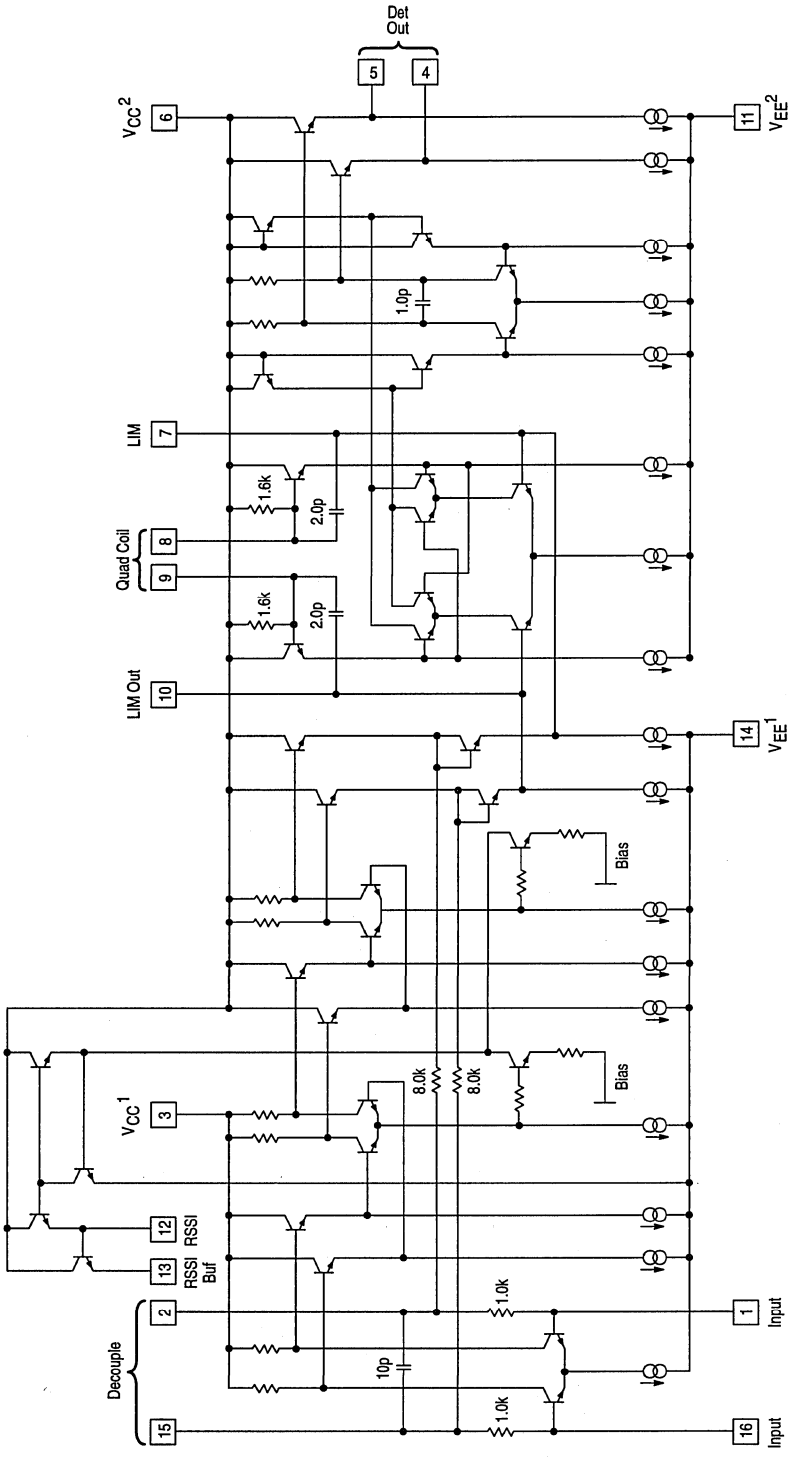


Figure 15. Simplified Internal Circuit Schematic

Figure 16. 70 MHz Video Receiver Application Circuit

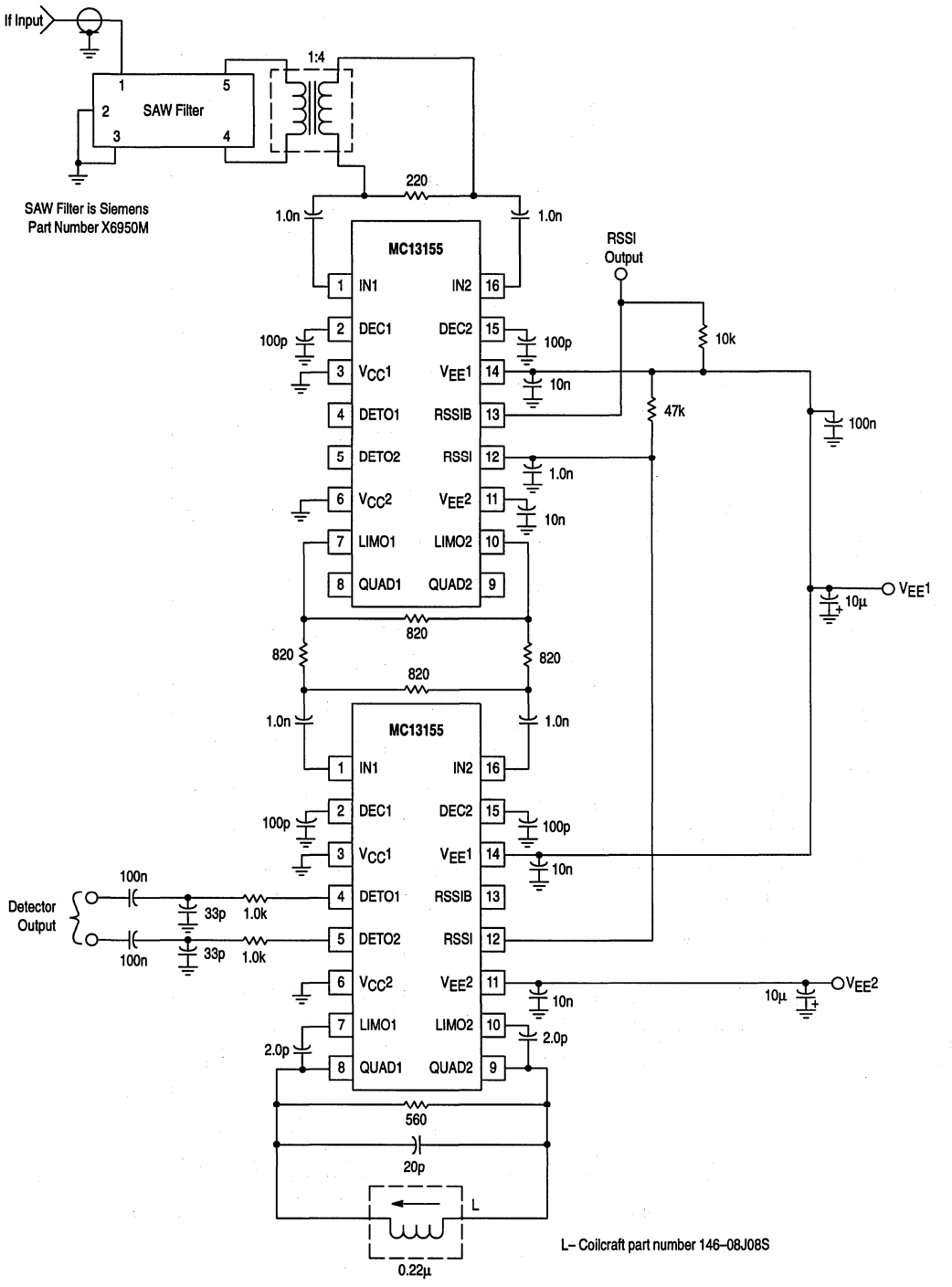


Figure 17. Component Placement (Circuit Side)

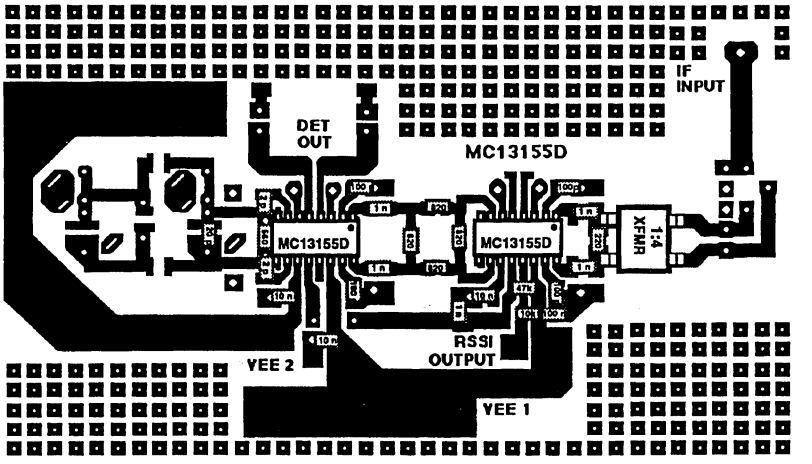


Figure 18. Component Placement (Ground Side)

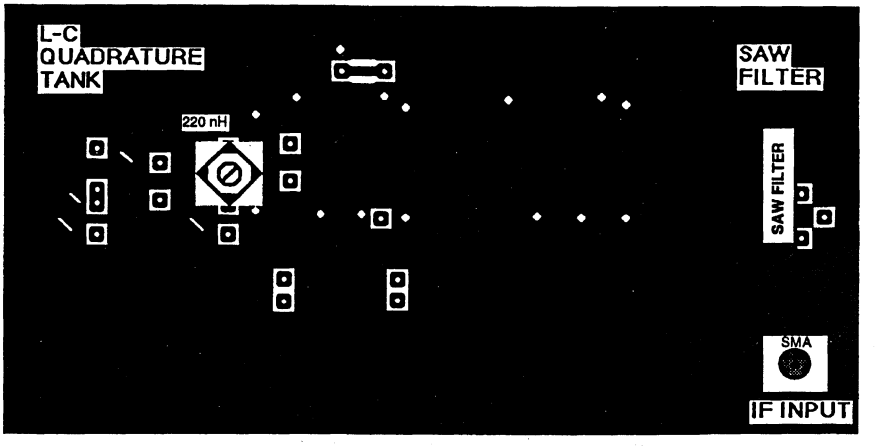


Figure 19. Circuit Side View

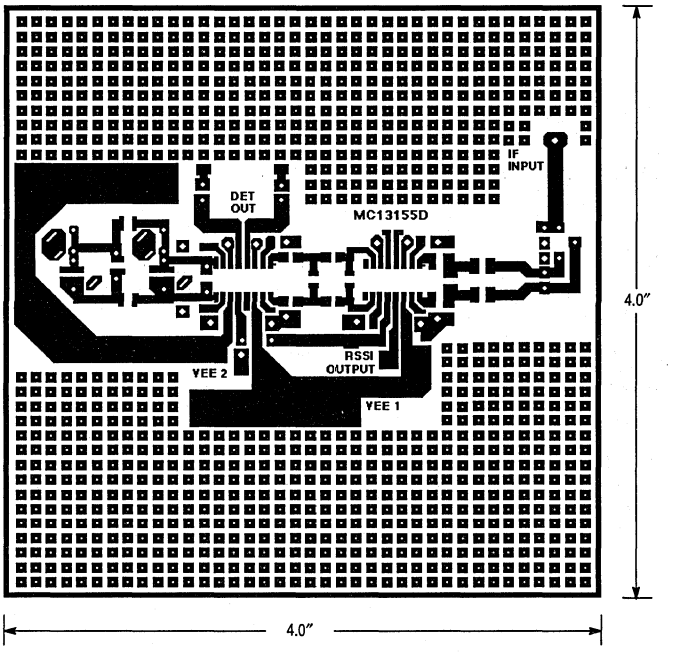
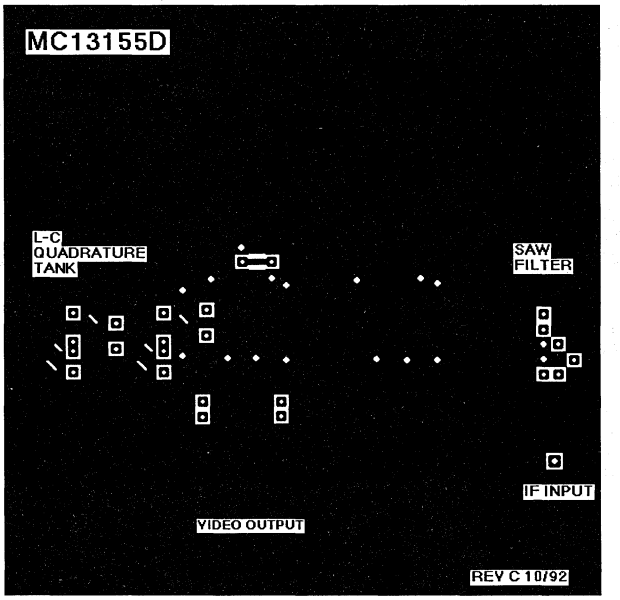


Figure 20. Ground Side View



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13156

Product Preview

Wideband FM IF System

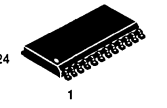
WIDEBAND FM IF SYSTEM for DIGITAL and ANALOG APPLICATIONS

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC13156 is a wideband FM IF subsystem targeted at high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13156 has an onboard Colpitts VCO for PLL controlled multichannel operation. The mixer is useful to beyond 200 MHz and may be used in a differential, balanced, or single-ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has a hold function to preset the shaper for fast recovery of new data.

Applications for the MC13156 include CT–2, wideband data links, and other radio systems utilizing GMSK, FSK or FM modulation.

- 3.0 to 6.0 Vdc Operation
- Typical Sensitivity at 200 MHz of 6.0 μV for 12 dB SINAD
- RSSI Range of >70 dB
- High Performance Data Shaper for Enhanced CT-2 Operation
- Internal 330 Ω Termination for 10.7 MHz Filters
- Split IF for Improved Filtering and Extended RSSI Range
- 3rd Order Intercept (Input) Target of –10 dBm

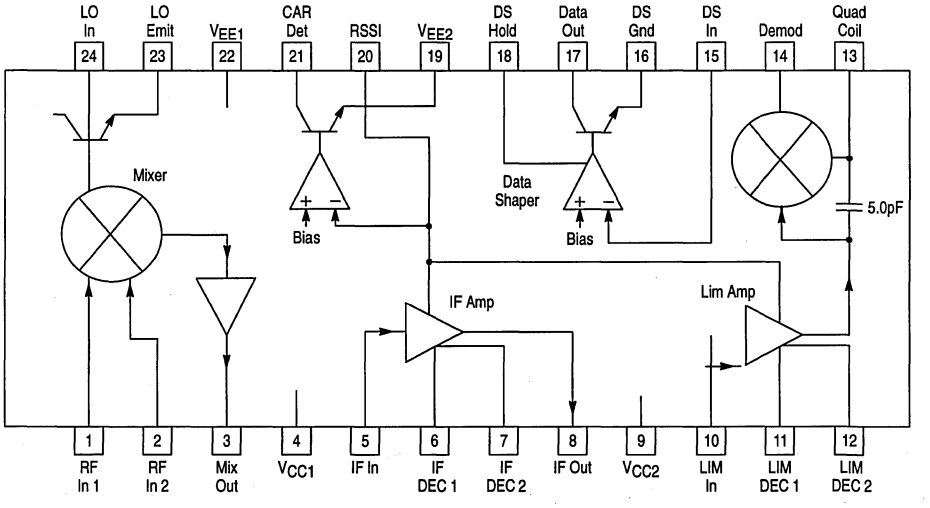


DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO-24L)

ORDERING INFORMATION

Device	Temperature Range	Package
MC13156DW	– 40° to + 85°C	SO-24L

Pin Connections and Block Diagram



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13175
MC13176

Advance Information

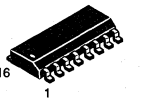
UHF FM/AM Transmitter

UHF FM/AM TRANSMITTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

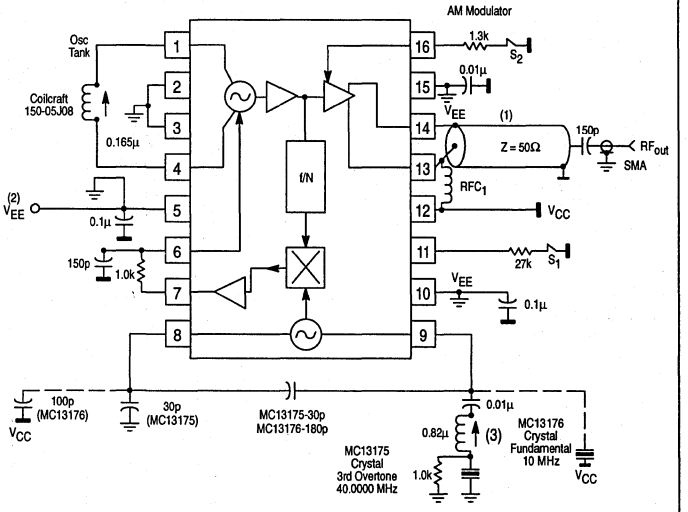
The MC13175 and MC13176 are one chip FM/AM transmitter subsystems designed for AM/FM communication systems. They include a Colpitts crystal reference oscillator, UHF oscillator, ÷ 8 (MC13175) or ÷ 32 (MC13176) prescaler and phase detector forming a versatile PLL system. Targeted applications are in the 260 to 470 MHz band and 902 to 928 MHz band covered by FCC Title 47; Part 15. Other applications include local oscillator sources in UHF and 900 MHz receivers, UHF and 900 MHz video transmitters, RF Local Area Networks (LANs), and high frequency clock drivers. The MC13175/76 offer the following features:

- UHF Current Controlled Oscillator
- Uses Easily Available 3rd Overtone or Fundamental Crystals for Reference
- Fewer External Parts Required
- Low Operating Supply Voltage (1.8 to 5.0 Vdc)
- Low Supply Drain Currents
- Power Output Adjustable (Up to +10 dBm)
- Differential Output for Loop Antenna or Balun Transformer Networks
- Power Down Feature
- ASK Modulated by Switching Output On and Off
- (MC13175) $f_O = 8 \times f_{ref}$; (MC13176) $f_O = 32 \times f_{ref}$



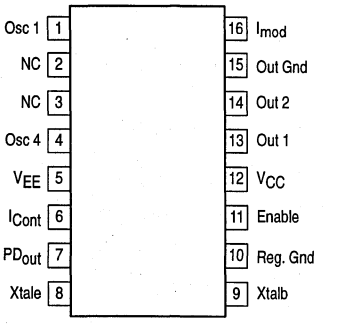
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

Figure 1. Typical Application as 320 MHz AM Transmitter



NOTES: 1. 50 Ω coaxial balun, 1/10 wavelength at 320 MHz equals 1.5 inches.
2. Pins 5, 10 & 15 are ground and connected to V_{EE} which is the component/DC ground plane side of PCB. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. The crystal oscillator circuit may be adjusted for frequency with the variable inductor (MC13175); recommended source is Coilcraft "slot seven" 7mm tuneable inductor, Part #7M3-821. 1.0k resistor. Shunting the crystal prevents it from oscillating in the fundamental mode.

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC13175D	– 40° to +85°C	SO-16
MC13176D		SO-16

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

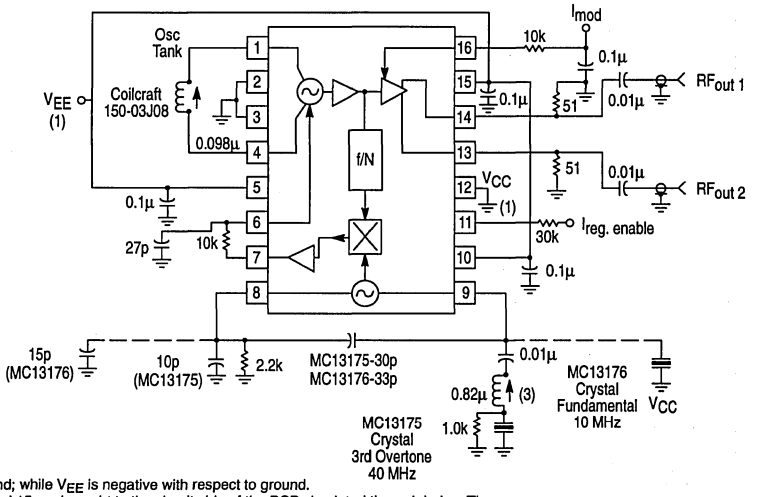
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	1.8 to 5.0	Vdc
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (Figure 2; V_{EE} = – 3.0 Vdc, T_A = 25°C, unless otherwise noted.)*

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Supply Current (Power down: I_{11} & I_{16} = 0)	—	I_{EE1}	– 0.5	—	—	µA
Supply Current (Enable [Pin 11] to V_{CC} thru 30 k, I_{16} = 0)	—	I_{EE2}	–18	–14	—	mA
Total Supply Current (Transmit Mode) (I_{mod} = 2.0 mA; f_o = 320 MHz)	—	I_{EE3}	– 39	– 34	—	mA
Differential Output Power (f_o = 320 MHz; V_{ref} [Pin 9] = 500 mV_{p-p}; f_o = N x f_{ref}) I_{mod} = 2.0 mA (see Figure 7, 8) I_{mod} = 0 mA	13 & 14	P_{out}	 2.0 —	 + 4.7 – 45	 — —	dBm
Hold-in Range (± Δf_{ref} x N) MC13175 (see Figure 7) MC13176 (see Figure 8)	13 & 14	± Δf_H	 3.5 4.0	 6.5 8.0	 — —	MHz
Phase Detector Output Error Current MC13175 MC13176	7	I_{error}	 20 22	 25 27	 — —	µA
Oscillator Enable Time (see Figure 22b)	11, 8	t_{enable}	—	4.0	—	ms
Amplitude Modulation Bandwidth (see Figure 24)	16	BW_{AM}	—	25	—	MHz
Spurious Outputs (I_{mod} = 2.0 mA) Spurious Outputs (I_{mod} = 0 mA)	13 & 14 13 & 14	P_{son} P_{soff}	— —	– 50 – 50	— —	dBc
Maximum Divider Input Frequency Maximum Output Frequency	— 13 & 14	f_{div} f_o	— —	950 950	— —	MHz

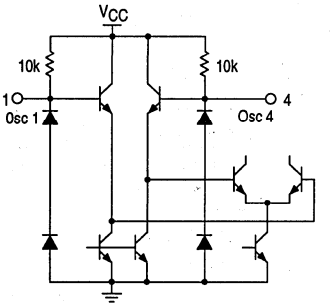
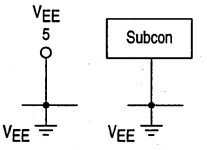
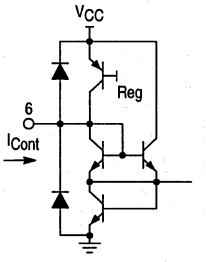
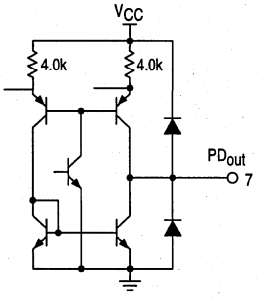
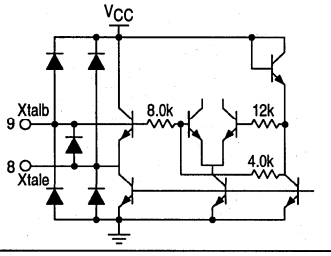
* For testing purposes, V_{CC} is ground (see Figure 2).

Figure 2. 320 MHz Test Circuit



NOTES: 1. V_{CC} is ground; while V_{EE} is negative with respect to ground.
2. Pins 5, 10 and 15 are brought to the circuit side of the PCB via plated through holes. They are connected together with a trace on the PCB and each Pin is decoupled to V_{CC} (ground).
3. Recommended source is Coilcraft "slot seven" inductor, part number 7M3-821.

PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1 & 4	Osc 1, Osc 4		**CCO Inputs** The oscillator is a current controlled type. An external oscillator coil is connected to Pins 1 and 4 which forms a parallel resonance LC tank circuit with the internal capacitance of the IC and with parasitic capacitance of the PC board. Three base-emitter capacitances in series configuration form the capacitance for the parallel tank. These are the base-emitters at Pins 1 and 4 and the base-emitter of the differential amplifier. The equivalent series capacitance in the differential amplifier is varied by the modulating current from the frequency control circuit (see Pin 6, internal circuit). A more thorough discussion is found in the Applications Information section.
5	V_{EE}		**Supply Ground (V_{EE})** In the PCB layout, the ground pins (also applies to Pins 10 and 15) should be connected directly to chassis ground. Decoupling capacitors to V_{CC} should be placed directly at the ground returns.
6	I_{Cont}		**Frequency Control** For V_{CC} = 3.0 Vdc, the voltage at Pin 6 is approximately 1.55 Vdc. The oscillator is current controlled by the error current from the phase detector. This current is amplified to drive the current source in the oscillator section which controls the frequency of the oscillator. Figures 9 and 10 show the Δf_{osc} versus I_{Cont}, Figure 5 shows the Δf_{osc} versus I_{Cont} at – 40°C, + 25°C and + 85°C for 320 MHz. The CCO may be FM modulated as shown in Figure 17, MC13176 320 MHz FM Transmitter. A detailed discussion is found in the Applications Information section.
7	PD_{out}		**Phase Detector Output** The phase detector provides ± 30 µA to keep the CCO locked at the desired carrier frequency. The output impedance of the phase detector is approximately 53 kΩ. Under closed loop conditions there is a DC voltage which is dependent upon the free running oscillator and the reference oscillator frequencies. The circuitry between Pins 7 and 6 should be selected for adequate loop filtering necessary to stabilize and filter the loop response. Low pass filtering between Pin 7 and 6 is needed so that the corner frequency is well below the sum of the divider and the reference oscillator frequencies, but high enough to allow for fast response to keep the loop locked. Refer to the Applications Information section regarding loop filtering and FM modulation.
8	Xtale		**Crystal Oscillator Inputs** The internal reference oscillator is configured as a common emitter Colpitts. It may be operated with either a fundamental or overtone crystal depending on the carrier frequency and the internal prescaler. Crystal oscillator circuits and specifications of crystals are discussed in detail in the applications section. With V_{CC} = 3.0 Vdc, the voltage at Pin 8 is approximately 1.8 Vdc and at Pin 9 is approximately 2.3 Vdc. 500 to 1000 mVp-p should be present at Pin 9. The Colpitts is biased at 200 µA; additional drive may be acquired by increasing the bias to approximately 500 µA. Use 6.2 k from Pin 8 to ground.

PIN DESCRIPTIONS

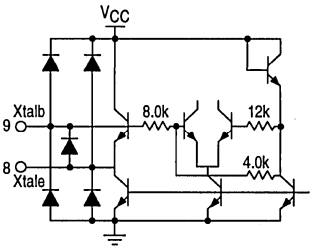
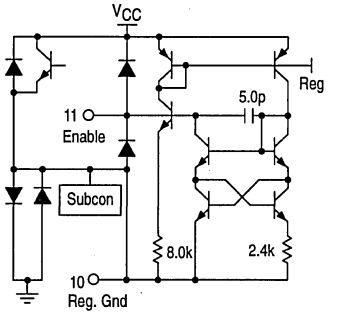
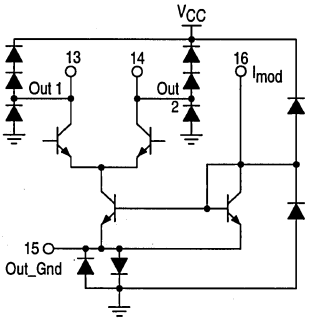
Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
9	Xtalb		**Crystal Oscillator Inputs** The internal reference oscillator is configured as a common emitter Colpitts. It may be operated with either a fundamental or overtone crystal depending on the carrier frequency and the internal prescaler. Crystal oscillator circuits and specifications of crystals are discussed in detail in the applications section. With V_{CC} = 3.0 Vdc, the voltage at Pin 8 is approximately 1.8 Vdc and at Pin 9 is approximately 2.3 Vdc. 500 to 1000 mVp-p should be present at Pin 9. The Colpitts is biased at 200 µA; additional drive may be acquired by increasing the bias to approximately 500 µA. Use 6.2 k from Pin 8 to ground.
10 11	Reg. Gnd Enable		**Regulator Ground** An additional ground pin is provided to enhance the stability of the system. Decoupling to the V_{CC} (RF ground) is essential; it should be done at the ground return for Pin 10. **Device Enable** The potential at Pin 11 is approximately 1.25 Vdc. When Pin 11 is open, the transmitter is disabled in a power down mode and draws less than 1.0 µA I_{CC} if the MOD at Pin 16 is also open (i.e., it has no current driving it). To enable the transmitter a current source of 10 µA to 90 µA is provided. Figures 3 and 4 show the relationship between I_{CC}, V_{CC} and $I_{reg.\ enable}$. Note that I_{CC} is flat at approximately 10 mA for $I_{reg.\ enable}$ = 5.0 to 100 µA (I_{mod} = 0).
12	V_{CC}		**Supply Voltage (V_{CC})** The operating supply voltage range is from 1.8 Vdc to 5.0 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactances along the trace; it is best to have it completely fill around the surface mount components and traces on the circuit side of the PCB.
13 & 14 15 16	Out 1 and Out 2 Out_Gnd I_{mod}		**Differential Output** The output is configured differentially to easily drive a loop antenna. By using a transformer or balun, as shown in the application schematic, the device may then drive an unbalanced low impedance load. Figure 6 shows how much the Output Power and Free-Running Oscillator Frequency change with temperature at 3.0 Vdc; I_{mod} = 2.0 mA. **Output Ground** This additional ground pin provides direct access for the output ground to the circuit board V_{EE}. **AM Modulation/Power Output Level** The DC voltage at this pin is 0.8 Vdc with the current source active. An external resistor is chosen to provide a source current of 1.0 to 3.0 mA, depending on the desired output power level at a given V_{CC}. Figure 23 shows the relationship of Power Output to Modulation Current, I_{mod}. At V_{CC} = 3.0 Vdc, 3.5 dBm power output can be acquired with about 35 mA I_{CC}. For FM modulation, Pin 16 is used to set the desired output power level as described above. For AM modulation, the modulation signal must ride on a positive DC bias offset which sets a static (modulation off) modulation current. External circuitry for various schemes is further discussed in the Applications Information section.

Figure 3. Supply Current versus Supply Voltage

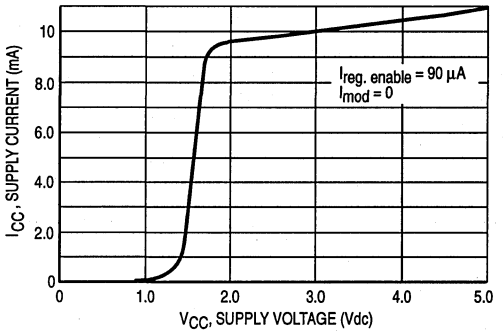


Figure 4. Supply Current versus Regulator Enable Current

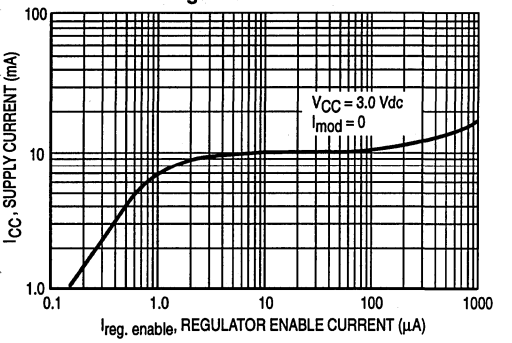


Figure 5. Change Oscillator Frequency versus Oscillator Control Current

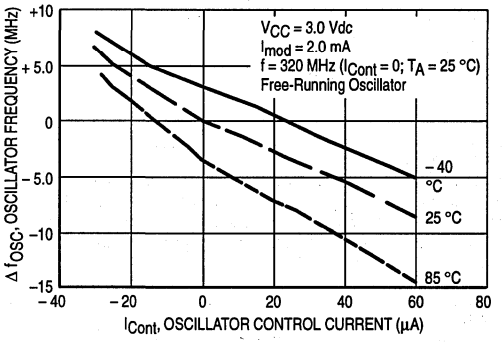


Figure 6. Change in Oscillator Frequency and Output Power versus Ambient Temperature

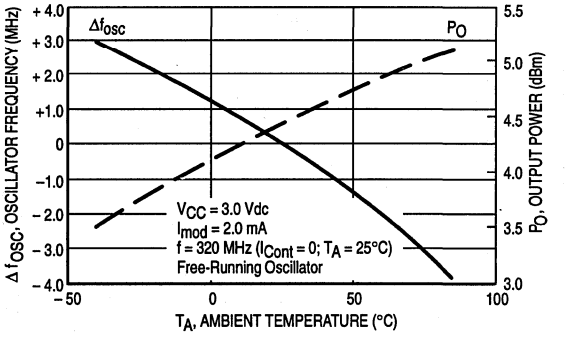


Figure 7. MC13175 Reference Oscillator Frequency versus Phase Detector Current

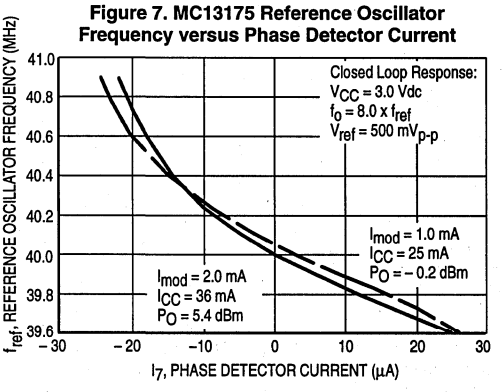


Figure 8. MC13176 Reference Oscillator Frequency versus Phase Detector Current

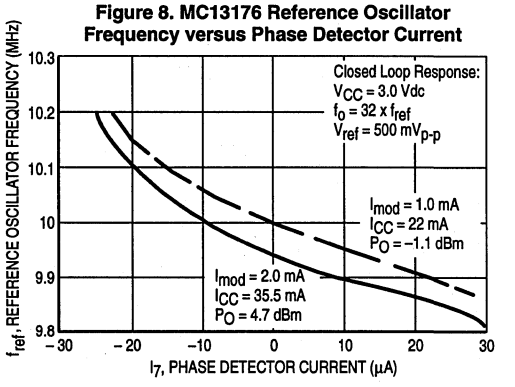


Figure 9. Change in Oscillator Frequency versus Oscillator Control Current

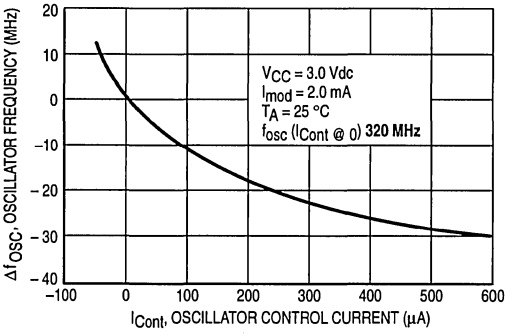
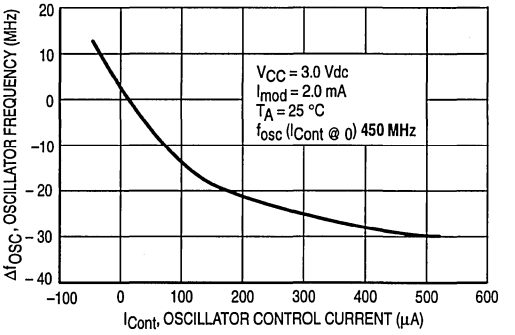


Figure 10. Change in Oscillator Frequency versus Oscillator Control Current



APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB, shown in Figures 26 and 27, is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 28 and 29). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Current Controlled Oscillator (Pins 1 to 4)

It is critical to keep the interconnect leads from the CCO (Pins 1 and 4) to the external inductor symmetrical and equal in length. With a minimum inductor the maximum free running frequency is greater than 1.0 GHz. Since this inductor will be small, it may be either a microstrip inductor, an air wound inductor or a tuneable RF coil. An air wound inductor may be tuned by spreading the windings, whereas, tuneable RF coils are tuned by adjusting the position of an aluminum core in a threaded coilform. As the aluminum core coupling to the windings is increased, the inductance is decreased. The temperature coefficient using an aluminum core is better than a ferrite core. The UniCoil™ inductors made by Coilcraft may be obtained with aluminum cores (Part No. 51-129-169).

Ground (Pins 5, 10 and 15)

Ground Returns: It is best to take the grounds to a backside ground plane via plated through holes or eyelets at the pins. The application PCB layout implements this technique. Note that the grounds are located at or less than 100 mils from the devices pins.

Decoupling: Decoupling each ground pin to V_{CC} isolates each section of the device by reducing interaction between sections and by localizing circulating currents.

Loop Characteristics (Pins 6 and 7)

Figure 11 is the component block diagram of the MC1317XD PLL system where the loop characteristics are described by the gain constants. Access to individual components of this PLL system is limited, inasmuch as the loop is only pinned out at the phase detector output and the frequency control input for the CCO. However, this allows for characterization of the gain constants of these loop components. The gain constants K_p, K_o and K_n are well defined in the MC13175 and MC13176.

Phase Detector (Pin 7)

With the loop in lock, the difference frequency output of the phase detector is DC voltage that is a function of the phase difference. The sinusoidal type detector used in this IC has the following transfer characteristic:

$$I_e = A \sin \theta_e$$

The gain factor of the phase detector, K_p (with the loop in lock) is specified as the ratio of DC output current, I_e to phase error, θ_e:

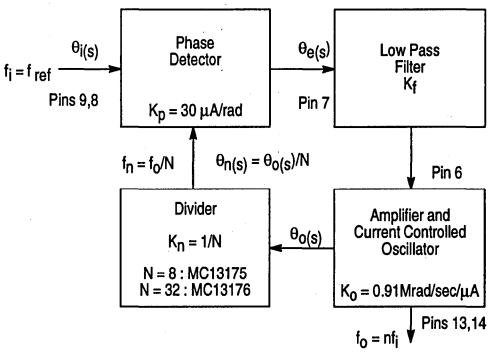
$K_p = I_e/\theta_e$ (Amps/radians)
$K_p = A \sin \theta_e/\theta_e$
$\sin \theta_e \sim \theta_e$ for $\theta_e \leq 0.2$ radians;
thus, $K_p = A$ (Amps/radians)

Figures 7 and 8 show that the detector DC current is approximately 30 μA where the loop loses lock at $\theta_e = \pm \pi/2$ radians; therefore, K_p is 30 μA/radians.

Current Controlled Oscillator, CCO (Pin 6)

Figures 9 and 10 show the non-linear change in frequency of the oscillator over an extended range of control current for 320 and 450 MHz applications. K_o ranges from approximately 6.3×10^5 rad/sec/μA or 100 kHz/μA (Figure 9) to 8.8×10^5 rad/sec/μA or 140 kHz/μA (Figure 10) over a relatively linear response of control current (0 to 100 μA). The oscillator gain factor depends on the operating range of the control current (i.e., the slope is not constant). Included in the CCO gain factor is the internal amplifier which can sink and source at least 30 μA of input current from the phase detector. The internal circuitry at Pin 6 limits the CCO control current to 50 μA of source capability while its sink capability exceeds 200 μA as shown in Figures 9 and 10. Further information to follow shows how to use the full capabilities of the CCO by addition of an external loop amplifier and filter (see Figure 15). This additional circuitry yields at $K_o = 0.145$ MHz/μA or 9.1×10^5 rad/sec/μA.

Figure 11. Block Diagram of MC1317XD PLL



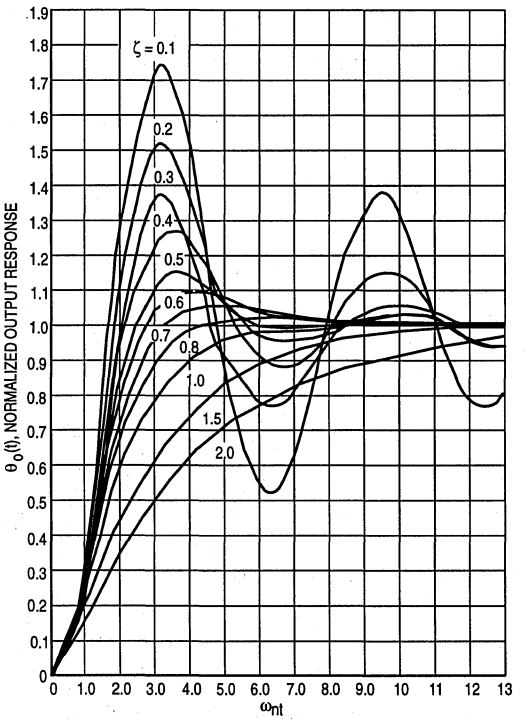
Where: K_p= Phase detector gain constant in µA/rad; K_p = 30 µA/rad
K_f = Filter transfer function
K_n= 1/N; N = 8 for the MC13175 and N = 32 for the MC13176
K_o= CCO gain constant in rad/sec/µA
K_o= 9.1 x 10^5 rad/sec/µA

Loop Filtering

The fundamental loop characteristics, such as capture range, loop bandwidth, lock-up time and transient response are controlled externally by loop filtering.

The natural frequency (ω_n) and damping factor (∂) are important in the transient response to a step input of phase or frequency. For a given ∂ and lock time, ω_n can be determined from the plot shown in Figure 12.

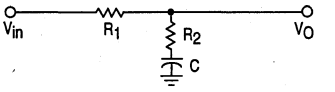
Figure 12. Type 2 Second Order Response



For ∂ = 0.707 and lock time = 1.0 ms;
then ω_n = 5.0/t = 5.0 krad/sec.

The loop filter may take the form of a simple low pass filter or a lag-lead filter which creates an additional pole at origin in the loop transfer function. This additional pole along with that of the CCO provides two pure integrators ($1/s^2$). In the lag-lead low pass network shown in Figure 13, the values of the low pass filtering parameters R_1, R_2 and C determine the loop constants ω_n and ∂. The equations $t_1 = R_1C$ and $t_2 = R_2C$ are related in the loop filter transfer functions $F(s) = 1 + t_2s/1 + (t_1 + t_2)s$.

Figure 13. Lag-Lead Low Pass Filter



The closed loop transfer function takes the form of a 2nd order low pass filter given by,

$$H(s) = K_vF(s)/s + K_vF(s)$$

From control theory, if the loop filter characteristic has F(0) = 1, the DC gain of the closed loop, K_v is defined as,

$$K_v = K_pK_oK_n$$

and the transfer function has a natural frequency,

$$\omega_n = (K_v/t_1 + t_2)^{1/2}$$

and a damping factor,

$$\partial = (\omega_n/2)\ (t_2 + 1/K_v)$$

Rewriting the above equations and solving for the MC13176 with ∂ = 0.707 and ω_n = 5.0 k rad/sec:

$$K_v = K_pK_oK_n = (30)\ (0.91 \bullet 10^6)\ (1/32) = 0.853 \bullet 10^6$$

$$t_1 + t_2 = K_v/\omega_n2 = 0.853 \bullet 10^6/(25 \bullet 106) = 34.1 \text{ ms}$$

$$t_2 = 2\partial/\omega_n = (2)\ (0.707)/(5 \bullet 10^3) = 0.283 \text{ ms}$$

$$t_1 = (K_v/\omega_n2) - t_2 = (34.1 - 0.283) = 33.8 \text{ ms}$$

For C = 0.47 μ;

then, $R_1 = t_1/C = 33.8 \bullet 10^{-3}/0.47 \bullet 10^{-6} = 72$ k

thus, $R_2 = t_2/C = 0.283 \bullet 10^{-3}/0.47 \bullet 10^{-6} = 0.60$ k

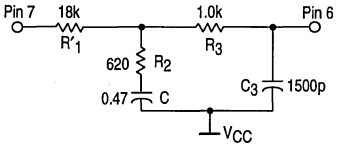
In the above example, the following standard value components are used,

$C = 0.47$ μ; $R_2 = 620$ and $R'_1 = 72$ k – 53 k ~ 18 k

(R'_1 is defined as R_1 – 53 k, the output impedance of the phase detector.)

Since the output of the phase detector is high impedance (~50 k) and serves as a current source, and the input to the frequency control, Pin 6 is low impedance (impedance of the two diode to ground is approximately 500 Ω), it is imperative that the second order low pass filter design above be modified. In order to minimize loading of the R_2C shunt network, a higher impedance must be established to Pin 6. A simple solution is achieved by adding a low pass network between the passive second order network and the input to Pin 6. This helps to minimize the loading effects on the second order low pass while further suppressing the sideband spurs of the crystal oscillator. A low pass filter with $R_3 = 1.0$ k and $C_2 = 1500$ p has a corner frequency (f_c) of 106 kHz; the reference sideband spurs are down greater than – 60 dBc.

Figure 14. Modified Low Pass Loop Filter



Hold-In Range

The hold-in range, also called the lock range, tracking range and synchronization range, is the ability of the CCO frequency, f_o to track the input reference signal, $f_{ref} \bullet N$ as it gradually shifted away from the free running frequency, f_f. Assuming that the CCO is capable of sufficient frequency deviation and that the internal loop amplifier and filter are not overdriven, the CCO will track until the phase error, θ_e approaches $\pm\pi/2$ radians. Figures 5 through 8 are a direct measurement of the hold-in range (i.e. $\Delta f_{ref} \bullet N = \pm\Delta f_H \bullet 2\pi$).

Since $\sin\theta_e$ cannot exceed ±1.0, as θ_e approaches $\pm\pi/2$ the hold-in range is equal to the DC loop gain, $K_V \bullet N$.

$$\pm\Delta\omega_H = \pm K_V \bullet N$$

where, $K_V = K_p K_o K_n$.

In the above example,

$$\pm\Delta\omega_H = \pm 27.3 \text{ Mrad/sec}$$

$$\pm\Delta f_H = \pm 4.35 \text{ MHz}$$

Extended Hold-in Range

The hold-in range of about 3.4% could cause problems over temperature in cases where the free-running oscillator drifts more than 2 to 3% because of relatively high temperature coefficients of the ferrite tuned CCO inductor. This problem might worsen for lower frequency applications where the external tuning coil is large compared to internal capacitance at Pins 1 and 4. To improve hold-in range performance, it is apparent that the gain factors involved must be carefully considered.

K_n = is either 1/8 in the MC13175 or 1/32 in the MC13176.

K_p = is fixed internally and cannot be altered.

K_o = Figures 9 and 10 suggest that there is capability of greater control range with more current swing. However, this swing must be symmetrical about the center of the dynamic response. The suggested zero current operating point for ±100 μA swing of the CCO is at about + 70 μA offset point.

Ka = External loop amplification will be necessary since the phase detector only supplies ± 30 μA.

In the design example in Figure 15, an external resistor (R_5) of 15 k to V_{CC} (3.0 Vdc) provides approximately 100 μA of current boost to supplement the existing 50 μA internal source current. R_4 (1.0 k) is selected for approximately 0.1 Vdc across it with 100 μA. R_1, R_2 and R_3 are selected to set the potential at Pin 7 and the base of 2N4402 at approximately 0.9 Vdc and the emitter at 1.55 Vdc when error current to Pin 6 is approximately zero μA. C_1 is chosen to reduce the level of the crystal sidebands.

Figure 15. External Loop Amplifier

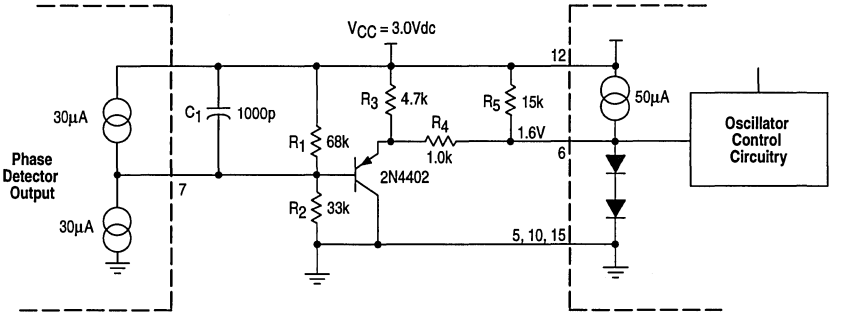
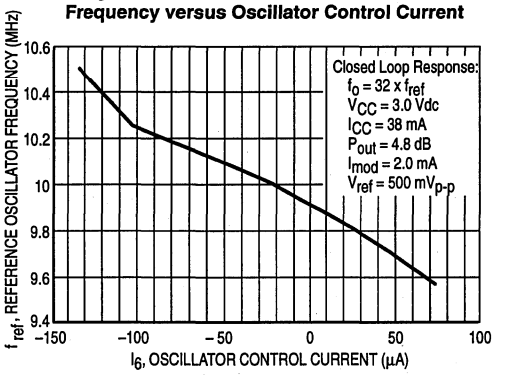


Figure 16 shows the improved hold-in range of the loop. The Δf_{ref} is moved 950 kHz with over 200 μA swing of control current for an improved hold-in range of ±15.2 MHz or ± 95.46 Mrad/sec.

Figure 16. MC13176 Reference Oscillator Frequency versus Oscillator Control Current



Lock-in Range/Capture Range

If a signal is applied to the loop not equal to free running frequency, f_f, then the loop will capture or lock-in the signal by making $f_S = f_O$ (i.e. if the initial frequency difference is not too great). The lock-in range can be expressed as $\Delta\omega_L \sim \pm 2\partial\omega_n$

FM Modulation

Noise external to the loop (phase detector input) is minimized by narrowing the bandwidth. This noise is minimal in a PLL system since the reference frequency is usually derived from a crystal oscillator. FM can be achieved by applying a modulation current superimposed on the control current of the CCO. The loop bandwidth must be narrow enough to prevent the loop from responding to the modulation frequency components, thus, allowing the CCO to deviate in frequency. The loop bandwidth is related to the natural frequency ω_n. In the lag-lead design example where the natural frequency, ω_n = 5.0 krad/sec and a damping factor, ∂ = 0.707, the loop bandwidth = 1.64 kHz. Characterization data of the closed loop responses for both the MC13175 and MC13176 at 320 MHz (Figures 7 and 8, respectively) show satisfactory performance using only a simple low-pass loop filter network. The loop filter response is strongly influenced by the high output impedance of the push-pull current output of the phase detector.

$f_C = 0.159/RC;$

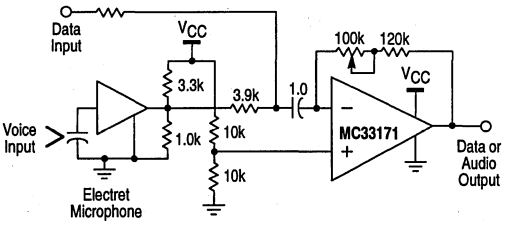
For R = 1.0 k + R_7 (R_7 = 53 k) and C = 390 pF

f_C = 7.55 kHz or ω_C = 47 krad/sec

The application example in Figure 17a of a 320 MHz FM transmitter demonstrates the FM capabilities of the IC. A high value series resistor (100 k) to Pin 6 sets up the current source to drive the modulation section of the chip. Its value is dependent on the peak to peak level of the encoding data and the maximum desired frequency deviation. The data input is AC coupled with a large coupling capacitor which is selected for the modulating frequency. The component placements on the circuit side and ground side of the PC board are shown in Figures 28 and 29, respectively. Figure 18a illustrates the input data of a 10 kHz modulating signal at 1.6 Vp-p. Figures 18b and 18c depict the deviation and resulting modulation spectrum showing the carrier null at – 40 dBc. Figure 18d shows the unmodulated carrier power output at 3.5 dBm for V_{CC} = 3.0 Vdc.

For voice applications using a dynamic or an electret microphone, an op amp is used to amplify the microphone's low level output. The microphone amplifier circuit is shown in Figure 19. Figure 17b shows an application example for NBFM audio or direct FSK in which the reference crystal oscillator is modulated.

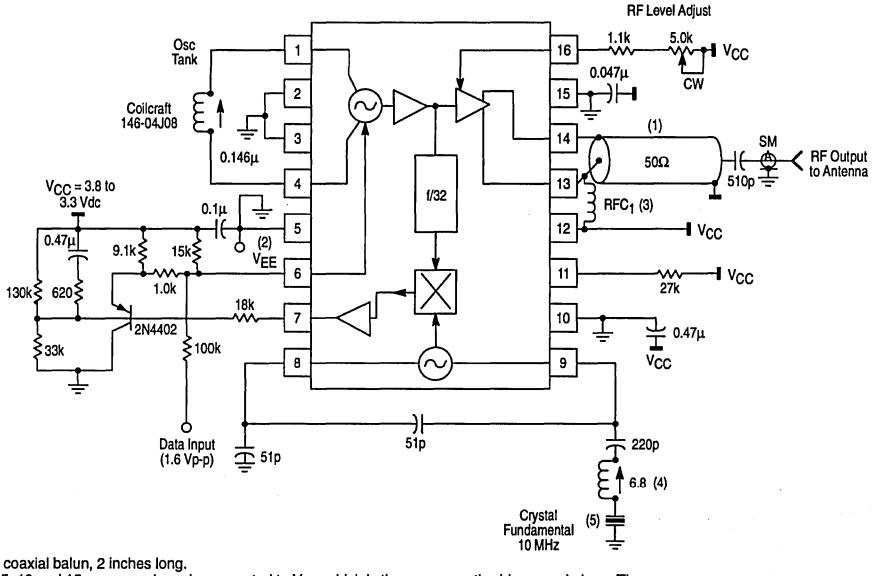
Figure 19. Microphone Amplifier



Local Oscillator Application

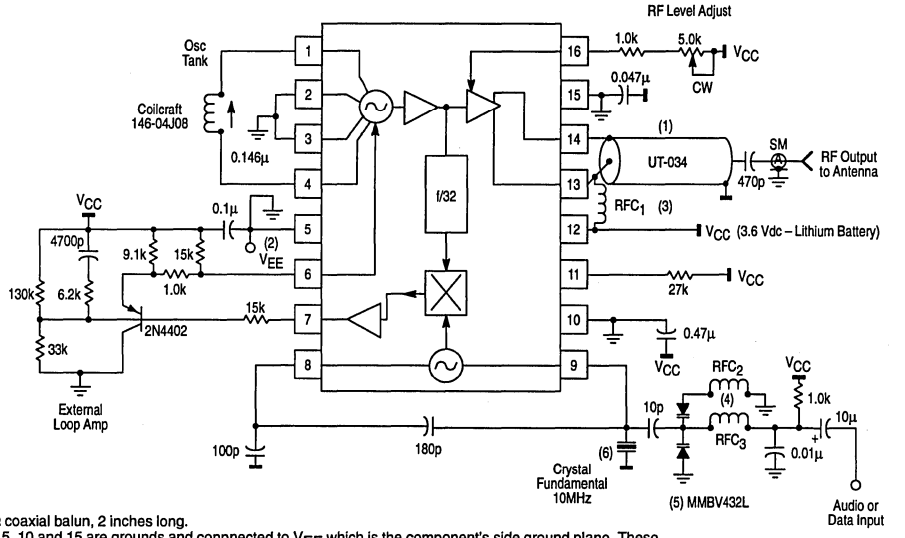
To reduce internal loop noise, a relatively wide loop bandwidth is needed so that the loop tracks out or cancels the noise. This is emphasized to reduce inherent CCO and divider noise or noise produced by mechanical shock and environmental vibrations. In a local oscillator application the CCO and divider noise should be reduced by proper selection of the natural frequency of the loop. Additional low pass filtering of the output will likely be necessary to reduce the crystal sideband spurs to a minimal level.

Figure 17a. 320 MHz MC13176D FM Transmitter



NOTES: 1. 50 Ω coaxial balun, 2 inches long.
2. Pins 5, 10 and 15 are grounds and connnected to V_{EE} which is the component's side ground plane. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. RFC_1 is 180 nH Coilcraft surface mount inductor or 190 nH Coilcraft 146-05J08.
4. Recommended source is a Coilcraft "slot seven" 7.0 mm tuneable inductor, part #7M3-682.
5. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

Figure 17b. 320 MHz NBFM Transmitter



NOTES: 1. 50 Ω coaxial balun, 2 inches long.
2. Pins 5, 10 and 15 are grounds and connnected to V_{EE} which is the component's side ground plane. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. RFC_1 is 180 nH Coilcraft surface mount inductor.
4. RFC_2 and RFC_3 are high impedance crystal frequency of 10 MHz; 8.2 µH molded inductor gives XL > 1000 Ω.
5. A single varactor like the MV2105 may be used whereby RFC_2 is not needed.
6. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

Figure 18a. Input Data Waveform

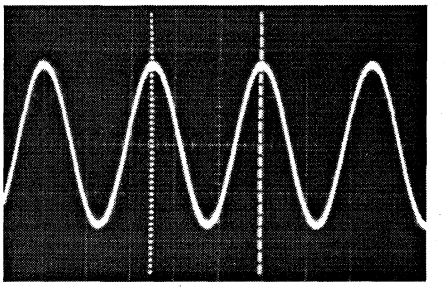


Figure 18b. Frequency Deviation

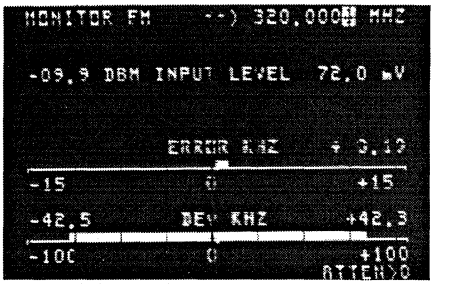


Figure 18c. Modulation Spectrum

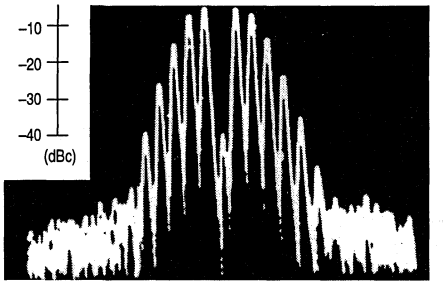
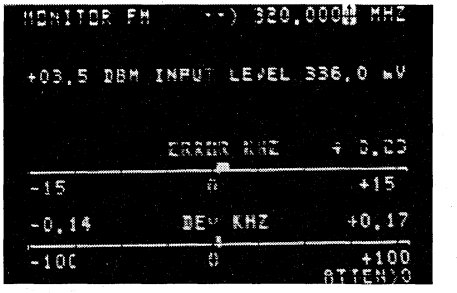


Figure 18d. Unmodulated Carrier



Reference Crystal Oscillator (Pins 8 and 9)

Selection of Proper Crystal: A crystal can operate in a number of mechanical modes. The lowest resonant frequency mode is its fundamental while higher order modes are called overtones. At each mechanical resonance, a crystal behaves like a RLC series-tuned circuit having a large inductor and a high Q. The inductor L_S is series resonance with a dynamic capacitor, C_S determined by the elasticity of the crystal lattice and a series resistance R_S, which accounts for the power dissipated in heating the crystal. This series RLC circuit is in parallel with a static capacitance, C_p which is created by the crystal block and by the metal plates and leads that make contact with it.

Figure 20 is the equivalent circuit for a crystal in a single resonant mode. It is assumed that other modes of resonance are so far off frequency that their effects are negligible.

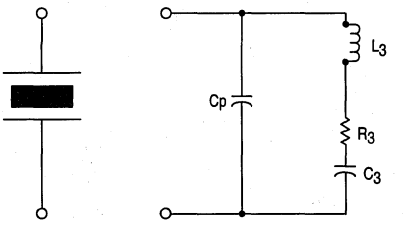
Series resonant frequency, f_S is given by;

$$f_S = 1/2\pi(L_S C_S)^{1/2}$$

and parallel resonant frequency, f_p is given by;

$$f_p = f_S(1 + C_S/C_p)^{1/2}$$

Figure 20. Crystal Equivalent Circuit



the frequency separation at resonance is given by;

$$\Delta f = f_p - f_S = f_S[1 - (1 + C_S/C_p)^{1/2}]$$

Usually f_p is less than 1% higher than f_S, and a crystal exhibits an extremely wide variation of the reactance with frequency between f_p and f_S. A crystal oscillator circuit is very stable with frequency. This high rate of change of impedance with frequency stabilizes the oscillator, because any significant change in os-

cillator frequency will cause a large phase shift in the feedback loop keeping the oscillator on frequency.

Manufacturers specify crystal for either series or parallel resonant operation. The frequency for the parallel mode is calibrated with a specified shunt capacitance called a "load capacitance". The most common value is 30 to 32 pF. If the load capacitance is placed in series with the crystal, the equivalent circuit will be series resonance at the specified parallel-resonant frequency. Frequencies up to 20 MHz use parallel resonant crystal operating in the fundamental mode, while above 20 MHz to about 60 MHz, a series resonant crystal specified and calibrated for operation in the overtone mode is used.

Application Examples

Two types of crystal oscillator circuits are used in the applications circuits: 1) Fundamental mode common emitter Colpitts (Figures 1, 17a, 17b, and 21). 2) Third overtone impedance inversion Colpitts (also Figures 1 and 21).

The fundamental mode common emitter Colpitts uses a parallel resonant crystal calibrated with a 32 pf load capacitance. The capacitance values are chosen to provide excellent frequency stability and output power of > 500 mVp-p at Pin 9. In Figures 1 and 21, the fundamental mode reference oscillator is fixed tuned relying on the repeatability of the crystal and passive network to maintain the frequency, while in the circuit shown in Figure 17, the oscillator frequency can be adjusted with the variable inductor for the precise operating frequency.

The third overtone impedance inversion Colpitts uses a series resonance crystal with a 25 ppm tolerance. In the application examples (Figures 1 and 21), the reference oscillator operates with the third overtone crystal at 40.0000 MHz. Thus, the MC13175 is operated at 320 MHz ($f_O/8$ = crystal; 320/8 = 40.0000 MHz. The resistor across the crystal ensures that the crystal will operate in the series resonant mode. A tuneable inductor is used to adjust the oscillation frequency; it forms a parallel resonant circuit with the series and parallel combination of the external capacitors forming the divider and feedback network and the base-emitter capacitance of the device. If the crystal is shorted, the reference oscillator should free-run at the frequency dictated by the parallel resonant LC network.

The reference oscillator can be operated as high as 60 MHz with a third overtone crystal. Therefore, it is possible to use the MC13175 up to at least 480 MHz and the MC13176 up to 950 MHz (based on the maximum capability of the divider network).

Enable (Pin 11)

The enabling resistor at Pin 11 is calculated by:

$$R_{reg.\ enable} = V_{CC} - 1.0\ Vdc / I_{reg.\ enable}$$

From Figure 4, $I_{reg.\ enable}$ is chosen to be 75 µA. So, for a V_{CC} = 3.0 Vdc $R_{reg.\ enable}$ = 26.6 kΩ, a standard value 27 kΩ resistor is adequate.

Layout Considerations

Supply (Pin 12): In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactance along the trace; it is best that V_{CC} (RF ground) completely fills around the surface mounted components and interconnect traces on the circuit side of the board. This technique is demonstrated in the evaluation PC board.

Battery/Selection/Lithium Types

The device may be operated from a 3.0 V lithium battery. Selection of a suitable battery is important. Because one of the major problems for long life battery powered equipment is oxidation of the battery terminals, a battery mounted in a clip-in socket is not advised. The battery leads or contact post should be isolated from the air to eliminate oxide build-up. The battery should have PC board mounting tabs which can be soldered to the PCB. Consideration should be given for the peak current capability of the battery. Lithium batteries have current handling capabilities based on the composition of the lithium compound, construction and the battery size. A 1300 mA/hr rating can be achieved in the cylindrical cell battery. The Rayovac CR2/3A lithium-manganese dioxide battery is a crimp sealed, spiral wound 3.0 Vdc, 1300 mA/hr cylindrical cell with PC board mounting tabs. It is an excellent choice based on capacity and size (1.358″ long by 0.665″ in diameter).

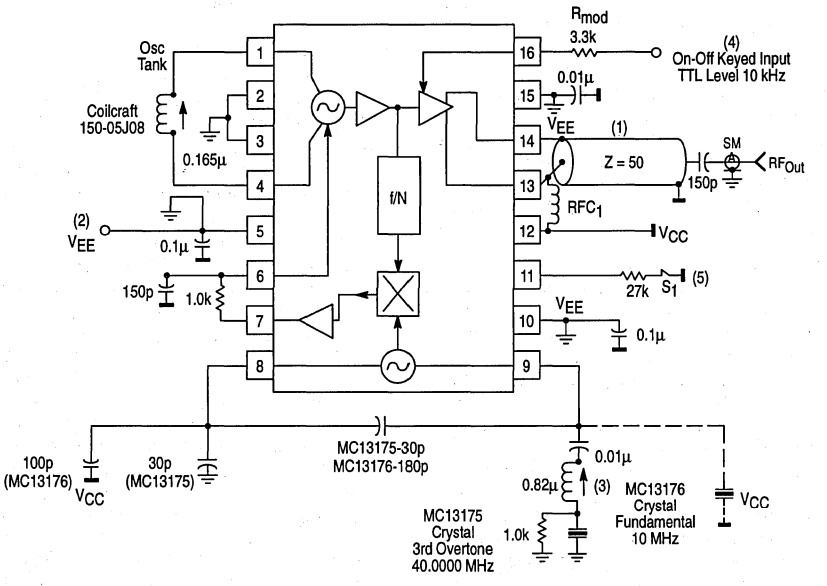
Differential Output (Pins 13, 14)

The availability of micro-coaxial cable and small baluns in surface mount and radial-leaded components allows for simple interface to the output ports. A loop antenna may be directly connected with bias via RFC or 50 Ω resistors. Antenna configuration will vary depending on the space available and the frequency of operation.

AM Modulation (Pin 16)

Amplitude Shift Key: The MC13175 and MC13176 are designed to accommodate Amplitude Shift Keying (ASK). ASK modulation is a form of digital modulation corresponding to AM. The amplitude of the carrier is switched between two or more values in response to the PCM code. For the binary case, the usual choice is On-Off Keying (often abbreviated OOK). The resultant amplitude modulated waveform consists of RF pulses called marks, representing binary 1 and spaces representing binary 0.

Figure 21. ASK 320 MHz Application Circuit



NOTES: 1. 50 Ω coaxial balun, 1/10 wavelength line (1.5″) provides the best match to a 50 Ω load.

2. Pins 5, 10 and 15 are ground and connnected to V_{EE} which is the component/DC ground plane side of PCB. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.

3. The crystal oscillator circuit may be adjusted for frequency with the variable inductor (MC13175); 1.0 k resistor shunting the crystal prevents it from oscillating in the fundamental mode. Recommended source is Coilcraft "slot seven" 7.0 mm tuneable inductor, part #7M3-821.

4. The On-Off keyed signal turns the output of the transmitter off and on with TTL level pulses through R_{mod} at Pin 16. The "On" power and I_{CC} is set by the resistor which sets $I_{mod} = VTTL - 0.8 / R_{mod}$. (see Figure 23).

5. S1 simulates an enable gate pulse from a microprocessor which will enable the transmitter. (see Figure 4 to determine precise value of the enabling resistor based on the potential of the gate pulse and the desired enable.)

Figure 21 shows a typical application in which the output power has been reduced for linearity and current drain. The current draw on the device is 16 mA I_{CC} (average) and – 22.5 dBm (average power output) using a 10 kHz modulating rate for the on-off keying. This equates to 20 mA and – 2.3 dBm "On", 13 mA and – 41 dBm "Off". In Figure 22a, the device's modulating waveform and encoded carrier are displayed. The crystal oscillator enable time is needed to set the acquisition timing. It takes typically 4.0 msec to reach full magnitude of the oscillator waveform (see Figure 22b, Oscillator Waveform, at Pin 8). A square waveform of 3.0 V peak with a period that is greater than the oscillator enable time is applied to the Enable (Pin 11).

Figure 22a. ASK Input Waveform and Modulated Carrier

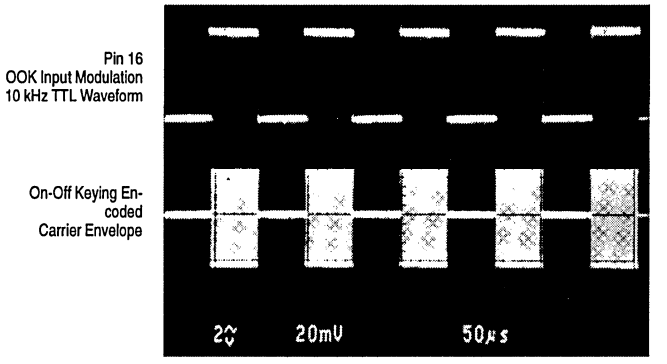


Figure 22b. Oscillator Enable Time, T_{enable}

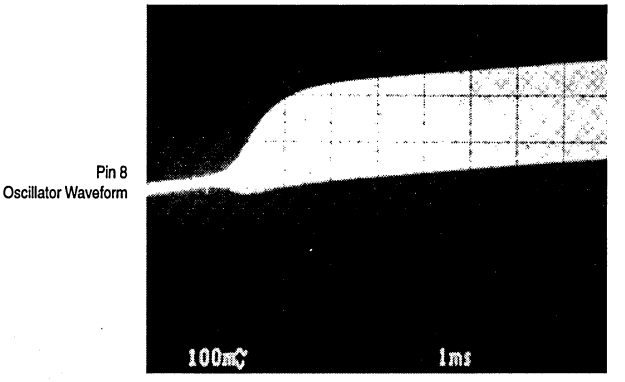
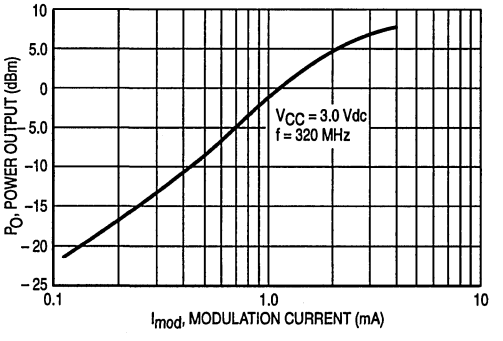


Figure 23. Power Output versus Modulation Current



Analog AM

In analog AM applications, the output amplifier's linearity must be carefully considered. Figure 23 is a plot of Power Output versus Modulation Current at 320 MHz, 3.0 Vdc. In order to achieve a linear encoding of the modulating sinusoidal waveform on the carrier, the modulating signal must amplitude modulate the carrier in the linear portion of its power output response. When using a sinewave modulating signal, the signal rides on a positive DC offset called V_{mod} which sets a static (modulation off) modulation current, I_{mod}. I_{mod} controls the power output of the IC. As the modulating signal moves around this static bias point the modulating current varies causing power output to vary or to be AM modulated. When the IC is operated at modulation current levels greater than 2.0 mAdc the differential output stage starts to saturate.

In the design example, shown in Figure 24, the operating point is selected as a tradeoff between average power output and quality of the AM.

For V_{CC} = 3.0 Vdc; I_{CC} = 18.5 mA and I_{mod} = 0.5 mAdc and a static DC offset of 1.04 Vdc, the circuit shown in Figure 24 completes the design. Figures 25a, 25b and 25c show the results of – 6.9 dBm output power and 100% modulation by the 10 kHz and 1.0 MHz modulating sinewave signals. The amplitude of the input signals is approximately 800 mVp-p.

Where R_{mod} = (V_{CC} – 1.04 Vdc)/0.5 mA = 3.92 k, use a standard value resistor of 3.9 k.

Figure 24. Analog AM Transmitter

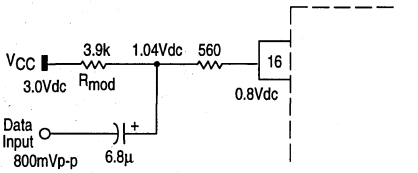


Figure 25a. Power Output of Unmodulated Carrier

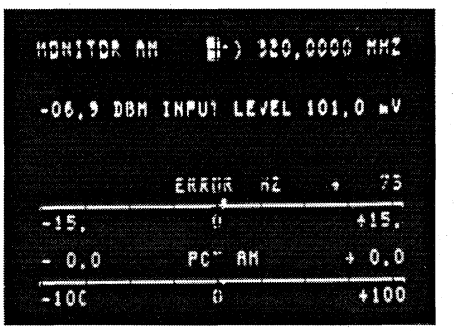


Figure 25b. Input Signal and AM Modulated Carrier for f_{mod} = 10 kHz

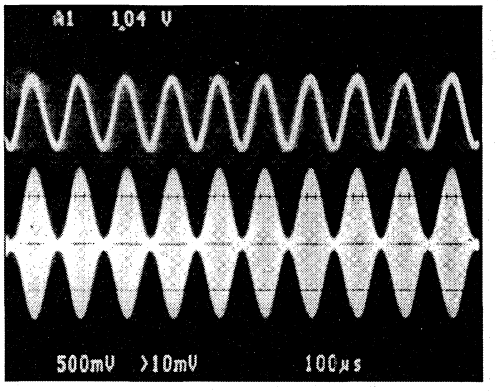


Figure 25c. Input Signal and AM Modulated Carrier for f_{mod} = 1.0 MHz

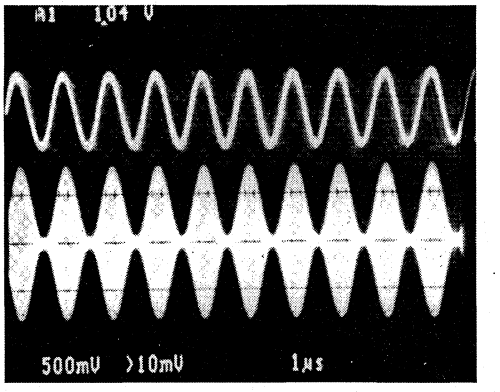


Figure 26. Circuit Side View of MC1317XD

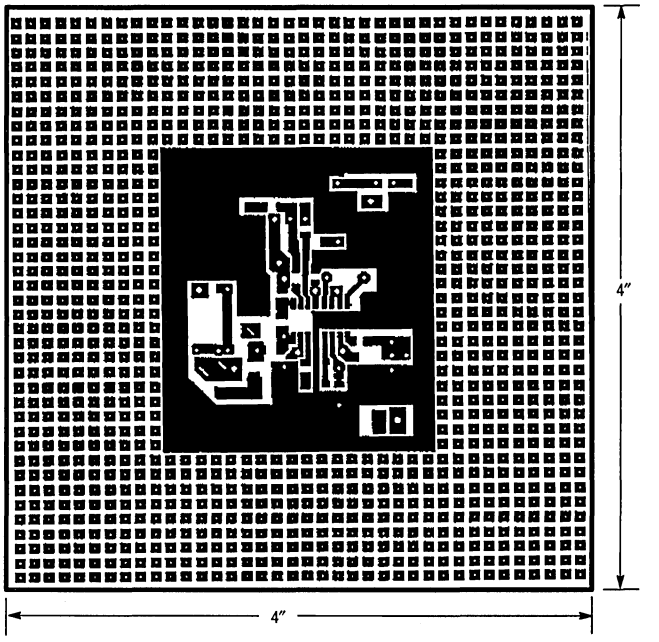


Figure 27. Ground Side View

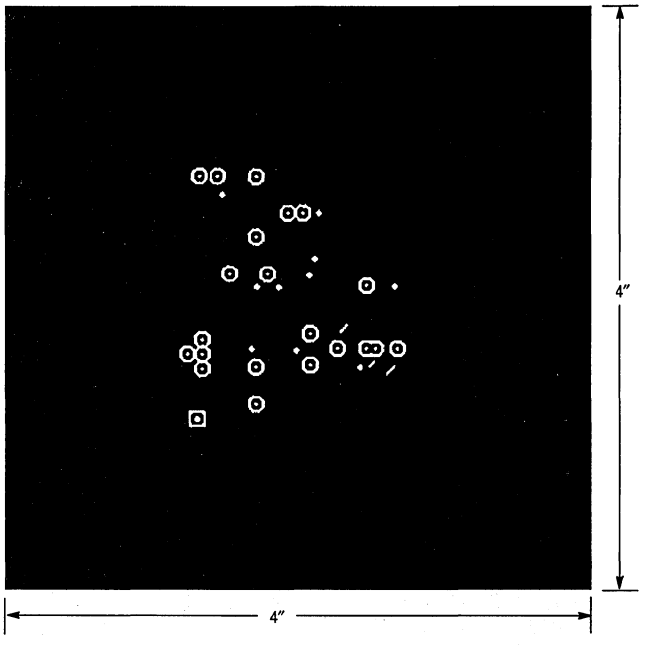
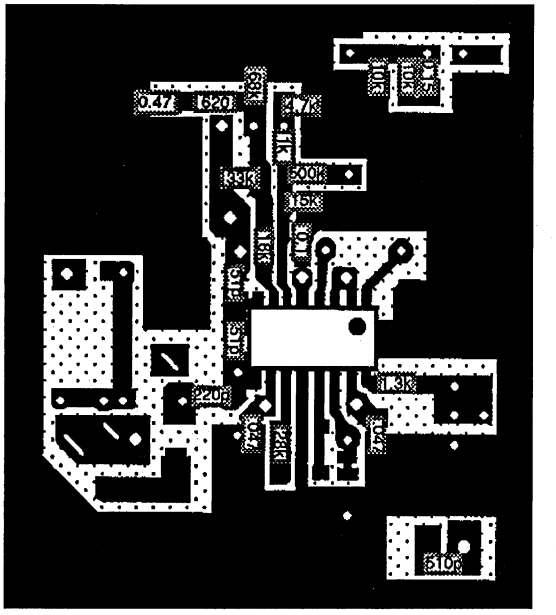


Figure 28. Surface Mounted Components Placement (on Circuit Side)


0.47
620
47K
1K
500K
15K
100K
10K
1.3K
220
6.8K
5.6K
6.8K
6.8K
6.8

MC14411

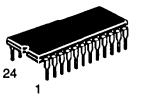
Bit Rate Generator

The MC14411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

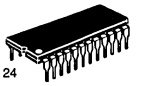
A crystal-controlled oscillator is the clock source for the network. A 2-bit address is provided to select one of four multiple output clock rates.

Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

- Single 5.0 Vdc (±5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (1.8432 MHz)
- 16 Different Output Clock Rates
- 50% Output Duty Cycle
- Programmable Time Bases for One of Four Multiple Output Rates
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock may be Applied to Pin 21
- Internal Pull-Up Resistor on Reset Input



L SUFFIX
CERAMIC
CASE 623

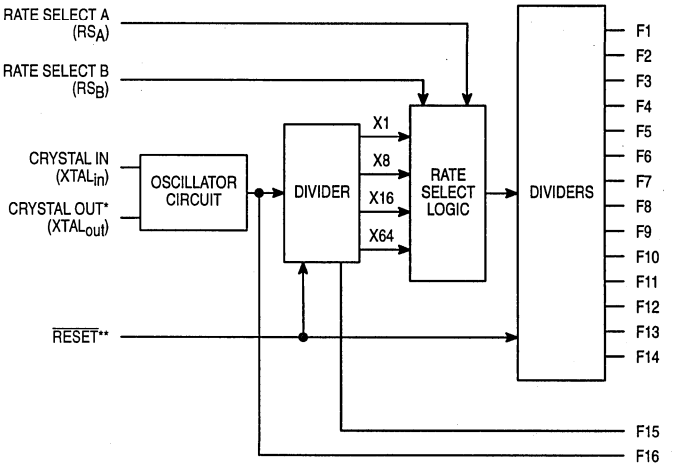


P SUFFIX
PLASTIC
CASE 709

DW SUFFIX
SOG
CASE 751E

NOT
RECOMMENDED
FOR NEW DESIGN

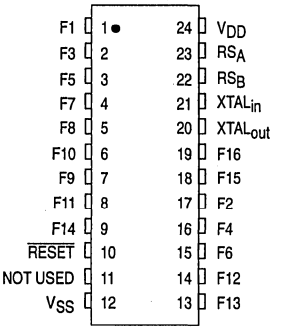
BLOCK DIAGRAM



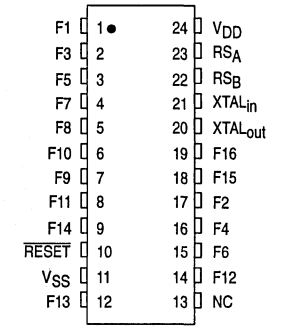
*See Figure 2 for typical crystal oscillator circuits.
**When $\overline{RESET}$ = 0, outputs F1–F14 = 0, outputs F15–F16 = 1.

PIN ASSIGNMENTS

L, P SUFFIX



DW SUFFIX



NC = NO CONNECTION

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12)

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage Range	5.25 to −0.5	V
V_{in}	Input Voltage, All Inputs	V_{DD} + 0.5 to V_{SS} − 0.5	V
I	DC Current Drain per Pin	10	mA
T_A	Operating Temperature Range	− 40 to + 85	°C
T_{stg}	Storage Temperature Range	− 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Symbol	Characteristic		V_{DD}	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
V_{DD}	Supply Voltage		—	4.75	5.25	4.75	5.0	5.25	4.75	5.25	V
V_{out}	Operating Voltage	"0" Level	5.0	—	0.05	—	0	0.05	—	0.05	V
		"1" Level	5.0	4.95	—	4.95	5.0	—	4.95	—	V
V_{IL}	Input Voltage	V_O = 4.5 or 0.5 V	5.0	—	1.5	—	2.25	1.5	—	1.5	V
V_{IH}		V_O = 0.5 or 4.5 Vdc	5.0	3.5	—	3.5	2.75	—	3.5	—	V
	Output Drive Current										
I_{OH}	V_{OH} = 2.5 V	Source	5.0	−0.23	—	−0.20	−1.7	—	−0.16	—	mA
I_{OL}	V_{OL} = 0.4 V	Sink	5.0	+0.23	—	+0.20	+0.78	—	+0.16	—	mA
I_{in}	Input Current	Pins 21, 22, 23	—	—	±0.1	—	±0.00001	±0.1	—	±1.0	µA
		Pin 10	5.0	—	—	−1.5	—	−7.5	—	—	µA
C_{in}	Input Capacitance (V_{in} = 0)		—	—	—	—	5.0	—	—	—	pF
P_Q	Quiescent Dissipation		5.0	—	2.5	—	0.015	2.5	—	15	mW
P_D	Power Dissipation **† (Dynamic plus Quiescent) (C_L = 15 pF)		5.0			$P_D = (7.5\ mW/MHZ)\ f + P_Q$					mW
t_{TLH}	Output Rise Time** $t_r = (3.0\ ns/pF)\ C_L + 25\ ns$		5.0	—	—	—	70	200	—	—	ns
t_{THL}	Output Fall Time** $t_f = (1.5\ ns/pF)\ C_L + 47\ ns$		5.0	—	—	—	70	200	—	—	ns
f_{CL}	Input Clock Frequency		5.0	—	1.85	—	—	1.85	—	1.85	MHz
$t_{W(C)}$	Clock Pulse Width		—	200	—	200	—	—	200	—	ns
$t_{W(R)}$	$\overline{RESET}$ Pulse Width		—	500	—	500	—	—	500	—	ns

† For dissipation at different external capacitance (C_L) refer to corresponding formula:
$P_T\ (C_L = P_D + 2.6 \times 10^{-3}\ (C_L - 15\ pF)\ V_{DD}{}^2 f$
where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

** The formula given is for the typical characteristics only.

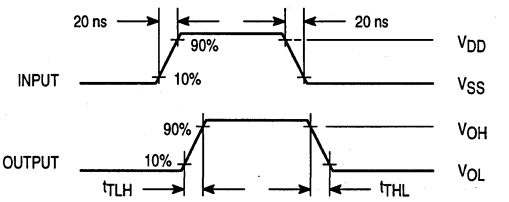


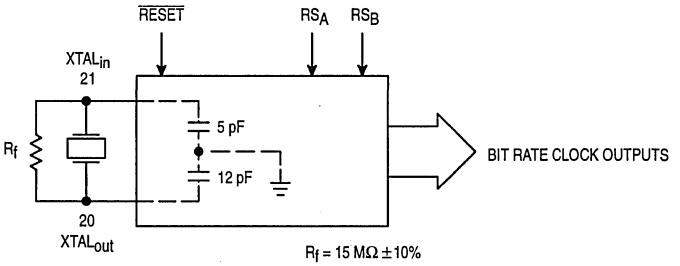
Figure 1. Dynamic Signal Waveforms

Table 1. Output Clock Rates

Rate Select		
B	A	Rate
0	0	X1
0	1	X8
1	0	X16
1	1	X64

Output Number	Output Rates (Hz)			
	X64	X16	X8	X1
F1	614.4 k	153.6 k	76.8 k	9600
F2	460.8 k	115.2 k	57.6 k	7200
F3	307.2 k	76.8 k	38.4 k	4800
F4	230.4 k	57.6 k	28.8 k	3600
F5	153.6 k	38.4 k	19.2 k	2400
F6	115.2 k	28.8 k	14.4 k	1800
F7	76.8 k	19.2 k	9600	1200
F8	38.4 k	9600	4800	600
F9	19.2 k	4800	2400	300
F10	12.8 k	3200	1600	200
F11	9600	2400	1200	150
F12	8613.2	2153.3	1076.6	134.5
F13	7035.5	1758.8	879.4	109.9
F14	4800	1200	600	75
F15	921.6 k	921.6 k	921.6 k	921.6 k
F16*	1.843 M	1.843 M	1.843 M	1.843 M

*F16 is a buffered oscillator output



Crystal Specifications	Crystal Mode
Parallel	Frequency 1.8432 MHz or ±0.05% @ 13 pF
R_S	540 Ω max
C_O	7.0 pF max
Temperature Range	0 to 70°C
Test Level	1 mW
Test Set	TS — 330/TSM or Equivalent

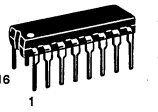
*Suggested Crystal Suppliers: Typco, CTS Knights

Figure 2. Typical Crystal Oscillator Circuit

MC14419

2-of-8 Keypad-to-Binary Tone Encoder

CMOS



P SUFFIX
PLASTIC
CASE 648

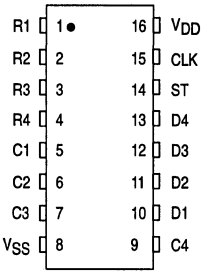
The MC14419 is designed for phone and dialer system applications, but finds many applications as a keypad-to-binary encoder. The device contains a 2-of-8 to binary encoder, a strobe generator, and an illegal state detector. The encoder has four row inputs and four column inputs and is designed to accept inputs from 16 keyswitches arranged in a 4 × 4 matrix. For an output on the four data lines, one and only one row along with one and only one column input line must be activated. All other combinations are suppressed by the illegal state detector to eliminate false data output.

The strobe generator produces a strobe pulse when any of the 10 keys corresponding to numerals 0–9 are depressed. The strobe output can be used to eliminate erroneous data entry due to contact bounce. For a strobe output to occur, the key row and column input lines must remain stable for 80 clock pulses after activation. When the contact bouncer has settled and 80 clock pulses have occurred, the output will be a single strobe pulse equal in width to that of the clock low state. The strobe generator will output one and only one pulse each time a numerical key is depressed. After the pulse has occurred, noise and bounce due to contact break will not cause another strobe pulse. With a 16 kHz clock frequency, the pulse occurs 5 ms after the last bounce.

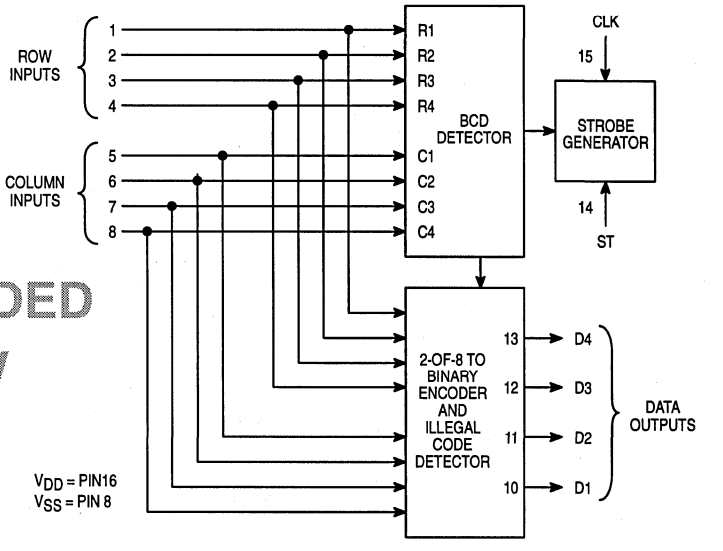
- Suppressed Output for Illegal Input Codes
- On-Chip Pull-Up Resistors for Row and Column Inputs
- Clock Input Conditioning Circuit
- Low Current Drain in Standby Mode: 5.0 μA Typical @ 5.0 Vdc
- Subsystem Complement to the MC14408/14409 Phone Pulse Converter
- Codes for Numbers 0–9 Produce a Strobe Pulse
- One Key Roll-Over Feature

PIN ASSIGNMENTS

P SUFFIX



BLOCK DIAGRAM



NOT RECOMMENDED FOR NEW DESIGN

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	+6.0 to −0.5	V
Input Voltage, All Inputs	V_{in}	V_{DD} + 0.5 to V_{SS} − 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} V dc	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Supply Voltage	V_{DD}	—	3.0	6.0	3.0	5.0	6.0	3.0	6.0	V
Operating Voltage "0" Level	V_{out}	5.0	—	0.01	—	0	0.01	—	0.05	V
Operating Voltage "1" Level		5.0	4.99	—	4.99	5.0	—	4.95	—	V
Noise Immunity	V_{NL}	5.0	1.5	—	1.5	2.25	—	1.4	—	Vdc
($\Delta V_{out} \le 0.8$ Vdc)	V_{NH}	5.0	1.4	—	1.5	2.25	—	1.5	—	Vdc
Output Drive Current V_{OH} = 2.5 V Source	I_{OH}	5.0	−0.23	—	−0.20	−1.7	—	−0.16	—	mAdc
V_{OL} = 0.4 V Sink	I_{OL}	5.0	+0.23	—	+0.20	+0.78	—	+0.16	—	mAdc
Input Leakage Current ($V_{in} = V_{DD}$)	I_{IH}	5.0	—	—	—	10	—	—	—	pAdc
Pull-Up Resistor Source Current (Row and Column Inputs) ($V_{in} = V_{SS}$)	I_{IL}	5.0	265	460	190	250	330	125	215	µAdc
Input Capacitance ($V_{in} = V_{SS}$)	C_{in}	—	—	—	—	5.0	—	—	—	pF
Standby Supply Current (f_{clock} = 16 kHz, No Keys Depressed)	I_{DDS}	3.0	—	3.0	—	1.0	3.0	—	6.0	µAdc
		5.0	—	15	—	5.0	15	—	30	
		6.0	—	60	—	20	60	—	120	
Function of Clock Frequency* (No Keys Depressed)		5.0	I_{DDS} = 0.09 µA / kHz + 3.0 µA							µAdc

* The formula given is for the typical characteristics only.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise and Fall Times, D1–D4 (Figure 1)	t_r, t_f	5.0	—	300	—	ns
Propagation Delay Time, Row or Column Input to Data Output (Figure 1)	t_{PLH}, t_{PHL}	5.0	—	1000	—	ns
Clock Pulse Frequency Range	PRF	3.0 to 6.0	4.0	16	80	kHz

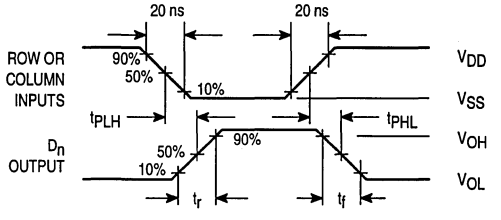


Figure 1. Switching Time Waveforms

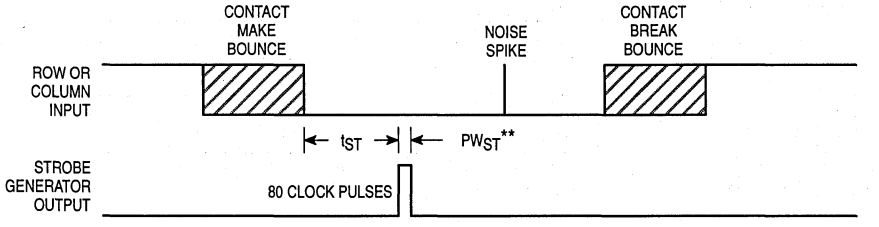
PRF Clock Frequency (kHz)	t_{ST}* Strobe Pulse Delay Time (ms)
4.0	20
8.0	10
16	5.0
32	2.5
80	1.0

*$t_{ST} = (1/PRF) \cdot 80$, with PRF in kHz, t_{ST} in ms

Table 2. Truth Table

Key**	Inputs								Outputs				
	Row				Column								
	R4	R3	R2	R1	C4	C3	C2	C1	D4	D3	D2	D1	Strobe
1	1	1	1	0	1	1	1	0	0	0	0	1	
2	1	1	1	0	1	1	0	1	0	0	1	0	
3	1	1	1	0	1	0	1	1	0	0	1	1	
A	1	1	1	0	0	1	1	1	1	1	0	0	0
4	1	1	0	1	1	1	1	0	0	1	0	0	
5	1	1	0	1	1	0	0	1	0	1	0	1	
6	1	1	0	1	1	1	1	1	0	1	1	0	
B	1	1	0	1	0	1	1	1	1	1	0	1	0
7	1	0	1	1	1	0	1	0	0	1	1	1	
8	1	0	1	1	1	1	0	1	1	0	0	0	
9	1	0	1	1	1	1	1	1	1	0	0	1	
C	1	0	1	1	0	0	1	1	1	1	1	0	0
*	0	1	1	1	1	1	1	0	1	0	1	0	0
0	0	1	1	1	1	1	0	1	0	0	0	0	
#	0	1	1	1	1	0	1	1	1	0	1	1	0
D	0	1	1	1	0	1	1	1	1	1	1	1	0
	All Other Combinations								0	0	0	0	0

**See Figure 3 for keypad designation.



**PW_{ST} = Strobe Pulse Width = Low State Clock Pulse Width (PW_L).

Figure 2. Strobe Generator Timing Diagram

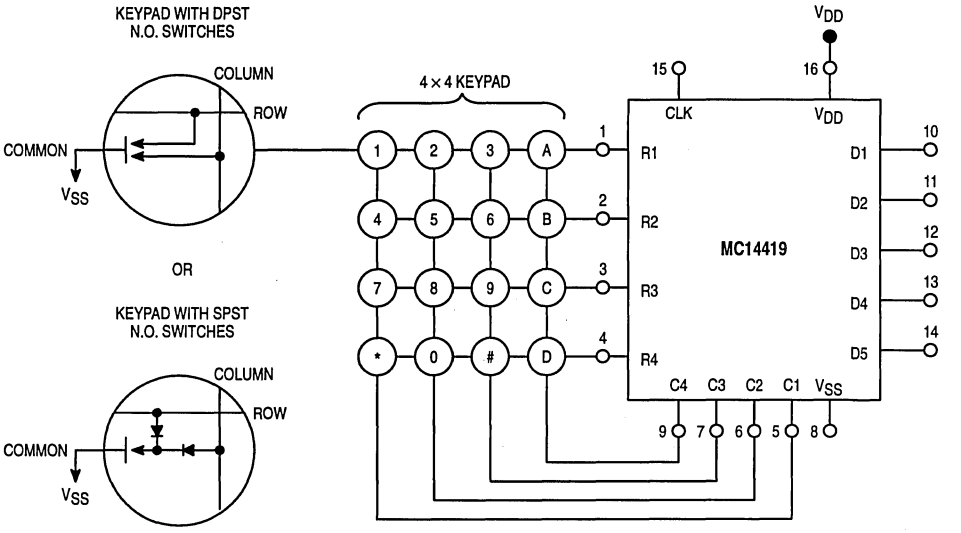


Figure 3. Typical Keypad Interface Application

MC14469

Addressable Asynchronous Receiver/Transmitter

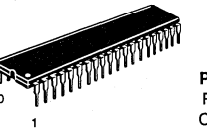
CMOS

The MC14469 receives one or two 11-bit words in a serial data stream. One of the incoming words contains the address and when the address matches, the MC14469 then transmits information in two 11-bit word data streams. Each of the transmitted words contains 8 data bits, an even parity bit, and start and stop bits.

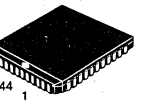
The received word contains 7 address bits with the address of the MC14469 set on seven pins. Therefore, 2^7 or 128 units can be interconnected in simplex or full-duplex data transmission. In addition to the address received, seven command bits may be received for general-purpose data or control use.

The MC14469 finds application in transmitting data from remote analog-to-digital converters, remote MPUs, or remote digital transducers to the master computer or MPU.

- Supply Voltage Range: 4.5 V to 18 V
- Low Quiescent Current: 75 µA Maximum @ 5 V, 25°C
- Guaranteed Data Rates to 4800 Baud @ 5 V, to 9600 Baud @ 12 V
- Receive — Serial to Parallel
  Transmit — Parallel to Parallel
- Transmit and Receive Simultaneously in Full Duplex
- Crystal or Resonator Operation for On-Chip Oscillator
- See Application Note AN806A
- Chip Complexity: 1200 FETs or 300 Equivalent Gates



P SUFFIX
PLASTIC
CASE 711



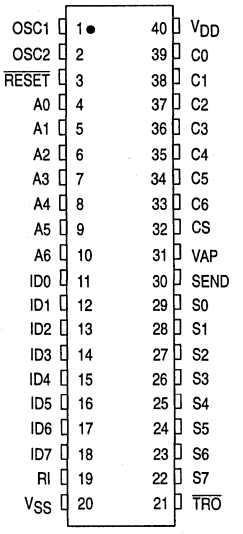
FN SUFFIX
PLCC
CASE 777

ORDERING INFORMATION

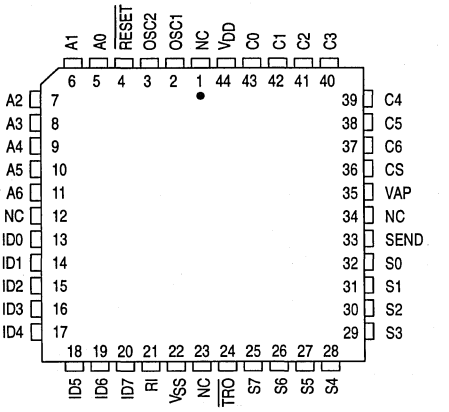
MC14469P	Plastic DIP
MC14469FN	PLCC

PIN ASSIGNMENTS

P SUFFIX



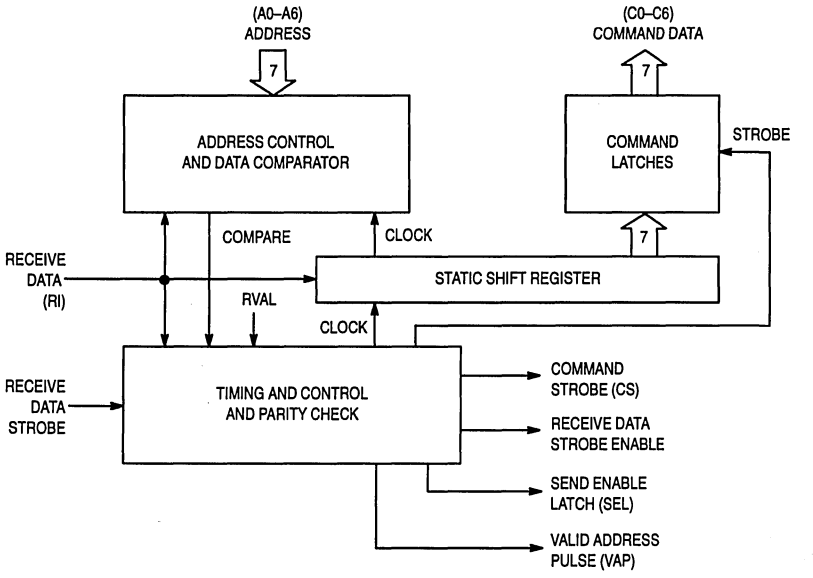
FN SUFFIX



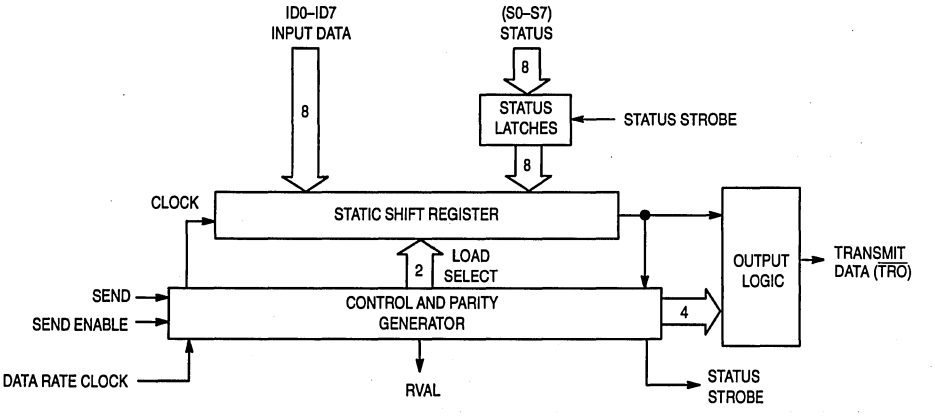
NC = NO CONNECTION

BLOCK DIAGRAM

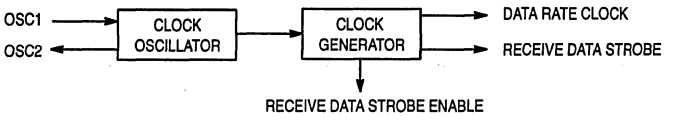
RECEIVE



TRANSMIT



CLOCKS



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages referenced to V_{SS})

Characteristic	Symbol	V_{DD}	−40°C Min	−40°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage									
"0" Level	V_{OL}	5.0	—	0.05	—	0.05	—	0.05	V
V_{in} = V_{DD} or 0		10	—	0.05	—	0.05	—	0.05	
		15	—	0.05	—	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.95	—	4.95	—	4.95	—	V
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	—	9.95	—	
		15	14.95	—	14.95	—	14.95	—	
Input Voltage (Except OSC1)									
"0" Level	V_{IL}								
V_O = 4.5 or 0.5 V		5.0	—	1.5	—	1.5	—	1.5	V
V_O = 9.0 or 1.0 V		10	—	3.0	—	3.0	—	3.0	
V_O = 13.5 or 1.5 V		15	—	4.0	—	4.0	—	4.0	
"1" Level	V_{IH}								
V_O = 0.5 or 4.5 V		5.0	3.5	—	3.5	—	3.5	—	V
V_O = 1.0 or 9.0 V		10	7.0	—	7.0	—	7.0	—	
V_O = 1.5 or 13.5 V		15	11	—	11	—	11	—	
Output Drive Current (Except OSC2)									
V_{OH} = 2.5 V Source	I_{OH}	5.0	−1.0	—	−0.8	—	−0.6	—	mA
V_{OH} = 4.6 V		5.0	−0.2	—	−0.16	—	−0.12	—	
V_{OH} = 9.5 V		10	−0.5	—	−0.4	—	−0.3	—	
V_{OH} = 13.5 V		15	−1.4	—	−1.2	—	−1.0	—	
V_{OL} = 0.4 V Sink	I_{OL}	5.0	0.52	—	0.44	—	0.36	—	mA
V_{OL} = 0.5 V		10	1.3	—	1.1	—	0.9	—	
V_{OL} = 1.5 V		15	3.6	—	3.0	—	2.4	—	
Output Drive Current (OSC2 Only)									
V_{OH} = 2.5 V Source	I_{OH}	5.0	−0.19	—	−0.16	—	−0.13	—	mA
V_{OH} = 4.6 V		5.0	−0.04	—	−0.035	—	−0.03	—	
V_{OH} = 9.5 V		10	−0.09	—	−0.08	—	−0.06	—	
V_{OH} = 13.5 V		15	−0.29	—	−0.27	—	−0.2	—	
V_{OL} = 0.4 V Sink	I_{OL}	5.0	0.1	—	0.085	—	0.07	—	mA
V_{OL} = 0.5 V		10	0.17	—	0.14	—	0.1	—	
V_{OL} = 1.5 V		15	0.5	—	0.42	—	0.3	—	
OSC Frequency*	f_{OSC}	4.5	0	400	0	365	0	310	kHz
		12	0	800	0	730	0	620	
Input Current	I_{in}	15	—	±0.3	—	±0.3	—	±1.0	µA
Pull-Up Current (A0–A6, ID0–ID7)	I_{UP}	15	12	120	10	100	8.0	85	µA
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0	—	75	—	75	—	565	µA
		10	—	150	—	150	—	1125	
		15	—	300	—	300	—	2250	
Supply Voltage	V_{DD}	—	+4.5	+18	+4.5	+18	+4.5	+18	V

*310 kHz at 85°C guarantees 4800 baud; 620 kHz at 85°C guarantees 9600 baud.

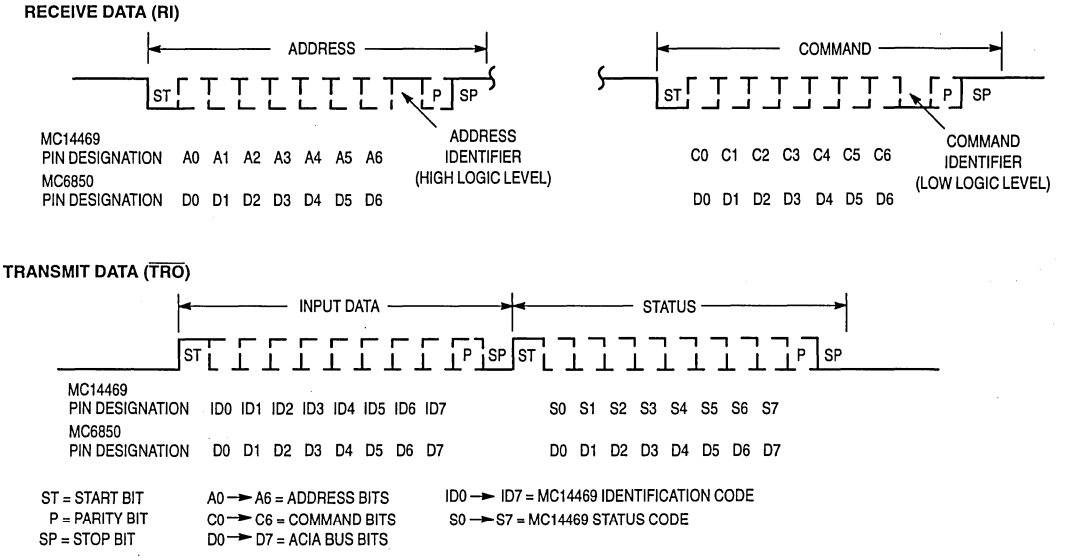


Figure 1. Data Format and Corresponding Data Position and Pins for MC14469 and MC6850

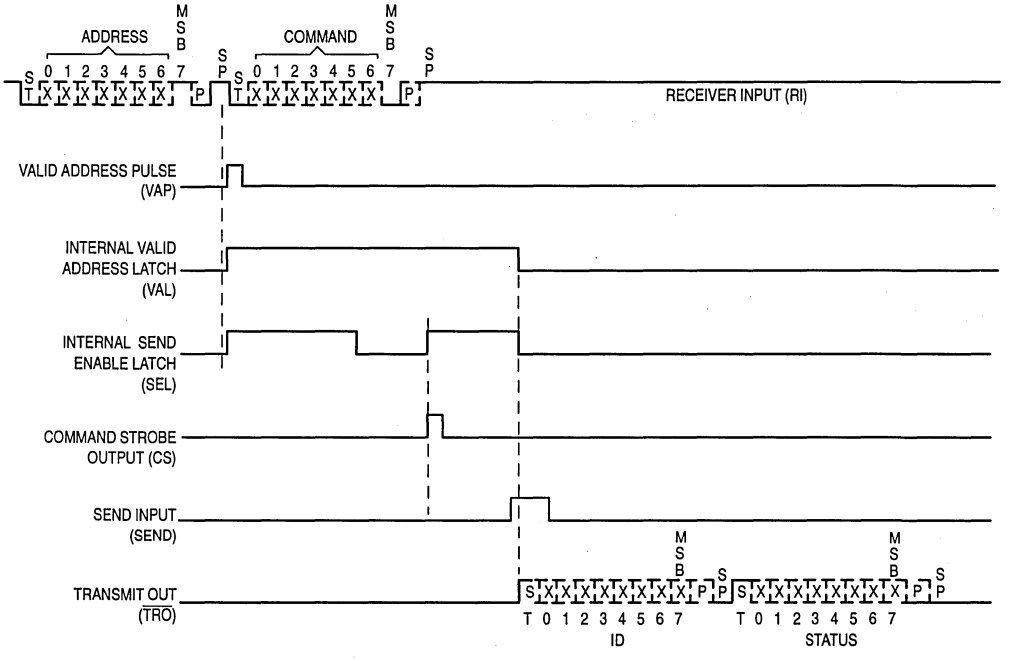


Figure 2. Typical Receive/Send Cycle

PIN DESCRIPTIONS

A0–A6
Address Inputs
These inputs are the address setting pins which contain the address match for the received signal. Pins A0–A6 have on-chip pull-up resistors.

C0–C6
Command Word
These pins are the readout of the general-purpose command word which is the second word of the received signal.

CS
Command Strobe
This is the output for the command strobe signifying a valid set of command data (C0–C6). The pulse width is one oscillator cycle. For eample, when a 307.2 kHz ceramic resonator is usd, the pulse width is approximately 3 μs.

ID0–ID7
Input Data Pins
These pins contain the input data for the first eight bits of data to be transmitted. Pins ID0–ID7 have on-chip pull-up resistors.

OSC1, OSC2
Oscillator Input and Oscillator Output
These pins are the oscillator input and output (see Figure 3).

$\overline{\text{RESET}}$
Reset
When this pin is pulled low for a minimum of 700 ns, the circuit is reset and ready for operation.

RI
Receive Input
This is the receive input pin.

S0–S7
Second or Status Input Data
These pins contain the input data for the second 8 bits of data to be transmitted.

SEND
Send
This pin accepts the send command after receipt of an address.

$\overline{\text{TRO}}$
Transmit Register Output Signal
This pin transmits the outgoing signal. Note that it is inverted from the incoming signal. It must go through one stage of inversion if it is to drive another MC14469.

VAP
Valid Address Pulse
This is the output for the valid address pulse upon receipt of a matched incoming address.

V_{DD}
Positive Power Supply
This pin is the package positive power supply connection. This pin may range from + 4.5 V to + 18 V with respect to V_{SS}.

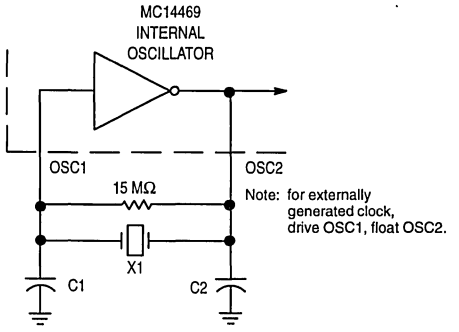
V_{SS}
Negative Power Supply
This pin is the negative power supply connection. Normally this pin is system ground.

OPERATING CHARACTERISTICS

The receipt of a start bit on the receive input (RI) line causes the receive clock to start at a frequency equal to that of the oscillator divided by 64. All received data is strobed in at the center of a receive clock period. The start bit is followed by 8 data bits. Seven of the bits are compared against states of the address of the particular circuit (A0–A6). Address is latched 31 clock cycles after the end of the start bit of the incoming address. The eighth bit signifies an address word "1" or a command word "0". Next, a parity bit is received and checked by the internal logic for even parity. Finally a stop bit is received. At the completion of the cycle if the address matches, a valid address pulse (VAP) occurs. Immediately following the address word, a command word is received. It also contains a start bit, eight data bits, even parity bit, and a stop bit. The 8 data bits are composed of a seven-bit command, and a "0" which indicates a command word. At the end of the command word a command strobe pulse (CS) occurs.

A positive transition on the send input initiates the transmit sequence. Send must occur within 7 bit times of CS. Again the transmitted data is made up of two eleven-bit words, i.e., address and command words. The data portion of the first word is made up from input data inputs (ID0–ID7), and the data for the second word from second input data (S0–S7) inputs. The data on inputs ID0–ID7 is latched one clock before the falling edge of the start bit. The data on inputs S0–S7 is latched on the rising edge of the start bit. The transmitted signal is the inversion of the received signal, which allows the use of an inverting amplifier to drive the lines. $\overline{\text{TRO}}$ begins either 1/2 or 1-1/2 bit times after send, depending where send occurs.

The oscillator can be crystal controlled or ceramic resonator controlled for required accuracy. OSC1 can be driven from an external oscillator (see Figure 3).



X1 = Ceramic Resonator: 307.2 kHz ± 1 kHz for 4800 baud rate.
C1 and C2 are sized per the ceramic resonator supplier's recommendation.

Ceramic Resonator Suppliers:*
1. Morgan Matroc, Inc., Bedford, OH, 216/232–8600
2. Radio Materials Co., Attica, IN, 317/762–2491

* Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of ceramic resonator suppliers.

Figure 3. Oscillator Circuit

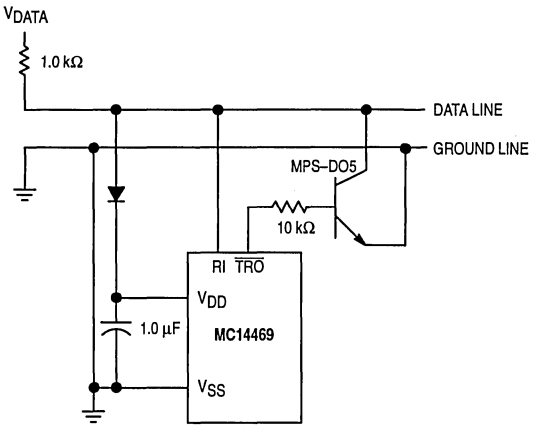


Figure 4. Rectified Power from Data Lines Circuit

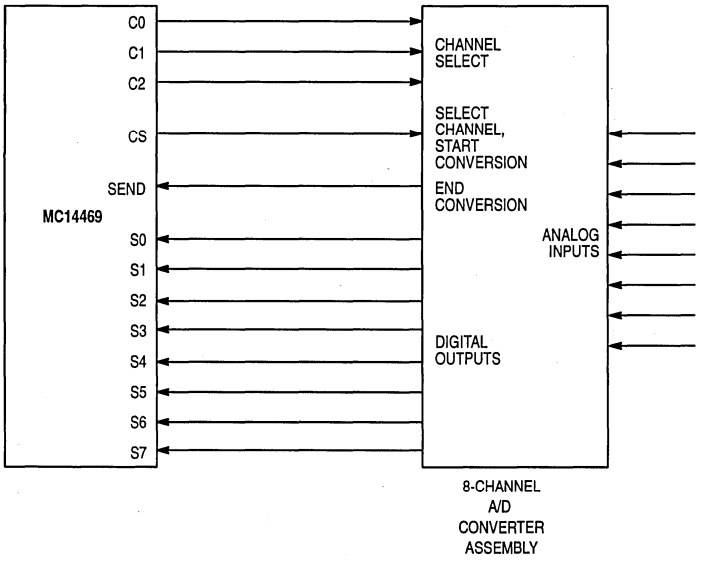


Figure 5. A-D Converter Interface

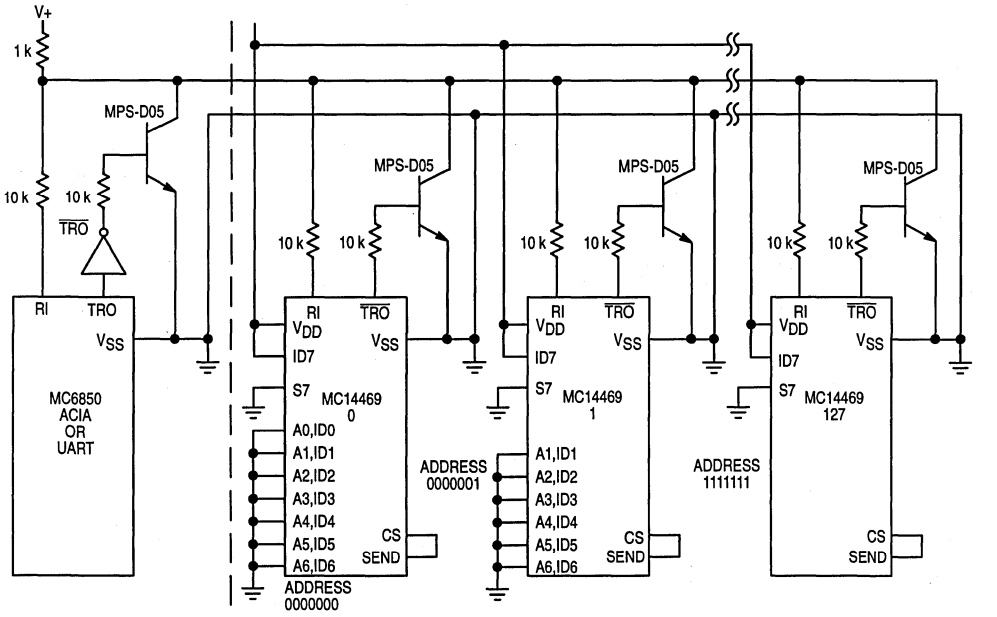


Figure 6. Single Line, Simplex Data Transmission

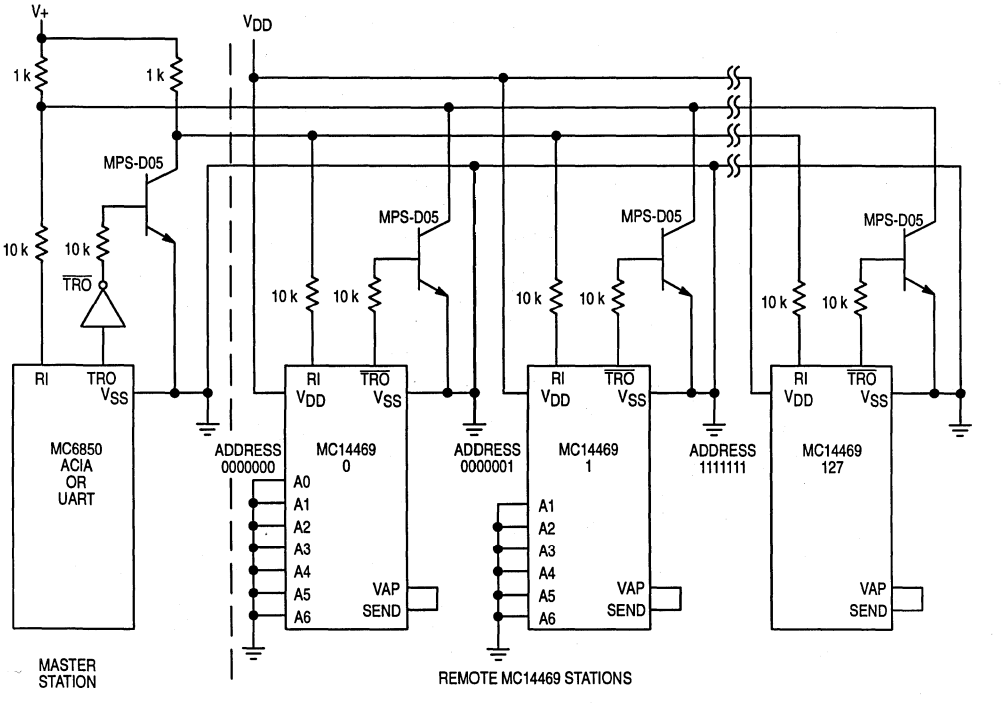


Figure 7. Double Line, Full Duplex Data Transmission

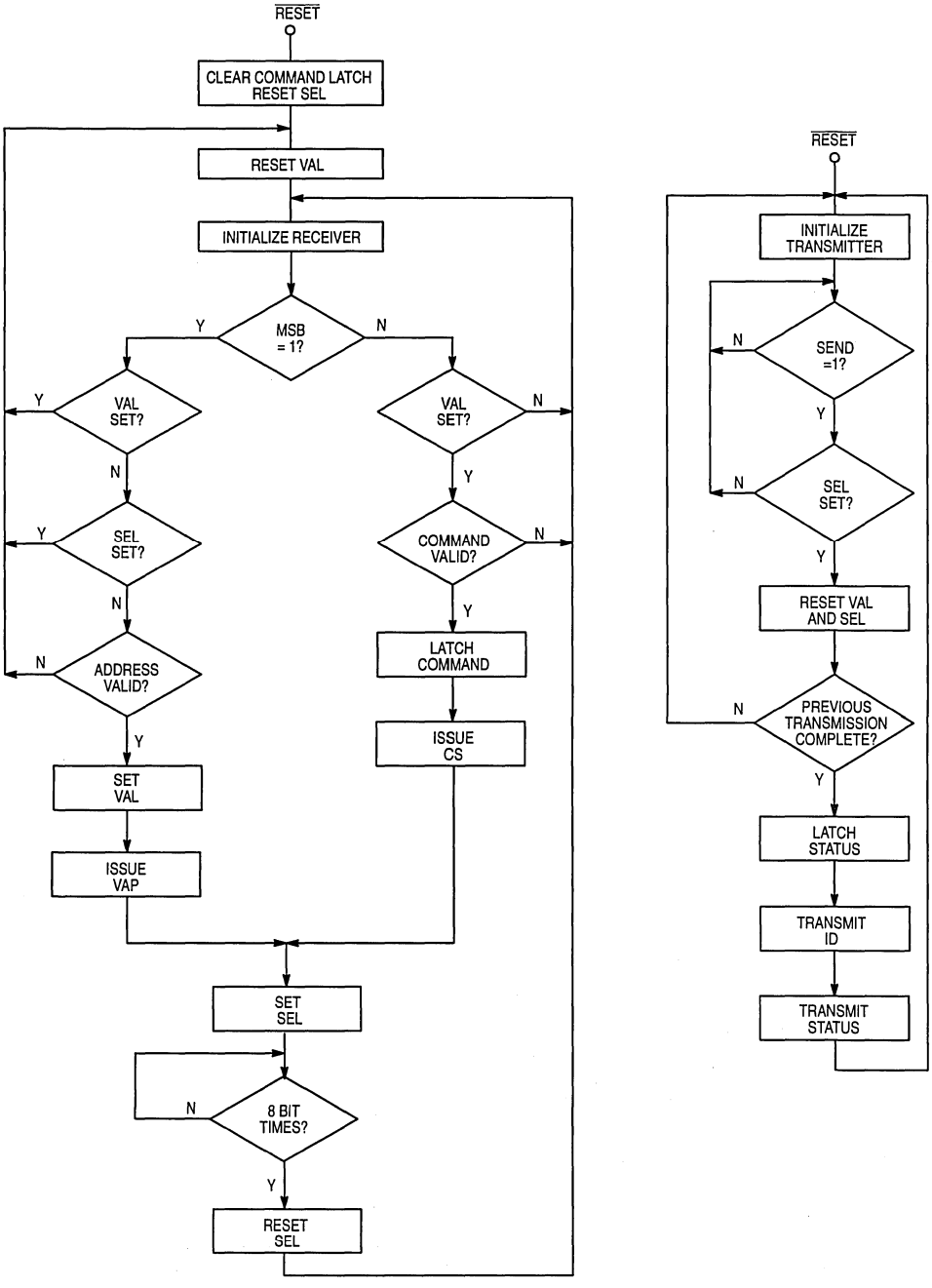


Figure 8. Flow Chart of MC14469 Operation

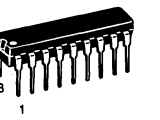
MC14497

PCM Remote Control Transmitter

The MC14497 is a PCM remote control transmitter realized in CMOS technology. Using a dual-single (FSK/AM) frequency bi-phase modulation, the transmitter is designed to work with the MC3373 receiver. Information on the MC3373 can be found in the Motorola *Linear* and *Interface Integrated Circuits* book (DL128/D).

There is not a decoder device which is compatible with the MC14497. Typically, the decoding resides in MCU software.

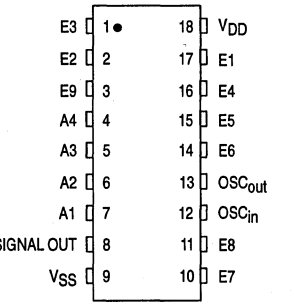
- Both FSK/AM Modulation Selectable
- 62 Channels (Up to 62 Keys)
- Reference Oscillator Controlled by Inexpensive Ceramic Resonator: Maximum Frequency = 500 kHz
- Very Low Duty Cycle
- Very Low Standby Current: 50 µA Maximum
- Infrared Transmission
- Selectable Start-Bit Polarity (AM only)
- Shifted Key Mode Available
- Wide Operating Voltage Range: 4 to 10 V
- See Application Notes AN1016 and AN1203



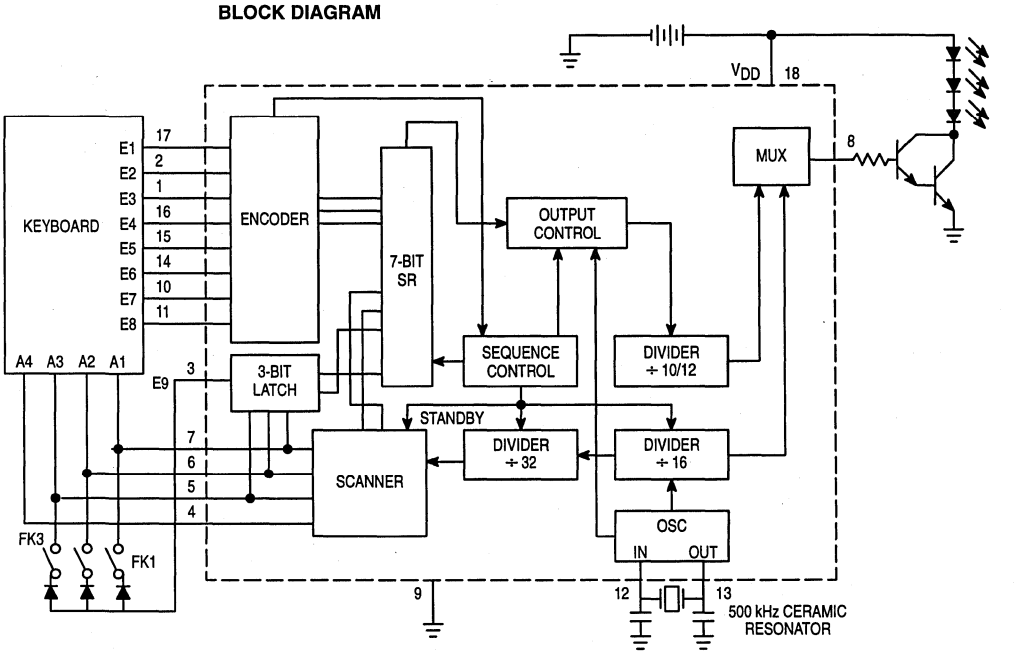
P SUFFIX
PLASTIC DIP
CASE 707

PIN ASSIGNMENTS

P SUFFIX



BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C; all Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD}	Min	Max	Unit
Supply Voltage		V_{DD}	—	4.0	10.0	V
Supply Current		I_{DD}				
Idle			10	—	50	µA
Operation			10	—	5	mA
Output Current — Signal						
V_{OH} = 3.0 V	Source	I_{OH}	4	−900	—	µA
V_{OL} = 0.5 V	Sink	I_{OL}	4	120	—	
Output Current — Scanner						
V_{OH} = 3.0 V	Source	I_{OH}	4	−30	—	µA
V_{OL} = 0.5 V	Sink	I_{OL}	4	245	—	
Output Current — Oscillator						µA
V_{OH} = 3.0 V	Source	I_{OH}	4	−300	—	
V_{OL} = 0.5 V	Sink	I_{OL}	4	245	—	
Input Current — Oscillator		I_{in}				
Operation			10	±2	±80	µA
Idle, V_{IL} = 0.5 V			4	30	—	
Input Current — Encoder		I_{in}				
V_{IH} = 9.0 V			10	−15	—	µA
V_{IL} = 0.5 V			4	—	−60	
Input Voltage — Encoder						
		V_{IH}	10	9	—	V
		V_{IL}	10	—	1.2	
		V_{IH}	4	3	—	
		V_{IL}	4	—	1.0	

CIRCUIT OPERATION

The transmitter sends a 6-bit, labelled A (LSB to F (MSB), binary code giving a total of 64 possible combinations or code words. All of these channels are user selectable, except the last two (where channel 63 is not sent while channel 62 is automatically sent by the transmitter at the end of each transmission as an "End of Transmission" code).

In either mode, FSK or AM, the transmitted signal is in the form of a bi-phase pulse code modulation (PCM) signal. The AM coding is shown in Figure 1.

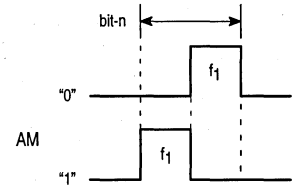


Figure 1. AM Coding

In the AM mode, f_1 is a train of pulses at the modulating frequency of 31.25 kHz for a reference frequency of 500 kHz.

In the FSK mode, two modulating frequencies are used as shown in Figure 2.

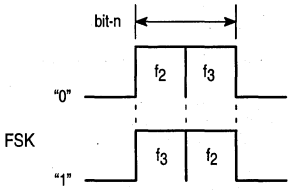


Figure 2. FSK Coding

In this mode, f_3 is 50 kHz and f_2 is 41.66 kHz for a reference frequency of 500 kHz.

The keyboard can be a simple switch matrix using no external diodes, connected to the four scanner inputs (A1–A4) and the eight row input (E1–E8). Under these coditions, only the first 32 code words are avilable since bit-F is always at logical 0. However, a simple 2-pole changeover switch, in the manner of a typewriter "shift" key (switch FK3 in the Block Diagram) can be used to change the polarity of bit-F to give access to the next full set of 32 instructions.

An alternative method of accessing more than 32 instructions is by the use of external diodes between the address inputs (see Figure 3). These have the effect of producing "phantom" address inputs by pulling two inputs low at the same time, which causes bit-F to go high (i.e., to logical 1). By interconnecting only certain address inputs it is possible to make an intermediate keyboard with between 32 and 64 keys.

The other two switches in the Block Diagram (FK1 and FK2) change the modulation mode. Closing FK1 changes the modulation from FSK to AM and the start-bit polarity. Closing FK2 changes the start–bit to a logical 0.

The full range of options available is illustrated in Table 1.

Table 1.

	Start Bit	Modulation	Bit-F	Channels
E9 = Open	1	FSK	0	0–31
E9 = A1 (FK1)	1	AM	0	0–31
E9 = A2 (FK2)	0	FSK	0	0–31*
E9 = A3 (FK3)	1	FSK	1	32–61
E9 = A1 • A2	0	AM	0	0–31
E9 = A1 • A3	1	AM	1	32–61
E9 = A2 • A3	0	FSK	1	32–61*
E9 = A1 • A2 • A3	0	AM	1	32–61

*Not allowed.

One of the transmitter's major features is its low power consumption (in the order of 10 μA in the idle state). For this reason, the battery is perpetually in circuit. It has in fact been found that a light discharge current is beneficial to battery life.

In its active state, the transmitter efficiency is increased by the use of a low duty cycle which is less than 2.5% for the modulating pulse trains.

While no key is pressed, the circuit is in its diel state and the reference oscillaotr is stopped. also, the eifht address input lines are held high through internal pull-up resistors.

As soon as a key is pressed, this takes the appropriate address line low, signaling to the circuit that a key has been selected. The oscillator is now enabled. If the key is released before the code word has been sent, the circuit returns to its idle state. to account for accidental activation of the transmitter, the circuit has a built-in rective time of approximately 20 ms, which also overcomes contact bounce. After this delay, the code word will be sent and repeated at 90 ms intervals for as long as the key is pressed. As soon as the key is released, the circuit automatically sends channel 62, the "End of Transmission" (EOT) code. The transmitter then returns to its idel steate.

The differences between the two modulation modes are illustrated in Figure 4. However, it should be noted that in the AM mode, each transmitted word is preceded bya burst of pulses lasting 512 μs. This is used to set up the AGC loop in the receiver's preamp. In the FSK mode, the first frequency of the first bit is extended by 1.5 ms and the AGC burst is suppressed. In either mode, it is assumed that the normal start-bit is present.

PIN DESCRIPTIONS

E1–E8
Row Inputs (Pins 1, 2, 10, 11, 14, 15, 16, 17)

Under idle conditions, these inputs are held high by internal pull-up resistors. As soon as a key is pressed, a logical 0 on that particular line signals to the circuit that a key has been selected. After a delay of 20 ms, the internal register is loaded with the code word for the key selected.

E9
Row Input (Pin 3)

This is a special programming input and when connected to the appropriate scanner output via a diode, it will modify the transmitted output according to Table 1.

In Table 1, the figures in brackets (FK1, etc.) refer to the switches shown in the Block Diagram and Figure 3. If only one option is required, the diode may be omitted. The connections shown in Table 1 may be made in any combination.

Although E9 is a row input, forcing this line low will not activate the circuit.

A1–A4
Scanner Outputs (Pins 4–7)

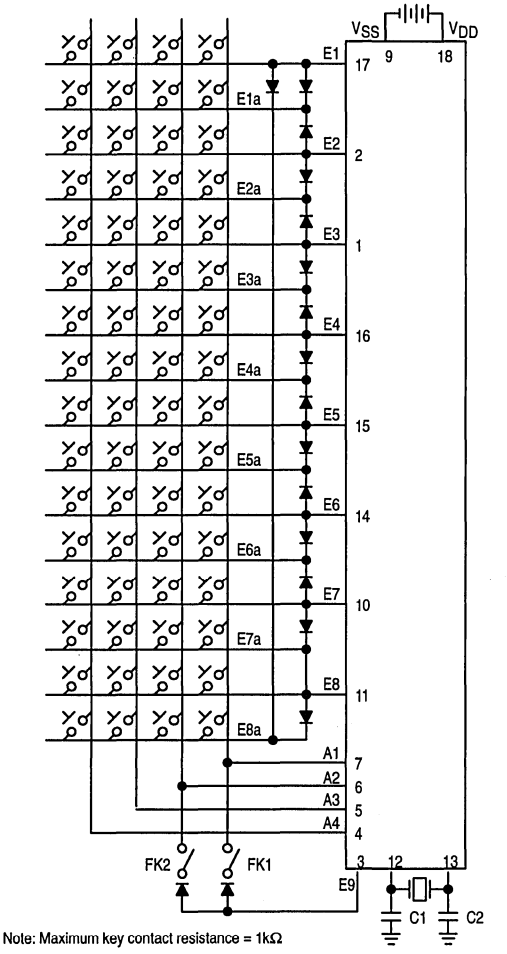
Under idle conditions, these outputs are held low, logical 0. when a key is pressed, the circuit is activated and the oscillator will start and release the outputs (see Figure 5).

OSC_{in}, OSC_{out}
Oscillator Input and Oscillator Output (Pins 12, 13)

These pins are designed to operate with a 500 kHz ceramic resonator or a tune LC circuit. It is important that a ceramic resonator and **not a filter** be used here, as the oscillator frequency cannot be guaranteed if a ceramic filter is used.

SIGNAL OUT
Signal Output (Pin 8)

This output provides the modulating signal ready to drive the modulation amplifier. If required, the transmitter can be used as a keyboard encoder for direct use with a receiver. In this case, the AM option is selected, the output inverted, and fed directly to the receiver's signal input pin.



Note: Maximum key contact resistance = 1kΩ

Figure 3. 64-Key Keyboard

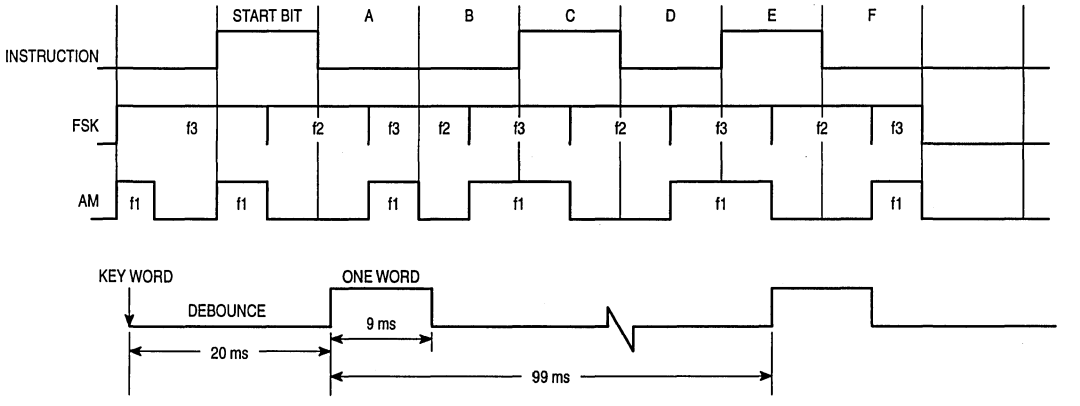


Figure 4. Transmitted Waveforms and Timing (not drawn to scale)

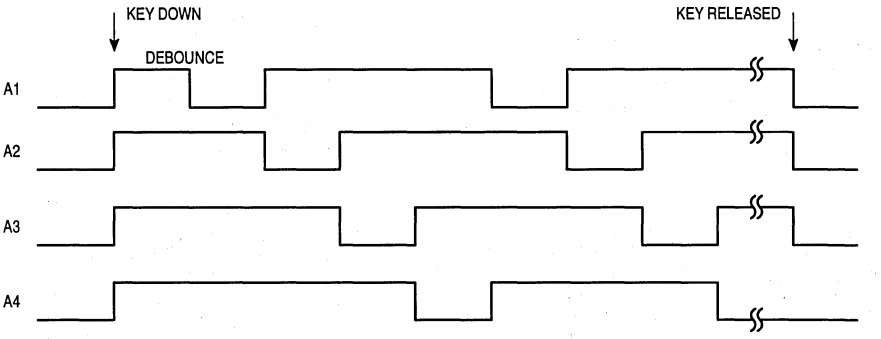
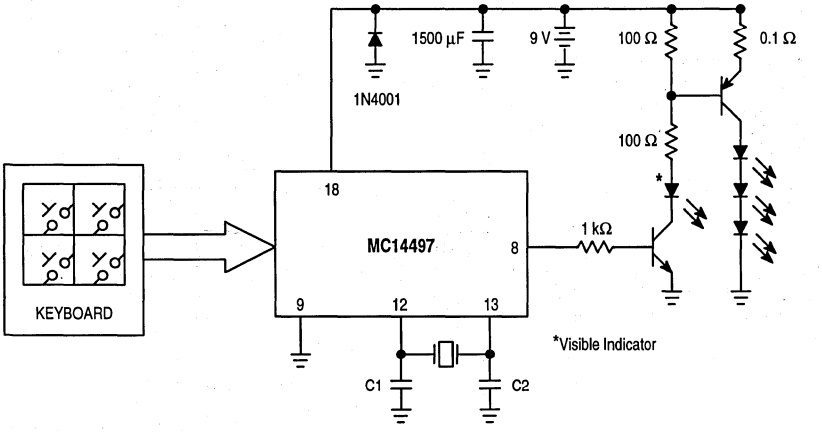
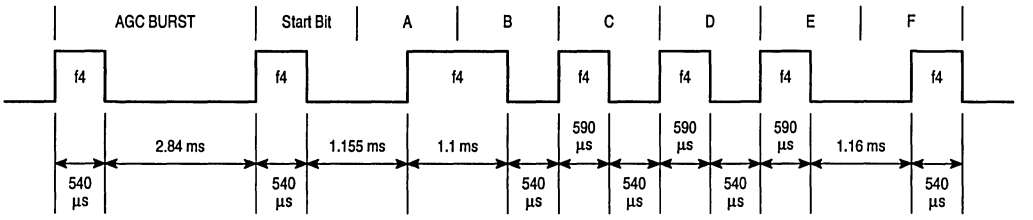


Figure 5. Scanner Output Timing Diagram



C1 and C2 are sized per the ceramic resonator supplier's recommendation.
Ceramic Resonator Suppliers:
1. Morgan Matrox, Inc., Bedford, OH, 216/232-8600
2. Radio Materials Co., Attica, IN, 317/762-2491
Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of ceramic resonator suppliers.

Figure 6. Typical Application Circuit



Notes:
1. f4 = 28.4 kHz.
2. Indicated time durations are approximated.

Figure 7. AM Mode Transmitted Wavetrain with 455 kHz Oscillator

Table 2. Transmitted Codes

Channel	Code Word F	E	D	C	B	A	Keyboard In	Out	Channel	Code Word F	E	D	C	B	A	Keyboard In	Out
0	0	0	0	0	0	0	E8	A4	32	1	0	0	0	0	0	E8a	A4
1				0	0	1	E1	A4	33				0	0	1	E1a	A4
2				0	1	0	E2	A4	34				0	1	0	E2a	A4
3				0	1	1	E3	A4	35				0	1	1	E3a	A4
4				1	0	0	E4	A4	36				1	0	0	E4a	A4
5				1	0	1	E5	A4	37				1	0	1	E5a	A4
6				1	1	0	E6	A4	38				1	1	0	E6a	A4
7				1	1	1	E7	A4	39				1	1	1	E7a	A4
8	0	0	1	0	0	0	E8	A1	40	1	0	1	0	0	0	E8a	A1
9				0	0	1	E1	A1	41				0	0	1	E1a	A1
10				0	1	0	E2	A1	42				0	1	0	E2a	A1
11				0	1	1	E3	A1	43				0	1	1	E3a	A1
12				1	0	0	E4	A1	44				1	0	0	E4a	A1
13				1	0	1	E5	A1	45				1	0	1	E5a	A1
14				1	1	0	E6	A1	46				1	1	0	E6a	A1
15				1	1	1	E7	A1	47				1	1	1	E7a	A1
16	0	1	0	0	0	0	E8	A3	48	1	1	0	0	0	0	E8a	A3
17				0	0	1	E1	A3	49				0	0	1	E1a	A3
18				0	1	0	E2	A3	50				0	1	0	E2a	A3
19				0	1	1	E3	A3	51				0	1	1	E3a	A3
20				1	0	0	E4	A3	52				1	0	0	E4a	A3
21				1	0	1	E5	A3	53				1	0	1	E5a	A3
22				1	1	0	E6	A3	54				1	1	0	E6a	A3
23				1	1	1	E7	A3	55				1	1	1	E7a	A3
24	0	1	1	0	0	0	E8	A2	56	1	1	1	0	0	0	E8a	A2
25				0	0	1	E1	A2	57				0	0	1	E1a	A2
26				0	1	0	E2	A2	58				0	1	0	E2a	A2
27				0	1	1	E3	A2	59				0	1	1	E3a	A2
28				1	0	0	E4	A2	60				1	0	0	E4a	A2
29				1	0	1	E5	A2	61				1	0	1	E5a	A2
30				1	1	0	E6	A2	62				1	1	0	E6a	A2
31	0	1	1	1	1	1	E7	A2	Not Transmitted	1	1	1	1	1	1	E7a	A2

NOTE: Although the "a" suffix applies to a phantom input when using a keyboard with up to 64 keys, the coding is identical with a 32-key keyboard when switch FK3 is closed.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33102

Advance Information

Sleep-Mode™ Two-State, Micropower Operational Amplifier

DUAL SLEEP-MODE™ OPERATIONAL AMPLIFIERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC33102 dual operational amplifier is an innovative design concept employing Sleep-Mode™ technology. Sleep-Mode amplifiers have two separate states, a sleepmode and an awakemode. In sleepmode, the amplifier is active and waiting for an input signal. When a signal is applied causing the amplifier to source or sink 160 μA (typically) to the load, it will automatically switch to the awakemode which offers higher slew rate, gain bandwidth, and drive capability.

- Two States: "Sleepmode" (Micropower) and "Awakemode" (High Performance)
- Switches from Sleepmode to Awakemode in 4.0 μs when Output Current Exceeds the Threshold Current (R_L = 600 Ω)
- Independent Sleepmode Function for Each Op Amp
- Standard Pinouts – No Additional Pins or Components Required
- Sleepmode State – Can Be Used in the Low Current Idle State as a Fully Functional Micropower Amplifier
- Automatic Return to Sleepmode when Output Current Drops Below Threshold
- No Deadband/Crossover Distortion; as Low as 1.0 Hz in the Awakemode
- Drop-in Replacement for Many Other Dual Op Amps
- ESD Clamps on Inputs Increase Reliability without Affecting Device Operation

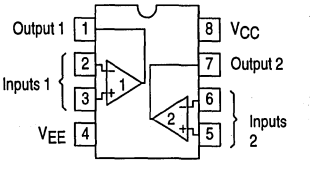
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

P SUFFIX
PLASTIC PACKAGE
CASE 626

TYPICAL SLEEPMODE/AWAKEMODE PERFORMANCE

Characteristic	Sleepmode (Typical)	Awakemode (Typical)	Unit
Low Current Drain	45	750	μA
Low Input Offset Voltage	0.15	0.15	mV
High Output Current Capability	0.15	50	mA
Low T.C. of Input Offset Voltage	1.0	1.0	μV/°C
High Gain Bandwidth (@20 kHz)	0.33	4.6	MHz
High Slew Rate	0.16	1.7	V/μs
Low Noise (@ 1.0 kHz)	28	9.0	$nV/\sqrt{Hz}$

PIN CONNECTIONS



(Dual Package, Top View)

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range Input Voltage Range	V_{IDR} V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	(Note 2)	sec
Maximum Junction Temperature Storage Temperature	T_J T_{stg}	+150 –65 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

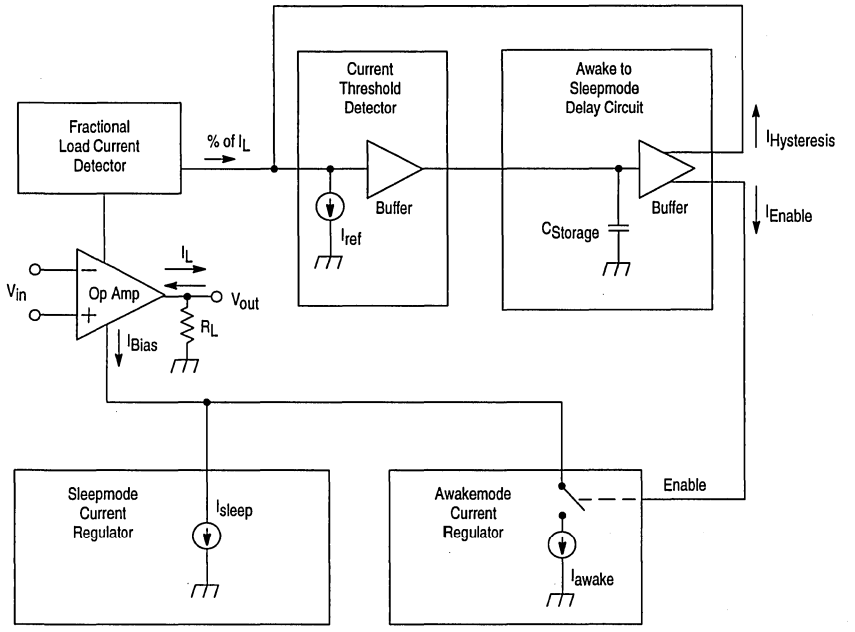
NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (refer to Figure 1).

ORDERING INFORMATION

Device	Temperature Range	Package
MC33102D	–40° to +85°C	SO-8
MC33102P		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Simplified Block Diagram



DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	2	$\lvert V_{IO} \rvert$				mV
Sleepmode						
T_A = +25°C			—	0.15	2.0	
T_A = –40° to +85°C			—	—	3.0	
Awakemode						
T_A = +25°C			—	0.15	2.0	
T_A = –40° to +85°C			—	—	3.0	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V) T_A = –40° to +85°C (Sleepmode and Awakemode)	3	$\Delta V_{IO}/\Delta T$	—	1.0	—	µV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	4, 6	I_{IB}				nA
Sleepmode						
T_A = +25°C			—	8.0	50	
T_A = –40° to +85°C			—	—	60	
Awakemode						
T_A = +25°C			—	100	500	
T_A = –40° to +85°C			—	—	600	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	—	$\lvert I_{IO} \rvert$				nA
Sleepmode						
T_A = +25°C			—	0.5	5.0	
T_A = –40° to +85°C			—	—	6.0	
Awakemode						
T_A = +25°C			—	5.0	50	
T_A = –40° to +85°C			—	—	60	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	5	V_{ICR}				V
Sleepmode and Awakemode			–13	–14.8	—	
			—	+14.2	+13	
Large Signal Voltage Gain	7	A_{VOL}				kV/V
Sleepmode (RL = 1.0 MΩ)						
T_A = +25°C			25	200	—	
T_A = –40° to +85°C			15	—	—	
Awakemode (V_O = ±10 V, R_L = 600 Ω)						
T_A = +25°C			50	700	—	
T_A = –40° to +85°C			25	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 10					V
Sleepmode (V_{CC} = +15 V, V_{EE} = –15 V)						
R_L = 1.0 MΩ		V_{O+}	+13.5	+14.2	—	
R_L = 1.0 MΩ		V_{O-}	—	–14.2	–13.5	
Awakemode (V_{CC} = +15 V, V_{EE} = –15 V)						V
R_L = 600 Ω		V_{O+}	+12.5	+13.6	—	
R_L = 600 Ω		V_{O-}	—	–13.6	–12.5	
R_L = 2.0 kΩ		V_{O+}	+13.3	+14	—	
R_L = 2.0 kΩ		V_{O-}	—	–14	–13.3	
Awakemode (V_{CC} = +2.5 V, V_{EE} = –2.5 V)						
R_L = 600 Ω		V_{O+}	+1.1	+1.6	—	
R_L = 600 Ω		V_{O-}	—	–1.6	–1.1	
Common Mode Rejection (V_{CM} = ±13 V)	11	CMR				dB
Sleepmode and Awakemode			80	90	—	
Power Supply Rejection (V_{CC}/V_{EE} = +15 V/–15 V, 5.0 V/–15 V, +15 V/–5.0 V)	12	PSR				dB
Sleepmode and Awakemode			80	100	—	
Output Transition Current	13, 14					µA
Sleepmode to Awakemode (Source/Sink)		$\lvert I_{TH1} \rvert$				
(V_S = ±15 V)			200	160	—	
(V_S = ±2.5 V)			250	200	—	
Awakemode to Sleepmode (Source/Sink)		$\lvert I_{TH2} \rvert$				
(V_S = ±15 V)			—	142	90	
(V_S = ±2.5 V)			—	180	140	
Output Short Circuit Current (Awakemode) (V_{ID} = ±1.0 V, Output to Ground)	15, 16	$\lvert I_{SC} \rvert$				mA
Source			50	110	—	
Sink			50	110	—	
Power Supply Current (per Amplifier) (A_{CL} = 1, V_O = 0V)	17	I_D				µA
Sleepmode (V_S = ±15 V)						
T_A = +25°C			—	45	65	
T_A = –40° to +85°C			—	48	70	
Sleepmode (V_S = ±2.5 V)						
T_A = +25°C			—	38	65	
T_A = –40° to +85°C			—	42	—	
Awakemode (V_S = ±15 V)						
T_A = +25°C			—	750	800	
T_A = –40° to +85°C			—	800	900	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −5.0 V to +5.0 V, C_L = 50 pF, A_V = 1.0)	18	SR				V/μs
Sleepmode (R_L = 1.0 MΩ)			0.10	0.16	—	
Awakemode (R_L = 600 Ω)			1.0	1.7	—	
Gain Bandwidth Product	19	GBW				MHz
Sleepmode (f = 10 kHz)			0.25	0.33	—	
Awakemode (f = 20 kHz)			3.5	4.6	—	
Sleepmode to Awakemode Transition Time	20, 21	t_{tr1}				μs
(A_{CL} = 0.1, V_{in} = 0 V to +5.0 V)						
R_L = 600 Ω			—	4.0	—	
R_L = 10 kΩ			—	15	—	
Awakemode to Sleepmode Transition Time	22	t_{tr2}	—	1.5	—	sec
Unity Gain Frequency (Open-Loop)		f_U				kHz
Sleepmode (R_L = 100 kΩ, C_L = 0 pF)			—	200	—	
Awakemode (R_L = 600 Ω, C_L = 0 pF)			—	2500	—	
Gain Margin	23, 25	A_M				dB
Sleepmode (R_L = 100 kΩ, C_L = 0 pF)			—	13	—	
Awakemode (R_L = 600 Ω, C_L = 0 pF)			—	12	—	
Phase Margin	24, 26	$\varnothing_M$				Degrees
Sleepmode (R_L = 100 kΩ, C_L = 0 pF)			—	60	—	
Awakemode (R_L = 600 Ω, C_L = 0 pF)			—	60	—	
Channel Separation (f = 100 Hz to 20 kHz)	29	CS				dB
Sleepmode and Awakemode			—	120	—	
Power Bandwidth (Awakemode)		BW_P				kHz
(V_O = 10 V_{p-p}, R_L = 100 kΩ, THD ≤ 1%)			—	20	—	
Total Harmonic Distortion (V_O = 2.0 V_{p-p}, A_V = 1.0)	30	THD				%
Awakemode (R_L = 600 Ω)						
f = 1.0 kHz			—	0.005	—	
f = 10 kHz			—	0.016	—	
f = 20 kHz			—	0.031	—	
DC Output Impedence (V_O = 0 V, A_V = 10, I_Q = 10 μA)	31	R_O				Ω
Sleepmode			—	1.0 k	—	
Awakemode			—	96	—	
Differential Input Resistance (V_{CM} = 0 V)		R_{in}				MΩ
Sleepmode			—	1.3	—	
Awakemode			—	0.17	—	
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}				pF
Sleepmode			—	0.4	—	
Awakemode			—	4.0	—	
Equivalent Input Noise Voltage (f = 1.0 kHz, R_S = 100 Ω)	32	e_n				nV/√Hz
Sleepmode			—	28	—	
Awakemode			—	9.0	—	
Equivalent Input Noise Current (f = 1.0 kHz)	33	i_n				pA/√Hz
Sleepmode			—	0.01	—	
Awakemode			—	0.05	—	

Figure 1. Maximum Power Dissipation versus Temperature

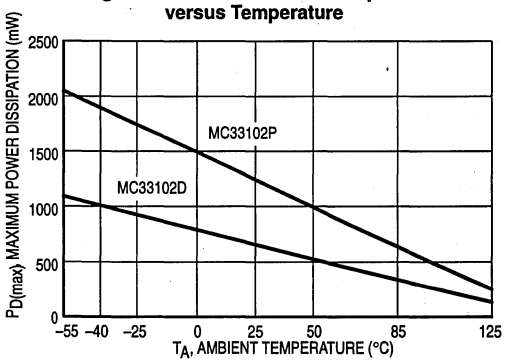


Figure 2. Distribution of Input Offset Voltage

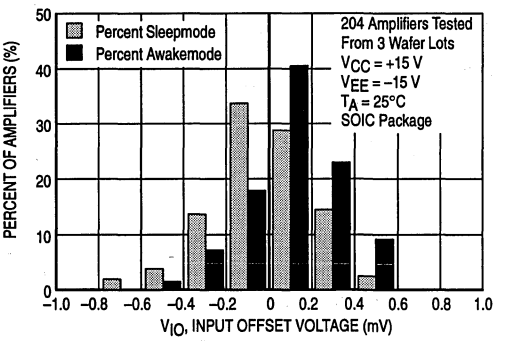


Figure 3. Input Offset Voltage Temperature Coefficient Distribution

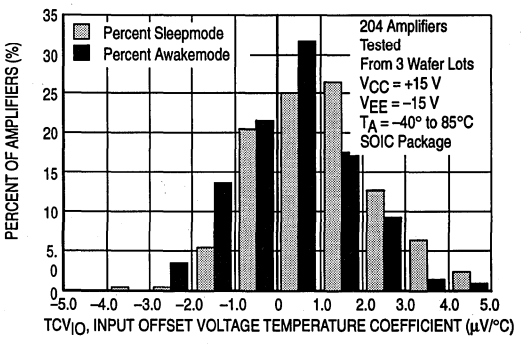


Figure 4. Input Bias Current versus Common Mode Input Voltage

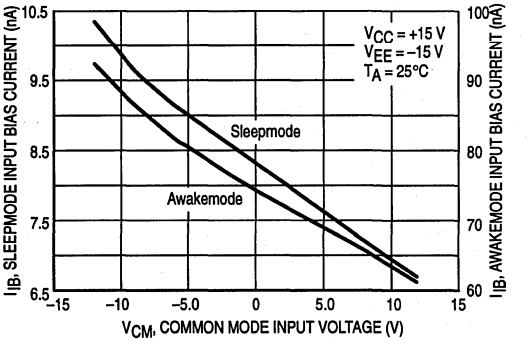


Figure 5. Input Common Mode Voltage Range versus Temperature

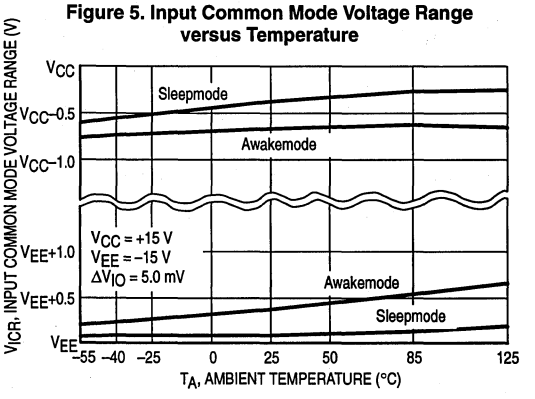


Figure 6. Input Bias Current versus Temperature

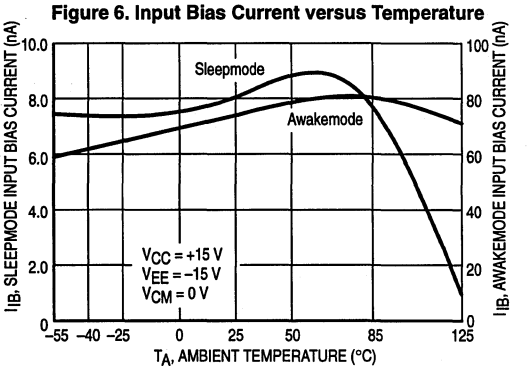


Figure 7. Open-Loop Voltage Gain versus Temperature

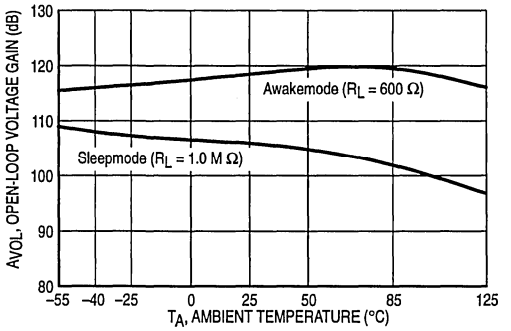


Figure 8. Output Voltage Swing versus Supply Voltage

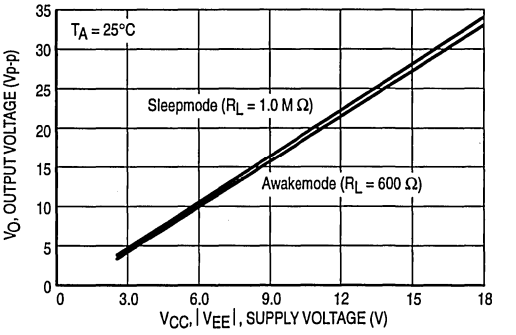


Figure 9. Output Voltage versus Frequency

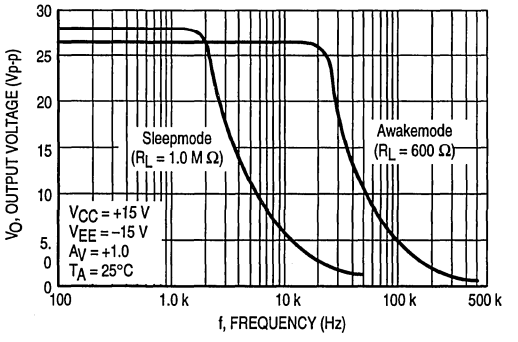


Figure 10. Maximum Peak-to-Peak Output Voltage Swing versus Load Resistance

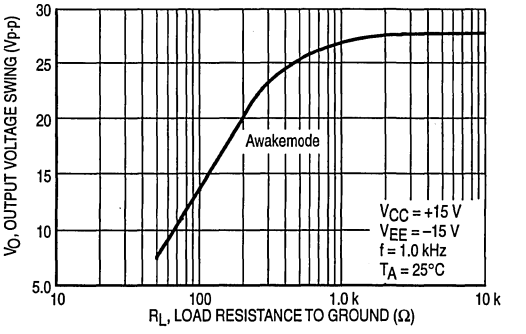


Figure 11. Common Mode Rejection versus Frequency

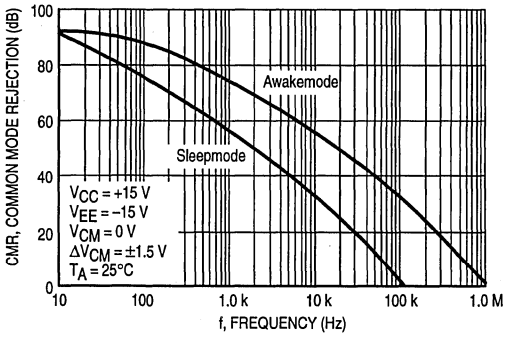


Figure 12. Power Supply Rejection versus Frequency

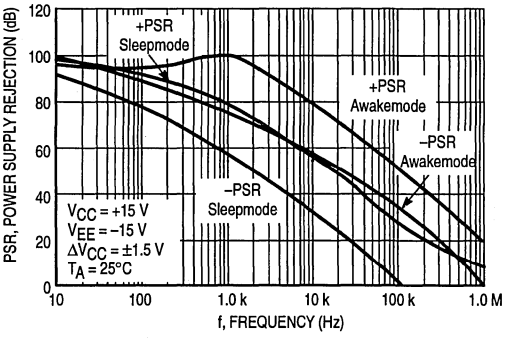


Figure 13. Sleepmode to Awakemode Current Threshold versus Supply Voltage

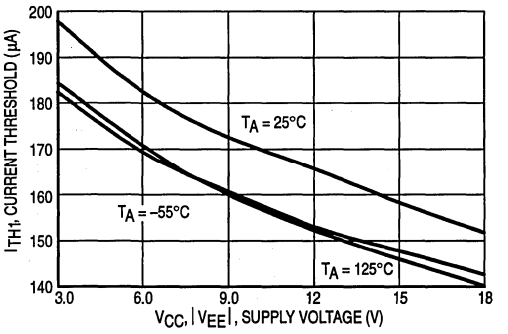


Figure 14. Awakemode to Sleepmode Current Threshold versus Supply Voltage

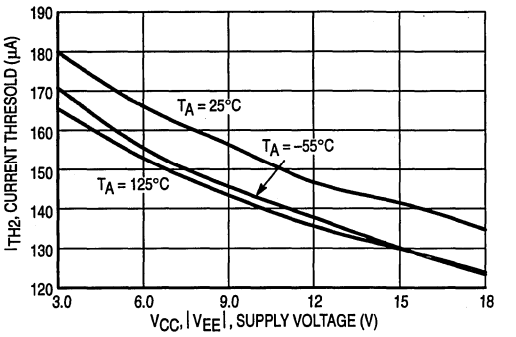


Figure 15. Output Short Circuit Current versus Output Voltage

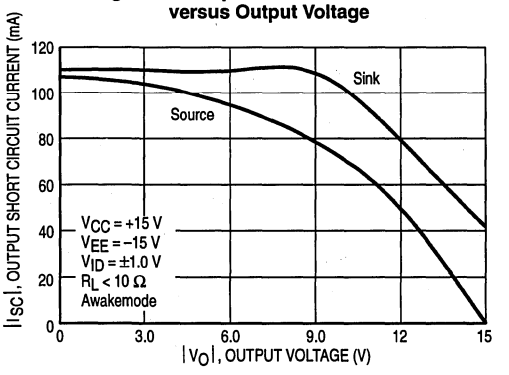


Figure 16. Output Short Ciruit Current versus Temperature

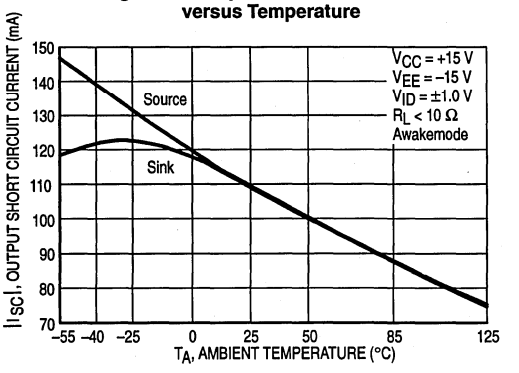


Figure 17. Power Supply Current Per Amplifier versus Temperature

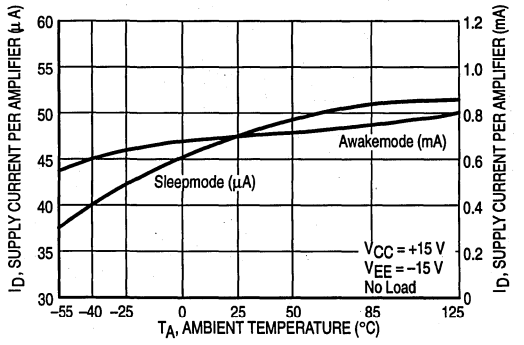


Figure 18. Slew Rate versus Temperature

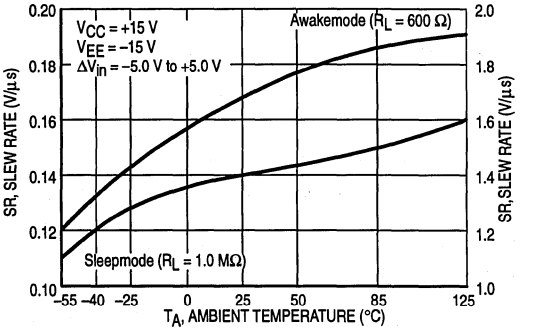


Figure 19. Gain Bandwidth Product versus Temperature

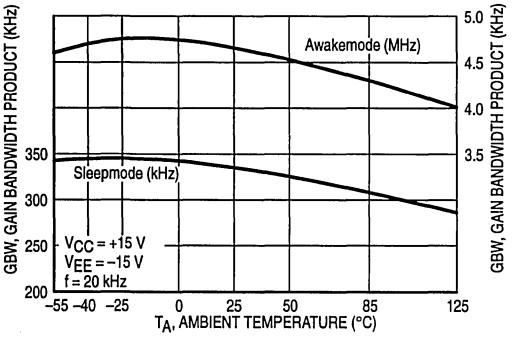


Figure 20. Sleepmode to Awakemode Transition Time

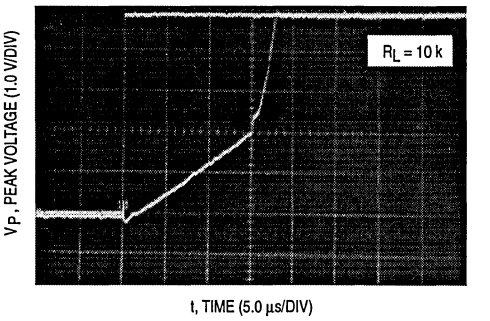


Figure 21. Sleepmode to Awakemode Transition Time

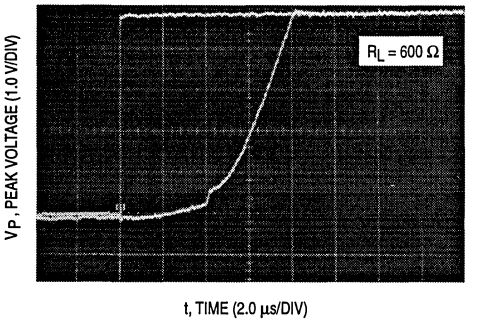


Figure 22. Awakemode to Sleepmode Transition Time versus Supply Voltage

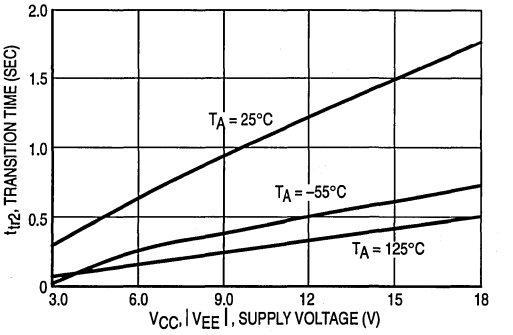


Figure 23. Gain Margin versus Differential Source Resistance

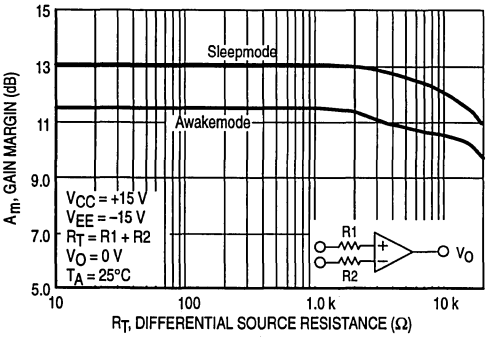


Figure 24. Phase Margin versus Differential Source Resistance

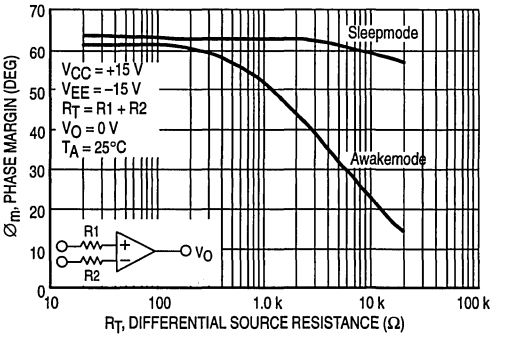


Figure 25. Open-Loop Gain Margin versus Output Load Capacitance

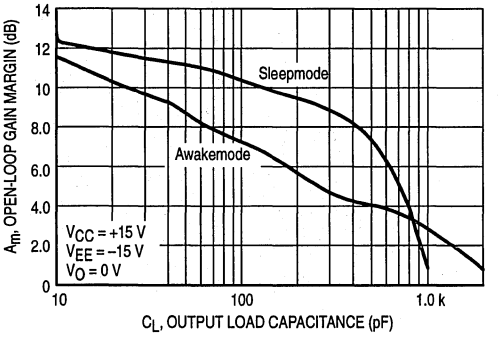


Figure 26. Phase Margin versus Output Load Capacitance

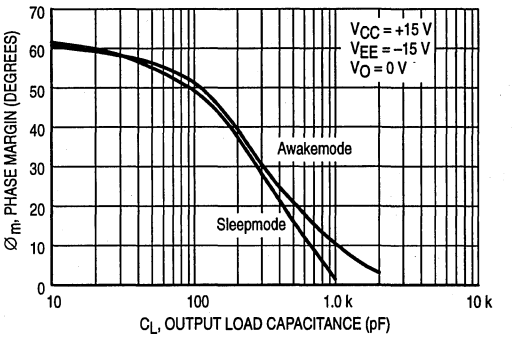


Figure 27. Sleepmode Voltage Gain and Phase versus Frequency

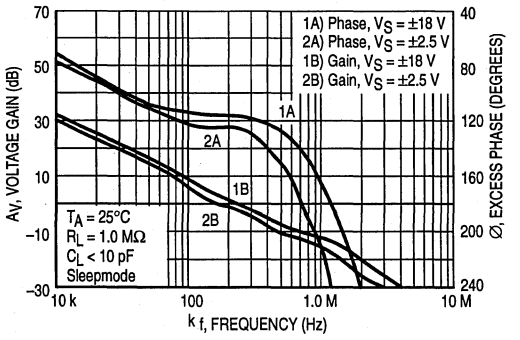


Figure 28. Awakemode Voltage Gain and Phase versus Frequency

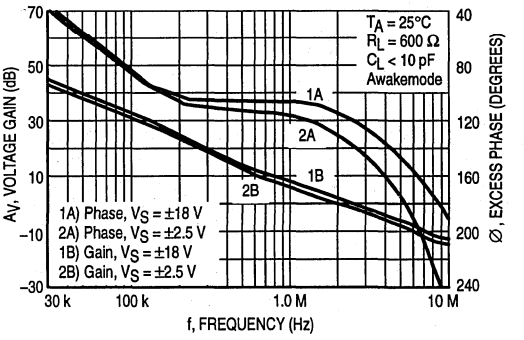


Figure 29. Channel Separation versus Frequency

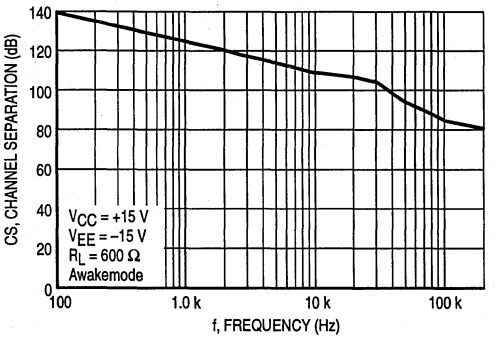


Figure 30. Total Harmonic Distortion versus Frequency

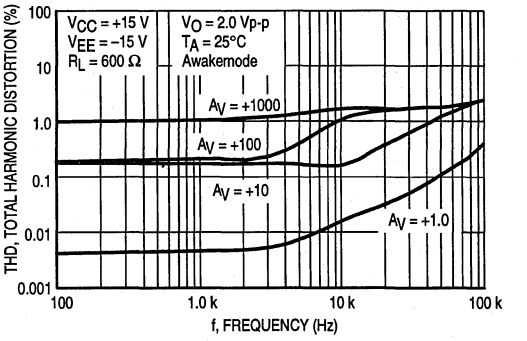


Figure 31. Awakemode Output Impedence versus Frequency

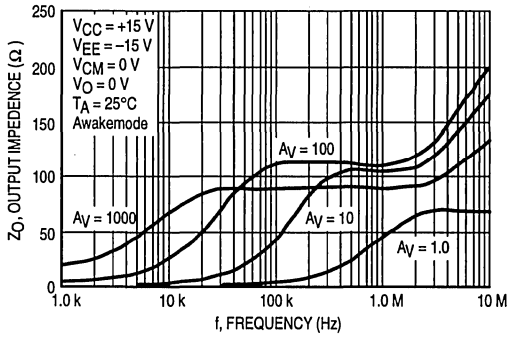


Figure 32. Input Referred Noise Voltage versus Frequency

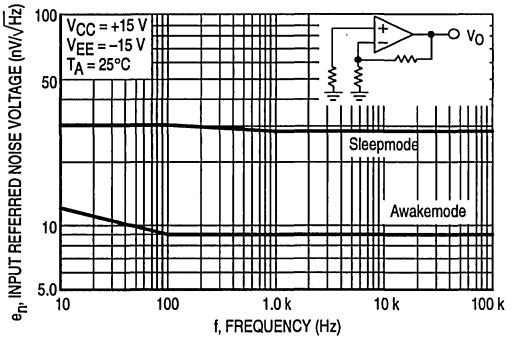


Figure 33. Current Noise versus Frequency

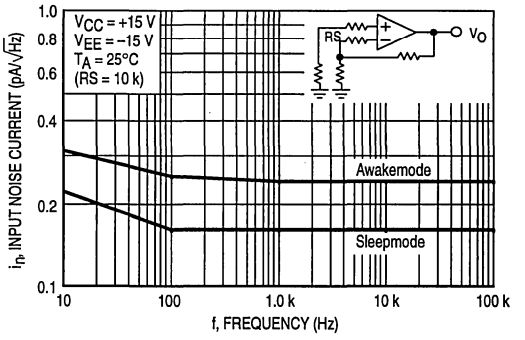


Figure 34. Percent Overshoot versus Load Capacitance

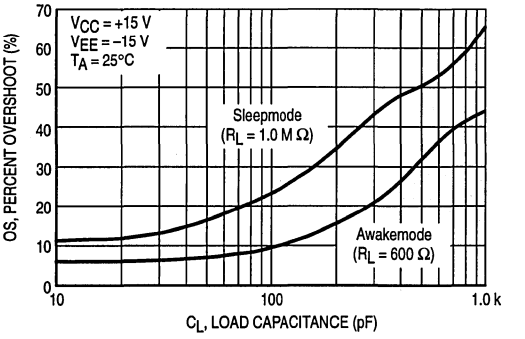


Figure 35. Sleepmode Large Signal Transient Response

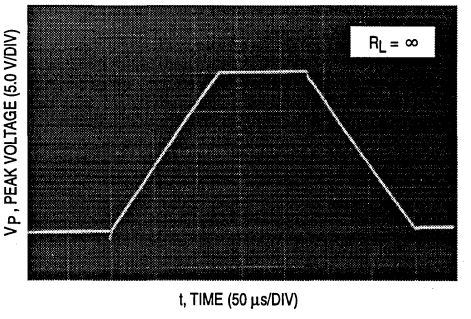


Figure 36. Awakemode Large Signal Transient Response

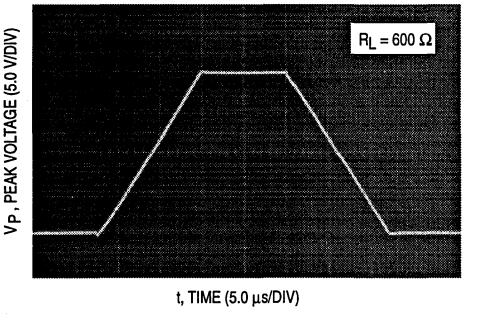


Figure 37. Sleepmode Small Signal Transient Response

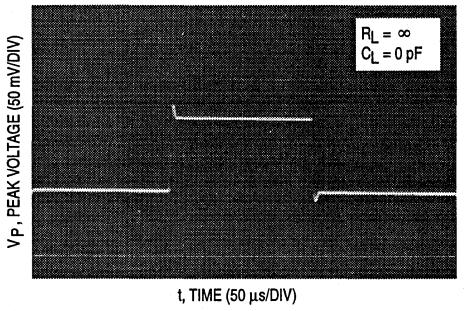
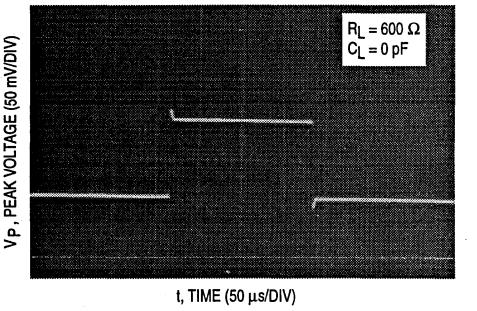


Figure 38. Awakemode Small Signal Transient Response



CIRCUIT INFORMATION

The MC33102 was designed primarily for applications where high performance (which requires higher current drain) is required only part of the time. The two-state feature of this op amp enables it to conserve power during idle times, yet to be powered up and ready for an input signal. Possible applications include laptop computers, automotive, cordless phones, baby monitors, and battery operated test equipment. Although most applications will require low power consumption, this device can be used in any application where better efficiency and higher performance is needed.

The Sleep-Mode™ amplifier has two states; a sleepmode and an awakemode. In the sleepmode state the amplifier is active and functions as a typical micropower op amp. When a signal is applied to the amplifier causing it to source or sink sufficient current (see Figure 13), the amplifier will automatically switch to the awakemode. See Figures 20 and 21 for transition times with 600 Ω and 10 kΩ loads.

The awakemode uses higher drain current to provide a high slew rate, gain bandwidth, and output current capability. In the awakemode, this amplifier can drive 27 Vp-p into a 600 Ω load with $V_S = \pm 15$ V.

An internal delay circuit is used to prevent the amplifier from returning to the sleepmode at every zero crossing. This delay circuit also eliminates the crossover distortion commonly found in micropower amplifiers. This amplifier can process frequencies as low as 1.0 Hz without the amplifier returning to sleepmode, depending on the load.

The first stage PNP differential amplifier provides low noise performance in both the sleep and awake modes, and an all NPN output stage provides symmetrical source and sink AC frequency response.

APPLICATIONS INFORMATION

The MC33102 will begin to function at power supply voltages as low as $V_S = \pm 1.0$ V at room temperature. (At this voltage, the output voltage swing will be limited to a few hundred millivolts). The input voltages must range between V_{CC} and V_{EE} supply voltages as shown in the maximum rating table. Specifically, **allowing the input to go more negative than 0.3 V below V_{EE} may cause product damage.** Also, exceeding the input common mode voltage range on either input may cause phase reversal, even if the inputs are between V_{CC} and V_{EE}.

When power is initially applied, the part may start to operate in the awakemode. This is because of the currents generated due to charging of internal capacitors. When this occurs and the sleepmode state is desired, the user will have to wait approximately 1.5 seconds before the device will switch back to the sleepmode. To prevent this from occurring, ramp the power supplies from 1.0 V to full supply. Notice that the device is more prone to switch into the awakemode when V_{EE} is adjusted than with a similar change in V_{CC}.

The amplifier is designed to switch from sleepmode to awakemode whenever the output current exceeds a preset current threshold (I_{TH}) of approximately 160 µA. As a result, the output switching threshold voltage (V_{ST}) is controlled by the output loading resistance (R_L). This loading can be a load resistor, feedback resistors, or both. Then:

$$V_{ST} = (160\ \mu A) * R_L$$

Large valued load resistors require a large output voltage to switch, but reduce unwanted transitions to the awakemode. For instance, in cases where the amplifier is connected with a large closed-loop gain (A_{CL}), the input offset voltage (V_{IO}) is multiplied by the gain at the output and could produce an output voltage exceeding V_{ST} with no input signal applied.

Small values of R_L allow rapid transition to the awakemode because most of the transition time is consumed slewing in the sleepmode until V_{ST} is reached (see Figures 20, 21). The output switching threshold voltage V_{ST} is higher for larger values of R_L, requiring the amplifier to slew longer in the slower sleepmode state before switching to the awakemode.

The transition time (t_{tr1}) required to switch from sleep to awake mode is:

$$t_{tr1} = t_D + I_{TH} (R_L/SR_{sleepmode})$$

where: t_D = Amplifier delay (<1.0 μs)
I_{TH} = Output threshold current for mode transition (160 μA)
R_L = Load resistance
$SR_{sleepmode}$ = Sleepmode slew rate (0.16 V/μs)

Although typically 160 μA, I_{TH} varies with supply voltage and temperature. In general, any current loading on the output which causes a current greater than I_{TH} to flow will switch the amplifier into the awakemode. This includes transition currents such as that generated by charging load capacitances. In fact, the maximum capacitance that can be driven while attempting to remain in the sleepmode is approximately 1000 pF.

$$C_{L(max)} = I_{TH}/SR_{sleepmode}$$
$$= 160\ \mu A/(0.16\ V/\mu s)$$
$$= 1000\ pF$$

Any electrical noise seen at the output of the MC33102 may also cause the device to transition to the awakemode. To minimize this problem, a resistor may be added in series with the output of the device (inserted as close to the device as possible) to isolate the op amp from both parasitic and load capacitance.

The awakemode to sleepmode transition time is controlled by an internal delay circuit, which is necessary to prevent the amplifier from going to sleep during every zero crossing. This time is a function of supply voltage and temperature as shown in Figure 22.

Gain bandwidth product (GBW) in both modes is an important system design consideration when using a sleepmode amplifier. The amplifier has been designed to obtain the maximum GBW in both modes. "Smooth" AC transitions between modes with no noticeable change in the amplitude of the output voltage waveform will occur as long as the closed-loop gains (A_{CL}) in both modes are substantially equal at the frequency of operation. For smooth AC transitions:

$$(A_{CLsleepmode})\ (BW) < GBW_{sleepmo}$$

where: $A_{CLsleepmode}$ = Closed-loop gain in the sleepmode
BW = The required system bandwidth or operating frequency

TESTING INFORMATION

To determine if the MC33102 is in the awakemode or the sleepmode, the power supply currents (I_{D}+ and I_{D}-) must be measured. When the magnitude of **either** power supply current exceeds 400 μA the device is in the awakemode. When the magnitudes of both supply currents are less than 400 μA, the device is in the sleepmode. Since the total supply current is typically ten times higher in the awakemode than the sleepmode, the two states are easily distinguishable.

The measured value of I_{D}+ equals the I_D of both devices (for a dual op amp) plus the output source current of device A and the output source current of device B. Similarly, the measured value of I_{D}- is equal to the I_{D}- of both devices plus the output sink current of each device. I_{out} is the sum of the currents caused by both the feedback loop and load resistance. The total I_{out} needs to be subtracted from the measured I_D to obtain the correct I_D of the dual op amp.

An accurate way to measure the awakemode I_{out} current on automatic test equipment is to remove the I_{out} current on both Channel A and B. Then measure the I_D values before the device goes back to the sleepmode state. The transition will take typically 1.5 seconds with ±15 V power supplies.

The large signal sleepmode testing in the characterization was accomplished with a 1.0 MΩ load resistor which ensured the device would remain in sleepmode despite large voltage swings.

MC33110

Low Voltage Compander

The MC33110 contains two variable gain circuits configured for compressing and expanding the dynamic range of an audio signal. One circuit is configured as an expander, while the other circuit can be configured as a compressor or expander. Each circuit has a full wave rectifier to provide average value information to a variable gain cell located in either the input stage or the feedback path. An internal, temperature stable bandgap reference provides the necessary precision voltages and currents required.

The MC33110 will operate from a supply voltage of 2.1 to 7.0 V, over a temperature range of −40° to +85°C. The device is designed to accommodate an 80 dB dynamic range from −60 dB to +20 dB, referenced to 100 mVrms.

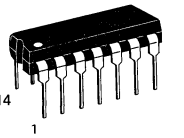
Applications include cordless telephone, CB, walkie-talkie, most voice RF links, and any application where the signal-to-noise ratio can be improved by reducing the transmitted dynamic range. Other applications include speakerphone and voice activated intercom, dictating machine, standard telephone, etc.

The MC33110 is packaged in a 14 pin DIP for through-the-hole applications and an SO-14 surface mount.

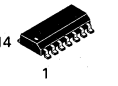
- Operating Supply Voltage: 2.1 to 7.0 V
- No Precision External Components Required
- 80 dB Dynamic Range Compressed to 40 dB, Re-expandable to 80 dB
- Unity Gain Level: 100 mVrms
- Adjustable Response Time
- Ambient Operating Temperature: −40° to +85°C
- Temperature Compensated Reference
- Applications Include Cordless Phone, CB Radio, Speakerphone, etc.

LOW VOLTAGE COMPANDER

SILICON MONOLITHIC INTEGRATED CIRCUIT

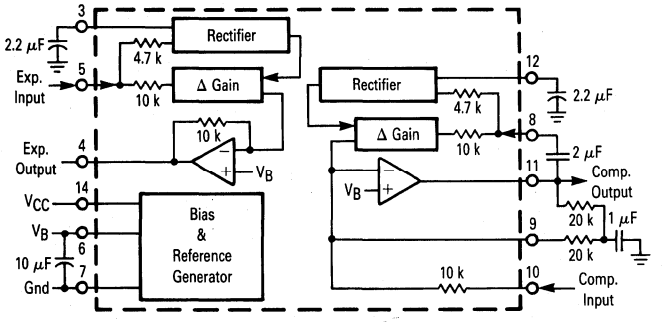


P SUFFIX
PLASTIC PACKAGE
CASE 646

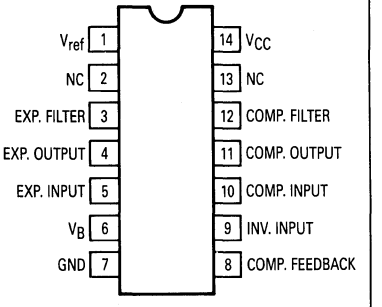


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

SIMPLIFIED BLOCK DIAGRAM



PIN CONNECTIONS
(TOP VIEW)



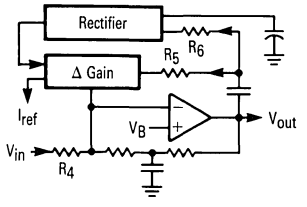
ORDERING INFORMATION

Device	Temperature Range	Package
MC33110D MC33110P	−40°C to +85°C	SO-14 Plastic DIP

PIN DESCRIPTION

Name	Pin	Description
V_{ref}	1	Normally this pin is not used and is left open. It can be used to make limited adjustments to the 0 dB level. Any noise or leakage at this pin will affect the 0 dB level and gain tracking.
NC	2, 13	No connection. These pins are not internally connected.
Expander Filter	3	Connect to an external capacitor to filter the full wave rectifier's output. This capacitor affects attack and decay times, as well as low frequency accuracy.
Expander Output	4	Output of the expander amplifier.
Expander Input	5	The input impedance is nominally 3.2 kΩ. Nominal signal range is 3.16 mVrms to 316 mVrms. Must be capacitor coupled to the signal source.
V_B	6	An internal reference voltage, nominally $V_{CC}/2$. This is an AC ground and must be well filtered to obtain high power supply rejection and low crosstalk.
Ground	7	Connect to a clean power supply ground.
Compressor Feedback	8	Input to the compressor variable gain stage and rectifier. Normally the signal is supplied by the compressor's output (Pin 11). Input impedance is nominally 3.2 kΩ.
Inverting Input	9	Inverting input to the compressor amplifier. Normally, this is connected to the compressor's output through a filtered DC feedback path.
Compressor Input	10	The input impedance is nominally 10 kΩ. Nominal signal range is 100 μVrms to 1.0 Vrms. Must be capacitor coupled to the signal source.
Compressor Output	11	Output of the compressor amplifier.
Compressor Filter	12	Connect to an external capacitor to filter the full wave rectifier's output. This capacitor affects attack & decay times, and low frequency accuracy.
V_{CC}	14	Power supply pin. Connect to a power supply providing between 2.1 V and 7.0 V. Nominal current consumption is 3.5 mA.

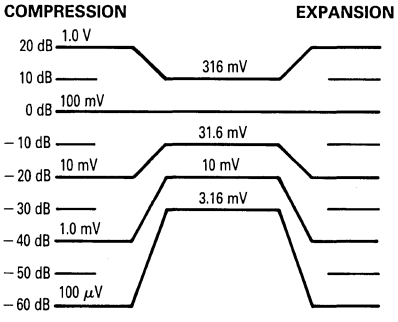
COMPRESSOR



$$V_{out} = \sqrt{\frac{R_5 \times R_6 \times I_{ref} \times V_{in}}{7.2 \times R_4}}$$

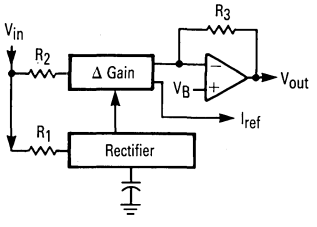
$$= 0.3162 \times \sqrt{V_{in}}$$

TRANSFER FUNCTIONS



(VOLTAGES ARE RMS)

EXPANDER



$$V_{out} = \frac{7.2 \times R_3 \times V_{in}^2}{R_1 \times R_2 \times I_{ref}}$$

$$= 10 \times V_{in}^2$$

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Supply Voltage	V_{CC}	+12, −0.5	Vdc
High Input Voltage (Pin 5 & 10)	V_{IH}	V_{CC} + 0.5	Vdc
Low Input Voltage	V_{IL}	−0.5	Vdc
Output Source Current (Pin 4 & 11)	I_{O+}	Self-Limiting	
Output Sink Current	I_{O-}	20	mA
Junction Temperature	T_J	−65, +150	°C

Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage	V_{CC}	2.1	—	7.0	Vdc
Input Voltage Range	V_{IR}				Vrms
Compressor, 2.1 V < V_{CC} < 7.0 V		0	—	1.0	
Expander, V_{CC} = 2.1 V		0	—	0.25	
Expander, 3.0 V < V_{CC} < 7.0 V		0	—	0.316	
Input Frequency	F_{in}	100	—	20 k	Hz
Output Load	R_L				Ω
Compressor (Pin 11, V_O = 100 mV)		300	—	∞	
Expander (Pin 4, V_O = 100 mV)		150	—	∞	
Ambient Temperature	T_A	−40	—	+85	°C

All limits are not necessarily functional concurrently.

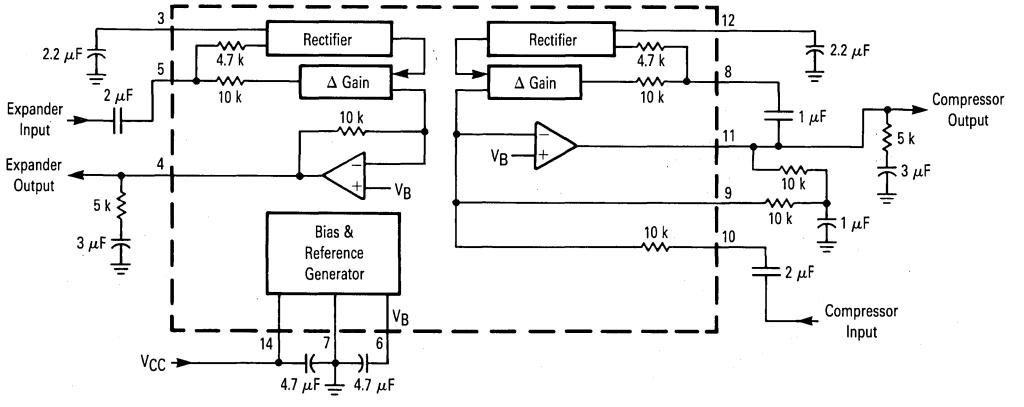
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, f = 1.0 kHz, unless otherwise noted, T_A = 25°C, see Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Power Supply Current	I_{CC}				mA
V_{CC} = +5.0 V		—	3.5	5.5	
V_{CC} = +2.1 V		—	3.3	—	
V_B Voltage	V_B				Vdc
V_{CC} = +5.0 V		2.4	2.5	2.6	
2.1 V < V_{CC} < 7.0 V		—	$V_{CC}/2$	—	
COMPRESSOR					
0 dB Gain	$G_{(CO)}$				dB
V_{in} = 100 mVrms, Pin 1 = Open		−1.5	0	1.5	
Gain Tracking	G_t				dB
@ V_{in} = 1.0 Vrms, output relative to $G_{(CO)}$		+9.0	+10	+11	
@ V_{in} = 10 mVrms, output relative to $G_{(CO)}$		—	−10	—	
@ V_{in} = 1.0 mVrms, output relative to $G_{(CO)}$		—	−20	—	
@ V_{in} = 100 μVrms, output relative to $G_{(CO)}$		−31	−30	−29	
Total Harmonic Distortion	THD				%
V_{in} = 100 mVrms, f = 1.0 kHz		0	0.1	1.5	
Power Supply Rejection	PSRR				dB
f = 1.0 kHz, C_{VB} = 10 μF, V_{in} = −20 dB		—	22	—	
Attack Time (Capacitor @ Pin 12 = 2.2 μF)	$t_{a(C)}$	—	6.0	—	ms
Decay Time (Capacitor @ Pin 12 = 2.2 μF)	$t_{d(C)}$	—	20	—	ms
Input Impedance Pin 10	R_{in}	—	10	—	kΩ
Pin 8		—	3.2	—	
Peak Output Current Pin 11	I_{pk}	—	0.3	—	mA
Output Offset	V_{OO}				mVdc
Pin 11, with respect to Pin 6, NO SIGNAL		−150	0	+150	
Change from NO SIGNAL to 1.0 Vrms at Input		—	50	—	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, f = 1.0 kHz, unless otherwise noted, T_A = 25°C, see Figure 1)

Characteristic		Symbol	Min	Typ	Max	Unit
EXPANDER						
0 dB Gain (V_{in} = 100 mVrms, Pin 1 = open)		$G_{(EO)}$	−1.5	0	1.5	dB
Gain Tracking @ V_{in} = 316 mVrms, output relative to $G_{(EO)}$ @ V_{in} = 31.6 mVrms, output relative to $G_{(EO)}$ @ V_{in} = 10 mVrms, output relative to $G_{(EO)}$ @ V_{in} = 3.16 mVrms, output relative to $G_{(EO)}$		G_t	 +19 — — −61	 +20 −20 −40 −60	 +21 — — −59	dB
Total Harmonic Distortion V_{in} = 100 mVrms, f = 1.0 kHz		THD	0	0.06	1.5	%
Power Supply Rejection (f = 1.0 kHz, C_{VB} = 10 μF)		PSRR	—	37	—	dB
Attack Time (Capacitor @ Pin 3 = 2.2 μF)		$t_{a(E)}$	—	19	—	ms
Decay Time (Capacitor @ Pin 3 = 2.2 μF)		$t_{d(E)}$	—	20	—	ms
Input Impedance	Pin 5	R_{in}	—	3.2	—	kΩ
Peak Output Current	Pin 4	I_{pk}	—	1.0	—	mA
Output Offset Pin 4, with respect to Pin 6, NO SIGNAL Change from NO SIGNAL to 316 mVrms at Input		V_{OO}	 −150 —	 0 25	 +150 —	mVdc
MISCELLANEOUS						
Gain (Pin 10 to Pin 4; Pin 11 capacitor coupled to Pin 5) V_{CC} = 7.0 V, V_{in} = 1.0 Vrms V_{CC} = 3.0 V, V_{in} = 1.0 Vrms V_{CC} = 2.1 V, V_{in} = 31.6 mVrms		A_V	 −2.5 −2.5 −2.5	 0 0 0	 +2.5 +2.5 +2.5	dB
Channel Separation Expander to Compressor, output measured at Pin 11 V_{in} @ Pin 5 = 316 mVrms, f = 1.0 kHz V_{in} @ Pin 5 = 316 mVrms, f = 10 kHz		CS	 43 —	 48 68	 — —	dB
Compressor to Expander, output measured at Pin 4 V_{in} @ Pin 10 = 1.0 Vrms, f = 1.0 kHz V_{in} @ Pin 10 = 1.0 Vrms, f = 10 kHz			 65 —	 107 114	 — —	

FIGURE 1 — TEST CIRCUIT



COMPRESSOR

FIGURE 2 — COMPRESSOR TRANSFER CHARACTERISTICS

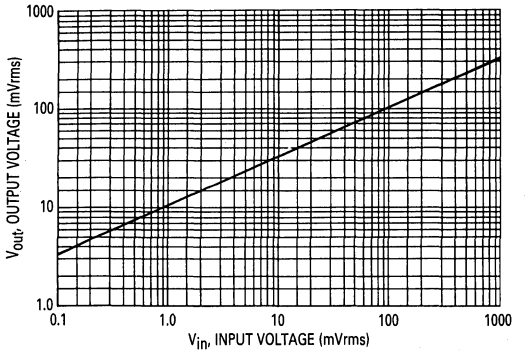


FIGURE 4 — COMPRESSOR TRANSFER CHARACTERISTICS

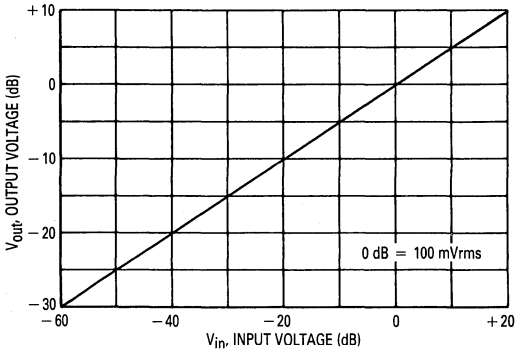
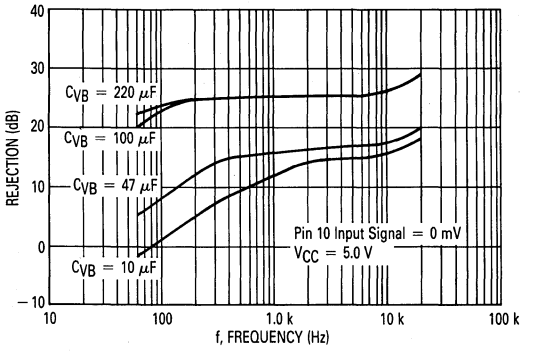


FIGURE 6 — POWER SUPPLY REJECTION (COMPRESSOR)



EXPANDER

FIGURE 3 — EXPANDER TRANSFER CHARACTERISTICS

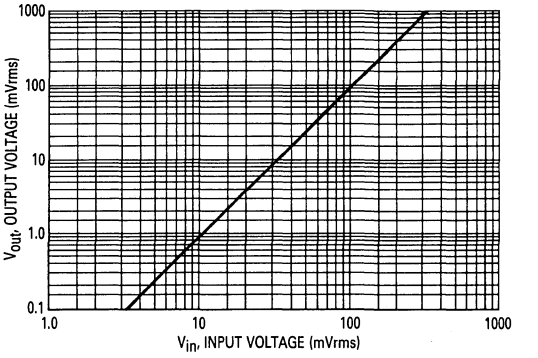


FIGURE 5 — EXPANDER TRANSFER CHARACTERISTICS

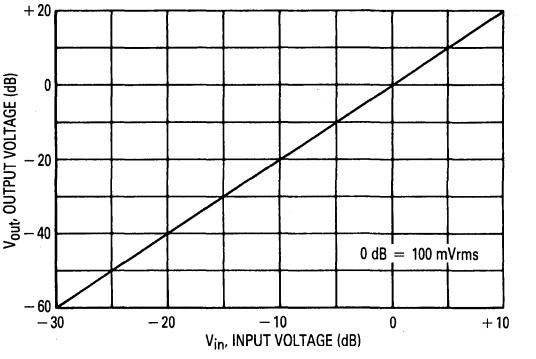
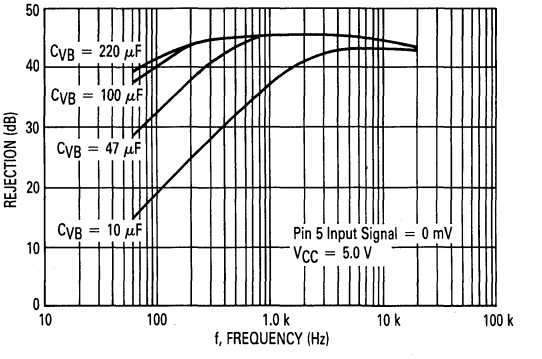
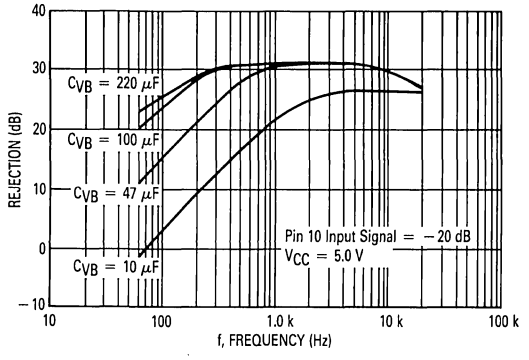


FIGURE 7 — POWER SUPPLY REJECTION (EXPANDER)



COMPRESSOR

FIGURE 8 — POWER SUPPLY REJECTION (COMPRESSOR)



EXPANDER

FIGURE 9 — POWER SUPPLY REJECTION (EXPANDER)

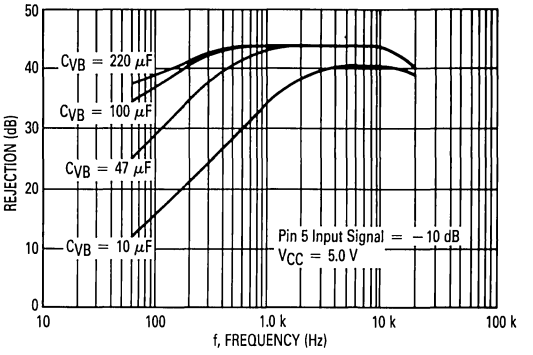


FIGURE 10 — FREQUENCY RESPONSE (COMPRESSOR)

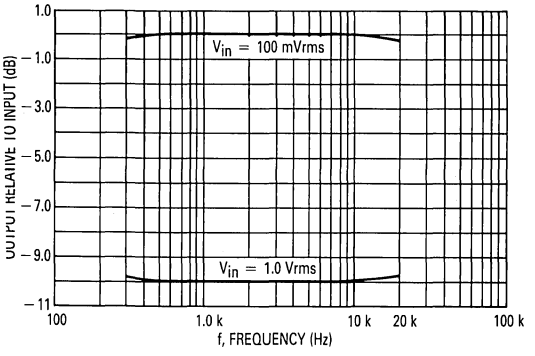


FIGURE 11 — FREQUENCY RESPONSE (EXPANDER)

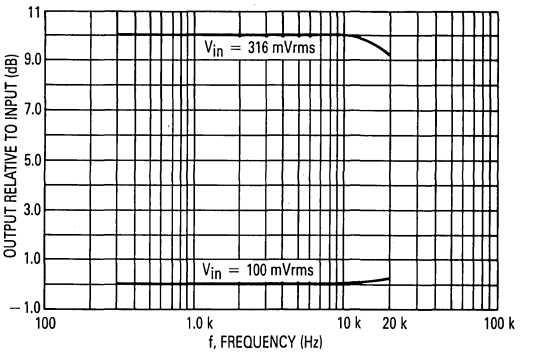


FIGURE 12 — FREQUENCY RESPONSE (COMPRESSOR)

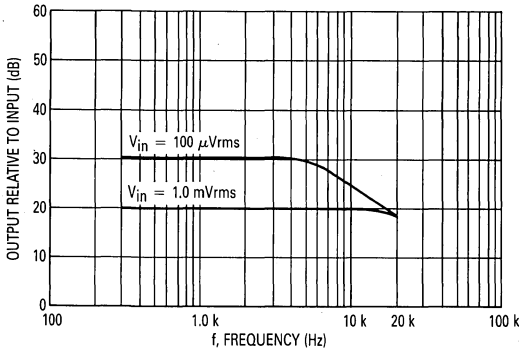


FIGURE 13 — FREQUENCY RESPONSE (EXPANDER)

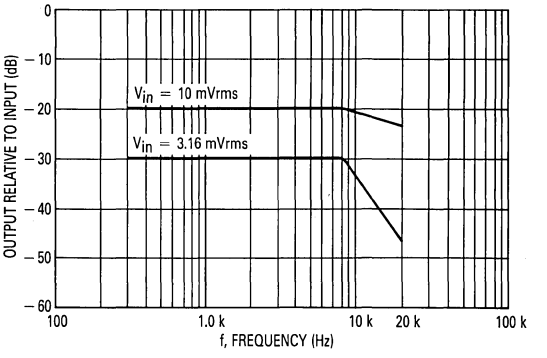


FIGURE 14 — ATTACK AND DECAY TIMES (COMPRESSOR)

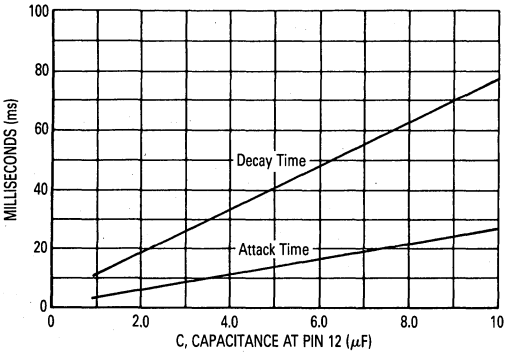


FIGURE 15 — ATTACK AND DECAY TIMES (EXPANDER)

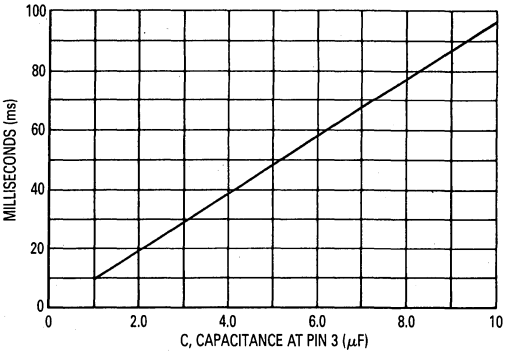
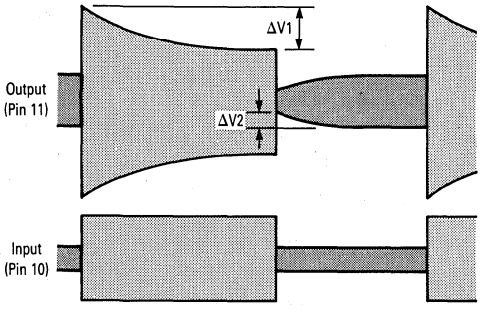
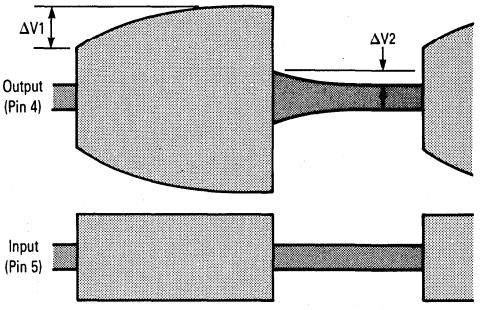


FIGURE 16 — ATTACK AND DECAY TIMES (COMPRESSOR)



Attack Time = Time to 63% of ΔV1.
Decay Time = Time to 63% of ΔV2.

FIGURE 17 — ATTACK AND DECAY TIMES (EXPANDER)



Attack Time = Time to 63% of ΔV1.
Decay Time = Time to 63% of ΔV2.

FIGURE 18 — MAXIMUM INPUT SIGNAL

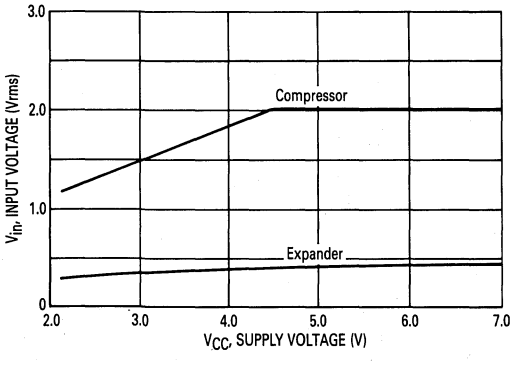
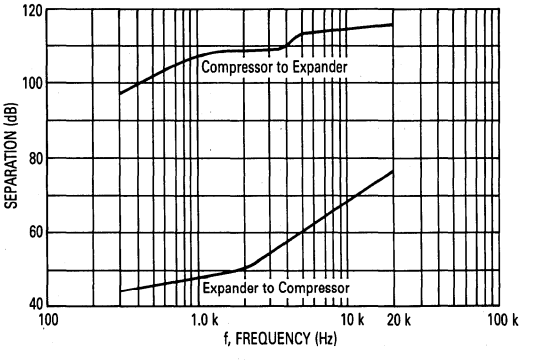
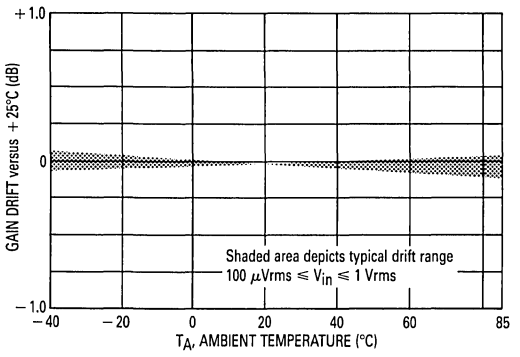


FIGURE 19 — CHANNEL SEPARATION



COMPRESSOR

FIGURE 20 — COMPRESSOR GAIN TRACKING versus TEMPERATURE



EXPANDER

FIGURE 21 — EXPANDER GAIN TRACKING versus TEMPERATURE

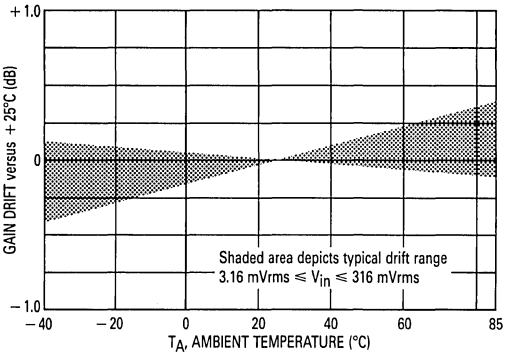


FIGURE 22 — COMPRESSOR THD versus TEMPERATURE

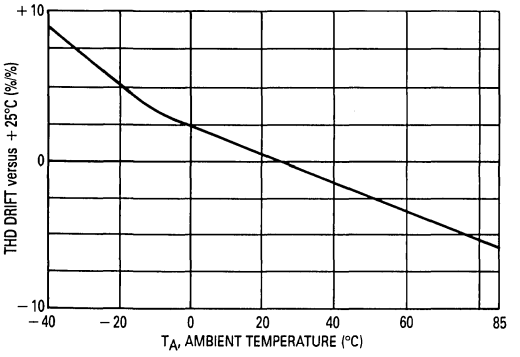
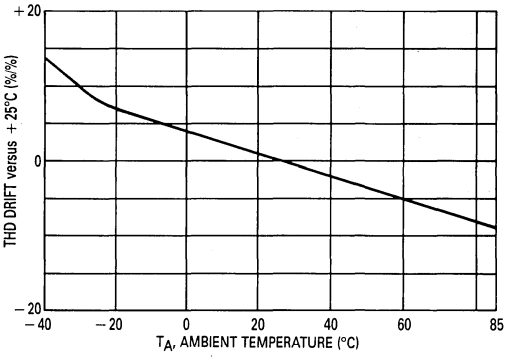


FIGURE 23 — EXPANDER THD versus TEMPERATURE



FUNCTIONAL DESCRIPTION

Introduction

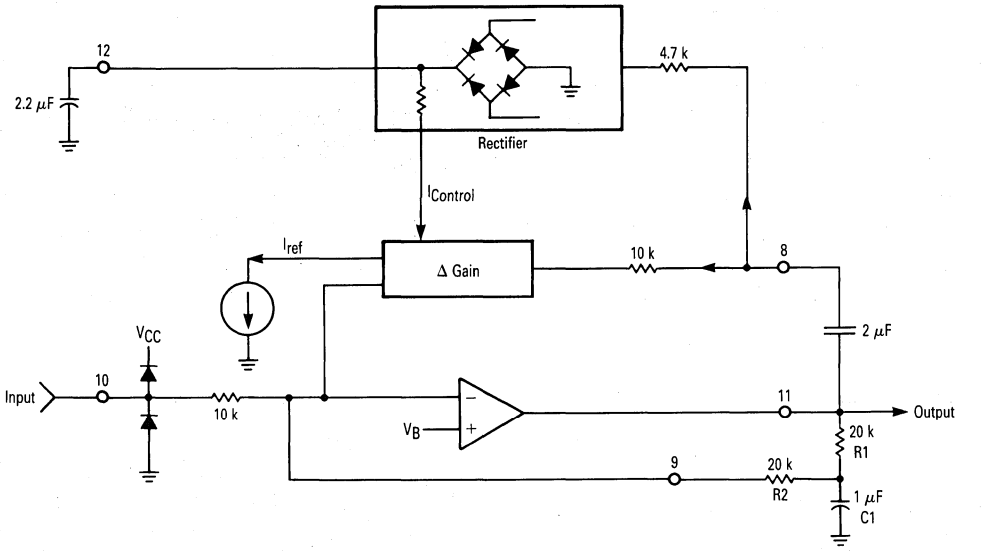
The MC33110 compander (COMpressor and exPANDER) is composed of two variable gain circuits which provide compression and expansion of the signal dynamic range. The compressor will take a signal with an 80 dB dynamic range (100 μV to 1.0 Vrms), and reduce that to a 40 dB dynamic range by attenuating strong signals, while amplifying low level signals. The expander does the opposite in that the 40 dB signal range is increased to a dynamic range of 80 dB by amplifying strong signals and attenuating low level signals. The 0 dB level is internally set at 100 mVrms — that is the signal level which is neither amplified nor attenuated. Both circuits contain the necessary precision full wave rectifier, variable gain cell, and temperature compensated references required for accurate and stable performance.

Note: All dB values mentioned in this data sheet, unless otherwise noted, are referred to 100 mVrms.

Compressor

The compressor is an operational amplifier with a fixed input resistor and a variable gain cell in its feedback path as shown in Figure 24.

FIGURE 24 — COMPRESSOR



The amplifier output is sampled by the precision rectifier which, in turn, supplies a DC signal ($I_{Control}$), representative of the rectifier's AC signal, to the variable gain cell. The reference current (I_{ref}) is an internally generated precision current. The effective impedance of the variable gain cell varies with the ratio of the two currents, and decreases as $I_{Control}$ increases, thereby providing compression. The output is related to the input by the following equation:

$$V_{out} = 0.3162 \times \sqrt{V_{in}} \qquad \text{(Equation 1)}$$

In terms of dB levels, the relationship is:

$$V_{out(dB)} = 0.5 \times V_{in(dB)} \qquad \text{(Equation 2)}$$

where 0 dB = 100 mVrms (see Figure 2 and 4).

The inputs and output are internally biased at V_B ($V_{CC/2}$), and must therefore be capacitor coupled to external circuitry. Pin 10 input impedance is nominally 10 kΩ (±20%), and the maximum functional input signal is shown in Figure 18. Bias currents required by the op amp and the variable gain cell are internally supplied. Due to clamp diodes at the input (to V_{CC} and ground), the input signal must be maintained between the supply rails. If the input signal goes more than 0.5 V above V_{CC} or below ground, excessive currents will flow and distortion will show up at the output.

When no AC signals are present at the input, the variable gain cell will attempt to set such a high gain that the circuit may become unstable. For this reason resistors R1 and R2, and capacitor C1 are added to provide DC stability. The pole formed by R1, R2 and C1 should have a pole frequency no more than 1/10th of the lowest frequency of interest. The pole frequency is calculated from:

$$f = \frac{R_1 + R_2}{2\pi \times R_1 R_2 C_1} \qquad \text{(Equation 3)}$$

for the component values shown, the pole frequency is ≈16 Hz.

Likewise, the capacitor between Pins 11 and 8 should be selected such that, in conjunction with the input impedance at Pin 8 (≈3200 Ω, ±20%), the resulting pole frequency is no more than 1/10 of the lowest frequency of interest. With the components shown, the pole frequency is <30 Hz. This pole frequency is calculated from:

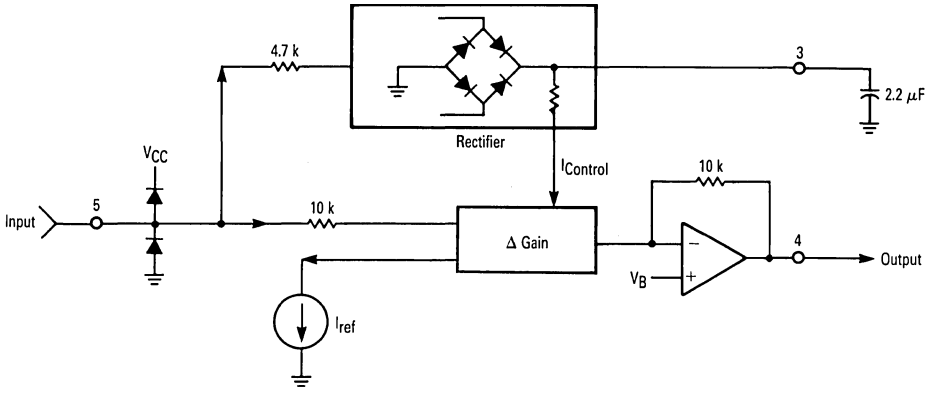
$$f = \frac{1}{2\pi \times 3.2\ k \times C} \qquad \text{(Equation 4)}$$

The output of the rectifier is filtered by the capacitor at Pin 12, which, in conjunction with an internal 10 k resistor, provides the time constant for the attack and decay times. Figure 14 and 16 indicate how the times vary with the capacitor value. The attack time for the compressor is always faster than the decay time due to the fact that the rectifier is fed from the output rather than the input. Since the output is initially larger than expected (immediately after the input has increased), the external capacitor is charged more quickly during the initial part of the time constant. When the input is decreased, the time constant is closer to that calculated by t = RC. If the attack and decay times are decreased by using a smaller capacitor, performance at low frequencies will degrade.

Expander

The expander is an operational amplifier with a fixed feedback resistor and a variable gain cell in its input path as shown in Figure 25.

FIGURE 25 — EXPANDER



The input signal is sampled by the precision rectifier which, in turn, supplies a DC signal ($I_{Control}$), representative of the AC input signal, to the variable gain cell. The reference current (I_{ref}) is an internally generated precision current. The effective impedance of the variable gain cell varies with the ratio of the two currents, and decreases as $I_{Control}$ increases, thereby providing expansion. The output is related to the input by the following equation:

$$V_{out} = 10 \times (V_{in})^2 \qquad \text{(Equation 5)}$$

In terms of dB levels, the relationship is:

$$V_{out(dB)} = 2.0 \times V_{in(dB)} \qquad \text{(Equation 6)}$$

where 0 dB = 100 mVrms (see Figure 3 and 5).

The inputs and output are internally biased at V_B ($V_{CC}/2$), and must therefore be capacitor coupled to external circuitry. The input impedance at Pin 5 is nominally 3.2 kΩ (±20%), and the maximum functional input signal is shown in Figure 18. Bias currents required by the op amp and the variable gain cell are internally supplied. Due to clamp diodes at the input (to V_{CC} and ground), the input signal must be maintained between the supply rails. If the input signal goes more than 0.5 V above V_{CC} or below ground, excessive currents will flow, and distortion will show up at the output.

The output of the rectifier is filtered by the capacitor at Pin 3, which, in conjunction with an internal 10 k resistor, provides the time constant for the attack and decay times. Figure 15 and 17 indicate how the times vary with the capacitor value. If the attack and decay times are decreased by using a smaller capacitor, performance at low frequencies will degrade.

Power Supply

The MC33110 requires a power supply voltage between 2.1 V and 7.0 V, and a nominal current of 3.5 mA. The supply voltage should be well filtered and free of ripple. A minimum of 4.7 μF in parallel with a 0.01 μF capacitor is recommended for filtering and RF bypass.

V_B (Pin 6) is an internally generated mid supply reference, and is used internally as an AC ground. The external capacitor at Pin 6 filters this voltage, and its value affects the power supply noise rejection as shown in Figures 6 through 9. This reference voltage may be used to bias external circuitry as long as the current draw is limited to <10 μA.

APPLICATIONS INFORMATION

Signal-to-Noise Improvement

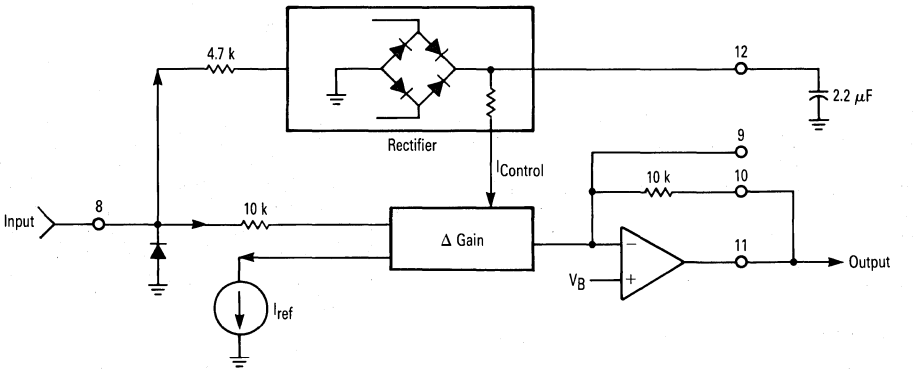
Among the basic reasons for the original development of compander type circuits was to improve the signal-to-noise ratio of long distance telecom circuits, and of voice circuits which are transmitted over RF links (CBs, walkie-talkies, cordless phones, etc.). Since much of the noise heard at the receiving end of a transmission is due to noise picked up, for example, in the airway portion of the RF link, the compressor was developed to increase the low-level signals at the transmitting end. Then any noise picked in the RF link would be a smaller percentage of the transmitted signal level. At the receiving end, the signal is then expanded back to its original level, retaining the same high signal-to-noise ratio. While the above explanation indicates it is not necessary to attenuate strong signals (at the transmitting end), a benefit of doing this is the reduced dynamic range which must be handled by the system transmitter and receiver. The MC33110 was designed for a two-to-one compression and expansion, i.e. an 80 dB dynamic signal is compressed to a 40 dB dynamic range, transmitted to the receiving end and then expanded back to an 80 dB dynamic range.

The MC33110 compander is not limited to RF or long distance telephony applications. It can be used in any system requiring an improved signal-to-noise ratio such as telephones, speakerphones, tape recorders, digital recording, and many others.

Second Expander

Should the application require it, the MC33110 can be configured as two expanders by reconfiguring the compressor side as shown in Figure 26.

FIGURE 26 — SECOND EXPANDER



This circuit will provide the same performance as the expander at Pins 3 through 5.

Power Supplies, Grounding

The PC board layout, the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC} or ground, can cause a distorted output, or incorrect gain level.

V_{CC} must be decoupled to the appropriate ground **at the IC** (within 1" max) with a 4.7 μF capacitor and a 0.01 μF ceramic. A tantalum capacitor is recommended for the larger value if very high frequency noise is present since electrolytic capacitors simply have too much inductance at those frequencies. The quality of the power supply voltage should be checked at the IC with a high frequency scope. Noise spikes (always present if digital circuits are near this IC) can easily exceed 400 mV, and if they get into the IC, the output can have noise or distortion. Noise can be reduced by inserting resistors and/or inductors between the supply and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 V or greater at frequencies of 50 kHz to 1.0 MHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, a three terminal regulator (MC78L05ACP), with appropriate high frequency filtering, should be used and dedicated to the analog portion of the circuit.

The ripple content of the supply should not allow its magnitude to exceed the values in the Recommended Operating Conditions table.

The PC board tracks supplying V_{CC} and ground to the MC33110 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The analog circuitry containing the MC33110 should be close to the power supply, or the connector where the supply voltages enter the board. If V_{CC} is supplying considerable current to other parts of the board, then it is preferable to have dedicated lines from the supply or connector directly to the MC33110 and associated circuitry.

PC Board Layout

Although this device is intended for use in the audio frequency range, the amplifiers have a bandwidth of ≈300 kHz, and can therefore oscillate at frequencies outside the voiceband should there be excessive stray capacitance or other unintended feedback loops. A solid ground plane is strongly recommended to minimize coupling of any digital noise into the analog section. Use of wire wrapped boards should definitely be avoided.

Since many applications of the MC33110 compander involve voice transmission over RF links, care must be taken in the design of the product to keep RF signals out of the MC33110 and associated circuitry. This involves proper layout of the PC boards, the physical arrangement of the boards, shielding, proper RF ground, etc.

GLOSSARY

ATTACK TIME — The settling time for a circuit after its input signal has been increased.

ATTENUATION — A decrease in magnitude of a communication signal, usually expressed in dB.

BANDWIDTH — The range of information carrying frequencies of a communication system.

CHANNEL SEPARATION — The ability of one circuit to reject outputting signals which are being processed by another circuit. Also referred to as crosstalk, it is usually expressed in dB.

COMPANDER — A contraction of the words compressor and expander. A compander is composed of two circuits, one of each kind.

COMPRESSOR — A circuit which compresses or reduces the dynamic range of a signal by attenuating strong signals and amplifying low level signals.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

$10 \times \log (P_1/P_2)$ for power measurements, and
$20 \times \log (V_1/V_2)$ for voltage measurements.

dBm — An indication of signal power. 1.0 mW across 600 Ω or 0.775 V rms, is typically defined as 0 dBm for telecom applications. Any voltage level is converted to dBm by:

$$dBm = 20 \times \log (Vrms/0.775), \text{ or}$$
$$dBm = [20 \times \log (Vrms)] + 2.22.$$

dBrn — Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = −90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

DECAY TIME — The settling time for a circuit after its input signal has been decreased.

EXPANDER — A circuit which expands or increases the dynamic range of a signal by amplifying strong signals and attenuating low level signals.

GAIN — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number and a decrease is a negative number.

POWER SUPPLY REJECTION RATIO — The ability of a circuit to reject outputting noise, or ripple, which is present on the power supply lines. PSRR is usually expressed in dB.

SIGNAL-TO-NOISE RATIO — The ratio of the desired signal to unwanted signals (noise) within a defined frequency range. The larger the number, the better.

VOICEBAND — That portion of the audio frequency range used for transmission across the telephone system. Typically, it is 300 to 3400 Hz.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33120

Subscriber Loop Interface Circuit

SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

THIN FILM SILICON MONOLITHIC INTEGRATED CIRCUIT

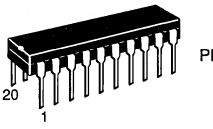
The MC33120 is designed to provide the interface between the 4-wire side of a central office, or PBX, and the 2-wire subscriber line. Interface functions include battery feed, proper loop termination AC impedance, hookswitch detection, adjustable transmit, receive, and transhybrid gains, and single/double fault indication. Additionally the MC33120 provides a minimum of 58 dB of longitudinal balance (4-wire and 2-wire).

The transmit and receive signals are referenced to analog ground, while digital signals are referenced to digital ground, easing the interface to codecs, filters, etc. The 2 status outputs (hookswitch and faults) and the Power Down Input are TTL/CMOS compatible. The Power Down Input permits local shutdown of the circuit.

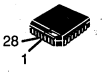
Internal drivers allow the external loop current pass transistors to be standard bipolar transistors (non-Darlington).

The MC33120 is available in a 20 pin DIP and a 28 pin PLCC surface mount package.

- 58 dB Longitudinal Balance Guaranteed; 4-wire and 2-wire
- Transmit, Receive, and Transhybrid Gains Externally Adjustable
- Return Loss Externally Adjustable
- Proper Hookswitch Detection With 30 kΩ Leakage
- Single/Double Fault Indication With Shutdown for Thermal Protection
- Critical Sense Resistors Included Internally
- Standard Power Supplies: – 42 V to – 58 V, and +5.0 V, ±10%
- On-Hook Transmission
- Power Down Input (TTL and CMOS Compatible)
- Operating Ambient Temperature: – 40°C to +85°C
- Available in a 20 Pin DIP and 28 Pin PLCC Package



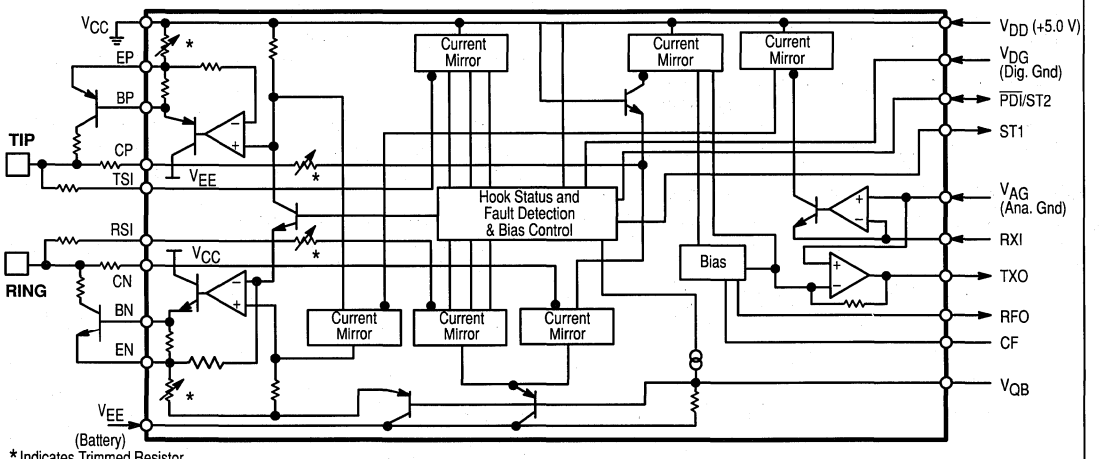
P SUFFIX
PLASTIC PACKAGE
CASE 738



FN SUFFIX
PLCC
CASE 776

ORDERING INFORMATION		
Device	**Temperature Range**	**Package**
MC33120P	– 40° to +85°C	Plastic DIP
MC33120FN		PLCC

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage with respect to V_{CC} with respect to V_{DG}	 V_{EE} V_{DD}	 – 60, +0.5 – 0.5, +7.0	Vdc
Input Voltage @ PDI, with respect to V_{DG} @ Pins 1–5, 16–20	V_{in}	 – 0.5, +7.0 V_{EE} to V_{CC}	Vdc
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Junction Temperature	T_J	150	°C

Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage (with respect to V_{CC}) (with respect to V_{DG})	 V_{EE} V_{DD}	 – 58 +4.5	 – 48 +5.0	 – 42 +5.5	Vdc
(with respect to V_{CC}) (with respect to V_{CC}) (with respect to V_{AG})	V_{AG} V_{DG}	– 3.0 – 3.0 – 3.0	0 0 0	+10 +7.0 +10	Vdc
(with respect to V_{EE}) (with respect to V_{CC} and V_{AG})	V_{DD}	— +3.5	— —	+63.5 —	Vdc
Loop Current	I_{LOOP}	15	—	50	mA
PDI Input Voltage	V_{PDI}	0	—	V_{DD}	Vdc
Sink Current ST1 ST2	 I_{ST1L} I_{ST2L}	 0 0	 — —	 1.0 1.0	mA
Transmit Signal Level at Tip & Ring Receive Signal Level at V_{RX}	S_{TX} S_{RX}	– 48 – 48	— —	+3.0 +3.0	dBm
Loop Resistance	R_L	0	—	2.0	kΩ
External Transistor Beta	H_{FE}	40	—	500	A/A
Operating Ambient Temperature (See text for derating)	T_A	– 40	—	+85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (V_{EE} = – 48 V, V_{DD} = +5.0 V, unless otherwise noted, V_{CC} = V_{AG} = V_{DG} = 0 V, T_A = 25°C, see Figure 1, unless otherwised noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLIES					
V_{EE} Current On Hook (R_L > 10 MΩ, V_{EE} = – 58 V) Off Hook (R_L = 0 Ω, V_{EE} = – 58 V)* V_{DD} Current On Hook (R_L > 10 MΩ, V_{DD} = +5.5 V) Off Hook (R_L = 0 Ω, V_{DD} = +5.5 V)	 I_{EEN} I_{EEF} I_{DDN} I_{DDF}	 – 2.7 – 75 — 5.5	 – 1.2 – 58 1.4 9.0	 — – 45 2.7 15	mA
V_{EE} Ripple Rejection f = 1.0 kHz, at V_{TX} (4-wire) f = 1.0 kHz, at Tip/Ring (2-wire) V_{DD} Ripple Rejection f = 1.0 kHz, at V_{TX} (4-wire) f = 1.0 kHz, at Tip/Ring (2-wire)	PSRR 	 40 40 37 37	 62 52 52 48	 — — — —	dB

*Includes loop current.

ELECTRICAL CHARACTERISTICS (V_{EE} = – 48 V, V_{DD} = +5.0 V, unless otherwise noted, V_{CC} = V_{AG} = V_{DG}, T_A = 25°C, see Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
LOOP FUNCTIONS					
Loop Current					mA
Maximum (RRF = 4.7 k, R_L = 10 Ω)	I_{LMAX}	41	43	53	
Nominal (RRF = 4.7 k, R_L = 600 Ω)	I_{LOOP}	37	40	48	
Minimum (RRF = 4.7 k, R_L = 1800 Ω)	I_{LMN}	19	21	—	
Battery Feed Resistance (RRF = 4.7 k, R_L = 1800 Ω)*	R_{BF}	475	508	675	Ω
Hookswitch Threshold					kΩ
On-to-Off Hook	R_{NF}	2.0	3.1	—	
Off-to-On Hook	R_{FN}	—	7.0	10	
Fault Detection Threshold					Ω
Ring-to-Ground (R_L = 600 Ω)	R_{RG}	600	660	—	
Tip-to-Battery (R_L = 600 Ω)	R_{TB}	600	660	—	

*Calculated from [(48/I_{LMN}) – 1800]

GAIN LEVELS

Transmit Voltage Gain (CP, CN to TXO)	G_{TX1}	—	0.328	—	V/V
Transmit Voltage Gain (V_{TX}/V_L)					dB
V_L = 0 dBm, f = 1.0 kHz	G_{TX2}	– 0.3	0.0	+0.3	
V_L = 0 dBm, f = 3.4 kHz, with respect to G_{TX2}		– 0.1	0.0	+0.1	
V_L = +3.0 dBm, f = 1.0 kHz, with respect to G_{TX2}		– 0.15	0.0	+0.15	
V_L = – 48 dBm, f = 1.0 kHz, with respect to G_{TX2}		—	±0.1	—	
Transmit Distortion (at Pin 11)	THD_T				%
(f = 300 Hz to 4.0 kHz, – 40 dBm ≤ V_{T-R} ≤ +5.0 dBm)		—	0.05	—	
Receive Current Gain (I_{EP}/I_{RXI})	G_{RX1}	94	102	110	mA/mA
Receive Voltage Gain (V_L/V_{RXI}) (R_L = 600 Ω)					dB
V_{RXI} = 0 dBm, f = 1.0 kHz	G_{RX2}	– 0.3	0.0	+0.3	
V_{RXI} = 0 dBm, f = 3.4 kHz, with respect to G_{RX2}		– 0.1	0.0	+0.1	
V_{RXI} = +3.0 dBm, f = 1.0 kHz, with respect to G_{RX2}		– 0.15	0.0	+0.15	
V_{RXI} = – 48 dBm, f = 1.0 kHz, with respect to G_{RX2}		—	±0.1	—	
Receive Distortion	THD_R	—	0.05	—	%
(f = 300 Hz to 4.0 kHz, – 40 dBm ≤ V_{RXI} ≤ +5.0 dBm)					
Return Loss (Reference = 600 Ω resistive, f = 1.0 kHz)	RL	30	>40	—	dB
Transhybrid Rejection (R_L = 600 Ω, f = 1.0 kHz, Figure 4)	THR	—	44	—	dB

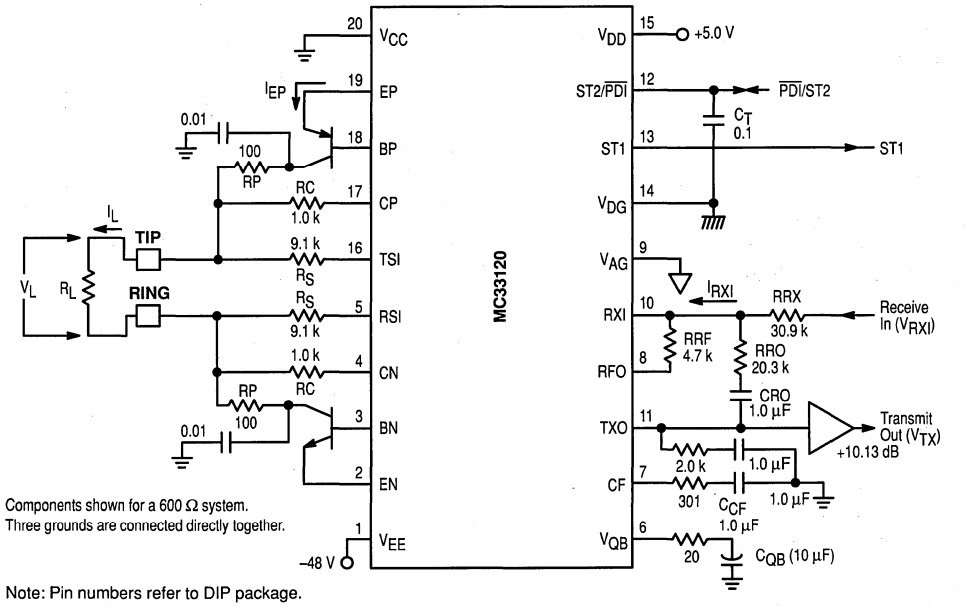
LONGITUDINAL SIGNALS (V_{CM} = 5.12 Vrms, see Figures 1 and 2)

2-Wire Balance, f = 1.0 kHz, Z_{ac} = 600 Ω (@ Tip/Ring)	LB	58	64	—	dB
4-Wire Balance, f = 1.0 kHz, Z_{ac} = 600 Ω (@ V_{TX})		58	64	—	
2-Wire Balance, f = 330 Hz, Z_{ac} = 600 Ω (@ Tip/Ring)		58	64	—	
4-Wire Balance, f = 330 Hz, Z_{ac} = 600 Ω (@ V_{TX})		58	64	—	
2-Wire Balance, f = 3.3 kHz, Z_{ac} = 600 Ω (@ Tip/Ring)		53	60	—	
4-Wire Balance, f = 3.3 kHz, Z_{ac} = 600 Ω (@ V_{TX})		53	60	—	
2-Wire Balance, f = 1.0 kHz, Z_{ac} = 900 Ω (@ Tip/Ring)		—	62	—	
4-Wire Balance, f = 1.0 kHz, Z_{ac} = 900 Ω (@ V_{TX})		—	62	—	
Signal Balance, f = 1.0 kHz (Figure 3)		40	55	—	
Longitudinal Impedance, RS = 9100 Ω	Z_{LONG}	150	180	210	Ω
Maximum Longitudinal Current per side	I_{LM}				mA
f = 1.0 kHz, I_{LOOP} = I_{LMN}, C_T = 0.1 μF		8.5	16	—	

ELECTRICAL CHARACTERISTICS (V_{EE} = – 48 V, V_{DD} = +5.0 V, unless otherwise noted, $V_{CC} = V_{AG} = V_{DG}$, T_A = 25°C, see Figure 1)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INTERFACE					
ST1 Output Voltage					Vdc
Low (I_{ST1} = 1.0 mA, V_{DD} = 5.5 V)	V_{OL}	V_{DG}	0.17	0.4	
High (I_{ST1} = – 100 µA, V_{DD} = 4.5 V)	V_{OH}	2.4	3.2	—	
ST2 Output Voltage					
Low (I_{ST2} = 1.0 mA, V_{DD} = 5.5 V)	V_{OL}	V_{DG}	0.17	0.4	
High (I_{ST2} = – 100 µA, V_{DD} = 4.5 V)	V_{OH}	2.4	4.3	—	
Time Delay					µs
Hookswitch Closure to ST1 Change	t_{ST11}	—	10	—	
Hookswitch Opening to ST1 Change	t_{ST12}	—	200	—	
Hookswitch Closure to 90% of Loop Current (C_T = 0.1 µF)	t_{HS}	—	19	—	ms
PDI Taken High-to-Low to 10% of Loop Current	t_{ST21}	—	18	—	ms
PDI Taken Low-to-High to 90% of Loop Current	t_{ST22}	—	10	—	µs
PDI Input Current	I_{IH}				µA
V_{PDI} = 3.0 V, R_L = 600 Ω, V_{DD} = 5.0 V		– 1250	– 800	– 300	
V_{PDI} = 0 V, R_L = 600 Ω, V_{DD} = 5.5 V		—	– 800	—	
PDI Input Voltage					V
Low	V_{IL}	V_{DG}	—	0.8	
High	V_{IH}	2.0	—	V_{DD}	
MISCELLANEOUS					
V_{QB} Voltage ($V_{QB} - V_{EE}$)	V_{QB}				Vdc
@ I_L = 20 mA		—	0.82	—	
@ I_L = 40 mA		—	0.95	—	
TXO Offset Voltage ($V_{TXO} - V_{AG}$) @ R_L = 600 Ω	V_{TXO}	– 400	+30	+400	mVdc
TXO Output Current	I_{TXO}	±275	±800	—	µA pk
RXI Offset Voltage ($V_{RXI} - V_{AG}$) @ R_L = 600 Ω	V_{RXOS}	—	0.8	—	mVdc
V_{AG} Input Current @ R_L = 600 Ω	I_{VAG}	—	0.2	—	µA
Idle Channel Noise (with C-message filter, R_L = 600 Ω)					dBrnc
@ TXO (Pin 11)	N_{IC4}	—	– 10	—	
@ Tip/Ring	N_{IC2}	—	– 5.0	—	
Thermal Resistance — Junction to Ambient	θ_{JA}				°C/W
(Either package, in still air, soldered to a PC board) (@ T_A = +25°C)		—	62	—	
(@ T_A = +85°C)		—	36	—	

FIGURE 1 — TEST CIRCUIT



Note: Pin numbers refer to DIP package.

FIGURE 2 — LONGITUDINAL BALANCE TEST

(Per IEEE-455)

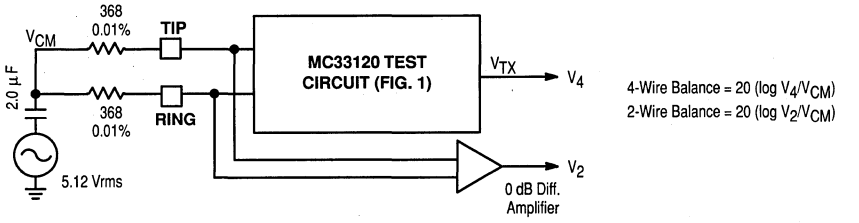


FIGURE 3 — SIGNAL BALANCE TEST

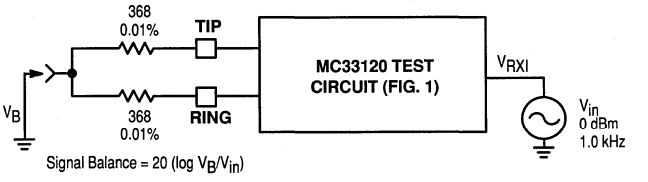
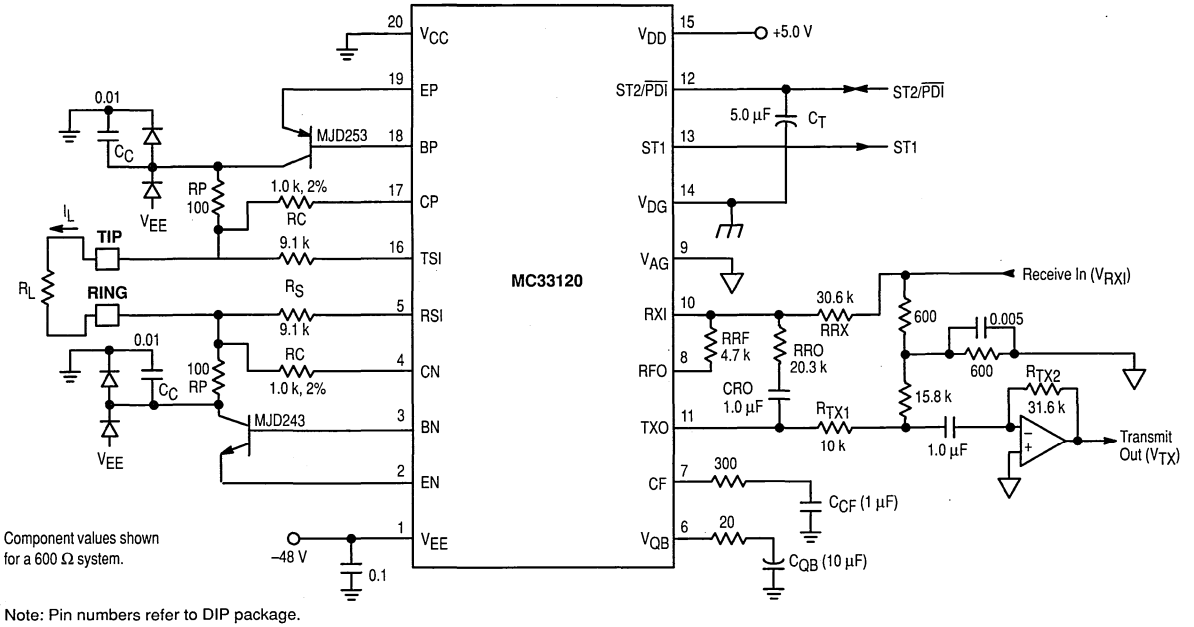


FIGURE 4 — APPLICATION CIRCUIT



Note: Pin numbers refer to DIP package.

PIN DESCRIPTION

Name	Pin		Description
	DIP	PLCC	
V_{CC}	20	28	Connect to noise-free Battery ground. Carries loop current and some bias currents.
EP	19	27	Connect to the emitter of the PNP pass transistor.
BP	18	26	Connect to the base of the PNP pass transistor.
CP	17	24	Connect to TIP through a current limiting protection resistor (R_C). CP is the noninverting input to the internal transmit amplifier (Figure 28). Input impedance is 31 kΩ.
TSI	16	23	Sense input. Connect to TIP through a current limiting protection resistor (R_S) which also sets the longitudinal impedance. Input impedance is ≈100 Ω to V_{CC}.
V_{DD}	15	22	Connect to a +5.0 V, ±10% supply, referenced to digital ground. Powers logic section and provides some bias currents for the loop current drivers.
V_{DG}	14	20	Digital Ground. Reference for ST1, ST2 and V_{DD}. Connect to system digital ground.
ST1	13	18	Status Output (TTL/CMOS). Indicates hook switch status — High when on-hook, low when off-hook, and pulse dialing information. Used with ST2 to indicate fault conditions.
ST2/PDI	12	17	Status output **and** an input (TTL/CMOS). As an output, ST2 can indicate hook status — Low when on-hook, high when off-hook. Used with ST1 to indicate fault conditions. As an input, it can be taken low (when off-hook) to deny subscriber loop current.
TXO	11	16	Transmit voltage output. Amplitude is ≈1/3 that across CP and CN. Nominally capable of 800 μA output current. DC referenced to V_{AG}.
RXI	10	14	Receive current input. Current at this pin is multiplied by 102 at EP and EN to generate loop current. RXI is a virtual ground at V_{AG} level. Current flow is **out** of this pin.
V_{AG}	9	13	Analog ground, reference for TXO and RXI. Connect to system analog ground.
RFO	8	12	A resistor between this pin and RXI sets the maximum loop current and DC feed resistance. Minimum resistor value is 3.3 k (see Figures 5–7).
CF	7	10	A low leakage capacitor between this pin and V_{AG} provides DC and AC signal separation. A series resistor is required for battery supply turn-on/off transient protection (Figure 4).
V_{QB}	6	8	Quiet Battery. A capacitor between V_{QB} and V_{CC} filters noise and ripple from V_{EE}, providing a quiet battery source for the speech amplifiers. A series resistor is required for battery supply turn-on/off transient protection (Figure 4).
RSI	5	7	Sense input. Connect to RING through a current limiting protection resistor which also sets the longitudinal impedance. Input impedance is ≈100 Ω to V_{QB}.
CN	4	6	Connect to RING through a current limiting protection resistor. CN is the inverting input to the internal transmit amplifier (Figure 28). Input impedance is 31 kΩ.
BN	3	4	Connect to the base of the NPN pass transistor.
EN	2	3	Connect to the emitter of the NPN pass transistor.
V_{EE}	1	2	Connect to battery voltage. Nominally – 48 V, it can range from – 42 to – 58 V.

(Pins 1, 5, 9, 11, 15, 19, 21, and 25 are not internally connected on the PLCC package).

FIGURE 5 — LOOP CURRENT versus LOOP RESISTANCE AND RRF

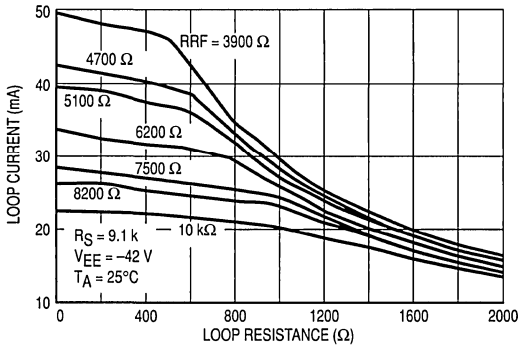


FIGURE 6 — LOOP CURRENT versus LOOP RESISTANCE AND RRF

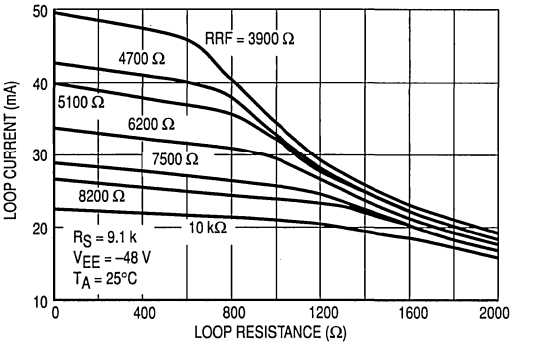


FIGURE 7 — LOOP CURRENT versus LOOP RESISTANCE AND RRF

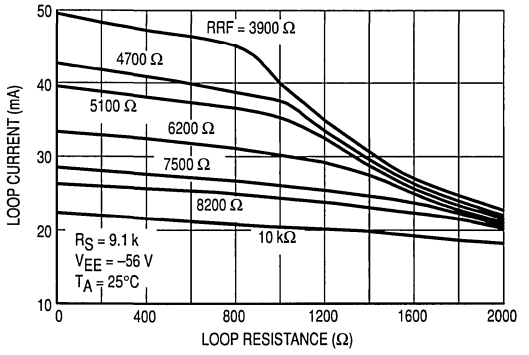


FIGURE 8 — OFF-HOOK TO ON-HOOK THRESHOLD versus RRF

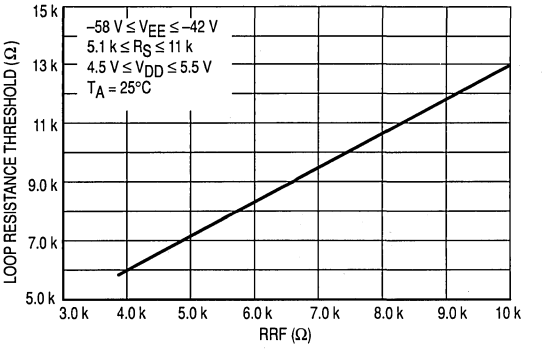


FIGURE 9 — ON-HOOK TO OFF-HOOK THRESHOLD versus R_S

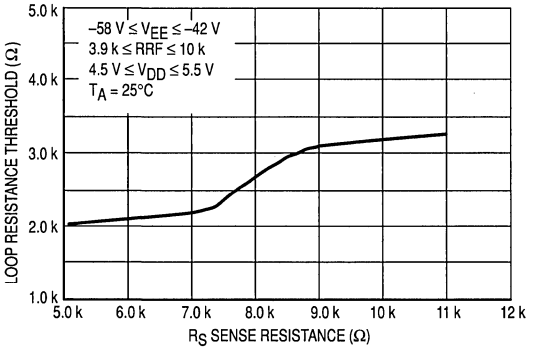


FIGURE 10 — I_{DD} versus LOOP CURRENT

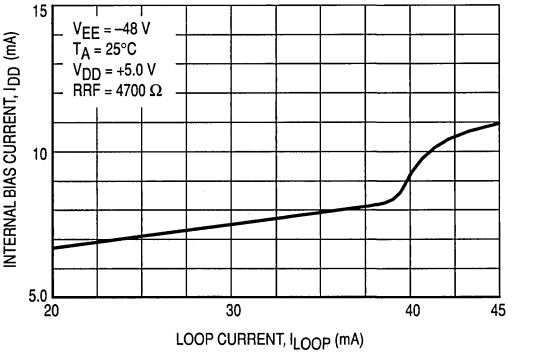


FIGURE 11 — FAULT THRESHOLD (ON-HOOK) versus R_S

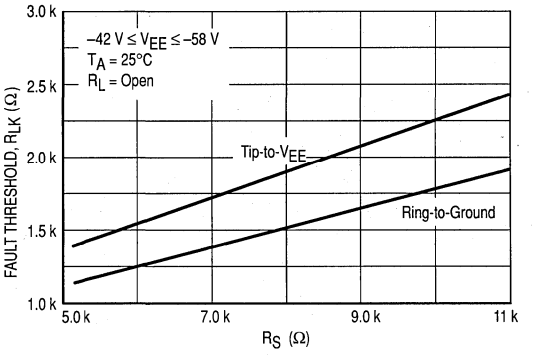


FIGURE 12 — FAULT THRESHOLD (OFF-HOOK) versus LOOP RESISTANCE

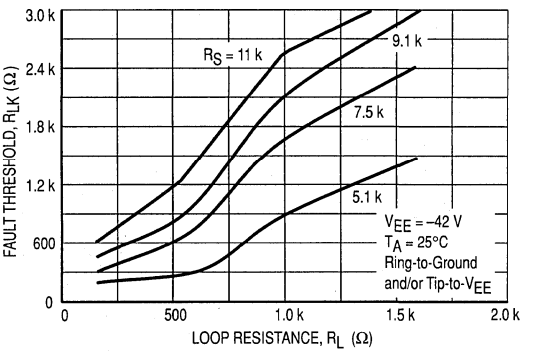


FIGURE 13 — FAULT THRESHOLD (OFF-HOOK) versus LOOP RESISTANCE

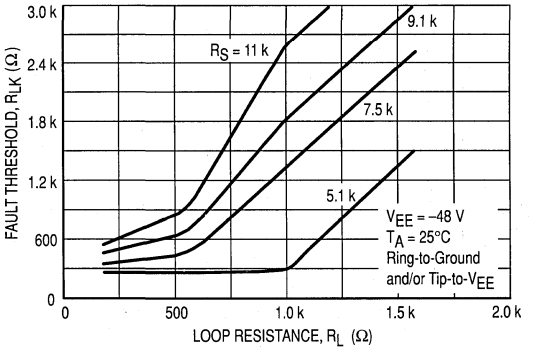


FIGURE 14 — FAULT THRESHOLD (OFF-HOOK) versus LOOP RESISTANCE

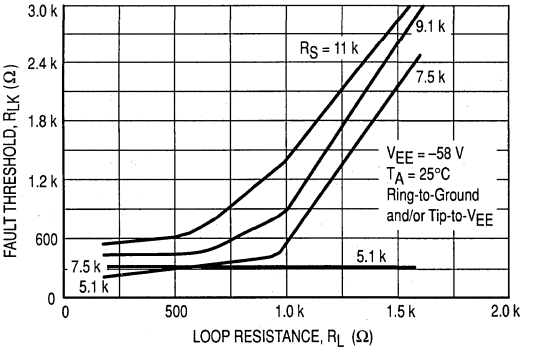


FIGURE 15 — FAULT THRESHOLD (OFF-HOOK) versus R_S

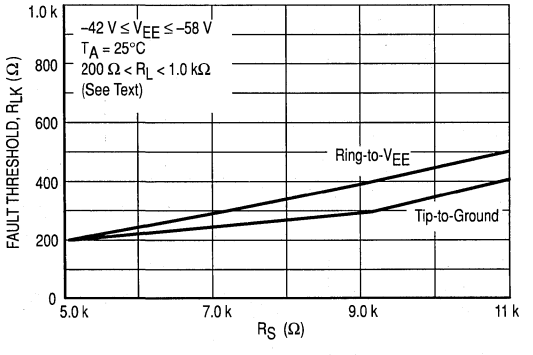


FIGURE 16 — V_{DD} RIPPLE REJECTION versus FREQUENCY

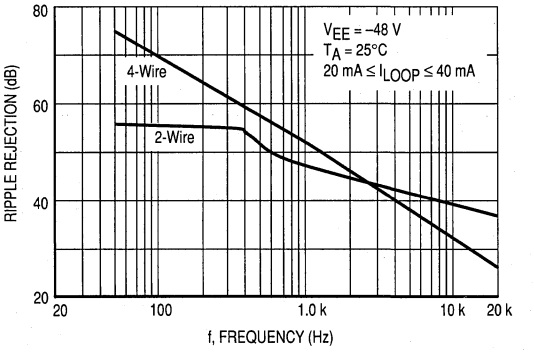


FIGURE 17 — V_{EE} RIPPLE REJECTION versus FREQUENCY

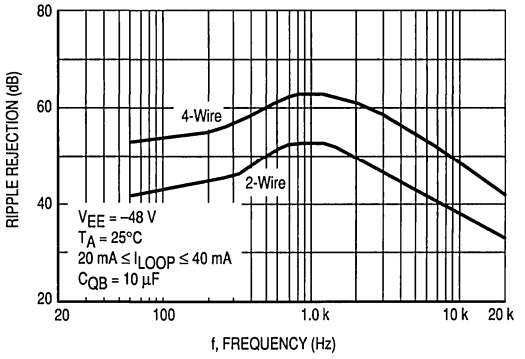


FIGURE 18 — V_{EE} RIPPLE REJECTION versus FREQUENCY AND C_{QB}

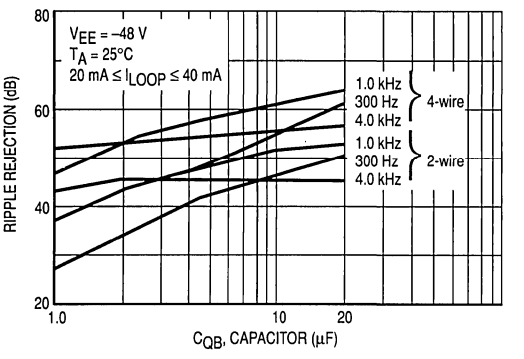


FIGURE 19 — ST1, V_{OL} versus I_{OL}

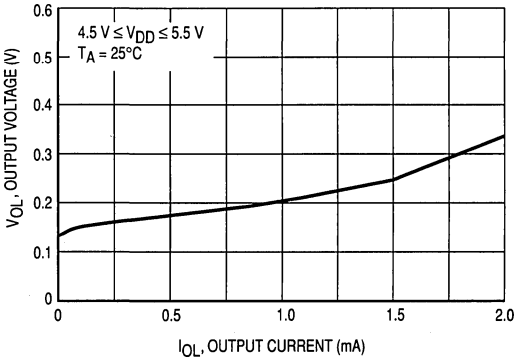


FIGURE 20 — ST1, V_{OH} versus I_{OH}

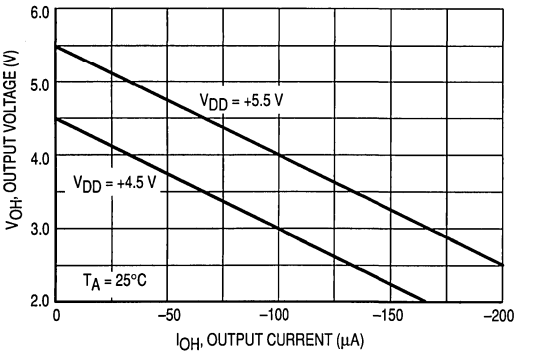


FIGURE 21 — ST2, V_{OL} versus I_{OL}

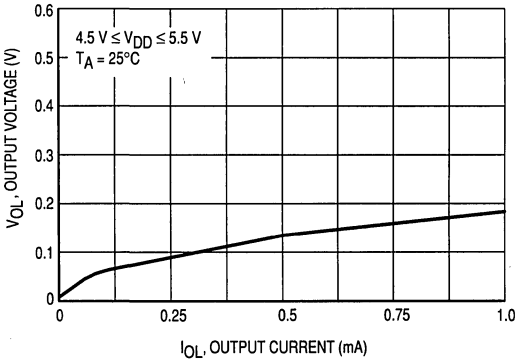


FIGURE 22 — ST2, V_{OH} versus I_{OH}

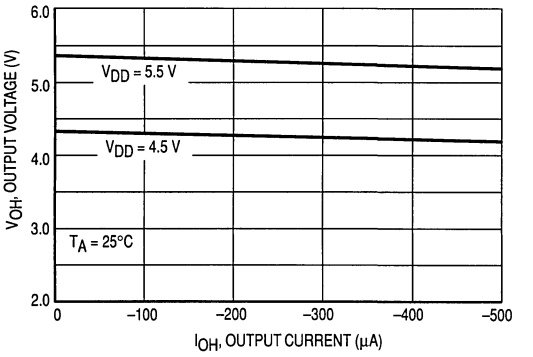


FIGURE 23 — IC POWER DISSIPATION versus LOOP RESISTANCE AND V_{EE}

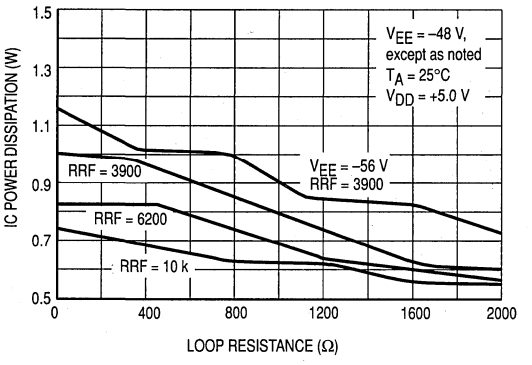


FIGURE 24 — TRANSISTOR POWER DISSIPATION versus LOOP RESISTANCE AND RRF

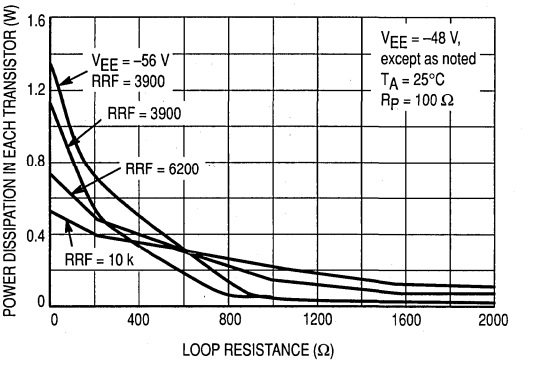


FIGURE 25 — MAXIMUM LONGITUDINAL CURRENT versus LOOP CURRENT

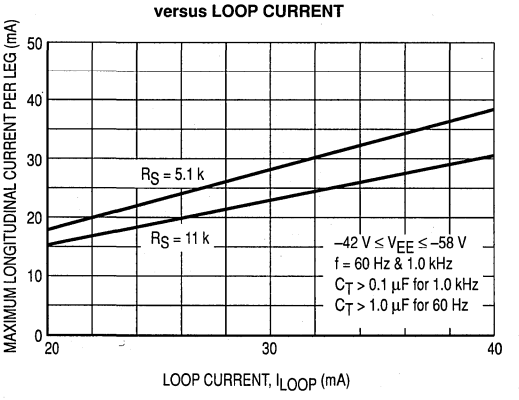
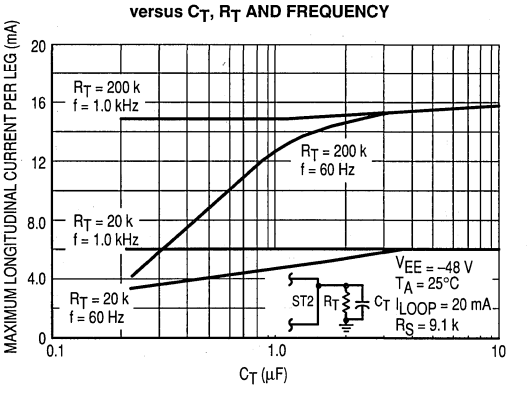


FIGURE 26 — MAXIMUM LONGITUDINAL CURRENT versus C_T, R_T AND FREQUENCY



FUNCTIONAL DESCRIPTION

Introduction

The MC33120 is a solid state SLIC (Subscriber Line Interface Circuit) which provides the interface between the two wire telephone line and the four wire side of a Central Office or PBX. Most of the BORSCHT functions are provided, specifically:

— **B**attery feed of the loop current to the line, with programmable maximum current for short lines and battery feed resistance for long lines.
— **O**vervoltage protection through internal clamp diodes and external resistors and diodes.
— **S**upervision, in that hook status is indicated in the presence of ≥30 kΩ leakage, and regardless of whether or not the circuit is powered down intentionally by the Central Office or PBX. Fault conditions are detected and indicated to the system. Dialing (pulse and DTMF) information is passed through the MC33120 to the 4-wire side.
— **H**ybrid function, in that the MC33120 is a 2-to-4 wire converter. Transmit, receive, return loss, and transhybrid gains are independently adjustable.

The MC33120 does not provide ring insertion, ring trip, digital coding/decoding of the speech signals, nor test functions. These must be provided external to this device.

The MC33120 controls two external transistors (one NPN and one PNP) through which the loop current flows. By appropriate circuit design, the power dissipation (which can exceed 3.0 watts under certain worst case conditions) is approximately equally distributed among the two transistors and the IC, thereby lowering junction temperatures and increasing long term reliability. In most situations, heatsinks will not be required.

The MC33120 incorporates critical sense resistors internally, which are trimmed for optimum performance. With this technique, the external resistors on the two wire side, which generally must be high wattage for transient protection reasons, can be non-precision.

Longitudinal balance is tested to a minimum of 58 dB @ 1.0 kHz (refer to Electrical Characteristics and Figure 1) for both the two wire and four wire side, and typically measures in the mid-60s. The longitudinal current capability is tested to a minimum of 8.5 mArms per side (refer to Electrical Characteristics and Figure 1) at a loop current of 20 mA.

Following is a description of the individual sections. Figure 4 is the reference schematic.

DC Loop Current

The DC loop current is determined by the battery voltage (V_{EE}), the load resistance across Tip and Ring, and the resistor at RFO. Varying the 4 resistors R_S and RC will influence the loop current a small amount (<5%). The curves of Figures 5–7 indicate the loop current versus loop resistance, different values of RRF, and for various values of V_{EE}. The graphs represent performance at T_A = 25°C and after the IC had reached a steady state temperature (>5 minutes).

FIGURE 27 — DC LOOP CURRENT PATH

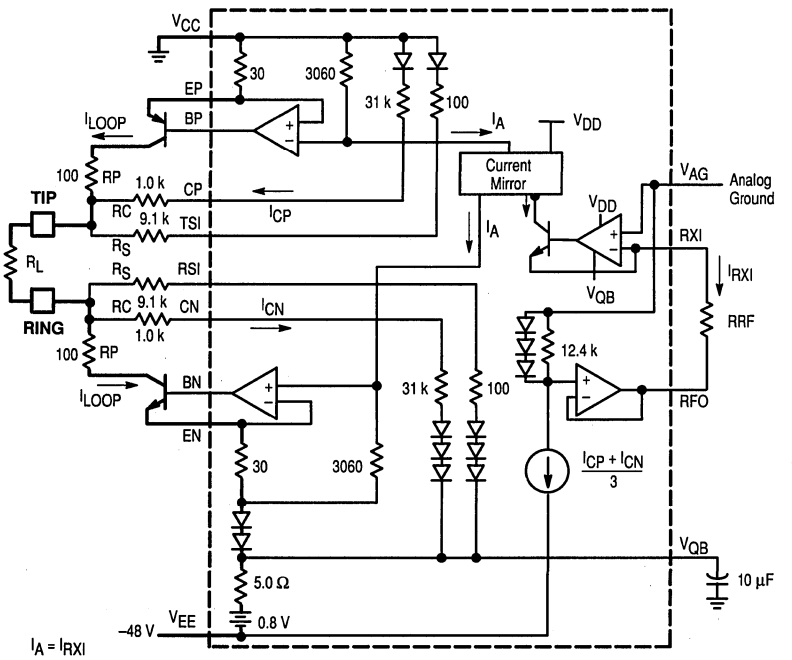


Figure 27 is representative of the DC loop current path (bold lines). On a long line (R_L > 1.0 kΩ), the loop current can be determined from the following equation:

$$I_{LOOP} = \frac{(|V_{EE}| - 3.6\ V) \bullet 13}{RRF + \{(R_L + 5) \bullet 13\}} \qquad \text{(Equation 1)}$$

On short lines (R_L < 1.0 kΩ), the three diodes across the 12.4 k resistor clamp the voltage at RFO, thereby preventing the RXI current from increasing as the load resistance is decreased. The maximum loop current is:

$$I_{LOOP\ (MAX)} = \frac{1.85\ V \bullet 102}{RRF} \ (T_A = 25°C) \qquad \text{(Equation 2)}$$

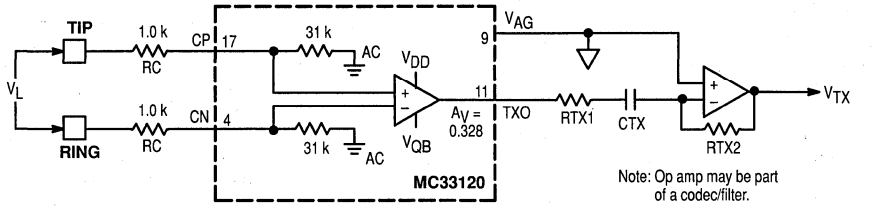
Due to the temperature dependence of a diode's forward voltage, the maximum loop current will change with temperature by ≈ −0.3%/°C.

The battery feed resistance ($\Delta V_{TIP}/\Delta I_L$) is ≈400 Ω, but depends on the loop current, V_{EE}, RRF, and is a valid parameter only on long lines where the current limit is not in effect. On short lines, the feed resistance is high since the loop current is clamped at a constant level. The AC impedance (Return Loss) however, is not determined nor affected by the DC parameters. See the Applications Section for Return Loss information.

Transmit Path

The transmit path, shown in Figure 28, consists of an internal amplifier which has inputs at CP and CN, and its output at TXO. The gain is internally fixed at 0.328 V/V (−9.7 dB). The output is in phase with the signal at CP (normally the same as TIP), and is out of phase with the signal at CN. The signal at TXO is also out of phase with that at V_{RX}, the receive signal input, described in another section.

FIGURE 28 — TRANSMIT PATH



The TXO output can swing ≈3.0 Vp-p, with a nominal current capability of ±800 µA peak (±275 µA minimum). The load on TXO is the parallel combination of RTX1 and the RRO network (described later). TXO is nominally internally biased at the V_{AG} DC level, but has an offset which varies with loop current.

In normal applications, the signal at CP/CN is reduced slightly from that at Tip/Ring by the voltage divider composed of the external RC resistors, and the internal 31 k resistors. The value of the RC resistors depends on the transient protection needed, described in another section, with 1.0 kΩ resistors being suitable for most applications. The resulting signal at TXO needs to be gained up to obtain 0 dB from Tip/Ring to V_{TX} (the 4-wire output). The common method involves an external op amp, as shown in Figure 28, with a gain of RTX2/RTX1. The gain from V_L to V_{TX} is:

$$\frac{V_{TX}}{V_L} = \frac{RTX2 \bullet 31\ k \bullet 0.328}{RTX1 \bullet (RC + 31\ k)} \qquad \text{(Equation 3)}$$

If a codec/filter is used, many of which include an internal op amp, a separate op amp is not needed. CTX is primarily for DC blocking (of the TXO offset), and is usually large (1.0 µF) so as to not affect the gain.

Receive Path

The receive path, shown in Figure 29, consists of the input at RXI, the transistor driver amplifiers, the external transistors, and the load at Tip/Ring.

RXI is a virtual ground (DC level = V_{AG}) and is a current input. Current flow is **out** of the pin. The RXI current is mirrored to the two transistor drivers which provide a gain of 102. The two external transistors are then two current sources, in series, operating at the same value. An additional internal circuit (not shown) balances the two current sources to maintain operation in their linear region.

The load current (through R_L) is slightly different from the transistor current due to the sense resistors RC and RS. The sense resistors add to the DC loop current, but subtract from the AC load current.

In normal operation, the current at RXI is composed of a DC current (from RFO), an AC current (from V_{RX}) which is the receive signal, and an AC current from TXO, which is the feedback signal to set the return loss (setting the return loss is discussed in the section on AC Terminating Impedance). The resulting AC signal at Tip is inverted from that at V_{RX}, while the signal at Ring is in phase with V_{RX}.

The resistors RP are for transient protection, and their value (defined in another section) depends on the amount of protection required. A nominal value of 100 Ω is suitable for most applications.

The system receive gain, from V_{RX} to Tip/Ring, is not described in this section since in normal applications, it involves the feedback which sets the AC terminating impedance. The Applications Section discusses these in detail.

Logic Interface (Hook status, pulse dialing, faults)

The logic interface section provides hookswitch status, fault information, and pulse dialing information to the 4-wire side of the system at the ST1 and ST2 outputs. Figure 30 is a representative diagram.

FIGURE 29 — RECEIVE PATH

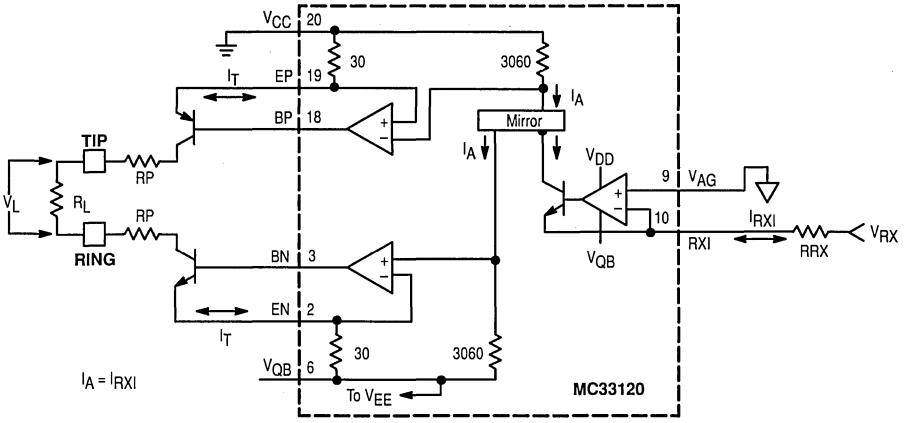
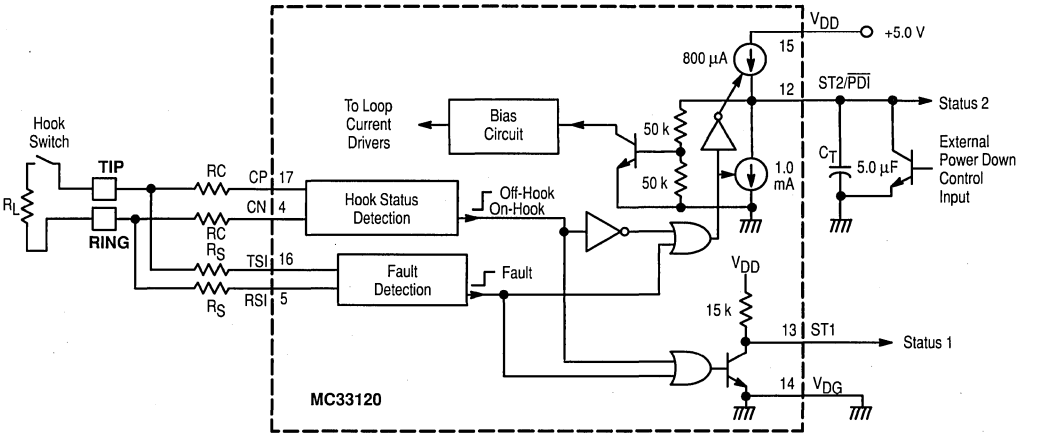


FIGURE 30 — LOGIC INTERFACE



The logic outputs operate according to the truth table in Table 1:

TABLE 1 — STATUS OUTPUT TRUTH TABLE

Hook Status	Fault Detection	Outputs		Circuit Condition
		ST1	ST2	
On Hook	No Fault	Hi	Lo	Internally powered down
Off Hook	No Fault	Lo	Hi	Powered up
On Hook	Fault	Lo	Lo	Internally powered down
Off Hook	Fault	Lo	Lo	Internally powered down

Referring to Figure 30, ST1 is configured as an active NPN pulldown with a 15 kΩ pullup resistor. ST2 has a 800 µA current source pullup, and a 1.0 mA current source for a pulldown. Current limiting this output controls the discharge from the external capacitor when ST2 switches low.

The condition where both ST1 and ST2 are high is not valid, but may occur momentarily during an off-hook to on-hook transition. The condition where both ST1 and ST2 are low may occur momentarily during an on-hook to off-hook transition — this should not be interpreted as a fault condition. ST1 and ST2 are TTL/CMOS compatible and are powered by the +5.0 V supply (V_{DD}). Refer to the Applications Section for more details.

Power Supplies, Grounds

The MC33120 requires 2 power supplies: battery voltage between – 42 V and – 58 V (V_{EE}), and an auxiliary voltage between +4.5 V and +5.5 V (V_{DD}).

V_{EE} is nominally – 48 V, with a typical range of – 42 V to – 58 V, and must be referenced to V_{CC} (battery ground). A 0.1 µF bypass capacitor should be provided between V_{CC} and V_{EE}. The V_{EE} current (I_{EE}) is nominally 1.2 mA when on-hook, 10 to 14 mA more than the loop current when off-hook, and ≈8.0 mA when off-hook but powered down by using the PDI pin. Ripple and noise rejection from V_{EE} is a minimum of 40 dB (with a 10 µF capacitor at V_{QB}), and

is dependent on the size and quality of the V_{QB} capacitor (C_{QB}) since V_{QB} is the actual internal supply voltage for the speech amplifiers. The absolute maximum for V_{EE} is – 60 V, and should not be exceeded by the combination of the battery voltage, its tolerance, and its ripple.

V_{DD} is normally supplied from the line card's digital +5.0 V supply, and is referenced to V_{DG} (digital ground). A 0.1 µF capacitor should be provided between V_{DD} and V_{DG}. The V_{DD} current (I_{DD}) is nominally 1.7 mA when on-hook and between 6.0 and 11 mA when off-hook (see Figure 10). When the MC33120 is intentionally powered down using the PDI pin, I_{DD} changes by <1.0 mA from the normal off-hook value.

V_{AG} is the analog ground for the MC33120, and is the reference for the speech signals (RXI and TXO). Current flow is **into** the pin, and is typically <0.5 µA.

Normally, V_{CC}, V_{DG} and V_{AG} are to be at the same DC level. However, if strong transients are expected at Tip and Ring, as in a Central Office application, V_{CC} should not be connected directly to V_{DG} and V_{AG} in order to prevent possible damage to the +5.0 V system. The MC33120 is designed to tolerate as much as ±30 V between V_{CC} and the other two grounds **on a transient basis only.** This feature permits V_{CC} and the other grounds to be kept separate (on an AC basis) on the line card by transient suppressors, or to be connected together farther into the system (at the power supplies). See the Applications Section on ground arrangements and transient protection for further information on connecting the MC33120 to the system supplies.

For operation of the MC33120 at supply voltages other than – 42 to – 58 V (such as – 24 V or – 28 V), contact your local Motorola sales office.

APPLICATIONS INFORMATION

This section contains information on the following topics:

Design Procedure ..... pg. 15
Power Dissipation Calculations and Considerations ..... pg. 22
Selecting the Transistors ..... pg. 23
Longitudinal Current Capability ..... pg. 23
PC Board Layout Considerations ..... pg. 24
Alternate Circuit Configurations ..... pg. 26

Design Procedure

This section describes the step-by-step sequence for designing in the MC33120 SLIC into a typical line card application for either a PBX or Central Office. The sequence is important so that each new component value which is calculated does not affect components previously determined. Figure 4 (Typical Application Circuit) is the reference circuit for most of this discussion. The recommended sequence (detailed below), consists of establishing the DC aspects first, and then the AC aspects:

1) Determine the maximum loop current for the shortest line, select RRF. Power dissipation must be considered here.
2) Select the main protection resistors (RP), and diodes, based on the expected transient voltages. Transient protection configuration must also be considered here.
3) Select RC based on the expected transient voltages.
4) Select RS based on the desired longitudinal impedance at Tip and Ring. Transient voltages are also a factor here.
5) Calculate RRO based on the desired AC terminating impedance (return loss).
6) Calculate RRX based on the desired receive gain.
7) Calculate RTX2 and RTX1 based on the desired transmit gain.
8) Calculate the balance resistor (RB), or network, as appropriate for desired transhybrid rejection.
9) Logic Interface

Preliminary

There is a primary AC feedback loop which has its main sense points at CP and CN (see Figure 34). The loop extends from there to TXO, through RRO to RXI, through the internal amplifiers to the transistor drivers, through RP to Tip and Ring, and through the RCs to CP and CN. Components within this loop, such as RP, RC, the transistors, and the compensation capacitors need not be tightly matched to each other in order to maintain good longitudinal balance. The tolerance requirements on these components, and others, are described in subsequent sections. Any components, however, which are placed **outside** the loop for additional line card functions, such as test relay contacts, fuses, resistors in series with Tip and Ring, etc. will affect longitudinal balance, signal balance, and gains if their values and mismatch is not carefully considered. The MC33120 cannot compensate for mismatch among components outside the loop.

The compensation capacitors (0.01 µF) shown at the transistor collectors (Figure 4) compensate the transistor driver amplifiers, providing the required loop stability. The required tolerance on these capacitors can be determined from the following guidelines:

A 10% mismatch (±5% tolerance) will degrade the longitudinal balance by ≈1.0 dB on a 60 dB device, and by ≈3.0 dB on a 70 dB device.

A 20% mismatch (±10% tolerance) will degrade the longitudinal balance by ≈3.0 dB on a 60 dB device, and by ≈6.0 dB on a 70 dB device.

High quality ceramic capacitors are recommended since they serve the secondary function of providing a bleedoff path for RF signals picked up on the phone line. These capacitors should be connected to a good quality RF ground.

The capacitors used at C_{QB} and C_F must be low leakage to obtain proper performance. Leakage at the C_{QB} capacitor will affect the DC loop current characteristics, while leakage at the C_F capacitor will affect the AC gain parameters.

1) Maximum Loop Current and Battery Feed Resistance

The maximum loop current (at R_L = 0) is determined by the RRF resistor between RFO and RXI. The current limit is accomplished by three internal series diodes (see Figure 27) which clamp the voltage across RRF as the loop resistance decreases, thereby limiting the current at RXI. Since the loop current is 102 x I_{RXI}, the loop current is therefore

clamped. The graphs of Figures 5–7 indicate the maximum loop current at an ambient temperature of +25°C, and after the IC has reached thermal equilibrium (approx. 10 minutes).

Although the maximum loop current is primarily a function of the RRF resistor, it is also affected by ambient temperature, and slightly by V_{EE}. The ambient temperature effects are due to the temperature dependence of the diodes' forward voltage drop, causing the maximum loop current to change by ≈ – 0.3%/°C. Changing V_{EE} affects the maximum current in that the power dissipation is changed, thereby changing the die temperature, which affects the diodes' voltage.

The maximum loop current is affected slightly (<5%) by the choice of the RS and RC resistors, since the sense currents through those resistors add to the current supplied by the transistors.

The battery feed resistance is determined by RRF, and is not adjustable independently of the current limit. Defined as $\Delta V_{TIP}/\Delta I_L$, it is ≈400 Ω, and is a valid parameter only on long lines where the current limit is not in effect. On short lines, the feed resistance is high since the loop current is clamped at a near constant level. The AC impedance (return loss) however, is not determined nor affected by these DC parameters. Return loss is discussed in another section.

If the application requires that the current limit value have a low temperature dependence, refer to the section following this design sequence which describes an alternate configuration.

2) Main Protection Resistors (RP) and Transient Currents

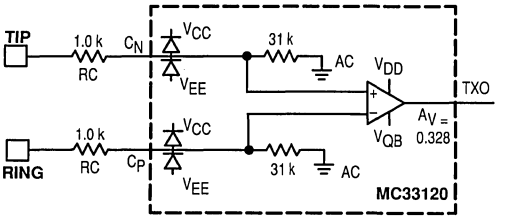
The purpose of the protection resistors (RP), along with the 4 clamp diodes shown in Figure 4, is to absorb the bulk of the transient energy when transient voltages come in from the phone line. The resistor value must be selected to limit the transient current to a value which can be tolerated by the diodes, while dissipating the energy. The recommended value shown (100 Ω) will limit the current from a 1500 V transient to 15 A, which can be carried by 1N4002 diodes under surge conditions. The resistors must be of a type which can tolerate the high instantaneous energy associated with transients. Resistor manufacturers should be consulted for this information.

Referring to Figure 4, a positive transient on either Tip or Ring, or both, will cause the transient current to be delivered to Ground. A negative transient will cause the transient current to come from the V_{EE} supply line. Therefore, the PC board track supplying V_{CC} and V_{EE} to the MC33120 must be designed to carry the transient currents as well as the normal operating currents. Additionally, since a negative transient will cause a current flow **out** of the power supply's negative output, which is opposite to the normal flow of current, provisions must be made for this reverse current flow. One suggested method is to place a zener transient suppressor (1N6290A) across the battery supply pins (V_{CC} to V_{EE}) **physically adjacent to the MC33120.** The inductance associated with PC board tracks and wiring will result in insufficient protection for the MC33120 if the suppressor is located at the opposite end of the line card, or at the power supplies.

Transient currents can be reduced by increasing the value of RP, with an upper limit determined by the DC conditions on the longest line (highest loop resistance) and minimum V_{EE} supply voltage. These conditions determine the minimum DC voltage across the transistors, which must be sufficient to handle the largest AC (transmit and receive) signals. If too large a value is selected for RP, the AC signals will be clipped. It is recommended that each transistor have no less than one volt (DC) across their collector to emitter. System AC specifications may require more than this.

Since the RP resistors are within the loop, their tolerance can be ±5% with no substantial degradation of longitudinal balance. A ±10% tolerance (20% mismatch) will degrade balance by ≈4.0 dB on a 65 dB device.

FIGURE 32 — RC PROTECTION RESISTORS



3) Selecting the RC Resistors

The primary purpose of the RC resistors is to protect the CP and CN pins from transient voltages and destructive currents. Internally, these pins have clamp diodes to V_{CC} and V_{EE} rated for a maximum of 1.0 A under surge conditions only (Figure 32). The 1.0 kΩ resistors shown in the figures, for example, will provide protection against surges up to 1.0 kV. Resistor manufacturers must be consulted for the proper type of resistor for this environment.

The RC resistors are in series with internal 31 kΩ resistors, and therefore form a voltage divider to the inputs of the transmit amplifier, as shown in Figure 32. This will affect the transmit gain, receive gain, return loss, and transhybrid rejection (described in subsequent sections). The tolerance of the RC resistors depends on the value selected for them, since any mismatch between them will create a differential voltage at CP and CN when longitudinal voltages are present on Tip and Ring. To ensure a minimum of 58 dB of longitudinal balance, the resistors' absolute value must not differ by more than 39 Ω. With a nominal value of 1.0 kΩ, their tolerance must be ±2%, or less. If their nominal value is 390 Ω or less, their tolerance can be ±5%.

4) Longitudinal Impedance (Z_{LONG}) — Selecting the RS Resistors

The longitudinal impedance is determined by the RS resistors at the TSI and RSI pins according to the following equation:

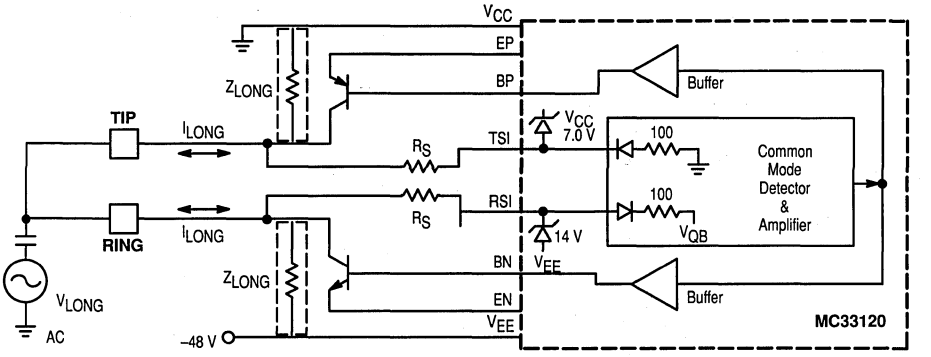
$$Z_{LONG} = \frac{RS + 100}{51} \qquad \text{(Equation 4)}$$

Z_{LONG} is defined as V_{LONG}/I_{LONG} as shown in Figure 33; for RS = 9.1 kΩ, Z_{LONG} = 180 Ω. The calculated value of Z_{LONG} includes the fact that the RS resistors are in parallel with the synthesized impedance. The tolerance of the RS resistors therefore depends on how much mismatch can be tolerated between the longitudinal impedances at Tip and at Ring. Calculations indicate the two RS resistors

can have a ±5% tolerance, and still comfortably provide a minimum of 58 dB longitudinal balance.

The resistors must be able to withstand transient voltages expected at Tip and Ring. The TSI and RSI pins have internal clamp diodes rated for a maximum of 1.0 A under surge conditions only (Figure 33). Resistor manufacturers must be consulted for the proper type of resistor for this environment.

FIGURE 33 — LONGITUDINAL IMPEDANCE

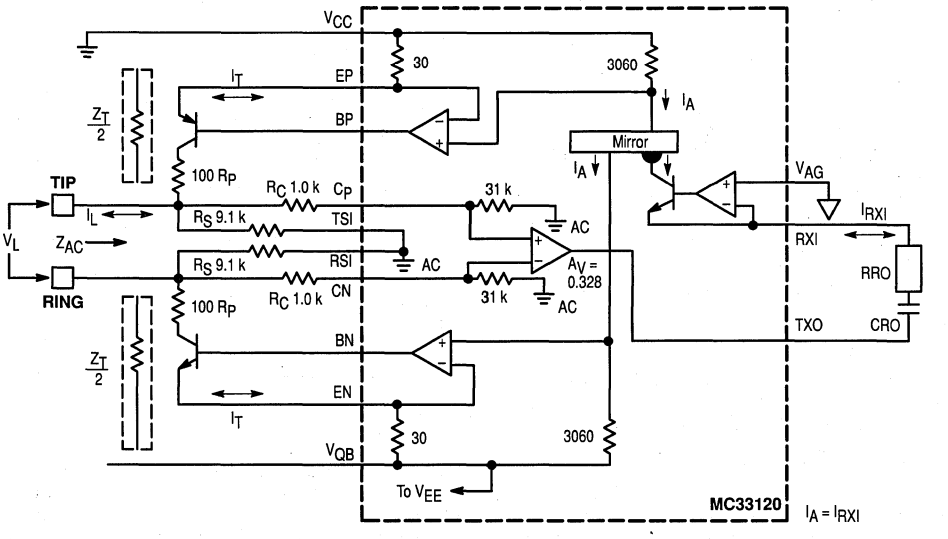


5) AC Terminating Impedance and Source Impedance (Z_{ac}) — Return Loss

The return loss measurement is a measure of how closely the AC impedance of the SLIC circuit matches the characteristic impedance of the phone line, or a reference impedance. The reference impedance can be, in some cases, a pure resistance (commonly 600 Ω or 900 Ω), a series resistor and capacitor (900 Ω + 2.16 μF), or a more complex network. To achieve proper return loss with the MC33120, the RRO impedance shown in Figure 34 is to have the same configuration as the reference impedance, but with values scaled according to the equations mentioned below.

CRO, used primarily for DC blocking, is generally a large value (1.0 μF) so as to not affect the impedance of RRO. However, it can be included in the RRO network if a complex network is required.

FIGURE 34 — AC TERMINATING IMPEDANCE



Z_{ac} is the impedance looking into the circuit from Tip and Ring (set by RRO), and is defined as V_L/I_L. Half of Z_{ac} is from Tip to V_{CC}, and the other half is from Ring to V_{QB} (an AC ground). Each half is made up of a synthesized impedance ($Z_T/2$) in parallel with R_S and (RC + 31 k).

Therefore Z_{ac} is equal to:

$$Z_{ac} = [Z_T/2 \,//R_S//(RC + 31\ k)] \bullet 2 \qquad \text{(Equation 5)}$$

$$\text{and } \frac{Z_T}{2} = \frac{\{R_S//(RC + 31\ k)\} \bullet (Z_{ac}/2)}{\{R_S//(RC + 31\ k)\} - (Z_{ac}/2)} \qquad \text{(Equation 6)}$$

The synthesized impedance Z_T is created as follows:

An incoming signal V_L produces a differential voltage at CP and CN, and therefore at TXO equal to:

$$V_{TXO} = \frac{V_L \bullet 31\ k \bullet 0.328}{(RC + 31\ k)} \qquad \text{(Equation 7)}$$

The signal at TXO creates an AC current I_{RXI} through RRO. RXI is a virtual ground, and CRO is insignificant for first order calculations.

I_{RXI} is gained up by a factor of 102 to produce the current I_T through the transistors.

Z_T is therefore V_L/I_T. The relationship between Z_T and RRO is:

$$RRO = \frac{Z_T \bullet 1.037 \bullet 10^6}{(31\ k + RC)} \qquad \text{(Equation 8)}$$

While equation 8 gives the exact value for RRO, a first order approximation is $Z_{ac} \bullet 33.5$.

a) Resistive Loads (with RC = 1.0 k, R_S = 9.1 k):

For a 600 Ω resistive system, Z_T calculates to 626 Ω, and RRO calculates to 20.3 kΩ.

For a 900 Ω resistive system, Z_T calculates to 961 Ω, and RRO calculates to 31.14 kΩ.

b) Complex Loads

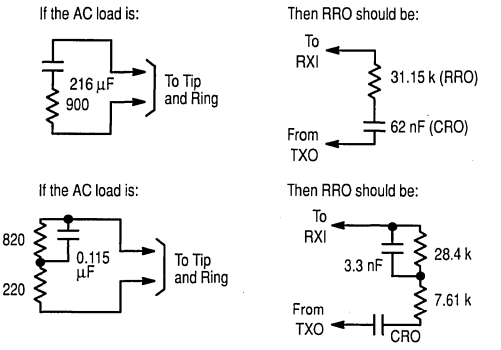
For complex (non-resistive) loads, the MC33120 must be made to look like a termination impedance equal to that complex load. This is accomplished by configuring RRO the same as the complex load, but with all impedance values increased according to the scaling factor of Equation 9.

$$SF = \frac{[(RC + 31\ k)//RS] \bullet 1.037 \bullet 10^6}{(RC + 31\ k) \bullet [(RC + 31\ k)//R_S - (Z_{ac}/2)]} \qquad \text{(Equation 9)}$$

Z_{ac} is computed at a nominal frequency of interest. A first order approximation of Equation 9 is:

$$SF = 1.037 \bullet 10^6/(RC + 31\ k) \qquad \text{(Equation 9a)}$$

For example:

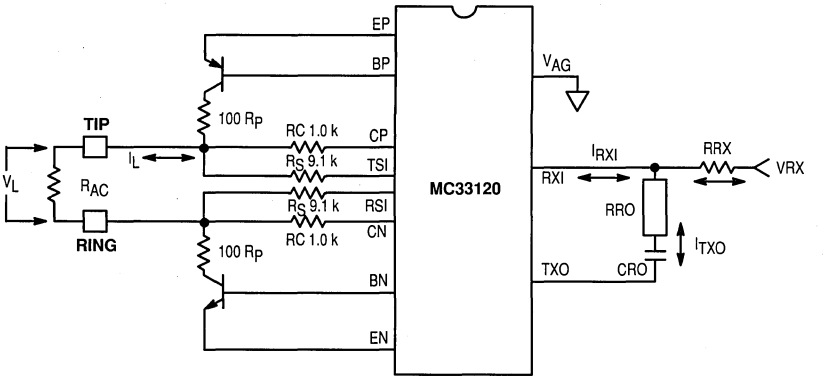


CRO must remain in series with the network to provide DC blocking. If the load network does not include a series capacitor (as in the second example above), CRO should be large (1.0 µF) so its impedance does not affect the RRO network. The above procedure will yield a return loss measurement which is constant with respect to frequency. The RRO resistor, or network, must have a tolerance equal to or better than the required system tolerance for return loss and receive gain.

6) Receive Gain (G_{RX})

The receive gain involves the same circuit as Figure 34, but with the addition of the RRX resistor (or network) which sets the receive gain. See Figure 35.

FIGURE 35 — RECEIVE GAIN



The receive gain (G_{RX}), defined as the voltage gain from V_{RX} to V_L, is calculated as follows:

RXI is a virtual ground, and R_{ac} is the AC impedance of the load (phone line).

The AC current generated in the transistors is $102 \bullet I_{RXI}$, which is equal to $102 \bullet (I_R - I_{TXO})$.

$I_R = V_{RX}/RRX$, and

$$I_{TXO} = \frac{V_{TXO}}{RRO} = \frac{V_L \bullet 31\ k \bullet 0.328}{RRO \bullet (31\ k + RC)} \qquad \text{(Equation 10)}$$

Using equations 5 and 8, involving Z_{ac}, RS and RC, and the above equations yields:

$$\frac{V_L}{V_{RX}} = G_{RX} = \frac{102 \bullet (R_{ac}//Z_{ac})}{RRX} \qquad \text{(Equation 11)}$$

$$\text{Therefore, } RRX = \frac{102 \bullet (R_{ac}//Z_{ac})}{G_{RX}} \qquad \text{(Equation 12)}$$

Equation 12 applies **only** for the case where R_{ac} and Z_{ac} have the same configuration. If they also have the same magnitude, then set $RRX = 51 \bullet R_{ac}$ to set a receive gain of 0 dB. The AC source impedance of the above circuit to Tip and Ring is Z_{ac}. For the case where $R_{ac} \neq Z_{ac}$, use the following equation:

$$\frac{V_L}{V_{RX}} = \frac{102}{RRX \bullet \left[\frac{1}{Z_L} + \frac{1.037 \bullet 10^6}{(31k + RC) \bullet RRO}\right]} \qquad \text{(Equation 13)}$$

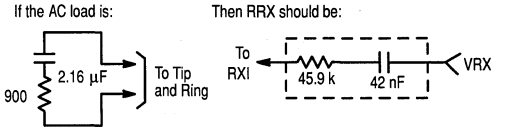
$$\text{where } Z_L = \left[\frac{R_{ac}}{2} // RS // (RC + 31\ k)\right] \bullet 2 \qquad \text{(Equation 14)}$$

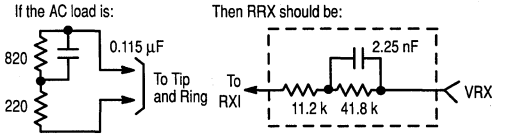
a) Resistive Loads

For a 600 Ω resistive system, set RRX = 30.6 kΩ, and for a 900 Ω resistive system, set RRX = 45.9 kΩ.

b) Complex Loads

For complex (non-resistive) loads, the RRX resistor needs to be replaced with a network having the same configuration as the complex load, but with all impedance values scaled up by a factor of 51 (for 0 dB gain). If a gain other than 0 dB is desired, the scaling factor is determined from Equation 12. This methods applies **only** if the RRO network has been made complex comparable to the load according to the procedure in the previous section (Equations 5–9a), such that $R_{ac} = Z_{ac}$. Using a scaling factor of 51, and the previous examples, yields:





The preceeding procedure will yield a receive gain which is constant with respect to frequency. The RRX resistor, or network, must have a tolerance equal to or better than the required system tolerance for receive gain.

7) Transmit Gain (G_{TX})

Setting the transmit gain involves selecting RTX1 and RTX2 in Figure 28. The voltage gain from V_L to V_{TX} is calculated from the following:

$$G_{TX} = \frac{V_{TX}}{V_L} = \frac{RTX2 \bullet 31\ k \bullet 0.328}{RTX1 \bullet (RC + 31\ k)} \qquad \text{(Equation 15)}$$

For 0 dB gain, set RTX2 = 3.15 x RTX1 (for RC = 1.0 k). The actual values of RTX2 and RTX1 are not critical — only their ratio so as to provide the proper gain at the op amp. Once the ratio is established, the two resistors can be selected from a set of standard resistor values. The minimum value for RTX1 is limited by the drive capability of TXO, which is a nominal ±800 µA peak (±275 µA minimum). As a general rule, RTX1 should be between 6.0 kΩ and 20 kΩ. The load on TXO is the parallel combination of RTX1 and RRO.

CTX is for DC blocking, and is typically a large value (1.0 µF) so as to not be a significant impedance. In general, it should **not** be used for low frequency rolloff as that will affect the transhybrid rejection (discussed in the next section). Low frequency rolloff should be done after the op amp. High frequency rolloff can be set by placing a capacitor across RTX2.

For complex loads (at Tip and Ring), if RRO and RRX have been made complex comparable to the load as described in the previous sections, neither RTX1 nor RTX2 needs to be complex since both the transmit and receive signals which appear at TXO will be flat with respect to frequency.

RTX1 and RTX2 must have a tolerance equal to or better than the required system tolerance for the transmit gain.

8) Balance Network (RB) — Transhybrid Rejection

When a receive signal is applied to V_{RX} to produce a signal at Tip and Ring, the two-to-four wire arrangement of a hybrid (the MC33120) results in a reflected signal at TXO. Transhybrid rejection involves canceling that reflected signal before it appears at V_{TX}. The method used is to insert the RB resistor (or network) as shown in Figure 36. The current I_B, supplied form V_{RX}, cancels the current I_{TX1} supplied from TXO (Node A is a virtual ground). Good transhybrid cancellation requires that the currents be equal in magnitude **and** 180° out of phase at node A.

Using the equations for transmit and receive gains, the current I_{TX1} is equal to:

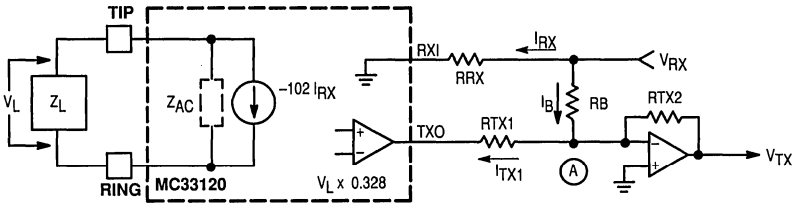
$$I_{TX1} = \frac{33.5 \bullet V_{RX} \bullet Z_{ac} \bullet Z_L \bullet 31\ k}{RRX \bullet [Z_{ac} + Z_L] \bullet RTX1 \bullet (RC + 31\ k)} \qquad \text{(Equation 16)}$$

a) For the case where RRO and RRX are comparable in configuration to Z_L:

Since $I_B = V_{RX}/RB$, then RB can be determined from:

$$RB = \frac{RRX \bullet RTX1 \bullet (RC + 31\ k)}{33.5 \bullet [Z_{ac}//Z_L] \bullet 31\ k} \qquad \text{(Equation 17)}$$

FIGURE 36 — BALANCE RESISTOR



Equation 17 provides a value for an RB resistor which will provide the correct magnitude for I_B. The correct phase relationship is provided by the fact that the signal at TXO is out of phase with that at V_{RX}. The phase relationship will be 180° **only** if RRO and RRX are of a configuration identical to that of the load. This applies regardless of whether the load, Z_L, (and RRO and RRX) are purely resistive or of a complex nature. Equation 17 reduces to a non-complex resistance if RRX, Z_{ac}, and Z_L are all comparably complex.

For the case where $Z_{ac} = Z_L$, RRX = 51 • Z_{ac}, and RC = 1.0 k, Equation 17 reduces to:

$$RB = 3.15 \bullet RTX1 \qquad \text{(Equation 18)}$$

b) For the case where Z_{ac} and Z_L do not have the same frequency characteristics:

For the case where, for reasons of cost and/or simplicity, the load (R_L) is considered resistive (whereas in reality it is not a pure resistance) and therefore resistors, rather than networks, were selected for RRO and RRX, using a simple resistor for RB may not provide sufficient transhybrid rejection due to a phase angle difference between V_{RX} and TXO. The terminating impedance may therefore not necessarily be matched exactly to the line impedance, but the resulting circuit still provides sufficiently correct performance for receive gain, transmit gain, and return loss. The rejection can be improved in this case by replacing RB with the configuration shown in Figure 37. Even on a very short phone line there is a reactive component to the load due to the two compensation capacitors (C_C, Figure 4) at the transistor collectors. The two capacitors can be considered in series with each other, and across the load as shown in Figure 37. To simplify the explanation, the current source and Z_{ac} of Figure 36 are replaced with the Thevenin voltage source and series Z_{ac}. Since Z_L and Z_{ac} are not matched, there will be a phase shift from V_{RX} to the signal across Tip and Ring. This phase shift is also present at TXO. The same phase shift is generated at node B in the RB network by making RB1 equal to Z_{ac}, and Z_L equal to the load. RB2 is then calculated from:

$$RB2 = \frac{RRX \bullet RTX1 \bullet (RC + 31\ k)}{33.5 \bullet Z_{ac} \bullet 31\ k} \qquad \text{(Equation 19)}$$

For example, for a system where the load is considered a 600 Ω resistor (RRO = 20.3 kΩ, RRX = 30.6 kΩ, RTX1 = 10 kΩ, and RC = 1.0 kΩ), RB1 would be a 600 Ω resistor, Z_L (in the RB network) would be a 600 Ω resistor in parallel with a 0.005 μF capacitor, and RB2 calculates to 15.715 kΩ.

The RB resistor, or network, must have a tolerance equal to or better than the required system tolerance for transhybrid rejection.

9) Logic Interface

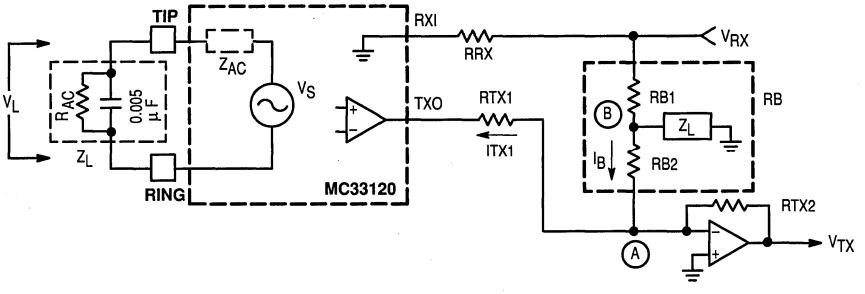
The logic circuit (output ST1, and the I/O labeled ST2/PDI) is depicted in Figure 30, and functions according to the truth table in Table 1.

a) Output Characteristics

ST1 is a traditional NPN pull-down with a 15 kΩ pull-up resistor. Figures 19 and 20 indicate its output characteristics.

ST2 is configured with the following items: a) a 1.0 mA current source for a pull-down which is active only when ST2 is internally set low; b) an 800 μA current source pull-up which is active only when ST2 is internally set high; c) a positive feedback aspect within this output circuit which provides considerable hysteresis for stability reasons. Its output characteristics are shown in Figures 21 and 22. Due to this configuration, any external pull-up resistance which is applied to this pin must be greater than 15 kΩ, or the output may not reliably switch from high to low. Any external pull-down resistance does not affect this output's ability to

FIGURE 37 — BALANCE NETWORK



switch from low-to-high, but **does** affect the maximum longitudinal currents which can be accepted by the circuit (see the section on Longitudinal Current capability). The capacitor (C_T) is required to provide a time delay, for stability reasons, during transitions between off-hook and on-hook. This capacitor additionally affects maximum longitudinal currents, as well as stability during pulse dialing (explained below).

b) Hook Status

The MC33120 uses the sense currents at CP and CN to activate the hook status circuit. The sensing is configured such that the circuit monitors the impedance across Tip/Ring, which results in the hookswitch thresholds being virtually independent of the battery voltage. The off-hook to on-hook threshold is affected by the choice of RRF according to the graph of Figure 8, but is not affected by the value of RS. The on-hook to off-hook threshold is affected by the value of RS according to the graph of Figure 9, but is not affected by RRF. Varying the RC resistors does not affect the thresholds significantly.

When the telephone is on-hook (ST1 = Hi, ST2 = Low), the MC33120 is internally powered down, the external transistors are shut off, and power consumption is at a minimum. Upon closure of the phone's hookswitch, ST1 will switch low within 10 µs. ST2 will then change state slowly due to the external capacitor (C_T = 5.0 µF). There is a ≈8.0 millisecond delay for ST2 to reach the threshold necessary to activate the internal bias circuit, which in turn activates the external drive transistors to supply loop current. This delay is necessary to prevent instabilities during the transition to off-hook.

Upon opening the telephone's hookswitch, ST1 will switch high within ≈200 µs. ST2 then requires ≈60 ms to reach the threshold to switch off the internal bias circuit, which in turn shuts down the external drive transistors.

c) Pulse Dialing

During pulse dialing, ST1 will change state concurrent with the hookswitch. ST2 is kept from switching during pulse dialing by the external capacitor (C_T), which keeps the MC33120 in a powered up condition and stable. If the C_T capacitor is too small, the voltage at ST2 could droop to the PDI threshold (see section e below) during each pulse. This could cause the MC33120 to create additional noise on the line as it would cycle between a power-up and power-down condition with each dialing pulse.

d) Fault Detection

Faults are defined as excessive leakage from Tip to V_{EE} and/or ground, and from Ring to V_{EE} and/or ground. A single fault is any one of the above conditions, while a double fault is defined as excessive leakage from Tip to V_{EE} **and** from Ring to V_{CC}, as depicted in Figure 38. Refer to Figures 11–15 for the resistance, R_{LK}, which will cause the MC33120 to switch to a power-down condition. If the leakage resistance is less than that indicated in the graphs, the MC33120 will power-down itself and the two external transistors, thereby protecting them from overheating. Both status outputs (ST1 and ST2) will be at a logic low, indicating a fault condition. A fault condition is detected by monitoring an imbalance in the magnitudes of the currents at TSI and RSI, and/or a polarity reversal at Tip and Ring.

The MC33120 will detect the following conditions:

1) When on-hook (see Figure 11):
   - a) <2.0 kΩ between Ring and V_{CC}, with no hysteresis at this threshold, or
   - b) <2.5 kΩ between Tip and V_{EE}, with no hysteresis at this threshold, or
   - c) Both a and b simultaneously.

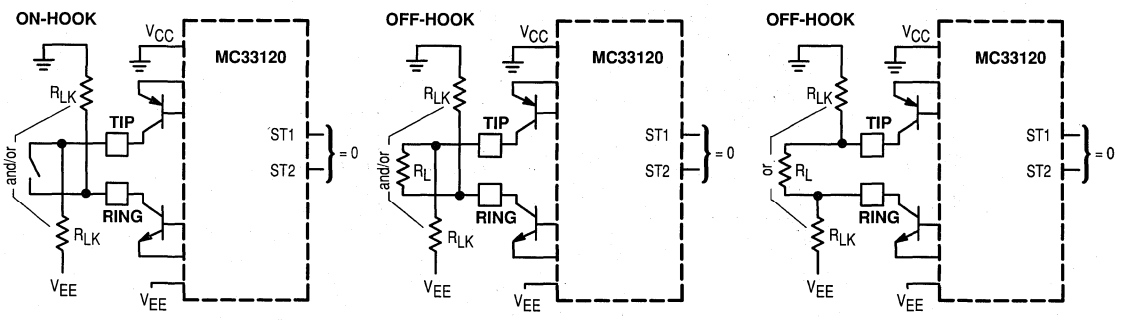
Leakage from Tip to V_{CC} and/or Ring to V_{EE} are not detected as faults while the MC33120 is on-hook.

2) When off-hook (600 Ω between Tip and Ring):
   - a) <500 Ω between Tip and V_{CC}, or
   - b) <600 Ω between Tip and V_{EE}, or
   - c) <500 Ω between Ring and V_{EE}, or
   - d) <600 Ω between Ring and V_{CC}, or
   - e) Both b and d simultaneously

A simultaneous occurrence of conditions a) and c) is not detected as a fault. See Figures 12–15 for the threshold variation with R_L. Resetting of the fault detection circuit requires that the leakage resistance be increased to a value between 10 kΩ and 20 kΩ, depending on V_{EE}, R_L, and R_S. Both ST1 and ST2 should be monitored for hookswitch status to preclude not detecting a fault condition.

Figure 15 indicates the variation in fault thresholds for Tip-to-V_{CC} and Ring-to-Battery faults, and is valid only for loop resistances of 200 Ω to 1.0 kΩ. On loops larger than

FIGURE 38 — FAULT DETECTION



1.0 kΩ, the MC33120 does not reliably indicate the fault condition at ST1 and ST2, but may indicate on-hook status instead. This does not apply to Tip-to-Battery and Ring-to-V_{CC} faults which are correctly detected for lines beyond 1.0 kΩ.

e) PDI Input

The ST2 output can also be used as an input (PDI input) to power down the circuit, denying loop current to the subscriber (by shutting off the external pass transistors), regardless of the hookswitch position. Powering down is accomplished by pulling PDI to a logic low with an open collector output, or an NPN transistor as shown in Figure 30. The switching threshold is ≈+1.5 V. The current out of PDI, when pulled low, is ≈800 μA. Releasing PDI allows the MC33120 to resume normal operation.

If the external telephone is off-hook while the MC33120 is powered down, sense currents at CP and TSI will result in some loop current flowing through the loop and back into CN and RSI. This current is generally on the order of 1.0 to 3.0 mA, determined primarily by the RS resistors, loop resistance, and V_{EE}. ST1 will continue to indicate the telephone's actual hook status while PDI is held low. The on-to-off hook threshold is the same as that during normal operation, but the off-to-on hook threshold is >250 kΩ.

When powered down with the PDI pin, the receive gain (V_{RXI} to Tip/Ring) is muted by >90 dB, and the transmit gain (Tip/Ring to TXO) is muted by >30 dB.

Power Dissipation, Calculation and Considerations

a) Reliability

The maximum power dissipated by the MC33120 must be considered, and managed, so as to not exceed the junction temperature listed in the Absolute Maximum Ratings. Exceeding this temperature on a recurring basis will reduce long term reliability, and possibly degrade performance. The junction temperature also affects the statistical lifetime of the device, due to long term thermal effects within the package. Today's plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However, when the ultimate in system reliability is required, thermal managements must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperature is consistent with system reliability goals.

Based on the results of almost ten years of +125°C operating life testing, Table 2 has been derived indicating the relationship between junction temperature and time to 0.1% wire bond failure.

TABLE 2 — STATISTICAL LIFETIME

Junction Temperature (°C)	Time (Hours)	Time (Years)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Motorola MECL Device Data, DL122

The "time" in Table 2 refers to the time the device is operating at that junction temperature. Since the MC33120 is at a low power condition (nominally 68 mW) when on-hook, the duty cycle must be considered. For example, if a statistical duty cycle of 20% off-hook time is used, operation at 130°C junction temperature (when off-hook) would result in a statistical lifetime of ≈10 years.

b) Power and Junction Temperature Calculation

The power within the IC is calculated by subtracting the power dissipated in the two wire side (the transistors and the load) from the power delivered to the IC by the power supplies. Refer to Figure 4 and 27.

$$P_D = |V_{DD} \bullet I_{DD}| + |V_{EE} \bullet I_{EE}| - (I_{LOOP} \bullet |V_{EP} - V_{EN}|)$$

(Equation 20)

The terms V_{EP} and V_{EN} are the DC voltages, with respect to ground, at the EP and EN pins. These voltages can be measured, or can be approximated by:

$$V_{EP} \approx -(30\ \Omega \bullet I_{LOOP})$$
$$V_{EN} \approx V_{EE} + 2.1\ V + (I_{LOOP} \bullet 35\ \Omega)$$

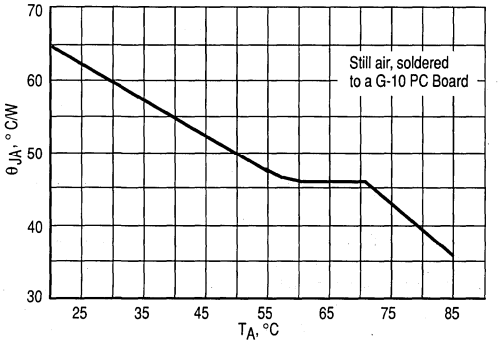
Refer to Figure 23. The junction temperature is then calculated from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \qquad \text{(Equation 21)}$$

where T_A is the ambient air temperature at the IC package, and θ_{JA} is the junction-to-ambient thermal resistance shown in Figure 39. The highest junction temperature will occur at maximum V_{EE} and V_{DD}, maximum loop current, and maximum ambient temperature.

If the above calculations indicate the junction temperature will exceed the maximum specified, then it is necessary to reduce the maximum loop current, ambient temperature, and/or V_{EE} supply voltage. Air flow should not be restricted near the IC by tall components or other objects since even a small amount of air flow can substantially reduce junction temperature. For example, typically an air flow of 300 LFPM (3.5 mph) can reduce the effective θ_{JA} by 14 to 20% from that which occurs in still air. Additionally, providing as much copper area as possible at the IC pins will assist in drawing away heat from within the IC package. For additional information on this subject, refer to the "Thermal Considerations" section of *Motorola MECL System Design Handbook* (HB205), and the "System Design Considerations" section of *Motorola MECL Device Data* (DL122).

FIGURE 39 — THERMAL RESISTANCE (JUNCTION TO AMBIENT)



Selecting the Transistors

The specifications for the two loop current pass transistors involve their current gain, voltage rating, and power dissipation capabilities at the highest ambient temperatures. Power dissipation during both normal operation and faults must be considered when determining worst case situations. Generally, more power is dissipated during a fault condition than during normal operation.

The transistors' minimum beta is recommended to be 40 at the loop currents involved in the application. A lower beta could degrade gain and balance performance. Maximum beta should be less than 500 to prevent possible oscillations. Darlington type transistors should not be used. The voltage rating should be a minimum of 80 V, although the choice of protection scheme may require a higher rating.

Referring to Figure 27, during normal operation the loop current and the voltage across the transistors are both at a maximum when the load impedance (R_L) is at a minimum. The loop current is determined by RRF and the graphs of Figures 5–7. The voltage across each transistor is determined from the following:

$$V_T = \frac{|V_{EE}| - 2.1 - [(65 + 2RP + R_L) \bullet I_{LOOP}]}{2} \quad \text{(Equation 22)}$$

The power in each transistor is then ($V_T \bullet I_{LOOP}$). The voltage across the two transistors will always be nearly equal during normal operation, resulting in equal power dissipation. The graph of Figure 24 indicates the power dissipated in each transistor where RP = 100 Ω.

During a fault condition, depicted in Figure 38, if the leakage resistance from Tip to V_{EE} or from Ring to V_{CC} is less than that shown in Figures 12–14 (when off-hook), the MC33120 will power down the transistors to protect them from overheating. Should the leakage resistance be slightly higher than that shown in the graphs, however, and the fault detection has not been activated, the power in one transistor (in a single fault, both transistors in a double fault) will be higher than normal. The power will depend on V_{EE}, R_L, RP and the leakage resistance. Table 3 is a guide of the power in the transistor dissipating the higher power level.

TABLE 3 — TRANSISTOR POWER DURING A FAULT

V_{EE}	R_S	R_L	P_{PNP}	P_{NPN}
–58	9.1 k	200	1.64	1.34
–48	9.1 k	200	1.05	0.957
–58	9.1 k	600	1.37	1.11
–48	9.1 k	600	0.746	0.616
–58	9.1 k	1.0 k	0.897	0.68
–48	9.1 k	1.0 k	0.232	0.194
–58	5.1 k	200	1.8	1.55
–58	11 k	200	1.53	1.3

The power (in watts) in the two right columns indicates the power dissipated by that transistor if it is carrying the maximum fault current. The system designer should attempt to predict possible fault conditions for the system, and then measure the conditions on the transistors during the worse case fault(s).

For most applications involving a nominal V_{EE} of – 48 V (with a maximum of – 58 V), a maximum loop current of 30 to 40 mA, and a maximum T_A of +85°C, the MJD243 and MJD253 DPAK transistors are recommended. When mounted as described in their data sheet, they will handle both the normal loop current as well as most fault conditions. If faults are not expected to occur in a particular application, then smaller package transistors, such as MPS6717 and MPS6729, may be used. Each application must be evaluated individually when selecting the transistors.

Other possible transistors which can be considered:

PNP	NPN
MJD253-1	MJD243-1
MJE253	MJE243
MJD32	MJD31
MJD42	MJD41
MJD350	MJD340
TIP30A,B,C	TIP29A,B,C

Longitudinal Current Capability

The maximum longitudinal current which can be handled without distortion is a function of loop current, battery feed resistance, the longitudinal impedance, and the components on ST2.

Since the pass transistors cannot pass current in the reverse direction, the DC loop current provides one upper boundary for the peak longitudinal current plus peak speech signal current. The battery feed resistance determines, in effect, the DC voltage across the transistors, which is a measure of the headroom available for the circuit to handle the peak longitudinal voltage plus peak speech signal voltage. The longitudinal impedance, determined by the R_S resistors (equation 4), determines the longitudinal current for a given longitudinal voltage.

While analysis of the above items may yield one value of maximum longitudinal current, a different limit (which may be higher or lower) is imposed by the capacitor C_T, and any pulldown resistance R_T, on Pin 12 (ST2). This is due to the fact that the sense currents at TSI and RSI will be alternately mismatched as Tip and Ring move up and down together in the presence of longitudinal signals. When the longitudinals are strong, the internal fault detect circuit is activated with each 1/2 cycle, which attempts to switch ST2 low (see the section on Fault Detection). The speed at which ST2 can

switch low is a function of both the external capacitor, C_T and any pulldown resistance, R_T.

The graphs of Figures 25 and 26 indicate the maximum longitudinal current which can be handled (in Tip **and** in Ring) without distortion or causing ST2 to switch low.

PC Board Layout Considerations

PC board considerations include thermal, RFI/EMI, transient conditions, interconnection of the four wire side to the codec/filter, and others. Wirewrapped boards should be avoided — breadboarding should be done on a (at least) reasonably neat PC board.

a) Thermal

Power dissipated by the MC33120 and the two transistors must be removed to prevent excessively high junction temperatures. The equations for calculating junction temperatures are mentioned elsewhere in this data sheet. Heat is removed by both air flow and copper foil on the PC board. Since even a small amount of air flow substantially reduces junction temperatures compared to still air, tall components or other objects should not be placed such that they block air flow across the heat generating devices. Increasing, wherever possible, the area of the copper foil at the IC pins will provide additional heat removal capability. A ground plane can generally help here, while at the same time helping to reduces RFI problems.

b) RFI/EMI

While the MC33120 is intended for use at audio frequencies, the internal amplifiers have bandwidths in excess of 1.0 MHz, and can therefore respond to externally induced RFI and EMI. Interference signals can come in on the phone line, or be radiated on to the PC board from nearby radio stations or from high frequency circuitry (digital & microprocessor circuitry) in the vicinity of the line card.

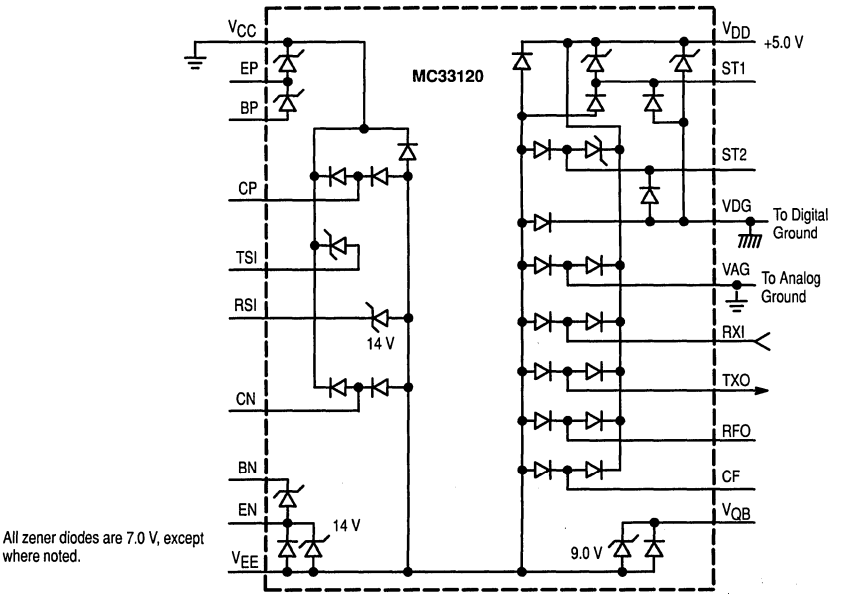
Usually RFI entering from the phone line at Tip and Ring can be removed by the compensation capacitors (C_C) provided they are connected to a good quality RF ground (generally the same ground which connects to V_{CC} on the MC33120). The ground track should be as wide and as direct as possible to minimize lead inductance. Generally better results can be obtained if an RF bleedoff to earth (or chassis) ground can be provided where the twisted pair phone line comes into the system.

To minimize problems due to noise radiating directly onto the PC board from nearby high frequency circuitry, all components associated with the MC33120 should be physically as close as possible to the IC. The most sensitive pins in this respect are the CP, CN, RSI, TSI, VAG and RXI pins. Keeping the tracks short minimizes their "antenna" effect.

c) Transient Conditions

When transient voltages come in to Tip and Ring, the transient currents, which can be several amperes, must be carried by the ground line (V_{CC}) and/or the V_{EE} line. These tracks, along with the protection and clamping devices, must be designed for these currents at the frequencies involved. If the tracks are narrow, not only may they be destroyed by the high currents, but their inductance can allow the voltage at the IC, and other nearby components, to rise to damaging levels.

FIGURE 40 — PROTECTION DIODES



The protection circuits shown in Figure 4, and in other figures in this data sheet, are such that the bulk of the transient energy is dissipated by **external** components (the protection resistors and the clamp diodes). The MC33120 has internal diodes to limit voltage excursions on the pins, and to pass a small amount of the transient current — typically less than 1.0 ampere peak. The arrangement of the diodes is shown in Figure 40.

d) Interconnection of the four-wire side

The connections on the four-wire side to the codec and other digital circuitry involves keeping digital noise out of the speech paths, and also ensuring that potentially destructive transients on Tip and Ring do not get through to the +5.0 V system.

Basically, digital connections to ST1 and ST2 should be referenced to the V_{DD} and V_{DG} pins, while the transmit and receive analog signals should be referenced to the analog ground (V_{AG}). V_{CC} should be connected to a clean battery ground, and generally should **not** be connected directly to V_{DG} and/or V_{AG} (on the line card) when strong transients are anticipated. Even with a good layout, V_{CC} can move several volts when a transient hits, possibly damaging components on the +5.0 V line **if** their grounds have a direct connection at the line card. The MC33120 is designed to allow V_{CC} to move as much as ±30 V with respect to V_{DG} and V_{AG} **on a transient basis only.** V_{CC} and the other grounds should preferably be connected together **at the power supply** rather than at the IC. Internally, the MC33120 has clamp diodes on the 4-wire side pins as shown in Figure 40.

If the codec has a single ground pin, as in Figure 41, it will be the reference for both the digital and analog signals, and must be connected to both V_{AG} and V_{DG} on the MC33120. If the codec has separate digital and analog grounds, as in Figure 42 (the MC145503 internally generates the analog ground), then each ground should be connected to the appropriate ground on the MC33120.

e) Other

A 0.1 µF capacitor should be provided across V_{CC} to V_{EE} on the MC33120 to help keep idle channel noise to a minimum.

The C_{QB} capacitor (on the V_{QB} pin) forms a pole with an internal 7.5 kΩ resistor to filter noise from the V_{EE} pin,

FIGURE 41 — CONNECTION TO A CODEC WITH A SINGLE GROUND

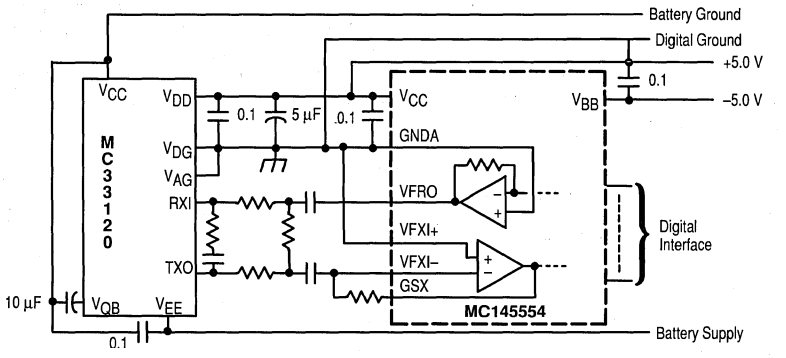
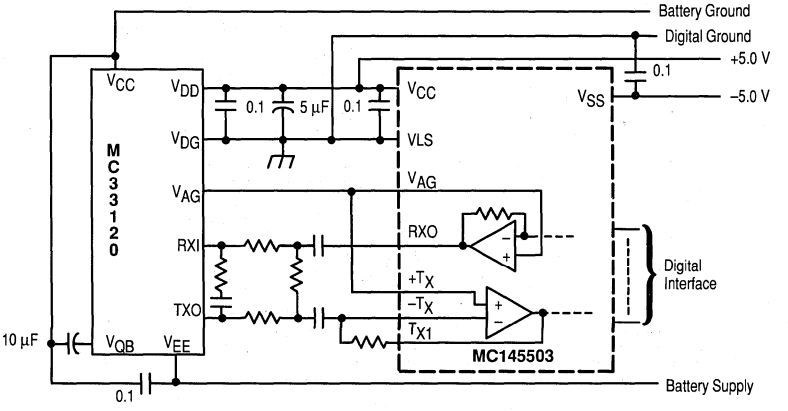


FIGURE 42 — CONNECTION TO A CODEC WITH SEPARATE GROUNDS



providing an internal quiet battery supply for the speech amplifiers. Power supply rejection will depend on the value and quality of this capacitor at the frequencies of concern. Tantalum capacitors generally have better high frequency characteristics then electrolytics. See Figure 17 and 18 for ripple rejection characteristics (the four-wire data was measured at pin 11 (TXO)). Figure 16 indicates ripple rejection from the +5.0 V supply (V_{DD}).

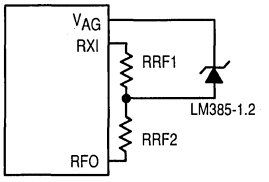
In general, PC board tracks carrying analog signals (on the four wire side and Tip/Ring) should not be routed through the digital section where they could pick up digital noise. Any tracks longer than a few inches should be considered an antenna and should be checked for potential noise or RFI pickup which could affect the circuit operation.

Alternate Circuit Configurations

a) Loop Current Limit

Replacing the RRF resistor with the circuit in Figure 43 will change the DC loop current characteristics in two ways from the graphs of Figures 5–7; a) the maximum loop current on a short line can be reduced while increasing the current on a long line, and b) the temperature dependence of the maximum current is reduced to the TC of the external reference diode.

FIGURE 43 — ALTERNATE CURRENT LIMIT CIRCUIT



The LM385-1.2 is a precision temperature stable zener diode. As the load impedance at Tip and Ring is reduced, the voltage at RFO goes increasingly negative. When the zener diode is turned on, the current into RXI is then clamped at a value determined by RRF1 and the zener diode. To calculate the two resistors, use the following procedure:

RRF1 must be >0.7 • (RRF1 + RRF2);

Determine RRF1 to set the current limit on a short line by using the following equation:

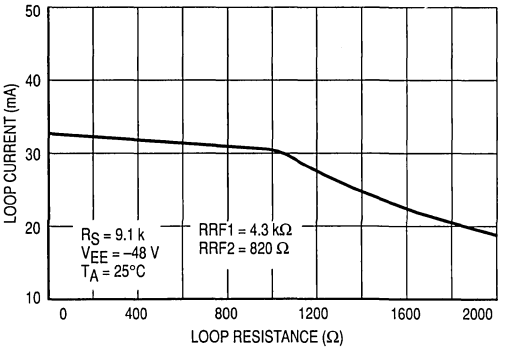
$$RRF1 = \frac{102 \bullet 1.23\ V}{I_{LOOP\ (MAX)} - 3.0\ mA} \qquad \text{(Equation 23)}$$

Then using Equation 1 calculate RRF for the long line current. RRF2 is then determined by;

$$RRF2 = RRF - RRF1 \qquad \text{(Equation 24)}$$

Figure 44 illustrates one example using the above circuit. Comparing this graph to the 5100 Ω curve of Figure 6 shows a substantial decrease in the current limit (at R_L = 0), resulting in reduced power consumption and dissipation. Use of this circuit does not affect the hookswitch or fault thresholds.

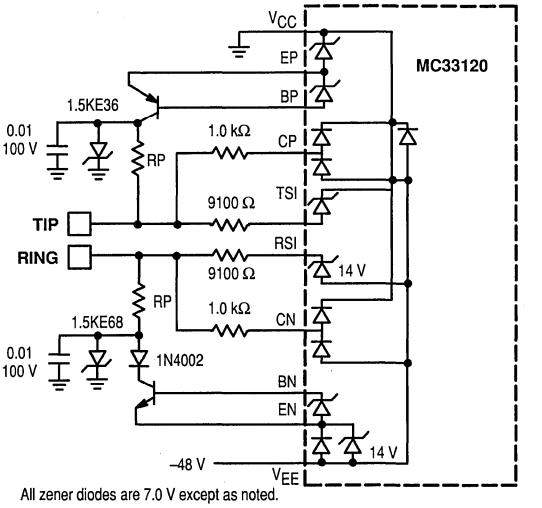
FIGURE 44 — LOOP CURRENT versus LOOP RESISTANCE ALTERNATE LOOP CURRENT LIMIT CONFIGURATION



b) Protection Scheme

The protection circuit shown in Figure 45 has the advantage of drawing ≈90% of the transient current from ground (V_{CC}) on a negative transient, rather than from the V_{EE} line as the circuit of Figure 4 does. The majority of the transient current flows through the RP resistors and the Mosorbs while a small amount (≈10%) flows through the sense resistors and the CP, CN, RSI pins. On a positive transient, all the current (except at RSI) is directed to ground. The diode in the NPN's collector prevents reverse current through the base-collector junction of the transistor during a negative transient.

FIGURE 45 — ALTERNATE PROTECTION SCHEME



All zener diodes are 7.0 V except as noted.

CIRCUIT PERFORMANCE

The following three circuits are presented as typical application examples, and the accompanying graphs indicate their measured performance. The first circuit (Figure 46) has a 600 Ω pure resistance as the AC load. The second circuit (Figures 47) has as an AC load a 900 Ω resistor in series with a 2.16 µF capacitor. The third circuit (Figure 48) has as an AC load, a complex network composed of an 820 Ω resistor in parallel with 0.115 µF, and those in series with a 220 Ω resistor. In the graphs of Figures 49–51, R_L = Return Loss, THR = Transhybrid Rejection, GTX = Transmit Gain, GRX = Receive Gain.

FIGURE 46 — 600 Ω SYSTEM

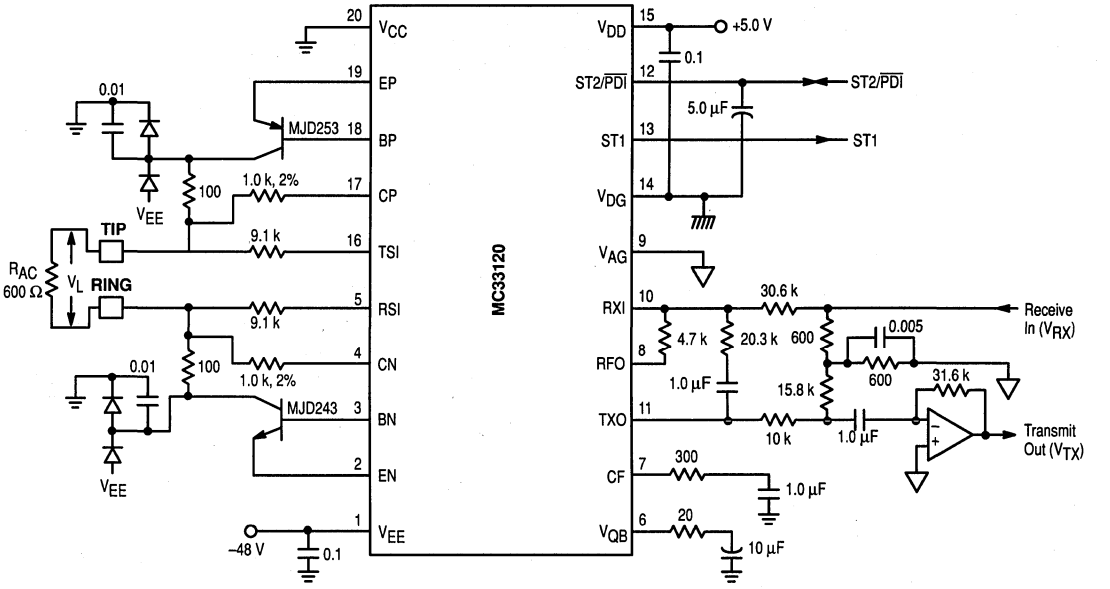


FIGURE 47 — 900 Ω + 2.16 µF SYSTEM

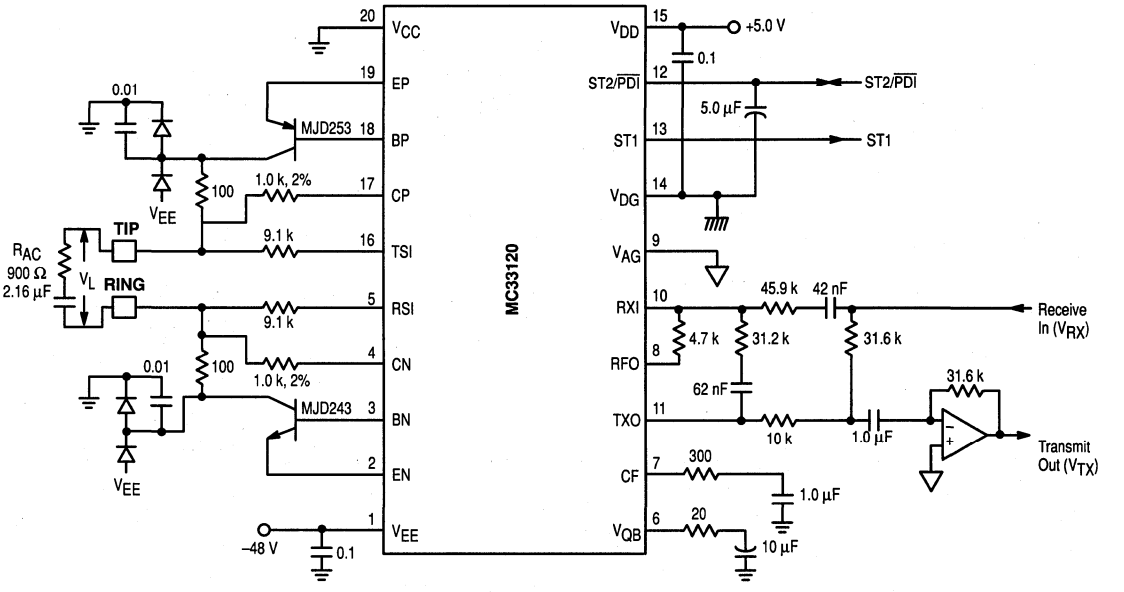


FIGURE 48 — 220 Ω + 820 Ω//0.115 μF SYSTEM

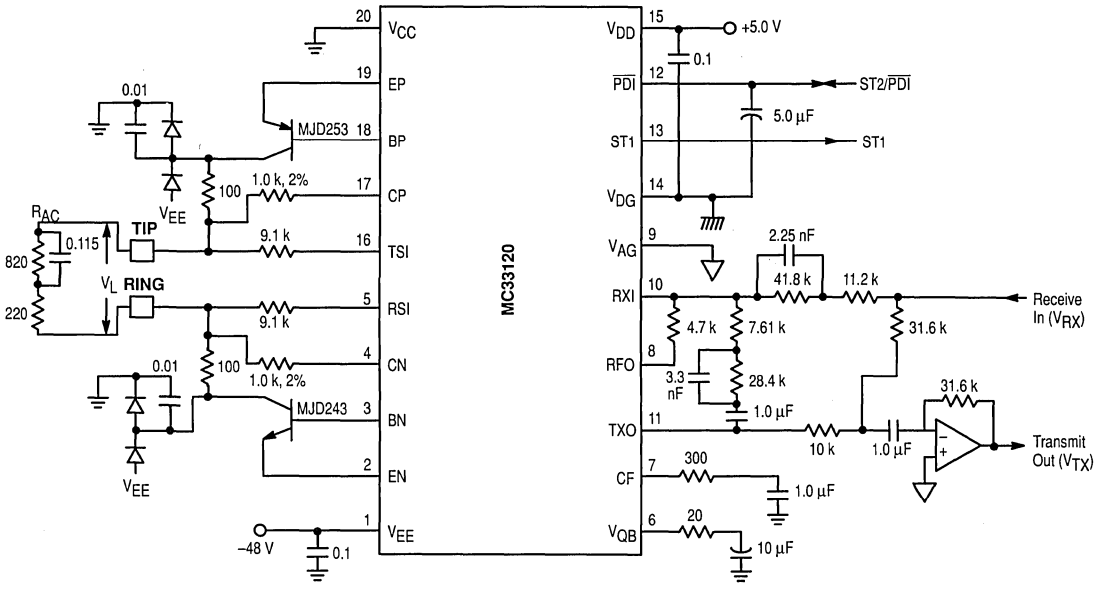


FIGURE 49 — CIRCUIT PERFORMANCE, 600 Ω SYSTEM

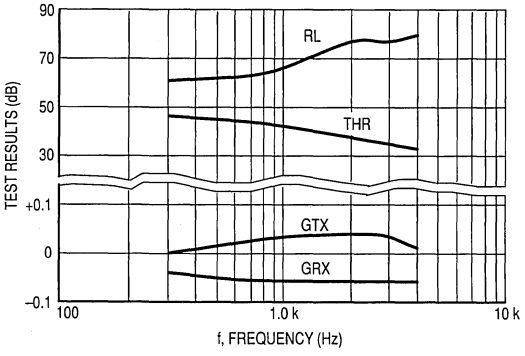


FIGURE 50 — CIRCUIT PERFORMANCE
900 Ω + 2.16 μF SYSTEM

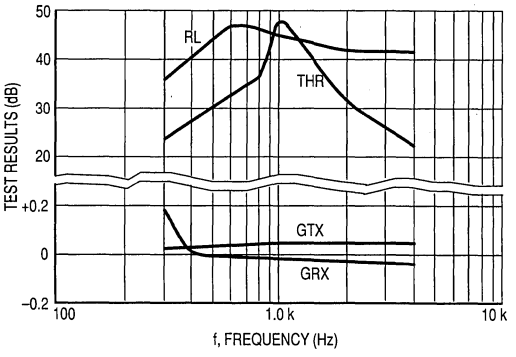


FIGURE 51 — CIRCUIT PERFORMANCE
820 Ω//0.115 μF + 220 Ω SYSTEM

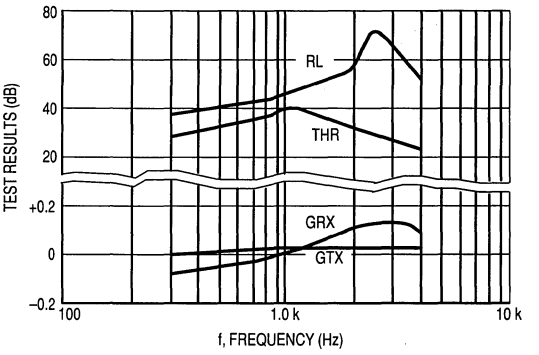
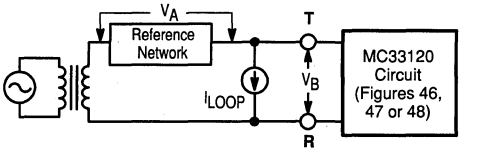


FIGURE 52 — RETURN LOSS TEST CIRCUIT
FOR FIGURES 46 TO 51



Reference Network = R_{AC} of Figures 46 to 48.

Return Loss = $20 \log \left| \frac{V_A + V_B}{V_A - V_B} \right|$

GLOSSARY

ATTENUATION — A decrease in magnitude of a communication signal, usually expressed in dB.

BALANCE NETWORK — That part of the SLIC circuit which provides transhybrid rejection.

BANDWIDTH — The range of information carrying frequencies of a communication system.

BATTERY — The voltage which provides the loop current, and in some cases powers the SLIC circuit. The name derives from the fact that COs have always used batteries, in conjunction with AC power, to provide this voltage.

BATTERY FEED RESISTANCE — The equivalent Thevenin DC resistance of the SLIC circuit for supplying loop current. Traditionally it is 400 Ω.

C-MESSAGE FILTER — A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

CENTRAL OFFICE — Abbreviated CO, it is a main telephone office, usually within a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A typical CO can handle up to 10,000 subscriber numbers.

CODEC — Coder/Decoder — Interfacing between the SLIC and the digital switch, it converts the SLIC's transmit signal to digital, and converts the digital receive signal to analog.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

$$10 \bullet \log (P_1 / P_2)$$

for power measurements, and

$$20 \bullet \log (V_1 / V_2)$$

for voltage measurements.

dBm — An indication of signal power. 1.0 mW across 600 Ω, or 0.775 V rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:

dBm = 20 • log (Vrms/0.775), or
dBm = [20 • log (Vrms)] + 2.22.

dBmp — Indicates dBm measurement using a psophometric weighting filter.

dBrn — Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = –90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

DTMF — Dual Tone Multifrequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a keypad.

FAULT — An incorrect condition where Tip is accidentally connected to the battery voltage, or Ring is connected to ground, or both. The most common fault is Ring to ground.

FOUR WIRE CIRCUIT — The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the transmit path, and one pair is for the receive path.

FULL DUPLEX — A transmission system which permits communication in both directions simultaneously. The standard handset telephone system is full duplex.

GAIN — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

HALF DUPLEX — A transmission system which permits communication in one direction at a time. CB radios, with "push-to-talk" switches, and voice activated speakerphones, are half duplex.

HOOKSWITCH — A switch, within the telephone, which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

HYBRID — Another name for a two-to-four wire converter.

IDLE CHANNEL NOISE — Residual background noise when transmit and receive signals are absent.

LINE CARD — The PC board and circuitry in the CO or PBX which connects to the subscriber's phone line. A line card may hold circuitry for one subscriber, or a number of subscribers.

LONGITUDINAL BALANCE — The ability of the SLIC to reject longitudinal signals on Tip and Ring.

LONGITUDINAL SIGNALS — Common mode signals.

LOOP — The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally, it is a floating system not referred to ground, or AC power.

LOOP CURRENT — The DC current which flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20 to 120 mA.

OFF HOOK — The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the DC current as an indication that the phone is busy.

ON HOOK — The condition when the telephone is disconnected from the phone system, and no DC loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange. In effect, a miniature central office, it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

PROTECTION, PRIMARY — Usually consisting of carbon blocks or gas discharge tubes, it absorbs the bulk of a lightning induced transient by clamping the voltages to less than ±1500 V.

PROTECTION, SECONDARY — Usually located on the line card, it protects the SLIC and associated circuits from transient surges. Typically, it must be capable of clamping a ±1.5 kV surge of 1.0 ms duration.

PULSE DIALING — A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 per second. The old rotary phones, and many new pushbutton phones, use pulse dialing.

RECEIVE PATH — Within the CO or PBX it is the speech path from the internal switching system towards the phone line (Tip & Ring).

REN — Ringer Equivalence Number. An indication of the impedance or loading factor of a telephone bell or ringer circuit. An REN of 1.0 equals ≈8.0 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

RETURN LOSS — Expressed in dB, it is a measure of how well the SLIC's AC impedance matches the line's AC characteristic impedance. With a perfect match, there is no reflected signal, and therefore infinite return loss. It is calculated from:

$$RL = 20 \bullet \log \frac{(Z_{LINE} + Z_{CKT})}{(Z_{LINE} - Z_{CKT})}$$

RING — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

SLIC — Subscriber Line Interface Circuit. It is the circuitry within the CO or PBX which connects to the user's phone line.

SUBSCRIBER — The customer at the telephone end of the line.

SUBSCRIBER LINE — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

TIP — One of the two wires connecitng the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

TRANSHYBRID REJECTION — The rejection (in dB) of the reflected signal in the transmit path resulting from a receive signal applied to the SLIC.

TRANSMIT PATH — Within the CO or PBX it is the speech path from the phone line (Tip & Ring) towards the internal switching system.

TWO WIRE CIRCUIT — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

TWO-TO-FOUR WIRE CONVERTER — A circuit which has four wires (on one side) — two (signal & ground) for the outgoing signal, and two for the incoming signal. The outgoing signal is sent out differentially on the two wire side (the other side), and incoming differential signals received on the two wire side are directed to the four wire side. Additional circuit within cancels the reflected outgoing signal to keep it separate from the incoming signal.

VOICEBAND — That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300 to 3400 Hz.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33121

Low Voltage Subscriber Loop Interface Circuit

LOW VOLTAGE SUBSCRIBER LOOP INTERFACE CIRCUIT (SLIC)

THIN FILM SILICON MONOLITHIC INTEGRATED CIRCUIT

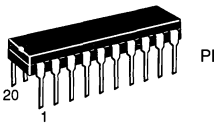
The MC33121 is designed to provide the interface between the 4-wire side of a central office, or PBX, and the 2-wire subscriber line. Interface functions include battery feed, proper loop termination AC impedance, hookswitch detection, adjustable transmit, receive, and transhybrid gains, and single/double fault indication. Additionally, the MC33121 provides a minimum of 58 dB of longitudinal balance (4-wire and 2-wire).

The transmit and receive signals are referenced to analog ground, while digital signals are referenced to digital ground, easing the interface to codecs, filters, etc. The 2 status outputs (hookswitch and faults) and the Power Down Input are TTL/CMOS compatible. The Power Down Input permits local shutdown of the circuit.

Internal drivers allow the external loop current pass transistors to be standard bipolar transistors (non-Darlington).

The MC33121 is available in a 20 pin DIP and a 28 pin PLCC surface mount package.

- 58 dB Longitudinal Balance Guaranteed; 4-wire and 2-wire
- Transmit, Receive, and Transhybrid Gains Externally Adjustable
- Return Loss Externally Adjustable
- Proper Hookswitch Detection With 30 kΩ Leakage
- Single/Double Fault Indication With Shutdown for Thermal Protection
- Critical Sense Resistors Included Internally
- Standard Power Supplies: – 21.6 V to – 42 V, and + 5.0 V, ± 10%
- On-Hook Transmission
- Power Down Input (TTL and CMOS Compatible)
- Operating Ambient Temperature: – 40°C to + 85°C
- Available in a 20 Pin DIP and 28 Pin PLCC Package



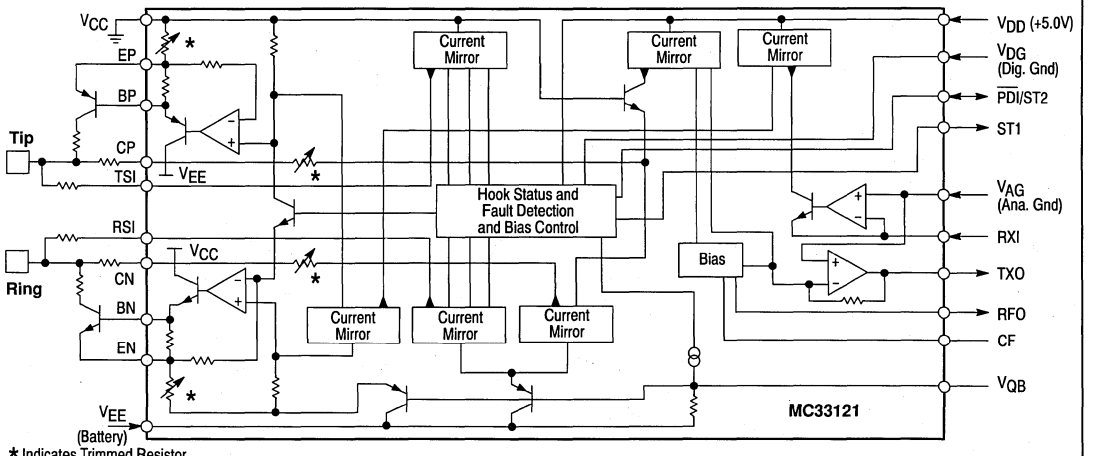
P SUFFIX
PLASTIC PACKAGE
CASE 738

FN SUFFIX
PLCC
CASE 776

ORDERING INFORMATION

Device	Temperature Range	Package
MC33121P	– 40° to + 85°C	Plastic DIP
MC33121FN		PLCC

SIMPLIFIED BLOCK DIAGRAM



MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage (with respect to V_{CC}) (with respect to V_{DG})	 V_{EE} V_{DD}	 – 60, +0.5 – 0.5, +7.0	Vdc
Voltage @ PDI, (with respect to V_{DG}) @ CP, CN EP, TSI BP RSI, EN BN	V_{in}	 – 0.5, +7.0 V_{EE} – 0.5, V_{CC} +0.5 V_{CC} – 7.0, V_{CC} +0.5 V_{CC} – 14, V_{CC} +0.5 V_{EE} – 0.5, V_{EE} +14 V_{EE} – 1.0, V_{EE} +21	Vdc
Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	– 65 to +150	°C

Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage (with respect to V_{CC}) (with respect to V_{DG})	 V_{EE} V_{DD}	 – 42 +4.5	 – 24 +5.0	 – 21.6 +5.5	Vdc
(with respect to V_{CC}) (with respect to V_{CC}) (with respect to V_{AG})	V_{AG} V_{DG}	– 3.0 – 3.0 – 3.0	0 0 0	+10 +7.0 +10	
(with respect to V_{EE}) (with respect to V_{CC} and V_{AG})	V_{DD}	— 3.5	— —	47.5 —	
Loop Current	I_L	15	—	50	mA
PDI Input Voltage	V_{PDI}	0	—	V_{DD}	Vdc
Sink Current ST1 ST2	 I_{ST1L} I_{ST2L}	 0 0	 — —	 1.0 1.0	mA
Transmit Signal Level at Tip & Ring Receive Signal Level at V_{RX}	S_{TX} S_{RX}	– 48 – 48	— —	+3.0 +3.0	dBm
Loop Resistance V_{EE} = – 42 V V_{EE} = – 24 V	R_L	0 0	— —	2.0 k 800	Ω
External Transistor Beta	H_{fe}	40	—	500	A/A
Operating Ambient Temperature (See text for derating)	T_A	– 40	—	+85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (V_{EE}= – 24 V, V_{DD}= +5.0 V, unless otherwise noted. V_{CC}=V_{AG}=V_{DG}= 0 V, T_A= 25°C, see Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLIES					
V_{EE} Current On Hook (R_L > 10 MΩ, V_{EE} = – 42 V) Off Hook (R_L = 0 Ω, V_{EE} = – 42 V)*	 I_{EEN} I_{EEF}	 – 2.7 – 72	 – 1.0 – 55	 — – 41	mA
V_{DD} Current On Hook (R_L > 10 MΩ, V_{DD} = +5.5 V) Off Hook (R_L = 0 Ω, V_{DD} = +5.5 V)	 I_{DDN} I_{DDF}	 — 4.0	 1.4 7.0	 2.7 14	
V_{EE} Ripple Rejection f = 1.0 kHz, @ V_{TX} (4-wire) f = 1.0 kHz, @ Tip/Ring (2-wire)	PSRR	 40 40	 62 52	 — —	dB
V_{DD} Ripple Rejection f = 1.0 kHz, @ V_{TX} (4-wire) f = 1.0 kHz, @ Tip/Ring (2-wire)		 37 37	 52 48	 — —	

*Includes loop current.

ELECTRICAL CHARACTERISTICS (V_{EE}= – 24 V, V_{DD}= +5.0 V, unless otherwise noted. V_{CC}=V_{AG}=V_{DG}= 0 V, T_A= 25°C, see Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
LOOP FUNCTIONS					
Loop Current					mA
Maximum (RRF = 4.7 k, R_L = 10 Ω)	$I_{L(max)}$	37	41	51	
Nominal (RRF = 4.7 k, R_L = 367 Ω)	I_L	21	27	34	
Minimum (RRF = 4.7 k, R_L = 796 Ω)	$I_{L(min)}$	16	17.5	—	
Battery Feed Resistance (RRF = 4.7 k, R_L = 796 Ω)*	R_{BF}	475	575	675	Ω
Hookswitch Threshold					kΩ
On-to-Off Hook	R_{NF}	2.0	4.1	—	
Off-to-On Hook	R_{FN}	—	7.7	10	
Fault Detection Threshold					Ω
Ring-to-Ground (R_L = 367 Ω)	R_{RG}	600	1100	—	
Tip-to-Battery (R_L = 367 Ω)	R_{TB}	600	1100	—	

*Calculated from [(24/$I_{L(min)}$) – 796]

GAIN LEVELS					
Transmit Voltage Gain (CP, CN to TXO)	G_{TX1}	—	0.328	—	V/V
Transmit Voltage Gain (V_{TX}/V_L)					dB
V_L = 0 dBm, f = 1.0 kHz	G_{TX2}	– 0.3	0	0.3	
V_L = 0 dBm, f = 3.4 kHz, with respect to G_{TX2}		– 0.1	0	0.1	
V_L = +3.0 dBm, f = 1.0 kHz, with respect to G_{TX2}		– 0.15	0	0.15	
V_I = – 48 dBm, f = 1.0 kHz, with respect to G_{TX2}		—	±0.1	—	
Transmit Distortion (at Pin 11)	THD_T				%
(f = 300 Hz to 4.0 kHz, – 40 dBm ≤ V_{T-R} ≤ +5.0 dBm)		—	0.05	—	
Receive Current Gain (I_{EP}/I_{RXI})	G_{RX1}	94	102	110	mA/mA
Receive Voltage Gain (V_L/V_{RXI}) (R_L = 600 Ω)					dB
V_{RXI} = 0 dBm, f = 1.0 kHz	G_{RX2}	– 0.3	0	0.3	
V_{RXI} = 0 dBm, f = 3.4 kHz, with respect to G_{RX2}		– 0.1	0	0.1	
V_{RXI} = +3.0 dBm, f = 1.0 kHz, with respect to G_{RX2}		– 0.15	0	0.15	
V_{RXI} = – 48 dBm, f = 1.0 kHz, with respect to G_{RX2}		—	±0.1	—	
Receive Distortion	THD_R	—	0.05	—	%
(f = 300 Hz to 4.0 kHz, – 40 dBm ≤ V_{RXI} ≤ +5.0 dBm)					
Return Loss (Reference = 600 Ω resistive, f = 1.0 kHz)	RL	30	>40	—	dB
Transhybrid Rejection (R_L = 600 Ω resistive, f = 1.0 kHz, Figure 4)	THR	—	44	—	dB
LONGITUDINAL SIGNALS (V_{CM} = 1.0 Vrms, see Figures 1 and 2)					
2-Wire Balance, f = 1.0 kHz, Z_{ac} = 600 Ω (@ Tip/Ring)	LB	58	64	—	dB
4-Wire Balance, f = 1.0 kHz, Z_{ac} = 600 Ω (@ V_{TX})		58	64	—	
2-Wire Balance, f = 330 Hz, Z_{ac} = 600 Ω (@ Tip/Ring)		58	64	—	
4-Wire Balance, f = 330 Hz, Z_{ac} = 600 Ω (@ V_{TX})		58	64	—	
2-Wire Balance, f = 3.3 kHz, Z_{ac} = 600 Ω (@ Tip/Ring)		53	60	—	
4-Wire Balance, f = 3.3 kHz, Z_{ac} = 600 Ω (@ V_{TX})		53	60	—	
2-Wire Balance, f = 1.0 kHz, Z_{ac} = 900 Ω (@ Tip/Ring)		—	62	—	
4-Wire Balance, f = 1.0 kHz, Z_{ac} = 900 Ω (@ V_{TX})		—	62	—	
Signal Balance, f = 1.0 kHz (Figure 3)		40	55	—	
Longitudinal Impedance, RS = 9100 Ω	Z_{Long}	150	180	210	Ω
Maximum Longitudinal Current, per side	$I_{Long(max)}$				mA
f = 1.0 kHz, I_{Loop} = $I_{L(min)}$, C_T = 0.1 μF		8.5	16	—	
V_{EE} = – 42, VCM = 5.12 Vrms					

ELECTRICAL CHARACTERISTICS (V_{EE}= – 24 V, V_{DD}= +5.0 V, unless otherwise noted. V_{CC}=V_{AG}=V_{DG}= 0 V, T_A= 25°C, see Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INTERFACE					
ST1 Output Voltage					Vdc
Low (I_{ST1} = 1.0 mA, V_{DD} = 5.5 V)	V_{OL}	V_{DG}	0.17	0.4	
High (I_{ST1} = – 100 µA, V_{DD} = 4.5 V)	V_{OH}	2.4	3.2	—	
ST2 Output Voltage					
Low (I_{ST2} = 1.0 mA, V_{DD} = 5.5 V)	V_{OL}	V_{DG}	0.17	0.4	
High (I_{ST2} = – 100 µA, V_{DD} = 4.5 V)	V_{OH}	2.4	4.3	—	
Time Delay					µs
Hookswitch Closure to ST1 Change	t_{ST11}	—	10	—	
Hookswitch Opening to ST1 Change	t_{ST12}	—	200	—	
Hookswitch Closure to 90% of Loop Current (C_T = 0.1 µF)	t_{HS}	—	19	—	ms
PDI Taken High-to-Low to 10% of Loop Current	t_{ST21}	—	18	—	ms
PDI Taken Low-to-High to 90% of Loop Current	t_{ST22}	—	10	—	µs
PDI Input Current	I_{IH}				µA
V_{PDI} = 3.0 V, R_L = 367 Ω, V_{DD} = 5.0 V		– 1250	– 800	– 300	
V_{PDI} = 0 V, R_L = 367 Ω, V_{DD} = 5.5 V		—	– 800	—	
PDI Input Voltage					Vdc
Low	V_{IL}	V_{DG}	—	0.8	
High	V_{IH}	2.0	—	V_{DD}	
MISCELLANEOUS					
V_{QB} Voltage (V_{QB} – V_{EE})	V_{QB}				Vdc
@ I_L = 20 mA		—	0.82	—	
@ I_L = 40 mA		—	0.95	—	
TXO Offset Voltage (V_{TXO} – V_{AG}) @ R_L = 600 Ω	V_{TXO}	– 400	+30	+400	mVdc
TXO Output Current	I_{TXO}	±275	±800	—	µA pk
RXI Offset Voltage (V_{RXI} – V_{AG}) @ R_L = 600 Ω	V_{RXOS}	—	0.8	—	mVdc
V_{AG} Input Current @ R_L = 600 Ω	I_{VAG}	—	0.2	—	µA
Idle Channel Noise (with C-message filter, R_L = 600 Ω)					dBrnc
@ TXO (Pin 11)	N_{IC4}	—	– 10	—	
@ Tip/Ring	N_{IC2}	—	– 5.0	—	
Thermal Resistance — Junction to Ambient	θ_{JA}				°C/W
(Either package, in still air, soldered to a PC board) (@ T_A = +25°C)		—	62	—	
(@ T_A = +85°C)		—	36	—	

Figure 1. Test Circuit

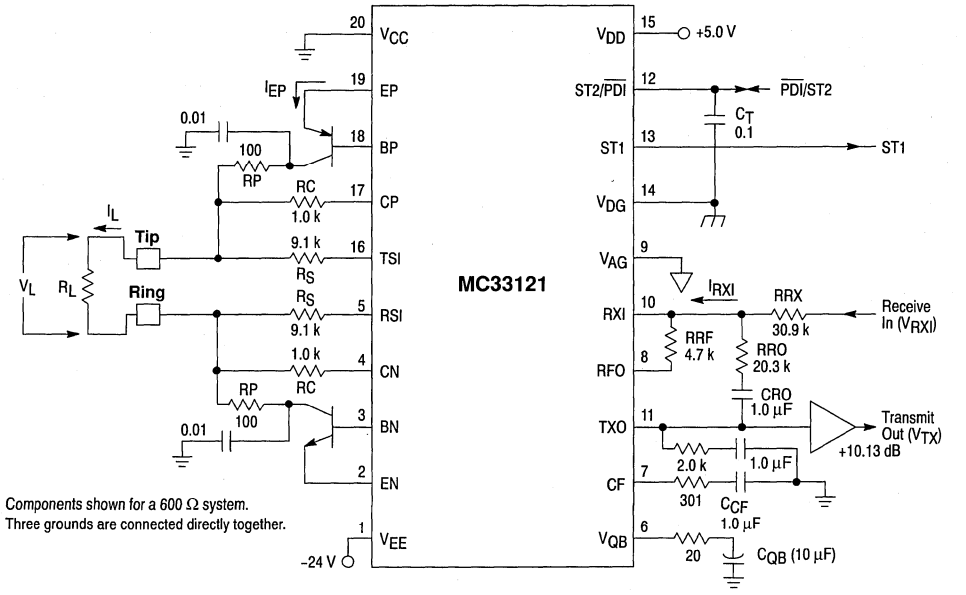


Figure 2. Longitudinal Balance Test

(Per IEEE-455)

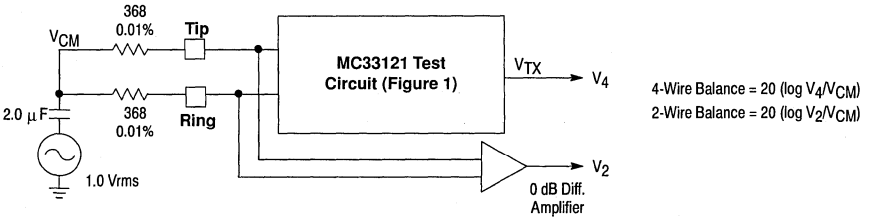


Figure 3. Signal Balance Test

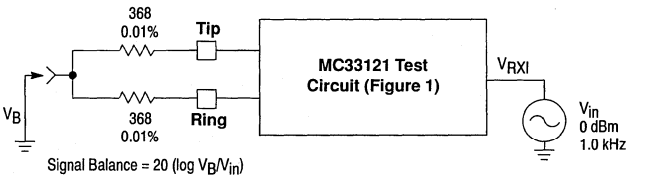
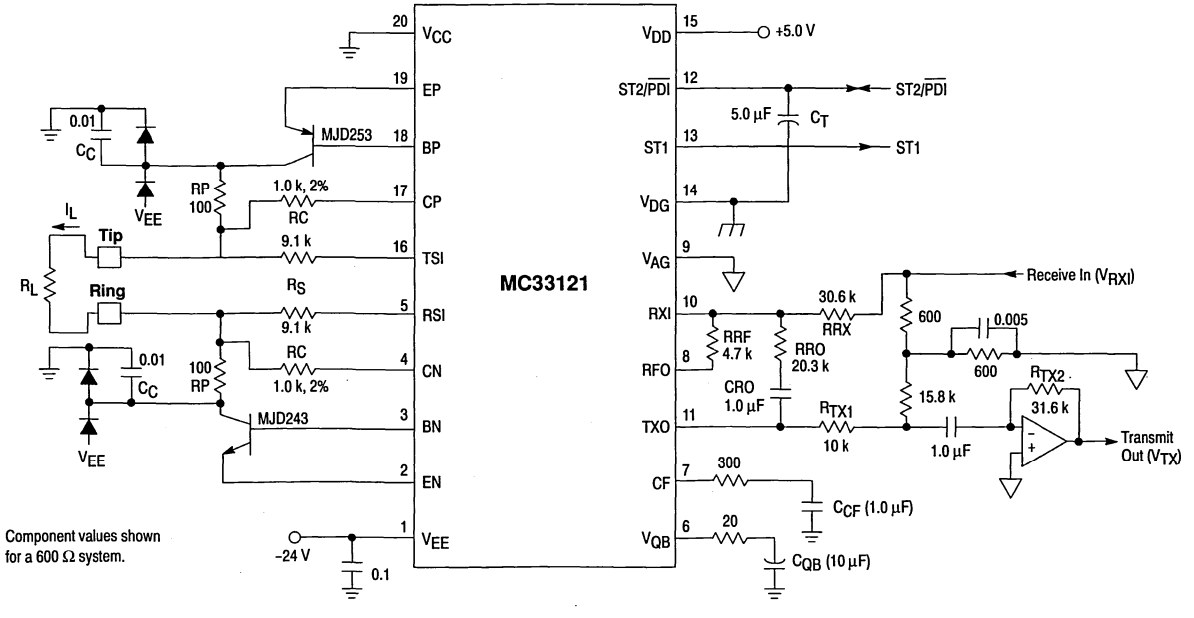


Figure 4. Application Circuit



PIN FUNCTION DESCRIPTION

Symbol	Pin		Description
	DIP	PLCC	
V_{CC}	20	28	Connect to noise-free battery ground. Carries loop current and some bias currents.
EP	19	27	Connect to the emitter of the PNP pass transistor.
BP	18	26	Connect to the base of the PNP pass transistor.
CP	17	24	Connect to TIP through a current limiting protection resistor (R_C). CP is the noninverting input to the internal transmit amplifier (Figure 28). Input impedance is 31 kΩ.
TSI	16	23	Sense input. Connect to TIP through a current limiting protection resistor (R_S) which also sets the longitudinal impedance. Input impedance is ≈100 Ω to V_{CC}.
V_{DD}	15	22	Connect to a +5.0 V, ±10% supply, referenced to digital ground. Powers logic section and provides some bias currents for the loop current drivers.
V_{DG}	14	20	Digital Ground. Reference for ST1, ST2 and V_{DD}. Connect to system digital ground.
ST1	13	18	Status Output (TTL/CMOS). Indicates hook switch status — high when on-hook, low when off-hook, and pulse dialing information. Used with ST2 to indicate fault conditions.
ST2/PDI	12	17	Status output and an input (TTL/CMOS). As an output, ST2 can indicate hook status — Low when on-hook, high when off-hook. Used with ST1 to indicate fault conditions. As an input, it can be taken low (when off-hook) to deny subscriber loop current.
TXO	11	16	Transmit voltage output. Amplitude is ≈1/3 that across CP and CN. Nominally capable of 800 μA output current. DC referenced to V_{AG}.
RXI	10	14	Receive current input. Current at this pin is multiplied by 102 at EP and EN to generate loop current. RXI is a virtual ground at V_{AG} level. Current flow is out of this pin.
V_{AG}	9	13	Analog ground, reference for TXO and RXI. Connect to system analog ground. Current flow is into this pin.
RFO	8	12	A resistor from this pin and RXI sets the maximum loop current and DC feed resistance. Minimum resistor value is 3.3 k (see Figures 5 to 7).
CF	7	10	A low leakage capacitor between this pin and V_{AG} provides DC and AC signal separation. A series resistor is required for battery supply turn-on/off transient protection (Figure 4).
V_{QB}	6	8	Quiet Battery. A capacitor between V_{QB} and V_{CC} filters noise and ripple from V_{EE}, providing a quiet battery source for the speech amplifiers. A series resistor is required for battery supply turn-on/off transient protection (Figure 4).
RSI	5	7	Sense input. Connect to RING through a current limiting protection resistor which also sets the longitudinal impedance. Input impedance is ≈100 Ω to V_{QB}.
CN	4	6	Connect to RING through a current limiting protection resistor. CN is the inverting input to the internal transmit amplifier (Figure 28). Input impedance is 31 kΩ.
BN	3	4	Connect to the base of the NPN pass transistor.
EN	2	3	Connect to the emitter of the NPN pass transistor.
V_{EE}	1	2	Connect to battery voltage (– 21.6 V to – 42 V).

(Pins 1, 5, 9, 11, 15, 19, 21, and 25 are not internally connected on the PLCC package.)

Figure 5. Loop Current versus Loop Resistance and RRF

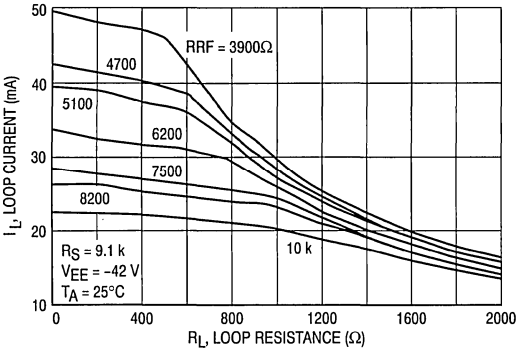


Figure 6. Loop Current versus Loop Resistance and RRF

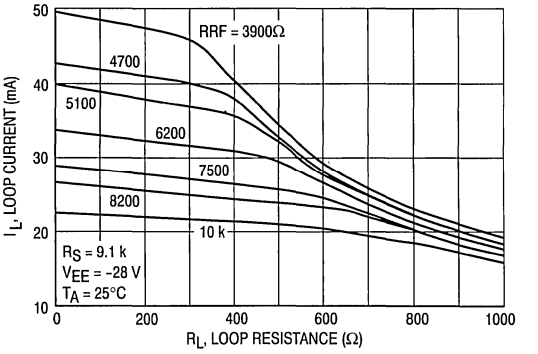


Figure 7. Loop Current versus Loop Resistance and RRF

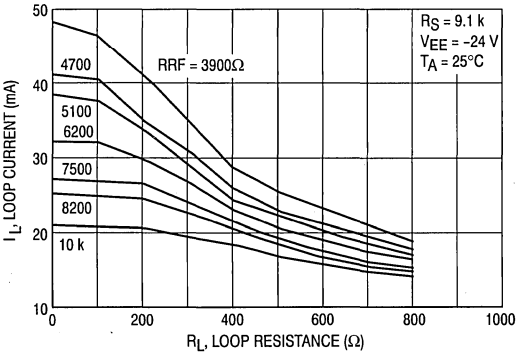


Figure 8. Off-Hook to On-Hook Threshold versus RRF

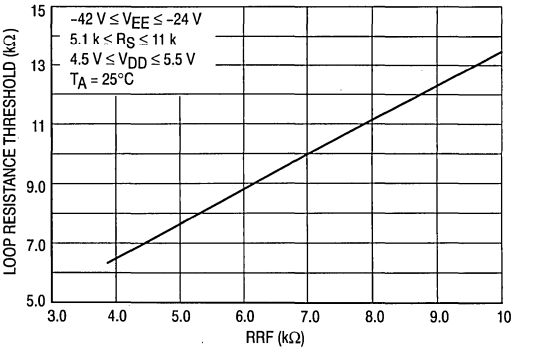


Figure 9. On-Hook to Off-Hook Threshold versus R_S

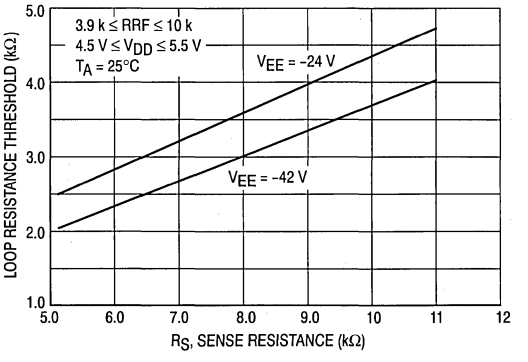


Figure 10. I_{DD} versus Loop Current

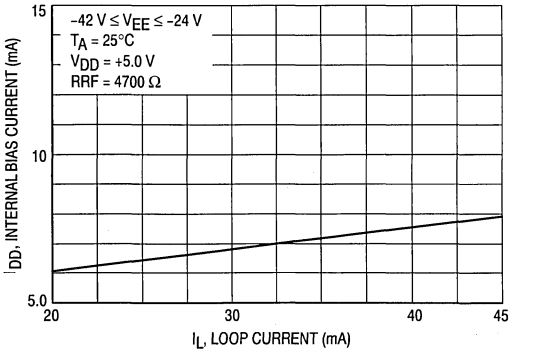


Figure 11. Fault Threshold (On-Hook) versus R_S

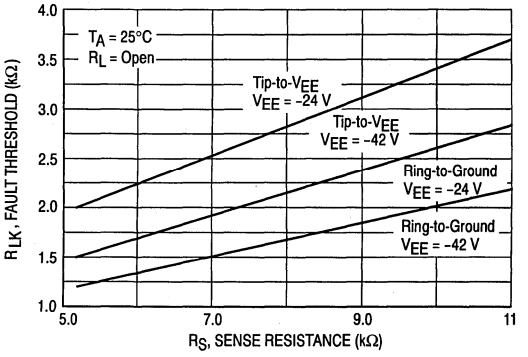


Figure 12. Fault Threshold (Off-Hook) versus Loop Resistance

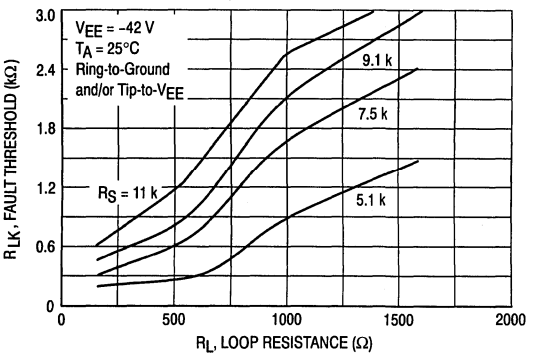


Figure 13. Fault Threshold (Off-Hook) versus Loop Resistance

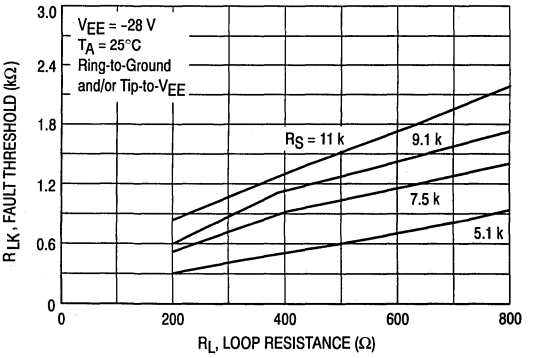


Figure 14. Fault Threshold (Off-Hook) versus Loop Resistance

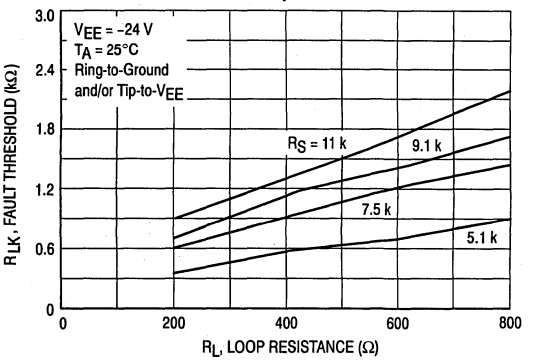


Figure 15. Fault Threshold (Off-Hook) versus R_S

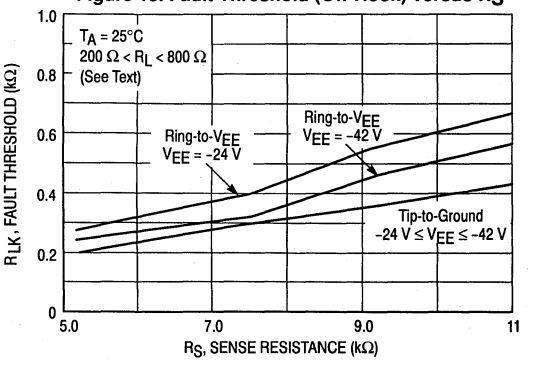


Figure 16. V_{DD} Ripple Rejection versus Frequency

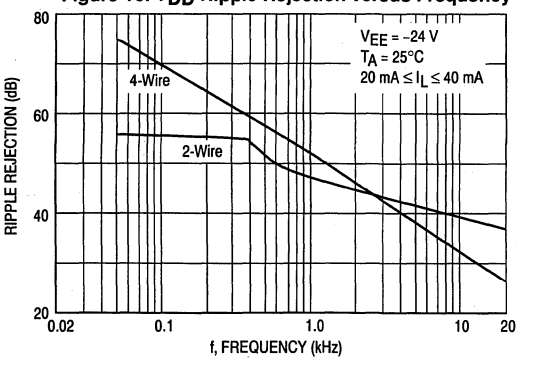


Figure 17. V_{EE} Ripple Rejection versus Frequency

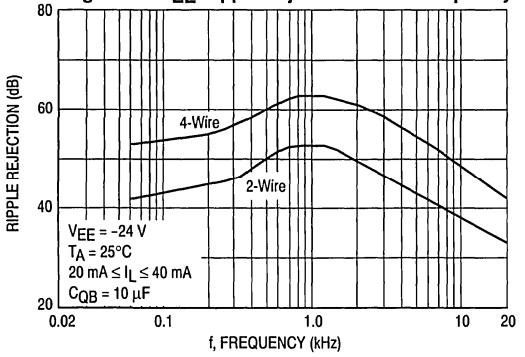


Figure 18. V_{EE} Ripple Rejection versus Frequency and C_{QB}

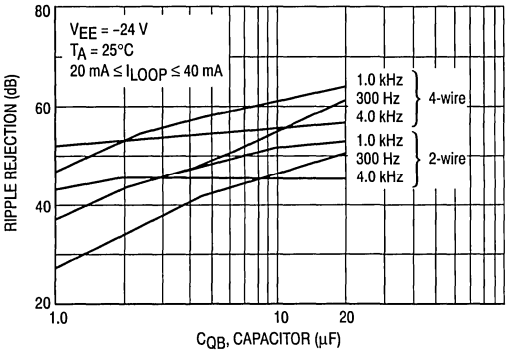


Figure 19. ST1, V_{OL} versus I_{OL}

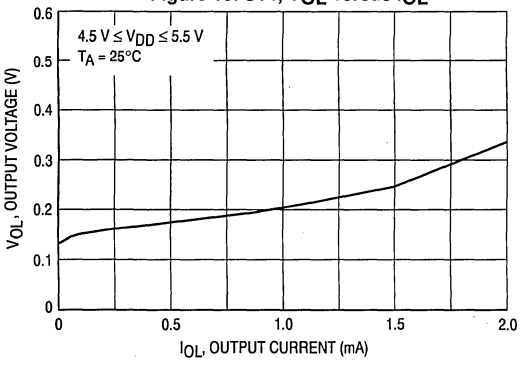


Figure 20. ST1, V_{OH} versus I_{OH}

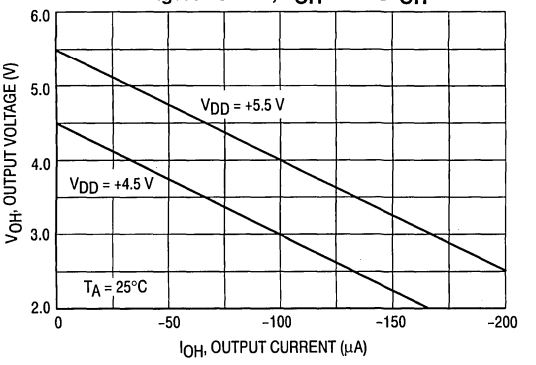


Figure 21. ST2, V_{OL} versus I_{OL}

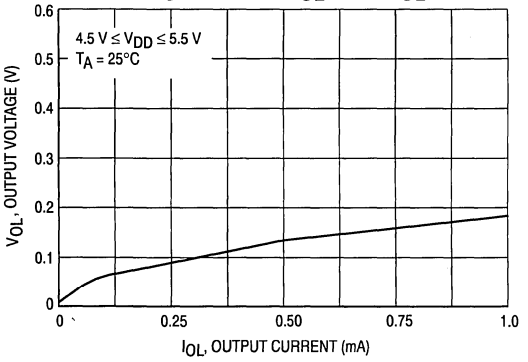


Figure 22. ST2, V_{OH} versus I_{OH}

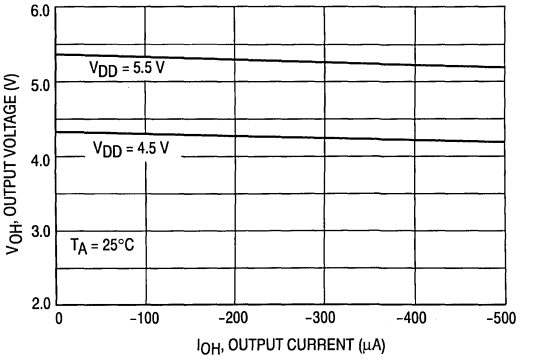


Figure 23. IC Power Dissipation versus Loop Resistance and RRF

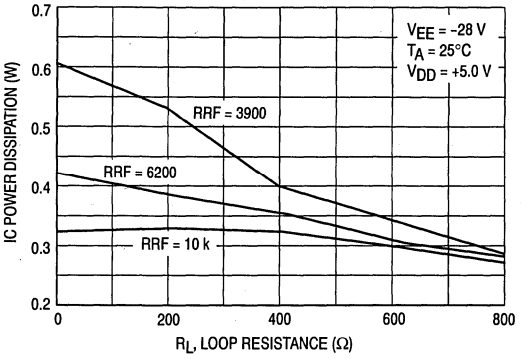


Figure 24. Transistor Power Dissipation versus Loop Resistance and RRF

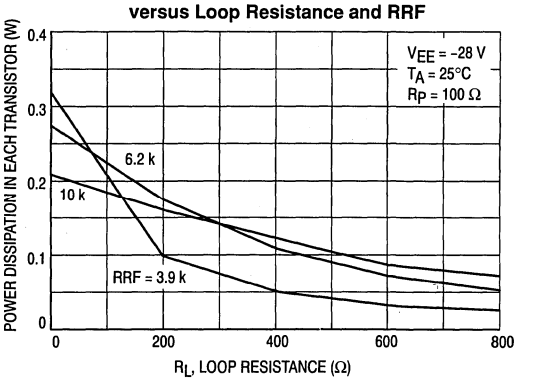


Figure 25. Maximum Longitudinal Current versus Loop Current

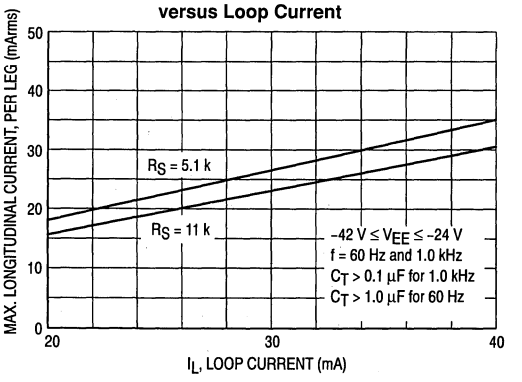
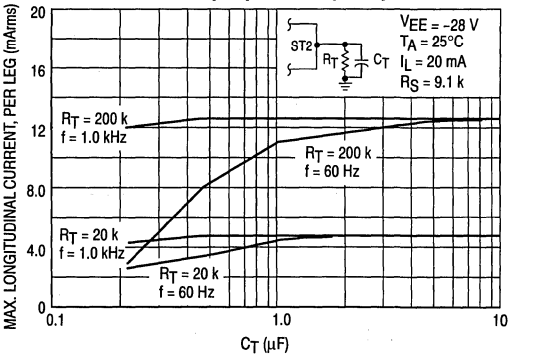


Figure 26. Maximum Longitudinal Current versus C_T, R_T and Frequency



FUNCTIONAL DESCRIPTION

Introduction

The MC33121 is a solid state SLIC (Subscriber Line Interface Circuit) which provides the interface between the two wire telephone line and the four wire side of a Central Office or PBX. Most of the BORSCHT functions are provided, specifically:

— **B**attery feed of the loop current to the line, with programmable maximum current for short lines and battery feed resistance for long lines.
— **O**vervoltage protection through internal clamp diodes and external resistors and diodes.
— **S**upervision, in that hook status is indicated in the presence of ≥30 kΩ leakage, and regardless of whether or not the circuit is powered down intentionally by the Central Office or PBX. Fault conditions are detected and indicated to the system. Dialing (pulse and DTMF) information is passed through the MC33121 to the 4-wire side.
— **H**ybrid function, in that the MC33121 is a 2-to-4 wire converter. Transmit, receive, return loss, and transhybrid gains are independently adjustable.

The MC33121 does not provide ring insertion, ring trip, digital coding/decoding of the speech signals, nor test functions. These must be provided external to this device.

The MC33121 controls two external transistors (one NPN and one PNP) through which the loop current flows. By appropriate circuit design, the power dissipation (which can exceed 3.0 W under certain worst case conditions) is approximately equally distributed among the two transistors and the IC, thereby lowering junction temperatures and increasing long term reliability. In most situations, heatsinks will not be required.

The MC33121 incorporates critical sense resistors internally, which are trimmed for optimum performance. With this technique, the external resistors on the two wire side, which generally must be high wattage for transient protection reasons, can be non-precision.

Longitudinal balance is tested to a minimum of 58 dB @ 1.0 kHz (refer to Electrical Characteristics and Figure 2) for both the two-wire and four-wire side, and typically measures in the mid-60s. The longitudinal current capability is tested to a minimum of 8.5 mArms per side (refer to Electrical Characteristics and Figure 2) at a loop current of 20 mA.

Following is a description of the individual sections. Figure 4 is the reference schematic.

DC Loop Current

The DC loop current is determined by the battery voltage (V_{EE}), the load resistance across Tip and Ring, and the resistor at RFO. Varying the 4 resistors R_S and RC will influence the loop current a small amount (<5%). The curves of Figures 5 to 7 indicate the loop current versus loop resistance, different values of RRF, and for various values of V_{EE}. The graphs represent performance at T_A = 25°C and after the IC had reached a steady state temperature (>5 minutes).

Figure 27. DC Loop Current Path

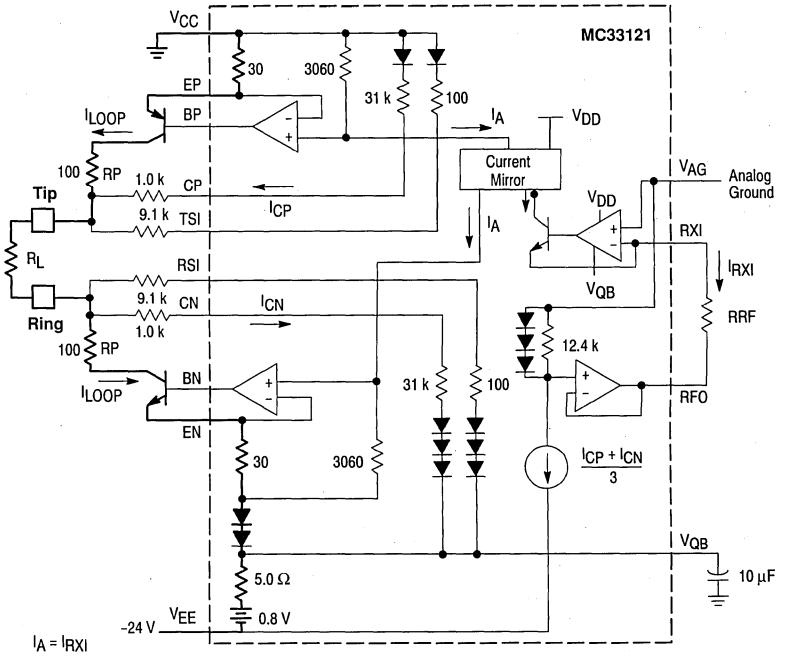


Figure 27 is representative of the DC loop current path (bold lines). On a long line (R_L > 400 Ω), the loop current can be determined from the following equation:

$$I_L = \frac{(|V_{EE}| - 3.6\ V) \bullet 13}{RRF + \{(R_L + 5) \bullet 13\}} \quad (1)$$

On short lines (R_L < 400 Ω), the three diodes across the 12.4 k resistor clamp the voltage at RFO, thereby preventing the RXI current from increasing as the load resistance is decreased. The maximum loop current is:

$$I_{L(max)} = \frac{1.85\ V \bullet 102}{RRF} \ (T_A = 25°C) \quad (2)$$

Due to the temperature dependence of a diode's forward voltage, the maximum loop current will change with temperature by ≈ –0.3%/°C.

The battery feed resistance ($\Delta V_{TIP}/\Delta I_L$) is ≈400 Ω, but depends on the loop current, V_{EE}, RRF, and is a valid parameter only on long lines where the current limit is not in effect. On short lines, the feed resistance is high since the loop current is clamped at a near constant level. The AC impedance (Return Loss) however, is not determined nor affected by the DC parameters. See the Applications Section for Return Loss information.

Transmit Path

The transmit path, shown in Figure 28, consists of an internal amplifier which has inputs at CP and CN, and its output at TXO. The gain is internally fixed at 0.328 V/V (–9.7 dB). The output is in phase with the signal at CP (normally the same as TIP), and is out of phase with the signal at CN. The signal at TXO is also out of phase with that at V_{RX}, the receive signal input, described in another section.

The TXO output can swing ≈3.0 Vp-p, with a nominal current capability of ±800 μA peak (±275 μA minimum). The load on TXO is the parallel combination of RTX1 and the RRO network (described later). TXO is nominally internally biased at the V_{AG} DC level, but has an offset which varies with loop current.

In normal applications, the signal at CP/CN is reduced slightly from that at Tip/Ring by the voltage divider composed of the external RC resistors, and the internal 31 k resistors. The value of the RC resistors depends on the transient protection needed, described in another section, with 1.0 kΩ resistors being suitable for most applications. The resulting signal at TXO needs to be gained up to obtain 0 dB from Tip/Ring to V_{TX} (the 4-wire output). The common method involves an external op amp, as shown in Figure 28, with a gain of RTX2/RTX1. The gain from V_L to V_{TX} is:

$$\frac{V_{TX}}{V_L} = \frac{RTX2 \bullet 31\ k \bullet 0.328}{RTX1 \bullet (RC + 31\ k)} \quad (3)$$

If a codec/filter is used, many of which include an internal op amp, a separate op amp is not needed. CTX is primarily for DC blocking (of the TXO offset), and is usually large (1.0 μF) so as to not affect the gain.

Receive Path

The receive path, shown in Figure 29, consists of the input at RXI, the transistor driver amplifiers, the external transistors, and the load at Tip/Ring.

RXI is a virtual ground (DC level = V_{AG}) and is a current input. Current flow is out of the pin. The RXI current is mirrored to the two transistor drivers which provide a gain of 102. The two external transistors are then two current sources, in series, operating at the same value. An additional internal circuit (not shown) balances the two current sources to maintain operation in their linear region.

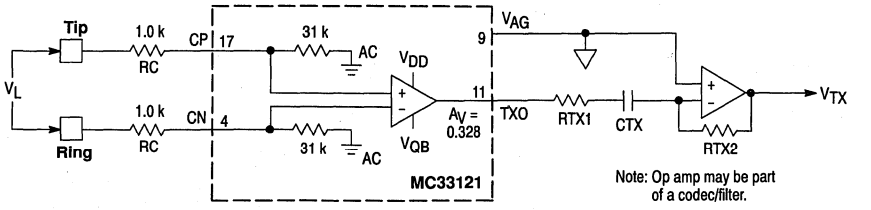
The load current (through R_L) is slightly different from the transistor current due to the sense resistors RC and RS. The sense resistors add to the DC loop current, but subtract from the AC load current.

In normal operation, the current at RXI is composed of a DC current (from RFO), an AC current (from V_{RX}) which is the receive signal, and an AC current from TXO, which is the feedback signal to set the return loss (setting the return loss is discussed in the section on AC Terminating Impedance). The resulting AC signal at Tip is inverted from that at V_{RX}, while the signal at Ring is in phase with V_{RX}.

The resistors RP are for transient protection, and their value (defined in another section) depends on the amount of protection required. A nominal value of 100 Ω is suitable for most applications.

The system receive gain, from V_{RX} to Tip/Ring, is not described in this section since in normal applications, it involves the feedback which sets the AC terminating impedance. The Applications Section discusses these in detail.

Figure 28. Transmit Path



Logic Interface (Hook status, pulse dialing, faults)

The logic interface section provides hookswitch status, fault information, and pulse dialing information to the 4-wire side of the system at the ST1 and ST2 outputs. Figure 30 is a representative diagram.

The logic outputs operate according to the truth table in Table 1:

Table 1. Status Output Truth Table

Hook Status	Fault Detection	Outputs		Circuit Condition
		ST 1	ST2	
On-Hook	No Fault	Hi	Lo	Internally powered down
Off-Hook	No Fault	Lo	Hi	Powered up
On-Hook	Fault	Lo	Lo	Internally powered down
Off-Hook	Fault	Lo	Lo	Internally powered down

Referring to Figure 30, ST1 is configured as an active NPN pulldown with a 15 kΩ pullup resistor. ST2 has a 800 µA current source pullup, and a 1.0 mA current source for a pulldown. Current limiting this output controls the discharge from the external capacitor when ST2 switches low.

The condition where both ST1 and ST2 are high is not valid, but may occur momentarily during an off-hook to on-hook transition. The condition where both ST1 and ST2 are low may occur momentarily during an on-hook to off-hook transition — this should not be interpreted as a fault condition. ST1 and ST2 are TTL/CMOS compatible and are powered by the +5.0 V supply (V_{DD}). Refer to the Applications Section for more details.

Power Supplies, Grounds

The MC33121 requires 2 power supplies: battery voltage between – 21.6 V and – 42 V (V_{EE}), and an auxiliary voltage between +4.5 V and +5.5 V (V_{DD}).

V_{EE} is nominally – 24 V, with a typical range of – 21.6 V to – 42 V, and must be referenced to V_{CC} (battery ground). A 0.1 µF bypass capacitor should be provided between V_{CC}

Figure 29. Receive Path

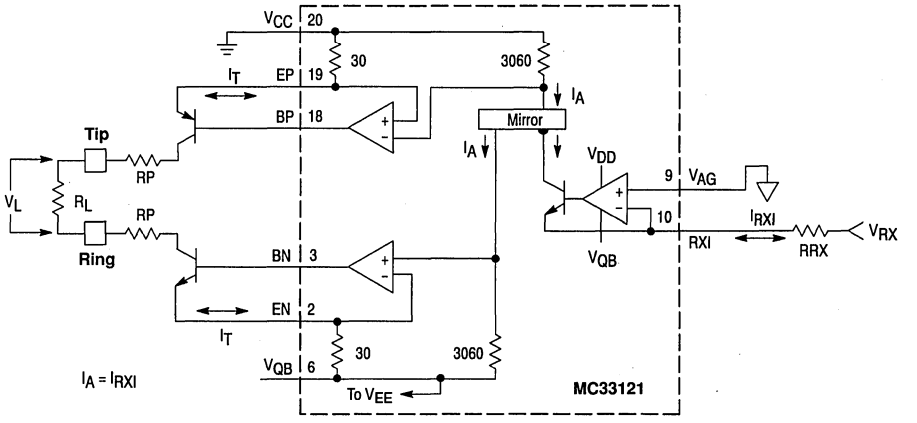
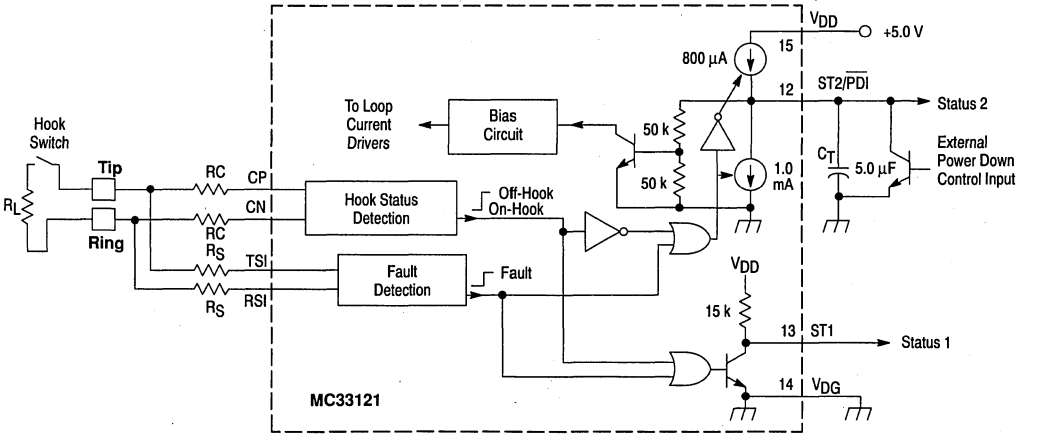


Figure 30. Logic Interface



and V_{EE}. The V_{EE} current (I_{EE}) is nominally 1.0 mA when on-hook, 8.0 to 12 mA more than the loop current when off-hook, and ≈5.0 mA when off-hook but powered down by using the PDI pin. Ripple and noise rejection from V_{EE} is a minimum of 40 dB (with a 10 μF capacitor at V_{QB}), and is dependent on the size and quality of the V_{QB} capacitor (C_{QB}) since V_{QB} is the actual internal supply voltage for the speech amplifiers. The absolute maximum for V_{EE} is – 60 V, and should not be exceeded by the combination of the battery voltage, its tolerance, and its ripple.

V_{DD} is normally supplied from the line card's digital +5.0 V supply, and is referenced to V_{DG} (digital ground). A 0.1 μF capacitor should be provided between V_{DD} and V_{DG}. The V_{DD} current (I_{DD}) is nominally 1.7 mA when on-hook and between 6.0 and 8.0 mA when off-hook (see Figure 10). When the MC33121 is intentionally powered down using the PDI pin, I_{DD} changes by <1.0 mA from the normal off-hook value.

V_{AG} is the analog ground for the MC33121, and is the reference for the speech signals (RXI and TXO). Current flow is **into** the pin, and is typically <0.5 μA.

Normally, V_{CC}, V_{DG} and V_{AG} are to be at the same DC level. However, if strong transients are expected at Tip and Ring, as in a Central Office application, or any application where the phone line is outdoors, V_{CC} should not be connected directly to V_{DG} and V_{AG} in order to prevent possible damage to the +5.0 V system. The MC33121 is designed to tolerate as much as ±30 V between V_{CC} and the other two grounds on a transient basis only. This feature permits V_{CC} and the other grounds to be kept separate (on an AC basis) on the line card by transient suppressors, or to be connected together farther into the system (at the power supplies). See the Applications Section on ground arrangements and transient protection for further information on connecting the MC33121 to the system supplies.

APPLICATIONS INFORMATION

This section contains information on the following topics:

Design Procedure ..... pg. 15
Power Dissipation Calculations and Considerations ..... pg. 22
Selecting the Transistors ..... pg. 23
Longitudinal Current Capability ..... pg. 23
PC Board Layout Considerations ..... pg. 23
Alternate Circuit Configurations ..... pg. 26

Design Procedure

This section describes the step-by-step sequence for designing in the MC33121 SLIC into a typical line card application for either a PBX or Central Office. The sequence is important so that each new component value which is calculated does not affect components previously determined. Figure 4 (Typical Application Circuit) is the reference circuit for most of this discussion. The recommended sequence (detailed below), consists of establishing the DC aspects first, and then the AC aspects:

1) Determine the maximum loop current for the shortest line, select RRF. Power dissipation must be considered here.
2) Select the main protection resistors (RP), and diodes, based on the expected transient voltages. Transient protection configuration must also be considered here.
3) Select RC based on the expected transient voltages.
4) Select RS based on the desired longitudinal impedance at Tip and Ring. Transient voltages are also a factor here.
5) Calculate RRO based on the desired AC terminating impedance (return loss).
6) Calculate RRX based on the desired receive gain.
7) Calculate RTX2 and RTX1 based on the desired transmit gain.
8) Calculate the balance resistor (RB), or network, as appropriate for desired transhybrid rejection.
9) Logic Interface

Preliminary

There is a primary AC feedback loop which has its main sense points at CP and CN (see Figure 34). The loop extends from there to TXO, through RRO to RXI, through the internal amplifiers to the transistor drivers, through RP to Tip and Ring, and through the RCs to CP and CN. Components within this loop, such as RP, RC, the transistors, and the compensation capacitors need not be tightly matched to each other in order to maintain good longitudinal balance. The tolerance requirements on these components, and others, are described in subsequent sections. Any components, however, which are placed outside the loop for additional line card functions, such as test relay contacts, fuses, resistors in series with Tip and Ring, etc. will affect longitudinal balance, signal balance, and gains if their values and mismatch is not carefully considered. The MC33121 cannot compensate for mismatch among components outside the loop.

The compensation capacitors (0.01 μF) shown at the transistor collectors (Figure 4) compensate the transistor driver amplifiers, providing the required loop stability. The required tolerance on these capacitors can be determined from the following guidelines:

- A 10% mismatch (±5% tolerance) will degrade the longitudinal balance by ≈1.0 dB on a 60 dB device, and by ≈3.0 dB on a 70 dB device.
- A 20% mismatch (±10% tolerance) will degrade the longitudinal balance by ≈3.0 dB on a 60 dB device, and by ≈6.0 dB on a 70 dB device.

High quality ceramic capacitors are recommended since they serve the secondary function of providing a bleedoff path for RF signals picked up on the phone line. These capacitors should be connected to a good quality RF ground.

The capacitors used at C_{QB} and C_F must be low leakage to obtain proper performance. Leakage at the C_{QB} capacitor will affect the DC loop current characteristics, while leakage at the C_F capacitor will affect the AC gain parameters, and possibly render the IC inoperative.

1) Maximum Loop Current and Battery Feed Resistance

The maximum loop current (at R_L = 0) is determined by the RRF resistor between RFO and RXI. The current limit is accomplished by three internal series diodes (see Figure 27) which clamp the voltage across RRF as the loop resistance decreases, thereby limiting the current at RXI. Since the loop current is 102 x $|I_{RXI}|$, the loop current is therefore clamped. The graphs of Figures 5 to 7 indicate the maximum

loop current at an ambient temperature of +25°C, and after the IC has reached thermal equilibrium (approx. 10 minutes).

Although the maximum loop current is primarily a function of the RRF resistor, it is also affected by ambient temperature, and slightly by V_{EE}. The ambient temperature effects are due to the temperature dependence of the diodes' forward voltage drop, causing the maximum loop current to change by $\approx -0.3\%/°C$. Changing V_{EE} affects the maximum current in that the power dissipation is changed, thereby changing the die temperature, which affects the diodes' voltage.

The maximum loop current is affected slightly (<5%) by the choice of the RS and RC resistors, since the sense currents through those resistors add to the current supplied by the transistors.

The battery feed resistance is determined by RRF, and is not adjustable independently of the current limit. Defined as $\Delta V_{TIP}/\Delta I_L$, it is ≈400 Ω, and is a valid parameter only on long lines where the current limit is not in effect. On short lines, the feed resistance is high since the loop current is clamped at a near constant level. The AC impedance (Return Loss) however, is not determined nor affected by these DC parameters. Return loss is discussed in another section.

If the application requires that the current limit value have a low temperature dependence, refer to the section following this design sequence which describes an alternate configuration.

2) Main Protection Resistors (RP) and Transient Currents

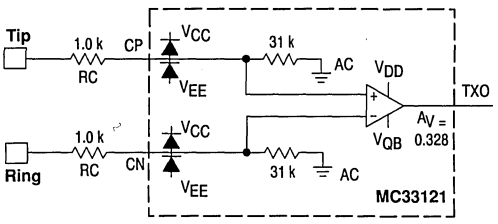
The purpose of the protection resistors (RP), along with the 4 clamp diodes shown in Figure 4, is to absorb the bulk of the transient energy when transient voltages come in from the phone line. The resistor value must be selected to limit the transient current to a value which can be tolerated by the diodes, while dissipating the energy. The recommended value shown (100 Ω) will limit the current from a 1500 V transient to 15 A, which can be carried by 1N4002 diodes under surge conditions. The resistors must be of a type which can tolerate the high instantaneous energy associated with transients. Resistor manufacturers should be consulted for this information.

Referring to Figure 4, a positive transient on either Tip or Ring, or both, will cause the transient current to be delivered to Ground. A negative transient will cause the transient current to come from the V_{EE} supply line. Therefore, the PC board track supplying V_{CC} and V_{EE} to the MC33121 must be designed to carry the transient currents as well as the normal operating currents. Additionally, since a negative transient will cause a current flow **out** of the power supply's negative output, which is opposite to the normal flow of current, provisions must be made for this reverse current flow. One suggested method is to place a zener transient suppressor (1N6287 for –42 V, 1N6282 for –28 V and –24 V) across the battery supply pins (V_{CC} to V_{EE}) physically adjacent to the MC33121. The inductance associated with PC board tracks and wiring will result in insufficient protection for the MC33121 if the suppressor is located at the opposite end of the line card, or at the power supplies.

Transient currents can be reduced by increasing the value of RP, with an upper limit determined by the DC conditions on the longest line (highest loop resistance) and minimum V_{EE} supply voltage. These conditions determine the minimum DC voltage across the transistors, which must be sufficient to handle the largest AC (transmit and receive) signals. If too large a value is selected for RP, the AC signals will be clipped. It is recommended that each transistor have no less than one volt (DC) across their collector to emitter. System AC specifications may require more than this.

Since the RP resistors are within the loop, their tolerance can be ±5% with no substantial degradation of longitudinal balance. A ±10% tolerance (20% mismatch) will degrade balance by ≈4.0 dB on a 65 dB device.

Figure 32. RC Protection Resistors



3) Selecting the RC Resistors

The primary purpose of the RC resistors is to protect the CP and CN pins from transient voltages and destructive currents. Internally, these pins have clamp diodes to V_{CC} and V_{EE} rated for a maximum of 1.0 A under surge conditions only (Figure 32). The 1.0 kΩ resistors shown in the figures, for example, will provide protection against surges up to 1.0 kV. Resistor manufacturers must be consulted for the proper type of resistor for this environment.

The RC resistors are in series with internal 31 kΩ resistors, and therefore form a voltage divider to the inputs of the transmit amplifier, as shown in Figure 32. This will affect the transmit gain, receive gain, return loss, and transhybrid rejection (described in subsequent sections). The tolerance of the RC resistors depends on the value selected for them, since any mismatch between them will create a differential voltage at CP and CN when longitudinal voltages are present on Tip and Ring. To ensure a minimum of 58 dB of longitudinal balance, the resistors' absolute value must not differ by more than 39 Ω. With a nominal value of 1.0 kΩ, their tolerance must be ±2%, or less. If their nominal value is 390 Ω or less, their tolerance can be ±5%.

4) Longitudinal Impedance (Z_{Long}) — Selecting the R_S Resistors

The longitudinal impedance is determined by the R_S resistors at the TSI and RSI pins according to the following equation:

$$Z_{Long} = \frac{R_S + 100}{51} \quad (4)$$

Z_{Long} is defined as V_{Long}/I_{Long} as shown in Figure 33; for R_S = 9.1 kΩ, Z_{Long} = 180 Ω. The calculated value of Z_{Long} includes the fact that the R_S resistors are in parallel with the synthesized impedance. The tolerance of the R_S resistors therefore depends on how much mismatch can be tolerated between the longitudinal impedances at Tip and at Ring. Calculations indicate the two R_S resistors can have a ±5% tolerance, and still comfortably provide a minimum of 58 dB longitudinal balance.

The resistors must be able to withstand transient voltages expected at Tip and Ring. The TSI and RSI pins have internal clamp diodes rated for a maximum of 1.0 A under surge conditions only (Figure 33). Resistor manufacturers must be consulted for the proper type of resistor for this environment.

5) AC Terminating Impedance and Source Impedance (Z_{ac}) — Return Loss

The return loss measurement is a measure of how closely the AC impedance of the SLIC circuit matches the characteristic impedance of the phone line, or a reference impedance. The reference impedance can be, in some cases, a pure resistance (commonly 600 Ω or 900 Ω), a series resistor and capacitor (900 Ω + 2.16 μF), or a more complex network. To achieve proper return loss with the MC33121, the RRO impedance shown in Figure 34 is to have the same configuration as the reference impedance, but with values scaled according to the equations mentioned below.

CRO, used primarily for DC blocking, is generally a large value (1.0 μF) so as to not affect the impedance of RRO. However, it can be included in the RRO network if a complex network is required.

Figure 33. Longitudinal Impedance

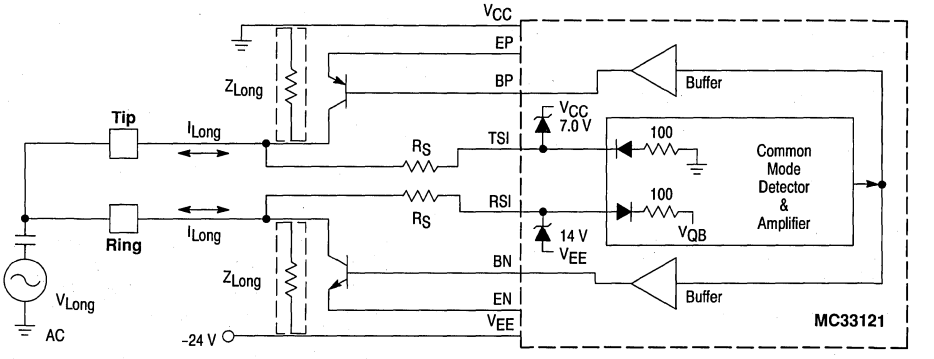
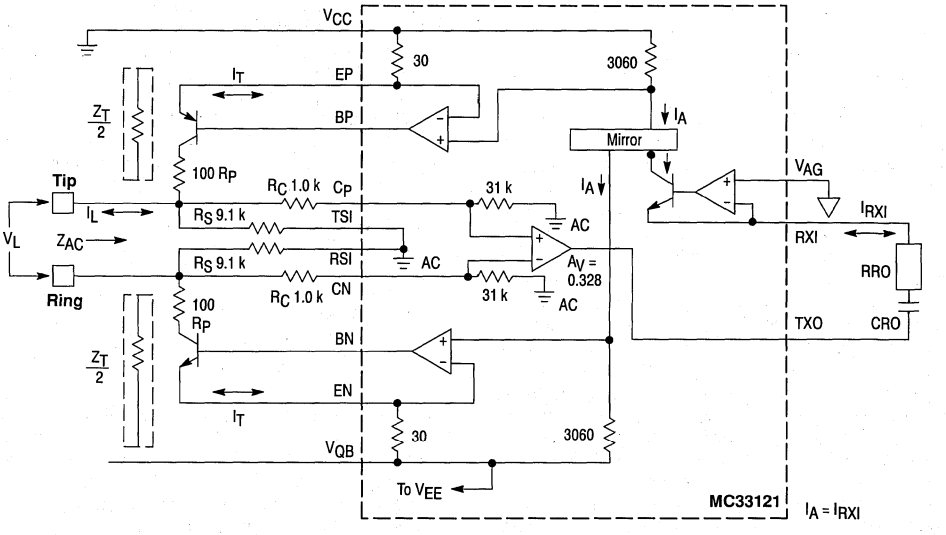


Figure 34. AC Terminating Impedance



Z_{ac} is the impedance looking into the circuit from Tip and Ring (set by RRO), and is defined as V_L/I_L. Half of Z_{ac} is from Tip to V_{CC}, and the other half is from Ring to V_{QB} (an AC ground). Each half is made up of a synthesized impedance ($Z_T/2$) in parallel with R_S and (RC + 31 k). Therefore, Z_{ac} is equal to:

$$Z_{ac} = [Z_T/2 \,//R_S//(RC + 31\ k)] \bullet 2 \qquad (5)$$

$$\text{and } \frac{Z_T}{2} = \frac{\{R_S//(RC + 31\ k)\} \bullet (Z_{ac}/2)}{\{R_S//(RC + 31\ k)\} - (Z_{ac}/2)} \qquad (6)$$

The synthesized impedance Z_T is created as follows:

An incoming signal V_L produces a differential voltage at CP and CN, and therefore at TXO equal to:

$$V_{TXO} = \frac{V_L \bullet 31\ k \bullet 0.328}{(RC + 31\ k)} \qquad (7)$$

The signal at TXO creates an AC current I_{RXI} through RRO. RXI is a virtual ground, and CRO is insignificant for first order calculations.

I_{RXI} is gained up by a factor of 102 to produce the current I_T through the transistors.

Z_T is therefore V_L/I_T. The relationship between Z_T and RRO is:

$$RRO = \frac{Z_T \bullet 1.037 \bullet 10^6}{(31\ k + RC)} \qquad (8)$$

While equation 8 gives the exact value for RRO, a first order approximation is $Z_{ac} \bullet 33.5$.

a) Resistive Loads (with RC = 1.0 k, R_S = 9.1 k):

For a 600 Ω resistive system, Z_T calculates to 626 Ω, and RRO calculates to 20.3 kΩ.

For a 900 Ω resistive system, Z_T calculates to 961 Ω, and RRO calculates to 31.14 kΩ.

b) Complex Loads

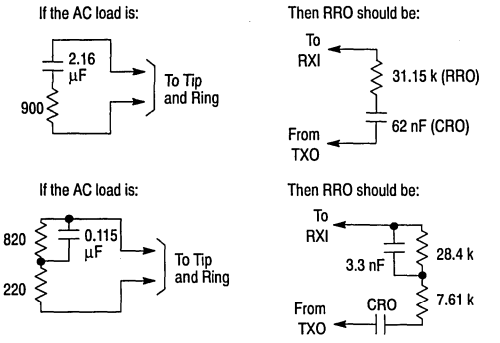
For complex (nonresistive) loads, the MC33121 must be made to look like a termination impedance equal to that complex load. This is accomplished by configuring RRO the same as the complex load, but with all impedance values increased according to the scaling factor of Equation 9.

$$SF = \frac{[(RC + 31\ k)//RS] \bullet 1.037 \bullet 10^6}{(RC + 31\ k) \bullet [(RC + 31\ k)//R_S - (Z_{ac}/2)]} \qquad (9)$$

Z_{ac} is computed at a nominal frequency of interest. A first order approximation of Equation 9 is:

$$SF = 1.037 \bullet 10^6/(RC + 31\ k) \qquad (9a)$$

For example:

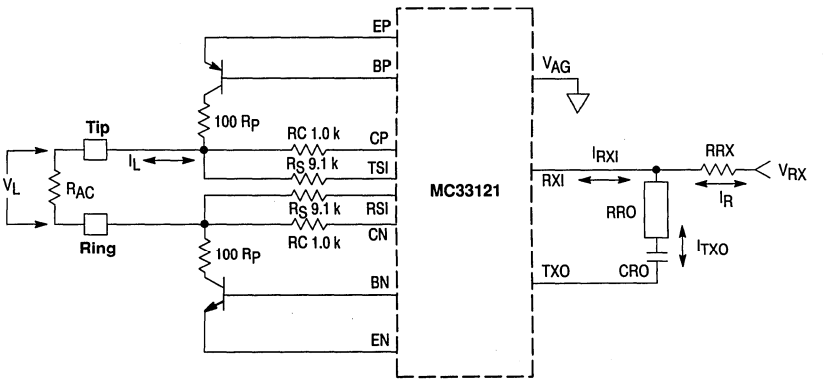


CRO must remain in series with the network to provide DC blocking. If the load network does not include a series capacitor (as in the second example above), CRO should be large (1.0 µF) so its impedance does not affect the RRO network. The above procedure will yield a return loss measurement which is constant with respect to frequency. The RRO resistor, or network, must have a tolerance equal to or better than the required system tolerance for return loss and receive gain.

6) Receive Gain (G_{RX})

The receive gain involves the same circuit as Figure 34, but with the addition of the RRX resistor (or network) which sets the receive gain. See Figure 35.

Figure 35. Receive Gain



The receive gain (G_{RX}), defined as the voltage gain from V_{RX} to V_L, is calculated as follows:

RXI is a virtual ground, and R_{ac} is the AC impedance of the load (phone line).

The AC current generated in the transistors is 102 • I_{RXI}, which is equal to 102 • ($I_R - I_{TXO}$).

$I_R = V_{RX}/RRX$, and

$$I_{TXO} = \frac{V_{TXO}}{RRO} = \frac{V_L \bullet 31\ k \bullet 0.328}{RRO \bullet (31\ k + RC)} \quad (10)$$

Using equations 5 and 8, involving Z_{ac}, RS and RC, and the above equations yields:

$$\frac{V_L}{V_{RX}} = G_{RX} = \frac{102 \bullet (R_{ac}//Z_{ac})}{RRX} \quad (11)$$

$$\text{Therefore, } RRX = \frac{102 \bullet (R_{ac}//Z_{ac})}{G_{RX}} \quad (12)$$

Equation 12 applies **only** for the case where R_{ac} and Z_{ac} have the same configuration. If they also have the same magnitude, then set RRX = 51 • R_{ac} to set a receive gain of 0 dB. The AC source impedance of the above circuit to Tip and Ring is Z_{ac}. For the case where $R_{ac} \neq Z_{ac}$, use the following equation:

$$\frac{V_L}{V_{RX}} = \frac{102}{RRX \bullet \left[\frac{1}{Z_L} + \frac{1.037 \bullet 10^6}{(31k + RC) \bullet RRO}\right]} \quad (13)$$

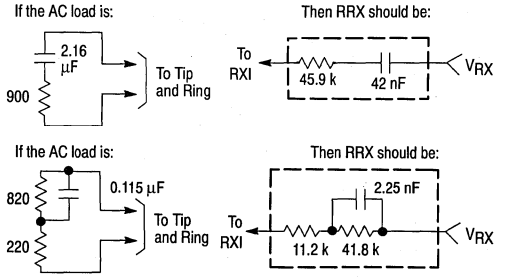
$$\text{where } Z_L = \left[\frac{R_{ac}}{2} // R_S // (RC + 31\ k)\right] \bullet 2 \quad (14)$$

a) Resistive Loads

For a 600 Ω resistive system, set RRX = 30.6 kΩ, and for a 900 Ω resistive system, set RRX = 45.9 kΩ.

b) Complex Loads

For complex (nonresistive) loads, the RRX resistor needs to be replaced with a network having the same configuration as the complex load, but with all impedance values scaled up by a factor of 51 (for 0 dB gain). If a gain other than 0 dB is desired, the scaling factor is determined from Equation 12. This method applies **only** if the RRO network has been made complex comparable to the load according to the procedure in the previous section (Equations 5-9a), such that $R_{ac} = Z_{ac}$. Using a scaling factor of 51, and the previous examples, yields:



The preceeding procedure will yield a receive gain which is constant with respect to frequency. The RRX resistor, or network, must have a tolerance equal to or better than the required system tolerance for receive gain.

7) Transmit Gain (G_{TX})

Setting the transmit gain involves selecting RTX1 and RTX2 in Figure 28. The voltage gain from V_L to V_{TX} is calculated from the following:

$$G_{TX} = \frac{V_{TX}}{V_L} = \frac{RTX2 \bullet 31\ k \bullet 0.328}{RTX1 \bullet (RC + 31\ k)} \quad (15)$$

For 0 dB gain, set RTX2 = 3.15 x RTX1 (for RC = 1.0 k). The actual values of RTX2 and RTX1 are not critical — only their ratio so as to provide the proper gain at the op amp. Once the ratio is established, the two resistors can be selected from a set of standard resistor values. The minimum value for RTX1 is limited by the drive capability of TXO, which is a nominal ±800 µA peak (±275 µA minimum). As a general rule, RTX1 should be between 5.0 kΩ and 20 kΩ. The load on TXO is the parallel combination of RTX1 and RRO.

CTX is for DC blocking, and is typically a large value (1.0 µF) so as to not be a significant impedance. In general, it should **not** be used for low frequency rolloff as that will affect the transhybrid rejection (discussed in the next section). Low frequency rolloff should be done after the op amp. High frequency roll-off can be set by placing a capacitor across RTX2.

For complex loads (at Tip and Ring), if RRO and RRX have been made complex comparable to the load as described in the previous sections, neither RTX1 nor RTX2 needs to be complex since both the transmit and receive signals which appear at TXO will be flat with respect to frequency.

RTX1 and RTX2 must have a tolerance equal to or better than the required system tolerance for the transmit gain.

8) Balance Network (RB) — Transhybrid Rejection

When a receive signal is applied to V_{RX} to produce a signal at Tip and Ring, the two-to-four wire arrangement of a hybrid (the MC33121) results in a reflected signal at TXO. Transhybrid rejection involves canceling that reflected signal before it appears at V_{TX}. The method used is to insert the RB resistor (or network) as shown in Figure 36. The current I_B, supplied from V_{RX}, cancels the current I_{TX1} supplied from TXO (Node A is a virtual ground). Good transhybrid cancellation requires that the currents be equal in magnitude **and** 180° out of phase at Node A.

Using the equations for transmit and receive gains, the current I_{TX1} is equal to:

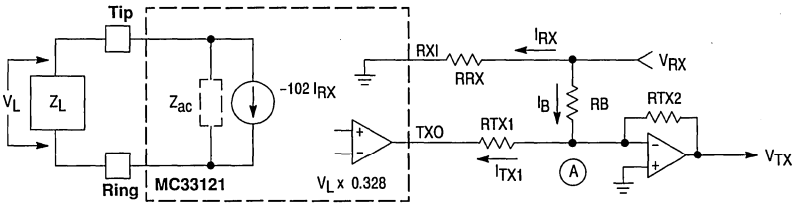
$$I_{TX1} = \frac{33.5 \bullet V_{RX} \bullet Z_{ac} \bullet Z_L \bullet 31\ k}{RRX \bullet [Z_{ac} + Z_L] \bullet RTX1 \bullet (RC + 31\ k)} \quad (16)$$

a) For the case where RRO and RRX are comparable in configuration to Z_L:

Since $I_B = V_{RX}/RB$, then RB can be determined from:

$$RB = \frac{RRX \bullet RTX1 \bullet (RC + 31\ k)}{33.5 \bullet [Z_{ac}//Z_L] \bullet 31\ k} \quad (17)$$

Figure 36. Balance Resistor



Equation 17 provides a value for an RB resistor which will provide the correct magnitude for I_B. The correct phase relationship is provided by the fact that the signal at TXO is out of phase with that at V_{RX}. The phase relationship will be 180° **only** if RRO and RRX are of a configuration identical to that of the load. This applies regardless of whether the load, Z_L, (and RRO and RRX) are purely resistive or of a complex nature. Equation 17 reduces to a non-complex resistance if RRX, Z_{ac}, and Z_L are all comparably complex.

For the case where $Z_{ac} = Z_L$, RRX = 51 • Z_{ac}, and RC = 1.0 k, Equation 17 reduces to:

$$RB = 3.15 \bullet RTX1 \qquad (18)$$

b) For the case where Z_{ac} and Z_L do not have the same frequency characteristics:

For the case where, for reasons of cost and/or simplicity, the load (R_L) is considered resistive (whereas in reality it is not a pure resistance) and therefore resistors, rather than networks, were selected for RRO and RRX, using a simple resistor for RB may not provide sufficient transhybrid rejection due to a phase angle difference between V_{RX} and TXO. The terminating impedance may therefore not necessarily be matched exactly to the line impedance, but the resulting circuit still provides sufficiently correct performance for receive gain, transmit gain, and return loss. The rejection can be improved in this case by replacing RB with the configuration shown in Figure 37. Even on a very short phone line there is a reactive component to the load due to the two compensation capacitors (C_C, Figure 4) at the transistor collectors. The two capacitors can be considered in series with each other, and across the load as shown in Figure 37.

To simplify the explanation, the current source and Z_{ac} of Figure 36 are replaced with the Thevenin voltage source and series Z_{ac}. Since Z_L and Z_{ac} are not matched, there will be a phase shift from V_{RX} to the signal across Tip and Ring. This phase shift is also present at TXO. The same phase shift is generated at node B in the RB network by making RB1 equal to Z_{ac}, and Z_L equal to the load. RB2 is then calculated from:

$$RB2 = \frac{RRX \bullet RTX1 \bullet (RC + 31\ k)}{33.5 \bullet Z_{ac} \bullet 31\ k} \qquad (19)$$

For example, for a system where the load is considered a 600 Ω resistor (RRO = 20.3 kΩ, RRX = 30.6 kΩ, RTX1 = 10 kΩ, and RC = 1.0 kΩ), RB1 would be a 600 Ω resistor, Z_L (in the RB network) would be a 600 Ω resistor in parallel with a 0.005 µF capacitor, and RB2 calculates to 15.715 kΩ.

The RB resistor, or network, must have a tolerance equal to or better than the required system tolerance for transhybrid rejection.

9) Logic Interface

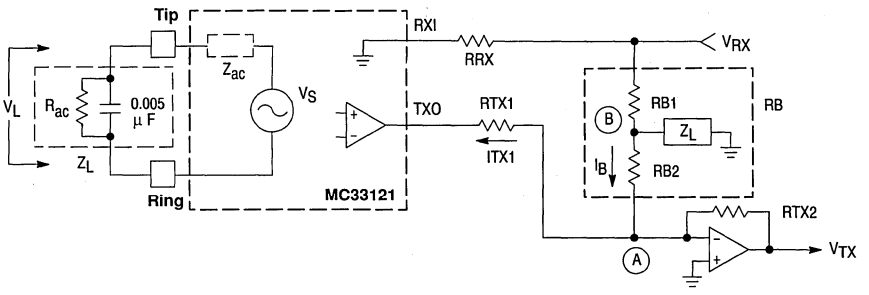
The logic circuit (output ST1, and the I/O labeled ST2/PDI) is depicted in Figure 30, and functions according to the Status Output Truth Table (Table 1).

a) Output Characteristics

ST1 is a traditional NPN pull-down with a 15 kΩ pull-up resistor. Figures 19 and 20 indicate its output characteristics.

ST2 is configured with the following items: a) a 1.0 mA current source for a pull-down which is active only when ST2 is internally set low; b) an 800 µA current source pull-up which is active only when ST2 is internally set high; c) a positive feedback aspect within this output circuit which

Figure 37. Balance Network



provides considerable hysteresis for stability reasons. Its output characteristics are shown in Figures 21 and 22. Due to this configuration, any external pull-up resistance which is applied to this pin must be greater than 15 kΩ, or the output may not reliably switch from high to low. Any external pull-down resistance does not affect this output's ability to switch from low-to-high, but does affect the maximum longitudinal currents which can be accepted by the circuit (see the section on Longitudinal Current Capability). The capacitor (C_T) is required to provide a time delay, for stability reasons, during transitions between off-hook and on-hook. This capacitor additionally affects maximum longitudinal currents, as well as stability during pulse dialing (explained below).

b) Hook Status

The MC33121 uses the sense currents at CP and CN to activate the hook status circuit. The sensing is configured such that the circuit monitors the impedance across Tip/Ring, which results in the hookswitch thresholds are minimally affected by the battery voltage. The off-hook to on-hook threshold is affected by the choice of RRF according to the graph of Figure 8, but is not affected by the value of RS. The on-hook to off-hook threshold is affected by the value of RS according to the graph of Figure 9, but is not affected by RRF. Varying the RC resistors does not affect the thresholds significantly.

When the telephone is on-hook (ST1 = High, ST2 = Low), the MC33121 is internally powered down, the external transistors are shut off, and power consumption is at a minimum. Upon closure of the phone's hookswitch, ST1 will switch low within 10 μs. ST2 will then change state slowly due to the external capacitor (C_T = 5.0 μF). There is a ≈8.0 ms delay for ST2 to reach the threshold necessary to activate the internal bias circuit, which in turn activates the external drive transistors to supply loop current. This delay is necessary to prevent instabilities during the transition to off-hook.

Upon opening the telephone's hookswitch, ST1 will switch high within ≈200 μs. ST2 then requires ≈60 ms to reach the threshold to switch off the internal bias circuit, which in turn shuts down the external drive transistors.

c) Pulse Dialing

During pulse dialing, ST1 will change state concurrent with the hookswitch. ST2 is kept from switching during pulse dialing by the external capacitor (C_T), which keeps the MC33121 in a powered up condition and stable. If the C_T capacitor is too small, the voltage at ST2 could drop to the PDI threshold (see section e below) during each pulse. This could cause the MC33121 to create additional noise on the line as it would cycle between a power-up and power-down condition with each dialing pulse.

d) Fault Detection

Faults are defined as excessive leakage from Tip to V_{EE} and/or ground, and from Ring to V_{EE} and/or ground. A single fault is any one of the above conditions, while a double fault is defined as excessive leakage from Tip to V_{EE} **and** from Ring to V_{CC}, as depicted in Figure 38. Refer to Figures 11-15 for the resistance, R_{LK}, which will cause the MC33121 to switch to a power-down condition. If the leakage resistance is less than that indicated in the graphs, the MC33121 will power-down itself and the two external transistors, thereby protecting them from overheating. Both status outputs (ST1 and ST2) will be at a logic low, indicating a fault condition. A fault condition is detected by monitoring an imbalance in the magnitudes of the currents at TSI and RSI, and/or a polarity reversal at Tip and Ring.

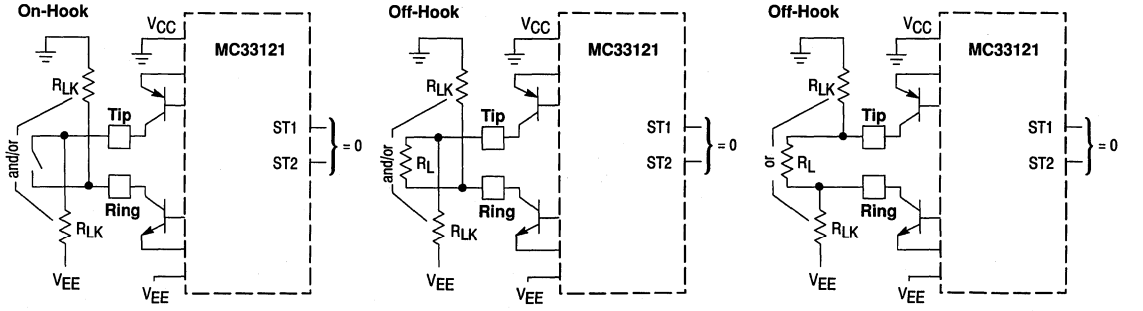
The MC33121 will detect the following conditions:

1) When on-hook (see Figure 11):
   a) <2.6 kΩ between Ring and V_{CC} (depending on R_S and V_{EE}), with no hysteresis at this threshold, or
   b) <3.7 kΩ between Tip and V_{EE} (depending on R_S and V_{EE}), with no hysteresis at this threshold, or
   c) Both a and b simultaneously.

Leakage from Tip to V_{CC} and/or Ring to V_{EE} are not detected as faults while the MC33121 is on-hook.

2) When off-hook (367 Ω between Tip and Ring):
   a) <400 Ω between Tip and V_{CC} (R_S = 6.2 kΩ), or
   b) <1800 Ω between Tip and V_{EE}, or
   c) <400 Ω between Ring and V_{EE} (R_S = 6.2 kΩ), or
   d) <1800 Ω between Ring and V_{CC}, or
   e) Both b and d simultaneously

Figure 38. Fault Detection



A simultaneous occurrence of conditions a) and c) is not detected as a fault. See Figures 12 to 15 for the threshold variation with R_L and V_{EE}. Resetting of the fault detection circuit requires that the leakage resistance be increased to a value between 10 kΩ and 20 kΩ, depending on V_{EE}, R_L, and R_S. Both ST1 and ST2 should be monitored for hookswitch status to preclude not detecting a fault condition.

Figure 15 indicates the variation in fault thresholds for Tip-to-V_{CC} and Ring-to-Battery faults, and is valid only for loop resistances of 200 Ω to 800 Ω. On loops larger than 800 Ω, the MC33121 does not reliably indicate the fault condition at ST1 and ST2, but may indicate on-hook status instead. This does not apply to Tip-to-Battery and Ring-to-V_{CC} faults which are correctly detected for lines beyond 800 Ω.

e) PDI Input

The ST2 output can also be used as an input (PDI Input) to power down the circuit, denying loop current to the subscriber (by shutting off the external pass transistors), regardless of the hookswitch position. Powering down is accomplished by pulling PDI to a logic low with an open collector output, or an NPN transistor as shown in Figure 30. The switching threshold is ≈1.5 V. The current out of PDI, when pulled low, is ≈800 μA. Releasing PDI allows the MC33121 to resume normal operation.

If the external telephone is off-hook while the MC33121 is powered down, sense currents at CP and TSI will result in some loop current flowing through the loop and back into CN and RSI. This current is generally on the order of 1.0 to 3.0 mA, determined primarily by the R_S resistors, loop resistance, and V_{EE}. ST1 will continue to indicate the telephone's actual hook status while PDI is held low. The on-to-off hook threshold is the same as that during normal operation, but the off-to-on hook threshold is >250 kΩ.

When powered down with the PDI pin, the receive gain (V_{RXI} to Tip/Ring) is muted by >90 dB, and the transmit gain (Tip/Ring to TXO) is muted by >30 dB.

Power Dissipation, Calculation and Considerations

a) Reliability

The maximum power dissipated by the MC33121 must be considered, and managed, so as to not exceed the junction temperature listed in the Maximum Ratings Table. Exceeding this temperature on a recurring basis will reduce long term reliability, and possibly degrade performance. The junction temperature also affects the statistical lifetime of the device, due to long term thermal effects within the package. Today's plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However, when the ultimate in system reliability is required, thermal managements must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperature is consistent with system reliability goals.

Based on the results of almost ten years of +125°C operating life testing, Table 2 has been derived indicating the relationship between junction temperature and time to 0.1% wire bond failure.

Table 2. Statistical Lifetime

Junction Temperature (°C)	Time (Hours)	TIme (Years)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

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The "Time" in Table 2 refers to the time the device is operating at that junction temperature. Since the MC33121 is at a low power condition (nominally 40 mW) when on-hook, the duty cycle must be considered. For example, if a statistical duty cycle of 20% off-hook time is used, operation at 130°C junction temperature (when off-hook) would result in a statistical lifetime of ≈10 years.

b) Power and Junction Temperature Calculation

The power within the IC is calculated by subtracting the power dissipated in the two-wire side (the transistors and the load) from the power delivered to the IC by the power supplies. Refer to Figure 4 and 27.

$$P_D = |V_{DD} \bullet I_{DD}| + |V_{EE} \bullet I_{EE}| - (I_L \bullet |V_{EP} - V_{EN}|) \quad (20)$$

The terms V_{EP} and V_{EN} are the DC voltages, with respect to ground, at the EP and EN pins. These voltages can be measured, or can be approximated by:

$$V_{EP} \approx -(30\ \Omega \bullet I_L)$$
$$V_{EN} \approx |V_{EE}| + 2.1\ V + (I_L \bullet 35\ \Omega)$$

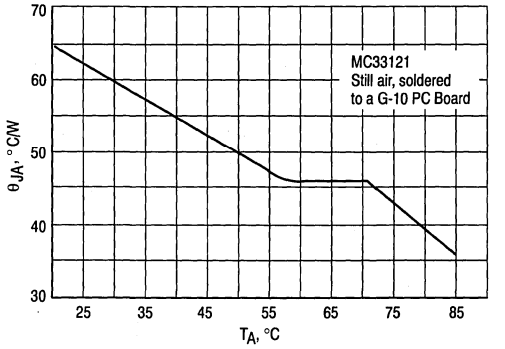
Refer to Figure 23. The junction temperature is then calculated from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (21)$$

where T_A is the ambient air temperature at the IC package, and θ_{JA} is the junction-to-ambient thermal resistance shown in Figure 39. The highest junction temperature will occur at maximum V_{EE} and V_{DD}, maximum loop current, and maximum ambient temperature.

If the above calculations indicate the junction temperature will exceed the maximum specified, then it is necessary to reduce the maximum loop current, ambient temperature, and/or V_{EE} supply voltage. Air flow should not be restricted near the IC by tall components or other objects since even a small amount of air flow can substantially reduce junction temperature. For example, typically an air flow of 300 LFPM (3.5 mph) can reduce the effective θ_{JA} by 14 to 20% from that which occurs in still air. Additionally, providing as much copper area as possible at the IC pins will assist in drawing away heat from within the IC package. For additional information on this subject, refer to the "Thermal Considerations" section of *Motorola MECL System Design Handbook*, and the "System Design Considerations" section of *Motorola MECL Device Data*.

Figure 39. Thermal Resistance (Junction-to-Ambient)



Selecting the Transistors

The specifications for the two loop current pass transistors involve their current gain, voltage rating, and power dissipation capabilities at the highest ambient temperatures. Power dissipation during both normal operation and faults must be considered when determining worst case situations. Generally, more power is dissipated during a fault condition than during normal operation.

The transistors' minimum beta is recommended to be 40 at the loop currents involved in the application. A lower beta could degrade gain and balance performance. Maximum beta should be less than 500 to prevent possible oscillations. Darlington type transistors should not be used. The voltage rating should be consistent with the maximum V_{EE}, expected transients, and the protection scheme used.

Referring to Figure 27, during normal operation the loop current and the voltage across the transistors are both at a maximum when the load impedance (R_L) is at a minimum. The loop current is determined by RRF and the graphs of Figures 5-7. The voltage across each transistor is determined from the following:

$$V_T = \frac{|V_{EE}| - 2.1 - [(65 + 2RP + R_L) \bullet I_L]}{2} \qquad (22)$$

The power in each transistor is then ($V_T \bullet I_L$). The voltage across the two transistors will always be nearly equal during normal operation, resulting in equal power dissipation. The graph of Figure 24 indicates the power dissipated in each transistor where RP = 100 Ω.

During a fault condition, depicted in Figure 38, if the leakage resistance from Tip to V_{EE} or from Ring to V_{CC} is less than that shown in Figures 12-14 (when off-hook), the MC33121 will power down the transistors to protect them from overheating. Should the leakage resistance be slightly higher than that shown in the graphs, however, and the fault detection has not been activated, the power in one transistor (in a single fault, both transistors in a double fault) will be higher than normal. The power will depend on V_{EE}, R_L, RP and the leakage resistance. Table 3 is a guide of the power in the transistor dissipating the higher power level.
The power (in watts) in the two right columns indicates the power dissipated by that transistor if it is carrying the maximum fault current. The system designer should attempt to predict possible fault conditions for the system, and then measure the conditions on the transistors during the worse case fault(s).

Table 3. Transistor Power During a Fault

V_{EE}	RL	P_{PNP}	P_{NPN}
–42	150	0.835	0.615
–24	150	0.257	0.176
–42	600	0.601	0.185
–24	600	0.109	0.057

For most applications involving a maximum loop current of 30-40 mA, and a maximum T_A of +85°C, and where faults may occur, the MJD243 and MJD253 DPAK transistors are recommended. When mounted as described in their data sheet, they will handle both the normal loop current as well as most fault conditions. If faults are not expected to occur in a particular application, then smaller package transistors, such as MPS6717 and MPS6729, may be used. Each application must be evaluated individually when selecting the transistors.

Other possible transistors which can be considered:

PNP	NPN
MJD253-1	MJD243-1
MJE253	MJE243
MJD32	MJD31
MJD42	MJD41
MJD350	MJD340
TIP30A,B,C	TIP29A,B,C

Longitudinal Current Capability

The maximum longitudinal current which can be handled without distortion is a function of loop current, battery feed resistance, the longitudinal impedance, and the components on ST2.

Since the pass transistors cannot pass current in the reverse direction, the DC loop current provides one upper boundary for the peak longitudinal current plus peak speech signal current. The battery feed resistance determines, in effect, the DC voltage across the transistors, which is a measure of the headroom available for the circuit to handle the peak longitudinal voltage plus peak speech signal voltage. The longitudinal impedance, determined by the R_S resistors (equation 4), determines the longitudinal current for a given longitudinal voltage.

While analysis of the above items may yield one value of maximum longitudinal current, a different limit (which may be higher or lower) is imposed by the capacitor C_T, and any pulldown resistance R_T, on Pin 12 (ST2). This is due to the fact that the sense currents at TSI and RSI will be alternately mismatched as Tip and Ring move up and down together in the presence of longitudinal signals. When the longitudinals are strong, the internal fault detect circuit is activated with each 1/2 cycle, which attempts to switch ST2 low (see the section on Fault Detection). The speed at which ST2 can switch low is a function of both the external capacitor, C_T and any pulldown resistance, R_T.

The graphs of Figures 25 and 26 indicate the maximum longitudinal current which can be handled (in Tip and in Ring) without distortion or causing ST2 to switch low.

PC Board Layout Considerations

PC board considerations include thermal, RFI/EMI, transient conditions, interconnection of the four wire side to the codec/filter, and others. Wirewrapped boards should be

avoided — breadboarding should be done on a (at least) reasonably neat PC board.

a) Thermal

Power dissipated by the MC33121 and the two transistors must be removed to prevent excessively high junction temperatures. The equations for calculating junction temperatures are mentioned elsewhere in this data sheet. Heat is removed by both air flow and copper foil on the PC board. Since even a small amount of air flow substantially reduces junction temperatures compared to still air, tall components or other objects should not be placed such that they block air flow across the heat generating devices. Increasing, wherever possible, the area of the copper foil at the IC pins will provide additional heat removal capability. A ground plane can generally help here, while at the same time helping to reduces RFI problems.

b) RFI/EMI

While the MC33121 is intended for use at audio frequencies, the internal amplifiers have bandwidths in excess of 1.0 MHz, and can therefore respond to externally induced RFI and EMI. Interference signals can come in on the phone line, or be radiated on to the PC board from nearby radio stations or from high frequency circuitry (digital & microprocessor circuitry) in the vicinity of the line card.

Usually RFI entering from the phone line at Tip and Ring can be removed by the compensation capacitors (C_C) provided they are connected to a good quality RF ground (generally the same ground which connects to V_{CC} on the MC33121). The ground track should be as wide and as direct as possible to minimize lead inductance. Generally better results can be obtained if an RF bleedoff to earth (or chassis) ground can be provided where the twisted pair phone line comes into the system.

To minimize problems due to noise radiating directly onto the PC board from nearby high frequency circuitry, all components associated with the MC33121 should be physically as close as possible to the IC. The most sensitive pins in this respect are the CP, CN, RSI, TSI, VAG and RXI pins. Keeping the tracks short minimizes their "antenna" effect.

c) Transient Conditions

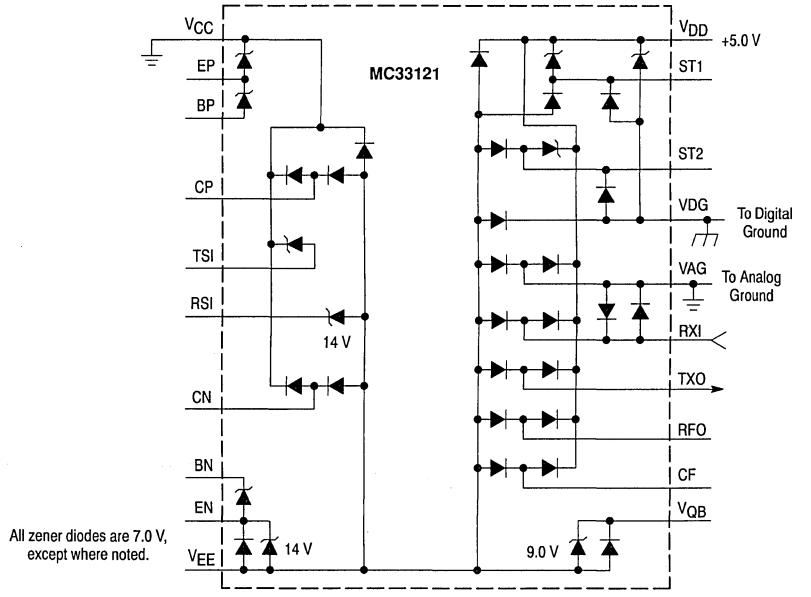
When transient voltages come in to Tip and Ring, the transient currents, which can be several amperes, must be carried by the ground line (V_{CC}) and/or the V_{EE} line. These tracks, along with the protection and clamping devices, must be designed for these currents at the frequencies involved. If the tracks are narrow, not only may they be destroyed by the high currents, but their inductance can allow the voltage at the IC, and other nearby components, to rise to damaging levels.

The protection circuits shown in Figure 4, and in other figures in this data sheet, are such that the bulk of the transient energy is dissipated by external components (the protection resistors and the clamp diodes). The MC33121 has internal diodes to limit voltage excursions on the pins, and to pass a small amount of the transient current — typically less than 1.0 A peak. The arrangement of the diodes is shown in Figure 40.

d) Interconnection of the four-wire side

The connections on the four-wire side to the codec and other digital circuitry involves keeping digital noise out of the speech paths, and also ensuring that potentially destructive transients on Tip and Ring do not get through to the +5.0 V system.

Figure 40. Protection Diodes



Basically, digital connections to ST1 and ST2 should be referenced to the V_{DD} and V_{DG} pins, while the transmit and receive analog signals should be referenced to the analog ground (V_{AG}). V_{CC} should be connected to a clean battery ground, and generally should not be connected directly to V_{DG} and/or V_{AG} (on the line card) when strong transients are anticipated. Even with a good layout, V_{CC} can move several volts when a transient hits, possibly damaging components on the +5.0 V line if their grounds have a direct connection at the line card. The MC33121 is designed to allow V_{CC} to move as much as ±30 V with respect to V_{DG} and V_{AG} on a transient basis only. V_{CC} and the other grounds should preferably be connected together at the power supply rather than at the IC. Internally, the MC33121 has clamp diodes on the 4-wire side pins as indicated in Figure 40.

If the codec has a single ground pin, as in Figure 41, it will be the reference for both the digital and analog signals, and must be connected to both V_{AG} and V_{DG} on the MC33121. If the codec has separate digital and analog grounds, as in Figure 42 (the MC145503 internally generates the analog ground), then each ground should be connected to the appropriate ground on the MC33121.

e) Other

A 0.1 µF capacitor should be provided across V_{CC} to V_{EE} on the MC33121 to help keep idle channel noise to a minimum.

The C_{QB} capacitor (on the V_{QB} pin) forms a pole with an internal 7.5 kΩ resistor to filter noise from the V_{EE} pin, providing an internal quiet battery supply for the speech amplifiers. Power supply rejection will depend on the value and quality of this capacitor at the frequencies of concern. Tantalum capacitors generally have better high frequency characteristics then electrolytics. See Figure 17 and 18 for ripple rejection characteristics (the four-wire data was measured at pin 11 (TXO)). Figure 16 indicates ripple rejection from the +5.0 V supply (V_{DD}).

In general, pc board tracks carrying analog signals (on the four-wire side and Tip/Ring) should not be routed through the digital section where they could pick up digital noise. Any tracks longer than a few inches should be considered an

Figure 41. Connection to a CODEC With a Single Ground

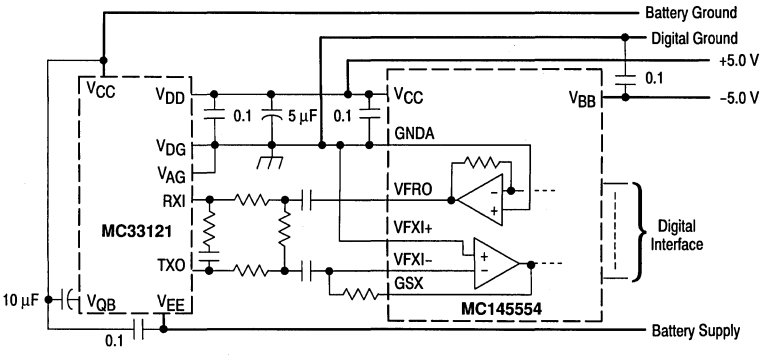
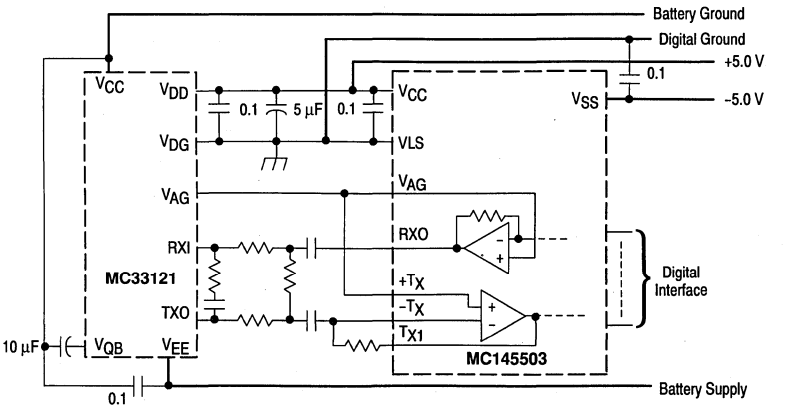


Figure 42. Connection to a CODEC With Separate Grounds



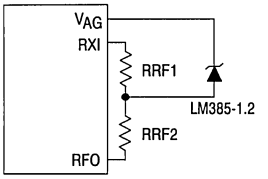
antenna and should be checked for potential noise or RFI pickup which could affect the circuit operation.

Alternate Circuit Configurations

a) Loop Current Limit

Replacing the RRF resistor with the circuit in Figure 43 will change the DC loop current characteristics in two ways from the graphs of Figures 5-7; a) the maximum loop current on a short line can be reduced while increasing the current on a long line, and b) the temperature dependence of the maximum current is reduced to the TC of the external reference diode.

Figure 43. Alternate Current Limit Circuit



The LM385-1.2 is a precision temperature stable zener diode. As the load impedance at Tip and Ring is reduced, the voltage at RFO goes increasingly negative. When the zener diode is turned on, the current into RXI is then clamped at a value determined by RRF1 and the zener diode. To calculate the two resistors, use the following procedure:

RRF1 must be >0.7 • (RRF1 + RRF2);

Determine RRF1 to set the current limit on a short line by using the following equation:

$$RRF1 = \frac{102 \bullet 1.23\ V}{I_{L(max)} - 3.0\ mA} \qquad (23)$$

Then using Equation 1 calculate RRF for the long line current. RRF2 is then determined by;

$$RRF2 = RRF - RRF1 \qquad (24)$$

Figure 44 illustrates one example using the above circuit. Comparing this graph to the 5100 Ω curve of Figure 7 shows a substantial decrease in the current limit (at R_L = 0), resulting in reduced power consumption and dissipation. Use of this circuit does not affect the hookswitch or fault thresholds.

b) Protection Scheme

The protection circuit shown in Figure 45 has the advantage of drawing ≈90% of the transient current from ground (V_{CC}) on a negative transient, rather than from the V_{EE} line as the circuit of Figure 4 does. The majority of the transient current flows through the RP resistors and the Mosorbs while a small amount (≈10%) flows through the sense resistors and the CP, CN, RSI pins. On a positive transient, all the current is directed to ground. The diode in the NPN's collector prevents reverse current through the base-collector junction of the transistor during a negative transient.

Figure 44. Loop Current versus Loop Resistance Alternate Loop Current Limit Configuration

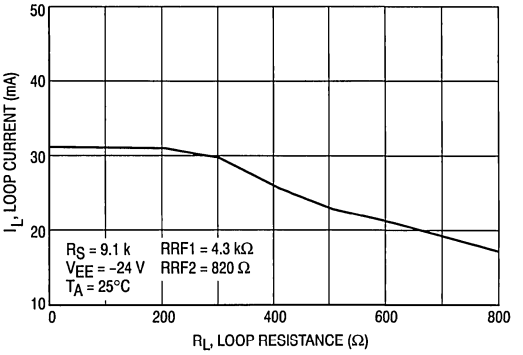
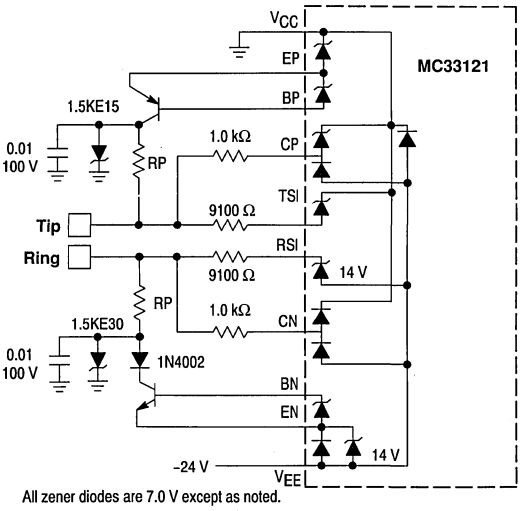


Figure 45. Alternate Protection Scheme



All zener diodes are 7.0 V except as noted.

CIRCUIT PERFORMANCE

The following three circuits are presented as typical application examples, and the accompanying graphs indicate their measured performance. The first circuit (Figure 46) has a 600 Ω pure resistance as the AC load. The second circuit (Figures 47) has as an AC load a 900 Ω resistor in series with a 2.16 μF capacitor. The third circuit (Figure 48) has as an AC load, a complex network composed of an 820 Ω resistor in parallel with 0.115 μF, and those in series with a 220 Ω resistor. In the graphs of Figures 49-51, R_L = Return Loss, THR = Transhybrid Rejection, GTX = Transmit Gain, GRX = Receive Gain.

Figure 46. 600 Ω System

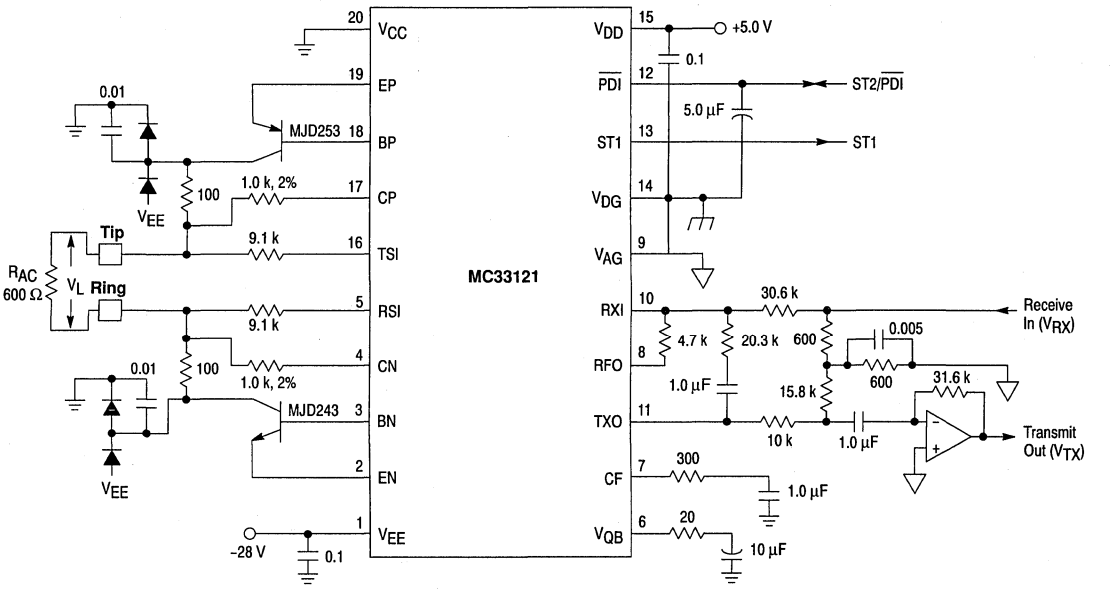


Figure 47. 900 Ω and 2.16 μF System

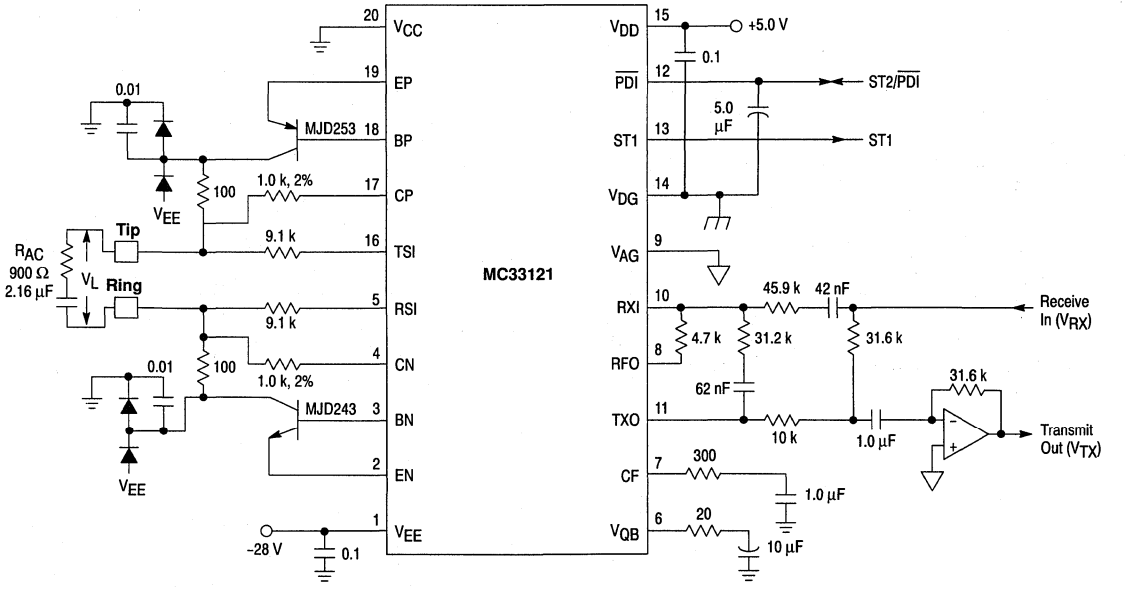


Figure 48. 220 Ω and 820 Ω//0.115 μF System

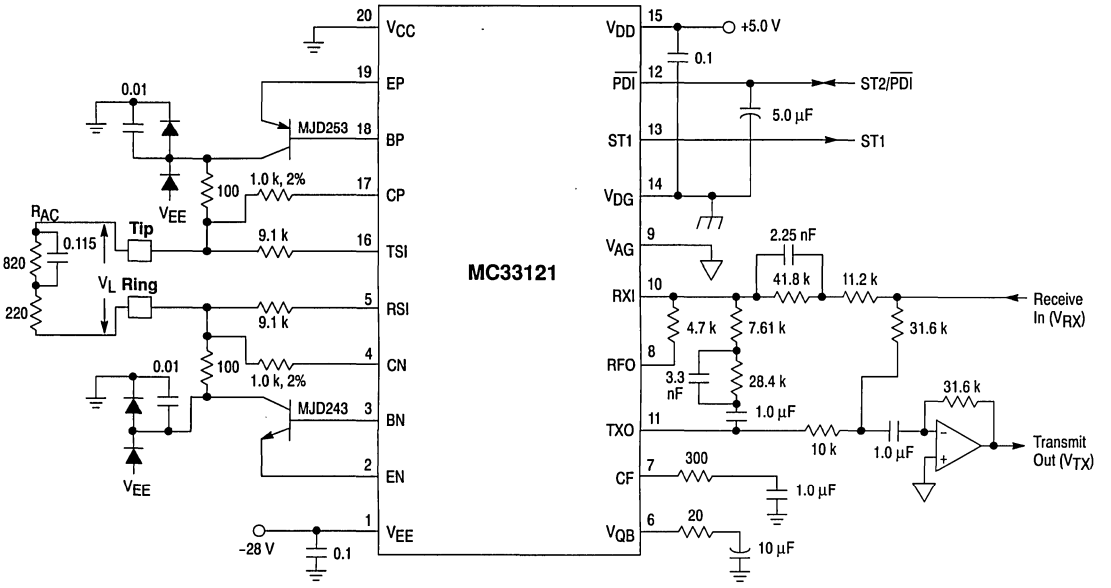


Figure 49. Circuit Performance, 600 Ω System

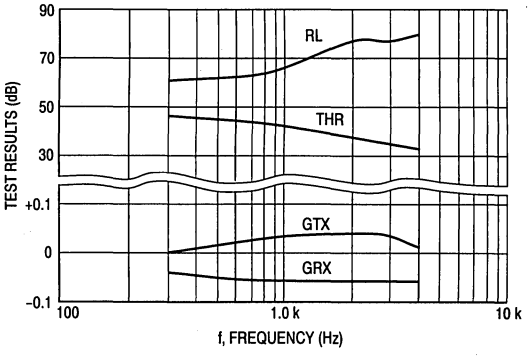


Figure 50. Circuit Performance 900 Ω and 2.16 μF System

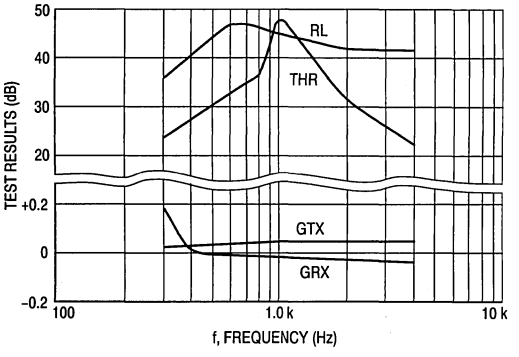


Figure 51. Circuit Performance 820 Ω//0.115 μF and 220 Ω System

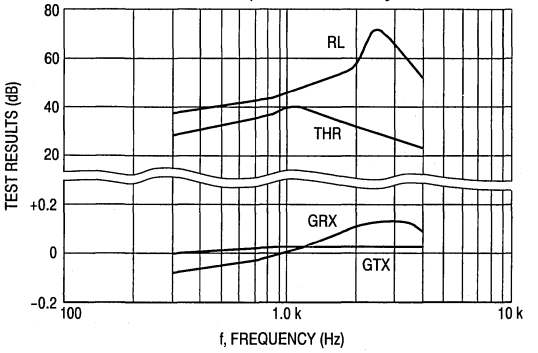
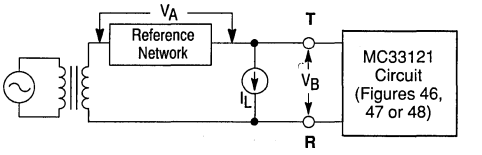


Figure 52. Return Loss Test Circuit for Figures 46 to 51



Reference Network = R_{AC} of Figures 46 to 48.

Return Loss = $20 \log \left| \frac{V_A + V_B}{V_A - V_B} \right|$

GLOSSARY

ATTENUATION — A decrease in magnitude of a communication signal, usually expressed in dB.

BALANCE NETWORK — That part of the SLIC circuit which provides transhybrid rejection.

BANDWIDTH — The range of information carrying frequencies of a communication system.

BATTERY — The voltage which provides the loop current, and in some cases powers the SLIC circuit. The name derives from the fact that COs have always used batteries, in conjunction with AC power, to provide this voltage.

BATTERY FEED RESISTANCE — The equivalent Thevenin DC resistance of the SLIC circuit for supplying loop current. Traditionally it is 400 Ω.

C-MESSAGE FILTER — A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

CENTRAL OFFICE — Abbreviated CO, it is a main telephone office, usually within a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A typical CO can handle up to 10,000 subscriber numbers.

CODEC — Coder/Decoder — Interfacing between the SLIC and the digital switch, it converts the SLIC's transmit signal to digital, and converts the digital receive signal to analog.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:
10 • log (P_1 / P_2) for power measurements, and
20 • log (V_1 / V_2) for voltage measurements.

dBm — An indication of signal power. 1.0 mW across 600 Ω, or 0.775 Vrms, is defined as 0 dBm. Any other voltage level is converted to dBm by:
dBm = 20 • log (Vrms/0.775), or
dBm = [20 • log (Vrms)] + 2.22.

dBmp — Indicates dBm measurement using a psophometric weighting filter.

dBrn — Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = –90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

DTMF — Dual Tone Multifrequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a keypad.

FAULT — An incorrect condition where Tip is accidentally connected to the battery voltage, or Ring is connected to ground, or both. The most common fault is Ring to ground.

FOUR WIRE CIRCUIT — The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the transmit path, and one pair is for the receive path.

FULL DUPLEX — A transmission system which permits communication in both directions simultaneously. The standard handset telephone system is full duplex.

GAIN — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

HALF DUPLEX — A transmission system which permits communication in one direction at a time. CB radios, with "push-to-talk" switches, and voice activated speakerphones, are half duplex.

HOOKSWITCH — A switch, within the telephone, which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

HYBRID — Another name for a two-to-four wire converter.

IDLE CHANNEL NOISE — Residual background noise when transmit and receive signals are absent.

LINE CARD — The PC board and circuitry in the CO or PBX which connects to the subscriber's phone line. A line card may hold circuitry for one subscriber, or a number of subscribers.

LONGITUDINAL BALANCE — The ability of the SLIC to reject longitudinal signals on Tip and Ring.

LONGITUDINAL SIGNALS — Common mode signals.

LOOP — The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally, it is a floating system not referred to ground, or AC power.

LOOP CURRENT — The DC current which flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20 to 120 mA.

OFF-HOOK — The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the DC current as an indication that the phone is busy.

ON-HOOK — The condition when the telephone is disconnected from the phone system, and no DC loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange. In effect, a miniature central office, it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

PROTECTION, PRIMARY — Usually consisting of carbon blocks or gas discharge tubes, it absorbs the bulk of a lightning induced transient by clamping the voltages to less than ±1500 V.

PROTECTION, SECONDARY — Usually located on the line card, it protects the SLIC and associated circuits from transient surges. Typically, it must be capable of clamping a ±1.5 kV surge of 1.0 ms duration.

PULSE DIALING — A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 per second. The old rotary phones, and many new pushbutton phones, use pulse dialing.

RECEIVE PATH — Within the CO or PBX it is the speech path from the internal switching system towards the phone line (Tip & Ring).

REN — Ringer Equivalence Number. An indication of the impedance or loading factor of a telephone bell or ringer circuit. An REN of 1.0 equals ≈8.0 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

RETURN LOSS — Expressed in dB, it is a measure of how well the SLIC's AC impedance matches the line's AC characteristic impedance. With a perfect match, there is no reflected signal, and therefore infinite return loss. It is calculated from:

$$RL = 20 \bullet \log \frac{(Z_{Line} + Z_{CKT})}{(Z_{Line} - Z_{CKT})}$$

RING — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

SLIC — Subscriber Line Interface Circuit. It is the circuitry within the CO or PBX which connects to the user's phone line.

SUBSCRIBER — The customer at the telephone end of the line.

SUBSCRIBER LINE — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

TIP — One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

TRANSHYBRID REJECTION — The rejection (in dB) of the reflected signal in the transmit path resulting from a receive signal applied to the SLIC.

TRANSMIT PATH — Within the CO or PBX it is the speech path from the phone line (Tip & Ring) towards the internal switching system.

TWO WIRE CIRCUIT — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

TWO-TO-FOUR WIRE CONVERTER — A circuit which has four wires (on one side) — two (signal & ground) for the outgoing signal, and two for the incoming signal. The outgoing signal is sent out differentially on the two wire side (the other side), and incoming differential signals received on the two wire side are directed to the four wire side. Additional circuit within cancels the reflected outgoing signal to keep it separate from the incoming signal.

VOICEBAND — That portion of the audio frequency range used for transmission across the telephone system. Typically, it is 300 to 3400 Hz.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33178
MC33179

HIGH OUTPUT CURRENT LOW POWER, LOW NOISE OPERATIONAL AMPLIFIERS

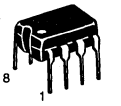
High Output Current Low Power, Low Noise Bipolar Operational Amplifiers

The MC33178/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This device family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input offset voltage, noise and distortion. In addition, the amplifier provides high output current drive capability while consuming only 420 μA of drain current per amplifier. The NPN output stage used, exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop high frequency output impedance, symmetrical source and sink AC frequency performance.

The MC33178/9 family offers both dual and quad amplifier versions, tested over the vehicular temperature range. These devices are available in DIP and SOIC packages.

- 600 Ω Output Drive Capability
- Large Output Voltage Swing
- Low Offset Voltage: 0.15 mV (Mean)
- Low T.C. of Input Offset Voltage: 2.0 μV/°C
- Low Total Harmonic Distortion: 0.0024% (@ 1.0 kHz w/600 Ω Load)
- High Gain Bandwidth: 5.0 MHz
- High Slew Rate: 2.0 V/μs
- Dual Supply Operation: ±2.0 V to ±18 V
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Performance

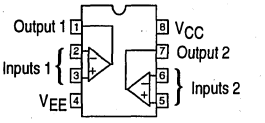
DUAL



P SUFFIX
PLASTIC PACKAGE
CASE 626

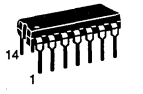
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



(Top View)

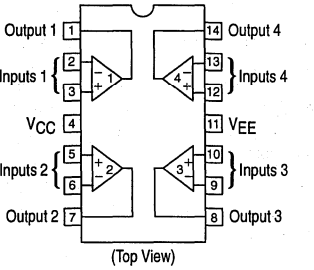
QUAD



P SUFFIX
PLASTIC PACKAGE
CASE 646

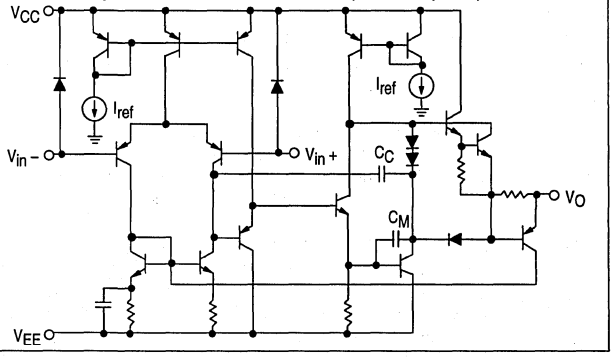
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

Equivalent Circuit Schematic (Each Amplifier)



ORDERING INFORMATION

Op Amp Function	Fully Compensated	Temperature Range	Package
Dual	MC33178D MC33178P	−40° to +85°C	SO-8 Plastic DIP
Quad	MC33179D MC33179P		SO-14 Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V) (V_{CC} = +2.5 V, V_{EE} = –2.5 V to V_{CC} = +15 V, V_{EE} = –15 V) T_A = +25°C T_A = –40° to +85°C	2	$\lvert V_{IO}\rvert$	 — —	 0.15 —	 3.0 4.0	mV
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V) T_A = –40° to +85°C	2	$\Delta V_{IO}/\Delta T$	 —	 2.0	 —	µV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	3, 4	I_{IB}	 — —	 100 —	 500 600	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C		$\lvert I_{IO}\rvert$	 — —	 5.0 —	 50 60	nA
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	5	V_{ICR}	–13 —	–14 +14	— +13	V
Large Signal Voltage Gain (V_O = –10 V to +10 V, R_L = 600 Ω) T_A = +25°C T_A = –40° to +85°C	6, 7	A_{VOL}	 50 k 25 k	 200 k —	 — —	V/V
Output Voltage Swing (V_{ID} = ±1.0 V) (V_{CC} = +15 V, V_{EE} = –15 V) R_L = 300 Ω R_L = 300 Ω R_L = 600 Ω R_L = 600 Ω R_L = 2.0 kΩ R_L = 2.0 kΩ (V_{CC} = +2.5 V, V_{EE} = –2.5 V) R_L = 600 Ω R_L = 600 Ω	8, 9, 10	 V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-}	 — — +12 — +13 — 1.1 —	 +12 –12 +13.6 –13 +14 –13.8 1.6 –1.6	 — — — –12 — –13 — –1.1	V
Common Mode Rejection (V_{in} = ±13 V)	11	CMR	80	110	—	dB
Power Supply Rejection V_{CC}/V_{EE} = +15 V/ –15 V, +5.0 V/ –15 V, +15 V/ –5.0 V	12	PSR	80	110	—	dB
Output Short Circuit Current (V_{ID} = ±1.0 V, Output to Ground) Source (V_{CC} = 2.5 V to 15 V) Sink (V_{EE} = –2.5 V to –15 V)	13, 14	I_{SC}	 +50 –50	 +80 –100	 — —	mA
Power Supply Current (V_O = 0 V) (V_{CC} = 2.5 V, V_{EE} = –2.5 V to V_{CC} = +15 V, V_{EE} = –15 V) MC33178 (Dual) T_A = +25°C T_A = –40° to +85°C MC33179 (Quad) T_A = +25°C T_A = –40° to +85°C	15	I_D	 — — — —	 — — 1.7 —	 1.4 1.6 2.4 2.6	mA

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See power dissipation performance characteristic, Figure 1.)

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = −10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0 V)	16, 31	SR	1.2	2.0	—	V/μs
Gain Bandwidth Product (f = 100 kHz)	17	GBW	2.5	5.0	—	MHz
AC Voltage Gain (R_L = 600 Ω, V_O = 0 V, f = 20 kHz)	18, 19	A_{VO}	—	50	—	dB
Unity Gain Frequency (Open-Loop) (R_L = 600 Ω, C_L = 0 pF)		f_U	—	3.0	—	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	20, 22, 23	A_m	—	15	—	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	21, 22, 23	ϕ_m	—	60	—	Degrees
Channel Separation (f = 100 Hz to 20 kHz)	24	CS	—	−120	—	dB
Power Bandwidth (V_O = 20 V_{p-p}, R_L = 600 Ω, THD ≤ 1.0%)		BW_p	—	32	—	kHz
Distortion (R_L = 600 Ω,, V_O = 2.0 V_{p-p}, A_V = +1.0 V) (f = 1.0 kHz) (f = 10 kHz) (f = 20 kHz)	25	THD	 — — —	 0.0024 0.014 0.024	 — — —	%
Open-Loop Output Impedance (V_O = 0 V, f = 3.0 MHz, A_V = 10 V)	26	$\lvert Z_O \rvert$	—	150	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{IN}	—	200	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{IN}	—	10	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω,) f = 10 Hz f = 1.0 kHz	27	e_n	 — —	 8.0 7.5	 — —	nV/√Hz
Equivalent Input Noise Current f = 10 Hz f = 1.0 kHz	28	i_n	 — —	 0.33 0.15	 — —	pA/√Hz

Figure 1. Maximum Power Dissipation versus Temperature

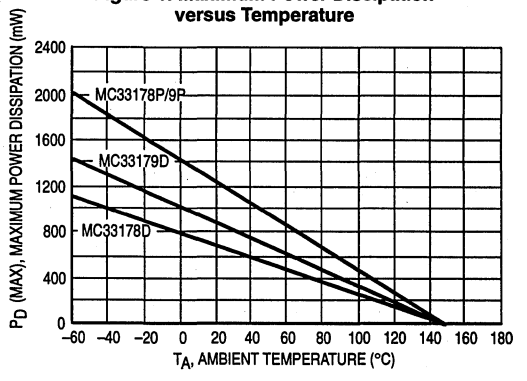


Figure 2. Input Offset Voltage versus Temperature for 3 Typical Units

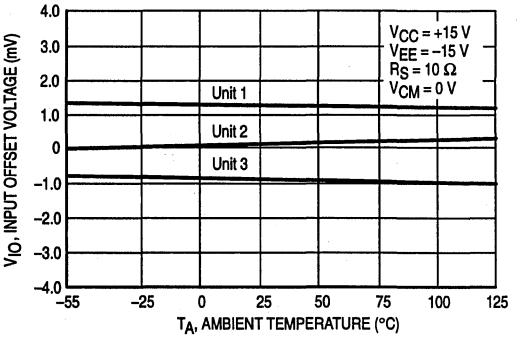


Figure 3. Input Bias Current versus Common Mode Voltage

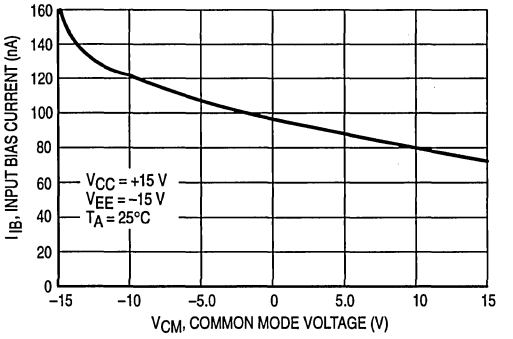


Figure 4. Input Bias Current versus Temperature

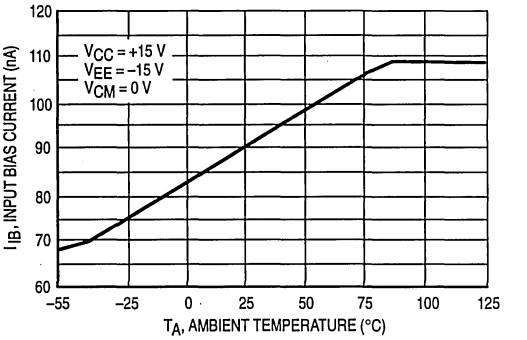


Figure 5. Input Common Mode Voltage Range versus Temperature

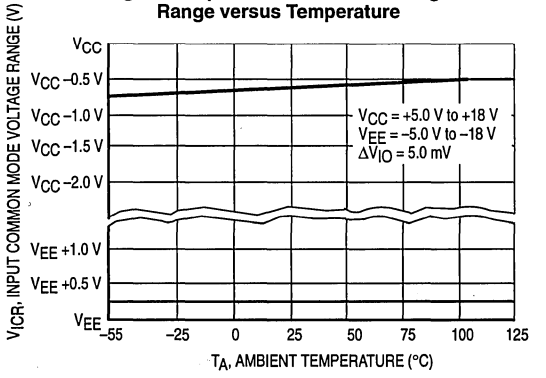


Figure 6. Open-Loop Voltage Gain versus Temperature

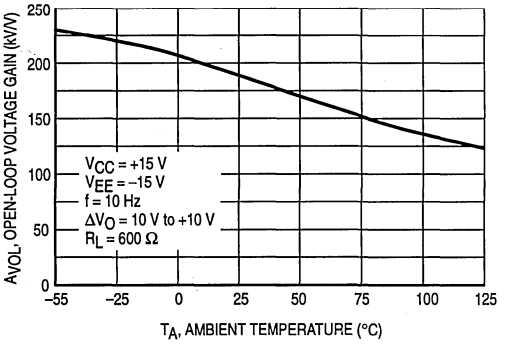


Figure 7. Voltage Gain and Phase versus Frequency

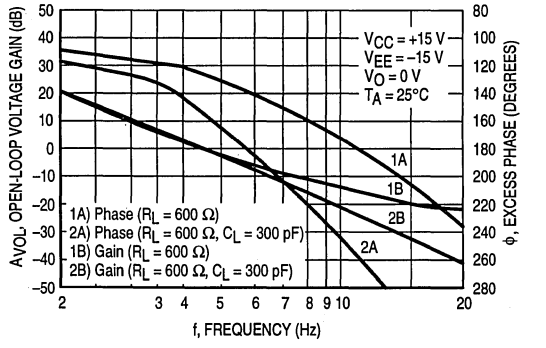


Figure 8. Output Voltage Swing versus Supply Voltage

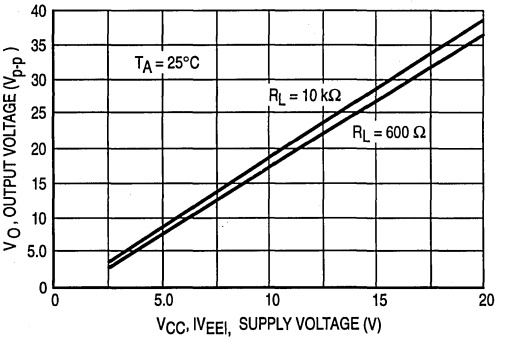


Figure 9. Output Saturation Voltage versus Load Current

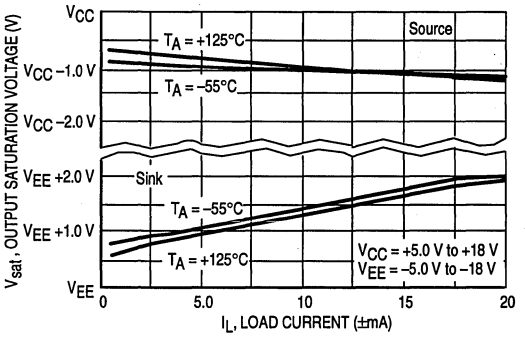


Figure 10. Output Voltage versus Frequency

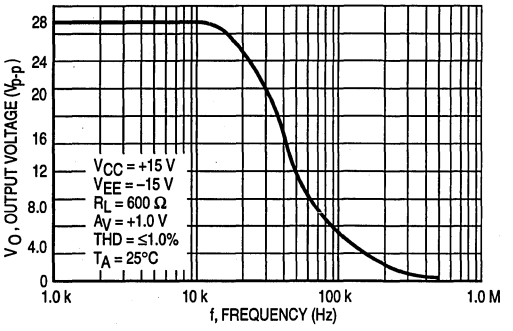


Figure 11. Common Mode Rejection versus Frequency Over Temperature

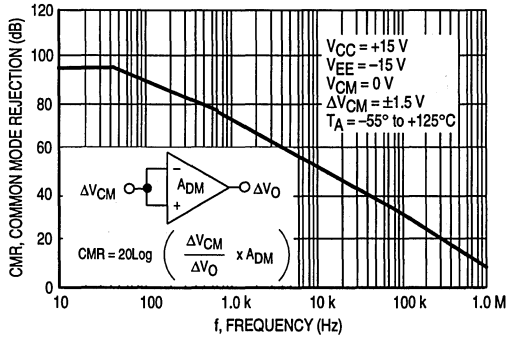


Figure 12. Power Supply Rejection versus Frequency Over Temperature

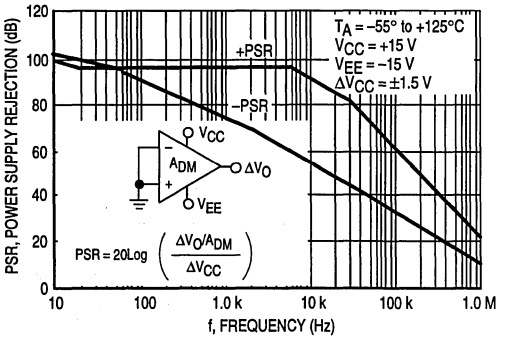


Figure 13. Output Short Circuit Current versus Output Voltage

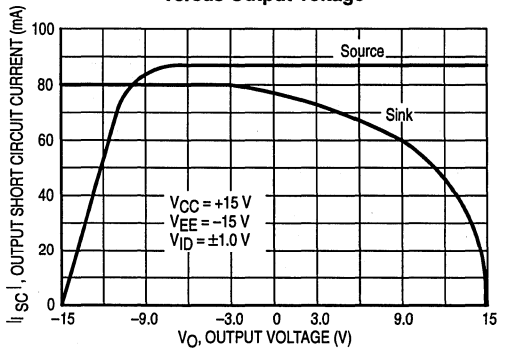


Figure 14. Output Short Circuit Current versus Temperature

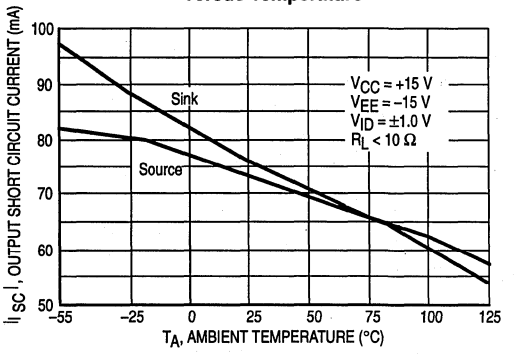


Figure 15. Supply Current versus Supply Voltage with No Load

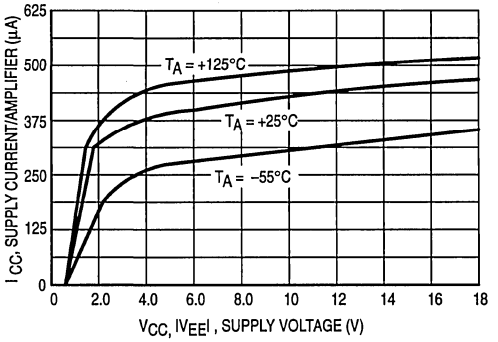


Figure 16. Normalized Slew Rate versus Temperature

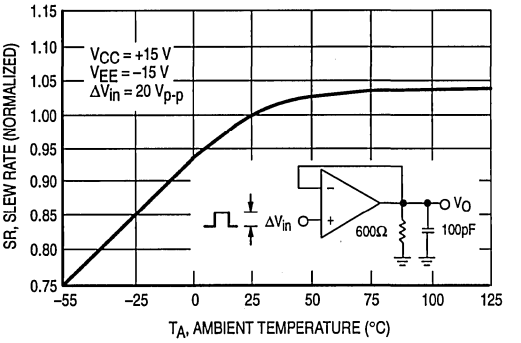


Figure 17. Gain Bandwidth Product versus Temperature

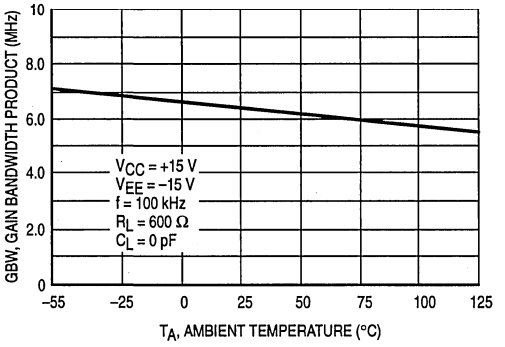


Figure 18. Voltage Gain and Phase versus Frequency

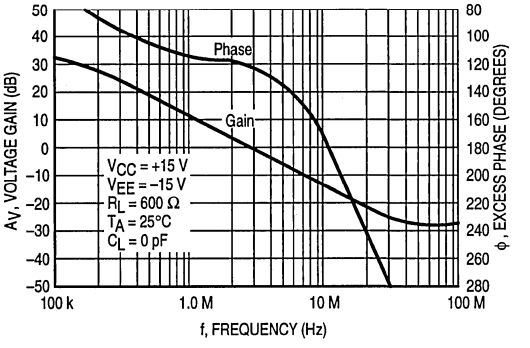


Figure 19. Voltage Gain and Phase versus Frequency

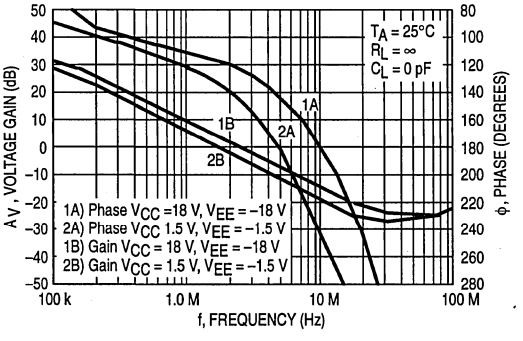


Figure 20. Open-Loop Gain Margin versus Temperature

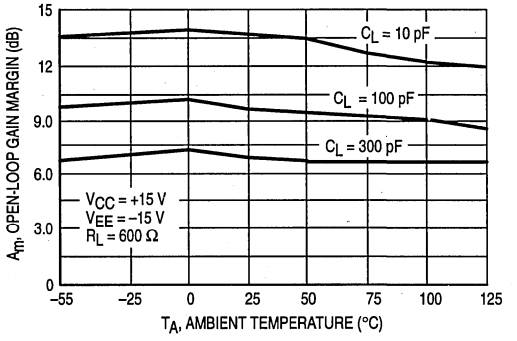


Figure 21. Phase Margin versus Temperature

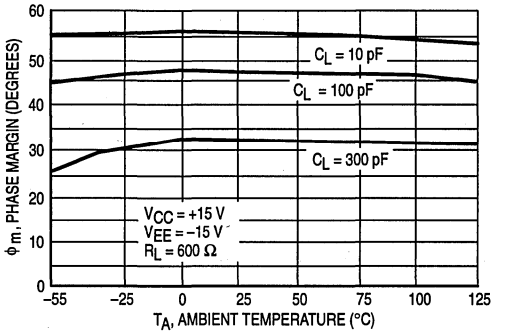


Figure 22. Phase Margin and Gain Margin versus Differential Source Resistance

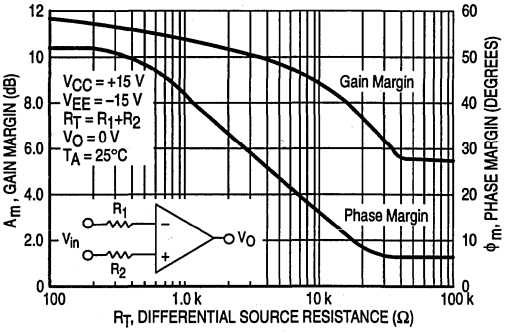


Figure 23. Open-Loop Gain Margin and Phase Margin versus Output Load Capacitance

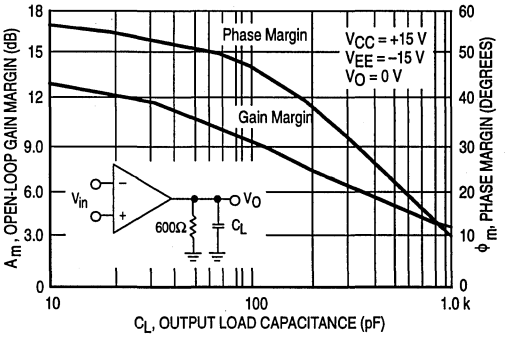


Figure 24. Channel Separation versus Frequency

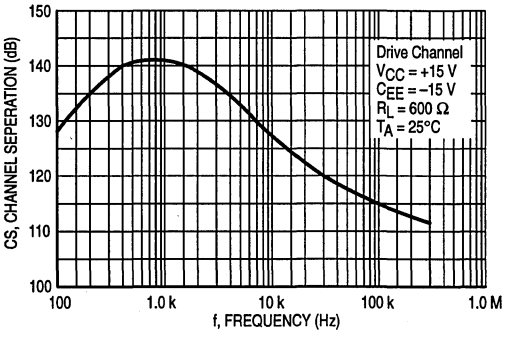


Figure 25. Total Harmonic Distortion versus Frequency

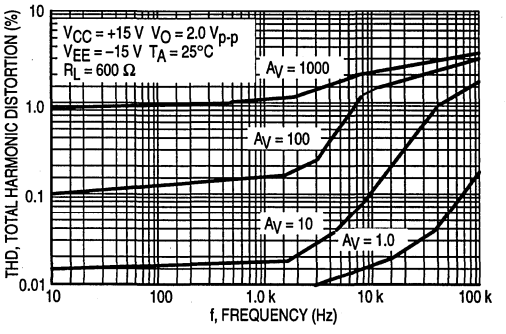


Figure 26. Output Impedance versus Frequency

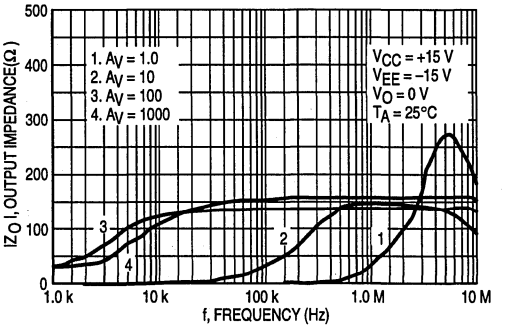


Figure 27. Input Referred Noise Voltage versus Frequency

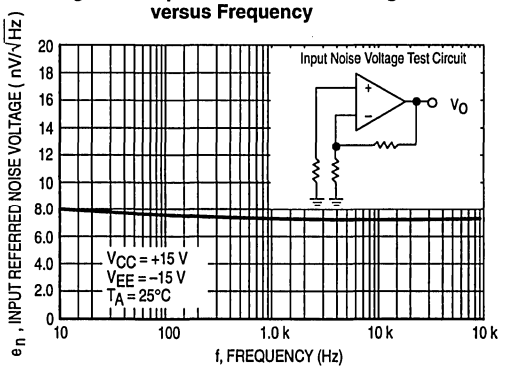


Figure 28. Input Referred Noise Current versus Frequency

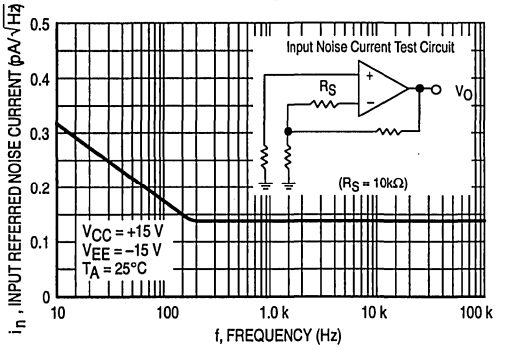


Figure 29. Percent Overshoot versus Load Capacitance

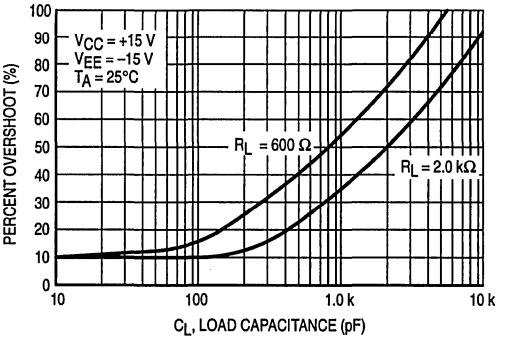


Figure 30. Noninverting Amplifier Slew Rate

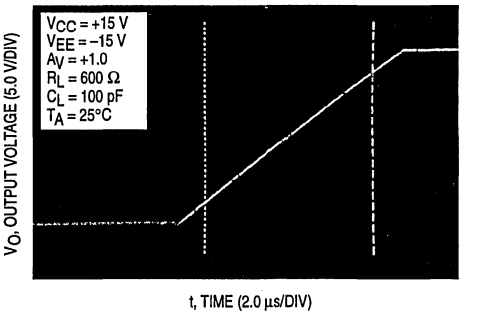


Figure 31. Small Signal Transient Response

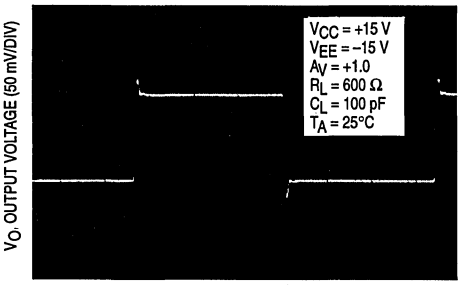


Figure 32. Large Signal Transient Response

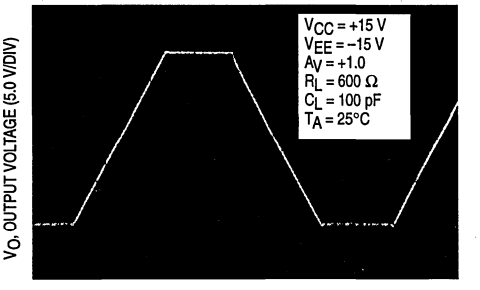
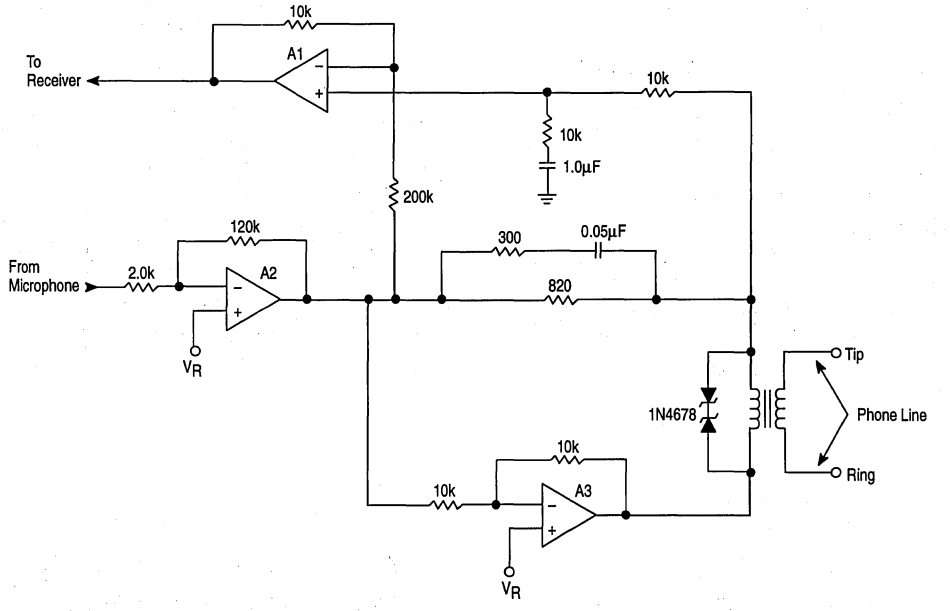


Figure 33. Telephone Line Interface Circuit



APPLICATION INFORMATION

This unique device uses a boosted output stage to combine a high output current with a drain current lower than similar bipolar input op amps. Its 60° phase margin and 15 dB gain margin ensure stability with up to 1000 pF of load capacitance (see Figure 23). The ability to drive a minimum 600 Ω load makes it particularly suitable for telecom applications. Note that in the sample circuit in Figure 33 both A2 and A3 are driving equivalent loads of approximately 600 Ω .

The low input offset voltage and moderately high slew rate and gain bandwidth product make it attractive for a variety of other applications. For example, although it is not single supply (the common mode input range does not include ground), it is specified at +5.0 V with a typical common mode rejection, of 110 dB. This makes it an excellent choice for use with digital circuits. The high common mode rejection, which is stable over temperature, coupled with a low noise figure and low distortion is an ideal op amp for audio circuits.

The output stage of the op amp is current limited and therefore has a certain amount of protection in the event of a short circuit. However, because of its high current output, it is especially important not to allow the device to exceed the maximum junction temperature, particularly with the MC33179 (quad op amp). Shorting more than one amplifier could easily exceed the junction temperature to the extent of causing permanent damage.

Stability

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole frequency for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supplying decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

Additional stability problems can be caused by high load capacitances and/or a high source resistance. Simple compensation schemes can be used to alleviate these effects.

If a high source of resistance is used (R1 > 1.0 kΩ), a compensation capacitor equal to or greater than the input capacitance of the op amp (10 pF) placed across the feedback resistor (see Figure 34) can be used to neutralize that pole and prevent outer loop oscillation. Since the closed loop transient response will be a function of that capacitance it is important to choose the optimum value for that capacitor. This can be determined by the following formula:

(1) $C_C = (1 + [R1/R2])^2 \bullet C_L (Z_O/R_2)$

where: Z_O is the output impedance of the op amp.

For moderately high capacitive loads (500 pF < C_L < 1500 pF) the addition of a compensation resistor on the order of 20 Ω between the output and the feedback loop will help to decrease miller loop oscillation (see Figure 35). For high capacitive loads (C_L > 1500 pF) a combined compensation scheme should be used (see Figure 36). Both the compensation resistor and the compensation capacitor affect the transient response and can be calculated for optimum performance. The value of C_C can be calculated using formula (1). The formula to calculate R_C is as follows:

(2) $R_C = Z_O \bullet R1/R2$

Figure 34. Compensation for High Source Impedance

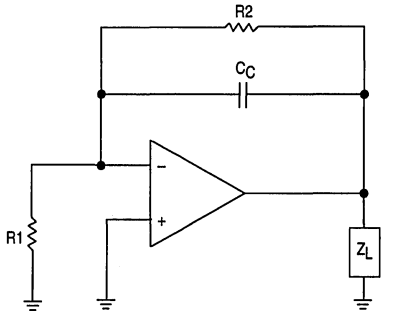


Figure 35. Compensation Circuit for Moderate Capacitve Loads

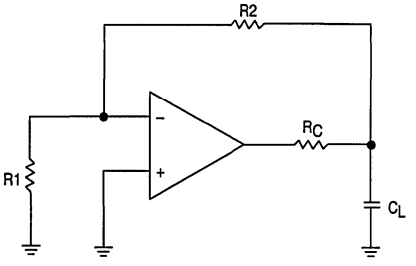
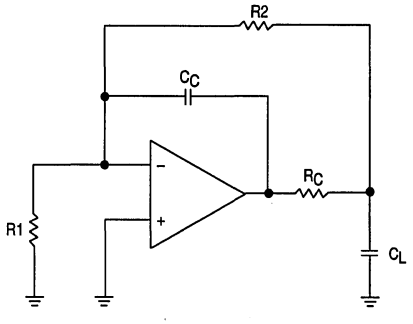


Figure 36. Compensation Circuit for High Capacitive Loads



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33218

Advance Information

Voice Switched Speakerphone with Microprocessor Interface

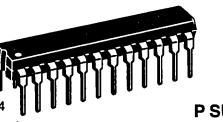
VOICE SWITCHED SPEAKERPHONE with μPROCESSOR INTERFACE

The Motorola MC33218 Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality, hands-free speakerphone system. Included are a microphone amplifier with mute, transmit and receive attenuators, a background monitoring system for both transmit and receive paths, and level detectors for each path. An AGC system reduces the receive gain on long lines where loop current and power are in short supply. A dial tone detector prevents loss of dial tone.

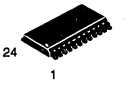
Additionally, the MC33218 has a serial data port which allows microprocessor control of various functions such as volume control, mute, attenuator range selection, and selection of receive, transmit, idle, or normal mode. The data port can be operated up to 1.0 MHz.

The MC33218 is available in a 24 pin, narrow body DIP, and a wide body SOIC package.

- Supply Voltage Range: 2.5 to 6.5 V
- Attenuator Range: 52 dB or 26 dB (Selectable)
- Background Noise Monitor for Each Path
- Microphone Amplifier with Mute Function
- 2 Point Signal Sensing
- Microprocessor Port for 8-bit Serial Data Entry Controls:
- Digital Volume Control (16 Steps)
- Attenuator Range Selection (52 dB or 26 dB)
- Mute Microphone Amplifier
- Force to Receive, Transmit, Idle, or Normal Operating Mode
- Chip Deselect Pin Powers Down Entire IC

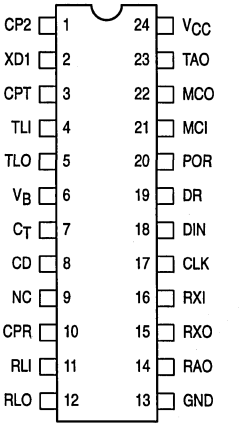


P SUFFIX
PLASTIC PACKAGE
CASE 724



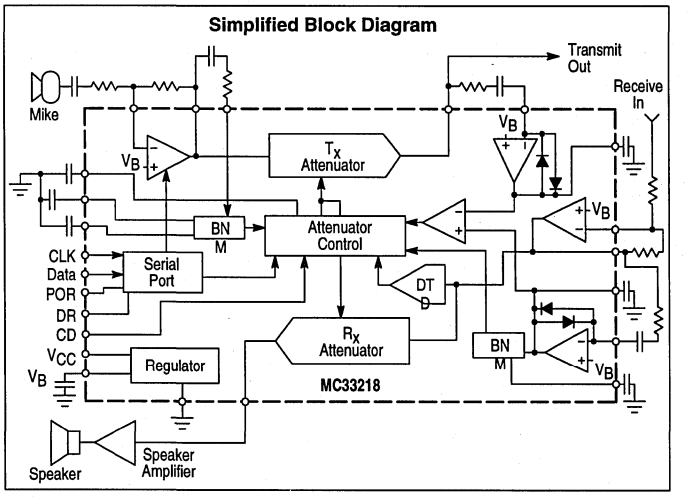
DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO-24L)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Temperature Range	Package
MC33218DW	– 40° to + 85°C	SO-24L
MC33218P		Plastic DIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	– 0.5	+7.0	Vdc
Maximum Junction Temperature	T_J	—	+150	°C
Storage Temperature Range	T_{stg}	– 65	+150	°C

Devices should not be operated at or outside these values. The "Recommended Operating Limits" table provides for actual device operation.

RECOMMENDED OPERATING LIMITS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage (Non-AGC Range) (AGC Range)	V_{CC}	3.5 2.5	— —	6.5 6.5	Vdc
Maximum Attenuator Input Signal	$V_{in(max)}$	—	—	350	mVrms
Clock and Data Rate (Serial Port)	F_{Data}	0	—	1.0	MHz
Operating Temperature Range	T_A	– 40	—	+ 85	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, f_{CLK} = 1.0 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Current (Enabled, CD = 0) Idle Mode Receive Mode Transmit Mode	I_{CC}	 3.0 — —	 4.0 5.0 5.0	 6.0 — —	mA
Supply Current (Disabled, CD = 1)	I_{CC}	—	50	85	µA
CD Input Resistance	R_{CD}	170	250	300	kΩ
V_B Output Voltage (I_{VB} = 0)	V_B	2.1	2.2	2.3	Vdc
V_B Output Resistance	R_{OVB}	—	300	—	W
ATTENUATOR CONTROL					
C_T Voltage (Full Attenuation Range) R_X Mode Idle Mode T_X Mode	$V_{CT} - V_B$	 — — —	 +150 0 – 105	 — — —	mV
C_T Current Source (Switching to R_X Mode) Sink (Switching to T_X Mode) Idle	 I_{CTR} I_{CTT} I_{CTI}	 – 55 65 – 3.0	 – 40 85 0	 – 25 115 3.0	µA
Receive Dial Tone Detector Threshold	V_{DT}	– 40	– 20	– 8.0	mV

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, f_{CLK} = 1.0 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ATTENUATORS					
Receive Attenuator Gain (f = 1.0 kHz)					dB
Full Volume, Full Attenuation Range					
R_X Mode	G_{RX}	3.0	6.0	9.0	
T_X Mode	G_{RXT}	– 49	– 46	– 43	
Idle Mode	G_{RXI}	– 28	– 25	– 22	
Range (R_X to T_X Mode)	ΔG_{RX}	49	52	55	
Full Volume, Half Attenuation Range					dB
R_X Mode	G_{RX}	– 10	– 7.0	– 4.0	
T_X Mode	G_{RXT}	– 37	– 34	– 31	
Idle Mode	G_{RXI}	– 28	– 25	– 22	
Range (R_X to T_X Mode)	ΔG_{RX}	23	26	29	
Volume Control Range (Rx Mode)	V_{CR}	31	37	41	dB
AGC Attenuation Range (V_{CC} = 3.5 to 2.7 V)	G_{AGC}	—	6.0	—	dB
RAO Offset Voltage With Respect to V_B	V_{RAO}				mVdc
(R_X Mode)		—	– 10	—	
(T_X Mode)		—	0	—	
Transmit Attenuator Gain (f = 1.0 kHz)					dB
Full Attenuation Range					
T_X Mode	G_{TX}	3.0	6.0	9.0	
R_X Mode	G_{TXR}	– 49	– 46	– 43	
Idle Mode	G_{TXI}	– 19	– 16	– 13	
Range (T_X to R_X Mode)	ΔG_{TX}	49	52	55	
Half Attenuation Range					
T_X Mode	G_{TX}	– 9.0	– 6.0	– 3.0	
R_X Mode	G_{TXR}	– 36	– 33	– 30	
Idle Mode	G_{TXI}	– 19	– 16	– 13	
Range (T_X to R_X Mode)	ΔG_{TX}	23	26	29	
TAO Offset Voltage With Respect to V_B	V_{TAO}				mVdc
(R_X Mode)		—	0	—	
(T_X Mode)		—	– 60	—	
RAO, TAO					Vdc
High Voltage (I_L = – 1.0 mA)	V_{TAOH}	3.7	4.1	—	
Low Voltage (I_L = +1.0 mA)	V_{TAOL}	V_B – 1.0	V_B – 1.4	V_B – 3.0	
AMPLIFIERS — Microphone Amplifier					
Output Offset with Respect to V_B	MCO_{VOS}	—	0	—	mVdc
Open Loop Gain (f < 100 Hz)	A_{VOL}	—	80	—	dB
Gain Bandwidth	GBW	—	0.8	—	MHz
Output High Voltage (I_{out} = – 1.0 mA)	V_{MCOH}	3.7	4.1	—	Vdc
Output Low Voltage (I_{out} = +1.0 mA)	V_{MCOL}	0	140	250	mVdc
Transmit Path Muting (Δ Gain) Pin 21 to Pin 23	GMT				dB
Microphone Amp (R_{Fdbk} = 300 kΩ), plus Transmit Attenuator in R_X Mode		80	125	—	
AMPLIFIERS — Receive Amplifier					
DC Voltage (R_X Mode)	V_{RXO}	—	V_B	—	Vdc
Output High Voltage (I_{out} = – 1.0 mA)	V_{RXOH}	3.7	4.0	—	Vdc
Output Low Voltage (I_{out} = +1.0 mA)	V_{RXOL}	—	100	250	mVdc

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, f_{CLK} = 1.0 MHz, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
LEVEL DETECTORS AND BACKGROUND NOISE MONITORS					
Transmit/Receive Switching Threshold	I_{TH}	0.8	1.0	1.2	µA/µA
CPR, CPT Output Resistance	R_{CP}	—	5.0	—	W
CPR, CPT Leakage Current	I_{CPLK}	—	– 0.1	—	µA
T_X and R_X Level Detector Source Current Sink Current	 I_{LDOH} I_{LDOL}	 — —	 – 2.6 2.0	 — —	 mA µA
CLOCK AND DATA					
POR Input Resistance	R_{POR}	70	115	160	kΩ
Data In/Clock Input Resistance (High) V_{in} = 5.0 V (Low) V_{in} = 0.9 V	R_{CLK}	 35 70	 55 120	 85 160	kΩ
Data Ready Input Resistance (High) V_{in} = 5.0 V (Low) V_{in} = 0.9 V	R_{DR}	 10 25	 20 45	 30 65	kΩ
Logic Input Threshold	V_{TH}	—	1.5	—	V
SYSTEM					
R_X Mode Distortion R_X Amplifier and Attenuator (f = 1.0 kHz, V_{in} = 350 mVrms) T_X Mode Distortion T_X Attenuator and Microphone Amplifier (f = 1.0 kHz, V_{in} = 3.5 mVrms)	THD_R THD_T	— —	0.3 0.3	3.0 3.0	%

TEMPERATURE CHARACTERISTICS (V_{CC} = 5.0 V, CD ≤ 0.8 V, f_{CLK} = 1.0 MHz, unless otherwise noted.)

Parameter	Typical Value @ – 40°C	Typical Value @ + 25°C	Typical Value @ + 85°C	Unit
V_{CC} Supply Current Idle Mode (Enabled, CD = 0) All Modes (Disabled, CD = 1)	 4.7 60	 4.2 50	 3.7 75	 mA µA
V_B	2.1	2.2	2.3	V
Receive Attenuator Range (f = 1.0 kHz) Full Volume Full Attenuation Range Half Attenuation Range	 52 26	 52 26	 53 27	dB
Transmit Attenuator Range (f = 1.0 kHz) Full Attenuation Range Half Attenuation Range	 52 26	 52 26	 53 27	dB
Transmit Path Muting (Δ Gain, Pin 21 to 23) Microphone Amp (R_{Fdbk} = 300 kΩ), plus Transmit Attenuator in R_X Mode	128	127	128	dB
Volume Control Range (R_X Mode)	34	36	40	dB

PIN FUNCTION DESCRIPTION

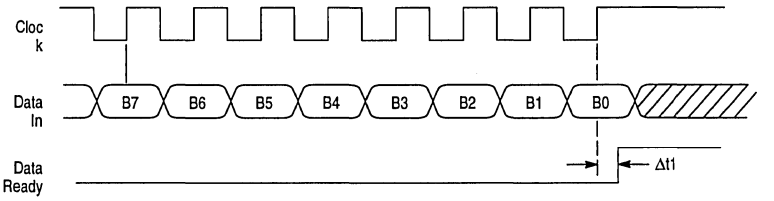
Name	Pin No.	Description
CP2	1	A capacitor at this pin stores a voltage representing the transmit background noise level.
XDI	2	Input to the transmit background noise monitor.
CPT	3	An RC sets the time constant for the transmit background noise monitor.
TLI	4	Input to the transmit level detector.
TLO	5	Output of the transmit level detector.
V_B	6	A reference voltage, and analog ground for the amplifiers.
C_T	7	An RC sets the response time to switch among the various modes.
CD	8	Chip deselect (Logic input). When low, the IC is active. When high, the entire IC is powered down and non-functional.
NC	9	No internal connection.
CPR	10	An RC sets the time constant for the receive background noise monitor.
RLI	11	Input to the receive level detector.
RLO	12	Output of the receive level detector.
GND	13	Ground pin for the entire IC.
RAO	14	Output of the receive attenuator.
RXO	15	Output of the receive path input amplifier, and input of the receive attenuator.
RXI	16	Inverting input of the receive path input amplifier.
CLK	17	Serial Port Clock. 1.0 MHz maximum, data is entered on clock's rising edge.
D_{IN}	18	Serial Port Data Input. Enter an 8-bit word, B7 first, B0 last.
DR	19	Serial Port Data Ready. Taking this line high latches new data in the registers.
POR	20	Power On Reset. Upon power up and/or enabling, all bits are set to 0.
MCI	21	Inverting input of the microphone amplifier.
MCO	22	Output of the microphone amplifier, and input of the transmit attenuator.
TAO	23	Output of the transmit attenuator.
V_{CC}	24	Power Supply pin. Operating range is 2.5 V to 6.5 Vdc.

Bits	Code	Function
B7, B6	00 01 10 11	Normal voice switched operation. Force to receive mode. Force to idle mode. Force to transmit mode.
B5	0 1	Attenuator range is 52 dB. Attenuator range is 26 dB.

Bits	Code	Function
B4	0 1	Microphone amplifier is active. Microphone amplifier is mute.
B3 – B0*	0000 1111	Maximum receive volume. Minimum receive volume.

*Bit B0 is the LSB for the volume control.

Figure 1. Serial Port Timing Diagram



NOTES: 1. Maximum clock and data rate is 1.0 MHz. There is no required minimum rate.
2. B7 is to be entered first, B0 last.
3. Data is entered on the clock rising edge.
4. Clock can continue to toggle after B0 is entered if Data Ready goes high before the clock's next rising edge.
5. Clock-to-data setup and hold times, and minimum Δt1 to be determined.
6. Upon power up, all bits are internally set to logic 0.

Figure 2. Typical Application

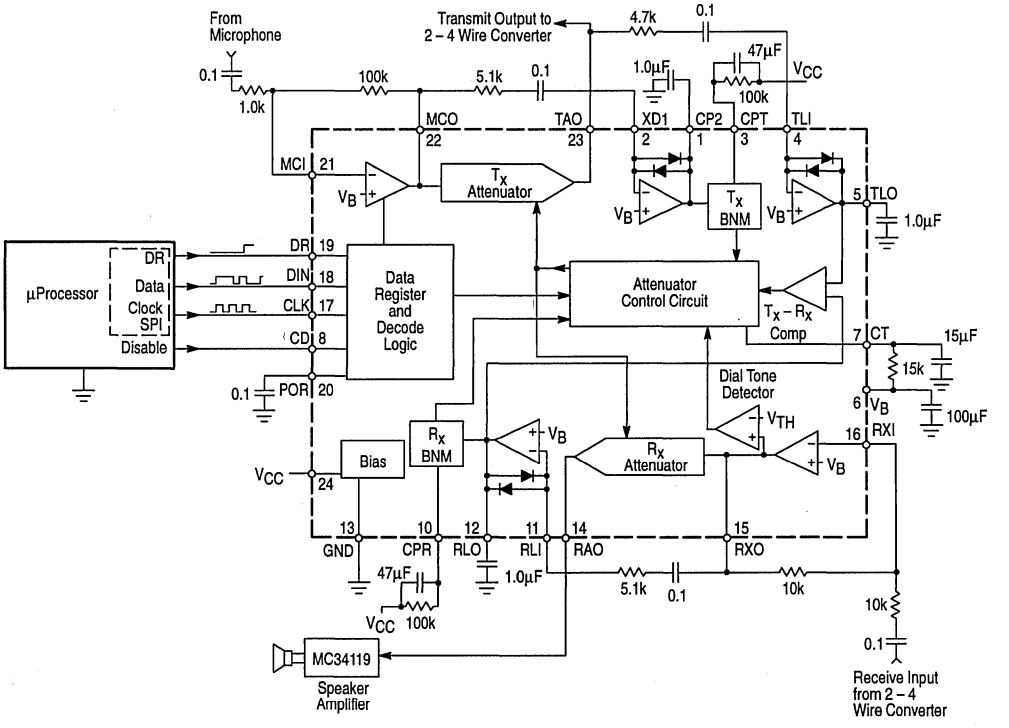


Figure 3. Attenuator Gain versus V_{CT}

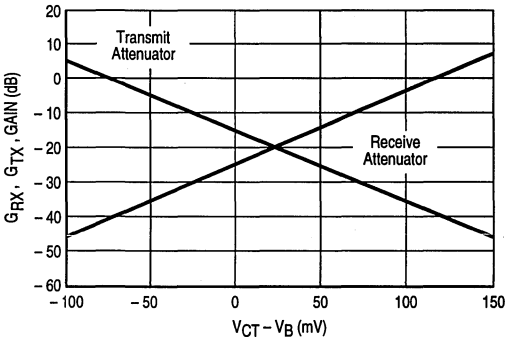


Figure 4. Attenuator Gain versus V_{CT} (Half Attenuation Range)

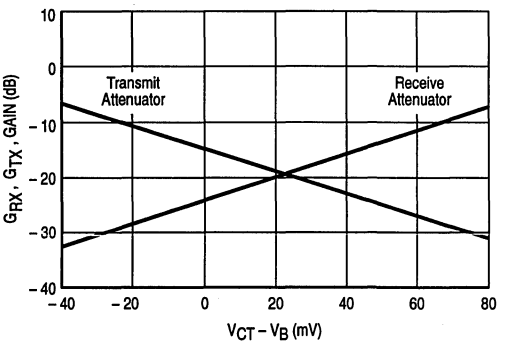


Figure 5. Level Detector DC Transfer Characteristics

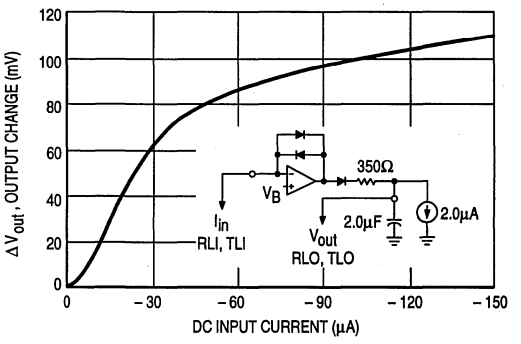


Figure 6. Level Detector AC Transfer Characteristics

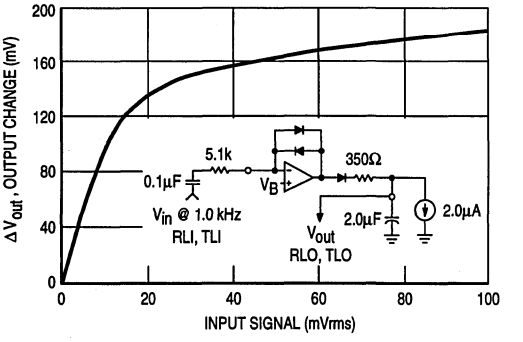


Figure 7. Level Detector AC Transfer Characteristic versus Frequency

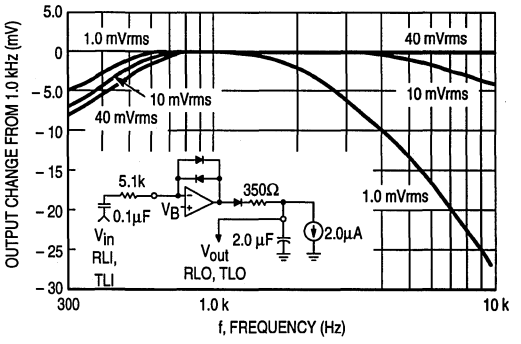


Figure 8. Receive Gain versus Volume Setting

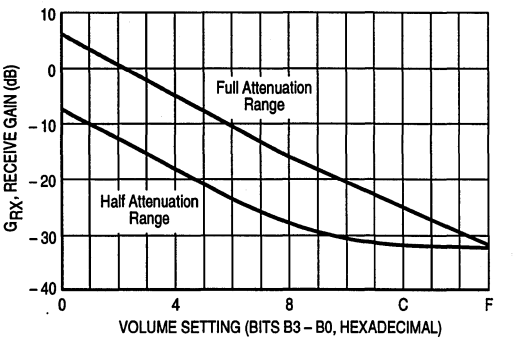


Figure 9. Supply Current versus Supply Voltage

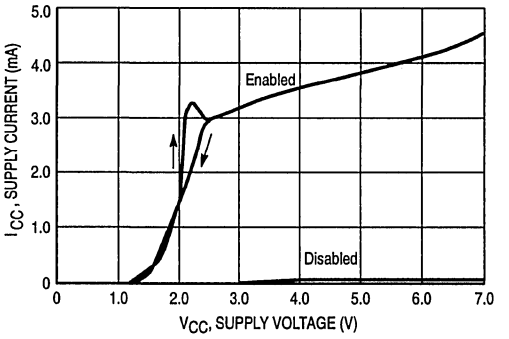


Figure 10. CD Input Characteristics

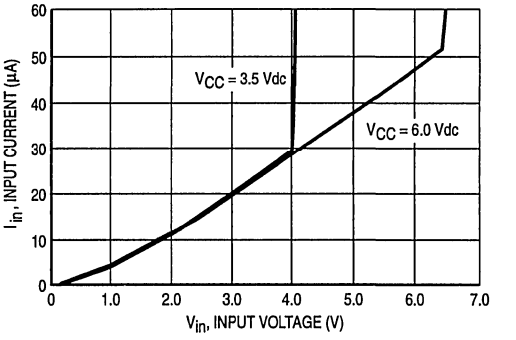


Figure 11. V_B Output Characteristics

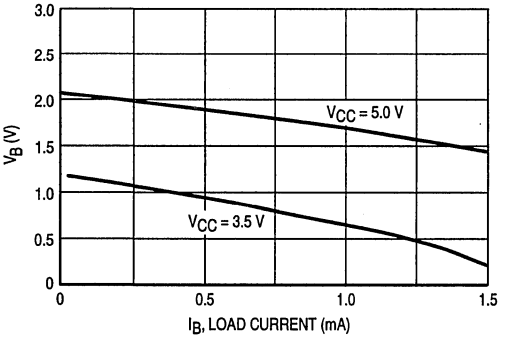


Figure 12. Typical Output Swing versus V_{CC}

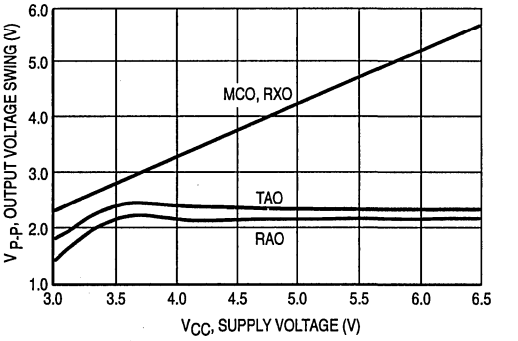


Figure 13. V_B Power Supply Rejection versus Frequency

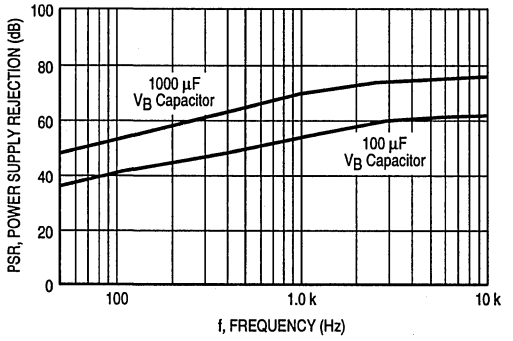


Figure 14. Data Ready, Data In, and Clock Input Characteristics

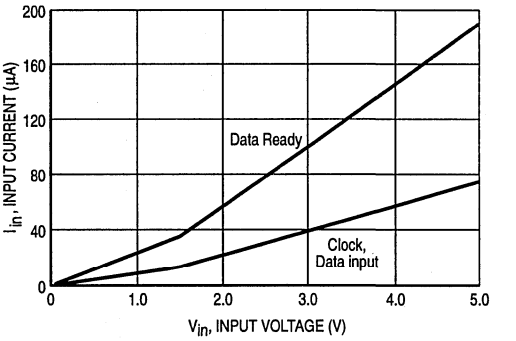
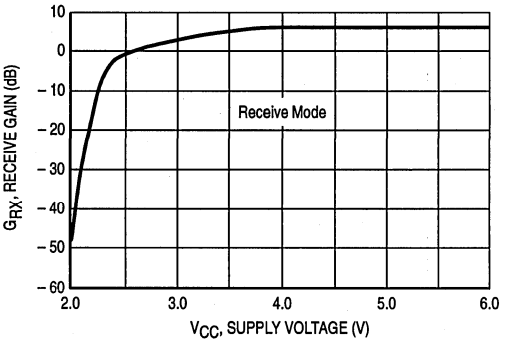


Figure 15. Receive Attenuator Gain versus V_{CC}



APPLICATIONS INFORMATION

Introduction

The MC33218 provides the necessary circuitry to perform a voice switched, half duplex, speakerphone function. The half duplex function is necessary to prevent oscillation resulting from the high gain and acoustic coupling. It includes transmit and receive attenuators, preamps, level detectors, and background noise monitors. An attenuator control circuit automatically adjusts the gain of the transmit and receive attenuators based on the microprocessor inputs and/or the relative strengths of the voice signals present.

Power Supply, V_B, and Chip Disable

The power supply voltage at Pin 24 is to be between 3.5 and 6.5 V for normal operation, with reduced operation possible down to 2.5 V (see AGC section).

The output voltage at V_B (Pin 6) is approximately equal to (V_{CC} – 0.7)/2, and provides the AC ground for the system. The output impedance at V_B is approximately 300 Ω (see Figure 9), and in conjunction with the external capacitor at V_B, forms a low pass filter for power supply rejection. The choice of V_B capacitor is application dependent based on whether the circuit is powered by the telephone line or a power supply.

The Chip Disable (Pin 8) permits powering down the IC for power conservation. With CD between 0 and 0.8 V, normal operation is in effect. With CD between 2.0 V and V_{CC}, the IC is powered down. When the IC is re-enabled, the speakerphone should return to normal mode (bits B0 – B7 equal to 0).

Transmit and Receive Attenuators

The transmit and receive attenuator sections are complementary, performing a log-antilog function. When one is at maximum gain, the other is at maximum attenuation; they are never both fully on or fully off. Both attenuators are controlled by a single output from the attenuator control which ensures the sum of their gains will remain constant at a typical value of – 40 dB. Their purpose is to provide the half-duplex operation required in a speakerphone. They are identical, and consist of a pre-amp, an input clamp, an attenuator, and a current to voltage converter. An internal control voltage determines the gain of each attenuator.

The inputs to the attenuators should not exceed 400 mVrms to prevent distortion.

Attenuator Control Section

There are five inputs to the attenuator control section: one each from the transmit/receive level comparator, dial tone detector, control logic block and transmit and receive background noise monitors. A single output sets the gain of both the transmit and receive attenuators.

A DC feedback loop samples the output current of the attenuator that is at full gain and compares it to a reference current. The resultant error current then drives an external resistor and capacitor at the C_T pin which corrects the control voltage, maintaining the desired attenuator gain. The external RC on the C_T pin determines the response time of the speakerphone.

Background Noise Monitors

The purpose of background noise monitors is to distinguish speech (which consists of bursts) from background noise (a relatively constant level). There are two background noise monitors — one for the receive path and one for the transmit path. Each is operated on by a level detector, which provides a DC voltage representative of the noise level. The voltages at the CPT and CPR pins have slow rise times (determined by an external RC), but fast decay times. When speech is present, the voltage on the non-inverting input of an internal comparator will rise faster than the voltage at the inverting input (due to the burst characteristic of speech), causing its output to change. This output is sensed by the Attenuator Control Block. The time constant of the external RCs (Pins 3 and 10) determine the response time to background noise variations.

Dial Tone Detector

Since the dial tone is considered continuous noise, the background noise monitor would tend to force the attenuators back to idle mode. The dial tone detector prevents the IC from changing to idle mode, thus preventing the dial tone from fading away. The dial tone detector is a comparator with one side connected to the input of the receive attenuator and the other input connected to V_B with a 15 mV offset. If the circuit is in the receive mode and the incoming signal is greater than 15 mV, the comparator's output will change, disabling the receive idle mode. The receive attenuator gain will then be determined solely by the volume control.

AGC

In the receive mode, the AGC circuit decreases the gain of the receive attenuator when the supply voltage at V_{CC} falls below 3.5 V to prevent the speaker from clipping or distorting. The purpose of this feature is to reduce the power (and current) used by the speaker when a line-powered speakerphone is connected to a long telephone line, where the available power is limited. Reducing the speaker power controls the voltage sag at V_{CC} and prevents clipping and distortion on the speaker output.

Microprocessor Control

The data register and decode logic are used to interface the data from the serial port to the required internal circuitry. This enables microprocessor control of the following functions:

Volume Control (16 levels)
Microphone Mute
Attenuator Range (52 dB or 26 dB)
Mode Select: Normal, Transmit, Receive, Idle

The logic inputs should not exceed V_{CC}, and they should never be allowed to go below ground. The maximum clock frequency is 1.0 MHz.

On power up, the internal registers are reset to all zeros (normal mode). An internal capacitor on the Power-on-Reset pin prevents the registers from accepting data input before the supply voltage has stabilized.

Volume Control

The volume control enables the receive attenuator gain to be increased or decreased in 16 equal 2.5 dB steps, independent of temperature, by microprocessor control. On power up, the volume control will be reset to maximum (bits B3 – B0 will be 0000). Bit B0 is the least significant bit (LSB), and bit B3 is the most significant bit (MSB). The transmit attenuator gain will be varied in a complementary manner.

Microphone Amplifier Mute

When activated by the microprocessor by pulling bit B4 high, it reduces the gain of the amplifier by approximately – 75 dB. For additional muting, force the Mode Select (bits B6 and B7) to receive during mute. This will ensure the transmit attenuator is at 46 dB of attenuation (in full range) and will provide a combined attenuation of 120 dB in the transmit path.

Attenuator Range Selection

Bit B5, the Attenuator Range Selector, provides a choice of 52 dB attenuation range (– 46 dB to + 6.0 dB, nominally) or 26 dB range (– 32 db to – 6.0 dB). At half attenuation, the volume control range will be reduced to approximately 26 dB (see Figure 6).

Mode

The MC33218 can be forced to transmit, receive, or idle mode by microprocessor input by using bits B7 and B6. The attenuators will be in the transmit mode for a (V_{CT}–V_B) of – 105 mV and the receive mode for a (V_{CT}–V_B) of + 150 mV. At idle mode, (V_{CT}–V_B) is approximately zero. The mode selection provides manual or remote control for testing, to overcome noise on the line, or to increase the transmit path attenuation during mute.

RFI Interference

Potential radio frequency interference (RFI) problems should be addressed early in the electrical and mechanical design of the speakerphone. RFI may enter the circuit through Tip and Ring, through the microphone wiring to the microphone amplifier, or through any of the PC board traces. The most sensitive pins on the MC33218 are the inputs to the level detectors (RLI, TLI) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. The board traces to these pins should be kept short, and the resistor and capacitor for each of these pins should be physically close to the pins. Any other high impedance input pin should also be considered sensitive to RFI signals.

In the Final Analysis

Proper operation of a speakerphone is a combination of proper mechanical (acoustic) design as well as proper electronic design. The acoustics of the enclosure must be considered early in the design of a speakerphone. In general, electronics cannot compensate for poor acoustics, low speaker quality, or any combination of the two. Proper acoustic separation of the speaker and microphone is essential. The physical location of the microphone, along with the characteristics of the selected microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

In the final analysis, the circuit shown in this data sheet will have to be fine tuned to match the acoustics of the enclosure, the specific hybrid, and the specific speaker and microphone selected. The components shown in this data sheet should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at the microphone and speaker amplifiers, respectively. The switching response can then be fine tuned by varying (in small steps) the components at the level detector inputs until satisfactory operation is obtained for both long and short lines.

For additional information on speakerphone design, please refer to the data sheet for the MC34118 Speakerphone IC.

GLOSSARY

AGC – *Automatic gain control.* In the speakerphone, the gain of the attenuators is reduced as the supply voltage decreases to prevent clipping or distortion on the output.

Attenuation – A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth – The range of information carrying frequencies of a communication system.

C-Message Filter – A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

Channel Separation – The ability of one circuit to reject outputting signals which are being processed by another circuit. Also referred to as *crosstalk*, it is usually expressed in dB.

dB – A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

10 x log (P1/P2) for power measurements, and
20 x log (V1/V2) for voltage measurements.

dBm – An indication of signal power. 1.0 mW across 600 Ω, or 0.775 Vrms, is typically defined as 0 dBm for telecom applications. Any voltage level is converted to dBm by:

dBm = 20 x log (Vrms/0.775), or
dBm = [20 x log (Vrms)] + 2.22.

dBmp – Indicates dBm measurement using a psophometric weighting filter.

dBrn – Indicates a dBm measurement relative to 1.0 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = – 90 dBm.

dBrnC – Indicates a dBrn measurement using a C-message weighting filter.

DTMF – *Dual Tone Multi Frequency.* It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad.

Four-Wire Circuit – The portion of a telephone or central office, which operates on two pairs of wires. One pair is for the Transmit path (generally from the microphone), and one pair is for the Receive path (generally from the receiver).

Full-Duplex – A transmission system which permits communication in both directions simultaneously. The standard handset telephone is full-duplex.

Gain – The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Half-Duplex – A transmission system which permits communication in one direction at a time. CB radios, with "push-to-talk" switches, and voice activated speakerphones, are half-duplex.

Hookswitch – A switch which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Hybrid – Another name for a two-to-four wire converter.

Line Length Compensation – Also referred to as *loop compensation*, it involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less, and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length.

Loop – The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground or AC power.

Loop Current – The DC current which flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20 to 120 mA.

Off-Hook – The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the DC current as an indication that the phone is busy.

On-Hook – The condition when the telephone is disconnected from the phone system, and no DC loop current flows. The central office regards an on-hook phone as available for ringing.

Power Supply Rejection Ratio – The ability of a circuit to reject outputting noise, or ripple, which is present on the power supply lines. PSRR is usually expressed in dB.

Pulse Dialing – A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 times per second. The old rotary phones, and many new pushbutton phones, use pulse dialing.

Receive Path – Within the telephone, it is the speech path from the phone line to the earpiece.

Ring – One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

Sidetone – The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2-to-4 wire conversion system. Sidetone was recognized by Alexander Graham Bell as necessary for a person to be able to speak properly while using a handset.

Signal to Noise Ratio – The ratio of the desired signal to unwanted signals (noise) within a defined frequency range. The larger the number, the better.

Speech Network – A circuit which provides 2-to-4 wire conversion, i.e. connects the microphone and receiver (or the transmit and receive paths) to the Tip and Ring phone lines. Additionally, it provides sidetone control, and in many cases, the DC loop current interface.

Tip – One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

Transmit Path – Within the telephone, it is the speech path from the microphone to the phone line.

Two-to-Four Wire Converter – A circuit which has four wires (on one side); two (signal and ground) for the outgoing signal, and two for the incoming signal. The outgoing signal is sent out differentially on the two-wire side (the other side), and incoming differential signals received on the two-wire side are directed to the four-wire side. Additional circuitry within cancels the reflected outgoing signal to keep it separate from the incoming signal.

Voiceband – That portion of the audio frequency range used for transmission across the telephone system. Typically, it is 300 to 3400 Hz.

MC34010

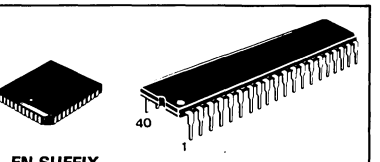
Advance Information

ELECTRONIC TELEPHONE CIRCUIT

- Provides All Basic Telephone Station Apparatus Functions in a Single IC, Including DTMF Dialer, Tone Ringer, Speech Network and Line Voltage Regulator
- DTMF Generator Uses Low-Cost Ceramic Resonator with Accurate Frequency Synthesis Technique
- Tone Ringer Drives Piezoelectric Transducer and Satisfies EIA RS-470 Impedance Signature Requirements
- Speech Network Provides Two–Four Wire Conversion with Adjustable Sidetone Utilizing an Electret Transmitter
- On-Chip Regulator Insures Stable Operation Over Wide Range of Loop Lengths
- I^2L Technology Provides Low 1.4 Volt Operation and High Static Discharge Immunity
- Microprocessor Interface Port for Automatic Dialing Features

ELECTRONIC TELEPHONE CIRCUIT

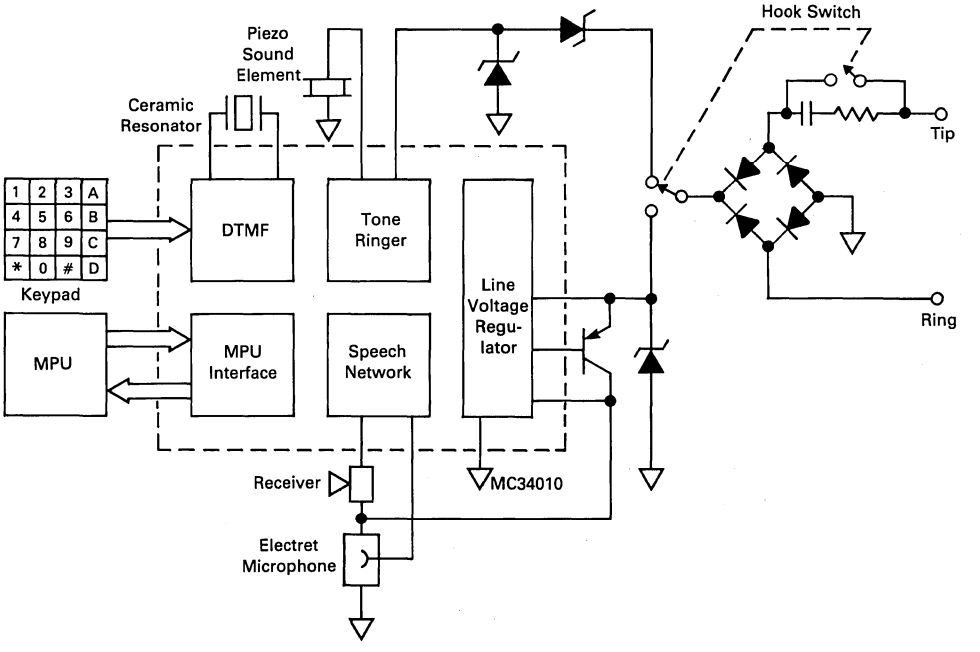
BIPOLAR LINEAR/I^2L



FN SUFFIX
44-PIN
PLCC
CASE 777

P SUFFIX
PLASTIC PACKAGE
CASE 711

FIGURE 1 — ELEMENTS OF THE ELECTRONIC TELEPHONE

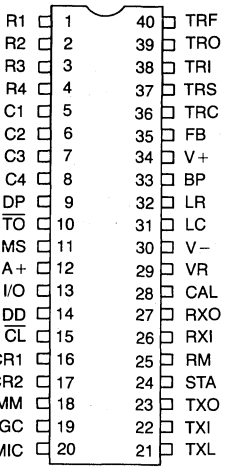


This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (Voltage References to V−)

Parameter	Value	Unit
V+ Terminal Voltage (Pin 34)	+20, −1.0	V
VR Terminal Voltage (Pin 29)	+2.0, −1.0	V
RXO Terminal Voltage (Pin 27)	+2.0, −1.0	V
TRS Terminal Voltage (Pin 37)	+35, −1.0	V
TRO (With Tone Ringer Inactive) Terminal Voltage	+2.0, −1.0	V
R1–R4 Terminal Current (Pins 1–4) C1–C4 (Pins 5–8)	±100	mA
$\overline{CL}$, $\overline{TO}$, DD, I/O, A+	+122, −1.0	V
Operating Ambient Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

PIN CONNECTIONS



GENERAL CIRCUIT DESCRIPTION

Introduction

The MC34010 Electronic Telephone Circuit (ETC) provide all the necessary elements of a tone dialing telephone in a single IC. The functional blocks of the ETC include the DTMF dialer, speech network, tone ringer, and dc line interface circuit (Figure 1). The MC34010 also provides a microprocessor interface port that facilitates automatic dialing features.

Low voltage operation is a necessity for telephones in networks where parallel telephone connections are common. An electronic speech network operating in parallel with a conventional telephone may receive line voltages below 2.5 volts. DTMF dialers operate at similarly low-line voltages when signaling through battery powered station carrier equipment. These low voltage requirements have been addressed by realizing the MC34010 in a bipolar/I^2L technology with appropriate circuit techniques. The resulting speech and dialer circuits maintain specified performance with instantaneous input voltage as low as 1.4 volts.

Line Voltage Regulator

The dc line interface circuit (Figure 3) determines the dc input characteristic of the telephone. At low input voltages (less than 3 volts) the ETC draws only the

FIGURE 3 — DC LINE INTERFACE BLOCK DIAGRAM

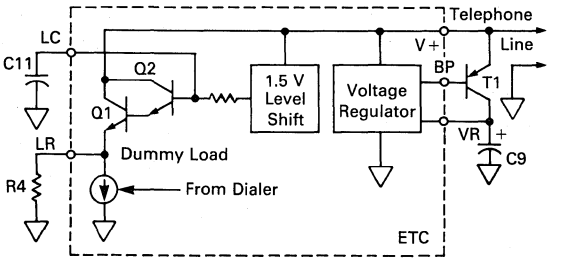
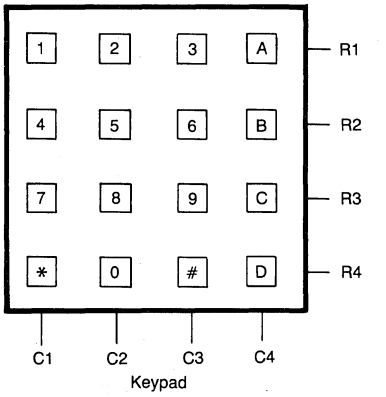


FIGURE 2 — MPU INTERFACE CODES

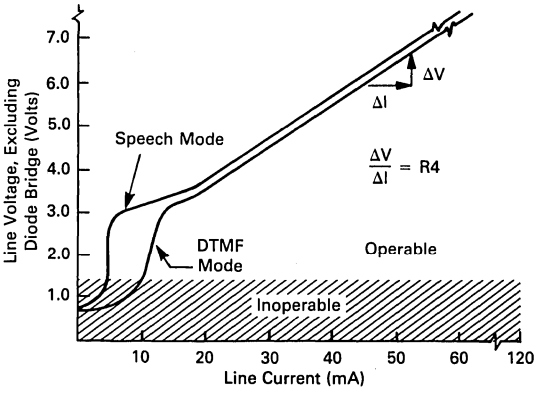


Key	Row	Column	Code (B3–B0)
1	1	1	1111
2	1	2	0111
3	1	3	1011
4	2	1	1101
5	2	2	0101
6	2	3	1001
7	3	1	1110
8	3	2	0110
9	3	3	1010
0	4	2	0100
A	1	4	0011
B	2	4	0001
C	3	4	0010
D	4	4	0000
*	4	1	1100
#	4	3	1000

GENERAL CIRCUIT DESCRIPTION (continued)

speech and dialer bias currents through the VR regulator. As input voltage increases, Q1 conducts the excess dc line current through resistor R4. The 1.5 volt level shift prevents saturation of Q2 with telephone line signals up to 2.0 volts peak (+5.2 dBm). A constant current (dummy load) is switched off when the DTMF dialer is activated to reduce line current transients. Figure 4 illustrates the dc voltage/current characteristic of an MC34010 telephone.

FIGURE 4 — DC V-I CHARACTERISTIC OF THE ETC



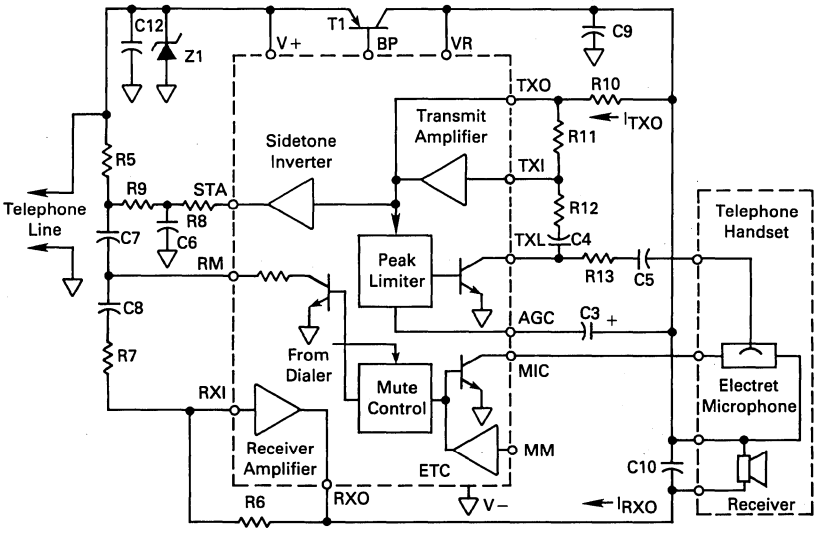
Speech Network

The speech network (Figure 5) provides the two-to-four wire interface between the telephone line and the instrument's transmitter and receiver. An electret microphone biased from VR drives the transmit amplifier. For very loud talkers, the peak limiter circuit reduces the transmit input level to maintain low distortion. The transmit amplifier output signal is inverted at the STA terminal and driven through an external R-C network to control the receiver sidetone level. The switched ac resistance at the RM terminal reduces receiver signal when dialing and suppresses clicks due to hook or keypad switch transitions. When transmitting, audio signal currents (i_{TXO} and i_{RXO}) flow through the voltage regulator pass transistor (T1) to drive the telephone line. This feature has two consequences: 1) In the transmitting mode the receiver sidetone current i_{RXO} contributes to the total signal on the line along with i_{TXO}; 2) The ac impedance of the telephone is determined by the receiver impedance and the voltage gain from the line to the receiver amplifier output.

DTMF Dialer

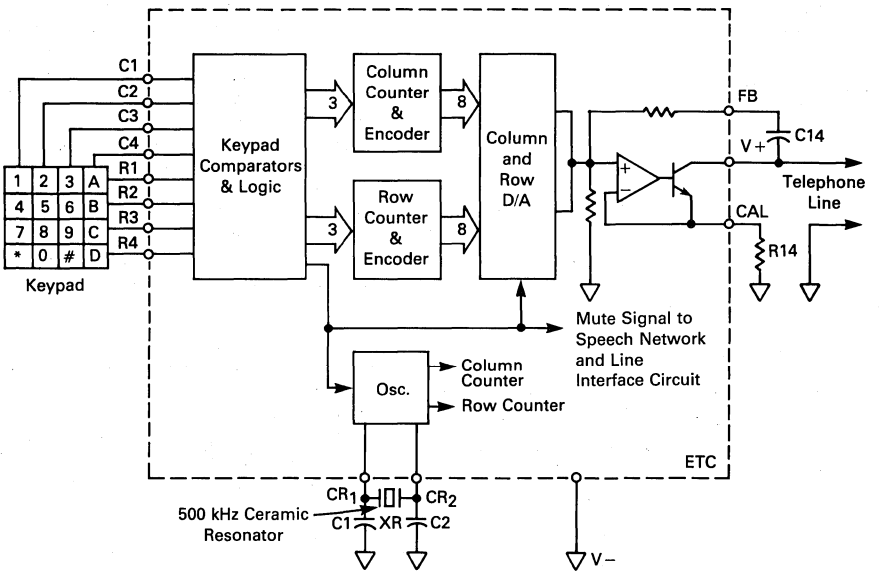
Keypad interface comparators activate the DTMF row and column tone generators (Figure 6) when a row and column input are connected through a SPST keypad. The keypad interface is designed to function with contact resistances up to 1.0 kΩ and leakage resistances as low as 150 kΩ. Single tones may be initiated by depressing two keys in the same row or column.

FIGURE 5 — SPEECH NETWORK BLOCK DIAGRAM



The programmable counters employ a novel design to produce non-integer frequency ratios. The various DTMF tones are synthesized with frequency division errors less than ±0.16% (Table 1). Consequently an inexpensive ceramic resonator can be used instead of a quartz crystal as the DTMF frequency reference. Total frequency error less than ±0.8% can be achieved with ±0.3% ceramic resonator. The row and column D/A converters produce 16-step approximations of sinusoidal waveforms. Feedback through terminal FB reduces the DTMF output impedance to approximately 2.0 kΩ to satisfy return loss specifications.

FIGURE 6 — DTMF DIALER BLOCK DIAGRAM



Tone Ringer

The tone ringer (Figure 7) generates a warbling square wave output drive to a piezo sound element when the ac line voltage exceeds a predetermined threshold level. The threshold detector uses a current mode comparator to prevent on/off chatter when the output current reduces the voltage available at the ringer input. When the average current into the tone ringer exceeds the threshold level, the ringer output TRO commences driving the piezo transducer. This output current sourced from TRI increases the average current measured by the threshold detector. As a result, hysteresis is produced beween the tone ringer on and off thresholds. The output frequency at TRO alternates between $f_O/8$ and $f_O/10$ at a warble rate of $f_O/640$, where f_O is the ringer oscillator frequency.

Microprocessor Interface

The MPU interface connects the keypad and DTMF sections of the ETC to a microprocessor for storing and retrieving numbers to be dialed. Figure 8 shows the major blocks of the MPU interface section and the interconnections between the keypad interface, DTMF generator and microprocessor. Each button of a 12 or 16 number keypad is represented by a four-bit code (Figure 2). This four-bit code is used to load the programmable counters to generate the appropriate row and column tones. The code is transferred serially to or from the microprocessor when the shift register is clocked by the microprocessor. Data is transferred through the I/O terminal, and the direction of data flow is determined by the Data Direction (DD) input terminal. In the manual dialing mode, DD is a Logic "0" and the four-bit code from the keypad is fed to the DTMF generator by the digital multiplexer and also output on the I/O terminal through the four-bit shift register. The data sequence on the I/O terminal is B3, B2, B1, B0 and is transferred on the negative edge of the clock input ($\overline{CL}$). In this mode the shift register load enable circuit cycles the register between the load and read modes such that multiple read cycles may be run for a single-key closure. Six complete clock cycles are required to output data from the ETC and reload the register for a second look.

In the automatic dialing mode, DD is a Logic "1" and the four-bit code is serially entered in the sequence B3, B2, B1, B0 into the four-bit shift register. Thus, only four clock cycles are required to transfer a number into the ETC. The keypad is disabled in this mode. A Logic "1" on the Tone Output ($\overline{TO}$) will disable tone outputs until valid data from the microprocessor is in place. Subsequently $\overline{TO}$ is switched to a Logic "0" to enable the DTMF generator. Figures 9 and 10 show the timing waveforms for the manual and automatic dialing modes and Table 2 specifies timing limitations.

The keypad decoder's exclusive OR circuit generates the DP and MS output signals. The DP output indicates (when at a Logic "1") that one, and only one, key is

depressed, thereby indicating valid data is available to the MPU. The DP output can additionally be used to initiate a data transfer sequence to the microprocessor. The MS output (when at a Logic "1") indicates the DTMF generator is enabled and the speech network is muted.

Pin A+ is to be connected to a source of 2.5 to 10 volts (generally from the microprocessor circuit) to enable the pullup circuits on the microprocessor interface outputs (DP, MS, I/O). Additionally, this voltage will power the entire circuitry (except Tone Ringer) in the absence of voltage at V+. This permits use of the transmit and receive amplifiers, keypad interface, and DTMF generator for non-typical telephone functions.

See Figure 45 for a typical interconnection to an MC6821 PIA (Peripheral Interface Adapter). Connection to a port on any other class of microprocessor will be similar.

FIGURE 7 — TONE RINGER BLOCK DIAGRAM

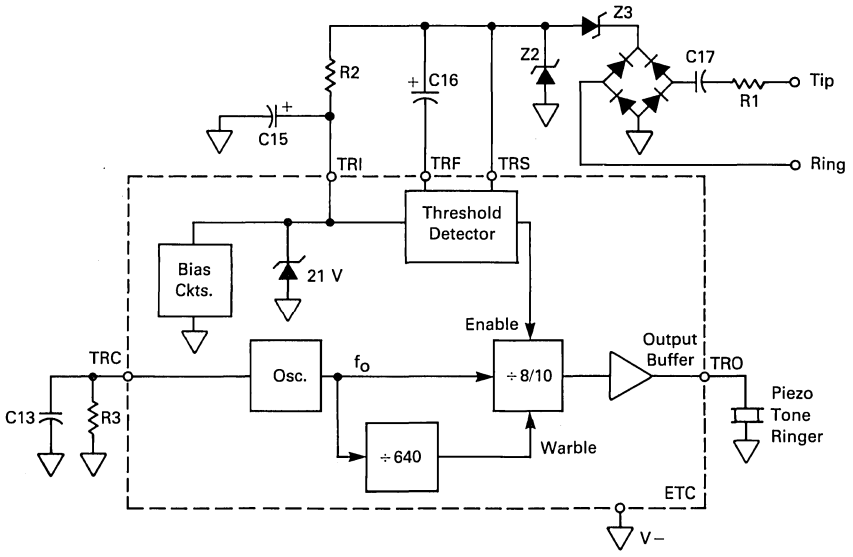


FIGURE 8 — MICROPROCESSOR INTERFACE BLOCK DIAGRAM

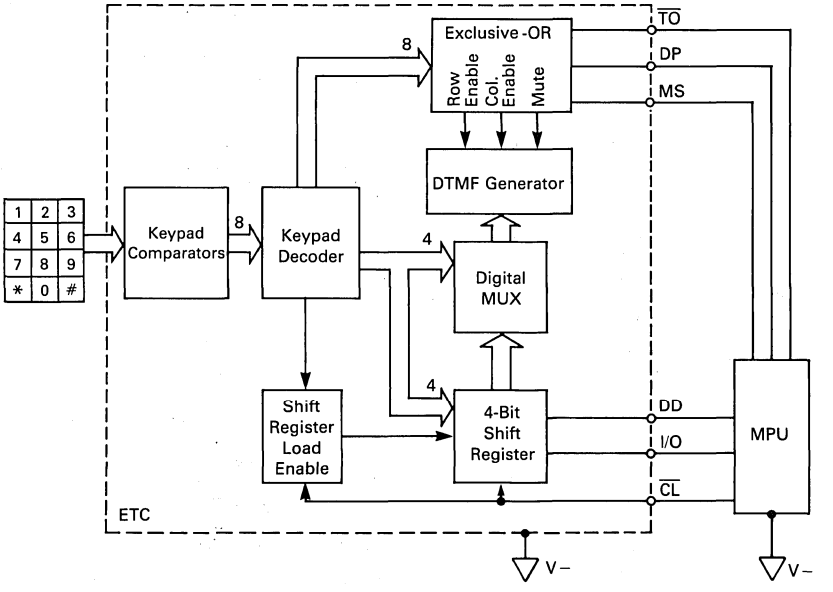


FIGURE 9 — OUTPUT DATA CYCLE

NOTE: $\overline{TO}$ may be low (Tone generator enabled) if desired.

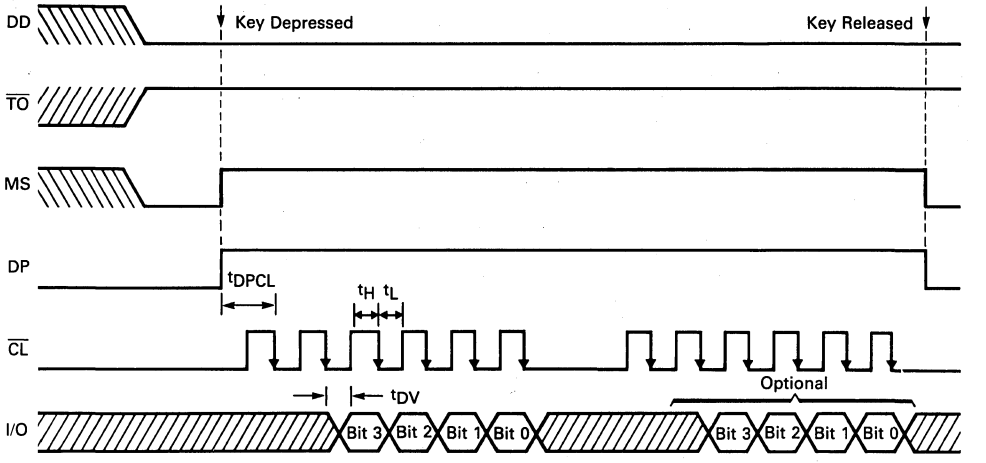


FIGURE 10 — INPUT DATA CYCLE

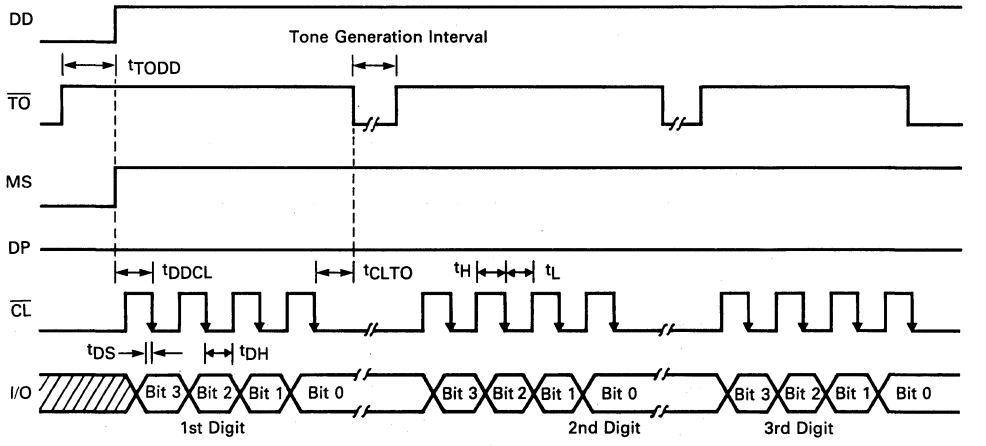


TABLE 1 — FREQUENCY SYNTHESIZER ERRORS

	DTMF Standard (Hz)	Tone Output Frequency with 500 kHz Oscillator	% Deviation from Standard
Row 1	697	696.4	−0.086
Row 2	770	769.2	−0.104
Row 3	852	853.2	+0.141
Row 4	941	939.8	−0.128
Column 1	1209	1207.7	−0.108
Column 2	1336	1336.9	+0.067
Column 3	1477	1479.3	+0.156
Column 4	1633	1634.0	+0.061

TABLE 2 — TIMING LIMITATIONS

Symbol	Parameter	Min	Typ	Max	Unit	Ref
f_{CL}	Clock Frequency	0	20	30	kHz	
t_H	Clock High Time	15	—	—	μs	Figs. 9,10
t_L	Clock Low Time	15	—	—	μs	Figs. 9,10
t_r, t_f	Clock Rise, Fall Time	—	—	2.0	μs	
t_{DV}	Clock Transition to Data Valid	—	—	10	μs	Fig. 9
t_{DPCL}	Time from DP High to $\overline{CL}$ Low	20	—	—	μs	Fig. 9
t_{DDCL}	Time from DD High to $\overline{CL}$ Low	20	—	—	μs	Fig. 10
t_{DS}	Data Setup Time	10	—	—	μs	Fig. 10
t_{DH}	Data Hold Time	10	—	—	μs	Fig. 10
t_{CLTO}	Time from $\overline{CL}$ Low to $\overline{TO}$ Low	10	—	—	μs	Fig. 10
t_{TODD}	Time from $\overline{TO}$ High to DD High	20	—	—	μs	Fig. 10

PIN DESCRIPTION

(See Figure 45 for external component identifications.)

PIN (PLCC)	PIN (DIP)	Designation	Function
1–4	1–4	R1–R4	Keypad inputs for Rows 1 through 4. When open, internal 8.0 kΩ resistors pull up the row inputs to a regulated (≈0.5 volt) supply. In normal operation, a row and a column input are connected through a SPST switch by the telephone keypad. Row inputs can also be activated by a Logic "0" (<250 mV) from a microprocessor port.
7–10	5–8	C1–C4	Keypad inputs for Columns 1 through 4. When open, internal 8.0 kΩ resistors pull down the column inputs to V−. In normal operation, connecting any column input to any row input produces the respective row and column DTMF tones. In addition to being connected to a row input, column inputs can be activated by a Logic "1" (>250 mV and <1.0 volt).
11	9	DP	Depressed Pushbutton (Output) — Normally low; A Logic "1" indicates one and only one, button of the DTMF keypad is depressed.
12	10	$\overline{TO}$	$\overline{Tone\ Output}$ (Input) — When a Logic "1," disables the DTMF generator. Keypad is not disabled.
13	11	MS	Mute/Single Tone (Output) — A Logic "1" indicates the tone generator is enabled. A Logic "0" indicates tone generator is disabled.
14	12	A+	MPU Power Supply (Input) — Enables pullups on the microprocessor section outputs. Additionally, this voltage will power the entire circuit (except Tone Ringer) in the absence of voltage at V+.
15	13	I/O	Input/Output — Serial Input or Output data (determined by DD input) to or from the microprocessor for storing or retrieving telephone numbers. Guaranteed to be a Logic "1" on powerup if DD = Logic "0."
16	14	DD	Data Direction (Input) — Determines direction of data flow through I/O pin. As a Logic "1," I/O is an input to the DTMF generator. As a Logic "0," I/O outputs keypad entries to the microprocessor.
17	15	$\overline{CL}$	$\overline{Clock}$ (Input) — Serially shifts data in or out of I/O pin. Data is transferred on negative edge typically at 20 kHz.
18,19	16,17	CR1, CR2	Ceramic Resonator oscillator input and feedback terminals, respectively. The DTMF dialer is intended to operate with a 500 kHz ceramic resonator from which row and column tones are synthesized.
31	28	CAL	Amplitude CALibration terminal for DTMF dialer. Resistor R14 from the CAL pin to V− controls the DTMF output signal level at Tip and Ring.
38	35	FB	FeedBack terminal for DTMF output. Capacitor C14 connected from FB to V+ provides ac feedback to reduce the output impedance to Tip and Ring when tone dialing.
32	29	VR	Voltage Regulator output terminal. VR is the output of a 1.1 volt voltage regulator which supplies power to the speech network amplifiers and DTMF generator during signaling. To improve regulator efficiency at low line current conditions, an external PNP pass-transistor T1 is used in the regulator circuit. Capacitor C9 frequency compensates the VR regulator to prevent oscillation.
36	33	BP	Base of a PNP Pass-transistor. Under long-loop conditions where low line voltages would cause VR to fall below 1.1 volts, BP drives the PNP transistor T1 into saturation, thereby minimizing the voltage drop across the pass transistor. At line voltages which maintain VR above 1.1 volts, BP biases T1 in the linear region thereby regulating the VR voltage. Transistor T1 also couples the ac speech signals from the transmit amplifier to Tip and Ring at V+.
37	34	V+	The more positive input to the regulator, speech, and DTMF sections connected to Tip and Ring through the polarity guard diode bridge.
33	30	V−	The dc common (more negative input) connected to Tip and Ring through the polarity guard bridge.
35	32	LR	DC Load Resistor. Resistor R4 from LR to V− determines the dc input resistance at Tip and Ring. This resistor is external not only to enable programming the dc resistance but also to avoid high on-chip power dissipation with short telephone lines. It acts as a shunt load conducting the excess dc line current. At low line voltages (<3.0 volts), no current flows through LR.
34	31	LC	DC Load Capacitor. Capacitor C11 from LC to V− forms a low-pass filter which prevents the resistor at LR from loading ac speech and DTMF signals.
22	20	MIC	MICrophone negative supply terminal. The dc current from the electret microphone is returned to V− through the MIC terminal which is connected to the collector of an on-chip NPN transistor. The base of this transistor is controlled either internally by the mute signal from the DTMF generator, or externally by the logic input pin MM.

(continued)

PIN DESCRIPTION (continued)

PIN (PLCC)	PIN (DIP)	Designation	Function
20	18	MM	Microphone Mute. The MM pin provides a means to mute the microphone in response to a digital control signal. When this pin is connected to a Logic "1" (>2.0 V) the microphone dc return path through the MIC terminal is disabled.
25	22	TXI	Transmit amplifier Input. TXI is the input to the transmit amplifier from an electret microphone. AC coupling capacitors allow the dc offset at TXI to be maintained approximately 0.6 V above V− by feedback through resistor R11 from TXO.
24	21	TXL	Transmit Input Limiter. An internal variable resistance element at the TXL terminal controls the transmitter input level to prevent clipping with high signal levels. Coupling capacitors C4 and C5 prevent dc current flow through TXL. The dynamic range of the transmit peak limiter is controlled by resistors R12 and R13.
26	23	TXO	Transmit Amplifier Output. The transmit amplifier output drives ac current through the voltage regulator pass-transistor T1 via resistor R10. The dc bias voltage at TXO is typically 0.6 volts above V−. The transmit amplifier gain is controlled by the R11/(R12 + R13) ratio.
21	19	AGC	Automatic Gain Control low-pass filter terminal. Capacitor C3 connected between AGC and VR sets the attack and decay time of the transmit limiter circuit. This capacitor also aids in reducing clicks in the receiver due to hook-switch transients and DTMF on/off transients. In conjunction with internal resistors, C3 (1.0 μF) forms a timer which mutes the receiver amplifier for approximately 20 milliseconds after the user goes off-hook or releases a DTMF Key.
30	27	RXO	Receiver Amplifier Output. This terminal is connected to the open-collector NPN output transistor of the receiver amplifier. DC bias current for the output device is sourced through the receiver from VR. The bias voltage at RXO is typically 0.6 volts above the V−. Capacitor C10 from RXO to VR provides frequency compensation for the receiver amplifier.
29	26	RXI	Receiver Amplifier Input. RXI is the input terminal of the receiver amplifier which is driven by ac signals from V+ and STA. Input coupling capacitor C8 allows RXI to be biased approximately 0.6 volts above the V− via feedback resistor R6.
28	25	RM	Receiver Amplifier Mute. A switched resistance at the RM terminal attenuates the receiver amplifier input signal produced by DTMF dialing tones at V+. RM also mutes clicks at the receiver which result from keypad or hook switch transitions. The ac resistance at RM is typically 540 Ω in the mute mode and 200 kΩ otherwise. Coupling capacitors C7 and C8 prevent dc current flow through RM.
27	24	STA	SideTone Amplifier output. STA is the output of the sidetone inverter amplifier whose input is driven by the transmit signal at TXO. The inverted transmit signal from STA subtracts from the receiver amplifier input current from V+, thus reducing the receiver sidetone level. Since the transmitted signal at V+ is phase shifted with respect to TXO by the reactive impedance of the phone line, the signal from STA must be similarly phase-shifted in order to provide adequate sidetone reduction. This phase relationship between the transmit signal at TXO and the sidetone cancellation signal from STA is controlled by R8, R9, and C6.
41	37	TRS	Tone Ringer Input Sense. TRS is the most positive input terminal of the tone ringer and the reference for the threshold detector.
42	38	TRI	Tone Ringer Input terminal. TRI is the positive supply voltage terminal for tone ringer circuitry. Current is supplied to TRI through resistor R2. When the average voltage across R2 exceeds an internal reference voltage (typically 1.6 volts) the tone ringer output is enabled.
44	40	TRF	Tone Ringer Input Filter capacitor terminal. Capacitor C16 connected from TRF to TRS forms a low-pass filter. This filter averages the signal across resistor R2 and presents this dc voltage to the input of the threshold detector. Line voltage transients are rejected if the duration is insufficient to charge C16 to 1.6 volts.
40	36	TRC	Tone Ringer oscillator Capacitor and resistor terminal. The relaxation oscillator frequency f_O is set by resistor R3 and capacitor C13 connected from TRC to V−. Typically, $f_O = (R3C13 + 8.0\ \mu s)^{-1}$.
43	39	TRO	Tone Ringer Output terminal. The frequency of the square wave output signal at TRO alternates from $f_O/8$ to $f_O/10$ at a warble rate of $f_O/640$. Typical output frequencies are 1000 Hz and 800 Hz with a 12.5 Hz warble rate. TRO sources or sinks up to 20 mA to produce an output voltage swing of 18 volts peak-to-peak across the piezo transducer. Tone ringer volume control can be implemented by a variable resistor in series with the piezo transducer.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

KEYPAD INTERFACE CIRCUIT

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
Row Input Pullup Resistance m^{th} Row Terminal: m = 1,2,3,4	7	R_{Rm}	4.0	8.0	11	kΩ
Column Input Pulldown Resistance n^{th} Column Terminal: n = 1,2,3,4	8	R_{Cn}	4.0	8.0	11	kΩ
Ratio of Row-to-Column Input Resistances $K_{m,n} = \frac{R_{Rm}}{R_{Cn}}$, m = 1,2,3,4 n = 1,2,3,4	7 & 8	$K_{m,n}$	0.88	1.0	1.12	—
Row Terminal Open Circuit Voltage	7a	V_{ROC}	280	380	500	mVdc
Row Threshold Voltage for m^{th} Row Terminal: m = 1,2,3,4	9	V_{Rm}	0.70 V_{ROC}	—	—	Vdc
Column Threshold Voltage for n^{th} Column Terminal: n = 1,2,3,4	10	V_{Cn}	—	—	0.39 V_{ROC}	Vdc

MICROPROCESSOR INTERFACE

Voltage Regulator Output A+ Regulator	29	$V_{R/A+}$	0.95	1.1	1.3	V
A+ Input Current Off-Hook	28a	I_A(off)	300	500	700	μA
A+ Input Current On-Hook	28b	I_A(on)	4.0	6.0	9.0	mA
Input Resistance (DD, $\overline{TO}$, $\overline{CL}$)	30	R_{in}	50	100	150	kΩ
Input Current (I/O)	31	I_{in}	—	80	200	μA
Input High Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	—	V_{IH}	2.0	—	A+	V
Input Low Voltage (DD, $\overline{TO}$, $\overline{CL}$, I/O)	—	V_{IL}	—	—	0.8	V
Output High Voltage (MS, DP, I/O)	32	V_{OH}	2.4	4.0	—	V
Output Low Voltage (MS, DP, I/O)	33	V_{OL}	—	0.1	0.4	V

LINE VOLTAGE REGULATOR

Voltage Regulator Output	1a	V_R	1.0	1.1	1.2	Volts
V+ Current in DTMF Mode	2a	I_{DT}	8.0	12	14	mA
Change in I_{DT} with Change in V+ Voltage	2b	ΔI_{DT}	—	0.8	2.0	mA
V+ Current in Speech Mode		I_{SP}				mA
V+ = 1.7 V	1b		3.5	5.0	7.0	
V+ = 5.0 V	1c		8.0	11	15	
Speech to DTMF Mode Current Difference	3	ΔI_{TR}	−2.0	2.0	3.5	mA
LR Level Shift		ΔV_{LR}				Vdc
V+ = 5.0 V, I_{LR} = 10 mA	4a		2.5	2.9	3.5	
V+ = 18 V, I_{LR} = 110 mA	4b		2.8	3.3	4.0	
LC Terminal Resistance	5	R_{LC}	30	50	75	kΩ
Load Regulation	6	ΔV_R	−20	−6.0	20	mVdc

ELECTRICAL CHARACTERISTICS (continued)

SPEECH NETWORK

Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
MIC Terminal Saturation Voltage	20	V_{MIC}	—	60	125	mVdc
MIC Terminal Leakage Current	21a	I_{MIC}	—	0.0	12.0	μA
MM Terminal Input Resistance	21b	R_{MM}	50	100	170	kΩ
TXO Terminal Bias	22a	B_{TXO}	0.46	0.53	0.62	—
TXI Terminal Input Bias Current	22b	I_{TXI}	—	50	250	nA
TXO Terminal Positive Swing	22c	$V_{TXO}(+)$	—	25	60	mVdc
TXO Terminal Negative Swing	22d	$V_{TXO}(-)$	—	130	200	mVdc
Transmit Amplifier Closed-Loop Gain	23a	G_{TX}	16.5	19	20	V/V
Sidetone Amplifier Gain	23b	G_{STA}	0.41	0.45	0.55	V/V
STA Terminal Output Current	24	I_{STA}	50	100	250	μA
RXO Terminal Bias	25a	B_{RXO}	0.46	0.62	0.62	—
RXI Terminal Input Bias Current	25b	I_{RXI}	—	100	400	nA
RXO Terminal Positive Swing	25c	$V_{RXO}(+)$	—	1.0	20	mVdc
RXO Terminal Negative Swing	25d	$V_{RXO}(-)$	—	40	100	mVdc
TXL Terminal OFF Resistance	26a	$R_{TXL}(OFF)$	125	200	300	kΩ
TXL Terminal ON Resistance	26b	$R_{TXL}(ON)$	—	20	100	Ω
RM Terminal OFF Resistance	27a	$R_{RM}(OFF)$	125	180	300	kΩ
RM Terminal ON Resistance	27b	$R_{RM}(ON)$	410	570	770	Ω

DTMF GENERATOR

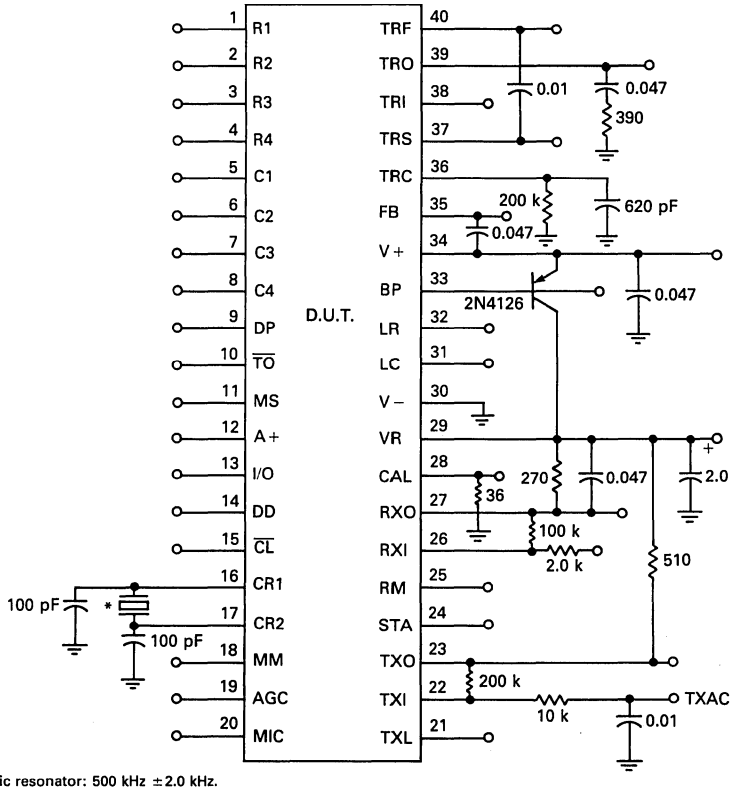
Row Tone Frequency	Row 1	11a, 11b	f_{Rm}	692.9	696.4	699.9	Hz
	Row 2			765.3	769.2	773.0	
	Row 3			848.9	853.2	857.5	
	Row 4			935.1	939.8	944.5	
Column Tone Frequency	Column 1	11c, 11d	f_{Cn}	1201.6	1207.7	1213.7	Hz
	Column 2			1330.2	1336.9	1343.6	
	Column 3			1471.9	1479.3	1486.7	
	Column 4			1625.2	1633.4	1641.5	
Row Tone Amplitude		11e	V_{Row}	0.34	0.39	0.50	V_{rms}
Column Tone Amplitude		11f	V_{Col}	0.43	0.48	0.62	V_{rms}
Column Tone Pre-emphasis		11g	dB_{CR}	0.5	1.8	3.0	dB
DTMF Distortion		12	% Dis	—	4.0	6.0	%
DTMF Output Resistance		13	R_o	1.0	2.5	3.0	kΩ

ELECTRICAL CHARACTERISTICS (continued)

TONE RINGER

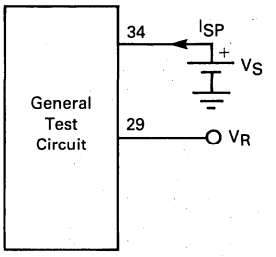
Characteristic	Test Method	Symbol	Min	Typ	Max	Unit
TRI Terminal Voltage	14	V_{TRI}	20	21.5	23	Vdc
TRS Terminal Input Current		I_{TRS}				
V_{TRS} = 24 volts	15a		70	120	170	μA
V_{TRS} = 30 volts	15b		0.4	0.8	1.5	mA
TRF Threshold Voltage	16a	V_{TRF}	1.2	1.6	1.9	Vdc
TRF Threshold Hysteresis	16b	ΔV_{TRF}	100	200	400	mVdc
TRF Filter Resistance	17	R_{TRF}	30	50	75	kΩ
High Tone Frequency	18	f_H	920	1000	1080	Hz
Low Tone Frequency	18	f_L	736	800	864	Hz
Warble Frequency	18	f_W	11.5	12.5	13.5	Hz
Tone Ringer Output Voltage	19	$V_{o(p-p)}$	18	20	22	Vp-p

FIGURE 11 — GENERAL TEST CIRCUIT



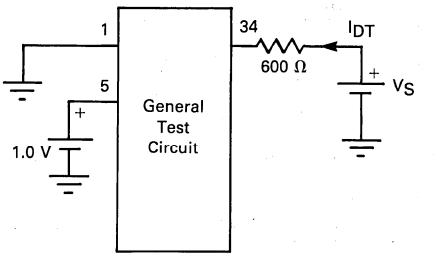
Notes:
1. *Selected ceramic resonator: 500 kHz ±2.0 kHz.
2. Capacitances in μF unless noted.
3. All resistances in ohms.
4. Pin outs shown are for the 40 pin DIP.

FIGURE 12 — TEST ONE



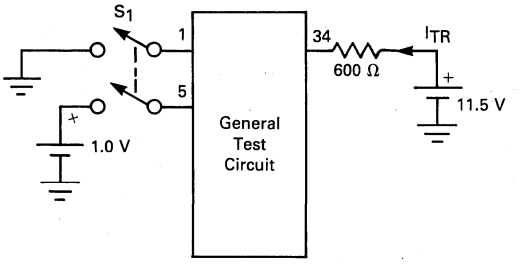
a. Measure V_R with V_S = 1.7 V
b. Measure I_{SP} with V_S = 1.7 V
c. Measure I_{SP} with V_S = 5.0 V

FIGURE 13 — TEST TWO



a. Measure I_{DT} with V_S = 11.5 V
b. Measure I_{DT} with V_S = 26 V. Calculate
$\Delta I_{DT} = I_{DT}\Big|_{26\ V} - I_{DT}\Big|_{11.5\ V}$

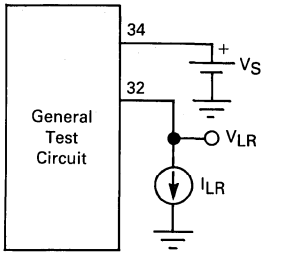
FIGURE 14 — TEST THREE



With S_1 open measure I_{TR}. Close S_1 and again measure I_{TR}. Calculate:

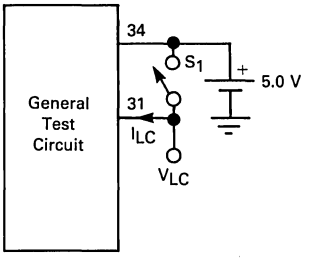
$\Delta I_{TR} = I_{TR}\Big|_{S_1\ Closed} - I_{TR}\Big|_{S_1\ Open}$

FIGURE 15 — TEST FOUR



a. Set V_S = 5.0 V and I_{LR} = 10 mA. Measure V_{LR}. Calculate $\Delta V_{LR} = V_S - V_{LR}$
b. Repeat Test 4a with V_S = 18 V and I_{LR} = 110 mA

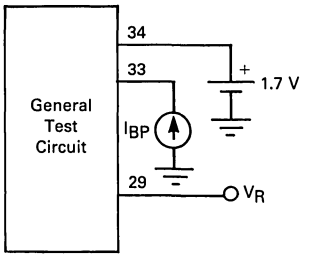
FIGURE 16 — TEST FIVE



With S_1 open measure V_{LC}.
Close S_1 and measure I_{LC}.
Calculate:

$$R_{LC} = \frac{5.0 - V_{LC}}{I_{LC}}$$

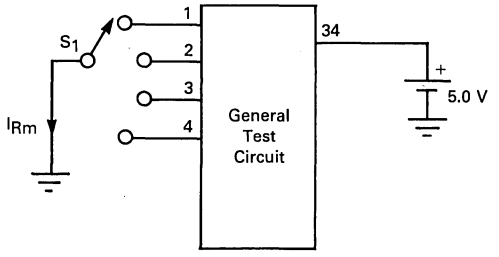
FIGURE 17 — TEST SIX



Set I_{BP} = 0.0 μA and measure V_R.
Set I_{BP} = 150 μA and measure V_R. Calculate:

$$\Delta V_R = V_R\Big|_{0.0\ \mu A} - V_R\Big|_{150\ \mu A}$$

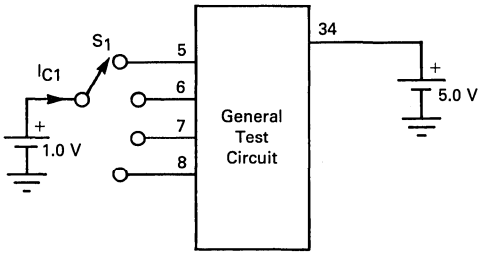
FIGURE 18 — TEST SEVEN



Subscript m corresponds to row number.

a. Set S_1 to Terminal 2 and measure voltage at Terminal 1 (V_{ROC}).
b. Set S_1 to Terminal 1 (m = 1) and measure I_{R1}. Calculate:
$R_{R1} = V_{ROC} \div I_{R1}$
c,d,e. Repeat Test 7b for m = 2,3,4.

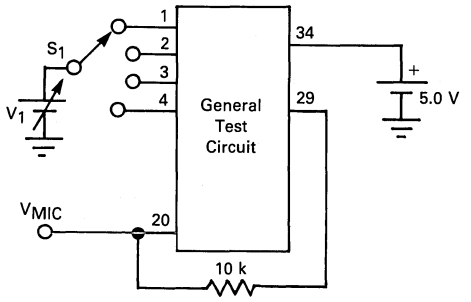
FIGURE 19 — TEST EIGHT



Subscript n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) and measure I_{C1}. Calculate:
$R_{C1} = 1.0\ V \div I_{C1}$
b,c,d. Repeat Test 8a for n = 2,3,4.

FIGURE 20 — TEST NINE

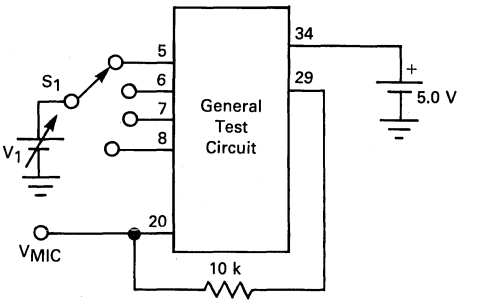


m corresponds to row number.

a. Set S_1 to Terminal 1 (m = 1) with V_1 = 1.0 Vdc. Verify V_{MIC} is Low (V_{MIC} < 0.3 Vdc). Decrease V_1 to 0.70 V_{ROC} and verify V_{MIC} switches high. (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 9a for rows 2,3, and 4. (m = 2,3,4)

FIGURE 21 — TEST TEN

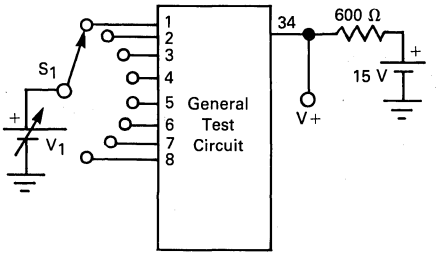


n corresponds to column number.

a. Set S_1 to Terminal 5 (n = 1) with V_1 = 0 Vdc. Verify V_{MIC} is low (V_{MIC} < 0.3 Vdc). Increase V_1 to 0.39 V_{ROC} and verify V_{MIC} switches high, (V_{MIC} > 0.5 Vdc). V_{ROC} is obtained from Test 7a.

b,c,d. Repeat Test 10a for columns 2,3, and 4. (n = 2,3,4)

FIGURE 22 — TEST ELEVEN



m corresponds to row number.
n corresponds to column number.

a. With V_1 = 0.0 V set S_1 to Terminal 1 (m = 1) and measure frequency of tone at V+.

b. Repeat Test 11a for rows 2,3 and 4. (m = 2,3,4).

c. With V_1 = 1.0 V set S_1 to Terminal 5. (n = 1) and measure frequency of tone at V+.

d. Repeat Test for columns 2,3, and 4. (n = 2,3,4).

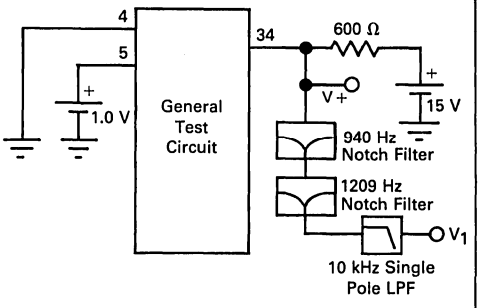
e. Set S_1 to Terminal 4 and V_1 = 0.0 V. Measure row tone amplitude at V+ (V_{ROW}).

f. Set S_1 to Terminal 8 and V_1 = 1.0 V. Measure column tone amplitude at V+. (V_{COL}).

g. Using results of Tests 11e and 11f, calculate:

$$dB_{CR} = 20 \log_{10} \frac{V_{COL}}{V_{ROW}}$$

FIGURE 23 — TEST TWELVE

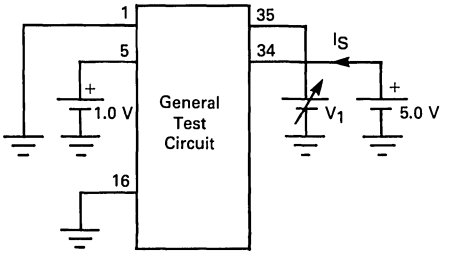


Note: The notch filters must have 50 dB attenuation at their respective center frequencies.

Measure V+ and V_1 with a true rms voltmeter. Calculate:

$$\% \text{ DIS} = \frac{V_1(\text{rms})}{V+(\text{rms})} \times 100$$

FIGURE 24 — TEST THIRTEEN

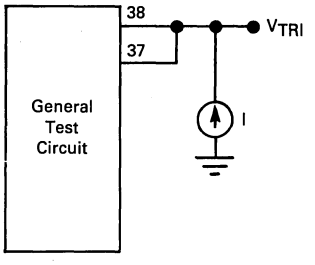


Measure I_S at V_1 = 1.8 V and V_1 = 2.8 V.

Calculate:

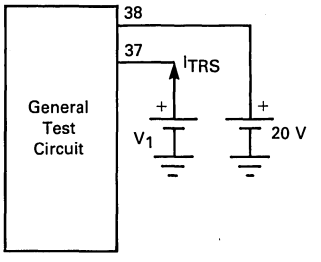
$$R_O = 1.0 \text{ V} \div \left[I_S \Big|_{2.8 \text{ V}} - I_S \Big|_{1.8 \text{ V}} \right]$$

FIGURE 25 — TEST FOURTEEN



Set I = 1.0 mA and measure V_{TRI}.

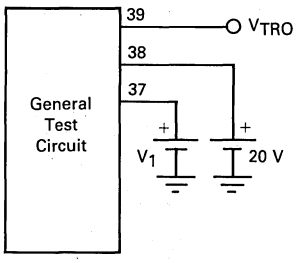
FIGURE 26 — TEST FIFTEEN



a. Measure I_{TRS} with V_1 = 24 V.

b. Measure I_{TRS} with V_1 = 30 V.

FIGURE 27 — TEST SIXTEEN



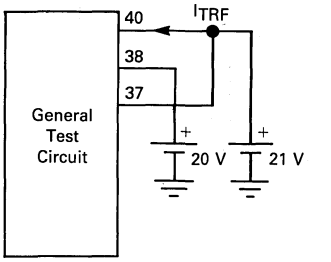
a. Increase V_1 from 21 V until V_{TRO} switches on. Note that V_{TRO} will be an 16 V_{pp} square wave. Record this value of V_1. Calculate:

$V_{TRF} = V_1 - 20$ V

b. Decrease V_1 from its setting in Test 16a until V_{TRO} ceases switching. Record this value of V_1. Calculate:

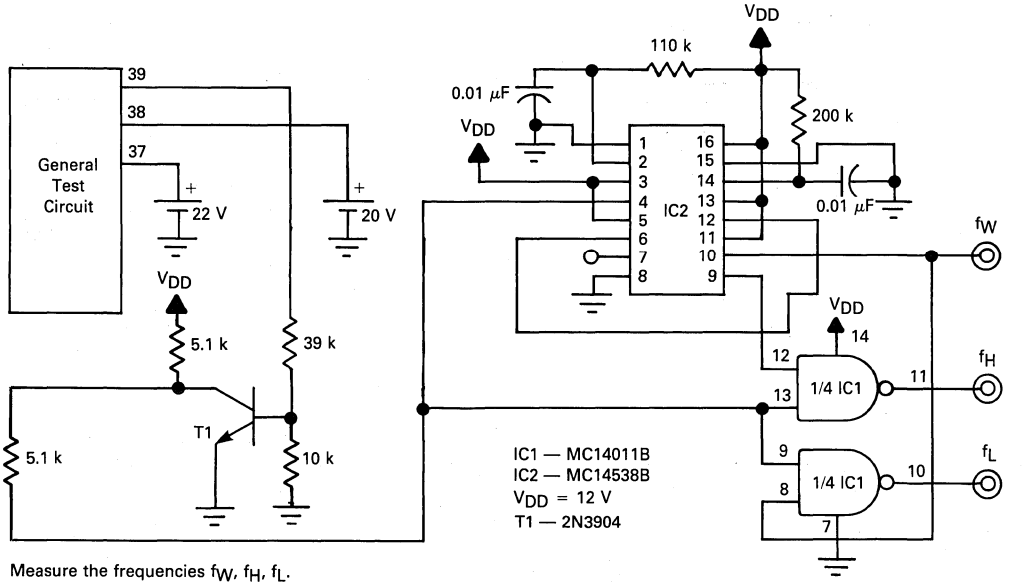
$$\Delta V_{TRF} = V_1\Big|_{\substack{\text{Test}\\16a}} - V_1\Big|_{\substack{\text{Test}\\16b}}$$

FIGURE 28 — TEST SEVENTEEN



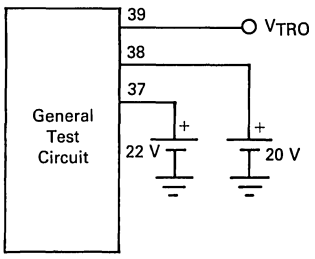
Measure I_{TRF}. Calculate: $R_{TRF} = 1.0 \div I_{TRF}$.

FIGURE 29 — TEST EIGHTEEN



Measure the frequencies f_W, f_H, f_L.

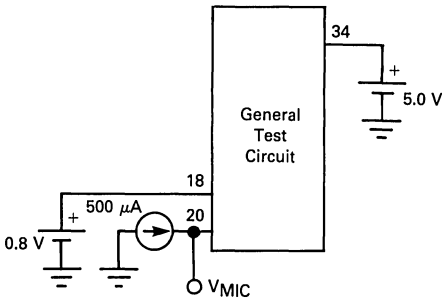
FIGURE 30 — TEST NINETEEN



Measure V_{TRO} peak-to-peak voltage swing.
Using V_{TRI} from Test 14 Calculate:

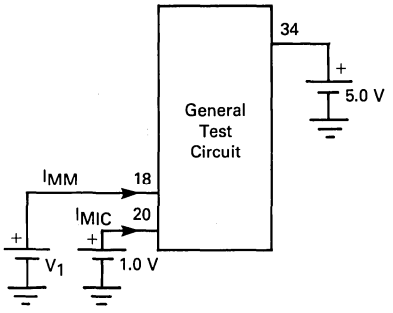
$V_{o(p-p)} = V_{TRI} - 20\ V + V_{TRO}$

FIGURE 31 — TEST TWENTY



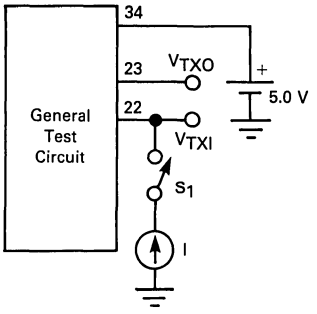
Measure V_{MIC}

FIGURE 32 — TEST TWENTY-ONE



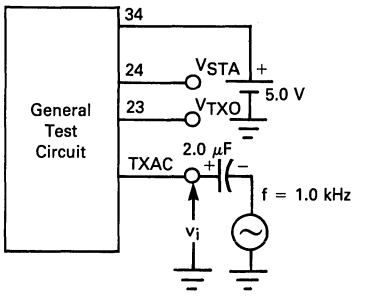
a. Set V_1 = 2.0 V and measure I_{MIC}.
b. Set V_1 = 5.0 V and measure I_{MM}.
Calculate: $R_{MM} = 5.0\ V \div I_{MM}$

FIGURE 33 — TEST TWENTY-TWO



a. With S_1 open, measure V_{TXO}. Using V_R obtained in Test 1 Calculate: $B_{TXO} = V_{TXO} \div V_R$
b. With S_1 open, measure V_{TXO} and V_{TXI}. Calculate: $I_{TXI} = (V_{TXO} - V_{TXI}) \div 200\ k\Omega$
c. Close S_1 and set I = −10 μA. Measure V_{TXO}. Calculate: $V_{TXO}(+) = V_R - V_{TXO}$ where V_R is obtained from Test 1.
d. Close S_1 and set I = +10 μA. Measure V_{TXO}. $V_{TXO}(-) = V_{TXO}$.

FIGURE 34 — TEST TWENTY-THREE



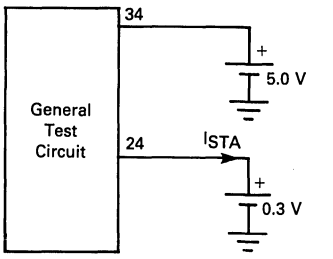
a. Set the generator for v_i = 3.0 mV_{rms}. Measure ac voltage V_{TXO}. Calculate:

$$G_{TX} = \frac{V_{TXO}}{v_i}$$

b. Measure ac voltage V_{STA}. Using V_{TXO} from Test 23a calculate:

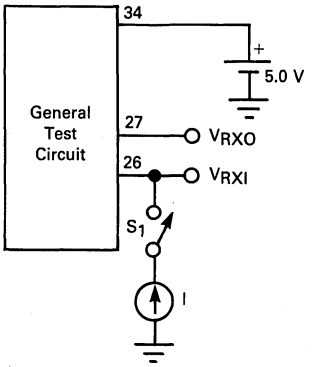
$$G_{STA} = \frac{V_{STA}}{V_{TXO}}$$

FIGURE 35 — TEST TWENTY-FOUR



Measure I_{STA}.

FIGURE 36 — TEST TWENTY-FIVE



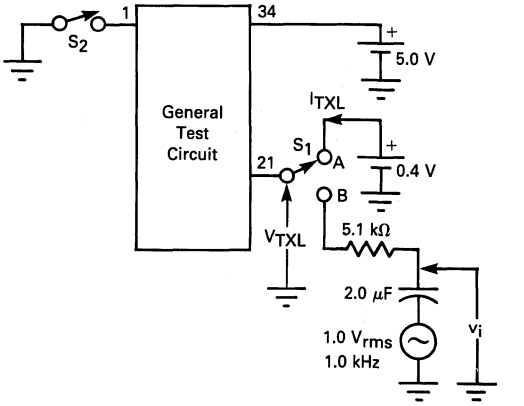
a. With S_1 open, measure V_{RXO}. Using V_R obtained in Test 1, calculate: $B_{RXO} = V_{RXO} \div V_R$.

b. With S_1 open, measure V_{RXO} and V_{RXI}. Calculate: $I_{RXI} = (V_{RXO} - V_{RX1}) \div 100\ k\Omega$

c. Close S_1 and set I = −10 μA. Measure V_{RXO}. Using V_R obtained in Test 1, calculate: $V_{RXO}(+) = V_R - V_{RXO}$.

d. Close S_1 and set I = +10 μA and measure V_{RXO}. $V_{RXO}(-) = V_{RXO}$.

FIGURE 37 — TEST TWENTY-SIX

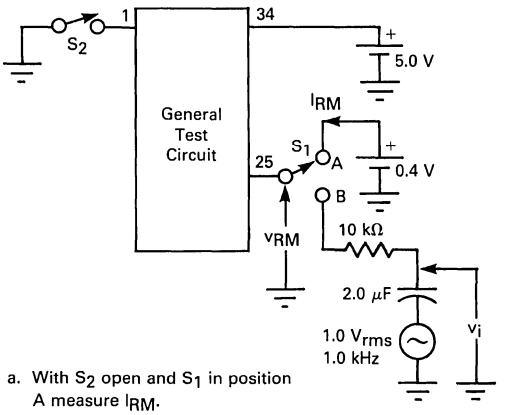


a. Set S_1 to position A with S_2 open. Measure I_{TXL}. Calculate: R_{TXL} (OFF) = 0.4 V ÷ I_{TXL}.

b. Set S_1 to position B and close S_2. Measure ac voltages v_i and V_{TXL}. Calculate:

$$R_{TXL}\ (ON) = \frac{V_{TXL}}{v_i - V_{TXL}} \times 5.1\ k\Omega$$

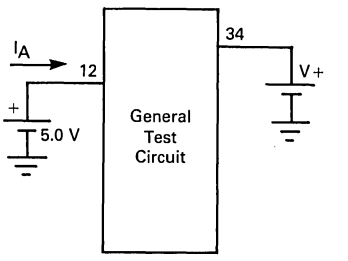
FIGURE 38 — TEST TWENTY-SEVEN



a. With S_2 open and S_1 in position A measure I_{RM}.
Calculate: $R_{RM(OFF)} = 0.4\ V \div I_{RM}$

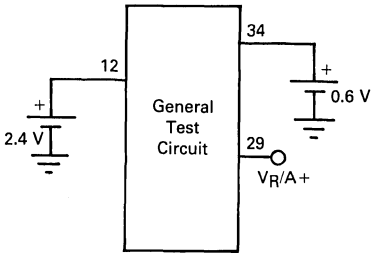
b. Close S_2 and switch S_1 to position B. Measure ac voltages v_i and V_{RM}.
Calculate:
$$R_{RM(ON)} = \frac{V_{RM}}{v_i - V_{RM}} \times 10\ k\Omega$$

FIGURE 39 — TEST TWENTY-EIGHT



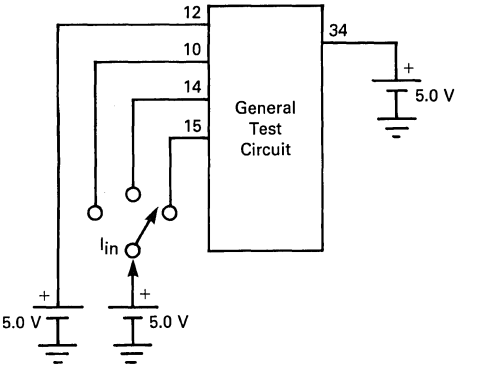
a. Set V+ = 1.4 V. Measure $I_{A(OFF)}$
b. Set V+ = 0.6 V. Measure $I_{A(ON)}$

FIGURE 40 — TEST TWENTY-NINE



Measure $V_R/A+$

FIGURE 41 — TEST THIRTY



Measure I_{in} at each of three inputs. For each, calculate:
$R_{in} = 5.0\ V/I_{in}$

FIGURE 42 — TEST THIRTY-ONE

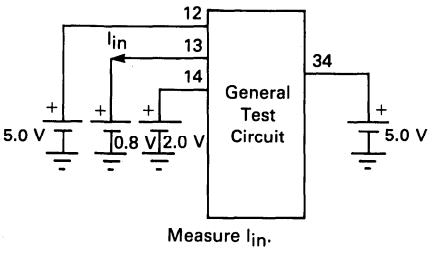
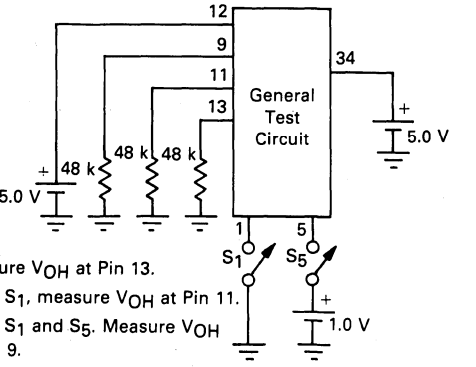
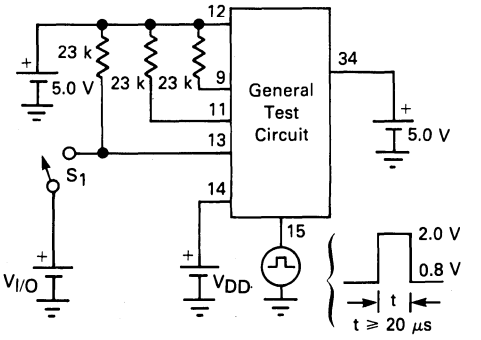


FIGURE 43 — TEST THIRTY-TWO



a. Measure V_{OH} at Pin 13.
b. Close S_1, measure V_{OH} at Pin 11.
c. Close S_1 and S_5. Measure V_{OH} at Pin 9.

FIGURE 44 — TEST THIRTY-THREE



a. Set V_{DD} to 0.8 V Measure V_{OL} voltages at Pins 9 and 11.
b. Close S_1. Force $V_{I/O}$ to 0.8 V and V_{DD} to 2.0 V. Apply 4 clock pulses to Pin 15. Open S_1 and decrease V_{DD} to 0.8 V. Measure V_{OL} at Pin 13.

APPLICATIONS INFORMATION

Figure 45 specifies a typical application circuit for the MC34010. Complete listings of external components are provided at the end of this section along with nominal component values.

The hook switch and polarity guard bridge configuration in Figure 45 is one of several options. If two bridges are used, one for the tone ringer and the other for speech and dialer circuits, then the hook switch can be simplified. Component values should be varied to optimize telephone performance parameters for each application. The relationships between the application circuit components and certain telephone parameters are briefly described in the following:

On-Hook Input Impedance

R1, C17, and Z3 are the significant components for on-hook impedance. C17 dominates at low frequencies, R1 at high frequencies and Z3 provides the non-linearity required for 2.5 V and 10 V impedance signature tests. C17 must generally be ≤ 1.0 μF to satisfy 5.0 Hz impedance specifications.

Tone Ringer Output Frequencies

R3 and C13 control the frequency (f_o) of a relaxation oscillator. Typically $f_o = (R3C13 + 8.0\ \mu s)^{-1}$. The output tone frequencies are $f_o/10$ and $f_o/8$. The warble rate is $f_o/640$. The tone ringer will operate with f_o from 1.0 kHz to 10 kHz. R3 should be limited to values between 150 k and 300 k.

Tone Ringer Input Threshold

After R1, C17, and Z3 are chosen to satisfy on-hook impedance specifications, R2 is chosen for the desired ring start threshold. Increasing R2 reduces the ac input voltage required to activate the tone ringer output. R2 should be limited to values between 0.8 k and 2.0 kΩ.

Off-Hook DC Resistance

R4 conducts the dc line current in excess of the speech and dialer bias current. Increasing R4 increases the input resistance of the telephone for line currents above 10 mA. R4 should be selected between 30 Ω and 120 Ω.

Off-Hook AC Impedance

The ac input impedance is equal to the receive amplifier load impedance (at RXO) divided by the receive amplifier gain (voltage gain from V+ to RXO). Increasing the impedance of the receiver increases the impedance of the telephone. Increasing the gain of the receiver amplifier decreases the impedance of the telephone.

DTMF Output Amplitude

R14 controls the amplitude of the row and column DTMF tones. Decreasing R14 increases the level of tones generated at V+. The ratio of the row and column tone amplitudes is internally fixed. R14 should be greater than 20 Ω to avoid excessive current in the DTMF output amplifier.

Transmit Output Level

R10 controls the maximum signal amplitude produced at V+ by the transmit amplifier. Decreasing R10 increases the transmit output signal at V+. R10 should be greater than 220 Ω to limit current in the transmit amplifier output.

Transmit Gain

The gain from the microphone to the telephone line varies directly with R11. Increasing R11 increases the signal applied to R10 and the ac current driven through R10 to the telephone line. The closed loop-gain from the microphone to the TXO terminal should be greater than 10 to prevent transmit amplifier oscillations.

Note: Adjustments to transmit level and gain are complicated by the addition of receiver sidetone current to the transmit amplifier output current at V+. Normally the sidetone current from the receiver will increase the transmit signal (if the current in the receiver is in phase with that in R10). Thus the transmit gain and sidetone levels cannot be adjusted independently.

Receiver Gain

Feedback resistor R6 adjusts the gain at the receiver amplifier. Increasing R6 increases the receiver amplifier gain.

Sidetone Level

Sidetone reduction is achieved by the cancellation of receiver amplifier input signals from R9 and R5. R8, R15, and C6 determine the phase of the sidetone balance signal in R9. The ac voltage at the junction of R8 and R9 should be 180° out of phase with the voltage at V+. R9 is selected such that the signal current in R9 is slightly greater than that in R5. This insures that the sidetone current in the receiver adds to the transmit amplifier output current.

Hook-Switch Click Suppression

When the telephone is switched to the off-hook condition C3 charges from 0 volts to a 300 mV bias voltage. During this time interval, receiver clicks are suppressed by a low impedance at the RM terminal. If this click suppression mechanism is desired during a rapid succession of hook switch transitions, then C3 must be quickly discharged when the telephone is on-hook, R16 and S3 provide a rapid discharge path for C3 to reset the click suppression timer. R16 is selected to limit the discharge current in S3 to prevent damage to switch contacts.

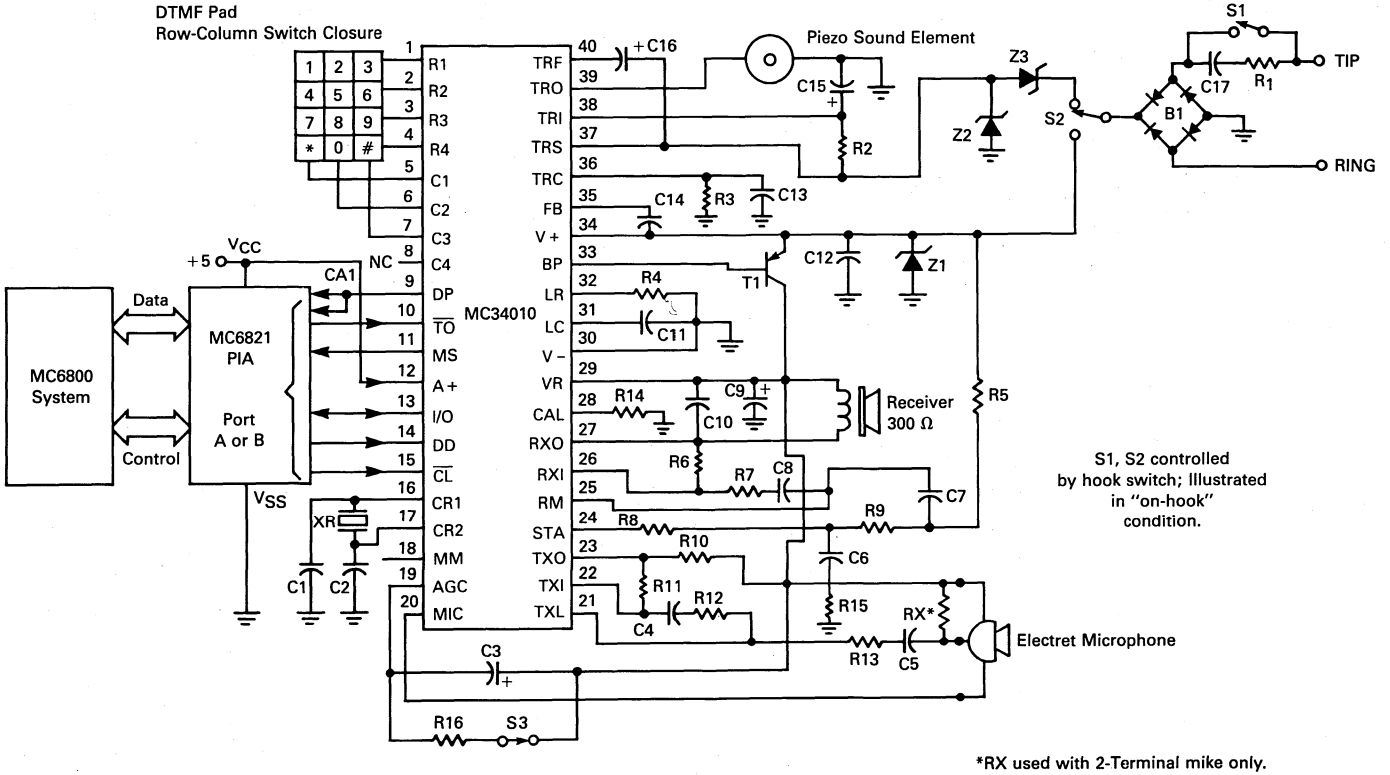
Microprocessor Interface

The six microprocessor interface lines (DP, $\overline{TO}$, MS, DD, I/O, and $\overline{CL}$) can be connected directly to a port, as shown in Figure 47. The DP line (Depressed Pushbutton) is also connected to an interrupt line to signal the microprocessor to begin a read data sequence when storing a number into memory. The MC34010A clock speed requirement is slow enough (typically 20 kHz) so that it is not necessary to divide down the processor's system clock, but rather a port output can be toggled. This facilitates synchronizing the clock and data transfer, eliminating the need for hardware to generate the clock.

The DD pin must be maintained at a Logic "0" when the microprocessor section is not in use, so as to permit normal operation of the keypad.

When the microprocessor interface section is not in use, the supply voltage at Pin 12 (A+) may be disconnected to conserve power. Normally the speech circuitry is powered by the voltage supplied at the V+ terminal (Pin 34) from the telephone lines. During this time, A+ powers only the active pullups on the three microprocessor outputs (DP, MS, and I/O). When the telephone is "on-hook," and V+ falls below 0.6 volts, power is then supplied to the telephone speech and dialer circuitry from A+. Powering the circuit from the A+ pin permits communication with a microprocessor, and/or use of the transmit and receiver amplifiers, while the telephone is "on-hook."

FIGURE 45 — ELECTRONIC TELEPHONE APPLICATION CIRCUIT



EXTERNAL COMPONENTS

(Component Labels Referenced to Figure 45)

Capacitors	Nominal Value	Description
C1, C2	100 pF	Ceramic Resonator oscillator capacitors.
C3	1.0 μF, 3.0 V	Transmit limiter low-pass filter capacitor: controls attack and decay time of transmit peak limiter.
C4, C5	0.1 μF	Transmit amplifier input capacitors: prevent dc current flow into TXL pin and attenuate low-frequency noise on microphone lead.
C6	0.05 μF	Sidetone network capacitor: provides phase-shift in sidetone path to match that caused by telephone line reactance.
C7, C8	0.05 μF	Receiver amplifier input capacitors: prevent dc current flow into RM terminal and attenuates low frequency noise on the telephone line.
C9	2.2 μF, 3.0 V	VR regulator capacitor: frequency compensates the VR regulator to prevent oscillation.
C10	0.01 μF	Receiver amplifier output capacitor: frequency compensates the receiver amplifier to prevent oscillation.
C11	0.1 μF	DC load filter capacitor: prevents the dc load circuit from attenuating ac signals on V+.
C12	0.01 μF	Telephone line bypass capacitor: terminates telephone line for high frequency signals and prevents oscillation in the VR regulator.
C13	620 pF	Tone ringer oscillator capacitor: determines clock frequency for tone and warble frequency synthesizers.
C14	0.1 μF	DTMF output feedback capacitor: ac couples feedback around the DTMF output amplifier which reduces output impedance.
C15	4.7 μF, 25 V	Tone ringer input capacitor: filters the rectified tone ringer input signal to smooth the supply potential for oscillator and output buffer.
C16	1.0 μF, 10 V	Tone ringer filter capacitor: integrates the voltage from current sense resistor R2 at the input of the threshold detector.
C17	1.0 μF, 250 Vac Non-polarized	Tone ringer line capacitor: ac couples the tone ringer to the telephone line; partially controls the on-hook input impedance of telephone.

Resistors	Nominal Value	Description
R1	6.8 k	Tone ringer input resistor: limits current into the tone ringer from transients on the telephone line and partially controls the on-hook impedance of the telephone.
R2	1.8 k	Tone ringer current sense resistor: produces a voltage at the input of the threshold detector in proportion to the tone ringer input current.
R3	200 k	Tone ringer oscillator resistor: determines the clock frequency for tone and warble frequency synthesizers.
R4	82, 1.0 W	DC load resistor: conducts all dc line current in excess of the current required for speech or dialing circuits; controls the off-hook dc resistance of the telephone.
R5, R7	150 k, 56 k	Receiver amplifier input resistors: couple ac input signals from the telephone line to the receiver amplifier; signal in R5 subtracts from that in R9 to reduce sidetone in receiver.
R6	200 k	Receiver amplifier feedback resistor: controls the gain of the receiver amplifier.
R8, R9	1.5 k, 30 k	Sidetone network resistors: drive receiver amplifier input with the inverted output signal from the transmitter; phase of signal in R9 should be opposite that in R5.
R10	270	Transmit amplifier load resistor: converts output voltage of transmit amplifier into a current that drives the telephone line; controls the maximum transmit level.
R11	200 k	Transmit amplifier feedback resistor: controls the gain of the transmit amplifier.
R12, R13	4.7 k, 4.7 k	Transmit amplifier input resistors: couple signal from microphone to transmit amplifier; control the dynamic range of the transmit peak limiter.
R14	36	DTMF calibration resistor: controls the output amplitude of the DTMF dialer.
R15	2.0 k	Sidetone network resistor (optional): reduces phase shift in sidetone network at high frequencies.
R16	100	Hook switch click suppression current limit resistor (optional): limits current when S3 discharges C3 after switching to the on-hook condition.
R_X	3.0 k	Microphone bias resistor: sources current from VR to power a 2-terminal electret microphone; R_X is not used with 3-terminal microphones.

EXTERNAL COMPONENTS (continued)

Semiconductors	Electret Mic	Receiver
B1 = MDA101A, or equivalent, or 4-1N4005 T1 = 2N4126 or equivalent Z1 = 18 V, 1.5 W, 1N5931A Z2 = 30 V, 1.5 W, 1N5936A Z3 = 4.7 V, 1/2 W, 1N750 XR — muRata Erie CSB 500 kHz Resonator, or equivalent Piezo — PBL 5030BC Toko Buzzer or equivalent	2 Terminal, Primo EM-95 (Use R_X) or equivalent 3 Terminal, Primo 07A181P (Remove R_X) or equivalent	Primo Model DH-34 (300 Ω) or equivalent

Motorola Inc. does not endorse or warrant the suppliers referenced.

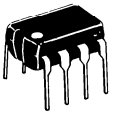
MC34012-1
MC34012-2
MC34012-3

TELEPHONE TONE RINGER

- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Base Frequency Options—MC34012-1: 1.0 kHz
  MC34012-2: 2.0 kHz
  MC34012-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

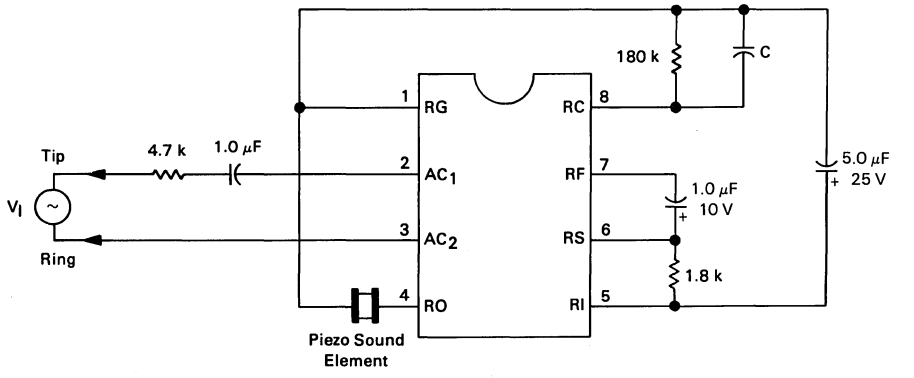
TELEPHONE TONE RINGER

BIPOLAR LINEAR/I^2L



PLASTIC PACKAGE
CASE 626

APPLICATION CIRCUIT



MC34012-1: C = 1000 pF
MC34012-2: C = 500 pF
MC34012-3: C = 2000 pF

APPLICATION CIRCUIT PERFORMANCE

Characteristic	Typical Value	Units
Output Tone Frequencies MC34012-1 MC34012-2 MC34012-3 Warble Frequency	 832/1040 1664/2080 416/520 13	 Hz
Output Voltage ($V_I \geq 60\ V_{rms}$, 20 Hz)	20	V_{p-p}
Output Duty Cycle	50	%
Ringing Start Input Voltage (20 Hz)	36	V_{rms}
Ringing Stop Input Voltage (20 Hz)	28	V_{rms}
Maximum ac Input Voltage ($\leq$ 68 Hz)	150	V_{rms}
Impedance When Ringing $V_I = 40\ V_{rms}$, 15 Hz $V_I = 130\ V_{rms}$, 23 Hz	 20 10	kΩ
Impedance When Not Ringing $V_I = 10\ V_{rms}$, 24 Hz $V_I = 2.5\ V_{rms}$, 24 Hz $V_I = 10\ V_{rms}$, 5.0 Hz $V_I = 3.0\ V_{rms}$, 200–3200 Hz	 28 >1.0 55 >1.0	 kΩ MΩ kΩ MΩ
Maximum Transient Input Voltage ($T \leq 2.0$ ms)	1500	V

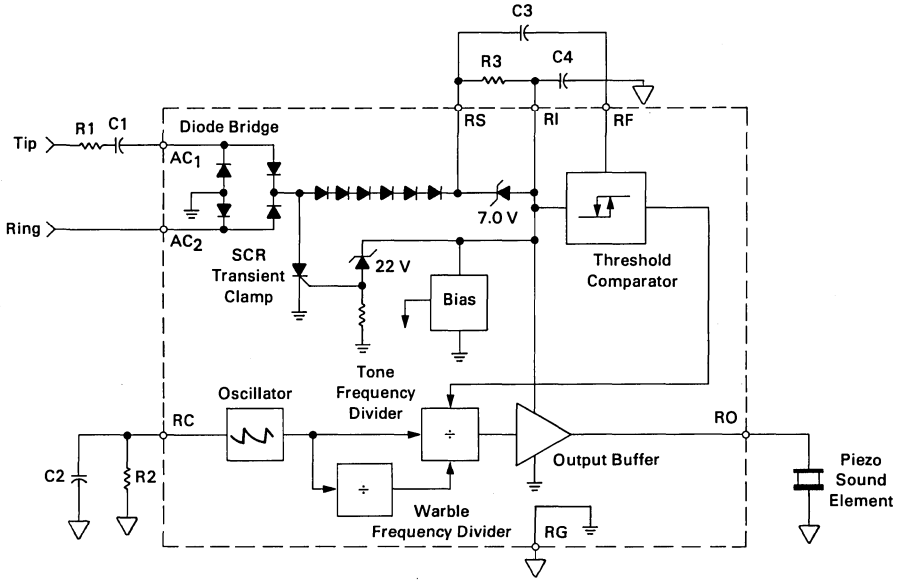
PIN DESCRIPTIONS

Name	Description
AC_1, AC_2	The input terminals to the full-wave diode bridge. The ac ringing signal from the telephone line energizes the ringer through this bridge.
RS	The positive output of diode bridge to which an external current sense resistor is connected.
RI	The positive supply terminal for the oscillator, frequency divider and output buffer circuits.
RF	The terminal for the filter capacitor used in detection of ringing input signals.
RO	The tone ringer output terminal through which the sound element is driven.
RG	The negative output of the diode bridge and the negative supply terminal of the tone generating circuitry.
RC	The oscillator terminal for the external resistor and capacitor which control the tone ringer frequencies.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Test	Symbol	Min	Typ	Max	Units
Ringing Start Voltage ($V_{Start} = V_I$ @ Ring Start)						Vdc
$V_I > 0$	1a	$V_{Start(+)}$	31	34.5	38	
$V_I < 0$	1b	$V_{Start(-)}$	-31	-34.5	-38	
Ringing Stop Voltage ($V_{Stop} = V_I$ @ Ring Stop)	1c	V_{Stop}				Vdc
MC34012-1			16	20	25	
MC34012-2			13	18	22	
MC34012-3			16	20	25	
Output Frequencies (V_I = 50 V)	1d					Hz
MC34012-1 High Tone		f_H	967	1040	1113	
Low Tone		f_L	774	832	890	
Warble Tone		f_W	12	13	14	
MC34012-2 High Tone		f_H	1934	2080	2226	
Low Tone		f_L	1548	1664	1780	
Warble Tone		f_W	12	13	14	
MC34012-3 High Tone		f_H	967	1040	1113	
Low Tone		f_L	774	832	890	
Warble Tone		f_W	24	26	28	
Output Voltage (V_I = 50 V)	6	V_O	19	20	23	V_{p-p}
Output Short-Circuit Current	2	I_O	35	50	80	mA_{p-p}
Input Diode Voltage (I_I = 1.0 mA)	3	V_D	4.6	5.1	5.6	Vdc
Input Voltage—SCR Off (I_I = 30 mA)	4a	V_{off}	37	42	47	Vdc
Input Voltage—SCR On (I_I = 100 mA)	4b	V_{on}	3.2	4.2	6.0	Vdc
Threshold Filter Resistance $R_{RF} = 2.0\ V/I_{RF}$	5	R_{RF}	30	50	80	kΩ

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The MC34012 Tone Ringer derives its power supply by rectifying the ac ringing signal. It uses this power to activate a tone generator and drive a piezo-ceramic transducer. The tone generation circuitry includes a relaxation oscillator and frequency dividers which produce high and low frequency tones as well as the tone warble frequency. The relaxation oscillator frequency f_o is set by resistor R2 and capacitor C2 connected to pin RC. The oscillator will operate with f_o from 1.0 kHz to 10 kHz with the proper choice of external components (See Figure 1).

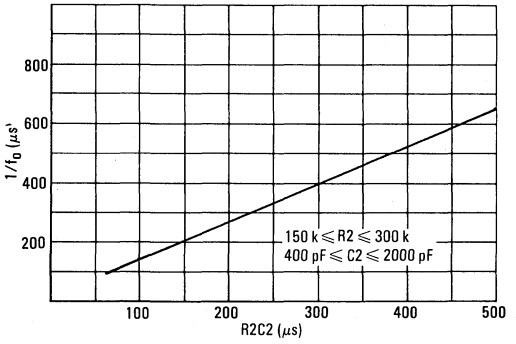
The frequency of the tone ringer output signal at pin RO alternates between $f_o/4$ to $f_o/5$. The warble rate at which the frequency changes is $f_o/320$ for the MC34012-1, $f_o/640$ for the MC34012-2, or $f_o/160$ for the MC34012-3. With a 4.0 kHz oscillator frequency, the MC34012-1 produces 800 Hz and 1000 Hz tones with a 12.5 Hz warble rate. The MC34012-2 generates 1600 Hz and 2000 Hz tones with a similar 12.5 Hz warble frequency from an 8.0 Hz oscillator frequency. The MC34012-3 will produce 400 Hz and 500 Hz tones with a 12.5 Hz warble rate from a 2.0 kHz oscillator frequency. The tone ringer output circuit can source or sink 20 mA with an output voltage swing of 20 volts peak-to-peak. Volume control is readily implemented by adding a variable resistance in series with the piezo transducer.

Input signal detection circuitry activates the tone ringer output when the ac line voltage exceeds programmed threshold level. Resistor R3 determines the ringing signal amplitude at which an output signal will be generated at RO. The ac ringing signal is rectified by the internal diode bridge. The rectified input signal produces a current through R3 which is input at terminal RI. The voltage across resistor R3 is filtered by capacitor C3 at the input to the threshold circuit. When the voltage on capacitor C3 exceeds 1.7 volts, the threshold comparator enables the tone ringer output. Line transients produced by pulse dialing telephones do not charge capacitor C3 sufficiently to activate the tone ringer output.

Capacitors C1 and C4 and resistor R1 determine the 10 volt, 24 Hz signature test impedance. C4 also provides filtering for the output stage power supply to prevent droop in the square wave output signal. Six diodes in series with the rectifying bridge provide the necessary non-linearity for the 2.5 volt, 24 Hz signature tests.

An internal shunt voltage regulator between the RI and RG terminals provides dc voltage to power output stage, oscillator, and frequency dividers. The dc voltage at RI is limited to approximately 22 volts in regulation. To protect the IC from telephone line transients, an SCR is triggered when the regulator current exceeds 50 mA. The SCR diverts current from the shunt regulator and reduces the power dissipation within the IC.

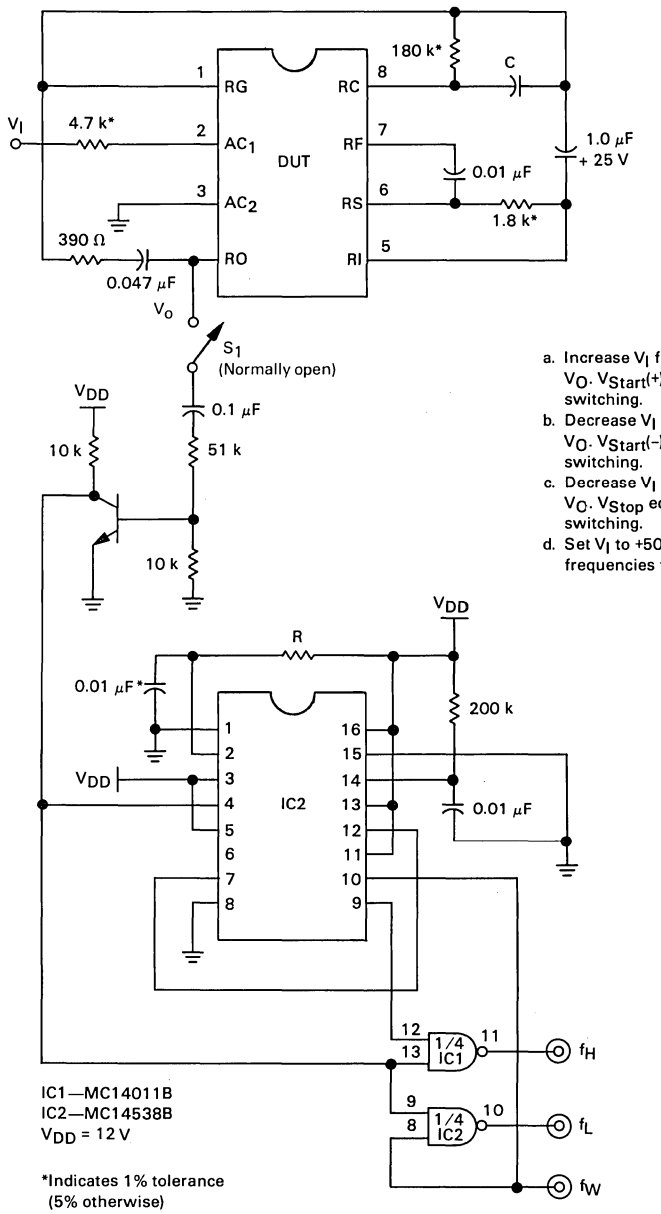
FIGURE 1 — OSCILLATOR PERIOD ($1/f_o$) versus OSCILLATOR R2 C2 PRODUCT



EXTERNAL COMPONENTS

R1	Line input resistor. R1 controls the tone ringer input impedance. It also influences ringing threshold voltage and limits current from line transients. (Range: 2.0 kΩ to 10 kΩ).
C1	Line input capacitor. C1 ac couples the tone ringer to the telephone line and controls ringer input impedance at low frequencies. (Range: 0.4 μF to 2.0 μF).
R2	Oscillator resistor. (Range: 150 kΩ to 300 kΩ).
C2	Oscillator capacitor. (Range: 400 pF to 2000 pF).
R3	Input current sense resistor. R3 controls the ringing threshold voltage. Increasing R3 decreases the ring-start voltage. (Range: 0.8 kΩ to 2.0 kΩ).
C3	Ringing threshold filter capacitor. C3 filters the ac voltage across R3 at the input of the ringing threshold comparator. It also provides dialer transient rejection. (Range: 0.5 μF to 5.0 μF).
C4	Ringer supply capacitor. C4 filters supply voltage for the tone generating circuits. It also provides an ac current path for the 10 V_{rms} ringer signature impedance. (Range: 1.0 μF to 10 μF).

FIGURE 2 — TEST ONE



MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

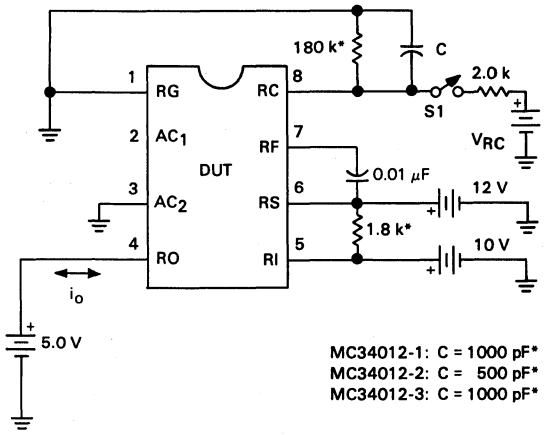
a. Increase V_I from +30 volts while monitoring V_O. $V_{Start}(+)$ equals V_I when V_O commences switching.
b. Decrease V_I from –30 volts while monitoring V_O. $V_{Start}(-)$ equals V_I when V_O commences switching.
c. Decrease V_I from +40 volts while monitoring V_O. V_{Stop} equals V_I when V_O ceases switching.
d. Set V_I to +50 volts. Close S1. Measure frequencies f_H, f_L, and f_W.

IC1—MC14011B
IC2—MC14538B
V_{DD} = 12 V

*Indicates 1% tolerance
(5% otherwise)

MC34012-1: R = 110 kΩ*
MC34012-2: R = 55 kΩ*
MC34012-3: R = 110 kΩ*

FIGURE 3 — TEST TWO



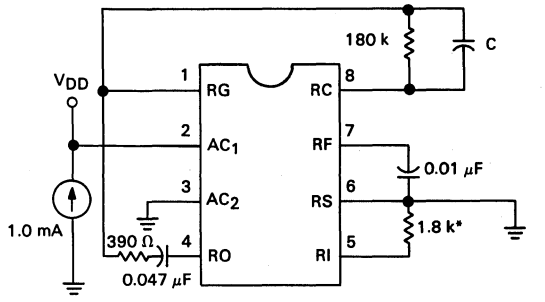
MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

With V_{RC} = 3.5 volts, close S1. Measure the current at Pin 4 (I_{O1}). Repeatedly switch V_{RC} between 3.5 volts and 0 volts until Pin 4 current changes polarity. Measure this opposite polarity current (I_{O2}).
Calculate:

$I_O = |I_{O1}| + |I_{O2}|$

*Indicates 1% tolerance (5% otherwise)

FIGURE 4 — TEST THREE

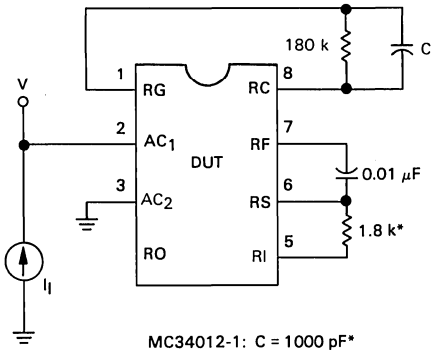


MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

Measure voltage at Pin 2.

*Indicates 1% tolerance (5% otherwise)

FIGURE 5 — TEST FOUR

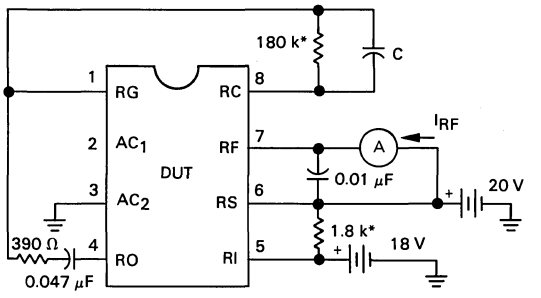


MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

a. Set I_I to 30 mA. Measure voltage at Pin 2 (V_{off}).
b. Set I_I to 100 mA. Measure voltage at Pin 2 (V_{on}).

*Indicates 1% tolerance (5% otherwise)

FIGURE 6 — TEST FIVE



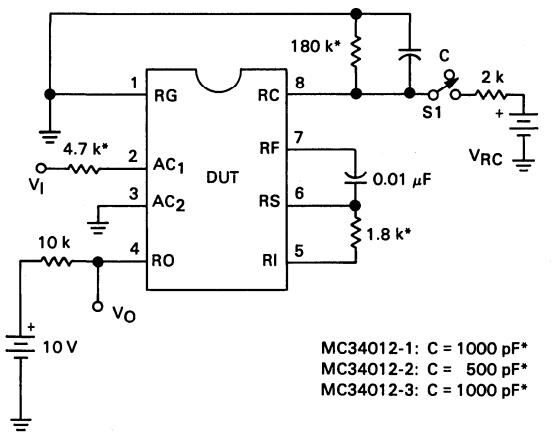
MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

Measure current into Pin 7 (I_{RF}). Calculate:

R_{RF} = 2 volts ÷ I_{RF}

*Indicates 1% tolerance (5% otherwise)

FIGURE 7 — TEST SIX



MC34012-1: C = 1000 pF*
MC34012-2: C = 500 pF*
MC34012-3: C = 1000 pF*

With V_{RC} = 3.5 volts, close S1. Set V_I to 50 volts. Measure dc voltage at Pin 4 (V_{O1}). Repeatedly change V_{RC} between 3.5 volts and 0 volts until Pin 4 changes state. Measure the new voltage at Pin 4 (V_{O2}).
Calculate the peak-to-peak output voltage:

$$V_{Op\text{-}p} = | V_{O2} - V_{O1} |$$

*Indicates 1% tolerance (5% otherwise)

MC34014

Specifications and Applications Information

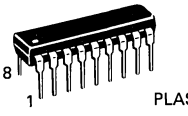
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

The MC34014 is a Telephone Speech Network integrated circuit which incorporates adjustable transmit, receive, and sidetone functions, a dc loop interface circuit, tone dialer interface, and a regulated output voltage for a pulse/tone dialer. Also included is an equalization circuit which compensates gains for line length variations. The conversion from 2-to-4 wire is accomplished with a supply voltage as low as 1.5 volts. The MC34014 is packaged in a standard 18-pin (0.3" wide) plastic DIP and a 20-pin SOIC package.

- Transmit, Receive, and Sidetone Gains Set by External Resistors
- Loop Length Equalization for Transmit, Receive, and Sidetone Functions
- Operates Down to 1.5 volts (V+) in Speech Mode
- Provides Regulated Voltage for CMOS Dialer
- Speech Amplifiers Muted During Pulse and Tone Dialing
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Compatible with Receiver Impedances of 150 Ω and Higher

TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

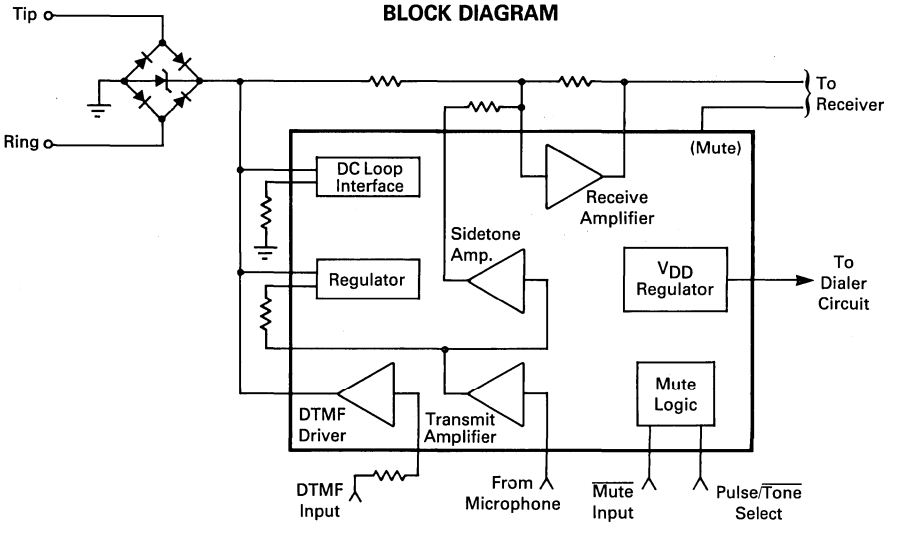
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 707

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
SO-20L

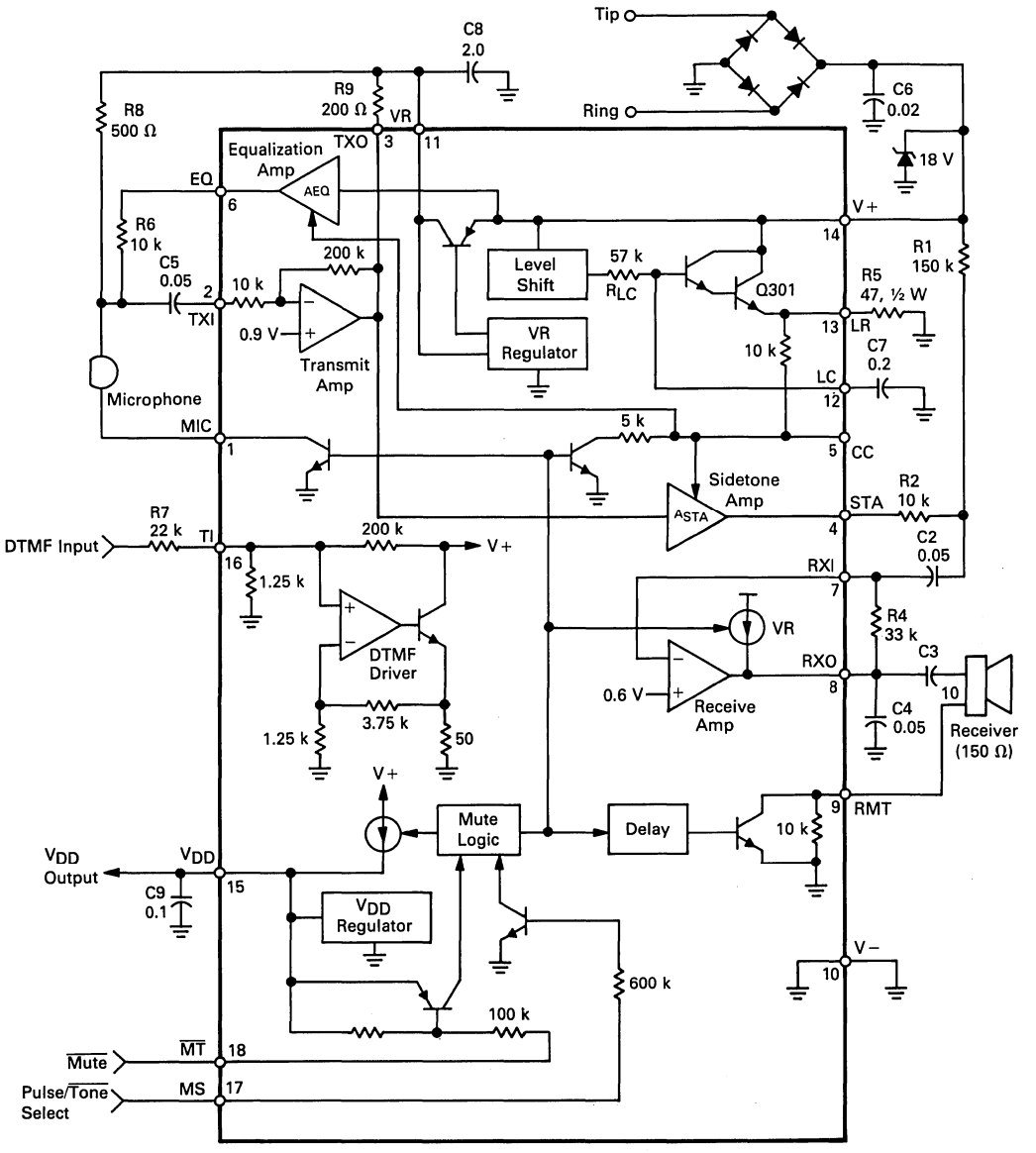
BLOCK DIAGRAM



PIN DESCRIPTION (See Figure 1)

Pin # SOIC	Pin # DIP	Name	Description
1	1	MIC	Microphone negative supply. Bias current from the electret microphone is returned to V− through this pin, through an open collector NPN transistor whose base is controlled by an internal mute signal. During dialing, the transistor is off, disabling the microphone.
2	2	TXI	Transmit amplifier input. Input impedance is 10 kΩ. Signals from the microphone are input through capacitor C5 to TXI.
3	3	TXO	Transmit amplifier output. The ac signal current from this output flows through the V_R series pass transistor via R9 to drive the line at V+. Increasing R9 will decrease the signal at V+. The output is biased at ≈0.65 V to allow for maximum swing of ac signals. The closed loop gain from TXI to TXO is internally set at 26 dB.
4	4	STA	Sidetone amplifier output. Input to this amplifier is TXO. The signal at STA cancels the sidetone signals in the receive amplifier. The signal level at STA increases with loop length.
5	5	CC	Compensation Capacitor. A capacitor from CC to ground will compensate the loop length equalization circuit when additional stability is required. In most applications, CC remains open.
7	6	EQ	Equalization amplifier output. A portion of the V+ signal is present on this pin to provide negative feedback around the transmit amplifier. The feedback decreases with increasing loop length, causing the ac impedance of the circuit to increase.
8	7	RXI	Receive amplifier input. Input impedance is >100 kΩ. Signals from the line and sidetone amplifier are summed at RXI.
9	8	RXO	Receive Amplifier output. RXO is biased by a 2.5 mA current source. Feedback maintains the dc bias voltage at ≈0.65 V. Increasing R4 (between RXO and RXI) will increase the receive gain. C4 stabilizes the amplifier. C3 couples the signals to the receiver. The 2.5 mA current source is reduced to 0.4 mA when dialing.
10	9	RMT	Receiver Mute. The ac receiver current is returned to V− through an open collector NPN transistor and a parallel 10 kΩ resistor. The base of the NPN is controlled by an internal mute signal. During dialing the transistor is off, leaving the 10 kΩ resistor in series with the receiver.
11	10	V−	Negative supply. The most negative input connected to Tip and Ring through the polarity guard diode bridge.
12	11	VR	Regulated voltage output. The VR voltage is regulated at 1.2 V and biases the microphone and the speech circuits. An internal series pass PNP transistor allows for regulation with a line voltage as low as 1.5 V. Capacitor C8 stabilizes the regulator.
13	12	LC	DC load capacitor. An external capacitor C7 and an internal resistor form a low pass filter between V+ and LR to prevent ac signals from being loaded by the dc load resistor R5. Forcing LC to V− will turn off the dc load current and increase the V+ voltage.
14	13	LR	DC load resistor. Resistor R5 from LR to V− determines the dc resistance of the telephone, and removes power dissipation from the chip. The LR pin is biased 2.8 volts below the V+ voltage (4.5 volts in the tone dialing mode).
15	14	V+	Positive supply. V+ is the positive line voltage (from Tip & Ring) through the polarity guard bridge. All sections of the MC34014 are powered by V+.
17	15	V_{DD}	V_{DD} regulator. V_{DD} is the output of a shunt type regulator with a nominal voltage of 3.3 V. The nominal output current is increased from 550 μA to 2 mA when dialing. Capacitor C9 stabilizes the regulator and sustains the V_{DD} voltage during pulse dialing.
18	16	TI	Tone input. The DTMF signal from a dialer circuit is input at TI through an external resistor R7. The current at TI is amplified to drive the line at V+. Increasing R7 will reduce the DTMF output levels. The input impedance at TI is nominally 1.25 kΩ.
19	17	MS	Mode select. This pin is connected through an internal 600 kΩ resistor to the base of an NPN transistor. A Logic "1" (>2.0 V) selects the pulse dialing mode. A Logic "0" (<0.3 V) selects the tone dialing mode.
20	8	$\overline{MT}$	Mute input. $\overline{MT}$ is connected through an internal 100 kΩ resistor to the base of a PNP transistor, with the emitter at V_{DD}. A Logic "0" (<1.0 V) will mute the network for either pulse or tone dialing. A Logic "1" (>V_{DD} − 0.3 V) puts the MC34014 into the speech mode.

FIGURE 1 — TEST CIRCUIT



NOTE: Pin numbers are for 18 pin DIP.

ABSOLUTE MAXIMUM RATINGS (Voltages referred to V−, T_A = 25°C) (See Note 1.)

Parameter	Value	Units
V+ Voltage	−1.0, +18	Vdc
V_{DD} (externally applied, V+ = 0)	−1.0, +6	Vdc
V_{LR}	−1.0, V+ − 3.0	Vdc
$\overline{MT}$, MS Inputs	−1.0, V_{DD} +1.0	Vdc
Storage Temperature	−65, +150	°C

NOTE 1: Devices should not be operated at these values. The "Recommended Operating Conditions" provide conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Units
V+ Voltage (Speech Mode) (Tone Dialing Mode)	+1.5 to +15 +3.3 to +15	Vdc Vdc
I_{TXO} (Instantaneous)	0 to 10	mA
Ambient Temperature	−20 to +60	°C

ELECTRICAL CHARACTERISTICS (Refer to Figure 1) (T_A = 25°C)

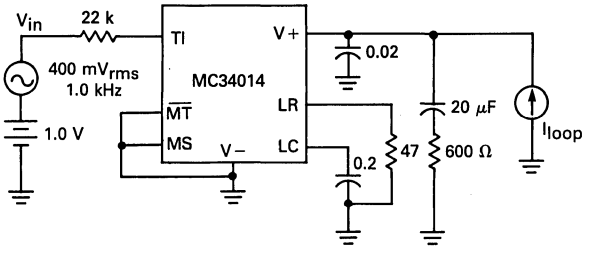
Parameter	Symbol	Min	Typ	Max	Units
LINE INTERFACE					
V+ Voltage	V+				Vdc
I_{loop} = 20 mA (Speech/Pulse Mode)		2.6	3.2	3.8	
I_{loop} = 30 mA (Speech/Pulse Mode)		3.0	3.7	4.4	
I_{loop} = 120 mA (Speech/Pulse Mode)		7.0	8.2	9.5	
I_{loop} = 20 mA (Tone Mode)		4.1	4.9	5.7	
I_{loop} = 30 mA (Tone Mode)		4.6	5.4	6.2	
V+ Current (Pin 12 Grounded)	I+				mA
V+ = 1.7 V (Speech Mode)		4.0	6.6	8.5	
V+ = 12 V (Speech/Pulse Modes)		5.5	8.4	12.5	
V+ = 12 V (Tone Mode)		6.0	8.8	14.0	
LR Level Shift (V+ − V_{LR})	ΔV_{LR}				Vdc
(Speech/Pulse Mode)		—	2.7	—	
(Tone Mode)		—	4.3	—	
LC Terminal Resistance	R_{LC}	36	57	94	kΩ
VOLTAGE REGULATORS					
VR Voltage (V+ = 1.7 V)	V_R	1.1	1.2	1.3	Vdc
Load Regulation (0 mA < I_R < 6.0 mA)	ΔV_{RLD}	—	20	—	mV
Line Regulation (2.0 V < V+ < 6.5 V)	ΔV_{RLN}	—	25	—	mV
V_{DD} Voltage (V+ = 4.5 V)	V_{DD}	3.0	3.3	3.8	Vdc
Load Regulation (0 < I_{DD} < 1.6 mA) (Dialing Mode)	ΔV_{DDLD}	—	0.25	—	Vdc
Line Regulation (All Modes) (4.0 V < V+ < 9.0 V)	ΔV_{DDLN}	—	50	—	mV
Max. Output Current (Speech Mode)	I_{DDSP}	375	550	1000	μA
Max. Output Current (Dialing Mode)	I_{DDDL}	1.6	2.0	3.6	mA
V_{DD} Leakage Current (V+ = 0, V_{DD} = 3.0 V)	I_{DDLK}	—	—	1.5	μA
SPEECH AMPLIFIERS					
Transmit Amplifier					
Gain (TXI to TXO)	A_{TXO}	—	20	—	V/V
TXO Bias Voltage (Speech/Pulse Mode)	V_{TXOSP}	0.45	0.52	0.60	x V_R
TXO Bias Voltage (Tone Mode Mode)	V_{TXODL}	VR−25	VR−5.0	—	mV
TXO High Voltage (Speech/Pulse Mode)	V_{TXOH}	VR−25	VR−5.0	—	mV
TXO Low Voltage (Speech/Pulse Mode)	V_{TXOL}	—	125	250	mV
TXI Input Resistance	R_{TXI}	—	10	—	kΩ
Receive Amplifier					
RXO Bias Voltage (All Modes)	V_{RXO}	0.45	0.52	0.60	x VR
RXO Source Current (Speech Mode)	I_{RXOSP}	1.5	2.0	—	mA
RXO Source Current (Pulse/Tone Mode)	I_{RXODL}	200	400	—	μA
RXO High Voltage (All Modes)	V_{RXOH}	VR−100	VR−50	—	mV
RXO Low Voltage (All Modes)	V_{RXOL}	—	50	150	mV

ELECTRICAL CHARACTERISTICS — (continued) (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Units
MICROPHONE, RECEIVER CONTROLS					
MIC Saturation Voltage (Speech Mode, I = 500 μA)	$V_{OL_{MIC}}$	—	50	125	mV
MIC Leakage Current (Dialing Mode, Pin 1 = 3.0 V)	$I_{MIC_{LK}}$	—	0	5.0	μA
RMT Resistance (Speech Mode) (Dialing Mode)	$R_{RMT_{SP}}$ $R_{RMT_{DL}}$	— 5.0	8.0 10	15 18	Ω kΩ
RMT Delay (Dialing to Speech)	t_{RMT}	2.0	4.0	20	ms
DIALING INTERFACE					
$\overline{MT}$ Input Resistance	R_{MT}	58	100	—	kΩ
$\overline{MT}$ Input High Voltage	V_{IHMT}	$V_{DD}-0.3$	—	—	Vdc
$\overline{MT}$ Input Low Voltage	V_{ILMT}	—	—	1.0	Vdc
MS Input Resistance	R_{MS}	280	600	—	kΩ
MS Input High Voltage	V_{IHMS}	2.0	—	—	Vdc
MS Input Low Voltage	V_{ILMS}	—	—	0.3	Vdc
TI Input Resistance	R_{TI}	—	1.25	—	kΩ
DTMF Gain (See Figure 2) ($V+/V_{in}$)	A_{DTMF}	3.2	4.8	6.2	dB
SIDETONE AMPLIFIER					
Gain (TXO to STA) (Speech Mode) @ V_{LR} = 0.5 V (Speech Mode) @ V_{LR} = 2.5 V (Pulse Mode) @ V_{LR} = 0.2 V (Pulse Mode) @ V_{LR} = 1.0 V	A_{STA}	 — — — —	 −15 −21 −15 −21	 — — — —	dB
STA Bias Voltage (All Modes)	V_{STA}	0.65	0.8	0.9	x V_R
EQUALIZATION AMPLIFIER					
Gain (V+ to EQ) (Speech Mode) @ V_{LR} = 0.5 V (Speech Mode) @ V_{LR} = 2.5 V (Pulse Mode) @ V_{LR} = 0.2 V (Pulse Mode) @ V_{LR} = 1.0 V	A_{EQ}	 — — — —	 −12 −2.5 −12 −2.5	 — — — —	dB
EQ Bias Voltage (Speech Mode) @ V_{LR} = 0.5 V (Pulse Mode) @ V_{LR} = 0.5 V (Speech, Pulse) @ V_{LR} = 2.5 V	V_{EQ}	 — — —	 0.66 1.3 3.3	 — — —	Vdc

NOTE: Typical values are not tested or guaranteed.

FIGURE 2 — DTMF DRIVER TEST



SYSTEM SPECIFICATIONS (T_A = 25°C) (See Figures 1–4)

Parameter	Min	Typ	Max	Unit
Tip-Ring Voltage (including polarity guard bridge drop of 1.4 V)				Vdc
(Speech Mode) I_{loop} = 5.0 mA	—	2.4	—	
I_{loop} = 10 mA	—	3.9	—	
I_{loop} = 20 mA	—	4.6	—	
I_{loop} = 40 mA	—	5.6	—	
I_{loop} = 60 mA	—	6.6	—	
Transmit				
Gain from V_S to V+ (Figure 3) (I_{loop} = 20 mA)	28	30	31	dB
Gain change as I_{loop} is increased to 60 mA	−6.0	−4.5	−3.6	dB
Distortion	—	2.0	—	%
Output noise	—	11	—	dBrnc
Receive				
V_{RXO}/V_S (f = 1.0 kHz, I_{loop} = 20 mA) (See Figure 4)	−16	−15	−13	dB
Receive gain change as I_{loop} is increased to 60 mA	−5.0	−3.0	−2.0	dB
Distortion	—	2.0	—	%
Sidetone Level				dB
$V_{RXO}/V+$ (Figure 3)				
I_{loop} = 20 mA	—	−36	—	
I_{loop} = 60 mA	—	−21	—	
Sidetone Cancellation $\left[\frac{V_{RXO}}{V+}\text{ (Figure 4)}\right]$ dB − $\left[\frac{V_{RXO}}{V+}\text{ (Figure 3)}\right]$ dB I_{loop} = 20 mA	20	26	—	dB
DTMF Driver	3.2	4.8	6.2	dB
$V+/V_{in}$ (Figure 2) I_{loop} = 20 mA				
AC Impedance				Ω
Speech mode (incl. C_6, See Figure 4) I_{loop} = 20 mA	—	750	—	
Z_{ac} = (600)V+/(V_S − V+) I_{loop} = 60 mA	—	300	—	
Tone mode (including C_6) 20 mA < I_{loop} < 60 mA	—	1650	—	

NOTE: Typicals are not tested or guaranteed.

FIGURE 3 — TRANSMIT AND SIDETONE LEVEL TEST

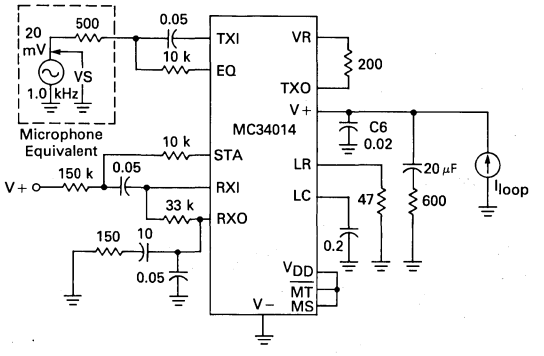
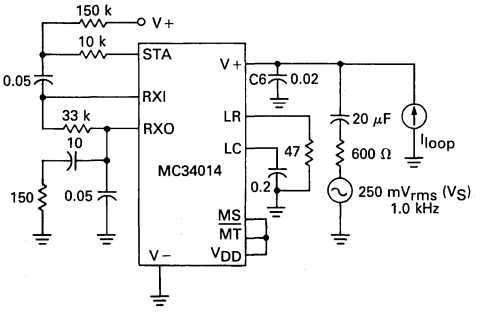


FIGURE 4 — AC IMPEDANCE, RECEIVE AND SIDETONE CANCELLATION TEST



DESIGN GUIDELINES (Refer to Figure 1)

INTRODUCTION

The MC34014 is a speech network meant for connection to the Tip & Ring lines through a polarity guard bridge. The circuit incorporates four amplifiers: transmit, receive, sidetone, and equalization. Some parameters of each amplifier are set by external components, and in addition, the gains of the sidetone and equalization amplifiers vary with loop current.

The line interface portion determines the dc voltage versus loop current characteristics, and provides the required regulated voltages for internal and external use.

The dialer interface provides three modes of operation: speech (non-dialing), pulse dialing, and tone (DTMF) dialing. When switching to either dialing mode some parameters of the various sections are changed in order to optimize the circuit operation for that mode. The following table summarizes those changes:

TABLE 1 — OPERATING PARAMETERS AS A FUNCTION OF OPERATING MODE

Function	Speech	Pulse	Tone
LR Level Shift ($V+ - V_{LR}$)	2.7 V	2.7 V	4.3 V
V_{DD} Source Current	550 μA	2.0 mA	2.0 mA
Transmit Amplifier	Functional	Functional	Inoperative
MIC Switch (Pin 1)	On	Off	Off
Equalization Amplifier	See Transfer Curves — Figure 8		
Sidetone Amplifier	See Transfer Curves — Figure 6		
Receive Amplifier Output Current	2.5 mA	400 μA	400 μA
RMT (Pin 9) Impedance	8.0 Ω	10 kΩ	10 kΩ
DTMF Amplifier	Inoperative	Inoperative	Functional
CC Voltage	$V_{LR}/3$	V_{LR}	V_{LR}

DC LINE INTERFACE (Figure 5)

The dc line interface circuit (Pins 10, 12–14) sets the dc voltage characteristics with respect to the loop current. The loop current enters at Pin 14 where the internal circuitry of the MC34014 draws 5–6 mA. Pin 3 sinks (typically) 3 mA through R_9. The remainder of the loop current is passed through Q_{301} and R_5. The resulting voltage across the entire circuit is therefore equal to the voltage across R_5, plus the level shift voltage from Pin 13 (LR) to Pin 14 (V+), nominally 2.7 volts in the speech and pulse modes. In the tone mode, the level shift increases to 4.3 volts, the internal current changes slightly (Figure 6), and the current required at Pin 3 decreases to near zero. These changes increase the equivalent dc resistance of the circuit, raising the voltage at V+ to ensure adequate voltage at V_{DD} for the external tone dialer. See Figure 7 for typical voltage versus loop current characteristics.

Capacitor C_7 at Pin 12 provides high frequency rolloff (above 10 Hz) so that R_5 does not load down the speech and DTMF signals.

The voltage at V_R is an internally regulated 1.2 volt supply which provides the bias currents for the microphone and the transmit amplifier output (Pin 3), as well as internal bias for the various amplifiers. Capacitor C_8 stabilizes the regulator. The use of an (internal) PNP transistor allows V_R to be regulated with a V+ voltage as low as 1.5 volts.

FIGURE 5 — DC LINE INTERFACE

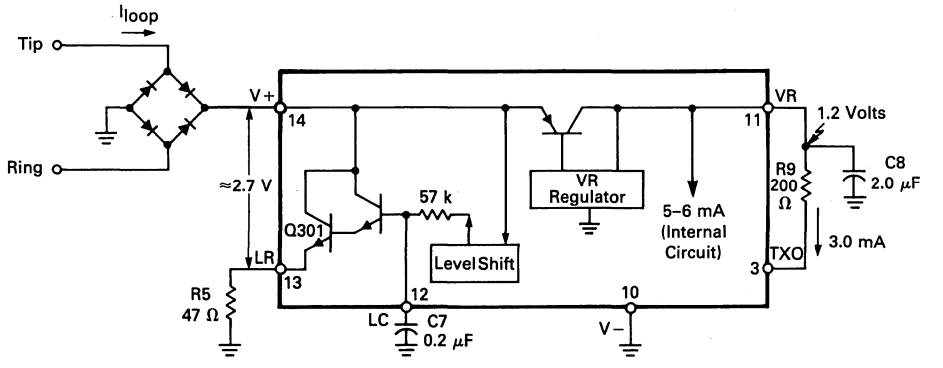


FIGURE 6 — INTERNAL CURRENT versus VOLTAGE

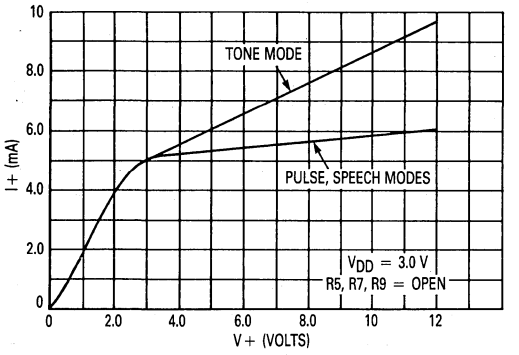
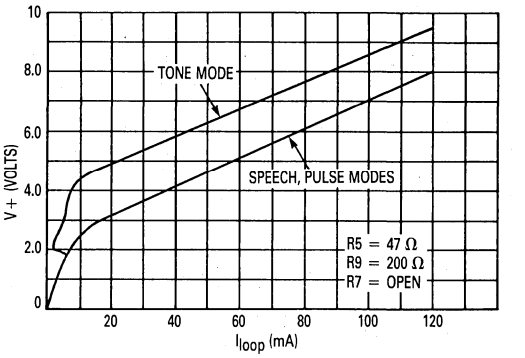


FIGURE 7 — CIRCUIT VOLTAGE versus LOOP CURRENT



TRANSMIT AMPLIFIER

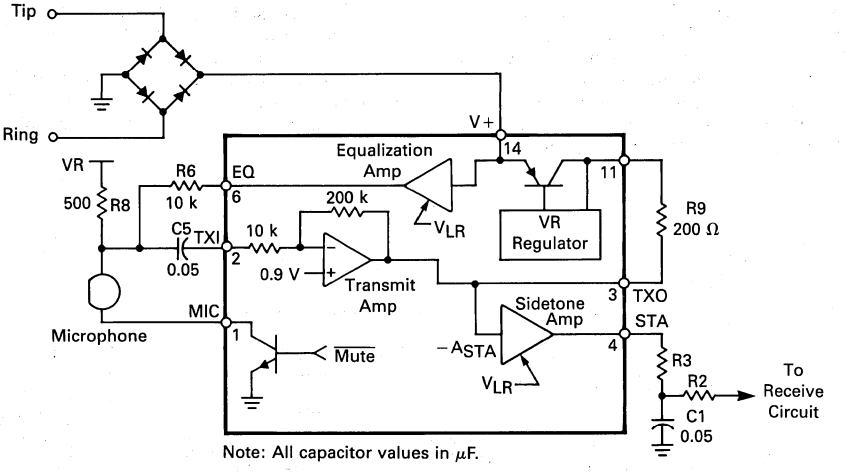
The transmit amplifier (from TXI to TXO) is inverting, with a fixed internal gain of 20 V/V (26 dB), and a typical input impedance of 10 kΩ (Figure 8). The input bias currents are internally supplied, allowing capacitive coupling of the microphone signals to the amplifier.

In the speech and pulse modes, the dc bias level at TXO is typically 0.52 x VR (≈0.63 V), which permits the output to swing 0.55 volts in both positive and negative directions without clipping. The ac voltage signal at TXO (the amplified speech signal) is converted to an ac current by R_9. The ac current passes through the VR series pass transistor to V+, modulating the loop current. The voltage signal at V+ is out of phase with the signal at TXI.

In the tone dialing mode, the TXO dc bias level is clamped at approximately VR-10 mV, rendering the amplifier inoperative. This action also reduces the TXO bias current from 3.0 mA to less than 125 μA.

MIC (Pin 1) is connected to an open-collector NPN transistor, and provides the ground path for the microphone bias current. In either dialing mode, the transistor is off, disabling the microphone.

FIGURE 8 — TRANSMIT SECTION



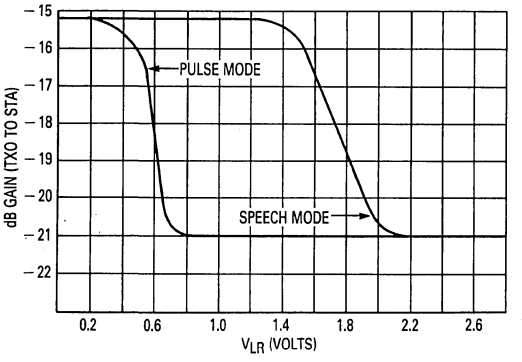
Note: All capacitor values in μF.

SIDETONE AMPLIFIER

The sidetone amplifier provides inversion of the TXO signal for the reduction of the sidetone signal at the receive amplifier (Figure 8). Resistors R_2 and R_3 determine the amount of sidetone cancellation. Capacitor C_1 provides phase shift to compensate for the phase shift created by the complex impedance of the Tip & Ring lines.

The gain of the sidetone amplifier varies with the voltage at LR (Pin 13), in effect making it a function of the loop current. The maximum gain is −15 dB (0.17 V/V) at low loop currents, and the minimum gain is −21 dB (0.09 V/V) at high loop current (see Figure 9 for transfer curves). For example, using 47 Ω for R_5, the gain would begin to decrease at ≈30 mA, and would stop decreasing at ≈57 mA (speech mode). The dc bias voltage at STA (Pin 4) changes slightly (≈50 mV) with variations in loop current. The output is inverted from TXO, which is the input to this amplifier. Since the transmit amplifier is inoperative in the tone dialing mode, the sidetone amplifier is also inoperative in that mode.

FIGURE 9 — SIDETONE AMPLIFIER GAIN



RECEIVE AMPLIFIER

The gain of the receive amplifier (from V+ to RXO) is determined according to the following equation (refer to Figure 10):

$$\frac{V_{RXO}}{V+} = \frac{R_4}{R_1} + \frac{(X_C//R_2)\,(A_{EQ})\,(A_{TXO})\,(A_{STA}) \times R_A \times R_4}{((X_C//R_2)+R_3)\,(R_A+R_6) \times R_2}$$

Where $R_A = R_8//10\ k\Omega$ (10 kΩ = R_{in} of T_X Amp)
A_{EQ} = Gain of Equalization Amp
A_{TXO} = Gain of Transmit Amp (20 V/V)
A_{STA} = Gain of sidetone Amp
X_C = Impedance of C_1 at frequency of interest

The waveform at STA (Pin 4) is in phase with that at V+ (for receive signals), hence the plus sign between the terms. Due to the variations of A_{EQ} and A_{STA} with loop current, the receive gain will vary by ≈1.5 dB. If capacitor C_1 is not used, the above equation is simplified by deleting the terms containing X_C.

The output at RXO is inverted from V+ in the receive mode. In the transmit mode, the V+-to-RXO phase relationship depends on the amount of sidetone cancellation (determined by R_2 and R_3 and C_1), and can vary from 0° to 180°.

In the speech mode, the output current capability (at RXO) is typically 2.0 mA. In either dialing mode, the current capability is reduced to 400 μA in order to reduce internal current consumption. This feature is beneficial when this device is used in conjunction with a line-powered speakerphone circuit, such as the MC34018, where the majority of the loop current is needed for the speakerphone.

RMT (Pin 9) is the return path for the receiver's ac current. This pin is internally connected to an open collector NPN transistor, paralleled by a 10 kΩ resistor. In the speech mode, the transistor is on, providing a low impedance from RMT to ground. In either dialing mode, the transistor is off, muting the receive signal. This prevents loud "clicks" or loud DTMF tones from being heard in the receiver during dialing. When switching from either dialing mode to the speech mode ($\overline{MT}$ switches from low to high), the RMT pin switches back to a low impedance after a delay of 2–20 ms. The delay reduces clicks in the receiver associated with switching from the dialing to speech mode.

EQUILIZATION AMPLIFIER

The equalization amplifier gain varies with loop current, and is configured in the circuit so as to cause a variation of the network ac impedance (when looking in from the Tip & Ring lines). The gain varies with the voltage at LR (Pin 13), in effect making it a function of the loop current. The maximum gain is −2.5 dB (0.75 V/V) at high loop current, and the minimum gain is −12 dB (0.25 V/V) and low loop current (see Figure 11 for transfer curve). For example, using 47 Ω for R_5, the gain would begin to increase at ≈30 mA, and would stop increasing at ≈57 mA (speech mode). The output signal is in phase with the signal at V+, which is the input to this amplifier.

The dc bias level at EQ (Pin 6) varies with the voltage at LR (Pin 13) according to the curve of Figure 12. In most applications, this level shift is of little consequence, and may be ignored. If a particular circuit configuration should be sensitive to the shift, however, the output signal at EQ may be ac coupled to the rest of the circuit.

The equalization amplifier remains functional in all three modes, although in the tone mode, its function has no consequence when the circuit is configured as shown in Figure 1.

V_{DD} REGULATOR

The V_{DD} regulator is a shunt type regulator which supplies a nominal 3.3 volts for external dialers, and/or

other circuitry. In the speech mode, the output current capability at Pin 15 is typically 550 μA. In either dialing mode, the current capacity is increased to 2.0 mA.

V_{DD} will be regulated whenever V+ is >300 mV above the regulated value. As V+ is lowered, and the internal pass transistor becomes saturated, the circuit steers current away from the external load through an internal current source, in order that the V_{DD} capacitor (C9) does not load down speech and DTMF signals at V+. As V+ is lowered below 1 volt, Pin 15 switches to a high impedance state to prevent discharging of any storage capacitors, or batteries used for memory retention.

The V_{DD} voltage is unaffected by the choice of operating mode.

DIALER INTERFACE

The dialer interface consists of the mode control pins, $\overline{MT}$ and MS (Pins 18 and 17), and the DTMF current amplifier.

The $\overline{MT}$ pin, when at a Logic "1" (> V_{DD} – 0.3 V), sets the circuit into the speech mode, independent of the state of the MS pin. When the $\overline{MT}$ pin is at a Logic "0" (< 1.0 V), the dialing mode is determined by the MS pin. When MS is at a Logic "1" (> 2.0 V), the circuit is in the pulse dialing mode, and when at a Logic "0" (< 0.3 V) the tone (DTMF) mode is in effect.

The input impedance of the $\overline{MT}$ pin is typically 100 kΩ, with the input current flowing out of the pin (from V_{DD}). The input impedance of the MS pin is typically 600 kΩ, and the input current flows into the pin (Figure 1).

The DTMF amplifier (Figure 13) is a current amplifier which transmits DTMF signals to the V+ pin, and consequently onto the Tip & Ring lines. Waveforms from a DTMF dialer are input at TI (Pin 16) through a current limiting resistor (R_7). Negative feedback around the amplifier reduces the overall gain so that return loss specifications may be met. The voltage gain is calculated using the following equation:

$$\frac{V+}{V_i} = \frac{80\ R_E}{(1\ +\ 0.795R_7\ +\ 0.4R_ER_7)}$$

(R_E, R_7 in kΩ)
where $R_E = R_L//2$ kΩ (2 kΩ = internal dynamic impedance)

Using 22 kΩ for R_7, and 600 Ω for R_L, the voltage gain is a nominal 4.3 dB. The minimum loop current at which the circuit of Figure 1 will operate without distortion is 12 mA.

The DTMF amplifier is functional only in the tone dialing mode, and the waveform at V+ is inverted from that at TI. The TI pin requires a dc bias current (into the pin) of 20–50 μA, which may be supplied by the Tone dialer circuit, or by using the biasing scheme of Figure 14.

CC (PIN 5)

The CC pin (Compensation Capacitor) has two functions: 1) to provide equalization loop stability where the normal stabilizing components are ineffective; and 2) to allow optional control of the equalization functions.

In most applications, the capacitor at LC (Pin 12) provides the required stability, and no further compensation is required. In applications where changes are forced at Pin 12 and/or 13 (e.g., see Figure 23), the LC capacitor's effectiveness may be lost. The addition of a 10 μF capacitor to Pin 5 will provide the required additional compensation.

The CC pin may be used to force the loop length compensation circuits to specific modes. Grounding CC will set the sidetone and equalization amplifiers at the low loop current values. Connecting CC to V_R will set the amplifiers at the high loop current values.

Variations in the curves of Figures 9 and 11 may be obtained by using external resistors from LR to CC, and from CC to V–.

FIGURE 10 — RECEIVE CIRCUIT

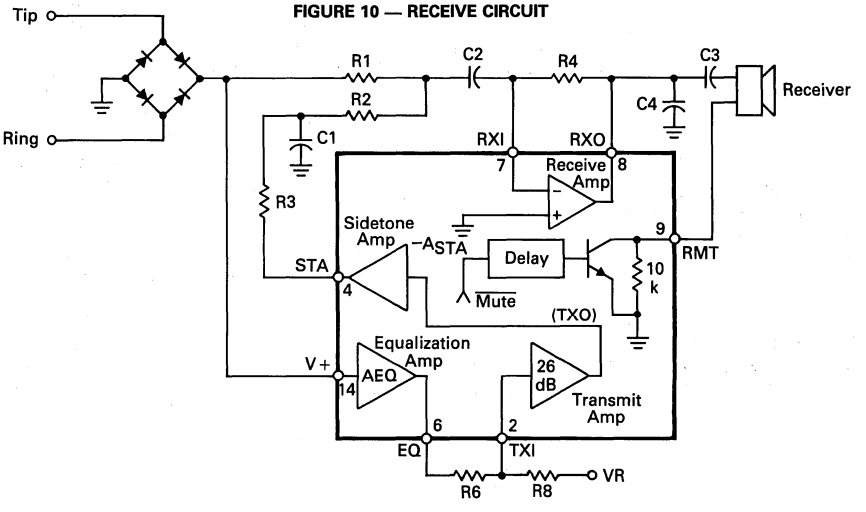


FIGURE 11 — EQUALIZATION AMPLIFIER GAIN

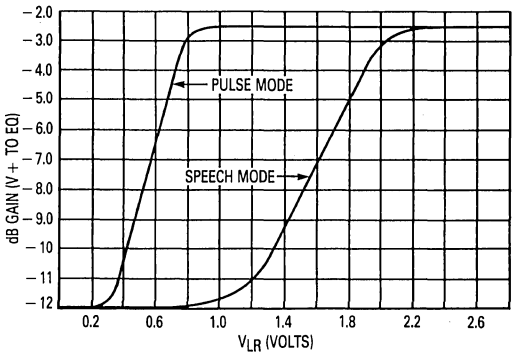


FIGURE 12 — EQ (PIN 6) DC VOLTAGE

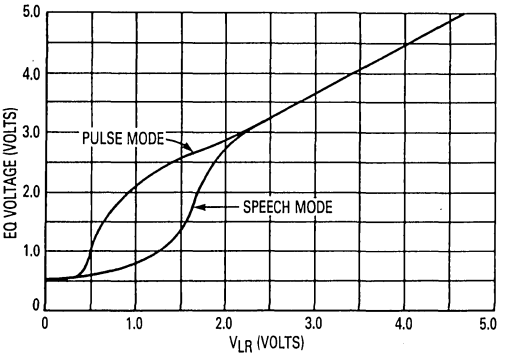


FIGURE 13 — DTMF TONE DIALER

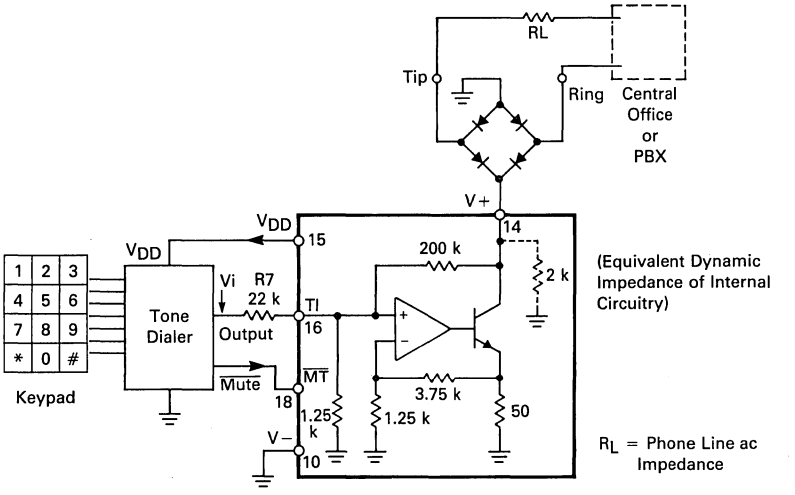
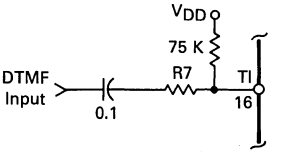


FIGURE 14 — INPUT BIASING



APPLICATIONS INFORMATION

AC IMPEDANCE

One of the basic problems with early telephones is that the performance varied with different line lengths (distance from the Central Office to the telephone). If a particular phone were optimized for short loops and then connected to a long loop, both the transmitted and receive signals would be difficult to hear. On the other hand, phones optimized for long loops would then be annoyingly loud on short loops. The process of equalization is one whereby the performance is forced to vary with loop length inversly to the expected variations. Monitoring of loop length is accomplished by monitoring the loop current at the telephone. In the MC34014, loop length equalization is provided by varying the ac impedance of the telephone circuit. In this manner the MC34014 mimics a passive network, with varistors providing the equalization.

Figure 15 depicts the situation in the receive mode. The receive signal coming from the Central Office is V_S and is independent of the loop length. Z_R is the ac impedance of the Central Office, nominally 900 Ω. Z_L is the characteristic impedance of the phone line, and is a nominal 600 Ω. The signal applied to the line (V_1) is therefore a portion of V_S. That signal is attenuated by the distributive impedance of the phone line, with a resulting signal V_2 at the telephone. The amplitude of V_2 depends on the amount of attenuation, the impedance of the phone line at the telephone and the ac impedance of the telephone (Z_{ac}), according to:

$$V_2 = \frac{V_1' \times Z_{ac}}{Z_{ac} + Z_L}$$

where V_1' is the equivalent signal source at the receive end of the phone line, providing the signal V_2 through the impedance equal to the characteristic impedance of the line (Z_L). The value of V_1' depends on how much V_1 has been attenuated by the length of phone line. By increasing Z_{ac} on long loops, V_2 is a greater portion of V_1', resulting in a stronger receive signal at the telephone.

FIGURE 15 — RECEIVE MODE

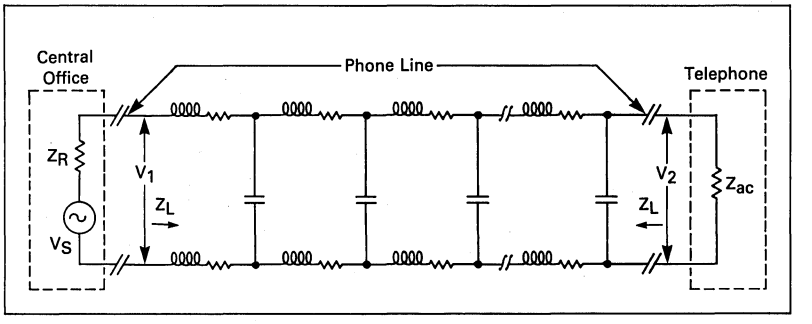
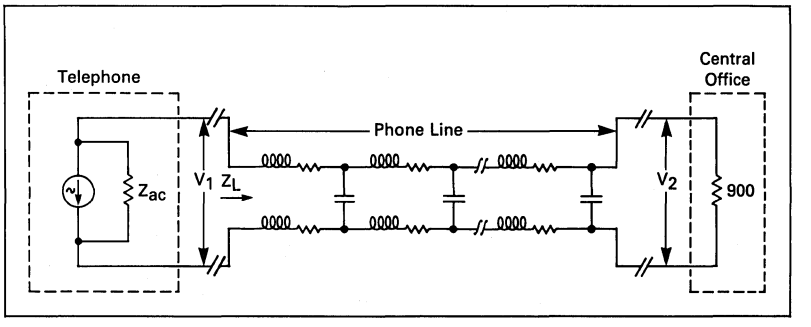


Figure 16 depicts the situation in the transmit mode. In this mode, the MC34014 is an ac current source, with a finite output impedance, modulating the loop current. The voltage signal V_1 is therefore equal to the ac signal current acting on Z_{ac} in parallel with the characteristic impedance of the phone line (Z_L). The signal is attenuated by the distributive impedance of the phone line, and so only a portion of that signal (V_2) appears at the Central Office. By increasing Z_{ac} on long loops, V_1 is increased, resulting in a higher signal level at V_2.

FIGURE 16 — TRANSMIT MODE



The ac impedance of the telephone circuit is determined by the transmit amplifier, equalization amplifier, and external resistors R_6, R_8, and R_9. In Figure 17, a portion of the receive signal at V+ appears at EQ. That signal is reduced at TXI by the R_8-R_6 divider (the electret microphone is a high impedance). The signal at TXI is then amplified by 20, and that signal (at TXO) is converted to an ac current by R9. The ac impedance of the circuit is therefore $V+/I_{TXO}$, and is defined by the following equation:

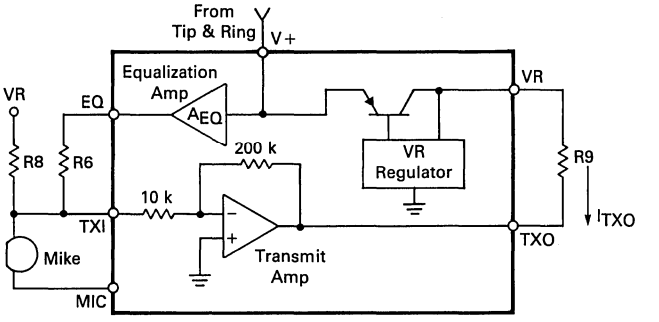
$$Z_{ac} = \frac{(1 + R_8/R_6)(R_9)}{20 \times A \times (R_8/R_6)}$$

where A = the gain of the equalization amplifier (0.25 to 0.75)

Since the gain of the equalization amplifier varies by a factor of 3, the ac impedance will vary the same amount. Using the resistor values indicated in Figure 1, the ac impedance will vary from 280 Ω (short loop) to 840 Ω (long loop).

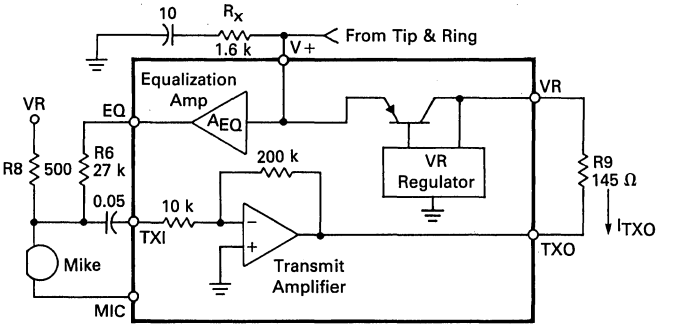
When calculating or measuring the ac impedance, capacitor C_6 (≈8.0 kΩ at 1.0 kHz) and the dynamic impedance of the MC34014 (≈10 kΩ) must be taken into account. If the microphone has an impedance lower than that of a typical electret, then its dynamic impedance must be accounted for in the above equation.

FIGURE 17 — DETERMINING AC IMPEDANCE



If a variation in Z_{ac} of less than 3:1 is desired, the circuit configuration of Figure 18 may be used. The ac impedance is the parallel combination of R_X and the impedance presented by the remainder of the circuit. With the values shown in Figure 18, the ac impedance varies from 400 Ω to 800 Ω.

FIGURE 18 — REDUCED AC IMPEDANCE VARIATION



TRANSMIT DESIGN PROCEDURE

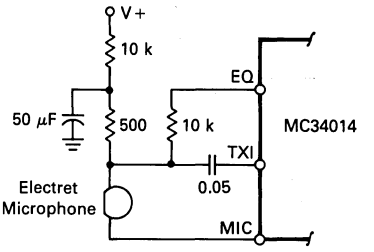
Referring to Figure 17, first select R_9 for the desired maximum output level at Tip & Ring, assuming a signal level at TXO of 1.0 V p-p. The maximum signal level at Tip & Ring will be approximately:

$$\frac{(V_{TXO})\ (Z_L)}{R_9}$$

where Z_L is the characteristic ac impedance of the phone line. Capacitor C_6 and the ≈10 kΩ dynamic impedance of the MC34014 must also be considered in the above computation, since they are in parallel with Z_L.

The next step is to select the R_6/R_8 ratio, according to the required Z_{ac}, using the equation on the previous page. Then R_8 is selected to set the microphone sensitivity. R_8 is typically in the range of 0.5 k to 1.5 kΩ, and is dependent on the characteristics of the microphone. R_6 is then calculated from the above mentioned ratio.

FIGURE 19 — ALTERNATE MICROPHONE BIAS



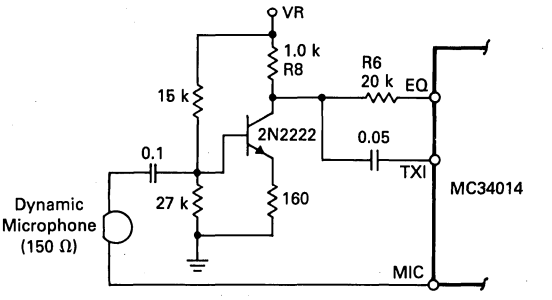
The overall gain from the microphone to V+ will vary with loop current due to the influence of the equalization amplifier on TXI. The signal at EQ is out of phase with that at TXI, therefore the signal at V+ decreases as loop current (and the EQ signal) increases. Variations are typically 2.0 to 5.0 dB and depend largely on the impedance characteristics of the microphone.

ALTERNATE MICROPHONE BIASING

In the event that the microphone cannot be properly biased from the 1.2 volt VR supply, a higher voltage can be obtained by biasing from the V+ supply. The configuration shown in Figure 19, provides a higher voltage to the microphone, and also filters the speech signals at V+ from reaching it, preventing an oscillatory loop from forming. The maximum voltage limit of the microphone must be considered when biasing this way.

If a dynamic microphone is to be used in place of an electret unit, the circuit in Figure 20 will buffer its low impedance from the MC34014 circuit, maintaining the high impedance required at the junction of R_8 and R_6. The circuit shown provides a gain of ≈2.6 for the microphone signals, and can be adjusted by varying the 160 Ω resistor.

FIGURE 20 — INTERFACING A DYNAMIC MICROPHONE



HANDSET/HANDS-FREE TELEPHONE

Figure 23 indicates a circuit using the MC34014 speech network, MC34018 speakerphone circuit, and the MC34017 tone ringer to provide a complete telephone/speakerphone. Switch HS (containing one normally open and one normally closed contact) is the hook switch actuated by the handset, shown in the on-hook position. When the handset is off-hook (HS1 open, HS2 closed), power is applied to the MC34014, and consequently the handset, and the $\overline{CS}$ pin of the MC34018 is held high so as to disable it. Upon closing the two poles of switch SS, and placing switch HS in the on-hook position, power is then applied to both the MC34014 and the MC34018, and $\overline{CS}$ is held low, enabling the speakerphone function. Anytime the handset is removed from switch HS, the circuit reverts to the handset mode. The diode circuitry sets the MC34014 to the pulse dialing mode to mute the handset microphone and receiver when using the speakerphone. To compensate for the different equalization response of the MC34014 when in the pulse dialing mode (Figures 9 and 11), the 47 Ω resistor normally found at Pin 13 of the MC34014 is instead divided into two resistors (33 Ω and 15 Ω). This arrangement provides similar equalization response in both the handset and in the speakerphone modes. Since the LC capacitor (Pin 12) is ineffective in the speakerphone mode, a capacitor is added at Pin 5 (CC) to provide compensation for the equalization loop when the speakerphone mode is in effect.

SWITCHABLE TONE/PULSE TELEPHONE

Figure 21 indicates a switchable tone/pulse telephone circuit using the MC145412 tone/pulse dialer, MC34014 speech network, and the MC34017 tone ringer. The dialer is programmable, and can store up to 10 phone numbers. As can be seen, the interface to the MC34014 is straightforward.

PULSE ONLY TELEPHONE

Figure 22 indicates a pulse only telephone circuit using the MC145409 pulse dialer, MC34014 speech network, and the MC34017 tone ringer. The dialer has last number redial, and provides a pacifier tone to the receiver during dialing.

FIGURE 21 — COMPLETE TELEPHONE WITH PULSE/TONE DIALING

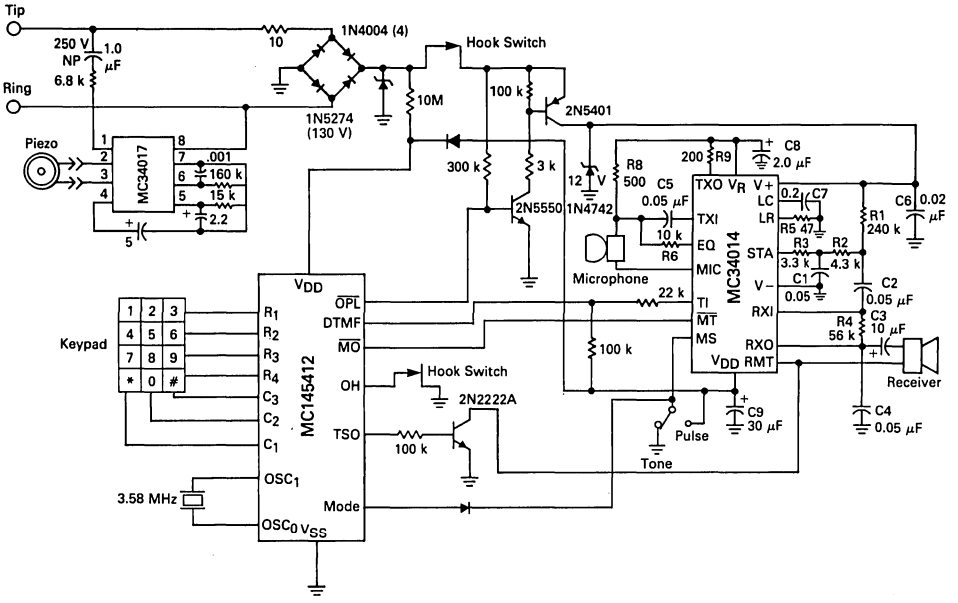


FIGURE 22 — COMPLETE TELEPHONE WITH PULSE DIALING

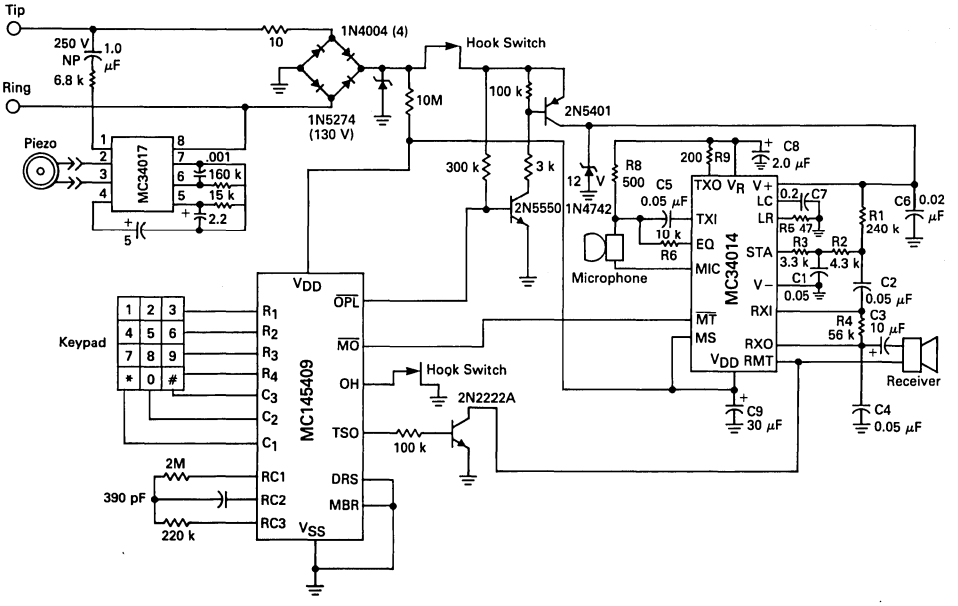
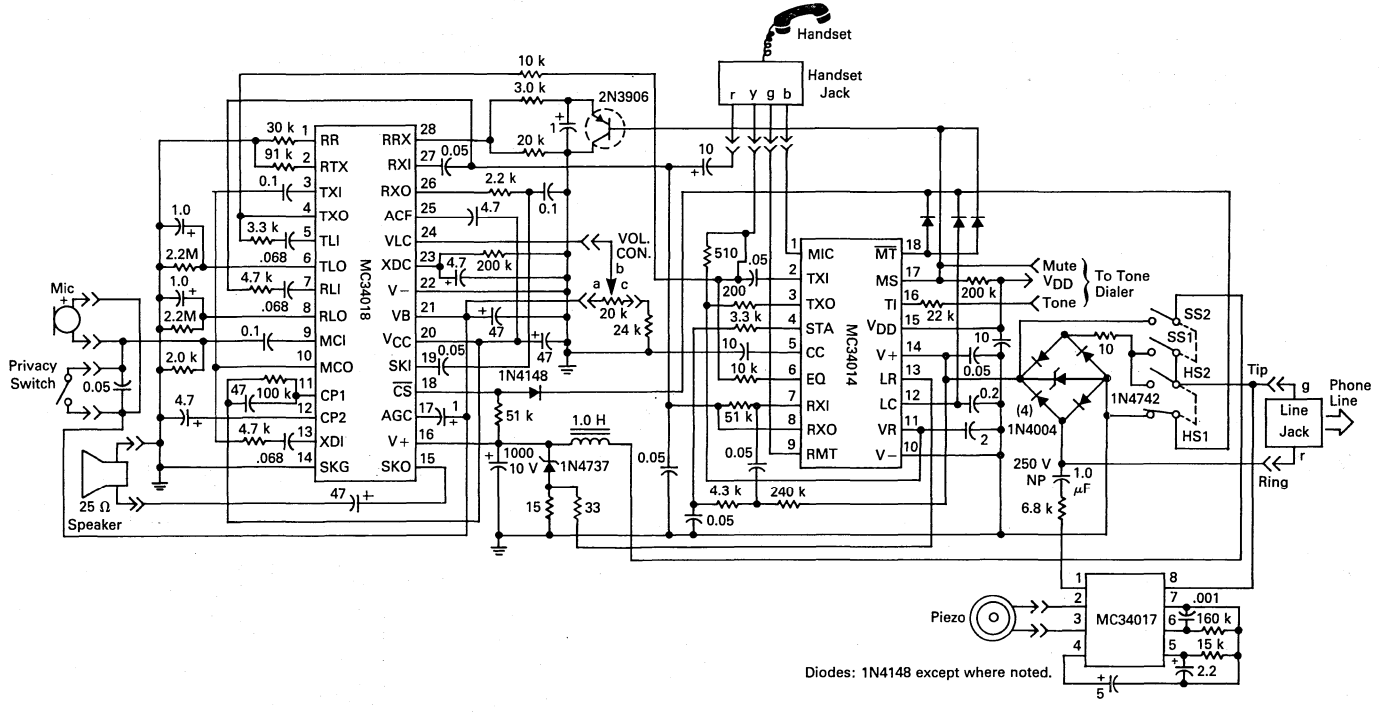


FIGURE 23 — SWITCHABLE HANDSET/HANDSFREE SYSTEM



Recommended External Components

Piezo Sounder
Models KSN 1113-1116
Motorola, Inc.
Albuquerque, N.M.
505-822-8801

Microphone/Receiver
Microphone model EM-95
Receiver model DH-34
Primo Microphone, Inc.
Elk Grove Village, Ill.
312-595-1022

Microphone Model KUC2123
Hosiden Electronics
Chicago, Ill.
312-956-7707

TRANSIENT PROTECTION & RFI SUPPRESSION

Protection from voltage transients is necessary in most telephone circuits, and may take the form of zener diodes, RC or LC filters, transient suppressors, or a combination of the above.

Potential radio frequency interference problems should be addressed early in the electrical and mechanical design of the telephone. RFI may enter the circuitry through the Tip & Ring lines, through the microphone and/or receiver leads in the handset cord, or through any of the wiring or PC board traces. Ceramic decoupling capacitors, ferrite beads, and other RFI suppression techniques may be needed. Good PC board design techniques, such as the avoidance of loops, should be used. Long tracks on high impedance nodes should be avoided.

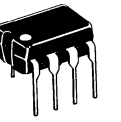
MC34017

TELEPHONE TONE RINGER

- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On-Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Push Pull Output Stage for Greater Output Power Capability
- Base Frequency Options — MC34017-1: 1.0 kHz
  MC34017-2: 2.0 kHz
  MC34017-3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

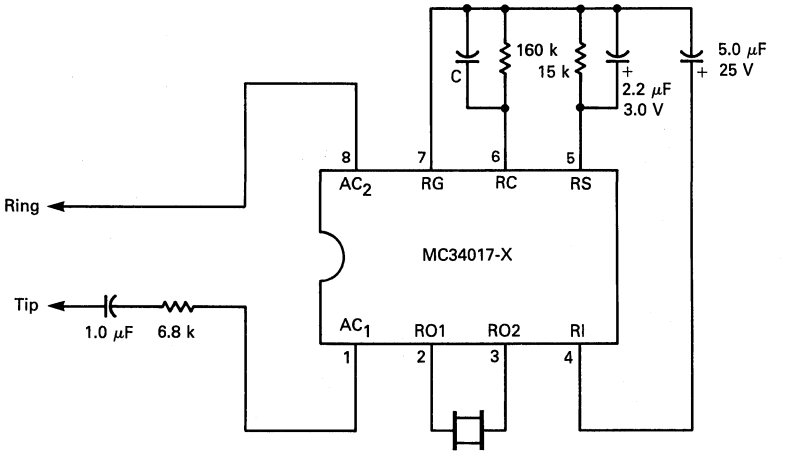
TELEPHONE TONE RINGER

BIPOLAR LINEAR/I^2L



PLASTIC PACKAGE
CASE 626

APPLICATION CIRCUIT



MC34017-1: C = 1000 pF
MC34017-2: C = 500 pF
MC34017-3: C = 2000 pF

APPLICATION CIRCUIT PERFORMANCE (Refer to Circuit on First Page.)

Characteristic	Typical Value	Units
Output Tone Frequencies MC34017-1 MC34017-2 MC34017-3 Warble Frequency	 808/1010 1616/2020 404/505 12.5	Hz
Output Voltage ($V_I \geq 60\ V_{rms}$, 20 Hz)	37	V_{p-p}
Output Duty Cycle	50	%
Ringing Start Input Voltage (20 Hz)	36	V_{rms}
Ringing Stop Input Voltage (20 Hz)	21	V_{rms}
Maximum ac Input Voltage ($\leq$ 68 Hz)	150	V_{rms}
Impedance When Ringing $V_I = 40\ V_{rms}$, 15 Hz $V_I = 130\ V_{rms}$, 23 Hz	 >16 12	kΩ
Impedance When Not Ringing $V_I = 10\ V_{rms}$, 24 Hz $V_I = 2.5\ V_{rms}$, 24 Hz $V_I = 10\ V_{rms}$, 5.0 Hz $V_I = 3.0\ V_{rms}$, 200–3200 Hz	 28 >1.0 55 >200	 kΩ MΩ kΩ kΩ
Maximum Transient Input Voltage (T $\leq$ 2.0 ms)	1500	V
Ringer Equivalence: Class A Class B	0.5 0.9	— —

PIN DESCRIPTIONS

Name	Description
AC_1, AC_2	The input terminals to the full-wave diode bridge. The ac ringing signal from the telephone line energizes the ringer through this bridge.
RS	The input of the threshold comparator to which diode bridge current is mirrored and sensed through an external resistor (R3). Nominal threshold is 1.2 volts. This pin internally clamps at 1.5 volts.
RI	The positive supply terminal for the oscillator, frequency divider and output buffer circuits.
RO1, RO2	The tone ringer output terminals through which the sound element is driven.
RG	The negative terminal of the diode bridge and the negative supply terminal of the tone generating circuitry.
RC	The oscillator terminal for the external resistor and capacitor which control the tone ringer frequencies (R2, C2).

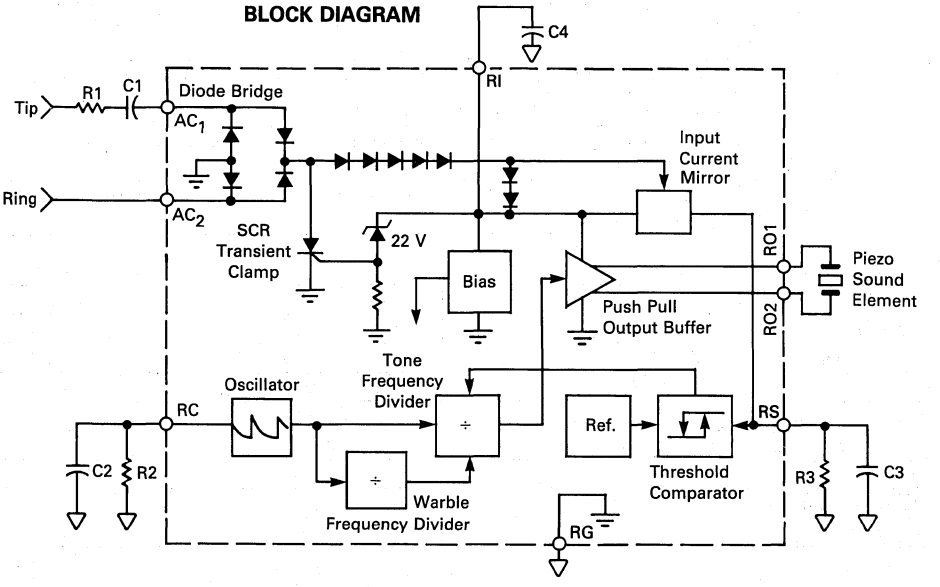
MAXIMUM RATINGS (Voltages Referenced to RG, Pin 7)

Parameter	Value	Unit
Operating AC Input Current (Pins 1, 8)	20	mA, RMS
Transient Input Current (Pins 1, 8) (T<2.0 ms)	±300	mA, peak
Voltage Applied at RC (Pin 6)	5.0	V
Voltage Applied at RS (Pin 5)	5.0	V
Voltage Applied to Outputs (Pins 2, 3)	−2.0 to V_{RI}	V
Power Dissipation (@ 25°C)	1.0	W
Operating Temperature Range	−20 to +60	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Test	Symbol	Min	Typ	Max	Units
Ringing Start Voltage (V_{Start} = V_I @ Ring Start)						Vdc
V_I>0	1a	$V_{Start}(+)$	34	37.5	41	
V_I<0	1b	$V_{Start}(-)$	−34	−37.5	−41	
Ringing Stop Voltage (V_{Stop} = V_I @ Ring Stop)	1c	V_{Stop}				Vdc
MC34017-1			14	16	22	
MC34017-2			12	14	20	
MC34017-3			14	16	22	
Output Frequencies (V_I = 50 V)	1d					Hz
MC34017-1 High Tone		f_H	937	1010	1083	
Low Tone		f_L	752	808	868	
Warble Tone		f_W	11.5	12.5	14	
MC34017-2 High Tone		f_H	1874	2020	2166	
Low Tone		f_L	1504	1616	1736	
Warble Tone		f_W	11.5	12.5	14	
MC34017-3 High Tone		f_H	937	1010	1083	
Low Tone		f_L	752	808	868	
Warble Tone		f_W	23	25	28	
Output Voltage (V_I = 50 V)	6	V_O	34	37	43	V_{p-p}
Output Short-Circuit Current	2	I_{RO1}, I_{RO2}	35	60	80	mA_{p-p}
Input Diode Voltage (I_I = 5.0 mA)	3	V_D	5.4	6.2	6.8	Vdc
Input Voltage — SCR Off (I_I = 30 mA)	4a	V_{off}	30	38	43	Vdc
Input Voltage — SCR On (I_I = 100 mA)	4b	V_{on}	3.2	4.1	6.0	Vdc
RS Clamp Voltage (V_I = 50 V)	5	V_{clamp}	1.3	1.5	1.8	Vdc

BLOCK DIAGRAM



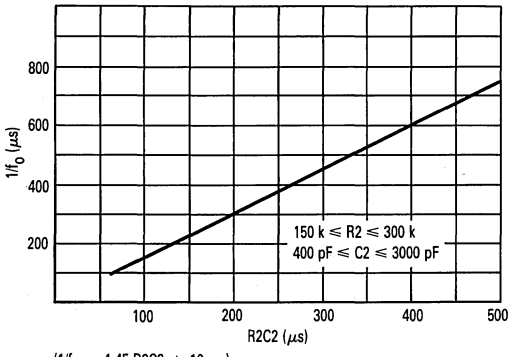
CIRCUIT DESCRIPTION

The MC34017 Tone Ringer derives its power supply by rectifying the ac ringing signal. It uses this power to activate a tone generator and drive a piezo-ceramic transducer. The tone generation circuitry includes a relaxation oscillator and frequency dividers which produce high and low frequency tones as well as the tone warble frequency. The relaxation oscillator frequency f_o is set by resistor R2 and capacitor C2 connected to pin RC. The oscillator will operate with f_o from 1.0 kHz to 10 kHz with the proper choice of external components (See Figure 1).

The frequency of the tone ringer output signal at RO1 and RO2 alternates between $f_o/4$ to $f_o/5$. The warble rate at which the frequency changes is $f_o/320$ for the MC34017-1, $f_o/640$ for the MC34017-2, and $f_o/160$ for the MC34017-3. With a 4.0 kHz oscillator frequency, the MC34017-1 produces 800 Hz and 1000 Hz tones with a 12.5 Hz warble rate. The MC34017-2 generates 1600 Hz and 2000 Hz tones with a similar 12.5 Hz warble frequency from an 8.0 kHz oscillator frequency. The MC34017-3 will produce 400 Hz and 500 Hz tones with a 12.5 Hz warble rate from a 2.0 kHz oscillator frequency. The tone ringer output circuit can source or sink 20 mA with an output voltage swing of 37 volts peak-to-peak. Volume control is readily implemented by adding a variable resistance in series with the piezo transducer.

Input signal detection circuitry activates the tone ringer output when the ac line voltage exceeds programmed threshold level. Resistor R3 determines the ringing signal amplitude at which an output signal at RO1 and RO2 will be generated. The ac ringing signal is rectified by the internal diode bridge. The rectified input signal produces a voltage across R3 which is referenced to RG. The voltage across resistor R3 is filtered by capacitor C3 at the input to the threshold circuit.

FIGURE 1 — OSCILLATOR PERIOD ($1/f_o$) versus OSCILLATOR R2 C2 PRODUCT



($1/f_o$ = 1.45 R2C2 + 10 μs)

When the voltage on capacitor C3 exceeds 1.2 volts, the threshold comparator enables the tone ringer output. Line transients produced by pulse dialing telephones do not charge capacitor C3 sufficiently to activate the tone ringer output.

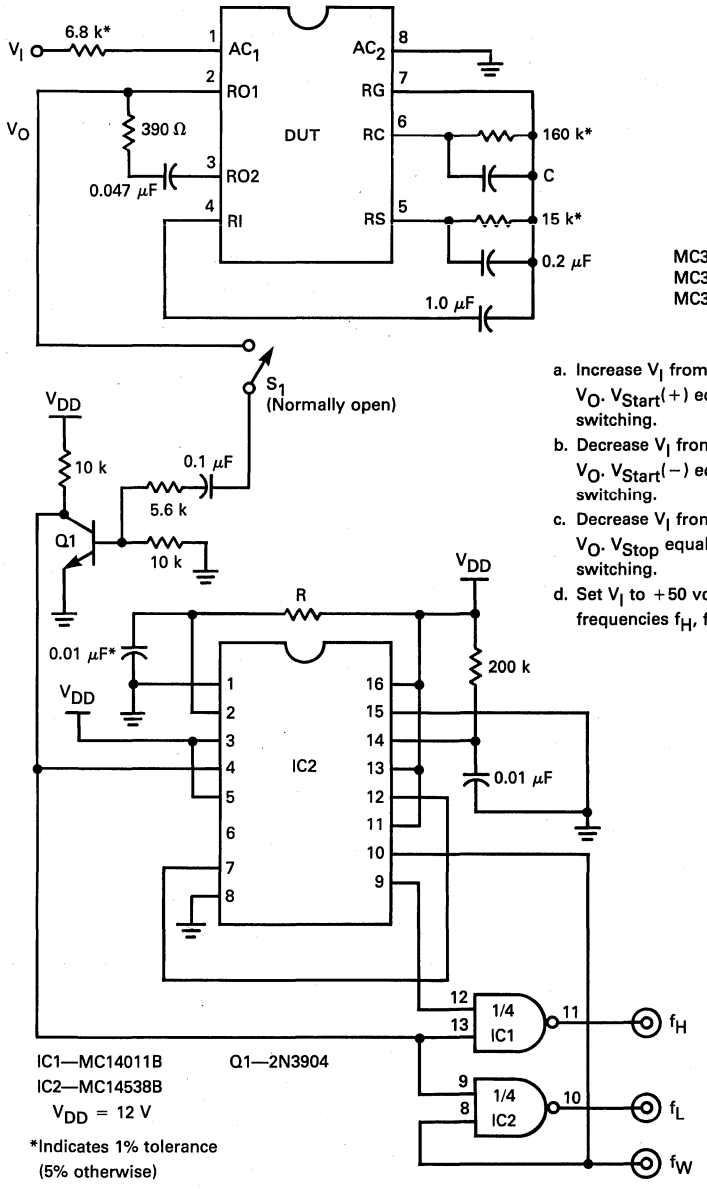
Capacitors C1 and C4 and resistor R1 determine the 10 volt, 24 Hz signature test impedance. C4 also provides filtering for the output stage power supply to prevent droop in the square wave output signal. Six diodes in series with the rectifying bridge provide the necessary non-linearity for the 2.5 volt, 24 Hz signature tests.

An internal shunt voltge regulator between the RI and RG terminals provides dc voltage to power output stage, oscillator, and frequency dividers. The dc voltage at RI is limited to approximately 22 volts in regulation. To protect the IC from telephone line transients, an SCR is triggered when the regulator current exceeds 50 mA. The SCR diverts current from the shunt regulator and reduces the power dissipation within the IC.

EXTERNAL COMPONENTS

R1	Line input resistor. R1 affects the tone ringer input impedance. It also influences ringing threshold voltage and limits current from line transients. (Range: 2.0 kΩ to 10 kΩ).
C1	Line input capacitor. C1 ac couples the tone ringer to the telephone line and controls ringer input impedance at low frequencies. (Range: 0.4 μF to 2.0 μF).
R2	Oscillator resistor. (Range: 150 kΩ to 300 kΩ).
C2	Oscillator capacitor. (Range: 400 pF to 3000 pF).
R3	Input current sense resistor. R3 controls the ringing threshold voltage. Increasing R3 decreases the ring-start voltage. (Range: 5.0 kΩ to 18 kΩ).
C3	Ringing threshold filter capacitor. C3 filters the ac voltage across R3 at the input of the ringing threshold comparator. It also provides dialer transient rejection. (Range: 0.5 μF to 5.0 μF).
C4	Ringer supply capacitor. C4 filters supply voltage for the tone generating circuits. It also provides an ac current path for the 10 V_{rms} ringer signature impedance. (Range: 1.0 μF to 10 μF).

FIGURE 2 — TEST ONE

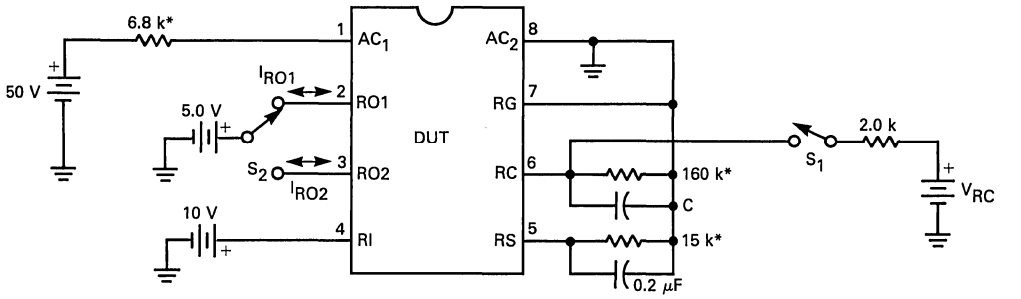


MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

a. Increase V_I from +33 volts while monitoring V_O. $V_{Start}(+)$ equals V_I when V_O commences switching.
b. Decrease V_I from −33 volts while monitoring V_O. $V_{Start}(-)$ equals V_I when V_O commences switching.
c. Decrease V_I from +40 volts while monitoring V_O. V_{Stop} equals V_I when V_O ceases switching.
d. Set V_I to +50 volts. Close S1. Measure frequencies f_H, f_L, and f_W.

MC34017-1: R = 110 kΩ*
MC34017-2: R = 55 kΩ*
MC34017-3: R = 110 kΩ*

FIGURE 3 — TEST TWO



With V_{RC} = 4.0 volts, close S_1. Switch S_2 to Pin 2 and measure current at Pin 2 (Io1). Repeatedly switch V_{RC} between 4.0 volts and 0 volts until Pin 2 current changes polarity. Measure the opposite polarity current (Io2). Calculate:

$I_{RO1} = |Io1| + |Io2|$

Switch S2 to Pin 3 and repeat.

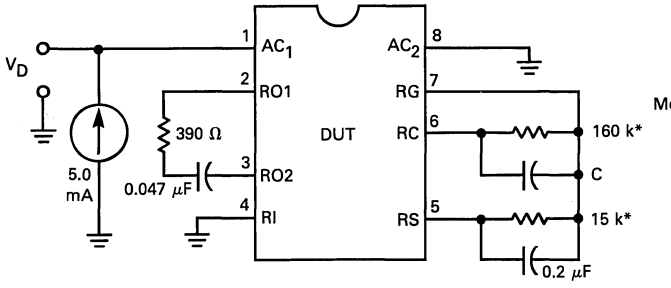
Calculate:

$I_{RO2} = |Io1| + |Io2|$

MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 4 — TEST THREE

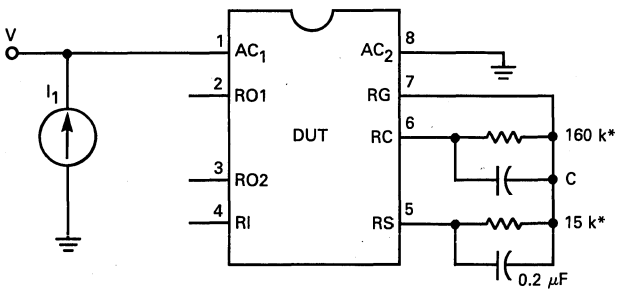


Measure voltage at Pin 1.

MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 5 — TEST FOUR



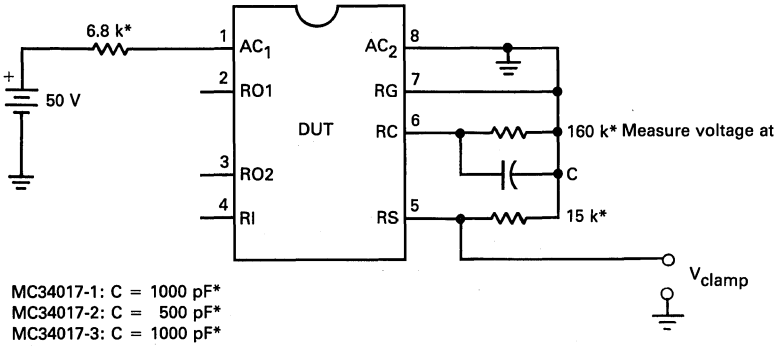
MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

a. Set I_I to 30 mA. Measure voltage at Pin 1 (V_{off}).
b. Set I_I to 100 mA. Measure voltage at Pin 1 (V_{on}).

(Each test < 30 ms)

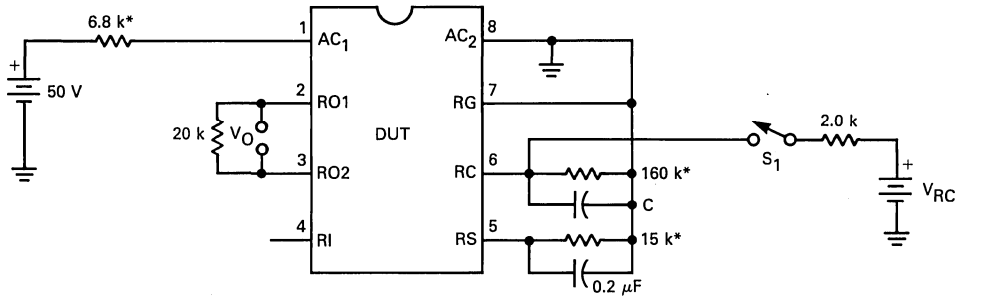
FIGURE 6 — TEST FIVE



MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

FIGURE 7 — TEST SIX



MC34017-1: C = 1000 pF*
MC34017-2: C = 500 pF*
MC34017-3: C = 1000 pF*

*Indicates 1% tolerance (5% otherwise)

With V_{RC} = 4.0 volts, close S_1. Measure dc voltage between Pins 2 and 3 (Vo1). Repeatedly switch V_{RC} between 4.0 volts and 0 volts until Pins 2 and 3 change state. Measure the new voltage between Pins 2 and 3 (Vo2).
Calculate:
$V_o = |Vo1| + |Vo2|$

MC34018

Specifications and Applications Information

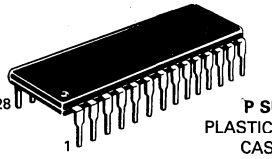
VOICE SWITCHED SPEAKERPHONE CIRCUIT

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a high quality hands-free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line-powered operation (no additional power supplies required). A Chip Select pin allows the chip to be powered down when not in use. A volume control function may be implemented with an external potentiometer. MC34018 applications include speakerphones for household and business use, intercom systems, automotive telephones, and others.

- All necessary level detection and attenuation controls for a hands-free telephone in a single integrated circuit
- Background noise level monitoring with long time constant
- Wide operating dynamic range through signal compression
- On-chip supply and reference voltage regulation
- Typical 100 mW output power (into 25 Ohms) with peak limiting to minimize distortion
- Chip Select pin for active/standby operation
- Linear Volume Control Function
- Standard 28-pin plastic DIP package (0.600 inch wide) and SOIC package

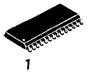
VOICE SWITCHED SPEAKERPHONE CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

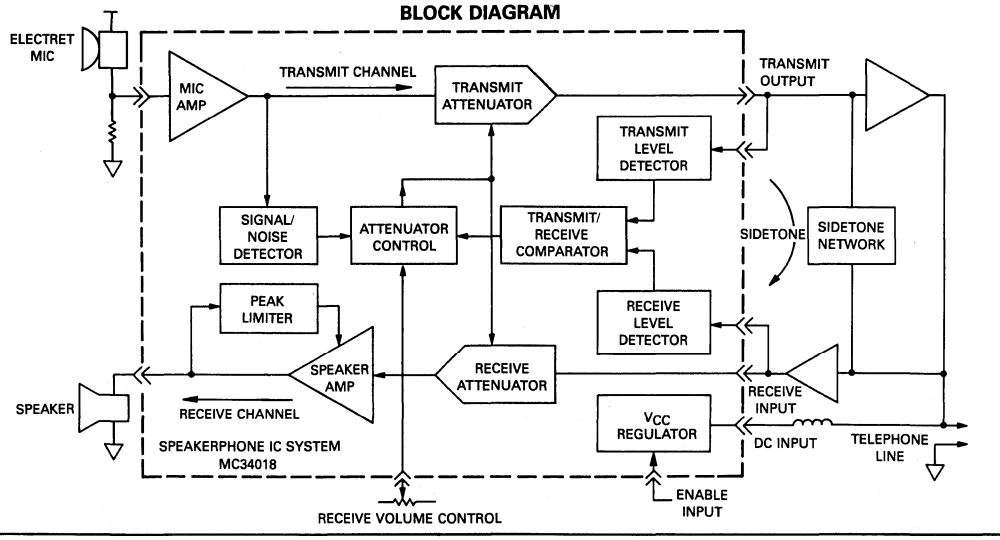


P SUFFIX
PLASTIC PACKAGE
CASE 710

DW SUFFIX
PLASTIC PACKAGE
CASE 751F
SO-28



BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Description
1	RR	A resistor to ground provides a reference current for the transmit and receive attenuators.
2	RTX	A resistor to ground determines the nominal gain of the transmit attenuator. The transmit channel gain is inversely proportional to the RTX resistance.
3	TXI	Input to the transmit attenuator. Input resistance is nominally 5.0 k ohms.
4	TXO	Output of the transmit attenuator. The TXO output signal drives the input of the transmit level detector, as well as the external circuit which drives the telephone line.
5	TLI	Input of the transmit level detector. An external resistor ac coupled to the TLI pin sets the detection level. Decreasing this resistor increases the sensitivity to transmit channel signals.
6	TLO	Output of the transmit level detector. The external resistor and capacitor set the time the comparator will hold the system in the transmit mode after speech ceases.
7	RLI	Input of the receive level detector. An external resistor ac coupled to the RLI pin sets the detection level. Decreasing this resistor increases the sensitivity to receive channel signals.
8	RLO	Output of the receive level detector. The external resistor and capacitor set the time the comparator will hold the system in the receive mode after the receive signal ceases.
9	MCI	Microphone amplifier input. Input impedance is nominally 10 k ohms and the dc bias voltage is approximately equal to VB.
10	MCO	Microphone amplifier output. The mic amp gain is internally set at 34 dB (50 V/V).
11	CP1	A parallel resistor and capacitor connected between this pin and V_{CC} holds a voltage corresponding to the background noise level. The transmit detector compares the CP1 voltage with the speech signal from CP2.
12	CP2	A capacitor at this pin peak detects the speech signals for comparison with the background noise level held at CP1.
13	XDI	Input to the transmit detector system. The microphone amplifier output is ac coupled to the XDI pin through an external resistor.
14	SKG	High current ground pin for the speaker amp output stage. The SKG voltage should be within 10 mV of the ground voltage at Pin 22.
15	SKO	Speaker amplifier output. The SKO pin will source and sink up to 100 mA when ac coupled to the speaker. The speaker amp gain is internally set at 34 dB (50 V/V).
16	V+	Input dc supply voltage. V+ can be powered from Tip and Ring if an ac decoupling inductor is used to prevent loading ac line signals. The required V+ voltage is 6.0 to 11 V (7.5 V nominal) at 7.0 mA.
17	AGC	A capacitor from this pin to VB stabilizes the speaker amp gain control loop, and additionally controls the attack and decay time of this circuit. The gain control loop limits the speaker amp input to prevent clipping at SKO. The internal resistance at the AGC pin is nominally 110 k ohms.
18	$\overline{CS}$	Digital chip select input. When at a Logic "0" (<0.7 V) the V_{CC} regulator is enabled. When at a Logic "1" (>1.6 V), the chip is in the standby mode drawing 0.5 mA. An open $\overline{CS}$ pin is a Logic "0". Input impedance is nominally 140 k ohms. The input voltage should not exceed 11 V.
19	SKI	Input to the speaker amplifier. Input impedance is nominally 20 k ohms.
20	V_{CC}	A 5.4 V regulated output which powers all circuits except the speaker amplifier output stage. V_{CC} can be used to power external circuitry such as a microprocessor (3.0 mA max). A filter capacitor is required. The MC34018 can be powered by a separate regulated supply by connecting V+ and V_{CC} to a voltage between 4.5 V and 6.5 V while maintaining $\overline{CS}$ at a Logic "1".
21	VB	An output voltage equal to approximately $V_{CC}/2$ which serves as an analog ground for the speakerphone system. Up to 1.5 mA of external load current may be sourced from VB. Output impedance is 250 ohms. A filter capacitor is required.
22	Gnd	Ground pin for the IC (except the speaker amplifier).
23	XDC	Transmit detector output. A resistor and capacitor at this pin hold the system in the transmit mode during pauses between words or phrases. When the XDC pin voltage decays to ground, the attenuators switch from the transmit mode to the idle mode. The internal resistor at XDC is nominally 2.6 k ohms (see Figure 1).
24	VLC	Volume control input. Connecting this pin to the slider of a variable resistor provides receive mode volume control. The VLC pin voltage should be less than or equal to VB.
25	ACF	Attenuator control filter. A capacitor connected to this pin reduces noise transients as the attenuator control switches levels of attenuation.
26	RXO	Output of the receive attenuator. Normally this pin is ac coupled to the input of the speaker amplifier.
27	RXI	Input of the receive attenuator. Input resistance is nominally 5.0 k ohms.
28	RRX	A resistor to ground determines the nominal gain of the receive attenuator. The receive channel gain is directly proportional to the RRX resistance.

Note: Pin numbers are identical for the DIP and SOIC packages.

ABSOLUTE MAXIMUM RATINGS

(Voltages referred to Pin 22) (T_A = 25°C)

Parameter	Value	Units
V+ Terminal Voltage (Pin 16)	+12, −1.0	V
$\overline{CS}$ (Pin 18)	+12, −1.0	V
Speaker Amp Ground (Pin 14)	+3.0, −1.0	V
VLC (Pin 24)	V_{CC}, −1.0	V
Storage Temperature	−65 to +150	°C

"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Electrical Characteristics" tables provide conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Value	Units
V+ Terminal Voltage (Pin 16)	+6.0 to +11	V
$\overline{CS}$ (Pin 18)	0 to +11	V
I_{CC} (Pin 20)	0 to 3.0	mA
VLC (Pin 24)	0.55VB to VB	V
Receive Signal (Pin 27)	0 to 250	mV_{rms}
Microphone Signal (Pin 9)	0 to 5.0	mV_{rms}
Speaker Amp Ground (Pin 14)	−10 to +10	mVdc
Ambient Temperature	−20 to +60	°C

ELECTRICAL CHARACTERISTICS (Refer to Figure 1)

Parameter	Symbol	Pin	Min	Typ	Max	Units
SUPPLY VOLTAGES						
V+ Supply Current	I_{V+}	16				
V+ = 11 V, Pin 18 = 0.7 V			—	—	9.0	mA
V+ = 11 V, Pin 18 = 1.6 V			—	—	800	μA
V_{CC} Voltage (V+ = 7.5 V)	V_{CC}	20	4.9	5.4	5.9	Vdc
Line Regulation (6.5 V < V+ < 11 V)	$\Delta V_{CC\ LN}$		—	65	150	mV
Output Resistance (I_{CC} = 3.0 mA)	R_{OVCC}		—	6.0	20	ohms
Dropout Voltage (V+ = 5.0 V)	$V_{CC\ SAT}$		—	80	300	mV
VB Voltage (V+ = 7.5 V)	V_B	21	2.5	2.9	3.3	Vdc
Output Resistance (IB = 1.7 mA)	R_{OVB}		—	250	—	ohms
ATTENUATORS						
Receive Attenuator Gain (@ 1.0 kHz)		26,				
Rx Mode, Pin 24 = VB; Pin 27 = 250 mV_{rms}	G_{RX}	27	2.0	6.0	10	dB
Range (Rx to Tx Modes)	ΔG_{RX}		40	44	48	dB
Idle Mode, Pin 27 = 250 mV_{rms}	G_{RXI}		−20	−16	−12	dB
RXO Voltage (Rx Mode)	V_{RXO}		1.8	2.3	3.2	Vdc
Delta RXO Voltage (Switch from RX to TX Mode)	ΔV_{RXO}		—	—	100	mV
RXO Sink Current (Rx Mode)	I_{RXOL}		75	—	—	μA
RXO Source Current (Rx Mode)	I_{RXOH}		1.0	—	3.0	mA
RXI Input Resistance	R_{RXI}		3.5	5.0	8.0	kΩ
Volume Control Range (Rx Attenuator Gain, Rx Mode, 0.6 VB < Pin 24 < VB)	V_{CR}		24.5	—	32.5	dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin	Min	Typ	Max	Units
ATTENUATORS						
Transmit Attenuator Gain (@ 1.0 kHz)		3,				
Tx Mode, Pin 3 = 250 mV_{rms}	G_{TX}	4	4.0	6.0	8.0	dB
Range, (Tx to Rx Mode)	ΔG_{TX}		40	44	48	dB
Idle Mode, Pin 3 = 250 mV_{rms}	G_{TXI}		−16.5	−13	−8.5	dB
TXO Voltage (Tx Mode)	V_{TXO}		1.8	2.3	3.2	Vdc
Delta TXO Voltage (Switch from Tx to Rx Mode)	ΔV_{TXO}		—	—	100	mV
TXO Sink Current (Tx Mode)	I_{TXOL}		75	—	—	μA
TXO Source Current (Tx Mode)	I_{TXOH}		1.0	—	3.0	mA
TXI Input Resistance	R_{TXI}		3.5	5.0	8.0	kΩ
ACF Voltage (V_{CC} − Pin 25 Voltage)	ΔV_{ACF}	20,				
Rx Mode		25	—	150	—	mV
Rx Mode			—	6.0	—	mV
Idle Mode			—	75	—	mV
SPEAKER AMPLIFIER						
Speaker Amp Gain (Pin 19 = 20 mV_{rms})	G_{SPK}	15, 19	33	34	35	dB
SKI Input Resistance	R_{SKI}		15	22	37	kΩ
SKO Voltage (Pin 19 = Cap Couple to GND)	V_{SKO}		2.4	3.0	3.6	Vdc
SKO High Voltage (Pin 19 = 0.1 V, −100 mA load at Pin 15)	V_{SKOH}		5.5	—	—	Vdc
SKO Low Voltage (Pin 19 = −0.1 V, +100 mA load at Pin 15)	V_{SKOL}		—	—	600	mV
MICROPHONE AMPLIFIER						
Mike Amp Gain (Pin 9 = 10 mV_{rms}, 1.0 kHz)	G_{MCI}	9, 10	32.5	34	35	dB
Mike Amp Input Resistance	R_{MCI}		6.5	10	16	kΩ
LOGAMPS						
RLO Leakage Current (Pin 8 = VB + 1.0 V)	I_{LKRLO}	8	—	—	2.0	μA
TLO Leakage Current (Pin 6 = VB + 1.0 V)	I_{LKTLO}	6	—	—	2.0	μA
Transmit-Receive Switching Threshold (Ratio of ITLI to IRLI — at 20 μA — to switch Tx-Rx Comparator)	I_{TH}	5,7 25	0.8	—	1.2	
TRANSMIT DETECTOR						
XDC Voltage — Idle Mode	V_{XDC}	23	—	0	—	Vdc
Tx Mode			—	4.0	—	Vdc
CP2 Current Source	I_{CP2}	12	5.0	10	13	μA
DISTORTION						
Rx Mode — RXI to SKO (Pin 27 = 10 mV_{rms}, 1.0 kHz)	R_{XD}	27, 15	—	1.5	—	%
Tx Mode — MCI to TXO (Pin 9 = 5.0 mV_{rms}, 1.0 kHz)	T_{XD}	4,9	—	2.0	—	%

NOTES: 1. V+ = 7.5 V, $\overline{CS}$ = 0.7 V except where noted.
2. Rx Mode: Pin 7 = −100 μA, Pin 5 = +100 μA, except where noted.
Tx Mode: Pin 5, 13 = −100 μA, Pin 7 = +100 μA, Pin 11 = 0 volts.
Idle Mode: Pin 5 = −100 μA, Pin 7, 13 = +100 μA.
3. Current into a pin designated as +; current out of a pin designated as −
4. Voltages referred to Pin 22. T_A = +25°C.

TEMPERATURE CHARACTERISTICS (−20 to +60°C)

Parameter	Pin	Typical Change	Units
V+ Supply Current (V+ = 11 V, Pin 18 = 0.7 V)	16	−0.2	%/°C
V+ Supply Current (V+ = 11 V, Pin 18 = 1.6 V)	16	−0.4	%/°C
V_{CC} Voltage (V+ = 7.5 V)	20	+0.1	%/°C
Attenuator Gain (Max and Min Settings)		±0.003	dB/°C
Delta RXO, TXO Voltages	4,26	±0.24	%/°C
Speaker Amp Gain	15,19	±0.003	dB/°C
Microphone Amp Gain	9,10	±0.001	dB/°C
Microphone Amp Input Resistance	9	+0.4	%/°C
Tx-Rx Switching Threshold (@ 20 μA)	5,7	±0.2	nA/°C

DESIGN GUIDELINES (Refer to Figure 1)

ATTENUATORS

The transmit and receive attenuators are complementary in function, i.e., when one is at maximum gain the other is at maximum attenuation, and vice versa. They are never both on or both off. Their main purpose is to control the transmit and receive paths to provide the half-duplex operation required of a speakerphone. The attenuators are controlled solely by the voltage at the ACF pin (Pin 25). The ACF voltage is provided by the Attenuator Control block, which receives 3 inputs: a) the Rx-Tx Comparator, b) the Transmit Detector Comparator, and c) the Volume Control. The response of the attenuators is based on the difference of the ACF voltage from V_{CC}, and therefore a simple method for monitoring the circuit operation is to monitor this voltage difference (referred to as ΔVacf). If ΔVacf is approximately 6 millivolts the transmit attenuator is fully on and the receive attenuator is fully off (transmit mode). If ΔVacf is approximately 150 millivolts the circuit is in the receive mode. If ΔVacf is approximately 75 millivolts, the circuit is in the idle mode, and the two attenuators are at gain settings approximately half way (in dB) between their fully on and fully off positions.

The maximum gain and attenuation values are determined by the three resistors RR, RTX, and RRX (Refer to Figures 2, 3 and 4). RR affects both attenuators according to its value RELATIVE to RTX and RRX, which is why Figure 4 indicates the variations versus the ratio of the other resistors to RR. (GRX and GTX are the maximum gains, and ARX and ATX are the maximum attenuations). RTX affects the gain and attenuation of only the transmit attenuator according to the curves of Figure 2, while RRX affects only the receive attenuator according to Figure 3. As can be seen from the figures, the gain difference (from on to off) is a reasonably constant 45 dB until the upper gain limit is approached. A value of 30 k is recommended for RR as a starting point, and then RTX and RRX selected to suit the particular design goals.

The input impedance of the attenuators (at TXI and RXI) is typically 5.0 kΩ, and the maximum input signal which will not cause output distortion is 250 mV_{rms} (707 mVp-p). The 4300 ohm resistor and 0.01 μF capacitor at RXO (in Figure 1) filters out high frequency components in the receive path. This helps minimize high frequency acoustic feedback problems which may occur if the filter were not present. The filter's insertion loss is 1.5 dB at 1.0 kHz. The outputs of the attenuators are inverted from their inputs.

Referring to the attenuator control block, the ΔVacf voltage at its output is determined by three inputs. The relationship of the inputs and output is summarized in the following truth table:

Tx-Rx Comp	Transmit Det Comp	Volume Control	ΔVacf	Mode
Transmit	Transmit	No Effect	6.0 mV	Transmit
Transmit	Idle	No Effect	75 mV	Idle
Receive	Transmit	Affects ΔVacf	50–150 mV	Receive
Receive	Idle	Affects ΔVacf	50–150 mV	Receive

As can be seen from the truth table, the Tx-Rx comparator dominates. The Transmit Detector Comparator is effective only in the transmit mode, and the Volume Control is effective only in the receive mode.

The Tx-Rx comparator is in the transmit position when there is sufficient transmit signal present over and above any receive signal. The Transmit Detector Comparator then determines whether the transmit signal is a result of background noise (a relatively stable signal), or speech which consists of bursts. If the signal is due to background noise, the attenuators will be put into the idle mode (ΔVacf = 75 mV). If the signal consists of speech, the attenuators will be switched to the transmit mode (ΔVacf = 6.0 mV.) A further explanation of this function will be found in the section on the Transmit Detector Circuit.

The Tx-Rx comparator is in the receive position when there is sufficient receive signal to overcome the background noise **AND** any speech signals. The ΔVacf voltage will now be 150 mV **IF** the volume control is at the maximum position, i.e. VLC (Pin 24) = VB. IF VLC is less than VB, the gain of the receive attenuator, and the attenuation of the transmit attenuator, will vary in a complementary manner as shown in Figure 5. It can be seen that at the minimum recommended operating level (VLC = 0.55 VB) the gain of the transmit attenuator is actually greater than that of the receive attenuator. The effect of varying VLC is to vary ΔVacf, with a resulting variation in the gains of the attenuators. Figure 6 shows the gain variations with ΔVacf.

The capacitor at ACF (Pin 25) smooths the transition between operating modes. This keeps down any "clicks" in the speaker or transmit signal when the ACF voltage switches.

The gain separation of the two attenuators can be reduced from the typical 45 dB by adding a resistor between Pins 20 (V_{CC}) and 25 (ACF). The effect is a reduction of the maximum ΔVacf voltage in the receive mode, while not affecting ΔVacf in the transmit mode. As an example, adding a 12 kΩ resistor will reduce ΔVacf by approximately 15 mV (to 135 mV), decrease the gain of the receive attenuator by approximately 5.0 dB, and increase the gain of the transmit attenuator by a similar amount. If the circuit requires the receive attenuator gain to be +6.0 dB in the receive mode, RRX must be adjusted (to ≈ 27 k) to re-establish this value. This change will also increase the receive attenuator gain in the transmit mode by a similar amount. The resistor at TLI may also require changing to reset the sensitivity of the transmit level detector.

LOG AMPLIFIERS
(Transmit and Receive Level Detectors)

The log amps monitor the levels of the transmit and receive signals, so as to tell the Tx-Rx comparator which mode should be in effect. The input signals are applied to the amplifiers (at TLI and RLI) through AC coupling capacitors and current limiting resistors. The value of these components determines the sensitivity of the respective amplifiers, and has an effect on the switching times between transmit and receive modes. The feedback elements for the amplifiers are back-to-back diodes which provide a logarithmic gain curve, thus allowing operation over a wide range of signal levels. The outputs of the amplifiers are rectified, having a quick rise time and a slow decay time. The rise time is determined primarily by the external capacitor (at TLO or RLO) and an internal 500 ohm resistor, and is on the order of a fraction of a millisecond. The decay time is determined by the external resistor and capacitor, and is on the order of a fraction of a second. The switching time is not fixed, but depends on the relative values of the transmit and receive signals, as well as these external components. Figure 7 indicates the dc transfer characteristics of the log amps, and Figure 8 indicates the transfer characteristics with respect to an ac input signal. The dc level at TLI, RLI, TLO, and RLO is approximately VB.

The Tx-Rx comparator responds to the voltages at TLO and RLO, which in turn are functions of the currents sourced out of TLI and RLI, respectively. If an offset at the comparator input is desired, e.g., to prevent noise from switching the system, or to give preference to either the transmit or receive channel, this may be achieved by biasing the appropriate input (TLI or RLI). A resistor to ground will cause a DC current to flow out of that input, thus forcing the output of that amplifier to be biased slightly higher than normal. This amplifier then becomes the preferred one in the system operation. Resistor values from 500 k to 10 M ohms are recommended for this purpose.

SPEAKER AMPLIFIER

The speaker amplifier has a fixed gain of 34 dB (50 V/V), and is noninverting. The input impedance is nominally 22 kΩ as long as the output signal is below that required to activate the Peak Limiter. Figure 9 indicates the typical output swing available at SKO (Pin 15). Since the output current capability is 100 mA, the lower curve is limited to a 5.0 volt swing. The output impedance depends on the output signal level and is relatively low as long as the signal level is not near the maximum limits. At 3 volts p-p the output impedance is <0.5 ohms, and at 4.5 volts p-p it is <3 ohms. The output is short circuit protected at approximately 300 mA.

When the amplifier is overdriven, the peak limiter causes a portion of the input signal to be shunted to ground, in order to maintain a constant output level. The effect is that of a gain reduction caused by a reduction of the input impedance (at SKI) to a value not less than 2.0 kΩ.

The capacitor at Pin 17 (AGC) determines the response time of the peak limiter circuit. When a large input signal is applied to SKI, the voltage at AGC (Pin 17) will drop quickly as a current source is applied to the external capacitor. When the large input signal is reduced, the current source is turned off, and an internal 110 kΩ resistor discharges the capacitor so the voltage at AGC can return to its normal value (1.9 Vdc). The capacitor additionally stabilizes the peak limiting feedback loop.

If there is a need to mute the speaker amplifier without disabling the rest of the circuit, this may be accomplished by connecting a resistor from the AGC pin to ground. A 100 kΩ resistor will reduce the gain by 34 dB (0 dB from SKI to SKO), and a 10 k resistor will reduce the gain by almost 50 dB.

TRANSMIT DETECTOR CIRCUIT

The transmit detector circuit, also known as the background noise monitor, distinguishes speech (which consists of bursts) from the background noise (a relatively constant signal). It does this by storing a voltage level, representative of the average background noise, in the capacitor at CP1 (Pin 11). The resistor and capacitor at this pin have a time constant of approximately 5 seconds (in Figure 1). The voltage at Pin 11 is applied to the inverting input of the Transmit Detector Comparator. In the absence of speech signals, the noninverting input receives the same voltage level minus an offset of 36 mV. In this condition, the output of the comparator will be low, the output transistor turned off, and the voltage at XDC (Pin 23) will be at ground. If the Tx-Rx comparator is in the transmit position, the attenuators will be in the idle mode (ΔVacf = 75 mV). When speech is presented to the microphone, the signal burst appearing at XDI reaches the noninverting input of the transmit detector comparator before the voltage at the inverting input can change, causing the output to switch high, driving the voltage at XDC up to approximately 4 volts. This high level causes the attenuator control block to switch the attenuators from the idle mode to the transmit mode (assuming the Tx-Rx comparator is in

the transmit mode). As long as the speech continues to arrive, and is maintained at a level above the background, the voltage at XDC will be maintained at a high level, and the circuit will remain in the transmit mode. The time constant of the components at XDC will determine how much time the circuit requires to return to the idle mode after the cessation of microphone speech signals, such as occurs during the normal pauses in speech.

The series resistor and capacitor at XDI (Pin 13) determine the sensitivity of the transmit detector circuit. Figure 10 indicates the change in DC voltage levels at CP2 and CP1 in response to a steady state sine wave applied at the input of the 0.068 μF capacitor and 4700 ohm resistor (the voltage change at CP1 is 2.7 times greater than the change at CP2). Increasing the resistor, or lowering the capacitor, will reduce the response at these pins. The first amplifier (between XDI and CP2) is logarithmic in order that this circuit be able to handle a wide range of signal levels (or in other words, it responds equally well to people who talk quietly and to people who shout). Figure 7 indicates the dc transfer characteristics of the log amp.

Figure 11 indicates the response at Pins 11, 12, and 23 to a varying signal at the microphone. The series of events in Figure 11 is as follows:

1) CP2 (Pin 12) follows the peaks of the speech signals, and decays at a rate determined by the 10 μA current source and the capacitor at this pin.

2) CP1 (Pin 11) increases at a rate determined by the RC at this pin after CP2 has made a positive transition. It will follow the decay pattern of CP2.

3) The noninverting input of the Transmit Detector Comparator follows CP2, gained up by 2.7, and reduced by an offset of 36 mV. This voltage, compared to CP1, determines the output of the comparator.

4) XDC (Pin 23) will rise quickly to 4 Vdc in response to a positive transition at CP2, but will decay at a rate determined by the RC at this pin. When XDC is above 3.25 Vdc, the circuit will be in the transmit mode. As it decays towards ground, the attenuators are taken to the idle mode.

MICROPHONE AMPLIFIER

The microphone amplifier is noninverting, has an internal gain of 34 dB (50 V/V), and a nominal input impedance of 10 kΩ. The output impedance is typically <15 ohms. The maximum p-p voltage swing available at the output is approximately 2.0 volts less than V_{CC}, which is substantially more than what is required in most applications. The input at MCI (Pin 9) should be ac coupled to the microphone so as to not upset the bias voltage. Generally, microphone sensitivity may be adjusted by varying the 2 k microphone bias resistor, rather than by attempting to vary the gain of the amplifier.

POWER SUPPLY

The voltage supply for the MC34018 at V+ (Pin 16) should be in the range of 6.0 to 11 volts, although the circuit will operate down to 4.0 volts. The voltage can be supplied either from Tip and Ring, or from a separate supply. The required supply current, with no signal to the speaker, is shown in Figure 12. The upper curve indicates the normal operating current when Chip Select (Pin 18) is at a Logic "0". Figure 13 indicates the average dc current required when supplying various power levels to a 25 ohm speaker. Figure 13 also indicates the minimum supply voltage required to provide the indicated power levels. The peak in the power supply current at 5.0–5.4 volts occurs as the V_{CC} circuit comes into regulation.

It is imperative that the V+ supply (Pin 16) be a good ac ground for stability reasons. If this pin is not well filtered (by a 1000 μF capacitor AT THE IC), any variation at V+ caused by the required speaker current flowing through this pin can cause a low frequency oscillation. The result is usually that the circuit will cut the speaker signal on and off at the rate of a few hertz. Experiments have shown that only a few inches of wire between the supply and the IC can cause the problem if the filter capacitor is not physically adjacent to the IC. It is equally imperative that both ground pins (Pins 14 and 22) have a low loss connection to the power supply ground.

V_{CC}

V_{CC} (Pin 20) is a regulated output voltage of 5.4 volts, +/−0.5 V. Regulation will be maintained as long as V+ is (typically) 80 mV greater than the regulated value of V_{CC}. Up to 3 milliamps can be sourced from this supply for external use. The output impedance is <20 ohms.

The 47 μF capacitor indicated for connection to Pin 20 is essential for stability reasons. It must be located adjacent to the IC.

If the circuit is deselected (see section on Chip Select), the V_{CC} voltage will go to 0 volts.

If the MC34018 is to be powered from a regulated supply (not the Tip and Ring lines) of less than 6.5 volts, the configuration of Figure 14 may be used so as to ensure that V_{CC} is regulated. The regulated voltage is applied to both V+ and V_{CC}, with $\overline{CS}$ held at a Logic "1" so as to turn off the internal regulator (the Chip Select function is not available when the circuit is used in this manner). Figure 15 indicates the supply current used by this configuration, with no signal at the speaker. When a signal is sent to the speaker, the curves of Figure 13 apply.

VB

VB is a regulated output voltage with a nominal value of 2.9 volts, +/−0.4 volts. It is derived from V_{CC} and tracks it, holding a value of approximately 54% of V_{CC}. 1.5 milliamps can be sourced from this supply at a typical output impedance of 250 ohms.

The 47 μF capacitor indicated for connection to the VB pin is required for stability reasons, and must be adjacent to the IC.

If the circuit is deselected (see section on Chip Select), the VB voltage will go to 0 volts.

CHIP SELECT

The Chip Select pin (Pin 18) allows the chip to be powered down anytime its functions are not required. A Logic "1" level in the range of 1.6 V to 11 V deselects the chip, and the resulting supply current (at V+) is shown in Figure 12. The input resistance at Pin 18 is >75 kΩ. The V_{CC} and VB regulated voltages go to 0.0 when the chip is deselected. Leaving Pin 18 open is equivalent to a Logic "0" (chip enabled).

FIGURE 1 — TEST CIRCUIT

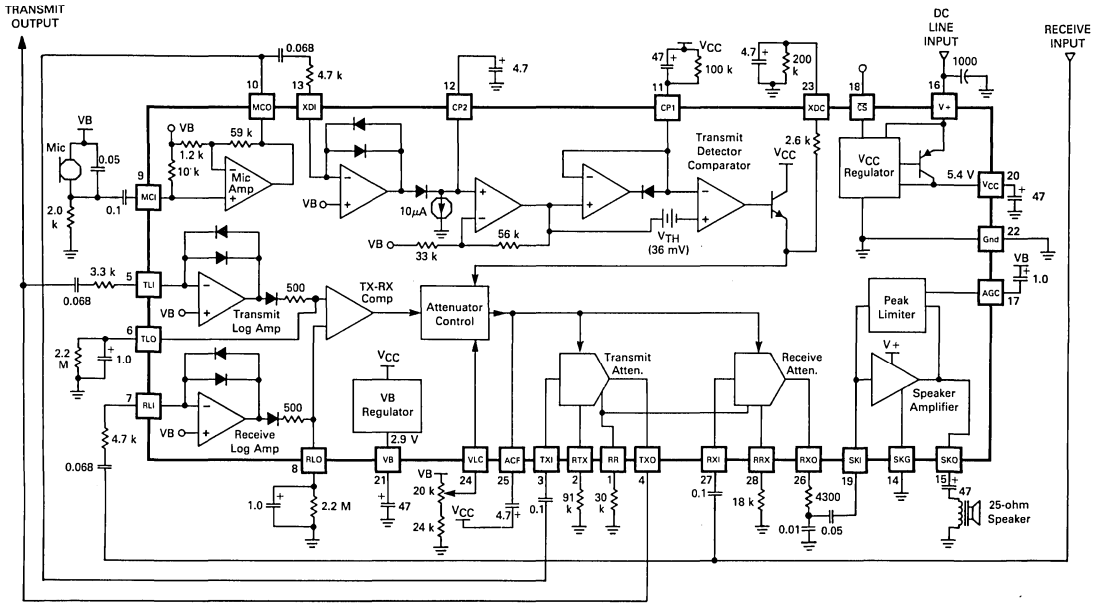


FIGURE 2 — TRANSMIT ATTENUATOR versus RTX

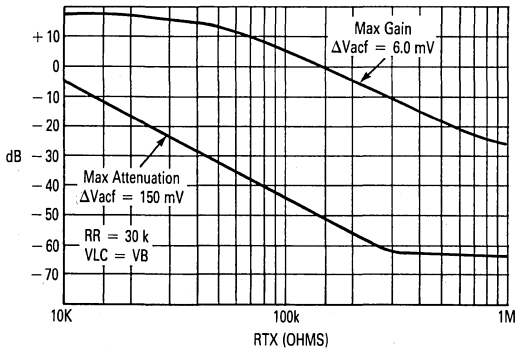


FIGURE 3 — RECEIVE ATTENUATOR versus RRX

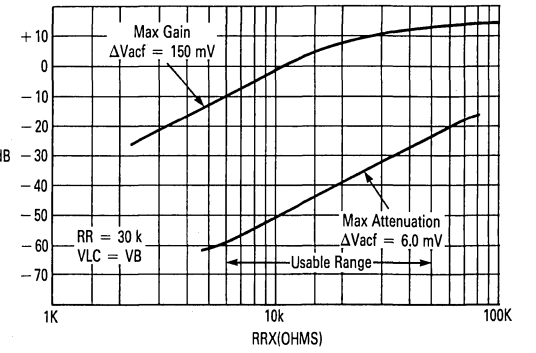


FIGURE 4 — GAIN AND ATTENUATION versus RESISTOR RATIOS

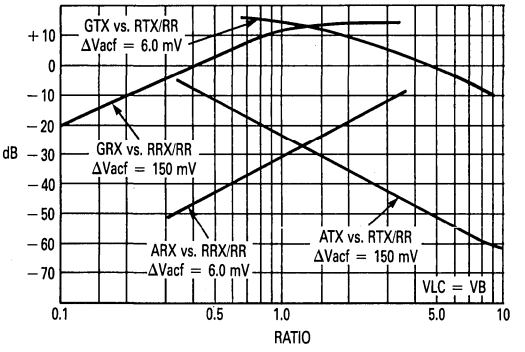


FIGURE 5 — ATTENUATOR GAIN versus VLC

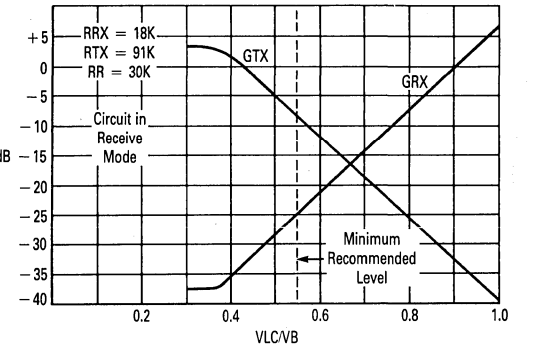


FIGURE 6 — ATTENUATOR GAIN versus ΔVacf

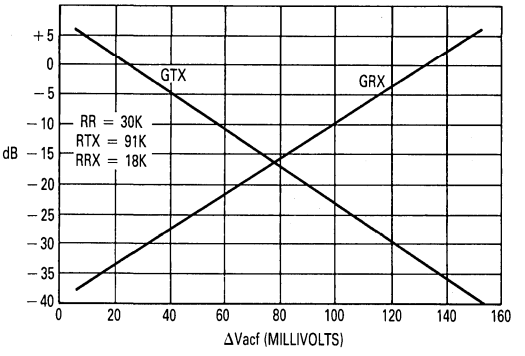


FIGURE 7 — LOG AMP TRANSFER CHARACTERISTICS

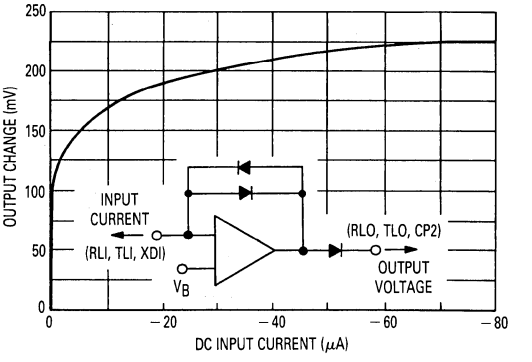


FIGURE 8 — LOG AMP TRANSFER CHARACTERISTICS

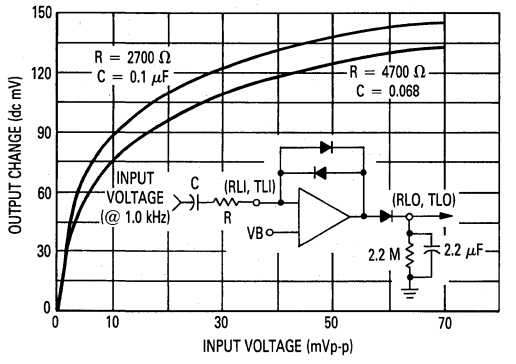


FIGURE 9 — SPEAKER AMP OUTPUT versus SUPPLY VOLTAGE

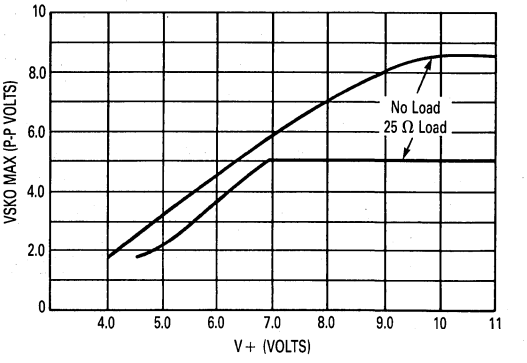


FIGURE 10 — RESPONSE AT CP2 AND CP1

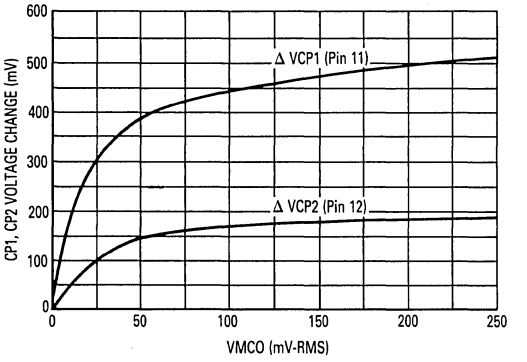


FIGURE 11 — TRANSMIT DETECTOR OPERATION

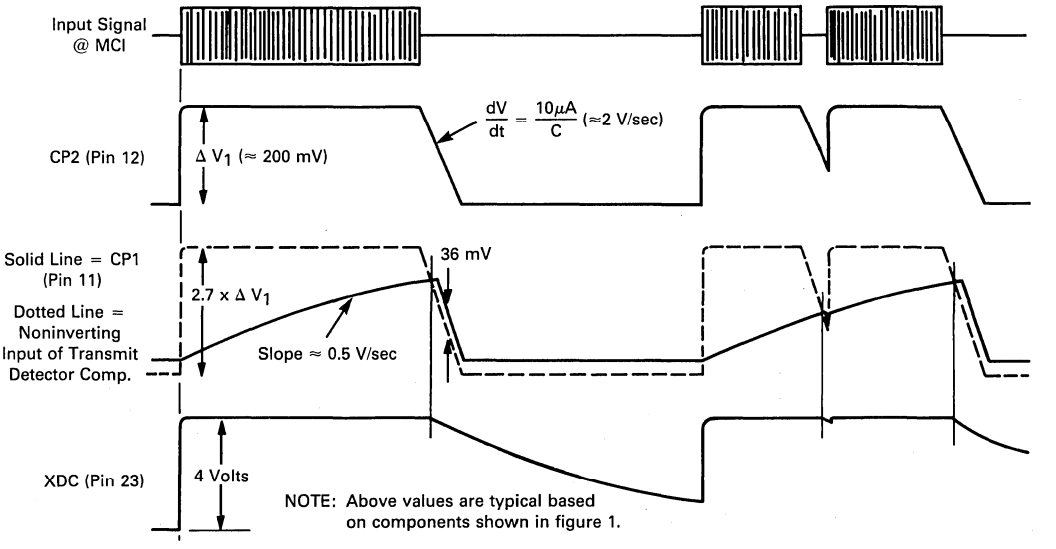


FIGURE 12 — SUPPLY CURRENT versus SUPPLY VOLTAGE

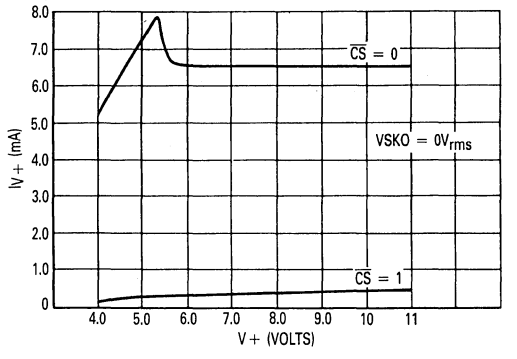


FIGURE 13 — SUPPLY CURRENT
versus SUPPLY VOLTAGE versus SPEAKER POWER

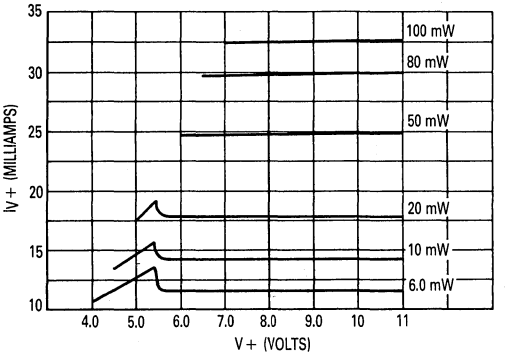


FIGURE 14 — ALTERNATE POWER SUPPLY CONFIGURATION

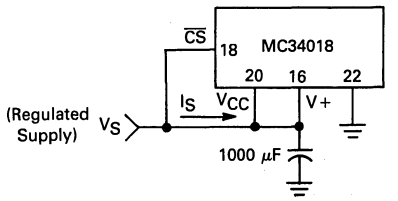
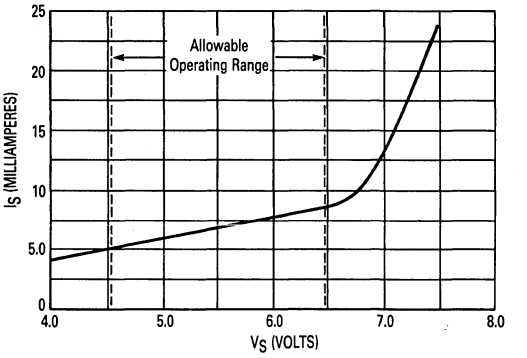


FIGURE 15 — SUPPLY CURRENT versus SUPPLY VOLTAGE (SEE FIGURE 14)



SWITCHING TIME

The switching times of the speakerphone circuit depend not only on the various external components, but also on the operating condition of the circuit at the time a change is to take effect. For example, the switching time from idle to transmit is generally quicker than the switching time from receive to transmit (or transmit to receive).

The components which most significantly affect the timing between the transmit and receive modes are those at Pins 5 (transmit turn-on), 6 (transmit turn-off), 7 (receive turn-on), and 8 (receive turn-off). These four timing functions are not independent, but interact since the Tx-Rx comparator operates on a RELATIVE Tx-Rx comparison, rather than on absolute values. The components at Pins 11, 12, 13, and 23 affect the timing from the transmit to the idle mode. Timing from the idle mode to transmit mode is relatively quick (due to the quick charging of the various capacitors), and is not greatly affected by the component values. Pins 5–8 do not affect the idle-to-transmit timing since the Tx-Rx comparator must already be in the transmit mode for this to occur.

The following table provides a summary of the effect on the switching time of the various components, including the volume control:

Additionally, the following should be noted:

1) The RCs at Pins 5 and 7 have a dual function in that they affect the sensitivity of the respective log amplifiers, or in other words, how loud the speech must be in order to gain control of the speakerphone circuit.

2) The RC at Pin 13 also has a dual function in that it determines the sensitivity of the transmit detector circuit.

3) The volume control affects the switching speed, and the relative response to transmit signals, in the following manner: When the circuit is in the receive mode, reducing the volume control setting increases the signal at TXO, and consequently the signal to the TLI pin. Therefore a given signal at TXI will switch the circuit into the transmit mode quicker at low volume settings.

The photographs of Figures 16 and 17 indicate experimentally obtained switching response times for the circuit of Figure 1. In Figure 16, the circuit is provided a continuous receive signal of 1.1 mVp-p at RXI (trace #3). A repetitive burst signal of 7.2 mVp-p, lasting 120

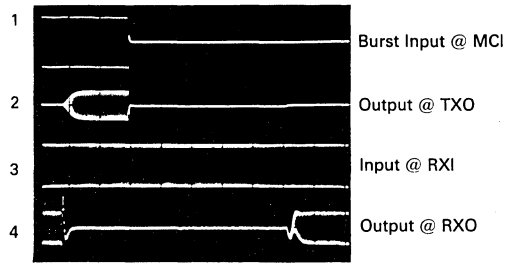
Components	Tx to Rx	Rx to Tx	Tx to Idle
RC @ Pin 5	Moderate	Significant	No effect
RC @ Pin 6	Significant	Moderate	No effect
RC @ Pin 7	Significant	Moderate	No effect
RC @ Pin 8	Moderate	Significant	No effect
RC @ Pin 11	No effect	Slight	Moderate
C @ Pin 12	No effect	Slight	Significant
RC @ Pin 13	No effect	Slight	Slight
RC @ Pin 23	No effect	Slight	Significant
V @ Pin 24	No effect	Moderate	No effect
C @ Pin 25	Moderate	Moderate	Slight

milliseconds, and repeated every 1 second, is applied to MCI (Trace #1). Trace #2 is the output at TXO, and is approximately 650 mVp-p at its maximum. Trace #4 is the output at RXO, and is approximately 2.2 mVp-p at its maximum. The time to switch from the receive mode to the transmit mode is approximately 40 ms, as indicated by the time required for TXO to turn on, and for RXO to turn off. After the signal at MCI is shut off, the switching time back to the receive mode is approximately 210 ms.

In Figure 17, a continuous signal of 7.6 mVp-p is applied to MCI (Trace #1), and a repetitive burst signal of 100 mVp-p is applied to RXI (Trace #3), lasting approximately 120 ms, and repeated every 1 second. Trace #2 is the output at TXO and is approximately 90 mVp-p at its maximum, and Trace #4 indicates the output at RXO, and is approximately 150 mVp-p at its maximum. In this sequence, the circuit switches between the idle and receive modes. The time required to switch from idle to receive is approximately 70 ms, as indicated by the first part of Traces 2 and 4. After the receive signal is shut off, the time to switch back to the idle mode is approximately 100 ms.

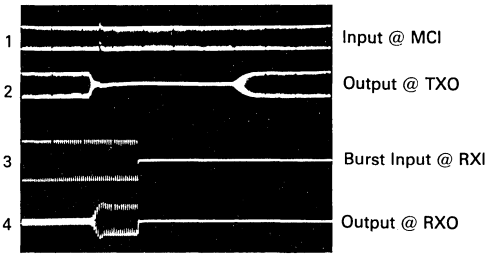
All of the above mentioned times will change significantly by varying the amplitude of the input signals, as well as by varying the external components.

FIGURE 16 — TRANSMIT-RECEIVE SWITCHING



Time Base = 40 ms/Div

FIGURE 17 — IDLE-RECEIVE SWITCHING



Time Base = 30 ms/Div

APPLICATIONS INFORMATION

The MC34018 Speakerphone IC is designed to provide the functions additionally required when a speakerphone is added to a standard telephone. The IC provides the necessary relative level detection and comparison of the speech signals provided by the talkers at the speakerphone (near end speaker) and at the distant telephone (far end speaker).

The MC34018 is designed for use with an electret type microphone, a 25 ohm speaker, and has an output power capability of (typically) 100 mW. All external components surrounding this device are passive, however, this IC does require additional circuitry to interface to the Tip and Ring telephone lines. Two suggested circuits are shown in this data sheet.

Figure 18 depicts a circuit using the MC34014 Speech Network (to provide the line interface), as well as the circuitry necessary to switch between the handset mode and the speakerphone mode. Switch HS (containing one normally open and one normally closed contact) is the hook switch actuated by the handset, shown in the on-hook position. When the handset is off-hook (HS1 open, HS2 closed), power is applied to the MC34014 speech network, and consequently the handset, and the $\overline{CS}$ pin of the MC34018 is held high so as to disable it. Upon closing the two poles of switch SS, **AND** placing switch HS in the on-hook position, power is then applied to both the MC34014 and the MC34018, and $\overline{CS}$ is held low, enabling the speakerphone function. Anytime the handset is removed from switch HS, the circuit reverts to the handset mode. The diode circuitry sets the operational mode of the MC34014 so as to optimize the speakerphone operation (see the MC34014 data sheet for further details). The tone dialer interface is meant for connection to a DTMF dialer with an active low MUTE signal. The V_{DD} supply from the MC34014 is a nominal 3.3 volts. The MC34017 and piezo sounder provide the ringing function.

Figure 19 depicts a configuration which does not include a handset, dialer, or ringer. The only controls are S1 (to make the connection to the line), S2 (a "privacy" switch), and the volume control. It is meant to be used in parallel with a normal telephone which has the dialing and ringing functions.

Figure 20 depicts a means of providing logic level signals that indicate which mode of operation the MC34018 is in. Comparator A indicates whether the circuit is in the receive or transmit/idle mode, and comparator B indicates (when in the transmit/idle mode) whether the circuit is in the transmit or idle mode. The LM393 dual comparator was chosen because of its low current requirement (<1.0 mA), low voltage requirement (as low as 2.0 volts), and low cost.

FIGURE 18 — SWITCHABLE HANDSET/HANDSFREE SYSTEM

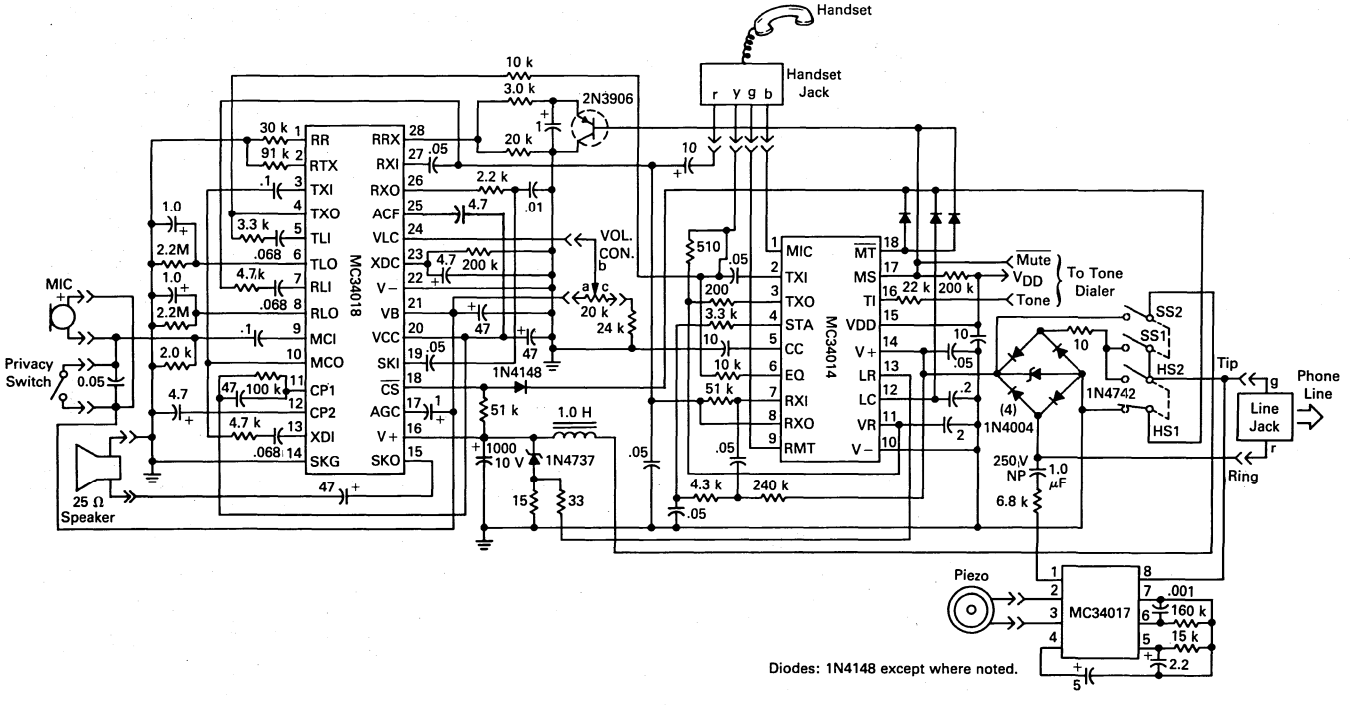
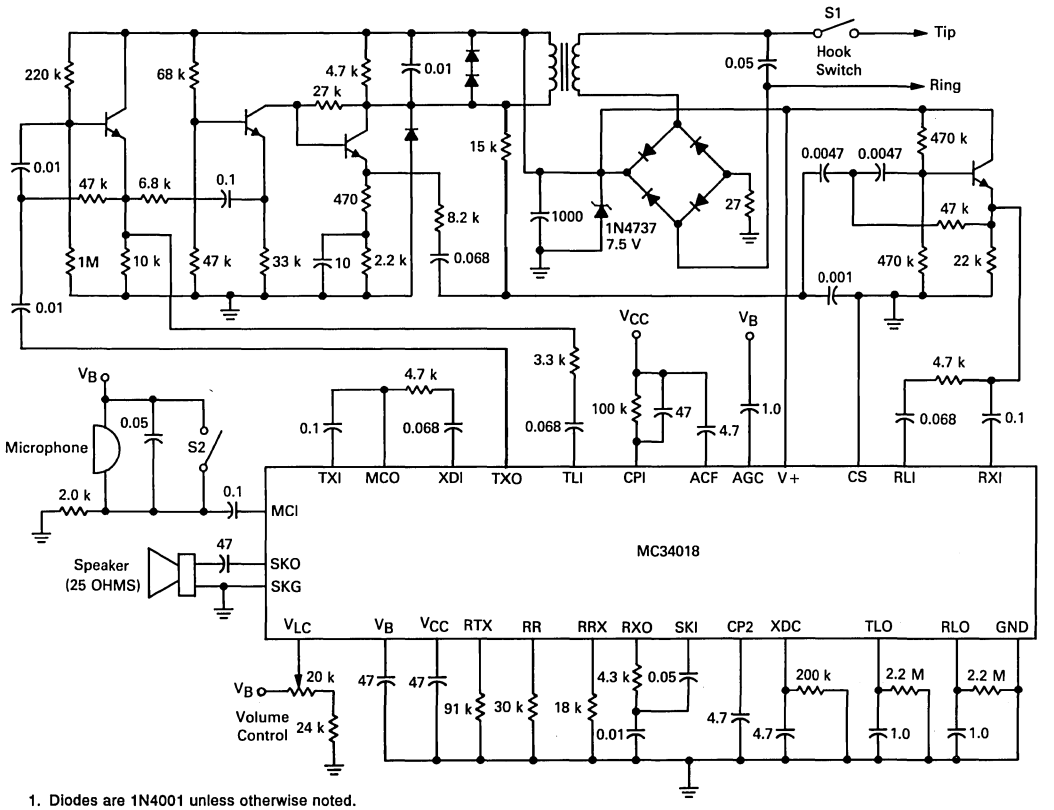
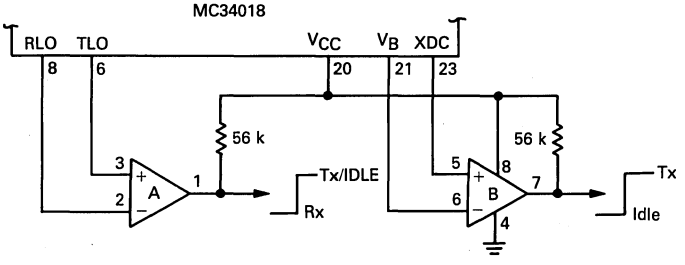


FIGURE 19 — BASIC LINE POWERED SPEAKERPHONE



1. Diodes are 1N4001 unless otherwise noted.
2. 4 Transistors are 2N3904.
3. Recommended Transformer: Microtran T5115.

FIGURE 20 — DIGITAL TRANSMIT/IDLE/RECEIVE INDICATION



Comparators A & B = LM393 (Dual)

MC34114

Specifications and Applications Information

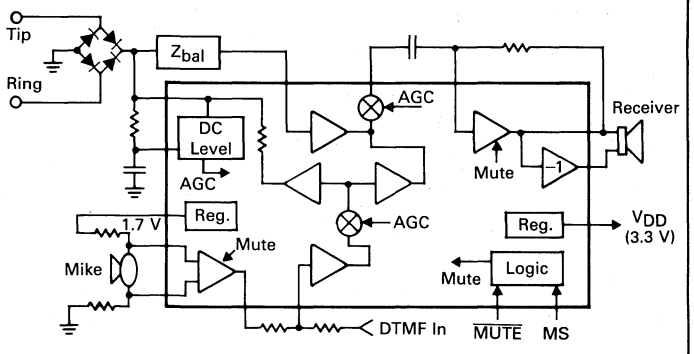
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

The MC34114 is a monolithic integrated telephone speech network designed to replace the bulky magnetic hybrid circuit of a telephone set. The MC34114 incorporates the necessary functions of transmit amplification, receive amplification, and sidetone control, each with externally adjustable gain. Loop length equalization varies the gains based on loop current. The microphone amplifier has a balanced, differential input stage designed to reduce RFI problems. A $\overline{\text{MUTE}}$ input mutes the microphone and receive amplifiers during dialing. A regulated output voltage is provided for biasing of the microphone, and a separate output voltage powers an external dialer, microprocessor, or other circuitry. The MC34114 is designed to operate at a minimum of 1.2 volts, making party line operation possible.

A circuit using the MC34114 can be made to comply with Bell Telephone, British Telecom (BT), and NTT (Nippon Telegraph & Telephone) standards. It is available in a standard 18-pin DIP, and a 20-pin SOIC (surface mount) package.

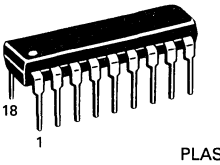
- Operation Down to 1.2 Volts
- Externally Adjustable Transmit, Receive, and Sidetone Gains
- Differential Microphone Amplifier Input Minimizes RFI Susceptibility
- Transmit, Receive, and Sidetone Equalization on Both Voice and DTMF Signals
- Regulated 1.7 Volts Output for Biasing Microphone
- Regulated 3.3 Volts Output for Powering External Dialer or MPU
- Microphone and Receive Amplifiers Muted During Dialing
- Differential Receive Amplifier Output Eliminates Coupling Capacitor
- Operates with Receiver Impedances of 50 Ohms and Higher
- Complies with NTT, Bell Telephone and BT Standards

SIMPLIFIED BLOCK DIAGRAM

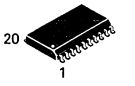


TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

SILICON MONOLITHIC INTEGRATED CIRCUIT

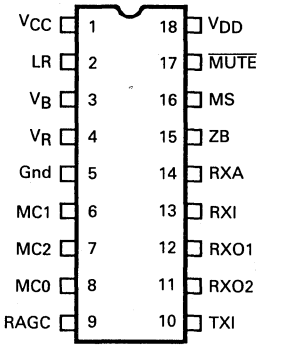


P SUFFIX
PLASTIC PACKAGE
CASE 707



DW SUFFIX
PLASTIC PACKAGE
CASE 751D

PIN CONNECTIONS
(Top View)
(DIP Package)



ORDERING INFORMATION

Package	Part No.
18-Pin Plastic DIP	MC34114P
20-Pin Surface Mount	MC34114DW

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
V_{CC} Supply Voltage	−1.0, +12	Vdc
Voltage at V_{DD} (Externally Applied, V_{CC} = 0)	−1.0, +6.0	Vdc
Voltage at $\overline{MUTE}$, MS (V_{CC} > 1.5 Volts)	−1.0, V_{DD} + 0.5	Vdc
Voltage at $\overline{MUTE}$, MS (V_{CC} = 0)	−1.0, +6.0	Vdc
Voltage at RAGC (0 < V_{CC} < 12 Volts)	−1.0, +6.0	Vdc
Current through V_{CC}, LR	130	mA
Current into Z_B (Pin 15)	3.0	mA
Storage Temperature	−65, +150	°C

"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices can be operated at these limits. The "Recommended Operating Conditions" provides conditions for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
V_{CC} Voltage (Speech, Pulse Mode) (Tone Dialing Mode)	+1.2 +3.3	— —	+10.5 +10.5	Vdc
Loop Current (into V_{CC}) (Speech, Pulse Mode) (Tone Dialing Mode)	4.0 15	— —	120 120	mA
Receiver Impedance	50	—	—	Ω
Voltage at $\overline{MUTE}$, MS (V_{CC} > 1.5 Volts)	0	—	V_{DD}	Vdc
R1 (Resistor from V_{CC} to V_B)	100	—	1800	Ω
Ambient Temperature	−20	—	+70	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, See Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
SUPPLY CURRENT					
Supply Current into V_{CC} (Pin 2 open, R12 = 25 k, V_{DD} unloaded)					mA
Speech Mode (Figure 2) V_{CC} = 1.2 Volts	I_{ccsp}	4.0	5.0	5.5	
V_{CC} = 3.5 Volts		9.0	11	12	
V_{CC} = 8.0 Volts		10	12	14	
V_{CC} = 10.5 Volts		—	13	—	
Tone Mode (Figure 4) V_{CC} = 3.3 Volts	I_{cct}	—	14	—	
V_{CC} = 8.0 Volts		—	16	—	
V_{CC} = 10 Volts		—	18	—	
VOLTAGE REGULATORS					
V_R Voltage (I_R = 65 μA, V_{CC} = 2.5 V, Figure 5)	V_R	1.6	1.7	1.85	Vdc
Load Regulation (0 < I_R < 300 μA, V_{CC} = 2.5 V)		—	0.2	0.5	Vdc
Line Regulation (I_R = 65 μA, 2.5 < V_{CC} < 10.5 V)		−70	±20	+70	mVdc
V_{DD} Voltage (V_{CC} ≥ 3.8 V, I_{DD} = 0, Figure 6)	V_{DD}	3.1	3.3	3.7	Vdc
Line Regulation (I_{DD} = 0, 5.0 V < V_{CC} < 10.5 V)		−70	±30	+70	mVdc
Maximum Output Current (V_{CC} = 3.8 V, V_{DD} ≥ 3.0 V)	I_{DDMAX}				mA
Speech Mode		0.8	1.0	—	
Pulse, Tone Mode		2.2	2.5	—	
Input Leakage Current (V_{CC} = 0, 3.3 Volts applied to V_{DD})	I_{lkg}				μA
$\overline{Mute}$ open or at V_{DD}		—	0.02	0.5	
$\overline{Mute}$ = 0 Volts		—	180	—	

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C, See Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
MICROPHONE AMPLIFIER					
Gain ($\overline{Mute}$ = V_{DD})	G_{MIC}	28	30	32	dB
Input Common Mode Rejection Ratio (1.0 kHz)	CMRR	20	26	—	dB
Input Impedance (Each Input)	R_{INMIC}	14	20	27	kΩ
MCO DC Bias Voltage (V_{CC} > 3.4 V, $\overline{Mute}$ = Hi) (V_{CC} = 1.2 V, $\overline{Mute}$ = Hi) ($\overline{Mute}$ = 0 V)	V_{MCODC}	0.85 0.6 —	1.1 0.71 0.08	1.25 0.93 —	Vdc
MCO Max Voltage Swing (THD = 5%, V_{CC} > 2.7 V) (THD = 5%, V_{CC} = 1.2 V)	V_{MCOAC}	— —	2.0 500	— —	Vp-p mVp-p
MCO Output Impedance	Z_{MCO}	—	270	—	Ω
MCO Output Current Capability (THD = 5%)	I_{MCO}	—	160	—	μA
Gain Reduction when Muted ($\overline{Mute}$ = 0 Volts, f = 1.0 kHz)	G_{MUT}	55	70	—	dB
RECEIVE AMPLIFIER					
RXI Bias Current (Mute = Hi)	I_{IBR}	—	50	—	nA
RXO1, RXO2 Bias Voltage (V_{CC} = 1.2 V) (V_{CC} > 3.0. V)	R_{XDC}	580 585	630 650	695 720	mVdc
RXO1–RXO2 Offset Voltage (V_{CC} > 3.0 V)	R_{XVOS}	−35	0	+35	mVdc
RXO1–RXO2 Max Voltage Swing (Figure 9) (THD = 5%, Receiver = ∞) (THD = 5%, Receiver = 150 Ω)	V_{RXAC}	 — —	 2.2 800	 — —	 Vp-p mVp-p
Internal Feedback Resistor (for muting)	R_{FINT}	—	1.0	—	kΩ
RXO1 & RXO2 Source Current	I_{RX}	2.6	3.2	3.5	mA
INTERNAL CURRENT AMPLIFIERS					
TXI Input Impedance	R_{TXI}	0.85	1.0	1.15	kΩ
ZB Input Impedance	R_{ZB}	—	500	—	Ω
RXA Output Impedance	R_{RXA}	—	10	—	kΩ
AC Current Gain TXI to V_{CC} (V_{RAGC} = 0 V) TXI to V_{CC} (V_{RAGC} = 1.3 V) ZB to RXA (V_{RAGC} = 0 V, RXA = AC Gnd) ZB to RXA (V_{RAGC} = 1.3 V, RXA = AC Gnd) TXI to RXA (V_{RAGC} = 0 V, RXA = AC Gnd) TXI to RXA (V_{RAGC} = 1.3 V, RXA = AC Gnd)	 G_{TX} G_{ZB} G_{STA} 	 — — — — — —	 100 50 0.5 0.25 1.22 0.61	 — — — — — —	A/A
DC INTERFACE					
LR Level Shift (V_{CC}–V_{LR}) (I_{LOOP} = 20 mA, $\overline{Mute}$ = V_{DD}) (I_{LOOP} = 80 mA, $\overline{Mute}$ = V_{DD}) (I_{LOOP} = 20 mA, $\overline{Mute}$ & MS = 0 V) (I_{LOOP} = 80 mA, $\overline{Mute}$ & MS = 0 V)	 ΔV_{LRS} ΔV_{LRT} 	 — — — —	 2.8 3.5 3.8 5.0	 — — — —	Vdc
V_{CC} Boost (I_{LOOP} = 20 mA, $\overline{Mute}$ & MS switched from Hi to Lo, R1 = 620 Ω)	ΔV_{LRB}	0.7	1.0	1.2	Vdc
RAGC Current (V_{RAGC} = 0 V) (V_{RAGC} = 1.0 V)	I_{RAGC}	— —	−40 −12	— —	μA

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C, See Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUTS					
$\overline{\text{MUTE}}$ Input Impedance (V_{CC} > 1.2 V)	R_{MUT}	—	60	—	kΩ
(V_{CC} = 0 V, 0 < $\overline{\text{Mute}}$ < 6.0 V)		—	>60	—	MΩ
Input Low Voltage	V_{ILMT}	0	—	1.0	Vdc
Input High Voltage	V_{IHMT}	V_{DD} − 0.5	—	V_{DD}	Vdc
Holdover (Delay for Receive amplifier to return to full gain after Pin 17 switches from 0 to V_{DD})	T_{MUT}	8.0	11	25	mSec
MS Input Impedance (V_{CC} > 1.2 V)	R_{MS}	—	60	—	kΩ
(V_{CC} = 0 V, $\overline{\text{Mute}}$ = open or V_{DD})		—	>50	—	MΩ
(V_{CC} = 0, $\overline{\text{Mute}}$ = 0)		—	4.0	—	kΩ
Input Low Voltage	V_{ILMS}	0	—	0.3	Vdc
Input High Voltage	V_{IHMS}	2.0	—	V_{DD}	Vdc

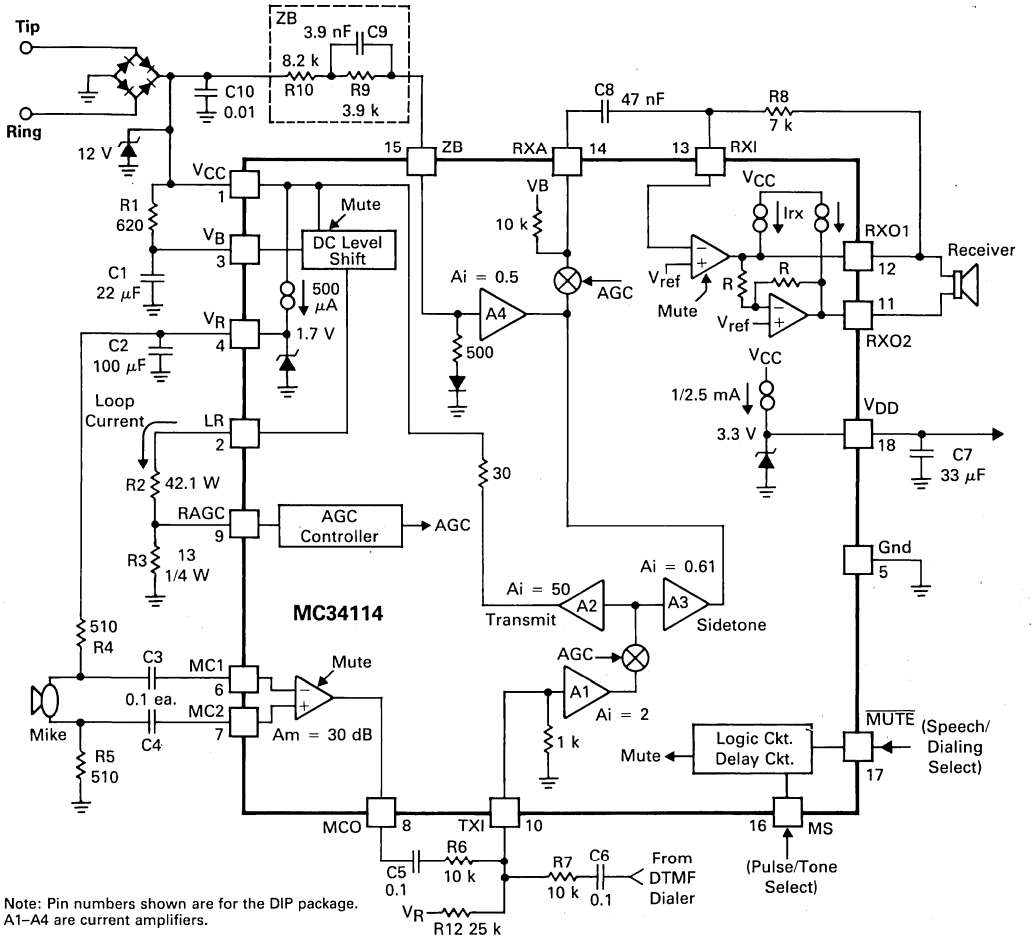
SYSTEM SPECIFICATIONS (f = 1.0 kHz unless noted, T_A = 25°C, Refer to Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
LINE INTERFACE					
V_{CC} DC Voltage (Pin 1)	V_{CC}				Vdc
Bell Telephone Standard and NTT Specs. (R2 = 43 Ω, R3 = 13 Ω)					
Speech Mode I_{LOOP} = 10 mA		1.7	2.0	2.3	
I_{LOOP} = 20 mA		3.0	3.4	3.7	
I_{LOOP} = 30 mA		3.5	4.1	4.5	
I_{LOOP} = 120 mA		8.5	9.9	10.5	
Tone Mode I_{LOOP} = 20 mA		3.9	4.1	4.3	
I_{LOOP} = 30 mA		4.5	5.1	5.5	
British Telecom Standard (R2 = 43 Ω + 2.5 V Zener, R3 = 13 Ω)					
Speech Mode I_{LOOP} = 10 mA		—	4.3	—	
I_{LOOP} = 20 mA		—	5.9	—	
I_{LOOP} = 30 mA		—	6.9	—	
I_{LOOP} = 70 mA		—	10	—	
AC Terminating Impedance (I_{LOOP} = 20 mA, Figure 11)	Z_{AC}	500	600	700	Ω
RECEIVE PATH					
Gain (V_{CC} to RXO1–RXO2, Figures 14, 15)	G_{RX}				dB
I_{LOOP} = 20 mA		−7.2	−6.1	−5.0	
I_{LOOP} = 100 mA		−13.5	−11	−9.5	
ΔGain (G_{RX} @ 100 mA versus 20 mA)	ΔG_{RX}	−7.5	−6.0	−4.5	dB
Muted Gain ($\overline{\text{Mute}}$ = Logic 0, I_{LOOP} = 20 mA)	G_{RXM}	—	−22	−20	dB
Distortion (at RXO1–RXO2, V_{CC} = 250 mVrms)	THD_R				%
f = 300 Hz		—	0.3	—	
f = 1.0 kHz		—	0.2	2.0	
f = 3.4 kHz		—	0.02	—	
Output Noise Across RXO1–RXO2 (@ 1.0 kHz)	N_{RXO}	—	4.0	—	μVrms
TRANSMIT PATH					
Gain (MC1–MC2 to V_{CC}, Figures 12, 13)	G_{TX}				dB
I_{LOOP} = 20 mA		36	38.5	40.5	
I_{LOOP} = 100 mA		29	32.5	35.5	
ΔGain (G_{TX} @ 100 mA versus 20 mA)	ΔG_{TX}	−7.5	−6.0	−4.5	dB
Max V_{CC} Voltage Swing (THD = 5%, Figure 8)	VTX_{MAX}				Vp-p
I_{LOOP} = 20 mA		—	3.0	—	
I_{LOOP} = 100 mA		—	2.3	—	
Gain Reduction when muted (MC1–MC2 to V_{CC}, $\overline{\text{Mute}}$ = 0 V)	G_{TXM}	—	68	—	dB
Distortion (0 dBm @ V_{CC})	THD_T				%
f = 300 Hz		—	0.5	—	
f = 1.0 kHz		—	1.5	3.0	
f = 3.4 kHz		—	1.3	—	
Output Noise at V_{CC} (@ 1.0 kHz)	N_{TXO}	—	17	—	μVrms
SIDETONE					
Sidetone Gain (Gain from V_{CC} to RXO1–RXO2 with signal applied to MC1/MC2, I_{LOOP} = 20 mA)	G_{ST}	—	−27	−22	dB

PIN DESCRIPTIONS

Symbol	Pin Number (SOIC)	Pin Number (DIP)	Description
V_{CC}	1	1	Power supply pin for the IC. Supply voltage is derived from loop current. Transmit amp output operates on this pin.
LR	2	2	Resistors R2+R3 at this pin set the DC characteristics of the circuit. The majority of the loop current flows through these resistors. Other components may be used to produce required DC characteristics for individual regulatory agencies.
V_B	3	3	A resistor or appropriate network (R1) connected from this pin to V_{CC} sets the AC terminating impedance (return loss spec).
V_R	4	4	A 1.7 volt regulated output which can be used to bias the microphone. Additionally, this voltage powers a portion of the internal circuitry. Can nominally supply 300–500 μA.
GND	5	5	Ground pin for the entire IC. Normally this is not connected to, nor to be confused with earth ground.
MC1	6	6	Inverting differential input to the microphone amplifier. Input impedance is typically 20 kΩ.
MC2	7	7	Non-inverting differential input to the microphone amplifier. Input impedance is typically 20 kΩ.
MC0	8	8	Microphone amplifier output. Amplifier's gain is fixed at 30 dB.
RAGC	10	9	Loop current sensing input. The voltage at this pin, determined by the loop current and R3, operates the loop length equalization circuit.
TXI	11	10	Input to the transmit amplifier from the microphone amplifier, DTMF source, and other sources. Input impedance ≈ 1.0 kΩ.
RXO2	12	11	Receive amplifier non-inverting differential output. Current capability to the receiver is typically set at ±3.0 mA peak.
RXO1	14	12	Receive amplifier inverting differential output. Current capability to the receiver is typically ±3.0 mA peak. Gain is set by R8.
RXI	15	13	Summing input to the receive amplifier. This pin is an AC virtual ground.
RXA	16	14	Summed outputs of the receive current amplifier, sidetone amplifier, and an AGC point. Normally connected to the receive amplifier input (RXI) through a coupling capacitor.
ZB	17	15	Input to the receive current amplifier. A balance network (ZB) is connected between this pin and V_{CC}. The network affects the receive level and sidetone performance. Input impedance is ≈500 Ω in series with a diode.
MS	18	16	Mode Select Input. A logic "1" sets the IC for pulse dialing. A logic "0" sets the IC for tone (DTMF) dialing. Effective only if $\overline{\text{MUTE}}$ is at a logic "0". Input impedance is ≈ 60 kΩ.
$\overline{\text{MUTE}}$	19	17	$\overline{\text{Mute}}$ input. A logic "1" sets normal speech mode. A logic "0" mutes the microphone and receive amplifiers and allows MS to be functional. Input impedance is ≈60 kΩ referenced to V_{DD}. An internal fixed delay of 11 mSec minimizes clicks in the receiver when returning to the speech mode.
V_{DD}	20	18	A regulated 3.3 volt output for an external dialer. Output source current capability is 1.0 mA in speech mode, 2.5 mA in tone dialing mode.

FIGURE 1 — BLOCK DIAGRAM AND TEST CIRCUIT



Note: Pin numbers shown are for the DIP package.
A1–A4 are current amplifiers.

FIGURE 2 — I_{CC} versus V_{CC} (SPEECH MODE)

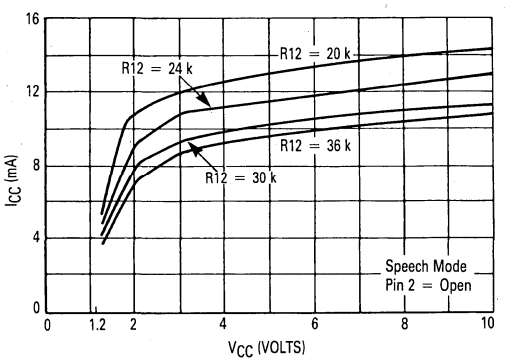


FIGURE 3 — I_{CC} versus V_{CC} (PULSE DIALING MODE)

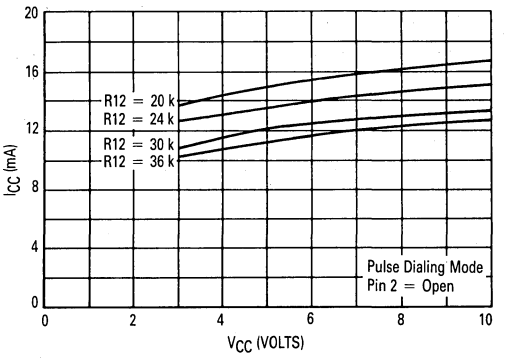


FIGURE 4 — I_{CC} versus V_{CC} (TONE DIALING MODE)

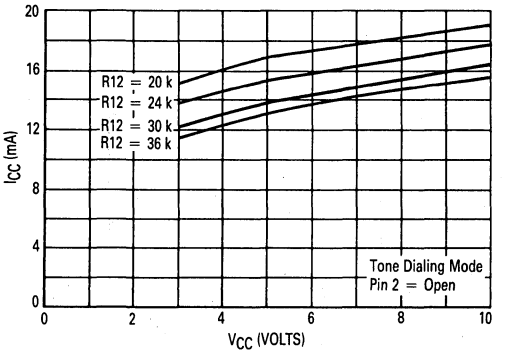


FIGURE 5 — V_R versus I_R versus V_{CC}

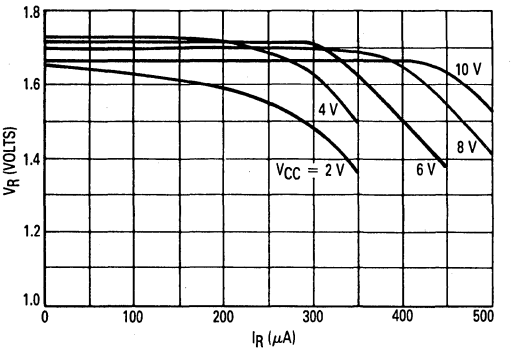


FIGURE 6 — V_{DD} versus I_{DD}

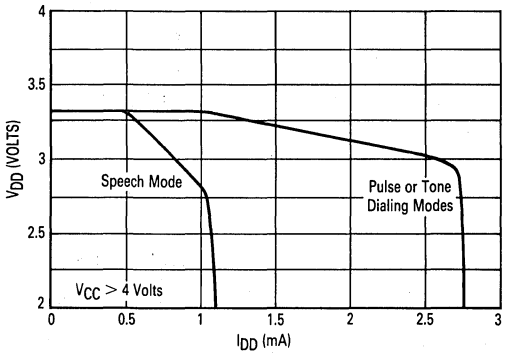


FIGURE 7 — AGC GAIN versus VOLTAGE AT PIN 9

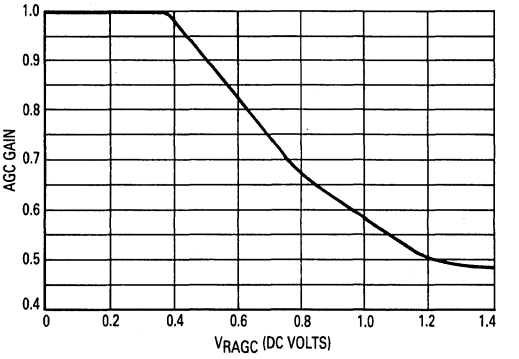


FIGURE 8 — MAXIMUM TRANSMIT SIGNAL AT V_{CC}

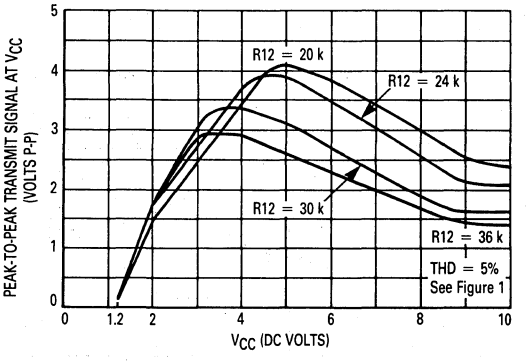
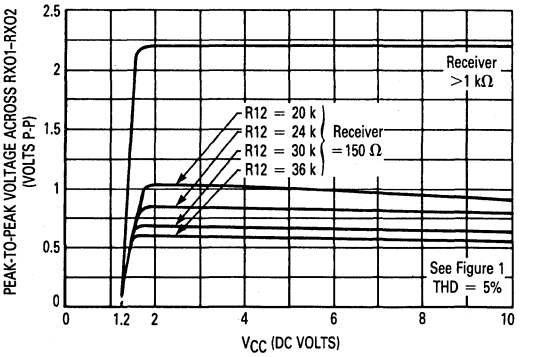


FIGURE 9 — MAXIMUM RECEIVER SIGNAL



SYSTEM PERFORMANCE

FIGURE 10 — TIP/RING VOLTAGE versus LOOP CURRENT

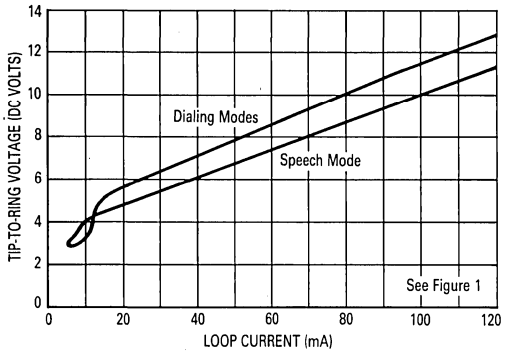


FIGURE 11 — AC TERMINATING IMPEDANCE versus LOOP CURRENT

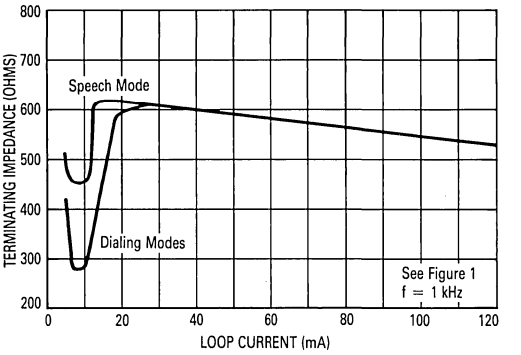


FIGURE 12 — TRANSMIT GAIN versus LOOP CURRENT

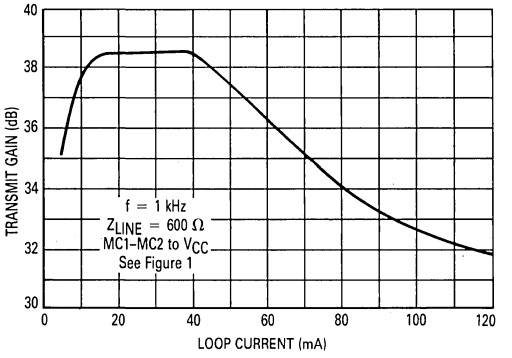


FIGURE 13 — TRANSMIT GAIN versus FREQUENCY

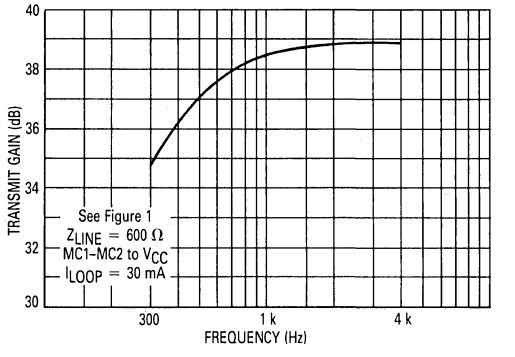


FIGURE 14 — RECEIVE GAIN versus LOOP CURRENT

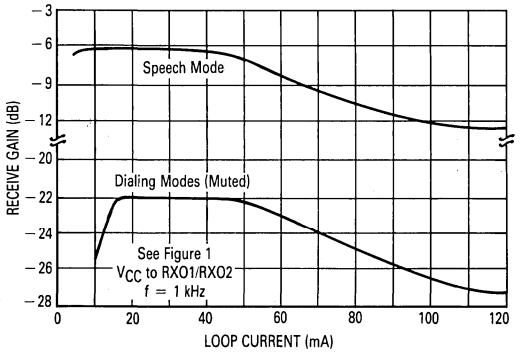
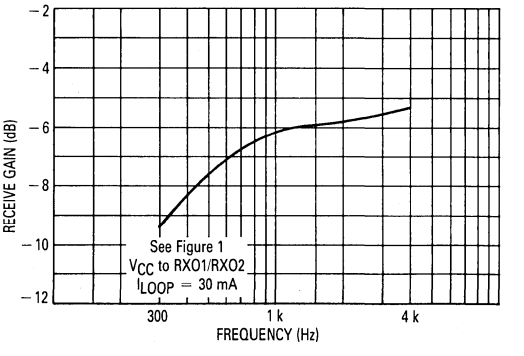


FIGURE 15 — RECEIVE GAIN versus FREQUENCY



SYSTEM PERFORMANCE

FIGURE 16 — TRANSMIT NOISE SPECTRUM

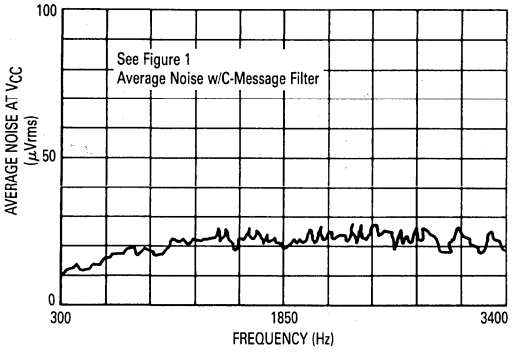


FIGURE 17 — RECEIVE NOISE SPECTRUM

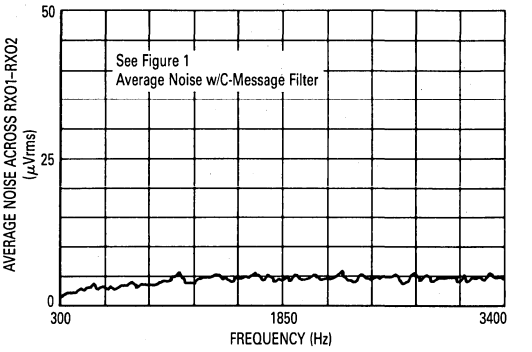


FIGURE 18 — V_{CC} versus TEMPERATURE

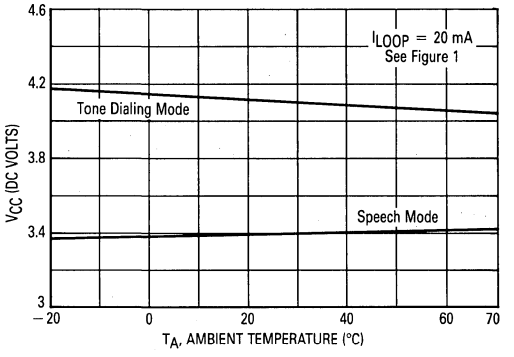


FIGURE 19 — TRANSMIT GAIN versus TEMPERATURE

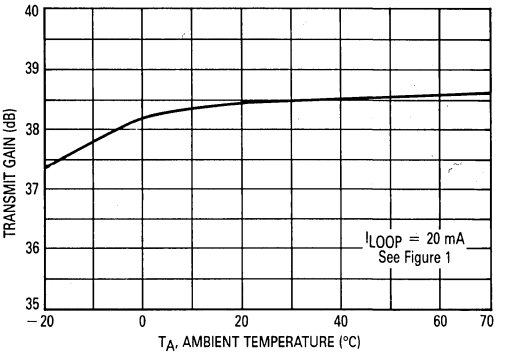


FIGURE 20 — RECEIVE GAIN versus TEMPERATURE

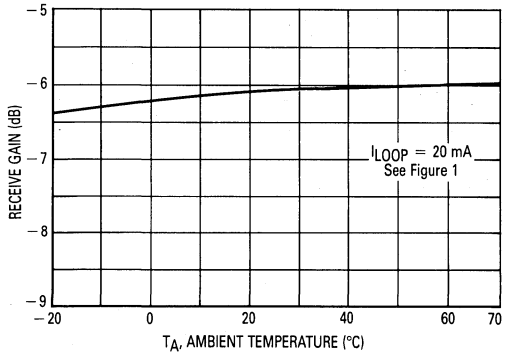
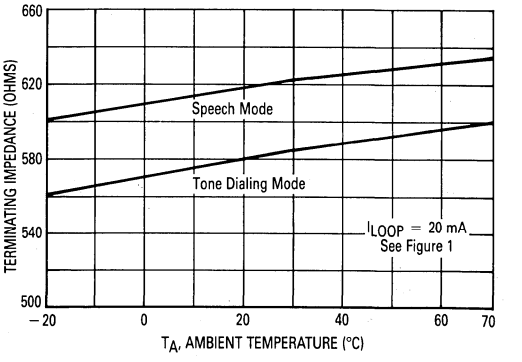


FIGURE 21 — AC TERMINATING IMPEDANCE versus TEMPERATURE



FUNCTIONAL DESCRIPTION

INTRODUCTION

The MC34114 is a speech network which provides the hybrid function and the DC loop current interface of a telephone, and is meant to connect to Tip and Ring through a polarity guard bridge. The transmit, receive, and sidetone gains are externally adjustable, and additionally, line length compensation varies the gains with variations in loop current. The microphone amplifier employs a differential input to minimize RFI susceptibility.

The loop current interface portion determines the dc voltage versus current characteristics, and provides the required regulated voltages for internal and external use.

The dialer interface provides three modes of operation: speech (non-dialing), pulse dialing and tone (DTMF) dialing. When switching among the modes, some parameters are changed in order to optimize the circuit operation for that mode. The following table summarizes those changes:

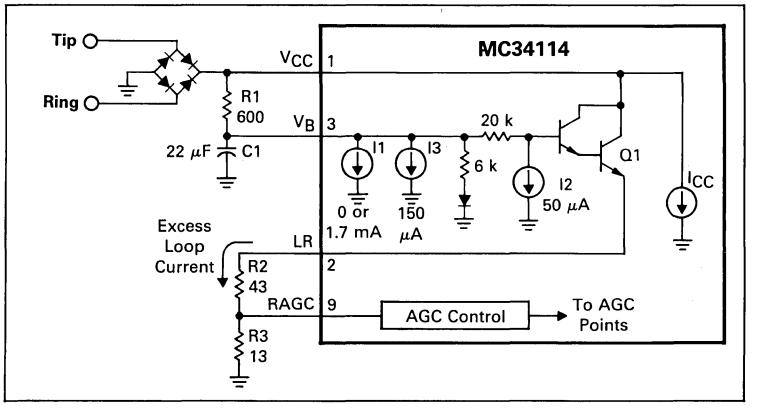
TABLE 1 — OPERATING PARAMETERS versus OPERATING MODE

Function	Speech	Pulse	Tone
LR Level Shift (V_{CC} – VLR)	2.8 V	2.8 V	3.8 V
V_{DD} Current Capability	1.0 mA	2.5 mA	2.5 mA
Microphone Amplifier	Functional	Muted	Muted
Receive Amp. Internal Feedback Resistor	Switched Out	Switched In	Switched In

DC LINE INTERFACE AND LINE LENGTH COMPENSATION

The DC line interface circuit (Pins 1, 2, 3) sets the DC voltage characteristics with respect to loop current. See Figure 22.

FIGURE 22 — DC LINE INTERFACE EQUIVALENT



The DC voltage at V_{CC} is determined by the level shift from V_{CC} to LR, plus the voltage across R2 and R3. I_{CC} is the internal bias current required by the MC34114, nominally in the range of 10 mA. I_{CC} can be reduced, if necessary, by increasing R12, consistent with the transmit and receive signal requirements (see the Transmit Path section). See Figures 2–4, 8 and 9.

In the speech and pulse dialing modes current source I1 is off, and the level shift is due to Q1's base-emitter drop (≈1.4 V), 1.0 volt across the 20 k resistor, and the voltage across R1, which varies with V_{CC} from 0.15 volts to ≈1.0 volt. When the loop current coming in from Tip and Ring exceeds the I_{CC} requirement, the excess current flows through Q1, R2 and R3, to set the slope of the V-I characteristic for the circuit (Q1 has an equivalent resistance of ≈10 Ω). See Figure 10.

In the tone dialing mode, current source I1 is on, drawing an additional 1.7 mA through R1, increasing the level shift by ≈1.0 volts (for R1 = 600 Ω). This feature ensures that, at low loop currents, sufficient voltage is present at V_{CC} for the DTMF signals, and that the V_{DD} regulator supplies sufficient voltage to an external dialer. The I_{CC} current increases by ≈1.3 mA in this mode.

R1 must be kept in the range of 100 to 1800 Ω. If it is too large, insufficient current will flow into V_B to bias up the circuit. If it is too small, insufficient filtering at V_B will result unless C1 is increased accordingly. Speech signals must be well filtered from V_B.

The voltage across R3 determines the operation of the AGC circuit (line length compensation). As the voltage at RAGC increases from ≈0.4 volts to ≈1.2 volts, the AGC Control varies the current gain of the two AGC

points (Figure 1) from 1.0 to 0.5, thereby reducing the gain of the transmit and receive paths by 6.0 dB. See Figure 7. Pin 9 is a high impedance input.

The values of R2 and R3 can be varied as required to comply with various regulatory agencies, to compensate for additional circuitry powered by the loop current (microprocessor, etc.), or to change the starting point of the AGC function. If the AGC is not used, Pin 9 should be connected to ground for high gains, or to V_R for low gains.

VOLTAGE REGULATORS

The MC34114 has two internal voltage regulators which are used to power external as well as internal circuitry.

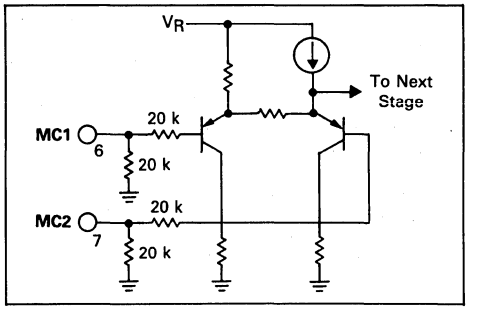
The V_R regulator provides 1.7 volts at a maximum current of 500 μA (see Figure 5). This output is normally used to set the DC bias into TXI (Pin 10), and to bias the electret microphone. V_R will typically be ≈300 mV less than V_{CC} when V_{CC} is below 2.0 volts.

The V_{DD} regulator provides 3.3 volts at a maximum of 1.0 mA in the speech mode, and 2.5 mA in the pulse or tone dialing modes (see Figure 6). It is normally used to power an external dialer, and other associated circuitry. V_{DD} is normally ≈0.5 volts less than V_{CC} until V_{DD} regulates. It is a shunt type regulator which automatically switches to a high impedance mode when V_{CC} falls below 1.4 volts. This feature prevents excessive battery drain in the event a memory sustaining battery is used with the external dialer. Leakage current (with V_{CC} = 0) is typically 0.02 μA with an applied voltage of up to 6.0 volts at V_{DD}, with pin 17 open or at V_{DD}. If Pin 17 is at ground, a current of several hundred microamps will flow into V_{DD} and out of pin 17 (see paragraph on Logic Interface).

MICROPHONE AMPLIFIER

The microphone amplifier (Pins 6, 7, 8) has a differential input, single ended output, and a fixed internal gain of +30 dB (31.1 V/V). The output is in phase with MC2, and out of phase with MC1. The inputs (see Figure 23) have a nominal impedance of 20 kΩ, and are matched to provide a high common mode rejection (typically 26 dB).

FIGURE 23 — INPUT STAGE



To preserve a high CMRR against unwanted signals induced in the microphone leads, the microphone should be biased with two equal value resistors as shown in Figure 1.

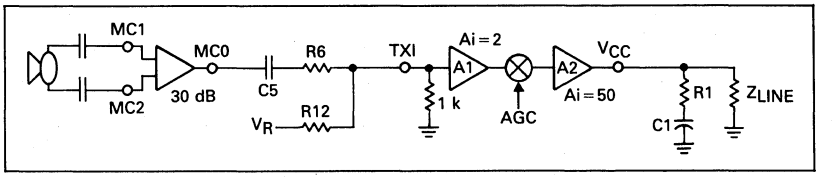
The output (MCO) has a DC bias voltage of ≈1.1 volts (V_{CC} > 3.0 volts), and can nominally swing ≈2.0 volts p-p (500 mV p-p at V_{CC} = 1.2 volts). The output impedance is ≈270 Ω, and has a peak current capability of ≈160 μA for 5% THD.

When the MC34114 is switched to either dialing mode, the microphone amplifier is muted by ≈70 dB (300 Hz–4 kHz), effectively disabling the microphone. The DC voltage at MCO is ≈80 mV when muted.

TRANSMIT PATH

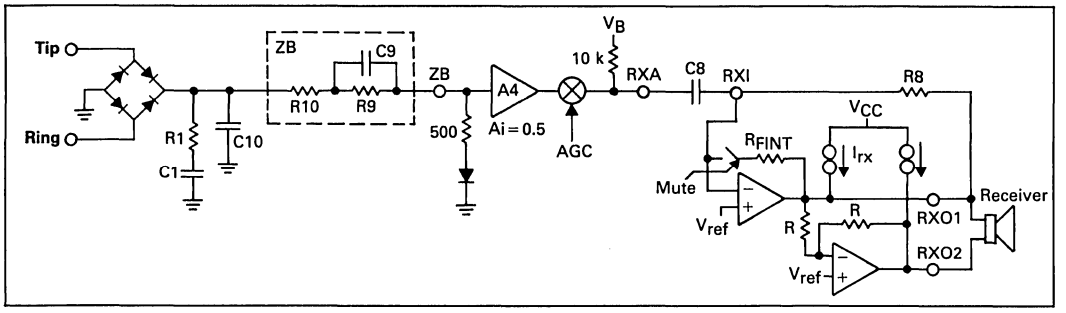
The AC transmit path consists of the components shown in Figure 24 (taken from Figure 1).

FIGURE 24 — TRANSMIT PATH



The voltage output at MCO is converted to a current into TXI by C5, R6, and TXI's 1.0 k input impedance (with a slight error due to R12). A1 and A2 are current amplifiers with a combined gain of 100. The AGC point has a current gain of 1.0 at low loop currents, and decreases to 0.5 as loop current increases. Therefore the current gain from TXI to V_{CC} varies from 100 to 50 as loop current is increased. The resulting current output at V_{CC} acts on R1 and the line impedance (nominally 600 Ω each, C1 is an AC short) to generate a voltage

FIGURE 25 — RECEIVE PATH



signal at V_{CC}, and consequently, at Tip and Ring. The voltage gain from MC1–MC2 to Tip and Ring is therefore (first order):

$$G_{TX} = \frac{Am \times 100 \times AGC \times R1//Z_{LINE}}{(R6 + 1.0\ k)} \qquad \text{(Equation 1)}$$

where Am is the gain of the microphone amplifier (31.1 V/V). At low loop currents G_{TX} ≈84 V/V (38.5 dB), and decreases to ≈42 V/V (32.5 dB) at higher loop currents, for the component values shown in Figure 1 (@ 1.0 kHz).

For more precise calculations, consideration should be given to the effects of C5 (in series with R6), R12 and R7 (each in parallel with TXI's 1.0 k impedance), and C10 and the ZB network (each in parallel with R1 and Z_{LINE}). The cumulative effects of these additional components is ≈1.5 dB.

The voltage signal at V_{CC} is out of phase with that at TXI, and in phase with that at MC1.

The maximum available voltage swing at V_{CC} is a function of the impedance at V_{CC} (R1//Z_{LINE}), the DC bias current at A2's output, and the V_{CC} DC voltage. A2's bias current is determined by the bias current through R12 (V_R/{R12 + 1.0 k}) which is gained up by A1, A2 and the AGC point. Figure 8 indicates the maximum voltage swing at V_{CC} (with 5% THD).

RECEIVE PATH

The AC receive path consists of the components shown in Figure 25 (taken from Figure 1).

R1, typically 600 Ω, provides the AC termination (return loss) for the receive signals coming in on Tip and Ring (C1 is an AC short). The receive signal creates an AC current through the ZB network and the 500 Ω resistor at the ZB pin. A4 reduces that current by 1/2, and then feeds it through the AGC point which has a gain of 1.0 at low loop currents. The AGC gain is reduced to 0.5 as loop current increases. The AC current out of the AGC point feeds through C8 to RXI, the receive amp's summing node (If C8 is large, RXA can be considered a virtual ground, and no AC current flows through the internal 10 k resistor). The voltage swing at RXO1 is then determined by the current through C8 and the R8 feedback resistor. The second op amp (at RXO2) is internally configured for inverting unity gain. The voltage gain from Tip and Ring to RXO1–RXO2 (differential) is (first order):

$$G_{RX} = \frac{R8 \times AGC}{(ZB + 500)} \qquad \text{(Equation 2)}$$

where ZB = R10 + R9//C9 (≈R10 + R9).

For more precise calculations, the effects of C9 and C8 must be considered. C9 provides a phase shift to aid sidetone cancellation (see paragraph on Sidetone), and C8 can be selected to provide low frequency roll-off. High frequency roll-off can be obtained by adding a feedback capacitor across R8. For the component values shown in Figure 1, the receive gain measured ≈0.495 V/V (−6.1 dB) at low loop currents, and reduces to ≈0.25 V/V (−12 dB) at higher loop currents (@ 1.0 kHz).

When the MC34114 is switched to either dialing mode ($\overline{Mute}$ = low), the receive gain is muted by the switching in of the internal feedback resistor (R_{FINT} from RXO1 to RXI) — typically 1.0 kΩ. The effective feedback resistor for the amplifier is now the parallel combination of R8 and R_{FINT}. The amount of muting (in dB) can be calculated from:

$$G_{RXM} = 20 \times \log\left(\frac{R8 + R_{FINT}}{R_{FINT}}\right) \qquad \text{(Equation 3)}$$

The internal resistor is switched in coincident with $\overline{Mute}$ (Pin 17) switching low. However, when $\overline{Mute}$ is switched high, a delay (nominally 11 mSec) occurs before the internal resistor is switched out. This feature prevents dialing transients (particularly during pulse dialing) from being heard as loud clicks in the receiver.

The DC bias voltages at RXI, RXO1 and RXO2 is ≈0.65 volts. The bias current at RXI is ≈50 nA into the pin. The maximum voltage swing at RXO1 and RXO2 is a function of the receiver impedance (typically 100–150 Ω), and the value of the two I_{rx} current sources in Figure 25. I_{rx}, set by R12 (between V_R and TXI), is equal to:

$$I_{rx} = \frac{V_R \times 50 \times AGC}{(R12 + 1.0\ k)} \qquad \text{(Equation 4)}$$

Figure 9 indicates the maximum voltage swing available to the receiver.

SIDETONE CANCELLATION

Sidetone cancellation is provided by current amplifier A3 (see Figure 1) which generates a current representative of the transmit signal to cancel the reflected sidetone signal coming in through ZB and A4. To achieve perfect cancellation (no AC current out of RXA), it is necessary that:

$$ZB = (40 \times R1 // Z_{LINE}) - 500\ \Omega \quad \text{(Equation 5)}$$

where ZB is the network composed of R9, R10, and C9, and Z_{LINE} is the AC impedance of the line. The reactive components of the line's impedance can be compensated for by making the ZB network comparably reactive. In Figure 1, C9 provides a phase shift to compensate for the phase shift created by the phone line.

LOGIC INTERFACE ($\overline{\text{Mute}}$ and MS)

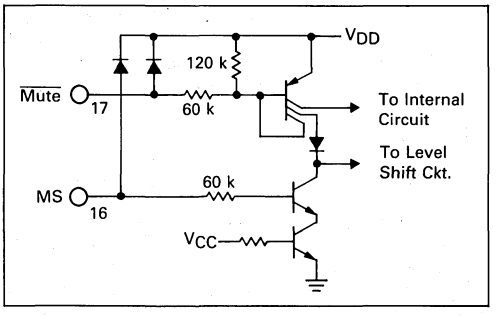
The two logic inputs ($\overline{\text{Mute}}$ and MS) are used to switch the MC34114 between the speech and dialing modes according to the following table:

TABLE 2 — LOGIC INPUTS

$\overline{\text{Mute}}$	MS	Mode
High	X	Speech
Low	High	Pulse Dialing
Low	Low	Tone Dialing

Table 2, together with Table 1, describes the condition of the MC34114 in the various modes. Figure 26 shows the input configuration for the $\overline{\text{Mute}}$ and MS pins.

FIGURE 26 — LOGIC INPUTS



The $\overline{\text{Mute}}$ input has a nominal input impedance of 60 kΩ, referenced to V_{DD}. This pin may be left open for a logic "1," or connected to V_{DD}. A logic "1" is defined as between V_{DD}–0.5 volts and V_{DD}. A logic "0" is defined as between ground and 1.0 volt. The switching threshold is ≈2.3 volts. When $\overline{\text{Mute}}$ is switched low (speech to dialing), the changes listed in Table 1 will occur within 10 μs. Upon switching high (back to speech mode), however, the receive amplifier feedback resistor will be switched out after a delay of (typically) 11 ms. This feature prevents dialing transients (particularly during pulse dialing) from being heard as loud clicks in the receiver. The other functions listed in Table 1 transfer within 10 μs.

The MS pin is functional only when $\overline{\text{Mute}}$ is low and its only function is to provide an additional voltage level shift between V_{CC} and LR in the tone dialing mode (see the section on DC Interface). The input impedance is ≈60 kΩ when $V_{CC} > 1.5$ volts. A logic "0" is between ground and 0.3 volts, and a logic "1" is between 2.0 volts and V_{DD}. The switching threshold is typically 0.75 volts. If unused, this pin must be connected to ground or V_{DD}, and not left open.

When $V_{CC} = 0$ (on-hook condition), and a voltage in the range of 0 to 6.0 volts is applied to $\overline{\text{Mute}}$, a leakage current of (typically) 0.02 μA will flow if $\overline{\text{Mute}}$ and V_{DD} are at the same voltage. If $\overline{\text{Mute}}$ is at a voltage different from V_{DD}, current will flow through the internal resistors and/or diode. If a memory sustaining battery is used in conjunction with an external dialer, and is configured so that its voltage appears at V_{DD}, $\overline{\text{Mute}}$ must be allowed to float or be connected to V_{DD} — otherwise current (in the range of 100–200 μA) will flow from the battery through V_{DD} and out of the $\overline{\text{Mute}}$ pin.

When $V_{CC} = 0$, and a voltage in the range of 0 to 6.0 volts is applied to MS, a leakage current of (typically) 0.01 μA will result as long as $\overline{\text{Mute}}$ is open or at V_{DD}. If $\overline{\text{Mute}}$ is at ground, an equivalent 3.5 kΩ parasitic resistance exists between MS and $\overline{\text{Mute}}$.

When $V_{CC} < 1.5$ volts, the Mute function is nonexistent and the MC34114 will be in the speech mode.

APPLICATIONS INFORMATION

DESIGN SEQUENCE

The design sequence for incorporating the MC34114 into most applications will be as follows (refer to Figure 1):

1) Decide on the AC terminating impedance (return loss), and select R1 to be that value (typically 600 Ω). If there are other devices powered by the loop current which will be in parallel with R1 (such as a pulse dialing circuit) which lower the effective terminating impedance, R1 can be increased accordingly.

2) Select the maximum value of R12 which will provide the minimum required transmit and receive signals according to Figures 8 and 9.

3) Select the sum {R2 + R3} to provide the desired Tip and Ring DC voltage versus loop current characteristics. Then select R3 for the desired starting point of the loop length compensation. The compensation begins when the voltage across R3 is ≈0.4 volt.

4) Select R4 and R5 (they should be equal) to properly bias the microphone. The microphone's manufacturer should be consulted for this information.

5) Select R6 for proper transmit gain. See equation 1. Then select C5 to provide low frequency roll-off. Adjust R6 as required.

6) Select the ZB network (R9, R10, C9) to provide sidetone cancellation. See equation 5.

7) Select R8 for proper receive gain (depends on the specific receiver used). See equation 2. Then select C8 to provide low frequency roll-off. Adjust R8 as required.

Additional comments on Figure 1 components:

1) Capacitors C1, C2, and C7 are required to stabilize the respective regulators. In most applications it should not be necessary to change from the values shown in Figure 1.

2) C3 and C4 can be selected to provide low frequency roll-off for the microphone signals.

3) C10 filters noise generated by the MC34114, and should be close to the V_{CC} pin. Its recommended value (0.01 μF) is such that it does not noticeably affect the system parameters. It can be increased, if desired, to provide high frequency roll-off for both transmit and receive signals. This, however, will affect the return loss specification at higher frequencies.

4) Since TXI is a (relatively) low impedance current input, it is a convenient point for injecting any signals which are to be transmitted out onto Tip and Ring. C6 and R7 are shown for transmitting the DTMF signals from a dialer. Additional RC networks can be connected to TXI for transmitting signals from speakerphones, modems, or other signal sources. The voltage gain from each signal source to Tip and Ring is:

$$G_S = \frac{Z_{LINE}//R1 \times 100 \times AGC}{(R_X + Z_{CX})} \quad \text{(Equation 6)}$$

where R_X and Z_{CX} represent the impedances of the R and C for the particular signal source. If several signal sources are connected to TXI, the parallel combination of R6, R12, the internal 1.0 k resistor, and any other RCs at this pin must be considered when setting the gain for each signal.

5) The 12 volt zener diode shown in Figure 1 is for transient protection, and normally does not conduct. Transient and overvoltage protection **MUST** be provided externally so that the Absolute Maximum Ratings are not exceeded.

BASIC TELEPHONE CIRCUIT

Figure 27 depicts a complete basic telephone using the MC34114 speech network, the MC145412 pulse/tone dialer, and the MC34017 tone ringer.

The MC34114 provides the speech network/hybrid functions, and its component values are calculated as described previously in this data sheet. The resistor from V_{CC} to V_B is 820 Ω (rather than 600 Ω) in this example since it is in parallel with the 2.0 kΩ resistor in the pulse dialing transistor network (providing and effective 600 Ω termination).

The MC145412 dialer is a pulse/tone dialer with 10 number memory, including last number redial. Power to the dialer is from the MC34114's V_{DD} output, diode connected with a memory sustaining battery.

The MC34017 tone ringer (see its data sheet for details) is connected directly to Tip and Ring as it is not necessary to disconnect it when off-hook. This circuit has an REN ≈0.5, and meets all EIA-470 and Bell system requirements for impedance, anti-bell tapping, and turn-on/off thresholds.

OPERATION WITH A POWER SUPPLY

Figure 28 indicates how to incorporate the MC34114 into a circuit where a power supply is used.

FIGURE 27 — BASIC PULSE/TONE TELEPHONE

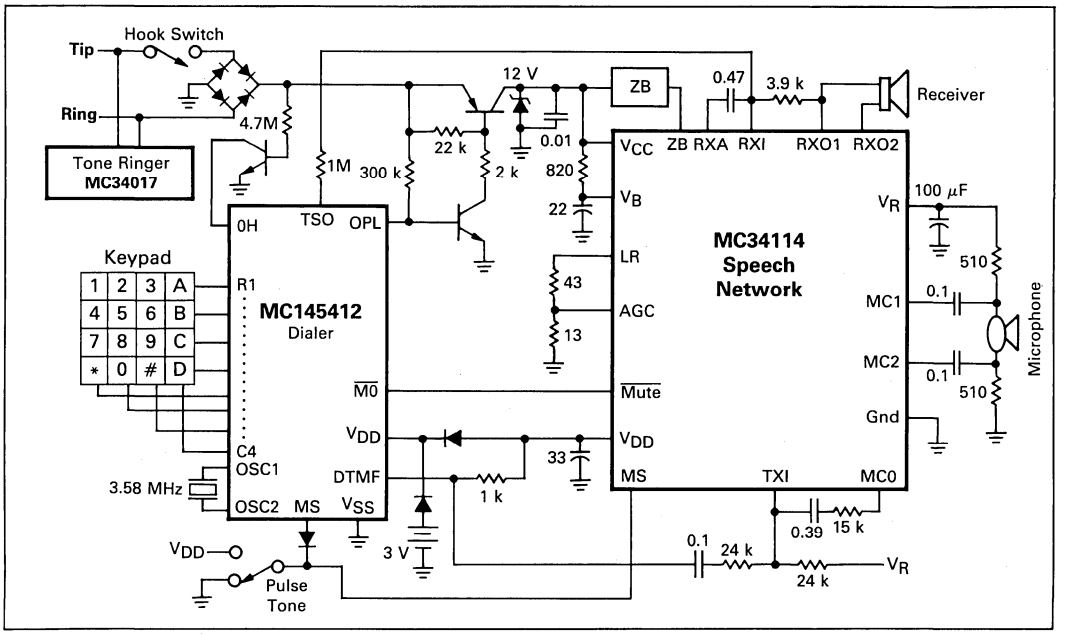
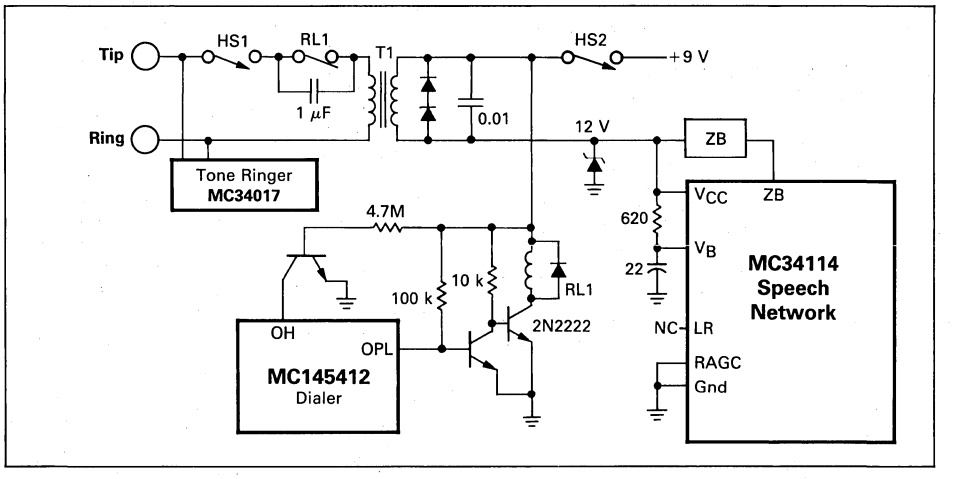


FIGURE 28 — USE WITH A POWER SUPPLY



A transformer (T1) is required at Tip and Ring to provide the isolation required between the phone line and any AC power and earth ground. (The transformer must be rated to handle the loop current.) Since the loop current does not pass through the MC34114, loop length compensation is not possible in this circuit, and pin 2 (LR) is left open. The RAGC pin is grounded, setting the transmit and receive gains to their maximum.

The transformer provides a path for the power supply to reach the MC34114, while simultaneously coupling speech signals between Tip/Ring and the MC34114. The two series diodes provide transient clamping, as does the 12 volt zener diode. Although a +9.0 volt supply is shown, other voltages can be used as long as the MC34114 receives between 4.0 and 10.5 volts at V_{CC}.

Because of the isolation requirement, the MC145412 dialer requires a relay (RL1) to break the loop current during pulse dialing. The relay is normally off, and energized only during pulse dialing. The 1.0 μF capacitor (rated 250 volts min., NPO) across the relay contacts helps absorb transients generated during pulse dialing.

ALTERNATE MICROPHONE CONFIGURATIONS

The MC34114 is designed for use with electret microphones, although dynamic microphones can be used. Carbon microphones are not recommended as they generally require considerable bias current which is not available from the MC34114's regulators.

When using an electret microphone which requires more than 1.7 volts, but less than 1.0 mA for bias, it can be biased from V_{DD} instead.

If a three terminal electret microphone (containing an internal biasing resistor or equivalent) is used, it should be connected to the MC34114 as shown in Figure 29. The common mode rejection of the balanced circuit shown in Figure 1 is not present however, and care should be taken to prevent unwanted signals (radio stations, noise, etc.) from being picked up by the microphone leads.

FIGURE 29 — 3-TERMINAL MICROPHONE

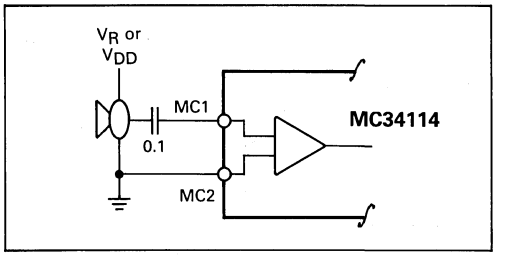
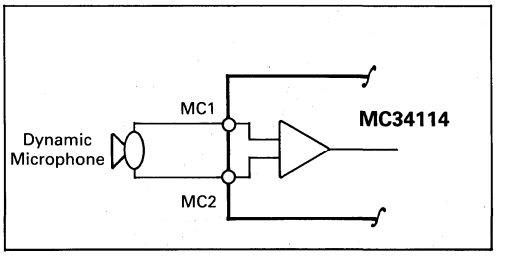


Figure 30 indicates use of the MC34114 with a dynamic microphone. The output level of dynamic microphones is generally lower than electret units, and so the gain of the transmit path will have to be adjusted accordingly.

FIGURE 30 — DYNAMIC MICROPHONE

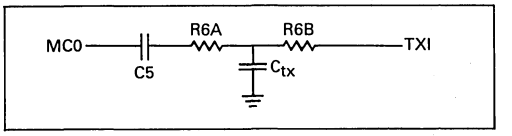


FREQUENCY CHARACTERISTICS

Frequency characteristics for both transmit and receive signals are dependent entirely on the external components. The amplifiers within the IC have bandwidths from DC extending to in excess of 50 kHz, and therefore do not provide roll-off within the voiceband.

Low frequency roll-off for the transmit signals can be set by adjusting C3 and C4, or C5, or a combination of the three. High frequency roll-off can be provided by replacing R6 with the network shown in Figure 31.

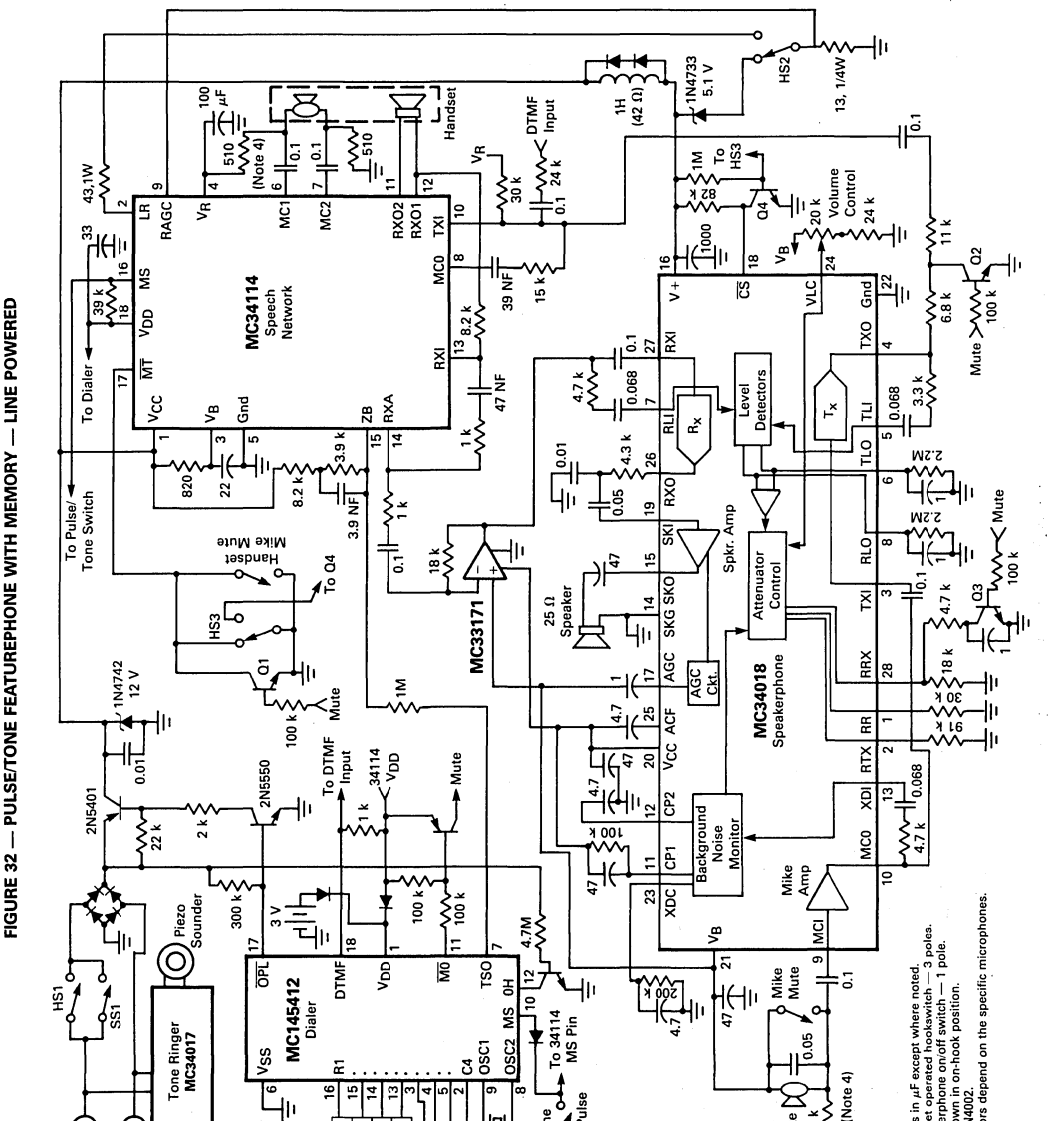
FIGURE 31 — TRANSMIT HF ROLL-OFF



The 3.0 dB upper frequency is determined by:

$$f = \frac{(R6A + R6B + 1.0\ k)}{2\pi\ (R6A \times (R6B + 1.0\ k) \times C_{tx})} \quad \text{(Equation 7)}$$

FIGURE 32 — PULSE/TONE FEATUREPHONE WITH MEMORY — LINE POWERED



Low frequency roll-off for the receive signals can be set by adjusting C8, and high frequency roll-off can be set by placing a capacitor across R8.

FEATUREPHONE DESIGN

Figure 32 and Figure 33 depict two featurephone circuits which include the following functions: selectable handset and speakerphone operation, ten number memory pulse/tone dialer, tone ringer, a "Privacy" (Mike mute) function, and line length compensation for both handset and speakerphone operation. Figure 32 uses the MC34018 speakerphone IC, while Figure 33 uses the MC34118 speakerphone IC. Application notes AN1002 and AN1004 (for Figure 32 and Figure 33 respectively) should be consulted for design and performance details, as well as variations of these two circuits.

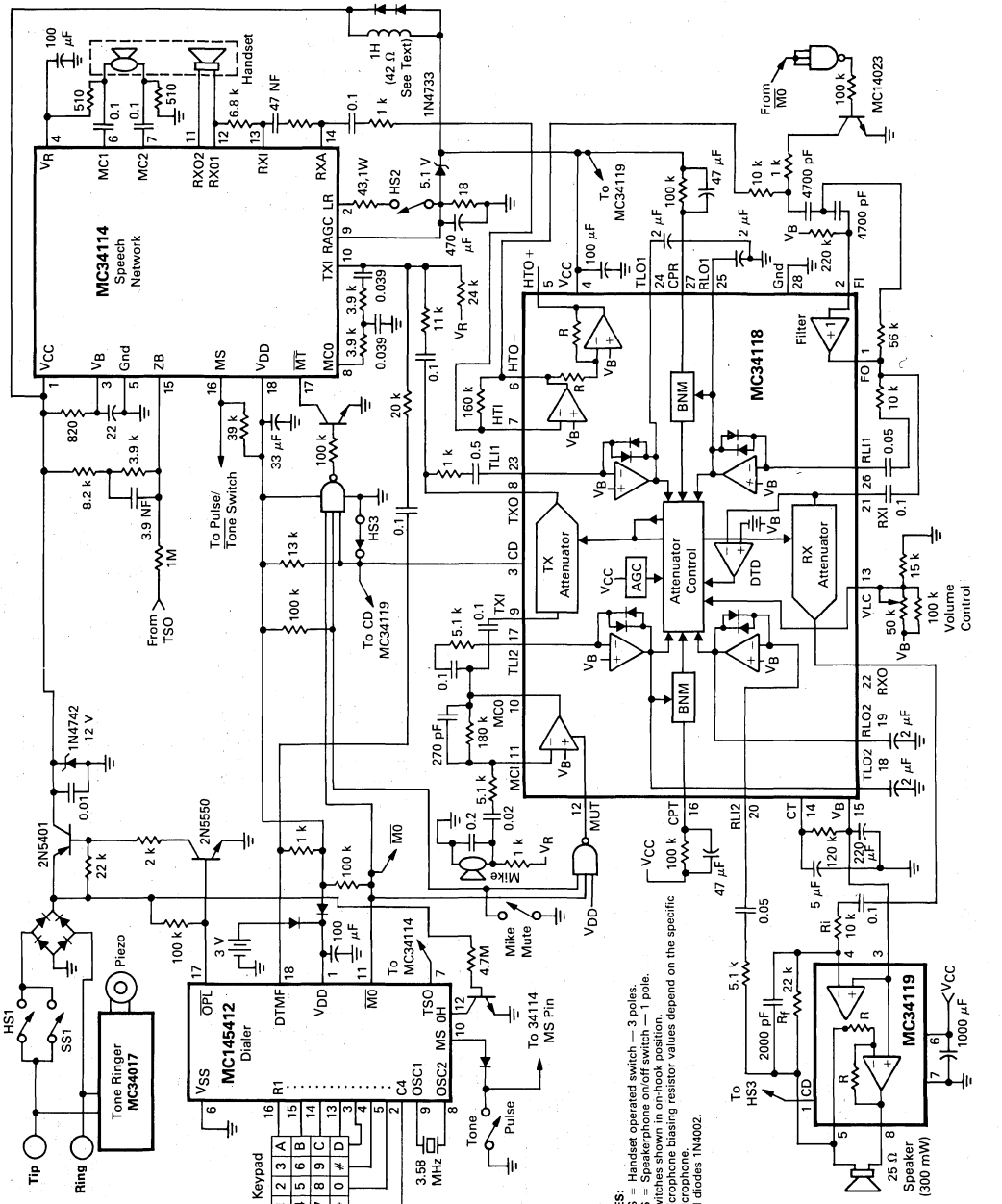


FIGURE 33 — PULSE/TONE FEATUREPHONE WITH MEMORY — LINE POWERED

EMI SUSCEPTIBILITY

Potential EMI susceptibility problems should be addressed early in the electrical and mechanical design of the telephone. EMI may enter the circuit through Tip and Ring, through the microphone wiring, or through any of the PC board traces. The most sensitive pins on the MC34114 are the microphone amplifier inputs (MC1, MC2). Board traces to these pins should be kept short, and the associated components should preferably be physically close to the pins. TXI, RXI, and ZB should also be considered sensitive to EMI signals.

The microphone wires within the handset cord can act as an antenna, and pick up nearby radio stations. If this is a problem in the final design, adding RF filters (consisting of ferrite beads and small (0.001 μF) ceramic capacitors) to the PC board where the wires attach to the board can generally reduce the problem.

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, Ill. 60106
312-595-1022
Model EM-60

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

Hosiden America Corp.
Elk Grove Village, Ill. 60007
312-981-1144
Model KUC2123

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
516-561-6050
Ask for Applications
Bulletin F232

Stancor Products
Logansport, IN 46947
219-722-2244

PREM Magnetics, Inc.
McHenry, Ill. 60050
815-385-2700

Onan Power/Electronics
Minneapolis, MN 55437
612-921-5600

Motorola Inc. does not endorse or warrant the suppliers referenced.
Compliance with FCC or other regulatory agencies of the circuits described herein is not implied or guaranteed by Motorola Inc.

MC34115

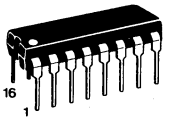
Specifications and Applications Information

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

Providing a simplified approach to digital speech encoding/decoding, the MC34115 CVSD is designed for speech synthesis and commercial telephone applications. A single IC provides both encoding and decoding functions.

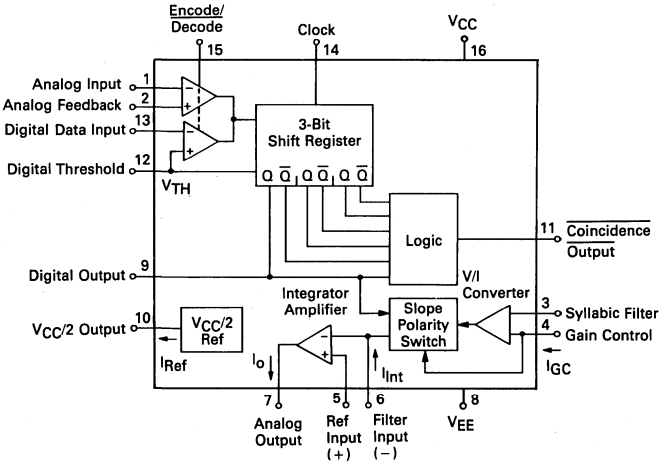
- Encode and Decode Functions Selectable with a Digital Input
- Utilization of Compatible I^2L — Linear Bipolar Technology
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable ($V_{CC}/2$ reference provided on chip)
- 3-Bit Algorithm

CONTINUOUSLY VARIABLE SLOPE DELTA MODULATOR/DEMODULATOR

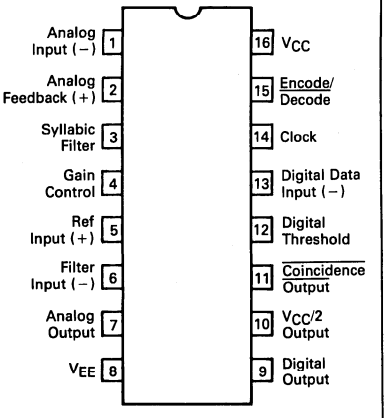


P SUFFIX
PLASTIC PACKAGE
CASE 648

CVSD BLOCK DIAGRAM



PIN CONNECTIONS



MAXIMUM RATINGS

(All voltages referenced to V_{EE}, T_A = 25°C unless otherwise noted.) (See Note 2.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.4 to +18	Vdc
Differential Analog Input Voltage	V_{ID}	±5.0	Vdc
Digital Threshold Voltage	V_{TH}	−0.4 to V_{CC}	Vdc
Logic Input Voltage (Clock, Digital Data, Encode/$\overline{\text{Decode}}$)	V_{Logic}	−0.4 to +18	Vdc
Coincidence Output Voltage	$V_{O(Con)}$	−0.4 to +18	Vdc
Syllabic Filter Input Voltage	$V_{I(Syl)}$	−0.4 to V_{CC}	Vdc
Gain Control Input Voltage	$V_{I(GC)}$	−0.4 to V_{CC}	Vdc
Reference Input Voltage	$V_{I(Ref)}$	$V_{CC}/2$ − 1.0 to V_{CC}	Vdc
$V_{CC}/2$ Output Current	I_{Ref}	−25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, V_{EE} = Gnd, T_A = 0°C to + 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range (Figure 1)	V_{CC}	4.75	12	16.5	Vdc
Power Supply Current (Figure 1) (Idle Channel)	I_{CC}				mA
V_{CC} = 5.0 V		—	4.6	7.5	
V_{CC} = 15 V		—	7.0	12	
Clock Rate	SR	—	16 k	—	Samples/s
Gain Control Current Range (Figure 2)	I_{GCR}	0.002	—	3.0	mA
Analog Comparator Input Range (Pins 1 and 2) 4.75 V ≤ V_{CC} ≤ 16.5 V	V_I	1.3	—	V_{CC} − 1.3	Vdc
Analog Output Range (Pin 7) 4.75 V ≤ V_{CC} ≤ 16.5 V, I_O = ±5.0 mA	V_O	1.3	—	V_{CC} − 1.3	Vdc
Input Bias Currents (Figure 3)	I_{IB}				μA
Comparator in Active Region					
Analog Input (I1)		—	0.5	2.5	
Analog Feedback (I2)		—	0.5	2.5	
Syllabic Filter Input (I3)		—	0.06	0.5	
Reference Input (I5)		—	−0.06	−0.5	
Input Offset Current	I_{IO}				μA
Comparator in Active Region					
Analog Input/Analog Feedback |I1–I2| — Figure 3		—	0.15	0.8	
Integrator Amplifier |I5–I6| — Figure 4		—	0.02	0.2	
Input Offset Voltage V/I Converter (Pins 3 and 4) — Figure 5	V_{IO}	—	2.0	10	mV
Transconductance	gm				mA/mV
V/I Converter, 0 to 3.0 mA		0.1	0.3	—	
Integrator Amplifier, 0 to +5.0 mA Load		1.0	10	—	
Propagation Delay Times (Note 1)					μs
Clock Trigger to Digital Output	t_{PLH}	—	1.0	3.0	
C_L = 25 pF to Gnd	t_{PHL}	—	0.8	3.0	
Clock Trigger to Coincidence Output	t_{PLH}	—	1.0	3.5	
C_L = 25 pF to Gnd	t_{PHL}	—	0.8	2.5	
R_L = 4.0 kΩ to V_{CC}					

NOTES 1. All propagation delay times measured 50% to 50% from the negative going (from V_{CC} to +0.4 V) edge of the clock.
2. Devices should not be operated at these values. The "Electrical Characteristics" provide conditions for actual device operation.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Coincidence Output Voltage — Low Logic State $I_{OL(Con)}$ = 3.0 mA	$V_{OL(Con)}$	—	0.12	0.25	Vdc
Coincidence Output Leakage Current — High Logic State V_{OH} = 15 V	$I_{OH(Con)}$	—	0.01	0.5	μA
Applied Digital Threshold Voltage Range (Pin 12)	V_{TH}	+1.2	—	V_{CC} −2.0	Vdc
Digital Threshold Input Current 1.2 V ≤ V_{th} ≤ V_{CC} −2.0 V	$I_{I(th)}$				μA
V_{IL} applied to Pins 13, 14 and 15		—	—	5.0	
V_{IH} applied to Pins 13, 14 and 15		—	−10	−50	
Maximum Integrator Amplifier Output Current	I_O	±5.0	—	—	mA
V_{CC}/2 Generator Maximum Output Current (Source only)	I_{Ref}	+10	—	—	mA
V_{CC}/2 Generator Output Impedance 0 to +10 mA	z_{Ref}	—	3.0	6.0	Ω
V_{CC}/2 Generator Tolerance 4.75 V ≤V_{CC}≤16.5 V	ϵ_r	—	—	±3.5	%
Logic Input Voltage (Pins 13, 14 and 15)					Vdc
Low Logic State	V_{IL}	Gnd	—	V_{th} −0.4	
High Logic State	V_{IH}	V_{th} +0.4	—	16.5	
Dynamic Total Loop Offset Voltage (Note 3) — Figures 3, 4 and 5	ΣV_{offset}				mV
I_{GC} = 33 μA, V_{CC} = 12 V					
T_A = 25°C		—	±2.5	±7.0	
0°C ≤ T_A ≤ +70°C		—	±3.0	±10	
I_{GC} = 33 μA, V_{CC} = 5.0 V					
T_A = 25°C		—	±4.0	±8.0	
0°C ≤ T_A ≤ +70°C		—	±4.5	±12	
Digital Output Voltage (Pin 9)					Vdc
I_{OL} = 3.6 mA	V_{OL}	—	0.1	0.4	
I_{OH} = −0.35 mA	V_{OH}	V_{CC} −1.0	V_{CC} −0.2	—	
Syllabic Filter Applied Voltage (Pin 3)	$V_{I(Syl)}$	+3.2	—	V_{CC}	Vdc
Integrating Current (Figure 2)	$\lvert I_{Int} \rvert$				
I_{GC} = 12 μA		8.0	10	12	μA
I_{GC} = 1.5 mA		1.4	1.5	1.6	mA
I_{GC} = 3.0 mA		2.75	3.0	3.25	mA
Dynamic Integrating Current Match (Figure 6) I_{GC} = 1.5 mA	$V_{O(Ave)}$	—	±100	±300	mV
Input Current — High Logic State V_{IH} = 16.5 V	I_{IH}				μA
Digital Data Input		—	—	+5.0	
Clock Input		—	—	+5.0	
Encode/$\overline{\text{Decode}}$ Input		—	—	+5.0	
Input Current — Low Logic State V_{IL} = 0 V	I_{IL}				μA
Digital Data Input		—	—	−10	
Clock Input		—	—	−360	
Encode/$\overline{\text{Decode}}$ Input		—	—	−36	
Clock Input, V_{IL} = 0.4 V		—	—	−72	

NOTE 3. Dynamic total loop offset (ΣV_{offset}) equals V_{IO} (comparator) (Figure 3) minus V_{IOX} (Figure 5). The input offset voltages of the analog comparator and of the integrator amplifier include the effects of input offset current through the input resistors. The slope polarity switch current mismatch appears as an average voltage across the 10 k integrator resistor. The clock frequency is 16 kHz. Idle channel performance is guaranteed if this dynamic total loop offset is less than one-half of the change in integrator output voltage during one clock cycle (ramp step size).

DEFINITIONS AND FUNCTION OF PINS

Pin 1 — Analog Input

This is the analog comparator inverting input where the voice signal is applied. It may be ac or dc coupled depending on the application. If the voice signal is to be level shifted to the internal reference voltage, then a bias resistor between Pins 1 and 10 is used. The resistor is used to establish the reference as the new dc average of the ac coupled signal. The analog comparator was designed for low hysteresis (typically less than 0.1 mV) and high gain (typically 70 dB).

Pin 2 — Analog Feedback

This is the non-inverting input to the analog signal comparator within the IC. In an encoder application it should be connected to the analog output of the encoder circuit. This may be Pin 7 or a low pass filter output connected to Pin 7. In a decode circuit Pin 2 is not used and may be tied to $V_{CC}/2$ on Pin 10, ground or left open.

The analog input comparator has bias currents of 2.5 μA max, thus the driving impedances of Pins 1 and 2 should be equal to avoid disturbing the idle channel characteristics of the encoder.

Pin 3 — Syllabic Filter

This is the point at which the syllabic filter voltage is returned to the IC in order to control the integrator step size. It is an NPN input to an op amp. The syllabic filter consists of an RC network between Pins 11 and 3. Typical time constant values of 6 ms to 50 ms are used in voice codecs.

Pin 4 — Gain Control Input

The syllabic filter voltage appears across C_S of the syllabic filter and is the voltage between V_{CC} and Pin 3. The active voltage to current (V–I) converter drives Pin 4 to the same voltage at a slew rate of typically 0.5 V/μs. Thus the current injected into Pin 4 (I_{GC}) is the syllabic filter voltage divided by the R_X resistance. Figure 7 shows the relationship between I_{GC} (x-axis) and the integrating current, I_{Int} (y-axis). The discrepancy, which is most significant at very low currents, is due to circuitry within the slope polarity switch which enables trimming to a low total loop offset. The R_X resistor is then varied to adjust the loop gain of the codec, but should be no larger than 5.0 kΩ to maintain stability.

Pin 5 — Reference Input

This pin is the non-inverting input of the integrator amplifier. It is used to reference the dc level of the output signal. In an encoder circuit it must reference the same voltage as Pin 1 and is tied to Pin 10.

Pin 6 — Filter Input

This inverting op amp input is used to connect the integrator external components. The integrating current (I_{Int}) flows into Pin 6 when the analog input (Pin 1) is high with respect to the analog feedback (Pin 2) in the encode mode or when the digital data input (Pin 13) is high in the decode mode. For the opposite states, I_{Int} flows out of Pin 6. Single integration systems require a capacitor and resistor between Pins 6 and 7. Multipole configurations will have different circuitry. The resistance between Pins 6 and 7 should typically be between 8 kΩ and 13 kΩ to maintain good idle channel characteristics.

Pin 7 — Analog Output

This is the integrator op amp output. It is capable of driving a 600-ohm load referenced to $V_{CC}/2$ to +6 dBm and can otherwise be treated as an op amp output. Pins 5, 6, and 7 provide full access to the integrator op amp for designing integration filter networks. The slew rate of the internally compensated integrator op amp is typically 0.5 V/μs. Pin 7 output is current limited for both polarities of current flow at typically 30 mA.

Pin 8 — V_{EE}

The circuit is designed to work in either single or dual power supply applications. Pin 8 is always connected to the most negative supply.

Pin 9 — Digital Output

The digital output provides the results of the delta modulator's conversion. It swings between V_{CC} and V_{EE} and is CMOS or TTL compatible. Pin 9 is inverting with respect to Pin 1 and non-inverting with respect to Pin 2. It is clocked on the falling edge of Pin 14. The typical 10% to 90% rise and fall times are 250 ns and 50 ns respectively for V_{CC} = 12 V and C_L = 25 pF to ground.

Pin 10 — $V_{CC}/2$ Output

An internal low impedance mid-supply reference is provided for use of the MC34115 in single supply applications. The internal regulator is a current source and must be loaded with a resistor to insure its sinking capability. If a +6 dBmo signal is expected across a 600 ohm input bias resistor, then Pin 10 must sink 2.2 V/600 Ω = 3.66 mA. This is only possible if Pin 10 sources 3.66 mA into a resistor normally and will source only the difference under peak load. The reference load resistor is chosen accordingly. A 0.1 μF bypass capacitor from Pin 10 to V_{EE} is also recommended. The $V_{CC}/2$ reference is capable of sourcing 10 mA and can be used as a reference elsewhere in the system circuitry.

Pin 11 — $\overline{\text{Coincidence Output}}$

The coincidence output will be low whenever the content of the internal 3 bit shift register is all 1s or all 0s. Pin 11 is an open collector of an NPN device and requires a pull-up resistor. If the syllabic filter is to have equal charge and discharge time constants, the value of R_p should be much less than R_S. In systems requiring different charge and discharge constants, the charging

constant is $R_S C_S$ while the decaying constant is $(R_S + R_P)C_S$. Thus longer decays are easily achievable. The NPN device should not be required to sink more than 3 mA. The typical 10% to 90% rise and fall times are 200 ns and 100 ns respectively for R_L = 4 kΩ to +12 V and C_L = 25 pF to ground.

Pin 12 — Digital Threshold

This input sets the switching threshold for Pins 13, 14, and 15. It is intended to aid in interfacing different logic families without external parts. Typically it is connected to the $V_{CC}/2$ reference for CMOS interface or can be biased two diode drops above V_{EE} for TTL interface.

Pin 13 — Digital Data Input

In a decode application, the digital data stream is applied to Pin 13. In an encoder it may be unused or may be used to transmit signaling message under the control of Pin 15. It is an inverting input with respect to Pin 9. When Pins 9 and 13 are connected, a toggle flip-flop is formed and a forced idle channel pattern can be transmitted. The digital data input level should be maintained for 0.5 μs before and after the clock trigger for proper clocking.

Pin 14 — Clock Input

The clock input determines the data rate of the codec circuit. A 16K bit rate requires a 16 kHz clock. The switching threshold of the clock input is set by Pin 12. The shift register circuit toggles on the falling edge of the clock input. The minimum width for a positive-going pulse on the clock input is 300 ns, whereas for a negative-going pulse, it is 900 ns.

Pin 15 — Encode/$\overline{\text{Decode}}$

This pin controls the connection of the analog input comparator and the digital input comparator to the internal shift register. If high, the result of the analog comparison will be clocked into the register on the falling edge at Pin 14. If low, the digital input state will be entered. This allows use of the IC as an encoder/decoder or simplex codec without external parts. Furthermore, it allows non-voice patterns to be forced onto the transmission line through Pin 13 in an encoder.

Pin 16 — V_{CC}

The power supply range is from 4.75 to 16.5 volts between pin V_{CC} and V_{EE}.

FIGURE 1 — POWER SUPPLY CURRENT

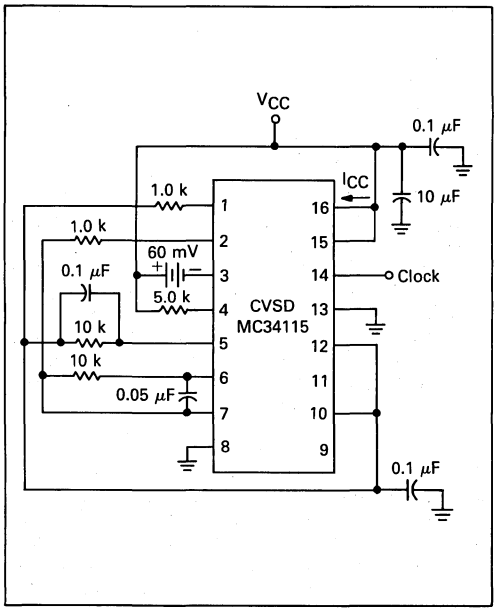


FIGURE 2 — I_{GCR}, GAIN CONTROL RANGE and I_{Int} — INTEGRATING CURRENT

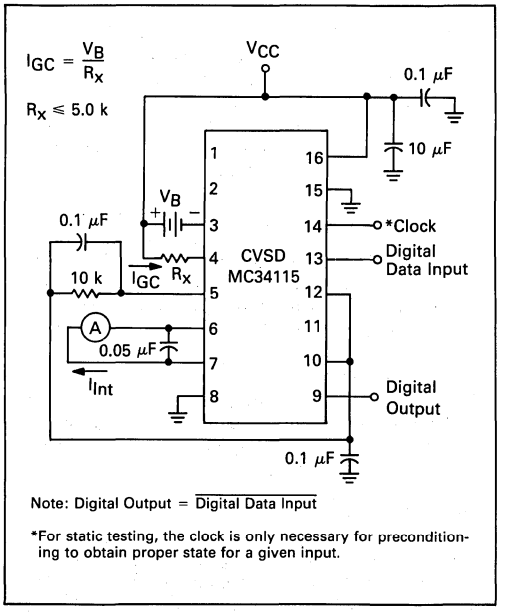
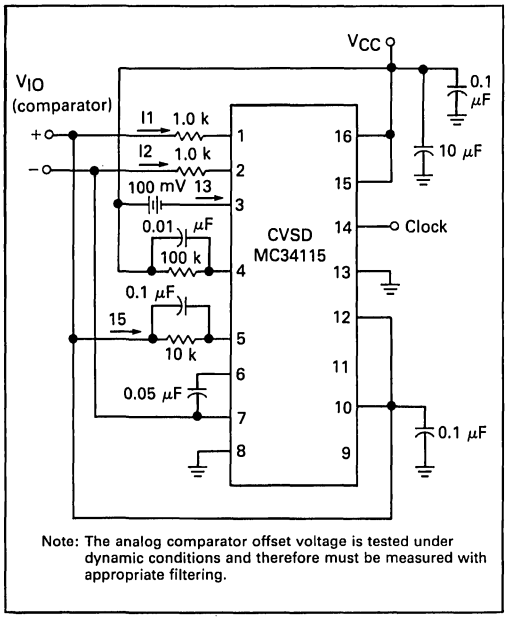


FIGURE 3 — INPUT BIAS CURRENTS, ANALOG COMPARATOR OFFSET VOLTAGE AND CURRENT



Note: The analog comparator offset voltage is tested under dynamic conditions and therefore must be measured with appropriate filtering.

FIGURE 4 — INTEGRATOR AMPLIFIER OFFSET VOLTAGE AND CURRENT

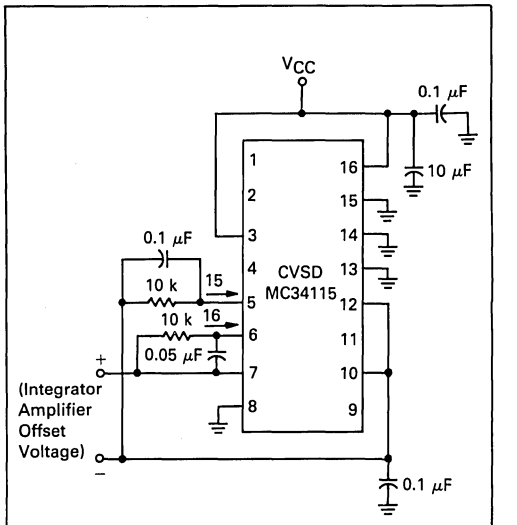
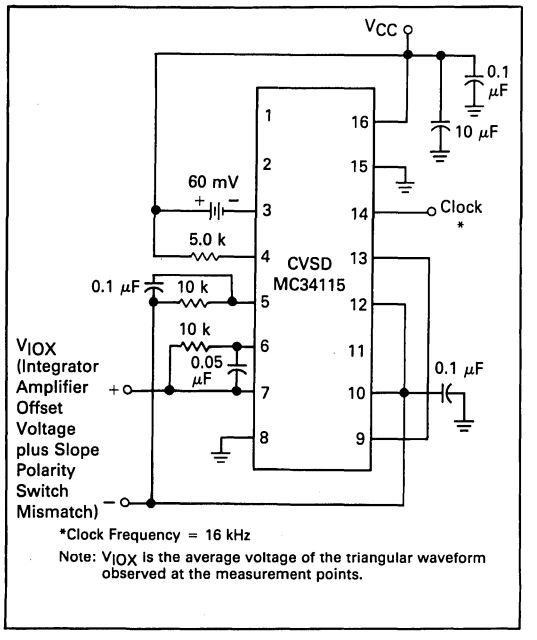


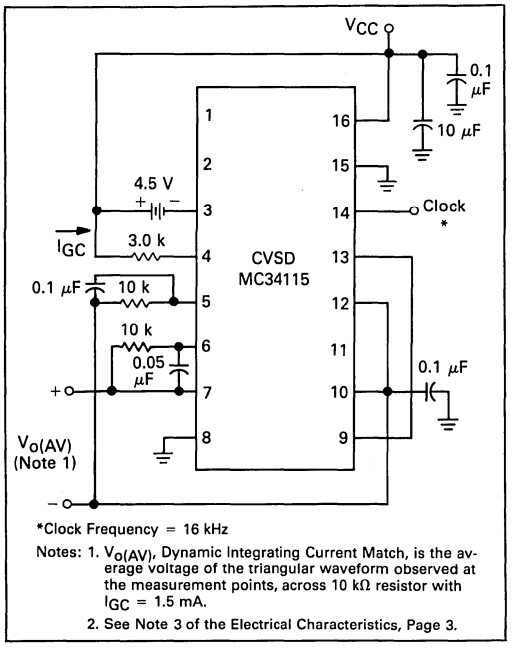
FIGURE 5 — V/I CONVERTER OFFSET VOLTAGE, V_{IO} and V_{IOX}



*Clock Frequency = 16 kHz

Note: V_{IOX} is the average voltage of the triangular waveform observed at the measurement points.

FIGURE 6 — DYNAMIC INTEGRATING CURRENT MATCH



*Clock Frequency = 16 kHz

Notes: 1. $V_{O(AV)}$, Dynamic Integrating Current Match, is the average voltage of the triangular waveform observed at the measurement points, across 10 kΩ resistor with I_{GC} = 1.5 mA.

2. See Note 3 of the Electrical Characteristics, Page 3.

TYPICAL PERFORMANCE CURVES

FIGURE 7 — TYPICAL I_{Int} versus I_{GC} (Mean ± 2σ)

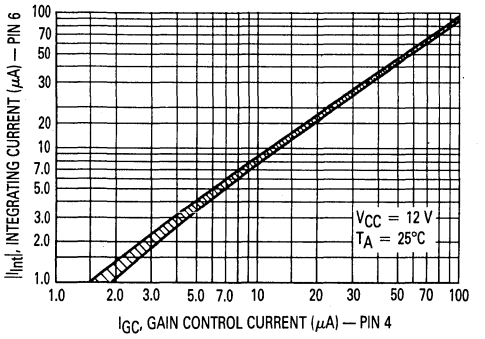


FIGURE 8 — NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus V_{CC}

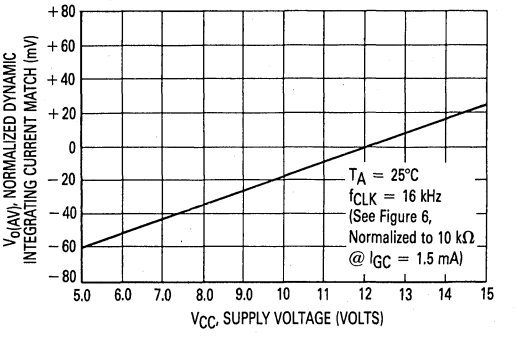


FIGURE 9 — NORMALIZED DYNAMIC INTEGRATING CURRENT MATCH versus CLOCK FREQUENCY

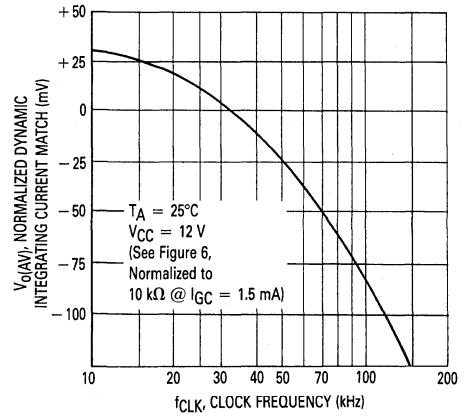


FIGURE 10 — DYNAMIC TOTAL LOOP OFFSET versus CLOCK FREQUENCY

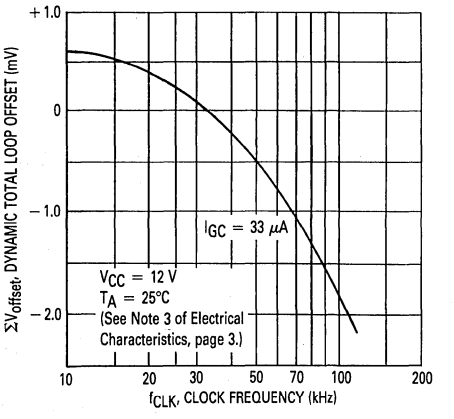


FIGURE 11 — BLOCK DIAGRAM OF THE CVSD ENCODER

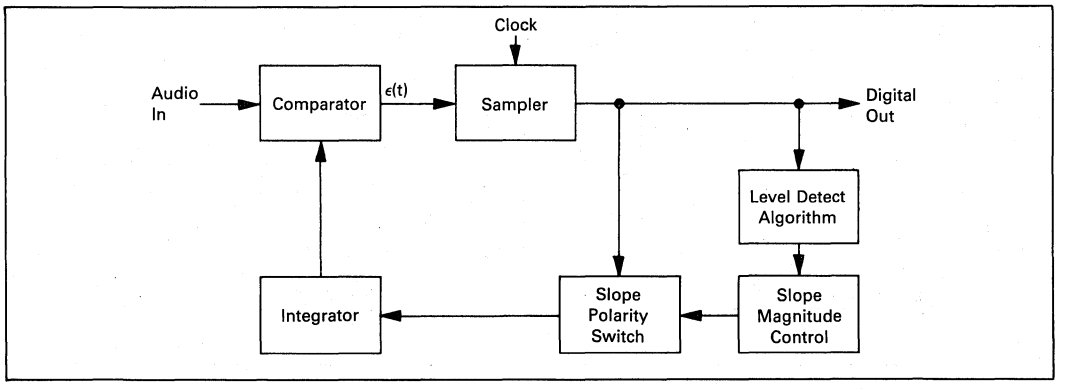


FIGURE 12 — CVSD WAVEFORMS

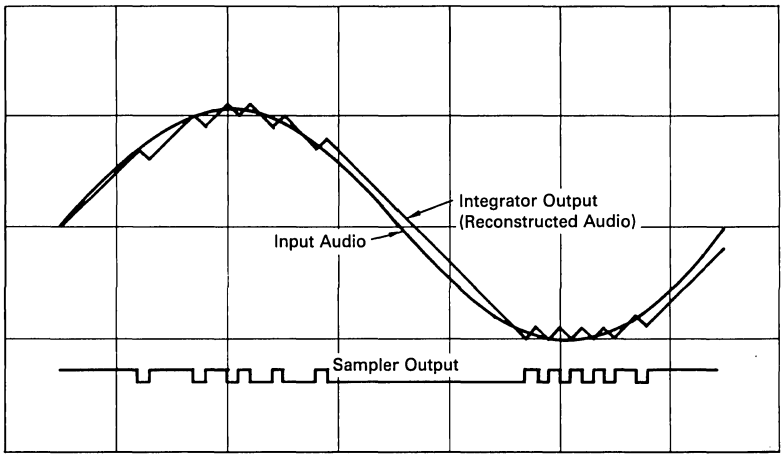
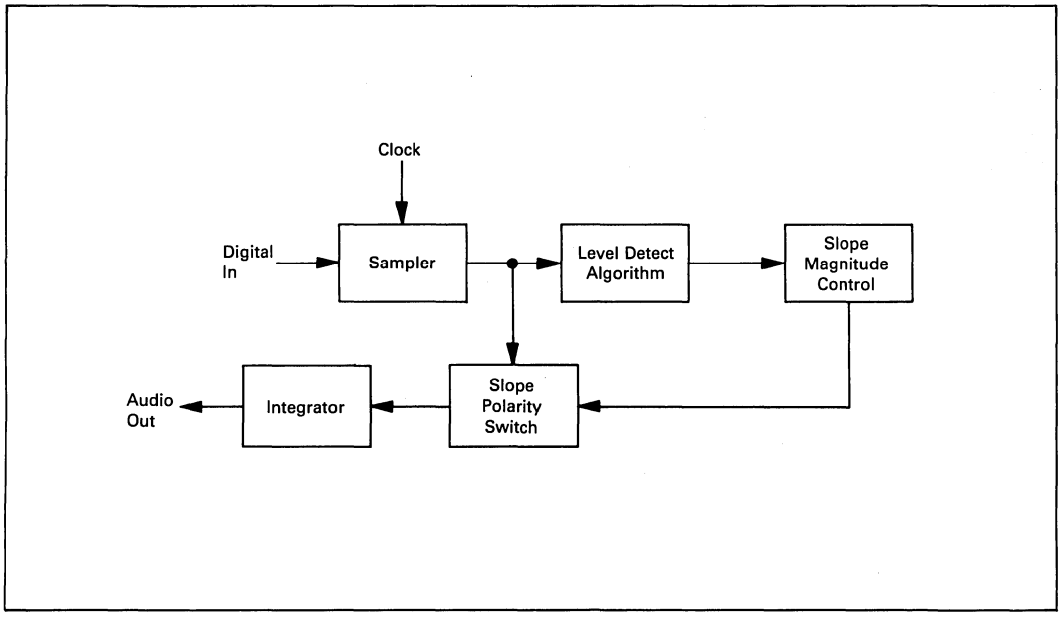
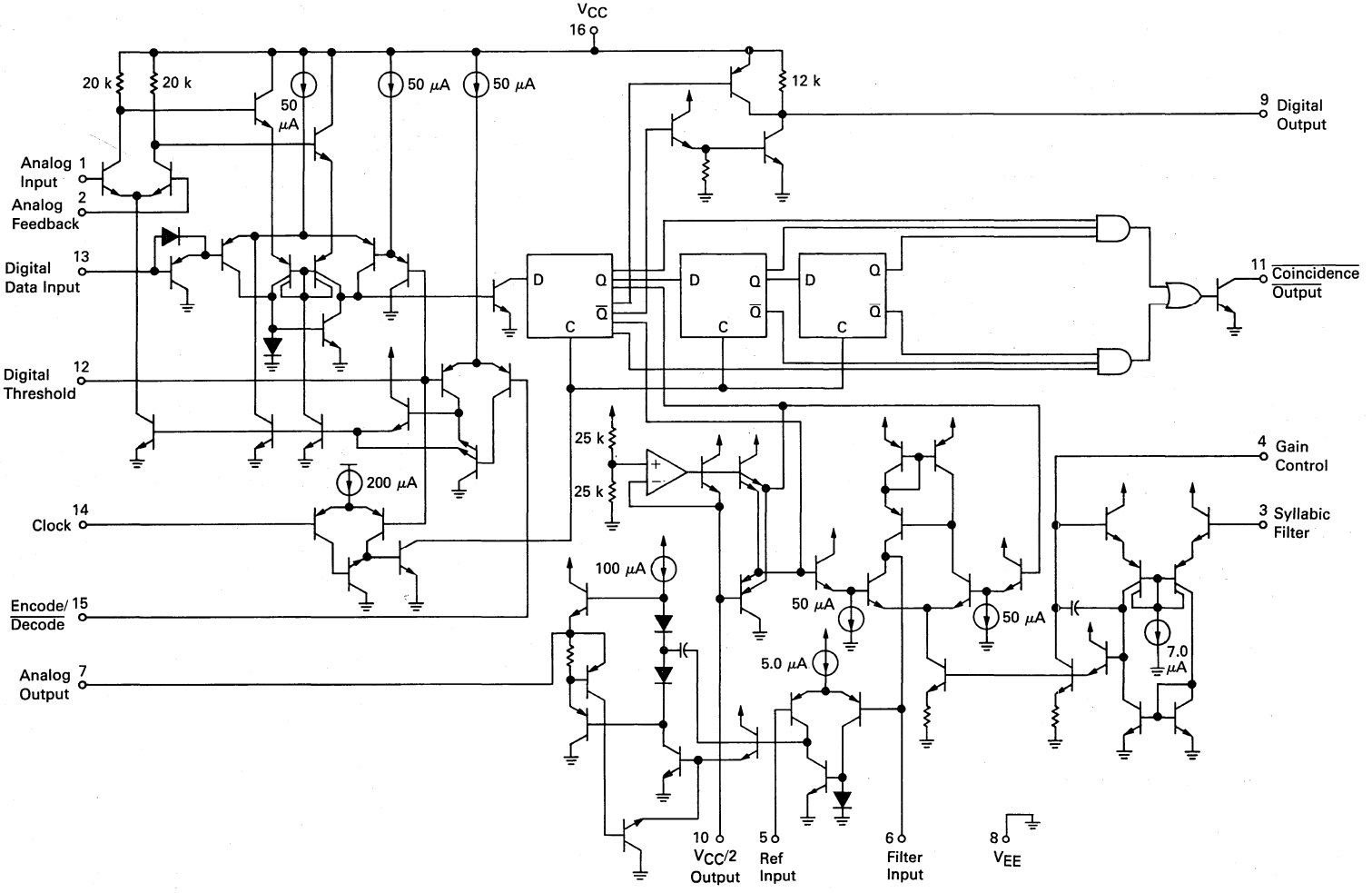


FIGURE 13 — BLOCK DIAGRAM OF THE CVSD DECODER



CVSD CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission and multiplexing, switching and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not meet the communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economically efficient means of digitizing analog inputs for transmission.

The Delta Modulator

The innermost control loop of a CVSD converter is a simple delta modulator. A block diagram CVSD Encoder is shown in Figure 11. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the intregrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting locations tracks the input signal, the remote receiver reproduces the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise, if the clock rate of the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates from 8 k and up are possible. Thus the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to zero and receive restart begins without framing when the receiver reacquires. Similarly a delta modulator is tolerant of sporadic bit errors. Figure 12 shows the delta modulator waveforms while Figure 13 shows the corresponding CVSD decoder block diagram.

The Companding Algorithm

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be band limited and amplitude limited. The frequency limitations are governed by the nyquist rate while the amplitude capabilities are set by the gain of the integrator.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth which will transmit the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For a signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 bits long. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all 1s or 0s. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low pass filter. The voltage output of this syllabic filter controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

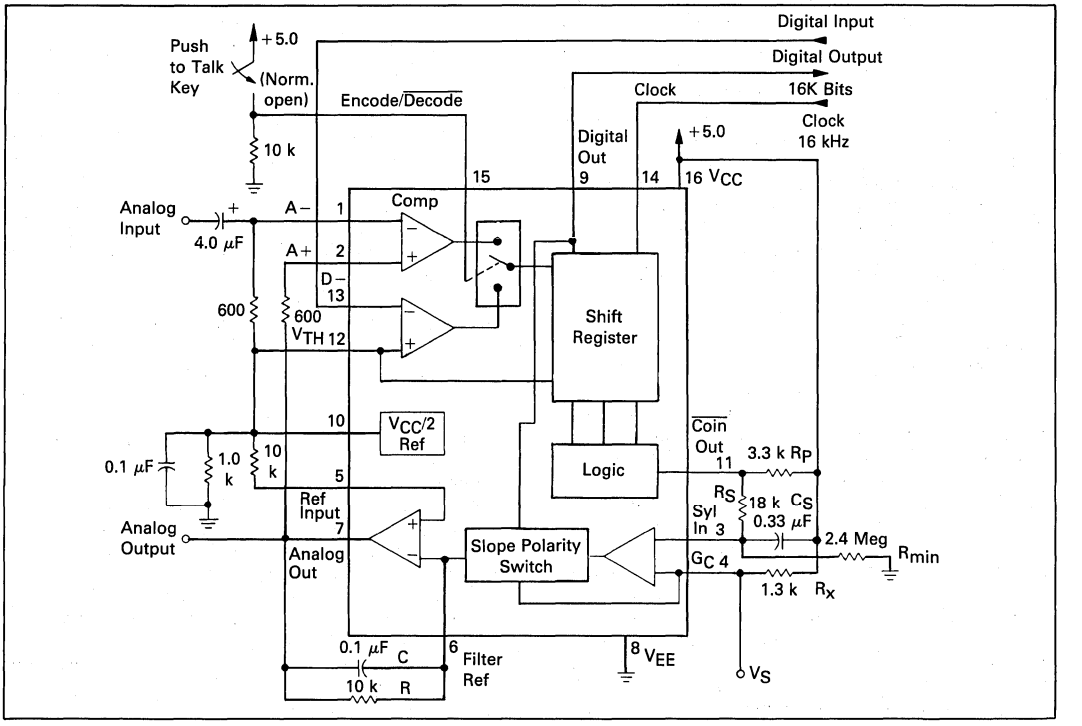
The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus a measure of the average input level is what is needed.

The algorithm is repeated in the receiver and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If a CVSD encoder is played into a basic delta modulator, the output of the delta modulator will reflect the shape of the input signal but all of the output will be at an equal level. Thus the algorithm at the output is needed to restore the level variations. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing a voice input in a manner which is especially convenient for digital communications requirements.

FIGURE 14 — 16 kHz SIMPLEX VOICE CODEC
(Using MC34115, Single Pole Companding and Single Integration)



APPLICATIONS INFORMATION

CVSD DESIGN CONSIDERATIONS

A simple CVSD encoder using the MC34115 is shown in Figure 14. This IC is a general purpose CVSD building block which allow the system designer to tailor the encoder's transmission characteristics to the application. Thus, the achievable transmission capabilities are constrained by the fundamental limitations of delta modulation and the design of encoder parameters. The performance is not dictated by the internal configuration of the MC34115. There are six design considerations involved in designing the basic CVSD building block into a specific codec application.

These are listed below:

1. Selection of clock rate
2. Selection of loop gain
3. Selection of minimum step size
4. Design of integration filter transfer function
5. Design of syllabic filter transfer function
6. Design of low pass filter at the receiver

The circuit in Figure 14 is the most basic CVSD circuit possible. For many applications in secure radio or other intelligible voice channel requirements, it is entirely sufficient. In this circuit, items 4 and 5 are reduced to their simplest form. They syllabic and integration filters are both single pole networks. The selection of items 1 through 3 govern the codec performance.

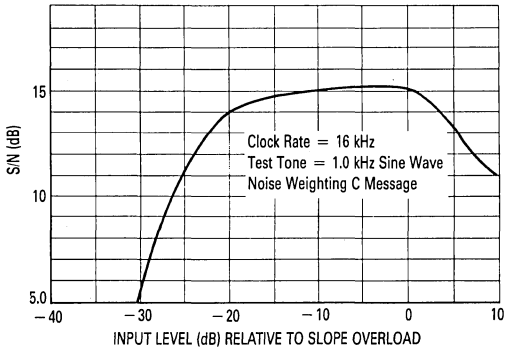
Layout Considerations

Care should be exercised to isolate all digital signal paths (Pins 9, 11, 13, and 14) from analog signal paths (Pins 1–7 and 10) in order to achieve proper idle channel performance.

Clock Rate

With minor modifications the circuit in Figure 14 may be operated anywhere from 9.6 kHz to 64 kHz clock rates. Obviously the higher the clock rate the higher the S/N performance. The circuit in Figure 14 typically produces the S/N performance shown in Figure 15. The selection of clock rate is usually dictated by the bandwidth of the transmission medium. Voice bandwidth systems will require no higher than 9600 Hz. Some radio systems will allow 12 kHz. Private 4-wire telephone systems are often operated at 16 kHz and commercial telephone performance can be achieved at 32K bits and above.

FIGURE 15 — SIGNAL-TO-NOISE PERFORMANCE OF MC34115 WITH SINGLE INTEGRATION, SINGLE-POLE AND COMPANDING AT 16K BITS — TYPICAL



Selection of Loop Gain

The gain of the circuit in Figure 14 is set by resistor R_X. R_X must be selected to provide the proper integrator step size for high level signals such that the companding ratio does not exceed about 25%. The companding ratio is the active low duty cycle of the coincidence output on Pin 11 of the codec circuit. Thus the system gain is dependent on:

1. The maximum level and frequency of the input signal.
2. The transfer function of the integration filter.

For voice codecs the typical input signal is taken to be a sine wave at 1 kHz of 0 dBmo level. In practice, the useful dynamic range extends about 6 dB above the design level. In any system the companding ratio should not exceed 30%.

To calculate the required step size current, we must describe the transfer characteristics of the integration filter. In the basic circuit of Figure 14, a single pole of 160 Hz is used.

$$R = 10\ k\Omega,\ C = 0.1\ \mu F$$

$$\frac{V_o}{I_i} = \frac{1}{C(S + 1/RC)} \equiv \frac{K}{S + \omega_o}$$

$$\omega_o = 2\pi f$$

$$10^3 = \omega_o = 2\pi f$$

$$f = 159.2\ Hz$$

Note that the integration filter produces a single-pole response from 300 to 3 kHz. The current required to move the integrator output a specific voltage from zero is simply:

$$I_i = \frac{V_o}{R} + C\frac{dV_o}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of a sine wave centered around the zero crossing, the sine wave changes by approximately its peak value. The CVSD step should trace that change. The required current for a 0 dBm 1 kHz sine wave is:

$$I_i = \frac{1.1\ V}{*2(10\ k\Omega)} + \frac{0.1\ \mu F(1.1)}{0.125\ ms} = 0.935\ mA$$

*The maximum voltage across R when maximum slew is required is:

$$\frac{1.1\ V}{2}$$

Now the voltage range of the syllabic filter is the power supply voltage, thus:

$$R_X = 0.25(V_{CC})\frac{1}{0.935\ mA}$$

A similar procedure can be followed to establish the proper gain for any input level and integration filter type.

Minimum Step Size

The final parameter to be selected for the simple codec in Figure 14 is idle channel step size. With no input signal, the digital output becomes a one-zero alternating pattern and the analog output becomes a small triangle wave. Mismatches of internal currents and offsets limit the minimum step size which will produce a perfect idle channel pattern. The MC34115 is tested to ensure that a 20 mVp-p mimimum step size at 16 kHz will attain a proper idle channel. The idle channel step size must be twice the specified total loop offset if a one-zero idle pattern is desired. In some applications a much smaller minimum step size (e.g., 0.1 mV) can produce quiet performance without providing a 1-0 pattern.

To set the idle channel step size, the value of R_{min} must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter capacitor (C_S) would decay to zero. However, the voltage divider of R_S and R_{min} (see Figure 14) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage must produce the desired ramps at the analog output. Again we write the filter input current equation:

$$I_i = \frac{V_o}{R} + C\frac{dV_o}{dt}$$

For values of V_o near $V_{CC}/2$ the V_o/R term is negligible; thus

$$I_i = C_S\frac{\Delta V_o}{\Delta T}$$

where ΔT is the clock period and ΔV_o is the desired peak-to-peak value of the idle output. For a 16K-bit system using the circuit in Figure 14

$$I_i = \frac{0.1\ \mu F\ 20\ mV}{62.5\ \mu s} = 32\ \mu A$$

The voltage on C_S which produces a 32 μA current is determined by the value of R_X.

$$I_i R_X = V_S min;\ \text{for } 32\ \mu A,\ V_S min = 41.6\ mV$$

In Figure 14 R_S is 18 kΩ. That selection is discussed with the syllabic filter considerations. The voltage divider of R_S and R_{min} must produce an output of 41.6 mV.

$$V_{CC}\frac{R_S}{R_S + R_{min}} = V_S min \quad R_{min} \simeq 2.4\ M\Omega$$

Having established these three parameters — clock rate, loop gain and minimum step size — the encoder circuit in Figure 14 will function at near optimum performance for input levels around 0 dBm.

INCREASING CVSD PERFORMANCE

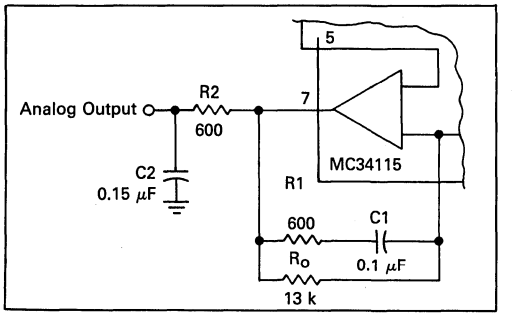
Integration Filter Design

The circuit in Figure 14 uses a single-pole integration network formed with a 0.1 μF capacitor and a 10 kΩ resistor. It is possible to improve the performance of the circuit in Figure 14 by 1 or 2 dB by using a two-pole integration network. The improved circuit is shown.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephony circuits, the second pole can be placed above 1.8 kHz to exceed the 1633 touchtone frequency. In other communication systems, values as low as 1 kHz may be selected. In general, the lower in frequency the second pole is placed, the greater the noise improvement. Then, to ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low-pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 235 Hz, 2 kHz and 5.2 kHz is typical for telephone applications while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. (Voice only channels can use an output low-pass filter which breaks at about 2.5 kHz.) The two-pole network in Figure 16 has a transfer function of:

$$\frac{V_o}{I_i} = \frac{R_0R_1\left(S + \frac{1}{R_1C_1}\right)}{R_2C_2(R_0 + R_1)\left(S + \frac{1}{(R_0 + R_1)C_1}\right)S + \left(\frac{1}{R_2C_2}\right)}$$

FIGURE 16 — IMPROVED FILTER CONFIGURATION



These component values are for the telephone channel circuit poles described in the text. The R2, C2 product can be provided with different values of R and C. R2 should be chosen to be equal to the termination resistor on Pin 1.

Thus the two poles and the zero can be selected arbitrarily as long as the zero is at a higher frequency than the first pole. The values in Figure 16 represent one implementation of the telephony filter requirement.

The selection of the two-pole filter network affects the selection of the loop gain value and the minimum step size resistor. The required integrator current for a given change in voltage now becomes:

$$I_i = \frac{V_o}{R_0} + \left(\frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\right)\frac{\Delta V_o}{\Delta T} + \left(R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\right)\frac{\Delta V_o{}^2}{\Delta T^2}$$

The calculation of desired gain resistor R_X then proceeds exactly as previously described.

Syllabic Filter Design

The syllabic filter in Figure 14 is a simple single-pole network of 18 kΩ and 0.33 μF. This produces a 6.0 ms time constant for the averaging of the coincidence output signal. The voltage across the capacitor determines the integrator current which in turn establishes the step size. The integrator current and the resulting step size determine the companding ratio and the S/N performance. The companding ratio is defined as the voltage across C_S/V_{CC}.

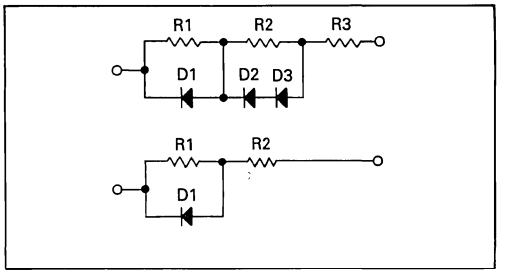
The S/N performance may be improved by modifying the voltage to current transformation produced by R_X. If different portions of the total R_X are shunted by diodes, the integrator current can be other than $(V_{CC} - V_S)/R_X$. These breakpoint curves must be designed experimentally for the particular system application. In general, one would wish that the current would double with input level. To design the desired curve, supply current to Pin 4 of the codec from an external source. Input a signal level and adjust the current until the S/N performance is optimum. Then record the syllabic filter voltage and the current. Repeat this for all desired signal levels. Then derive the resistor diode network which produces that curve on a curve tracer.

Once the network is designed with the curve tracer, it is then inserted in place of R_X in the circuit and the forced optimum noise performance will be achieved from the active syllabic algorithm.

Diode breakpoint networks may be very simple or moderately complex and can improve the usable dynamic range of any codec. In the past they have been used in high performance telephone codecs.

Typical resistor-diode networks are shown in Figure 17.

FIGURE 17 — RESISTOR-DIODE NETWORKS



Output Low Pass Filter

A low pass filter is required at the receiving circuit output to eliminate quantizing noise. In general, the lower the bit rate, the better the filter must be. The filter in Figure 18 provides excellent performance for 12 kHz to 40 kHz systems.

FIGURE 18 — HIGH PERFORMANCE ELLIPTIC FILTER FOR CVSD OUTPUT

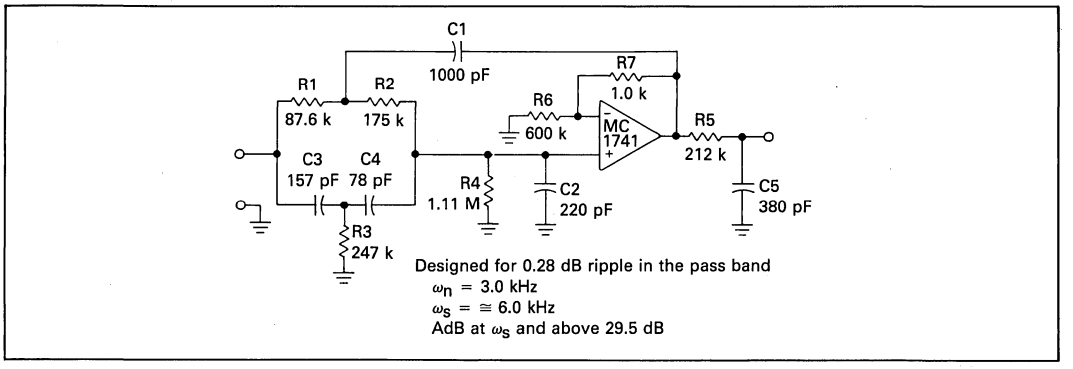
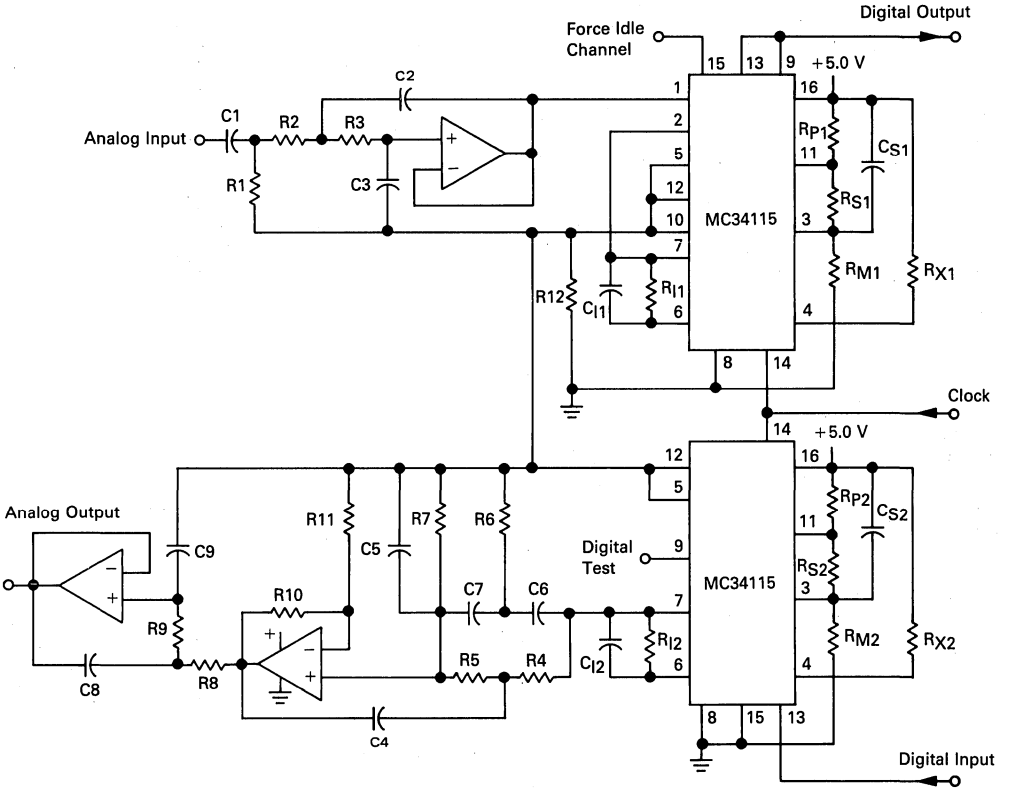


FIGURE 19 — FULL DUPLEX/16K BIT CVSD VOICE CODEC USING MC34115 AND MC3503/6 OP AMP



Codec Components

R_{X1}, R_{X2} — 3.3 kΩ
R_{P1}, R_{P2} — 3.3 kΩ
R_{S1}, R_{S2} — 100 kΩ
R_{I1}, R_{I2} — 20 kΩ
R_{12} — 1 kΩ
R_{M1}, R_{M2} — 10 MΩ
Minimum step size = 20 mV
C_{S1}, C_{S2} — 0.05 μF
C_{I1}, C_{I2} — 0.05 μF
2 MC34115
1 MC3403 (or MC3406)

Note: All Res. 5%
All Cap. 5%

Input Filter Specifications

12 dB/Octave Rolloff above 3.3 kHz
6 dB/Octave Rolloff below 50 Hz

Output Filter Specifications

Break Frequency — 3.3 kHz
Stop Band — 9 kHz
Stop Band Atten. — 50 dB
Rolloff — >40 dB/Octave

Filter Components

R1 — 965 Ω
R2 — 72 kΩ
R3 — 72 kΩ
R4 — 63.46 kΩ
R5 — 127 kΩ
R6 — 365.5 kΩ
R7 — 1.645 MΩ
R8 — 72 kΩ
R9 — 72 kΩ
R10 — 29.5 kΩ
R11 — 72 kΩ

C1 — 3.3 μF
C2 — 837 pF
C3 — 536 pF
C4 — 1000 pF
C5 — 222 pF
C6 — 77 pF
C7 — 38 pF
C8 — 837 pF
C9 — 536 pF

Note: All Res. 0.1% to 1%.
All Cap. 1.0%

MC34118

Specifications and Applications Information

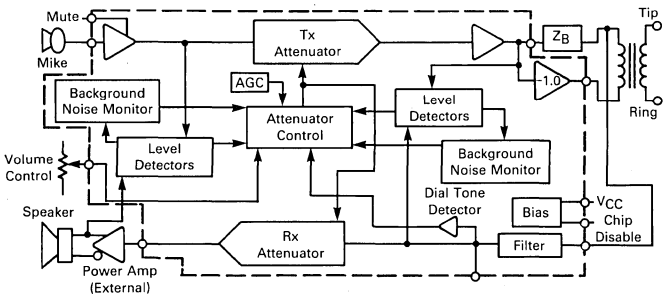
VOICE SWITCHED SPEAKERPHONE CIRCUIT

The MC34118 Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands-free speakerphone system. Included are a microphone amplifier with adjustable gain and MUTE control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at both input and output of both attenuators, and background noise monitors for both the transmit and receive channels. A Dial Tone Detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high-pass filter can be used to filter out 60 Hz noise in the receive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The MC34118 may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The MC34118 can be interfaced directly to Tip and Ring (through a coupling transformer) for stand-alone operation, or it can be used in conjunction with a handset speech network and/or other features of a featurephone.

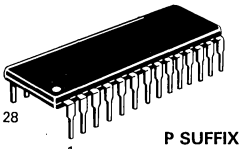
- Improved Attenuator Gain Range: 52 dB Between Transmit and Receive
- Low Voltage Operation for Line-Powered Applications (3.0–6.5 V)
- 4-Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for Both Transmit and Receive Paths
- Microphone Amplifier Gain Set by External Resistors — Mute Function Included
- Chip Disable for Active/Standby Operation
- On Board Filter Pinned-Out for User Defined Function
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Standard 28-Pin Plastic DIP Package and SOIC Package Available
- Compatible with MC34119 Speaker Amplifier

SIMPLIFIED BLOCK DIAGRAM

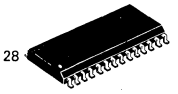


VOICE SWITCHED SPEAKERPHONE CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 710



DW SUFFIX
PLASTIC PACKAGE
CASE 751F

PIN CONNECTIONS

(Top View)

FO	1	28	GND
FI	2	27	CPR
CD	3	26	RLI1
V_{CC}	4	25	RLO1
HTO+	5	24	TLO1
HTO−	6	23	TLI1
HTI	7	22	RXO
TXO	8	21	RXI
TXI	9	20	RLI2
MCO	10	19	RLO2
MCI	11	18	TLO2
MUT	12	17	TLI2
VLC	13	16	CPT
CT	14	15	V_B

(Pin assignments same for both packages)

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltage (Pin 4)	−1.0, +7.0	Vdc
Voltage at CD (Pin 3), MUT (Pin 12)	−1.0, V_{CC} + 1.0	Vdc
Voltage at VLC (Pin 13)	−1.0, V_{CC} + 0.5	Vdc
Voltage at TXI (Pin 9), RXI (Pin 21), FI (Pin 2)	−0.5, V_{CC} + 0.5	Vdc
Storage Temperature Range	−65 to +150	°C

Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
Supply Voltage (Pin 4) (See Text)	3.5	—	6.5	Vdc
CD Input (Pin 3), MUT Input (Pin 12)	0	—	V_{CC}	Vdc
I_{VB} Current (Pin 15)	—	—	500	μA
VLC (Pin 13)	0.3 x V_B	—	V_B	Vdc
Attenuator Input Signal Voltage (Pins 9, 21)	0	—	350	mVrms
Microphone Amplifier, Hybrid Amplifier Gain	0	—	40	dB
Load Current @ RXO, TXO (Pins 8, 22) @ MCO (Pin 10) @ HTO−, HTO+ (Pins 6, 5)	0 0 0	— — —	±2.0 ±1.0 ±5.0	mA
Ambient Operating Temperature Range	−20	—	+60	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted)

Parameter	Symbol	Min	Typ	Max	Units
POWER SUPPLY					
V_{CC} Supply Current (V_{CC} = 6.5 V, CD = 0.8 V) (V_{CC} = 6.5 V, CD = 2.0 V)	I_{CC}	— —	5.5 600	8.0 800	mA μA
CD Input Resistance (V_{CC} = V_{CD} = 6.5 V) CD Input Voltage — High — Low	R_{CD} V_{CDH} V_{CDL}	50 2.0 0	90 — —	— V_{CC} 0.8	kΩ Vdc Vdc
V_B Output Voltage (V_{CC} = 3.5 V) (V_{CC} = 5.0 V)	V_B	— 1.8	1.3 2.1	— 2.4	Vdc
V_B Output Resistance (I_{VB} = 1.0 mA)	R_{OVB}	—	400	—	Ω
V_B Power Supply Rejection Ratio (C_{VB} = 220 μF, f = 1.0 kHz)	PSRR	—	54	—	dB
ATTENUATORS (T_A = +25°C)					
Receive Attenuator Gain (f = 1.0 kHz, V_{LC} = V_B) Rx Mode, RXI = 150 mVrms (V_{CC} = 5.0 V) Rx Mode, RXI = 150 mVrms (V_{CC} = 3.5 V) Gain Change − V_{CC} = 3.5 V versus V_{CC} = 5.0 V AGC Gain Change − V_{CC} = 2.8 V versus V_{CC} = 5.0 V* Idle Mode, RXI = 150 mVrms Range (Rx to Tx Mode)	 G_{RX} G_{RX} ΔG_{RX1} ΔG_{RX2} G_{RXI} ΔG_{RX3}	 +4.0 +4.0 −0.5 — −22 49	 +6.0 +6.0 0 −25 −20 52	 +8.0 +8.0 +0.5 −15 −17 54	dB
Volume Control Range (Rx Mode, 0.3 V_B < V_{LC} < V_B)	V_{CR}	27	35	—	dB
RXO DC Voltage (Rx Mode)	V_{RXO}	—	V_B	—	Vdc
ΔRXO DC Voltage (Rx to Tx Mode)	ΔV_{RXO}	—	±10	±150	mV
RXO High Voltage (I_{out} = −1.0 mA RXI = V_B + 1.5 V)	V_{RXOH}	3.7	—	—	Vdc
RXO Low Voltage (I_{out} = +1.0 mA, RXI = V_B − 1.0, Output measured with respect to V_B)*	V_{RXOL}	—	−1.5	−1.0	Vdc
RXI Input Resistance (RXI < 350 mVrms)	R_{RXI}	7.0	10	14	kΩ

(continued)

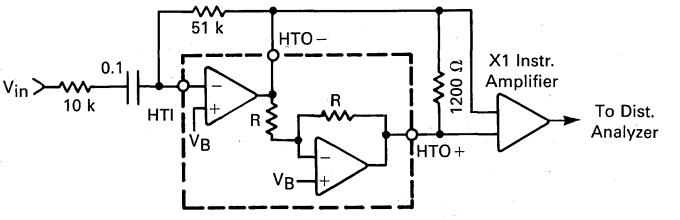
ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, CD ≤ 0.8 V, unless noted)

Parameter	Symbol	Min	Typ	Max	Units
ATTENUATORS — continued (T_A = +25°C)					
Transmit Attenuator Gain (f = 1.0 kHz) Tx Mode, TXI = 150 mVrms Idle Mode, TXI = 150 mVrms Range (Tx to Rx Mode)	 G_{TX} G_{TXI} ΔG_{TXI}	 +4.0 −22 49	 +6.0 −20 52	 +8.0 −17 54	dB
TXO DC Voltage (Tx Mode)	V_{TXO}	—	V_B	—	Vdc
ΔTXO DC Voltage (Tx to Rx Mode)	ΔV_{TXO}	—	±30	±150	mV
TXO High Voltage (I_{out} = −1.0 mA TXI = V_B + 1.5 V)	V_{TXOH}	3.7	—	—	Vdc
TXO Low Voltage (I_{out} = +1.0 mA, TXI = V_B − 1.0 V, Output measured with respect to V_B)*	V_{TXOL}	—	−1.5	−1.0	Vdc
TXI Input Resistance (TXI < 350 mVrms)	R_{TXI}	7.0	10	14	kΩ
Gain Tracking (G_{RX} + G_{TX}, @ Tx, Idle, Rx)*	G_{TR}	—	±0.1	—	dB
*See text for explanation.					
ATTENUATOR CONTROL (T_A = +25°C)					
C_T Voltage (Pin 14 − V_B) Rx Mode (V_{LC} = V_B) Idle Mode Tx Mode	V_{CT}	 — — —	 +240 0 −240	 — — —	mV
C_T Source Current (switching to Rx mode)	I_{CTR}	−85	−60	−40	μA
C_T Sink Current (switching to Tx mode)	I_{CTT}	+40	+60	+85	μA
C_T Slow Idle Current	I_{CTS}	—	0	—	μA
C_T Fast Idle Internal Resistance	R_{FI}	1.5	2.0	3.6	kΩ
V_{LC} Input Current	I_{VLC}	—	−60	—	nA
Dial Tone Detector Threshold	V_{DT}	10	15	20	mV
MICROPHONE AMPLIFIER (T_A = +25°C, V_{MUT} ≤ 0.8 V, A_{VCL} = 31 dB unless otherwise noted)					
Ouptut Offset (V_{MCO} − V_B, Feedback R = 180 kΩ)	MCO_{VOS}	−50	0	+50	mVdc
Open Loop Gain (f < 100 Hz)	A_{VOLM}	70	80	—	dB
Gain Bandwidth	GBW_M	—	1.0	—	MHz
Output High Voltage (I_{out} = −1.0 mA, V_{CC} = 5.0 V)	V_{MCOH}	3.7	—	—	Vdc
Output Low Voltage (I_{out} = +1.0 mA)	V_{MCOL}	—	—	200	mVdc
Input Bias Current (@ MCI)	I_{BM}	—	−40	—	nA
Muting (ΔGain) (f = 1.0 kHz, V_{MUT} = 2.0 V) (300 Hz < f < 10 kHz)	GMT	−55 —	— −68	— —	dB
MUT Input Resistance (V_{CC} = V_{MUT} = 6.5 V)	R_{MUT}	50	90	—	kΩ
MUT Input — High	V_{MUTH}	2.0	—	V_{CC}	Vdc
MUT Input — Low	V_{MUTL}	0	—	0.8	Vdc
Distortion (300 Hz < f < 10 kHz)	THD_M	—	0.15	—	%
HYBRID AMPLIFIERS (T_A = +25°C)					
HTO− Offset (V_{HTO-} − V_B, Feedback R = 51 kΩ)	H_{VOS}	−20	0	+20	mVdc
HTO− to HTO+ Offset (Feedback R = 51 kΩ)	HB_{VOS}	−30	0	+30	mVdc
Open Loop Gain (HTI to HTO−, f < 100 Hz)	A_{VOLH}	60	80	—	dB
Gain Bandwidth	GBW_H	—	1.0	—	MHz
Closed Loop Gain (HTO− to HTO+)	A_{VCLH}	−0.35	0	+0.35	dB
Input Bias Current (@HTI)	I_{BH}	—	−30	—	nA
HTO− High Voltage (I_{out} = −5.0 mA)	V_{HT-H}	3.7	—	—	Vdc
HTO− Low Voltage (I_{out} = +5.0 mA)	V_{HT-L}	—	—	250	mVdc
HTO+ High Voltage (I_{out} = −5.0 mA)	V_{HT+H}	3.7	—	—	Vdc
HTO+ Low Voltage (I_{out} = +5.0 mA)	V_{HT+L}	—	—	450	mVdc
Distortion (300 Hz < f < 10 kHz, See Figure 1)	THD_H	—	0.3	—	%

Parameter	Symbol	Min	Typ	Max	Units
LEVEL DETECTORS AND BACKGROUND NOISE MONITORS (T_A = +25°C)					
Transmit-Receive Switching Threshold (Ratio of Current at RLI1 + RLI2 to 20 μA at TLI1 + TLI2 to switch from Tx to Rx)	I_{TH}	0.8	1.0	1.2	
Source Current at RLO1, RLO2, TLO1, TLO2	I_{LSO}	—	−2.0	—	mA
Sink Current at RLO1, RLO2, TLO1, TLO2	I_{LSK}	—	4.0	—	μA
CPR, CPT Output Resistance (I_{out} = 1.5 mA)	R_{CP}	—	35	—	Ω
CPR, CPT Leakage Current	I_{CPLK}	—	−0.2	—	μA
FILTER (T_A = +25°C)					
Voltage Offset at FO (V_{FO} − V_B, 220 kΩ from V_B to FI)	FO_{VOS}	−200	−90	0	mV
FO Sink Current	I_{FO}	150	260	400	μA
FI Bias Current	I_{FI}	—	−50	—	nA
SYSTEM DISTORTION (T_A = +25°C, f = 1.0 kHz)					
Rx Mode (From FI to RXO, FO connected to RXI)	THD_R	—	0.5	3.0	%
Tx Mode (From MCI to HTO−/HTO+, includes Tx attenuator)	THD_T	—	0.8	3.0	%

1. All currents into a device pin are positive, those out of a pin are negative. Algebraic convention rather than magnitude is used to define limits.

FIGURE 1 — HYBRID AMPLIFIER DISTORTION TEST



TEMPERATURE CHARACTERISTICS

Parameter	Typical Value @ 25°C	Typical Change −20 to +60°C
V_{CC} Supply Current (CD = 0.8 V)	5.0 mA	−0.3 %/°C
V_{CC} Supply Current (CD = 2.0 V)	400 μA	−0.4 %/°C
V_B Output Voltage (V_{CC} = 5.0 V)	2.1 V	+0.8 %/°C
Attenuator Gain (Max Gain)	+6.0 dB	0.0008 dB/°C
Attenuator Gain (Max Attenuation)	−46 dB	0.004 dB/°C
Attenuator Input Resistance (@ TXI, RXI)	10 kΩ	+0.6 %/°C
Dial Tone Detector Threshold	15 mV	+20 μV/°C
CT Source, Sink Current	±60 μA	−0.15 %/°C
Microphone, Hybrid Amplifier Offset	0 mV	±4.0 μV/°C
Transmit-Receive Switching Threshold	1.0	±0.02 %/°C
Sink Current at RLO1, RLO2, TLO1, TLO2	4.0 μA	−10 nA/°C
Closed Loop Gain (HTO− to HTO+)	0 dB	0.001 %/°C

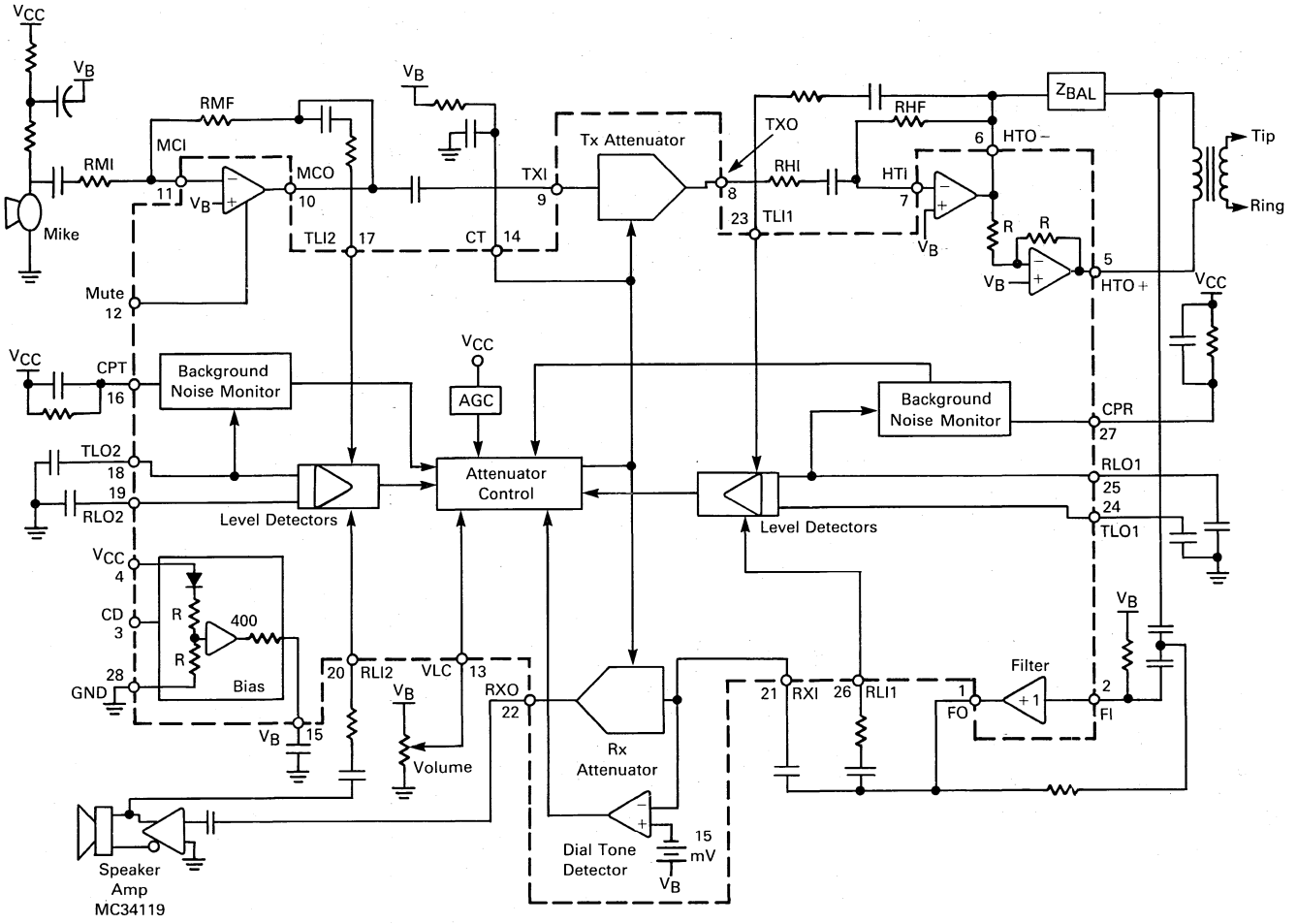
PIN DESCRIPTION

Pin	Name	Description
1	FO	Filter output. Output impedance is less than 50 ohms.
2	FI	Filter input. Input impedance is greater than 1.0 Mohm.
3	CD	Chip Disable. A logic low (<0.8 V) sets normal operation. A logic high (>2.0 V) disables the IC to conserve power. Input impedance is nominally 90 kΩ.
4	V_{CC}	A supply voltage of +2.8 to +6.5 volts is required, at ≈ 5.0 mA. As V_{CC} falls from 3.5 to 2.8 volts, an AGC circuit reduces the receive attenuator gain by ≈ 25 dB (when in the receive mode).
5	HTO+	Output of the second hybrid amplifier. The gain is internally set at −1.0 to provide a differential output, in conjunction with HTO−, to the hybrid transformer.
6	HTO−	Output of the first hybrid amplifier. The gain of the amp is set by external resistors.
7	HTI	Input and summing node for the first hybrid amplifier. DC level is ≈V_B.
8	TXO	Output of the transmit attenuator. DC level is approximately V_B.
9	TXI	Input to the transmit attenuator. Max. signal level is 350 mVrms. Input impedance is ≈10 kΩ.
10	MCO	Output of the microphone amplifier. The gain of the amplifier is set by external resistors.
11	MCI	Input and summing node of the microphone amplifier. DC level is ≈ V_B.
12	MUT	Mute input. A logic low (<0.8 V) sets normal operation. A logic high (>2.0 V) mutes the microphone amplifier without affecting the rest of the circuit. Input impedance is nominally 90 kΩ.

Pin	Name	Description
13	VLC	Volume control input. When VLC = V_B, the receive attenuator is at maximum gain when in the receive mode. When VLC = 0.3 V_B, the receive gain is down 35 dB. Does not affect the transmit mode.
14	C_T	An RC at this pin sets the response time for the circuit to switch modes.
15	V_B	An output voltage ≈V_{CC}/2. This voltage is a system ac ground, and biases the volume control. A filter cap is required.
16	CPT	An RC at this pin sets the time constant for the transmit background monitor.
17	TLI2	Input to the transmit level detector on the mike/speaker side.
18	TLO2	Output of the transmit level detector on the mike/speaker side, and input to the transmit background monitor.
19	RLO2	Output of the receive level detector on the mike/speaker side.
20	RLI2	Input to the receive level detector on the mike/speaker side.
21	RXI	Input to the receive attenuator and dial tone detector. Max input level is 350 mV RMS. Input impedance is ≈10 kΩ.
22	RXO	Output of the receive attenuator. DC level is approximately V_B.
23	TLI1	Input to the transmit level detector on the line side.
24	TLO1	Output of the transmit level detector on the line side.
25	RLO1	Output of the receive level detector on the line side, and input to the receive background monitor.
26	RLI1	Input to the receive level detector on the line side.
27	CPR	An RC at this pin sets the time constant for the receive background monitor.
28	GND	Ground pin for the entire IC.

Note: Pin numbers are identical for the DIP package and the SOIC package.

FIGURE 2 — MC34118 BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

INTRODUCTION

The fundamental difference between the operation of a speakerphone and a handset is that of half-duplex versus full-duplex. The handset is full duplex since conversation can occur in both directions (transmit and receive) simultaneously. A speakerphone has higher gain levels in both paths, and attempting to converse full duplex results in oscillatory problems due to the loop that exists within the system. The loop is formed by the receive and transmit paths, the hybrid, and the acoustic coupling (speaker to microphone). The only practical and economical solution used to date is to design the speakerphone to function in a half duplex mode — i.e., only one person speaks at a time, while the other listens. To achieve this requires a circuit which can detect who is talking, switch on the appropriate path (transmit or receive), and switch off (attenuate) the other path. In this way, the loop gain is maintained less than unity. When the talkers exchange function, the circuit must quickly detect this, and switch the circuit appropriately. By providing speech level detectors, the circuit operates in a "hands-free" mode, eliminating the need for a "push-to-talk" switch.

The handset, by the way, has the same loop as the speakerphone. But since the gains are considerably lower, and since the acoustic coupling from the earpiece to the mouthpiece is almost non-existent (the receiver is normally held against a person's ear), oscillations don't occur.

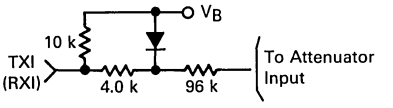
The MC34118 provides the necessary level detectors, attenuators, and switching control for a properly operating speakerphone. The detection sensitivity and timing are externally controllable. Additionally, the MC34118 provides background noise monitors which make the circuit insensitive to room and line noise, hybrid amplifiers for interfacing to Tip and Ring, the microphone amplifier, and other associated functions. Please refer to the Block Diagram (Figure 2) when reading the following sections.

ATTENUATORS

The transmit and receive attenuators are complementary in function, i.e., when one is at maximum gain (+6.0 dB), the other is at maximum attenuation (−46 dB), and vice versa. They are never both fully on or both fully off. The sum of their gains remains constant (within a nominal error band of ±0.1 dB) at a typical value of −40 dB (see Figure 10). Their purpose is to control the transmit and receive paths to provide the half-duplex operation required in a speakerphone.

The attenuators are non-inverting, and have a −3.0 dB (from max gain) frequency of ≈100 kHz. The input impedance of each attenuator (TXI and RXI) is nominally 10 kΩ (see Figure 3), and the input signal should be limited to 350 mVrms (990 mVp-p) to prevent distortion. That maximum recommended input signal is independent of the volume control setting. The diode clamp on the inputs limits the input swing, and therefore the maximum negative output swing. This is the reason for V_{RXOL} and V_{TXOL} specification being defined as they are in the Electrical Characteristics. The output impedance is <10 Ω until the output current limit (typically 2.5 mA) is reached.

FIGURE 3 — ATTENUATOR INPUT STAGE



The attenuators are controlled by the single output of the Control Block, which is measurable at the C_T pin (Pin 14). When the C_T pin is at +240 millivolts with respect to V_B, the circuit is in the receive mode (receive attenuator is at +6.0 dB). When the C_T pin is at −240 millivolts with respect to V_B, the circuit is in the transmit mode (transmit attenuator is at +6.0 dB). The circuit is in an idle mode when the C_T voltage is equal to V_B, causing the attenuators' gains to be halfway between their fully on and fully off positions (−20 dB each). Monitoring the C_T voltage (with respect to V_B) is the most direct method of monitoring the circuit's mode.

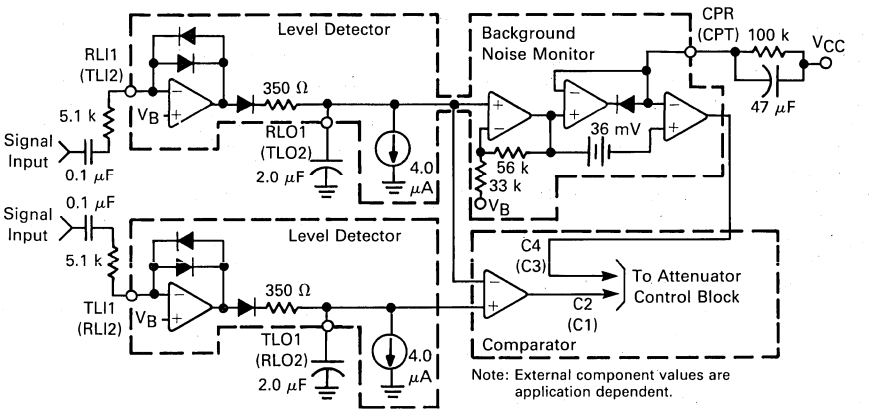
The inputs to the Control Block are seven: 2 from the comparators operated by the level detectors, 2 from the background noise monitors, the volume control, the dial-tone detector, and the AGC circuit. These seven inputs are described below.

LEVEL DETECTORS

There are four level detectors — two on the receive side and two on the transmit side. Refer to Figure 4 — the terms in parentheses form one system, and the other terms form the second system. Each level detector is a high gain amplifier with back-to-back diodes in the feedback path, resulting in non-linear gain, which permits operation over a wide dynamic range of speech levels. Refer to the graphs of Figures 11, 12 and 13 for their dc and ac transfer characteristics. The sensitivity of each level detector is determined by the external resistor and capacitor at each input (TLI1, TLI2, RLI1, and RLI2). Each output charges an external capacitor through a diode and limiting resistor, thus providing a dc representation of the input ac signal level. The outputs have a quick rise time (determined by the capacitor and an internal 350 Ω resistor), and a slow decay time set by an internal current source and the capacitor. The capacitors on the four outputs should have the same value (±10%) to prevent timing problems.

Referring to Figure 2, on the receive side, one level detector (RLI1) is at the receive input receiving the same

FIGURE 4 — LEVEL DETECTORS



signal as at Tip and Ring, and the other (RLI2) is at the output of the speaker amplifier. On the transmit side, one level detector (TLI2) is at the output of the microphone amplifier, while the other (TLI1) is at the hybrid output. Outputs RLO1 and TLO1 feed a comparator, the output of which goes to the Attenuator Control Block. Likewise, outputs RLO2 and TLO2 feed a second comparator which also goes to the Attenuator Control Block. The truth table for the effects of the level detectors on the Control Block is given in the section describing the Control Block.

BACKGROUND NOISE MONITORS

The purpose of the background noise monitors is to distinguish speech (which consists of bursts) from background noise (a relatively constant signal level). There are two background noise monitors — one for the receive path and one for the transmit path. Referring to Figure 4, the receive background noise monitor is operated on by the RLI1-RLO1 level detector, while the transmit background noise monitor is operated on by the TLI2-TLO2 level detector. They monitor the background noise by storing a dc voltage representative of the respective noise levels in capacitors at CPR and CPT. The voltages at these pins have slow rise times (determined by the external RC), but fast decay times. If the signal at RLI1 (or TLI2) changes slowly, the voltage at CPR (or CPT) will remain more positive than the voltage at the non-inverting input of the monitor's output comparator. When speech is present, the voltage on the non-inverting input of the comparator will rise quicker than the voltage at the inverting input (due to the burst characteristic of speech), causing its output to change. This output is sensed by the Attenuator Control Block.

The 36 mV offset at the comparator's input keeps the comparator from changing state unless the speech level exceeds the background noise by ≈4.0 dB. The time constant of the external RC (≈4.7 seconds) determines the response time to background noise variations.

VOLUME CONTROL

The volume control input at VLC (Pin 13) is sensed as a voltage with respect to V_B. The volume control affects the attenuators *only* in the receive mode. It has no effect in the idle or transmit modes.

When in the receive mode, the gain of the receive attenuator will be +6.0 dB, and the gain of the transmit attenuator will be −46 dB only when VLC is equal to V_B. As VLC is reduced below V_B, the gain of the receive attenuator is reduced (see Figure 14), and the gain of the transmit attenuator is increased such that their sum remains constant. Changing the voltage at VLC changes the voltage at C_T (see the Attenuator Control Block section), which in turn controls the attenuators.

The volume control setting does not affect the maximum attenuator input signal at which noticeable distortion occurs.

The bias current at VLC is typically 60 nA out of the pin, and does not vary significantly with the VLC voltage or with V_{CC}.

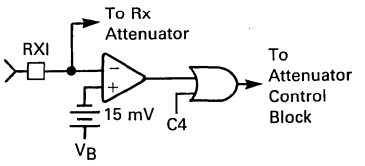
DIAL TONE DETECTOR

The dial tone detector is a comparator with one side connected to the receive input (RXI) and the other input connected to V_B with a 15 mV offset (see Figure 5). If the circuit is in the receive mode, and the incoming signal is greater than 15 mV (10 mVrms), the comparator's output will change, disabling the receive idle mode. The receive attenuator will then be at a setting determined solely by the volume control.

The purpose of this circuit is to prevent the dial tone

(which would be considered as continuous noise) from fading away as the circuit would have the tendency to switch to the idle mode. By disabling the receive idle mode, the dial tone remains at the normally expected full level.

FIGURE 5 — DIAL TONE DETECTOR



AGC

The AGC circuit affects the circuit only in the receive mode, and only when the supply voltage (V_{CC}) is less than 3.5 volts. As V_{CC} falls below 3.5 volts, the gain of the receive attenuator is reduced according to the graph of Figure 15. The transmit path attenuation changes such that the sum of the transmit and receive gains remains constant.

The purpose of this feature is to reduce the power (and current) used by the speaker when a line-powered speakerphone is connected to a long line, where the available power is limited. By reducing the speaker power, the voltage sag at V_{CC} is controlled, preventing possible erratic operation.

ATTENUATOR CONTROL BLOCK

The Attenuator Control Block has the seven inputs described above:

- The output of the comparator operated by RLO2 and TLO2 (microphone/speaker side) — designated C1.
- The output of the comparator operated by RLO1 and TLO1 (Tip/Ring side) — designated C2.
- The output of the transmit background noise monitor — designated C3.
- The output of the receive background noise monitor — designated C4.
- The volume control.
- The dial tone detector.
- The AGC circuit.

The single output of the Control Block controls the two attenuators. The effect of C1–C4 is as follows:

Inputs				Output
C1	C2	C3	C4	Mode
Tx	Tx	1	X	Transmit
Tx	Rx	y	y	Fast Idle
Rx	Tx	y	y	Fast Idle
Rx	Rx	X	1	Receive
Tx	Tx	0	X	Slow Idle
Tx	Rx	0	0	Slow Idle
Rx	Tx	0	0	Slow Idle
Rx	Rx	X	0	Slow Idle

X = Don't Care; y = C3 and C4 are not both 0.

A definition of the above terms:

1) "Transmit" means the transmit attenuator is fully on (+6.0 dB), and the receive attenuator is at max. attenuation (−46 dB).
2) "Receive" means both attenuators are controlled by the volume control. At max. volume, the receive attenuator is fully on (+6.0 dB), and the transmit attenuator is at max. attenuation (−46 dB).
3) "Fast Idle" means both transmit and receive speech are present in approximately equal levels. The attenuators are quickly switched (30 ms) to idle until one speech level dominates the other.
4) "Slow Idle" means speech has ceased in both transmit and receive paths. The attenuators are then slowly switched (1 second) to the idle mode.
5) Switching to the full transmit or receive modes from any other mode is at the fast rate (≈30 ms).

A summary of the truth table is as follows:

1) The circuit will switch to transmit if: a) *both* transmit level detectors sense higher signal levels relative to the respective receive level detectors (TLI1 versus RLI1, TLI2 versus RLI2), *and* b) the transmit background noise monitor indicates the presence of speech.

2) The circuit will switch to receive if: a) *both* receive level detectors sense higher signal levels relative to the respective transmit level detectors, *and* b) the receive background noise monitor indicates the presence of speech.

3) The circuit will switch to the fast idle mode if the level detectors *disagree* on the relative strengths of the signal levels, *and* at least one of the background noise monitors indicates speech. For example, referring to the Block Diagram (Figure 2), if there is sufficient signal at the microphone amp output (TLI2) to override the speaker signal (RLI2), *and* there is sufficient signal at the receive input (RLI1) to override the signal at the hybrid output (TLI1), *and* either or both background monitors indicate speech, then the circuit will be in the fast idle mode. Two conditions which can cause the fast idle mode to occur are a) when both talkers are attempting to gain control of the system by talking at the same time, and b) when one talker is in a very noisy environment, forcing the other talker to continually override that noise level. In general, the fast idle mode will occur infrequently.

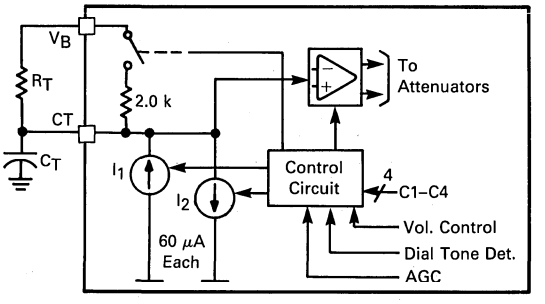
4) The circuit will switch to the slow idle mode when a) both talkers are quiet (no speech present), or b) when one talker's speech level is continuously overriden by noise at the other speaker's location.

The time required to switch the circuit between transmit, receive, fast idle and slow idle is determined in part by the components at the C_T pin (Pin 14). (See the section on Switching Times for a more complete explanation of the switching time components.) A schematic of the C_T circuitry is shown in Figure 6, and operates as follows:

- R_T is typically 120 kΩ, and C_T is typically 5.0 μF.
- To switch to the receive mode, I_1 is turned on (I_2 is off), charging the external capacitor to +240 mV above V_B. (An internal clamp prevents further charging of the capacitor.)
- To switch to the transmit mode, I_2 is turned on (I_1 is off) bringing down the voltage on the capacitor to −240 mV with respect to V_B.

— To switch to idle quickly (fast idle), the current sources are turned off, and the internal 2.0 kΩ resistor is switched in, discharging the capacitor to V_B with a time constant = 2.0 k x C_T.
— To switch to idle slowly (slow idle), the current sources are turned off, the switch at the 2.0 kΩ resistor is open, and the capacitor discharges to V_B through the external resistor R_T with a time constant = R_T x C_T.

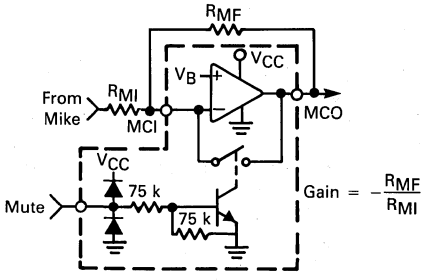
FIGURE 6 — CT ATTENUATOR CONTROL BLOCK CIRCUIT



MICROPHONE AMPLIFIER

The microphone amplifier (Pins 10, 11) has the noninverting input internally connected to V_B, while the inverting input and the output are pinned out. Unlike most op-amps, the amplifier has an all-NPN output stage, which maximizes phase margin and gain-bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain is typically 80 dB (f <100 Hz), and the gain-bandwidth is typically 1.0 MHz (See Figure 16). The maximum p-p output swing is typically 1.0 volt less than V_{CC} with an output impedance of <10 Ω until current limiting is reached (typically 1.5 mA). Input bias current at MCI is typically 40 nA out of the pin.

FIGURE 7 — MICROPHONE AMPLIFIER AND MUTE



The muting function (Pin 12), when activated, will reduce the gain of the amplifier to ≈ −39 dB (with RMI = 5.1 kΩ) by shorting the output to the inverting input (see Figure 7). The mute input has a threshold of ≈1.5 volts, and the voltage at this pin must be kept within the range of ground and V_{CC} (see Figure 17). If the mute function is not used, the pin should be grounded.

HYBRID AMPLIFIERS

The two hybrid amplifiers (at HTO +, HTO −, and HTI), in conjunction with an external transformer, provide the two-to-four wire converter for interfacing to the telephone line. The gain of the first amplifier (HTI to HTO −) is set by external resistors (gain = $-R_{HF}/R_{HI}$ in Figure 2), and its output drives the second amplifier, the gain of which is internally set at −1.0. Unlike most op-amps, the amplifiers have an all-NPN output stage, which maximizes phase margin and gain-bandwidth. This feature ensures stability at gains less than unity, as well as with a wide range of reactive loads. The open loop gain of the first amplifier is typically 80 dB, and the gain bandwidth of each amplifier is ≈1.0 MHz (see Figure 16). The maximum p-p output swing of each amplifier is typically 1.2 volts less than V_{CC} with an output impedance of <10 Ω until current limiting is reached (typically 8.0 mA). The output current capability is guaranteed to be a minimum of 5.0 mA. The bias current at HTI is typically 30 nA out of the pin.

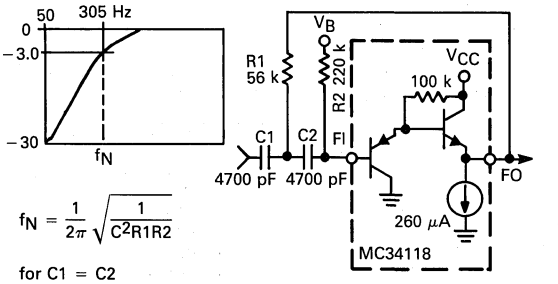
The connections to the coupling transformer are shown in the Block Diagram (Figure 2). The block labeled ZBal is the balancing network necessary to match the line impedance.

FILTER

The operation of the filter circuit is determined by the external components. The circuit within the MC34118, from pins FI to FO is a buffer with a high input impedance (>1.0 MΩ), and a low output impedance (<50 Ω). The configuration of the external components determines whether the circuit is a high-pass filter (as shown in Figure 2), a low-pass filter, or a band-pass filter.

As a high pass filter, with the components shown in Figure 8, the filter will keep out 60 Hz (and 120 Hz) hum which can be picked up by the external telephone lines.

FIGURE 8 — HIGH PASS FILTER



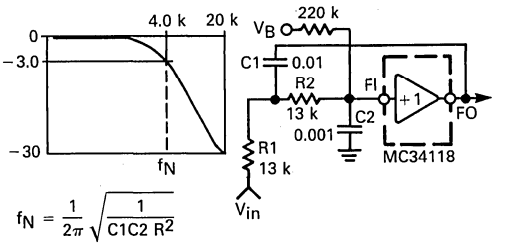
$$f_N = \frac{1}{2\pi}\sqrt{\frac{1}{C^2R1R2}}$$

for C1 = C2

As a low pass filter (Figure 9), it can be used to roll off the high end frequencies in the receive circuit, which aids in protecting against acoustic feedback problems.

With an appropriate choice of an input coupling capacitor to the low pass filter, a band pass filter is formed.

FIGURE 9 — LOW PASS FILTER



$$f_N = \frac{1}{2\pi}\sqrt{\frac{1}{C1C2\,R^2}}$$

for R1 = R2

POWER SUPPLY, V_B, AND CHIP DISABLE

The power supply voltage at V_{CC} (Pin 4) is to be between 3.5 and 6.5 volts for normal operation, with reduced operation possible down to 2.8 volts (see Figure 15 and the AGC section). The power supply current is shown in Figure 18 for both the power-up and power-down mode.

The output voltage at V_B (Pin 15) is $\approx(V_{CC} - 0.7)/2$, and provides the ac ground for the system. The output impedance at V_B is $\approx$400 Ω (see Figure 19), and in conjunction with the external capacitor at V_B, forms a low pass filter for power supply rejection. Figure 20 indicates the amount of rejection with different capacitors. The choice of capacitor is application dependent based on whether the circuit is powered by the telephone line or a power supply.

Since V_B biases the microphone and hybrid amplifiers, the amount of supply rejection at their outputs is directly related to the rejection at V_B, as well as their respective gains. Figure 21 depicts this graphically.

The Chip Disable (Pin 3) permits powering down the IC to conserve power and/or for muting purposes. With CD $\leq$0.8 volts, normal operation is in effect. With CD $\geq$2.0 volts and $\leq V_{CC}$, the IC is powered down. In the powered down mode, the microphone and the hybrid amplifiers are disabled, and their outputs go to a high impedance state. Additionally, the bias is removed from the level detectors. The bias is not removed from the filter (Pins 1, 2), the attenuators (Pins 8, 9, 21, 22), or from Pins 13, 14, and 15 (the attenuators are disabled, however, and will not pass a signal). The input impedance at CD is typically 90 kΩ, has a threshold of $\approx$1.5 volts, and the voltage at this pin must be kept within the range of ground and V_{CC} (see Figure 17). If CD is not used, the pin should be grounded.

FIGURE 10 — ATTENUATOR GAIN versus V_{CT} (PIN 14)

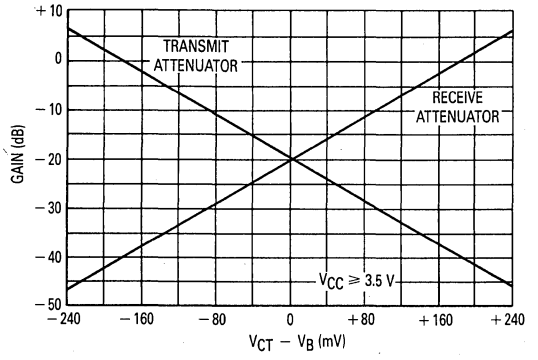


FIGURE 11 — LEVEL DETECTOR DC TRANSFER CHARACTERISTICS

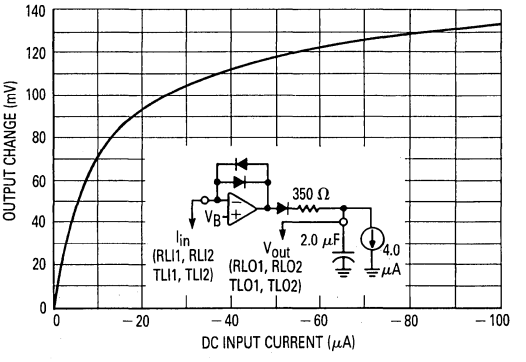


FIGURE 12 — LEVEL DETECTOR AC TRANSFER CHARACTERISTICS

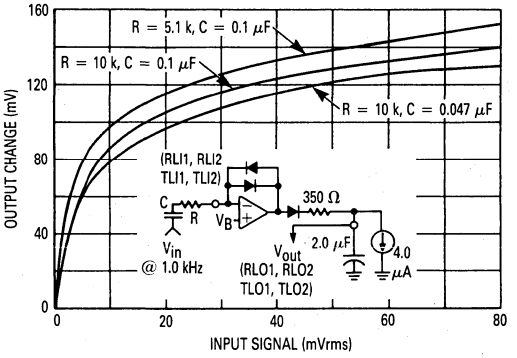


FIGURE 13 — LEVEL DETECTOR AC TRANSFER CHARACTERISTICS versus FREQUENCY

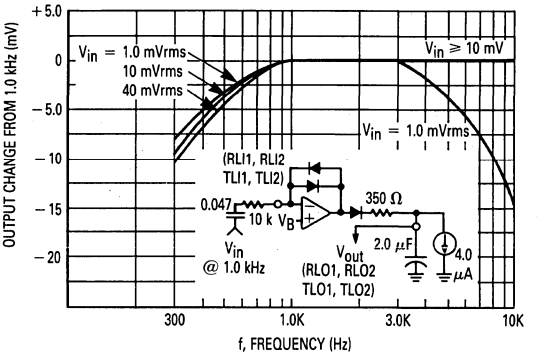


FIGURE 14 — RECEIVE ATTENUATOR versus VOLUME CONTROL

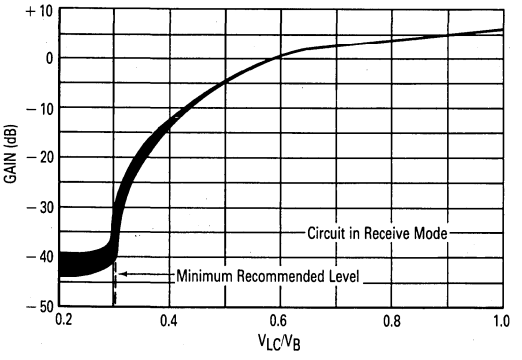


FIGURE 15 — RECEIVE ATTENUATION GAIN versus V_{CC}

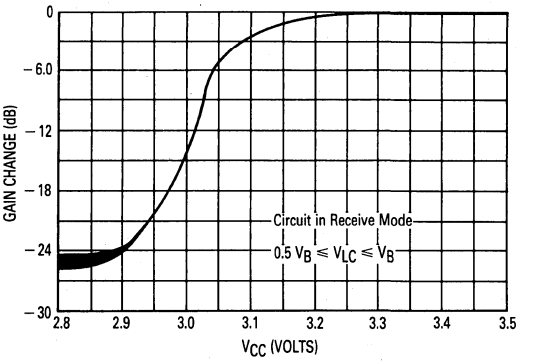


FIGURE 16 — MICROPHONE AMPLIFIER AND 1ST HYBRID AMPLIFIER OPEN LOOP GAIN AND PHASE

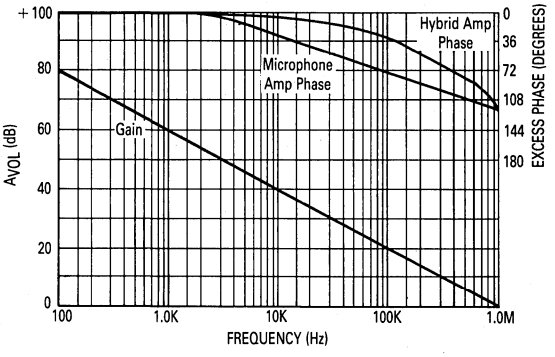


FIGURE 17 — INPUT CHARACTERISTICS @ CD, MUT

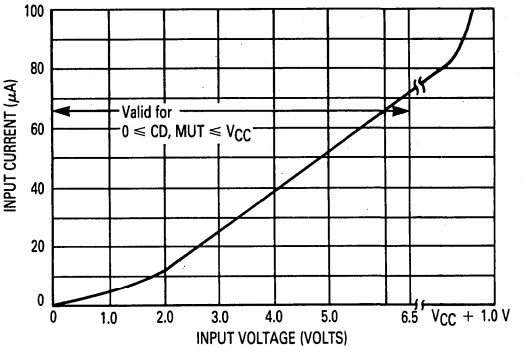


FIGURE 18 — SUPPLY CURRENT versus SUPPLY VOLTAGE

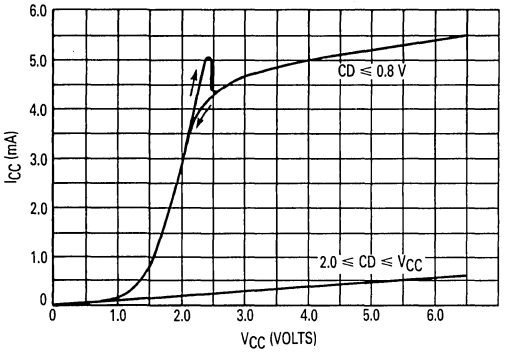


FIGURE 19 — V_B OUTPUT CHARACTERISTICS

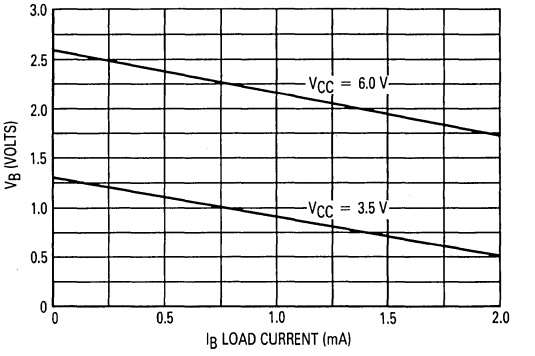


FIGURE 20 — V_B POWER SUPPLY REJECTION versus FREQUENCY AND V_B CAPACITOR

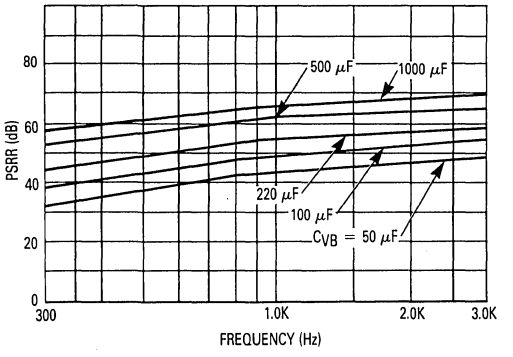


FIGURE 21 — POWER SUPPLY REJECTION OF THE MICROPHONE AND HYBRID AMPLIFIERS

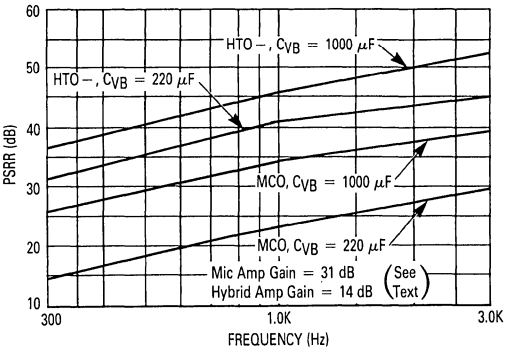
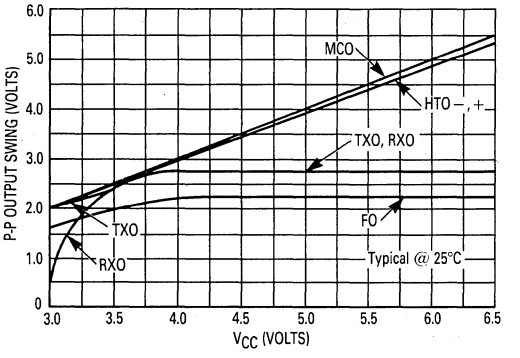


FIGURE 22 — TYPICAL OUTPUT SWING versus V_{CC}



DESIGN GUIDELINES

SWITCHING TIME

The switching time of the MC34118 circuit is dominated by the components at C_T (Pin 14, refer to Figure 6), and secondarily by the capacitors at the level detector outputs (RLO1, RLO2, TLO1, TLO2).

The time to switch to receive or to transmit from idle is determined by the capacitor at C_T, together with the internal current sources (refer to Figure 6). The switching time is:

$$\Delta T = \frac{\Delta V \times C_T}{I}$$

For the typical case where ΔV = 240 mV, I = 60 μA, and C_T is 5.0 μF, ΔT = 20 ms. If the circuit switches directly from receive to transmit (or vice-versa), the total switching time would be 40 ms.

The switching time from either receive or transmit to idle depends on which type of idle mode is in effect. If the circuit is going to "fast idle," the time constant is determined by the C_T capacitor, and the internal 2.0 kΩ resistor (Figure 6). With C_T = 5.0 μF, the time constant is ≈10 ms, giving a switching time to idle of ≈30 ms (for 95% change). Fast idle is an infrequent occurrence, however, occurring when both speakers are talking and competing for control of the circuit. The switching time from idle back to either transmit or receive is described above.

If the circuit is switching to "slow idle," the time constant is determined by the C_T capacitor and R_T, the external resistor (see Figure 6). With C_T = 5.0 μF, and R_T = 120 kΩ, the time constant is ≈600 ms, giving a switching time of ≈1.8 seconds (for 95% change). The switching period to slow idle begins when both speakers have stopped talking. The switching time back to the original mode will depend on how soon that speaker begins speaking again. The sooner the speaking starts during the 1.8 second period, the quicker the switching time since a smaller voltage excursion is required. That switching time is determined by the internal current sources as described above.

The above switching times occur, however, after the level detectors have detected the appropriate signal levels, since their outputs operate the Attenuator Control Block. Referring to Figure 4, the rise time of the level detectors' outputs to new speech is quick by comparison (≈1.0 ms), determined by the internal 350 Ω resistor and the external capacitor (typically 2.0 μF). The output's decay time is determined by the external capacitor, and an internal 4.0 μA current source giving a decay rate of ≈60 ms for a 120 mV excursion at RLO or TLO. However, the overall response time of the circuit is not a constant since it depends on the relative strength of the signals at the different level detectors, as well as the timing of the signals with respect to each other. The capacitors at the four outputs (RLO1, RLO2, TLO1, TLO2) must be equal value (±10%) to prevent problems in timing and level response.

The rise time of the level detector's outputs is not significant since it is so short. The decay time, however, provides a significant part of the "hold time" necessary to hold the circuit during the normal pauses in speech.

The components at the inputs of the level detectors (RLI1, RLI2, TLI1, TLI2) do not affect the switching time, but rather affect the relative signal levels required to switch the circuit, as well as the frequency response of the detectors.

DESIGN EQUATIONS

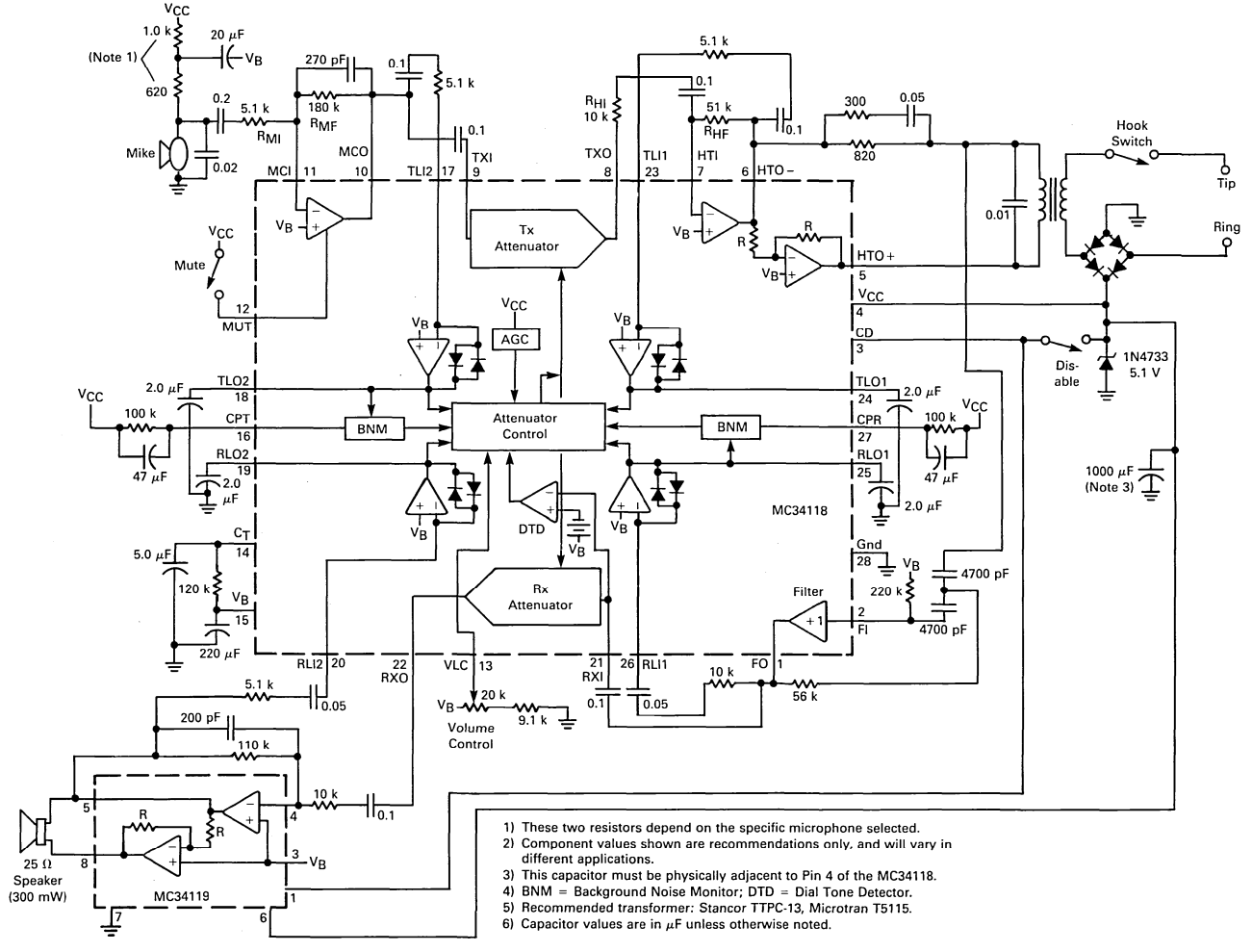
Referring to Figure 24 (the coupling capacitors have been omitted for simplicity), and the circuit of Figure 23, the following definitions will be used (all measurements are at 1.0 kHz):

- G_{MA} is the gain of the microphone amplifier measured from the microphone output to TXI (typically 35 V/V, or 31 dB);
- G_{TX} is the gain of the transmit attenuator, measured from TXI to TXO;
- G_{HA} is the gain of hybrid amplifiers, measured from TXO to the HTO−/HTO+ differential output (typically 10.2 V/V, or 20.1 dB);
- G_{HT} is the gain from HTO−/HTO+ to Tip/Ring for transmit signals, and includes the balance network (measured at 0.4 V/V, or −8.0 dB);
- G_{ST} is the sidetone gain, measured from HTO−/HTO+ to the filter input (measured at 0.18 V/V, or −15 dB);
- G_{HR} is the gain from Tip/Ring to the filter input for receive signals (measured at 0.833 V/V or −1.6 dB);
- G_{FO} is the gain of the filter stage, measured from the input of the filter to RXI, typically 0 dB at 1.0 kHz;
- G_{RX} is the gain of the receive attenuator measured from RXI to RXO;
- G_{SA} is the gain of the speaker amplifier, measured from RXO to the differential output of the MC34119 (typically 22 V/V or 26.8 dB);
- G_{AC} is the acoustic coupling, measured from the speaker differential voltage to the microphone output voltage.

I) Transmit Gain

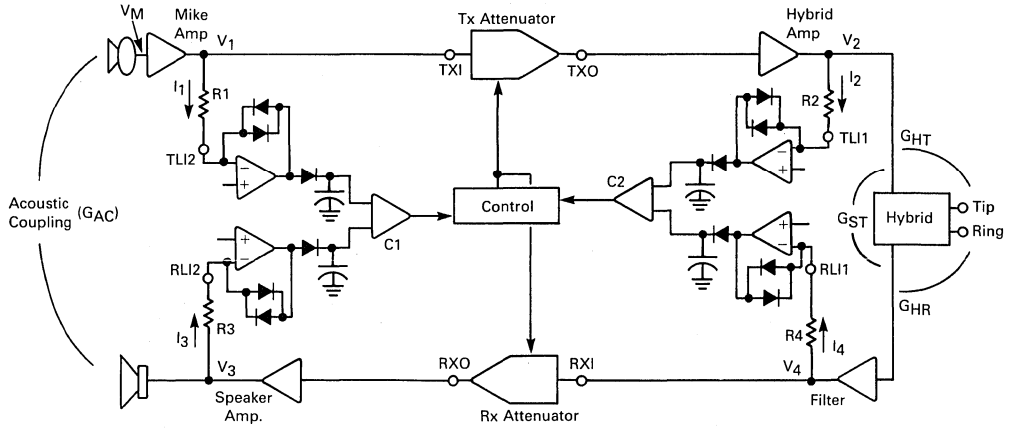
The transmit gain, from the microphone output (V_M) to Tip and Ring, is determined by the output characteristics of the microphone, and the desired transmit level. For example, a typical electret microphone will produce ≈0.35 mVrms under normal speech conditions. To achieve 100 mVrms at Tip/Ring, an overall gain of 285 V/V is necessary. The gain of the transmit attenuator is fixed at 2.0 (+6.0 dB), and the gain through the hybrid of Figure 23 (G_{HT}) is nominally 0.4 (−8.0 dB). Therefore a gain of 357 V/V is required of the microphone and hybrid amplifiers. It is desirable to have the majority of that gain in the microphone amplifier for three reasons: 1) the low level signals from the microphone should be amplified as soon as possible to minimize signal/noise

FIGURE 23 — MC34118 APPLICATION CIRCUIT (BASIC LINE POWERED SPEAKERPHONE)



1) These two resistors depend on the specific microphone selected.
2) Component values shown are recommendations only, and will vary in different applications.
3) This capacitor must be physically adjacent to Pin 4 of the MC34118.
4) BNM = Background Noise Monitor; DTD = Dial Tone Detector.
5) Recommended transformer: Stancor TTPC-13, Microtran T5115.
6) Capacitor values are in μF unless otherwise noted.

FIGURE 24 — BASIC BLOCK DIAGRAM FOR DESIGN PURPOSES



problems; 2) to provide a reasonable signal level to the TLI2 level detector; and 3) to minimize any gain applied to broadband noise generated within the attenuator. However, to cover the normal voiceband, the microphone amplifier's gain should not exceed 48 dB (see Figure 16). For the circuit of Figure 23, the gain of the microphone amplifier was set at 35 V/V (31 dB), and the differential gain of the hybrid amplifiers was set at 10.2 V/V (20.1 dB).

II) Receive Gain

The overall receive gain depends on the incoming signal level, and the desired output power at the speaker. Nominal receive levels (independent of the peaks) at Tip/Ring can be 35 mVrms (−27 dBm), although on long lines that level can be down to 8.0 mVrms (−40 dBm). The speaker power is:

$$P_{SPK} = \frac{10^{dBm/10} \times 0.6}{R_S} \qquad \text{(Equation 1)}$$

where R_S is the speaker impedance, and the dBm term is the incoming signal level increased by the gain of the receive path. Experience has shown that ≈30 dB gain is a satisfactory amount for the majority of applications. Using the above numbers and Equation 1, it would appear that the resulting power to the speaker is extremely low. However, Equation 1 does not consider the peaks in normal speech, which can be 10 to 15 times the rms value. Considering the peaks, the overall average power approaches 20–30 mW on long lines, and much more on short lines.

Referring to Figure 23, the gain from Tip/Ring to the filter input was measured at 0.833 V/V (−1.6 dB), the filter's gain is unity, and the receive attenuator's gain is 2.0 V/V (+6.0 dB) at maximum volume. The speaker amplifier's gain is set at 22 V/V (26.8 dB), which puts the overall gain at ≈31.2 dB.

III) Loop Gain

The total loop gain (of Figure 24) must add up to less than zero dB to obtain a stable circuit. This can be expressed as:

$$G_{MA} + G_{TX} + G_{HA} + G_{ST} + G_{FO} + G_{RX} + G_{SA} + G_{AC} < 0 \qquad \text{(Equation 2)}$$

Using the typical numbers mentioned above, and knowing that $G_{TX} + G_{RX} = -40$ dB, the required acoustic coupling can be determined:

$$G_{AC} < -[31 + 20.1 + (-15) + 0 + (-40) + 26.8] = -22.9 \text{ dB.} \qquad \text{(Equation 3)}$$

An acoustic loss of at least 23 dB is necessary to prevent instability and oscillations, commonly referred to as "singing." However, the following equations show that greater acoustic loss is necessary to obtain proper level detection and switching.

IV) Switching Thresholds

To switch comparator C1, currents I_1 and I_3 need to be determined. Referring to Figure 24, with a receive signal V_L applied to Tip/Ring, a current I_3 will flow through R3 into RLI2 according to the following equation:

$$I_3 = \frac{V_L}{R3}\left[G_{HR} \times G_{FO} \times G_{RX} \times \frac{G_{SA}}{2}\right] \qquad \text{(Equation 4)}$$

where the terms in the brackets are the V/V gain terms. The speaker amplifier gain is divided by two since G_{SA} is the differential gain of the amplifier, and V_3 is obtained from one side of that output. The current I_1, coming from the microphone circuit, is defined by:

$$I_1 = \frac{V_M \times G_{MA}}{R1} \qquad \text{(Equation 5)}$$

where V_M is the microphone voltage. Since the switching threshold occurs when $I_1 = I_3$, combining the above two equations yields:

$$V_M = V_L \times \frac{R1}{R3} \frac{[G_{HR} \times G_{FO} \times G_{RX} \times G_{SA}]}{G_{MA} \times 2} \qquad \text{(Equation 6)}$$

This is the general equation defining the microphone voltage necessary to switch comparator C1 when a receive signal V_L is present. The highest V_M occurs when the receive attenuator is at maximum gain (+6.0 dB). Using the typical numbers for Equation 6 yields:

$$V_M = 0.52\ V_L \qquad \text{(Equation 7)}$$

To switch comparator C2, currents I_2 and I_4 need to be determined. With sound applied to the microphone, a voltage V_M is created by the microphone, resulting in a current I_2 into TLI1:

$$I_2 = \frac{V_M}{R2}\left[G_{MA} \times G_{TX} \times \frac{G_{HA}}{2}\right] \qquad \text{(Equation 8)}$$

Since G_{HA} is the differential gain of the hybrid amplifiers, it is divided by two to obtain the voltage V_2 applied to R2. Comparator C2 switches when $I_4 = I_2$. I_4 is defined by:

$$I_4 = \frac{V_L}{R4}[G_{HR} \times G_{FO}] \qquad \text{(Equation 9)}$$

Setting $I_4 = I_2$, and combining the above equations results in:

$$V_L = V_M \times \frac{R4}{R2} \times \frac{[G_{MA} \times G_{TX} \times G_{HA}]}{[G_{HR} \times G_{FO} \times 2]} \qquad \text{(Equation 10)}$$

This equation defines the line voltage at Tip/Ring necessary to switch comparator C2 in the presence of a microphone voltage. The highest V_L occurs when the circuit is in the transmit mode (G_{TX} = +6.0 dB). Using the typical numbers for Equation 10 yields:

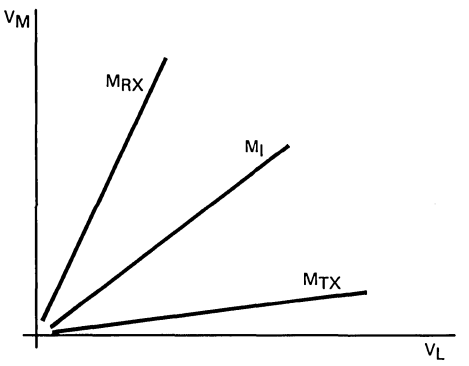
$$V_L = 840\ V_M \quad (\text{or } V_M = 0.0019\ V_L) \qquad \text{(Equation 11)}$$

At idle, where the gain of the two attenuators is −20 dB (0.1 V/V), Equations 6 and 10 yield the same result:

$$V_M = 0.024\ V_L \qquad \text{(Equation 12)}$$

Equations 7, 11, and 12 define the thresholds for switching, and are represented in the following graph:

FIGURE 25 — SWITCHING THRESHOLDS



The "M" terms are the slopes of the lines (0.52, 0.024, and 0.0019) which are the coefficients of the three equations. The M_{RX} line represents the receive to transmit threshold in that it defines the microphone signal level necessary to switch to transmit in the presence of a given receive signal level. The M_{TX} line represents the transmit to receive threshold. The M_I line represents the idle condition, and defines the threshold level on one side (transmit or receive) necessary to overcome noise on the other.

Some comments on the above graph:

— Acoustic coupling and sidetone coupling were not included in Equations 7 and 12. Those couplings will affect the actual performance of the final speakerphone due to their interaction with speech at the microphone, and the receive signal coming in at Tip/Ring. The effects of those couplings are difficult to predict due to their associated phase shifts and frequency response. In some cases the coupling signal will add, and other times subtract from the incoming signal. The physical design of the speakerphone enclosure, as well as the specific phone line to which it is connected, will affect the acoustic and sidetone couplings, respectively.

— The M_{RX} line helps define the maximum acoustic coupling allowed in a system, which can be found from the following equation:

$$G_{AC\text{-}MAX} = \frac{R1}{2 \times R3 \times G_{MA}} \qquad \text{(Equation 13)}$$

Equation 13 is independent of the volume control setting. Conversely, the acoustic coupling of a designed system helps determine the minimum slope of that line. Using the component values of Figure 23 in Equation

13 yields a $G_{AC\text{-}MAX}$ of −37 dB. Experience has shown, however, that an acoustic coupling loss of >40 dB is desirable.

— The M_{TX} line helps define the maximum sidetone coupling (G_{ST}) allowed in the system, which can be found from the following equation:

$$G_{ST} = \frac{R4}{2 \times R2 \times G_{FO}} \qquad \text{(Equation 14)}$$

Using the component values of Figure 23 in Equation 14 yields a maximum sidetone of 0 dB. Experience has shown, however, that a minimum of 6.0 dB loss is preferable.

The above equations can be used to determine the resistor values for the level detector inputs. Equation 6 can be used to determine the R1/R3 ratio, and Equation 10 can be used to determine the R4/R2 ratio. In Figure 24, R1–R4 each represent the combined impedance of the resistor and coupling capacitor at each level detector input. The magnitude of each RC's impedance should be kept within the range of 2.0 k–15 kΩ in the voiceband (due to the typical signal levels present) to obtain the best performance from the level detectors. The specific R and C at each location will determine the frequency response of that level detector.

APPLICATION INFORMATION

DIAL TONE DETECTOR

The threshold for the dial tone detector is internally set at 15 mV (10 mVrms) below V_B (see Figure 5). That threshold can be reduced by connecting a resistor from RXI to ground. The resistor value is calculated from:

$$R = 10\text{ k}\left[\frac{V_B}{\Delta V} - 1\right]$$

where V_B is the voltage at Pin 15, and ΔV is the amount of threshold reduction. By connecting a resistor from V_{CC} to RXI, the threshold can be increased. The resistor value is calculated from:

$$R = 10\text{ k}\left[\frac{V_{CC} - V_B}{\Delta V} - 1\right]$$

where ΔV is the amount of the threshold increase.

BACKGROUND NOISE MONITORS

For testing or circuit analysis purposes, the transmit or receive attenuators can be set to the "on" position, by disabling the background noise monitors, and applying a signal so as to activate the level detectors. Grounding the CPR pin will disable the receive background noise monitor, thereby indicating the "presence of speech" to the attenuator control block. Grounding CPT does the same for the transmit path.

Additionally, the receive background noise monitor is automatically disabled by the dial tone detector whenever the receive signal exceeds the detector's threshold.

TRANSMIT/RECEIVE DETECTION PRIORITY

Although the MC34118 was designed to have an idle mode such that the attenuators are halfway between their full on and full off positions, the idle mode can be biased towards the transmit or the receive side. With this done, gaining control of the circuit from idle will be easier for that side towards which it is biased since that path will have less attenuation at idle.

By connecting a resistor from C_T (Pin 14) to ground, the circuit will be biased towards the transmit side. The resistor value is calculated from:

$$R = R_T\left[\frac{V_B}{\Delta V} - 1\right]$$

where R is the added resistor, R_T is the resistor normally between Pins 14 and 15 (typically 120 kΩ), and ΔV is the difference between V_B and the voltage at C_T at idle (refer to Figure 10).

By connecting a resistor from C_T (Pin 14) to V_{CC}, the circuit will be biased towards the receive side. The resistor value is calculated from:

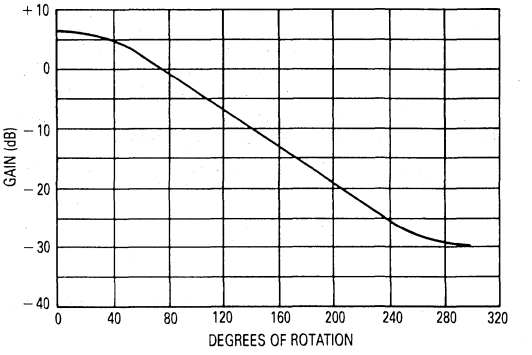
$$R = R_T\left[\frac{V_{CC} - V_B}{\Delta V} - 1\right]$$

R, R_T, and ΔV are the same as above. Switching time will be somewhat affected in each case due to the different voltage excursions required to get to transmit and receive from idle. For practical considerations, the ΔV shift should not exceed 100 mV.

VOLUME CONTROL

If a potentiometer with a standard linear taper is used for the volume control, the graph of Figure 14 indicates that the receive gain will not vary in a linear manner with respect to the pot's position. In situations where this may be objectionable, a potentiometer with an audio taper (commonly used in radio volume controls) will provide a more linear relationship as indicated in Figure 26. The slight non-linearity at each end of the graph is due to the physical construction of the potentiometer, and will vary among different manufacturers.

FIGURE 26 — RECEIVE ATTENUATOR GAIN versus POTENTIOMETER POSITION USING AUDIO TAPER



APPLICATION CIRCUIT

The circuit of Figure 23 is a basic speakerphone, to be used in parallel with any other telephone which con-

tains the ringer, dialer, and handset functions. The circuit is powered entirely by the telephone line's loop current, and its characteristics are shown in Figures 27–30.

FIGURE 27 — DC V-I CHARACTERISTICS

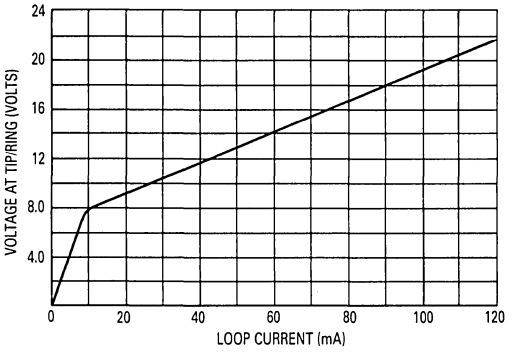


FIGURE 28 — AC TERMINATION IMPEDANCE

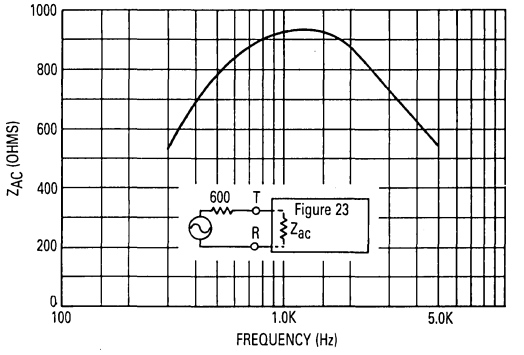


FIGURE 29 — TRANSMIT GAIN — MICROPHONE TO TIP/RING

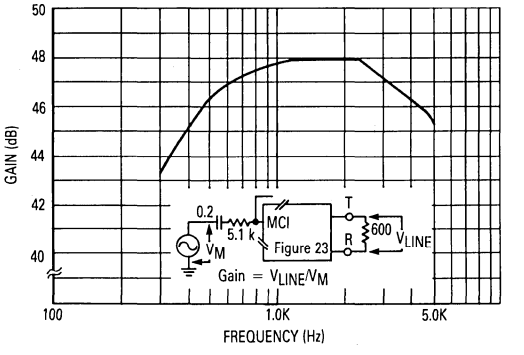


FIGURE 30 — RECEIVE GAIN

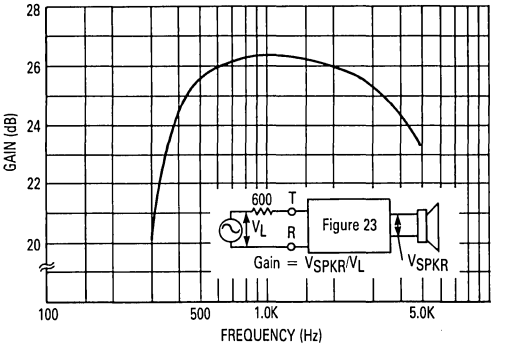
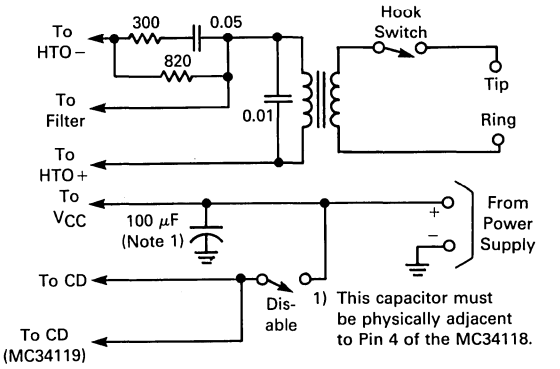


Figure 31 shows how the same circuit can be configured to be powered from a 3.5–6.0 volt power supply rather than the phone line.

FIGURE 31 — OPERATING FROM A POWER SUPPLY



ADDING A DIALER

Figure 32 shows the addition of a dialer to the circuit of Figure 23, with the additional components shown in bold. The MC145412 pulse/tone dialer is shown configured for DTMF operation. The DTMF output (Pin 18) is fed to the hybrid amplifiers at HTI, and the DTMF levels at Tip/Ring are adjusted by varying the 39 kΩ resistor. The Mute Output (active low at Pin 11) mutes the microphone amplifier, and attenuates the DTMF signals in the receive path (by means of the 10 k/3.0 k divider). The MC34118 is forced into the fast idle mode during dialing. The 3.0 volt battery provides for memory retention of the dialer's 10 number storage when the circuit is unpowered.

RFI INTERFERENCE

Potential radio frequency interference problems should be addressed early in the electrical and mechanical design of the speakerphone. RFI may enter the cir-

cuit through Tip and Ring, through the microphone wiring to the microphone amplifier, or through any of the PC board traces. The most sensitive pins on the MC34118 are the inputs to the level detectors (RLI1, RLI2, TLI1, TLI2) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. The board traces to these pins should be kept short, and the resistor and capacitor for each of these pins should be physically close to the pins. Any other high impedance input pin (MCI, HTI, FI, VLC) should be considered sensitive to RFI signals.

IN THE FINAL ANALYSIS . . .

Proper operation of a speakerphone is a combination of proper mechanical (acoustic) design as well as proper electronic design. The acoustics of the enclosure must be considered early in the design of a speakerphone. In general, electronics cannot compensate for poor acoustics, low speaker quality, or any combination of the two. Proper acoustic separation of the speaker and microphone, as described in the Design Equations, is essential. The physical location of the microphone, along with the characteristics of the selected microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

In the final analysis, the circuits shown in this data sheet will have to be "fine tuned" to match the acoustics of the enclosure, the specific hybrid, and the specific microphone and speaker selected. The component values shown in this data sheet should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at the microphone and speaker amplifiers, respectively. The switching response can then be fine tuned by varying (in small steps) the components at the level detector inputs until satisfactory operation is obtained for both long and short lines.

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, IL 60106
312-595-1022
Model EM-60

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

Hosiden America Corp.
Elk Grove Village, IL 60007
312-981-1144
Model KUC2123

25 Ω Speakers

Panasonic Industrial Co.
Seacaucus, N.J. 07094
201-348-5233
Model EAS-45P19S

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
516-561-6050
Various models — ask for catalog and Application Bulletin F232

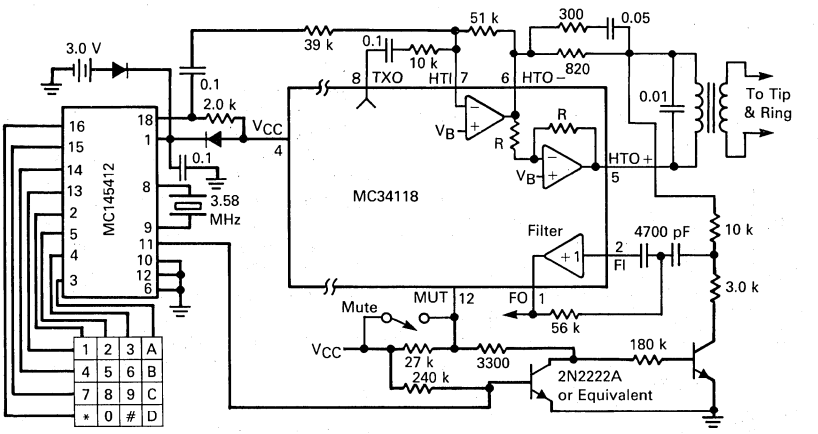
Stancor Products
Logansport, IN 46947
219-722-2244
Various models — ask for catalog

PREM Magnetics, Inc.
McHenry, IL 60050
815-385-2700
Various models — ask for catalog

Onan Power/Electronics
Minneapolis, MN 55437
612-921-5600
Model TC 38-6

Motorola Inc. does not endorse or warrant the suppliers referenced.

FIGURE 32 — ADDING A DIALER TO THE SPEAKERPHONE



MC34119

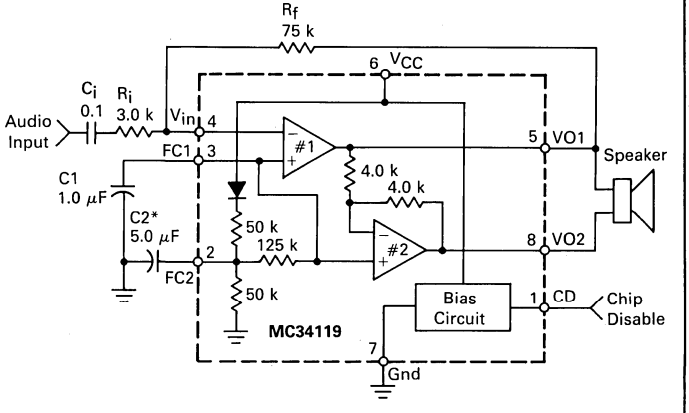
Specifications and Applications Information

LOW POWER AUDIO AMPLIFIER

The MC34119 is a low power audio amplifier integrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 volts minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80 dB, and the closed loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal. The MC34119 is available in a standard 8-pin DIP or a surface mount package.

- Wide Operating Supply Voltage Range (2–16 volts) — Allows Telephone Line Powered Applications
- Low Quiescent Supply Current (2.7 mA Typical) for Battery Powered Applications
- Chip Disable Input to Power Down the IC
- Low Power-Down Quiescent Current (65 μA Typical)
- Drives a Wide Range of Speaker Loads (8 Ohms and Up)
- Output Power Exceeds 250 mW with 32 Ohm Speaker
- Low Total Harmonic Distortion (0.5% Typical)
- Gain Adjustable from <0 dB to >46 dB for Voice Band
- Requires Few External Components

BLOCK DIAGRAM AND TYPICAL APPLICATION CIRCUIT

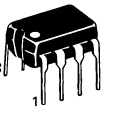


* = Optional

Differential Gain = $2 \times \frac{R_f}{R_i}$

LOW POWER AUDIO AMPLIFIER

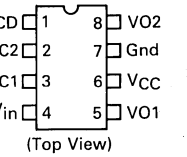
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
SO-8

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34119P	−20°C to +70°C	Plastic DIP
MC34119D		Plastic SOIC

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltage	−1.0 to +18	Vdc
Maximum Output Current at VO1, VO2	±250	mA
Maximum Voltage @ V_{in}, FC1, FC2, CD	−1.0, V_{CC}+1.0	Vdc
Applied Output Voltage to VO1, VO2 when disabled	−1.0, V_{CC}+1.0	Vdc
Junction Temperature	−55, +140	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	+2.0	—	+16	Vdc
Load Impedance	R_L	8.0	—	100	Ω
Peak Load Current	I_L	—	—	±200	mA
Differential Gain (5.0 kHz bandwidth)	AVD	0	—	46	dB
Voltage @ CD (Pin 1)	VCD	0	—	V_{CC}	Vdc
Ambient Temperature	T_A	−20	—	+70	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristics	Symbol	Min	Typ	Max	Units
AMPLIFIERS (AC CHARACTERISTICS)					
AC Input Resistance (@ V_{in})	r_i	—	>30	—	MΩ
Open Loop Gain (Amplifier #1, f < 100 Hz)	A_{VOL1}	80	—	—	dB
Closed Loop Gain (Amplifier #2) (V_{CC} = 6.0 V, f = 1.0 kHz, R_L = 32 Ω)	A_{V2}	−0.35	0	+0.35	dB
Gain Bandwidth Product	GBW	—	1.5	—	MHz
Output Power, V_{CC} = 3.0 V, R_L = 16 Ω, THD ≤ 10% V_{CC} = 6.0 V, R_L = 32 Ω, THD ≤ 10% V_{CC} = 12 V, R_L = 100 Ω, THD ≤ 10%	P_{out3} P_{out6} P_{out12}	55 250 400	— — —	— — —	mW
Total Harmonic Distortion (f = 1.0 kHz) (V_{CC} = 6.0 V, R_L = 32 Ω, P_{out} = 125 mW) (V_{CC} ≥ 3.0 V, R_L = 8.0 Ω, P_{out} = 20 mW) (V_{CC} ≥ 12 V, R_L = 32 Ω, P_{out} = 200 mW)	THD	 — — —	 0.5 0.5 0.6	 1.0 — —	%
Power Supply Rejection (V_{CC} = 6.0 V, ΔV_{CC} = 3.0 V) (C1 = ∞, C2 = 0.01 μF) (C1 = 0.1 μF, C2 = 0, f = 1.0 kHz) (C1 = 1.0 μF, C2 = 5.0 μF, f = 1.0 kHz)	PSRR	 50 — —	 — 12 52	 — — —	dB
Muting (V_{CC} = 6.0 V, 1.0 kHz ≤ f ≤ 20 kHz, CD = 2.0 V)	GMT	—	>70	—	dB
AMPLIFIERS (DC CHARACTERISTICS)					
Output DC Level @ VO1, VO2, V_{CC} = 3.0 V, R_L = 16 Ω (R_f = 75 k) V_{CC} = 6.0 V V_{CC} = 12 V	VO(3) VO(6) VO(12)	1.0 — —	1.15 2.65 5.65	1.25 — —	Vdc
Output High Level (I_{out} = −75 mA, 2.0 V ≤ V_{CC} ≤ 16 V)	V_{OH}	—	V_{CC}−1.0	—	Vdc
Output Low Level (I_{out} = 75 mA, 2.0 V ≤ V_{CC} ≤ 16 V)	V_{OL}	—	0.16	—	Vdc
Output DC Offset Voltage (VO1–VO2) (V_{CC} = 6.0 V, R_f = 75 kΩ, R_L = 32 Ω)	ΔV_O	−30	0	+30	mV
Input Bias Current @ V_{in} (V_{CC} = 6.0 V)	I_{IB}	—	−100	−200	nA
Equivalent Resistance @ FC1 (V_{CC} = 6.0 V)	R_{FC1}	100	150	220	kΩ
Equivalent Resistance @ FC2 (V_{CC} = 6.0 V)	R_{FC2}	18	25	40	kΩ
CHIP DISABLE (Pin 1)					
Input Voltage — Low	V_{IL}	—	—	0.8	Vdc
Input Voltage — High	V_{IH}	2.0	—	—	Vdc
Input Resistance (V_{CC} = V_{CD} = 16 V)	R_{CD}	50	90	175	kΩ
POWER SUPPLY					
Power Supply Current (V_{CC} = 3.0 V, R_L = ∞, CD = 0.8 V) (V_{CC} = 16 V, R_L = ∞, CD = 0.8 V) (V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	 I_{CC3} I_{CC16} I_{CCD}	 — — —	 2.7 3.3 65	 4.0 5.0 100	 mA μA

Note: Currents into a pin are positive, currents out of a pin are negative.

PIN DESCRIPTION

Symbol	Pin	Description
CD	1	Chip Disable — Digital input. A Logic "0" (<0.8 V) sets normal operation. A Logic "1" (≥2.0 V) sets the power down mode. Input impedance is nominally 90 kΩ.
FC2	2	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at FC1 is sufficient.
FC1	3	Analog Ground for the amplifiers. A 1.0 μF capacitor at this pin (with a 5.0 μF capacitor at Pin 2) provides (typically) 52 dB of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
V_{in}	4	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and VO1.
VO1	5	Amplifier Output #1. The dc level is ≈ (V_{CC} − 0.7 V)/2.
V_{CC}	6	DC supply voltage (+2.0 to +16 volts) is applied to this pin.
GND	7	Ground pin for the entire circuit.
VO2	8	Amplifier Output #2. This signal is equal in amplitude, but 180° out of phase with that at VO1. The dc level is ≈ (V_{CC} − 0.7 V)/2.

TYPICAL TEMPERATURE PERFORMANCE (−20° < T_A < +70°C)

Function	Typical Change	Units
Input Bias Current (@ V_{in})	±40	pA/°C
Total Harmonic Distortion (V_{CC} = 6.0 V, R_L = 32 Ω, P_{out} = 125 mW, f = 1.0 kHz)	+0.003	%/°C
Power Supply Current		μA/°C
(V_{CC} = 3.0 V, R_L = ∞, CD = 0 V)	−2.5	
(V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	−0.03	

DESIGN GUIDELINES

GENERAL

The MC34119 is a low power audio amplifier capable of low voltage operation (V_{CC} = 2.0 V minimum) such as that encountered in line-powered speakerphones. The circuit provides a differential output (VO1–VO2) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs to the amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

AMPLIFIERS

Referring to the block diagram, the internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open loop gain of ≥80 dB (at f ≤ 100 Hz), and the closed loop gain is set by external resistors R_f and R_i. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5 MHz. In order to adequately cover the telephone voice band (300–3400 Hz), a maximum closed loop gain of 46 dB is recommended. Amplifier #2 is internally set to a gain of −1.0 (0 dB).

The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200 mA. The outputs can typically swing to within ≈0.4 volts above ground, and to within ≈1.3 volts below V_{CC}, at the maximum current. See Figures 18 and 19 for V_{OH} and V_{OL} curves.

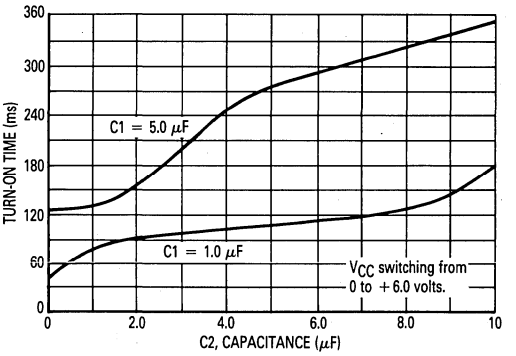
The output dc offset voltage (VO1–VO2) is primarily a function of the feedback resistor (R_f), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be similar for a particular IC, and therefore nearly cancel each other at the outputs. Amplifier #1's bias current, however, flows out of V_{in} (Pin 4) and through R_f, forcing VO1 to shift negative by an amount equal to [R_f x I_{IB}]. VO2 is shifted positive an equal amount. The output offset voltage specified in the Electrical Characteristics is measured with the feedback resistor shown in the Typical Application Circuit, and therefore takes into account the bias current as well as internal offset voltages of the amplifiers. The bias current is constant with respect to V_{CC}.

FC1 and FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the Typical Application Circuit) at FC1 and FC2. C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies, as shown in the graphs of Figures 4–7. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is a function of the capacitors, and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as R_{FC1} and R_{FC2}).

In addition to providing filtering, C1 and C2 also affect the turn-on time of the circuit at power-up, since the two capacitors must charge up through the internal 50 k and 125 kΩ resistors. The graph of Figure 1 indicates the turn-on time upon application of V_{CC} of +6.0 volts. The turn-on time is ≈60% longer for V_{CC} = 3.0 volts, and ≈20% less for V_{CC} = 9.0 volts. Turn-off time is <10 μs upon removal of V_{CC}.

FIGURE 1 — TURN-ON TIME versus C1, C2 AT POWER-ON



CHIP DISABLE

The Chip Disable (Pin 1) can be used to power down the IC to conserve power, or for muting, or both. When at a Logic "0" (0 to 0.8 volts), the MC34119 is enabled for normal operation. When Pin 1 is at a Logic "1" (2.0 to V_{CC} volts), the IC is disabled. If Pin 1 is open, that is equivalent to a Logic "0," although good design practice dictates that an input should never be left open. Input impedance at Pin 1 is a nominal 90 kΩ. The power supply current (when disabled) is shown in Figure 15.

Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70 dB. The turn-off time of the audio output, from the application of the CD signal, is <2.0 μs, and turn on-time is 12–15 ms. Both times are independent of C1, C2, and V_{CC}.

When the MC34119 is disabled, the voltages at FC1 and FC2 do not change as they are powered from V_{CC}. The outputs, VO1 and VO2, change to a high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of V_{CC} and Ground.

POWER DISSIPATION

Figures 8–10 indicate the device dissipation (within the IC) for various combinations of V_{CC}, R_L, and load power. The maximum power which can safely be dissipated within the MC34119 is found from the following equation:

$$P_D = (140°C - T_A)/\theta_{JA}$$

where T_A is the ambient temperature;
and θ_{JA} is the package thermal resistance (100°C/W for the standard DIP package, and 180°C/W for the surface mount package.)

The power dissipated within the MC34119, in a given application, is found from the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (I_{RMS} \times V_{CC}) - (R_L \times I_{RMS}^2)$$

where I_{CC} is obtained from Figure 15;
and I_{RMS} is the RMS current at the load;
and R_L is the load resistance.

Figures 8–10, along with Figures 11–13 (distortion curves), and a peak working load current of ±200 mA, define the operating range for the MC34119. The operating range is further defined in terms of allowable load power in Figure 14 for loads of 8.0 Ω, 16 Ω, and 32 Ω. The left (ascending) portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the MC34119. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long term reliability.

LAYOUT CONSIDERATIONS

Normally a snubber is not needed at the output of the MC34119, unlike many other audio amplifiers. However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally the speaker wires should be twisted tightly, and be not more than a few inches in length.

TYPICAL CHARACTERISTICS

FIGURE 2 — AMPLIFIER #1 OPEN LOOP GAIN AND PHASE

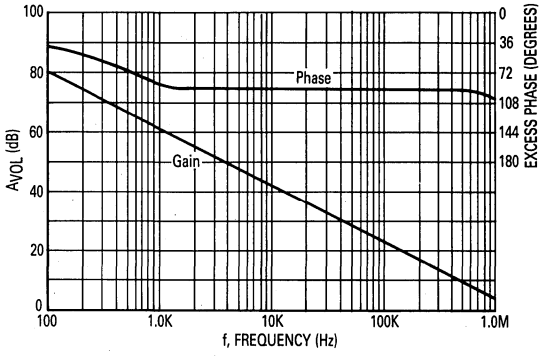
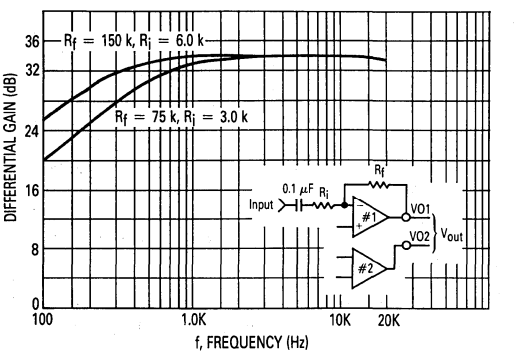


FIGURE 3 — DIFFERENTIAL GAIN versus FREQUENCY



POWER SUPPLY REJECTION versus FREQUENCY

FIGURE 4 — C2 = 10 μF

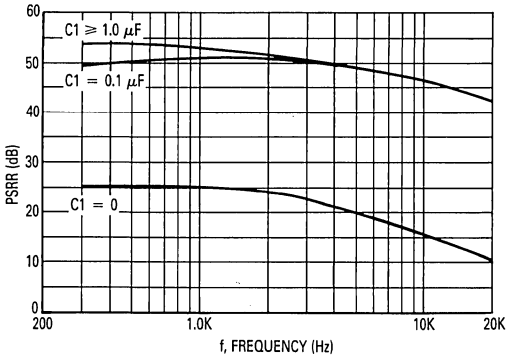


FIGURE 5 — C2 = 5.0 μF

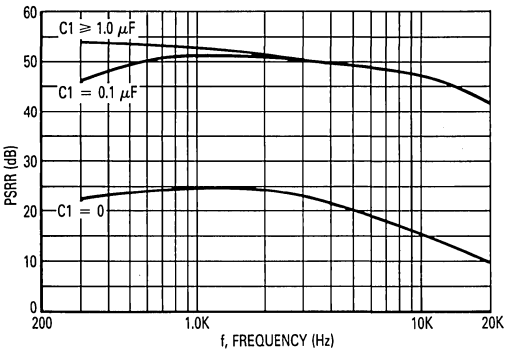


FIGURE 6 — C2 = 1.0 μF

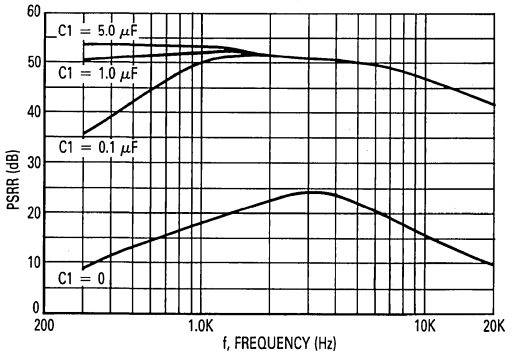


FIGURE 7 — C2 = 0

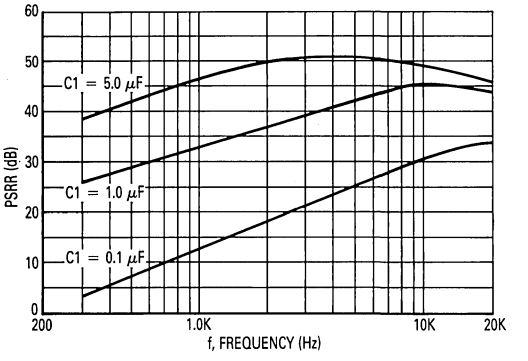


FIGURE 8 — DEVICE DISSIPATION 8.0 Ω LOAD

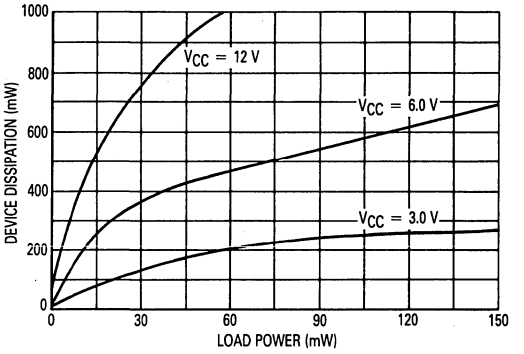


FIGURE 9 — DEVICE DISSIPATION 16 Ω LOAD

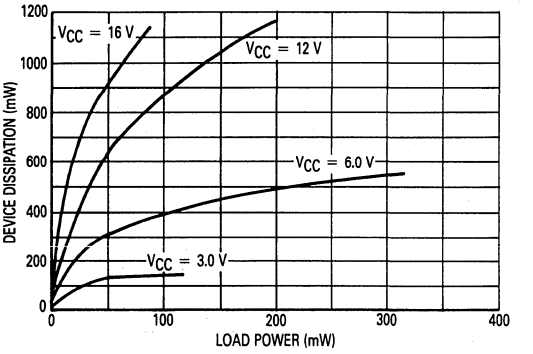


FIGURE 10 — DEVICE DISSIPATION 32 Ω LOAD

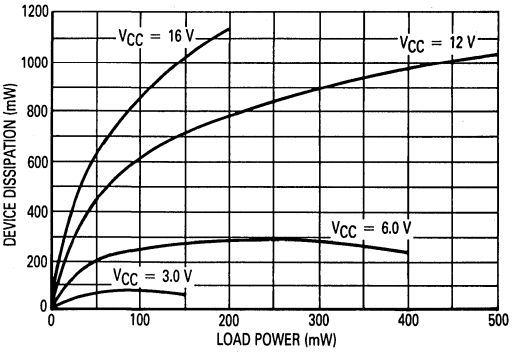


FIGURE 11 — DISTORTION versus POWER f = 1.0 kHz, AVD = 34 dB

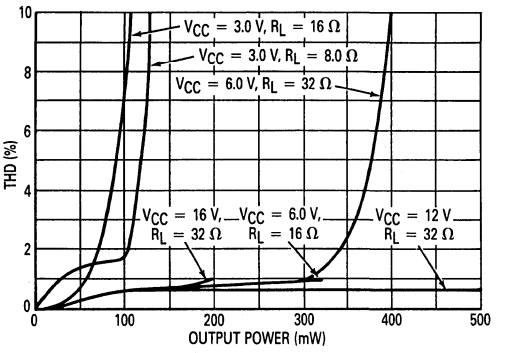


FIGURE 12 — DISTORTION versus POWER f = 3.0 kHz, AVD = 34 dB

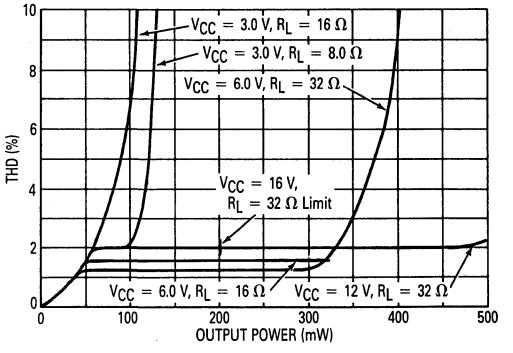


FIGURE 13 — DISTORTION versus POWER f = 1, 3.0 kHz, AVD = 12 dB

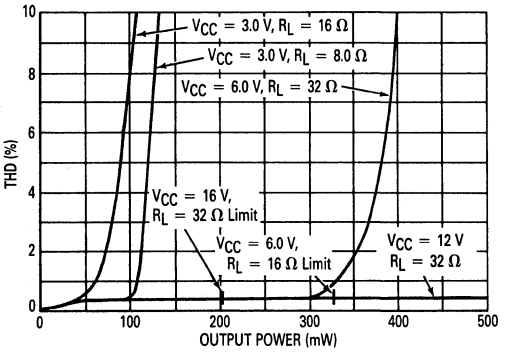


FIGURE 14 — MAXIMUM ALLOWABLE LOAD POWER

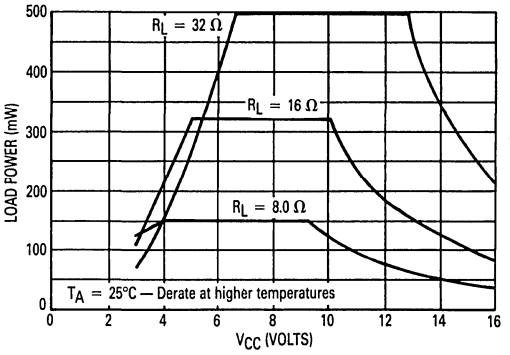


FIGURE 15 — POWER SUPPLY CURRENT

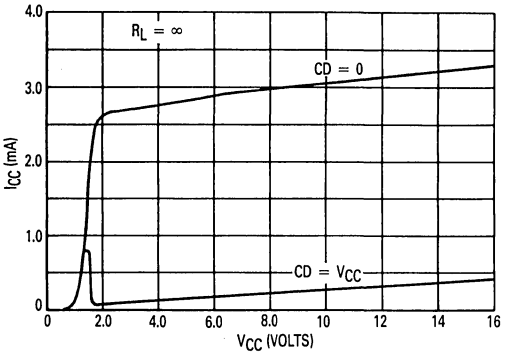


FIGURE 16 — SMALL SIGNAL RESPONSE

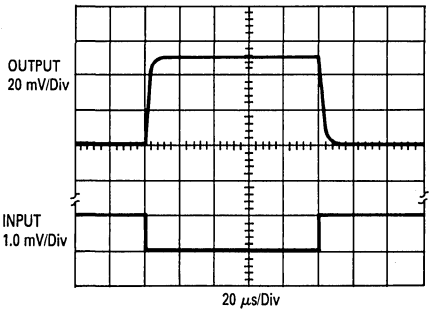


FIGURE 17 — LARGE SIGNAL RESPONSE

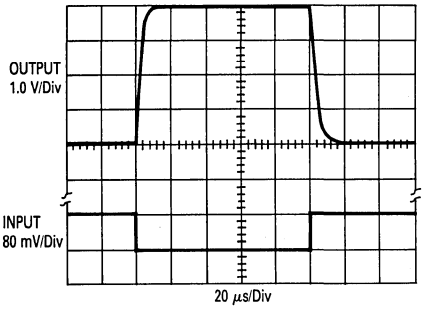


FIGURE 18 — V_{CC}–V_{OH} @ VO1, VO2 versus LOAD CURRENT

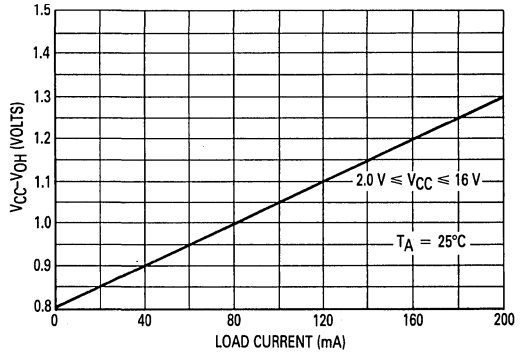


FIGURE 19 — V_{OL} @ VO1, VO2 versus LOAD CURRENT

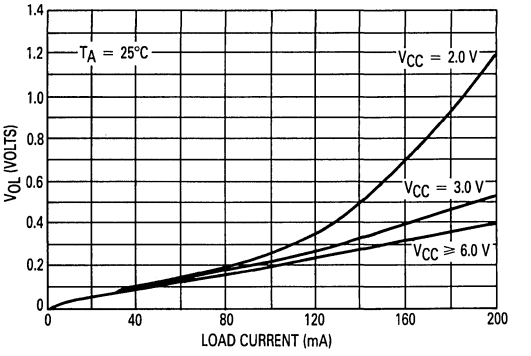


FIGURE 20 — INPUT CHARACTERISTICS @ CD (PIN 1)

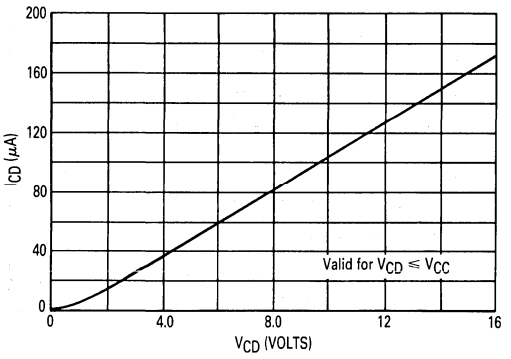
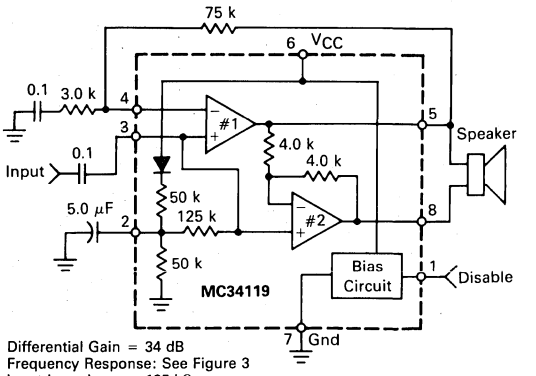


FIGURE 21 — AUDIO AMPLIFIER WITH HIGH INPUT IMPEDANCE



Differential Gain = 34 dB
Frequency Response: See Figure 3
Input Impedance ≈ 125 kΩ
PSRR ≈ 50 dB

FIGURE 22 — AUDIO AMPLIFIER WITH BASS SUPPRESSION

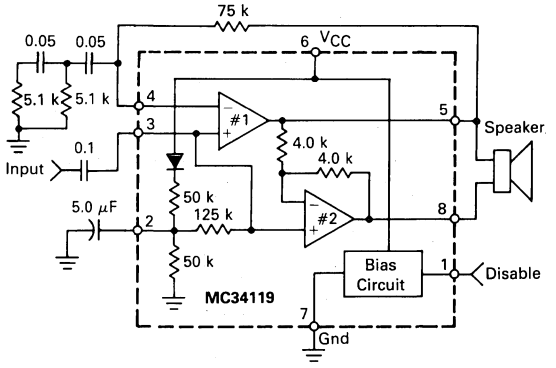


FIGURE 23 — FREQUENCY RESPONSE OF FIGURE 22

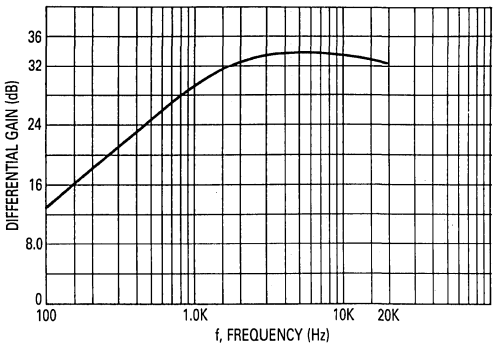


FIGURE 24 — AUDIO AMPLIFIER WITH BANDPASS

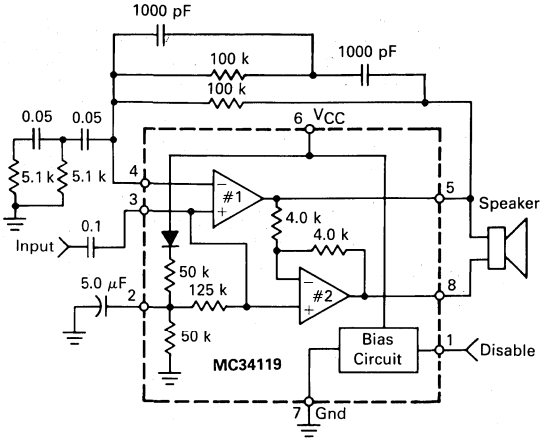


FIGURE 25 — FREQUENCY RESPONSE OF FIGURE 24

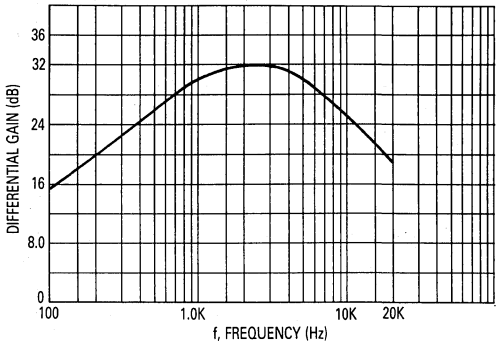
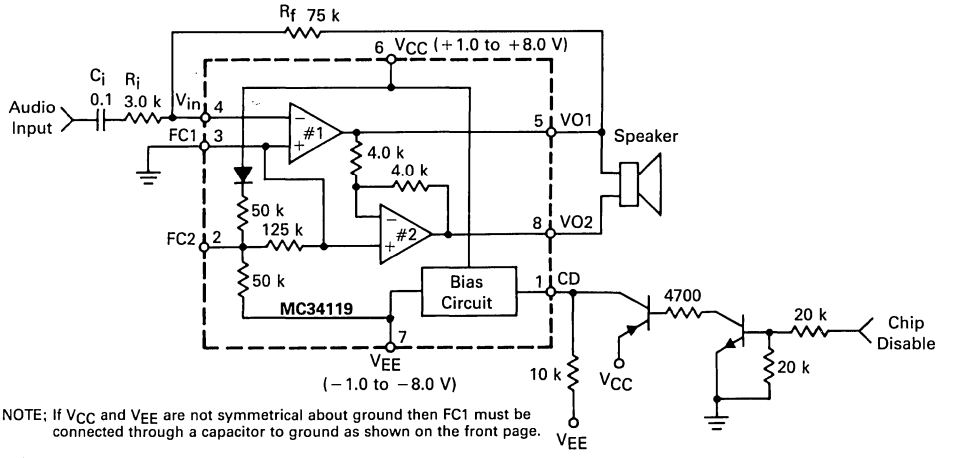


FIGURE 26 — SPLIT SUPPLY OPERATION



NOTE: If V_{CC} and V_{EE} are not symmetrical about ground then FC1 must be connected through a capacitor to ground as shown on the front page.

MC34129
MC33129

Specifications and Applications Information

HIGH PERFORMANCE CURRENT MODE CONTROLLER

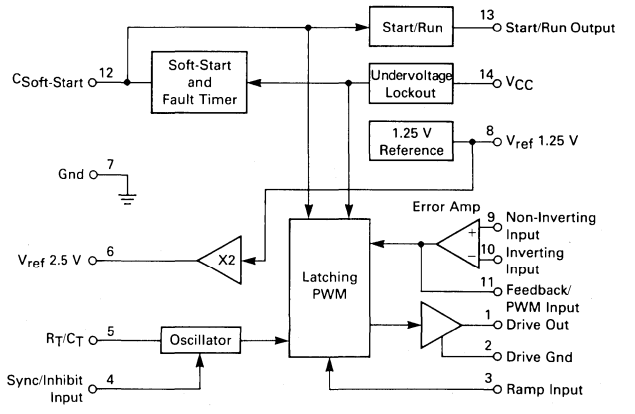
The MC34129 series are high performance current mode switching regulators specifically designed for use in low power digital telephone applications. These integrated circuits feature a unique internal fault timer that provides automatic restart for overload recovery. For enhanced system efficiency, a start/run comparator is included to implement bootstrapped operation of V_{CC}. Other functions contained are a temperature compensated reference, reference amplifier, fully accessible error amplifier, sawtooth oscillator with sync input, pulse width modulator comparator, and a high current totem pole driver ideally suited for driving a power MOSFET.

Also included are protective features consisting of soft-start, undervoltage lockout, cycle-by-cycle current limiting, adjustable dead time, and a latch for single pulse metering.

Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in many other applications.

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Continuous Retry after Fault Timeout
- Soft-Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- High Current Totem Pole Driver
- Input Undervoltage Lockout
- Low Start-Up and Operating Current
- Direct Interface with Motorola SENSEFET Products

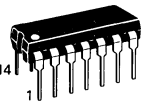
SIMPLIFIED BLOCK DIAGRAM



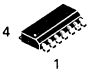
SENSEFET is a trademark of Motorola Inc.

HIGH PERFORMANCE CURRENT MODE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

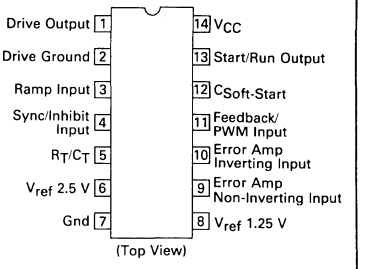


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
SO-14

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC34129D	0 to +70°C	SO-14 Plastic DIP
MC34129P	0 to +70°C	Plastic DIP
MC33129D	−40 to +85°C	SO-14 Plastic DIP
MC33129P	−40 to +85°C	Plastic DIP

MAXIMUM RATING

Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(V_{CC})}$	50	mA
Start/Run Output Zener Current	$I_{Z(Start/Run)}$	50	mA
Analog Inputs (Pins 3, 5, 9, 10, 11, 12)	—	−0.3 to 5.5	V
Sync Input Voltage	V_{sync}	−0.3 to V_{CC}	V
Drive Output Current, Source or Sink	I_{DRV}	1.0	A
Current, Reference Outputs (Pins 6, 8)	I_{ref}	20	mA
Power Dissipation and Thermal Characteristics D Suffix Package SO-14 Case 751A-01 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air P Suffix Package Case 646-06 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 552 145 800 100	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34129 MC33129	T_A	 0 to +70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1] unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTIONS					
Reference Output Voltage, T_A = 25°C 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.225 2.375	 1.250 2.500	 1.275 2.625	V
Reference Output Voltage, T_A = T_{low} to T_{high} 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.200 2.250	 — —	 1.300 2.750	V
Line Regulation (V_{CC} = 4.0 V to 12 V) 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	Reg_{line}	 — —	 2.0 10	 12 50	mV
Load Regulation 1.25 V Ref., I_L = −10 to +500 μA 2.50 V Ref., I_L = −0.1 to +1.0 mA	Reg_{load}	 — —	 1.0 3.0	 12 25	mV
ERROR AMPLIFIER					
Input Offset Voltage (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	V_{IO}	 — —	 1.5 —	 — 10	mV
Input Offset Current (V_{in} = 1.25 V)	I_{IO}	—	10	—	nA
Input Bias Current (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	I_{IB}	 — —	 25 —	 — 200	nA
Input Common-Mode Voltage Range	V_{ICR}	—	0.5 to 5.5	—	V
Open-Loop Voltage Gain (V_O = 1.25 V)	A_{VOL}	65	87	—	dB
Gain Bandwidth Product (V_O = 1.25 V, f = 100 kHz)	GBW	500	750	—	kHz
Power Supply Rejection Ratio (V_{CC} = 5.0 to 10 V)	PSRR	65	85	—	dB
Output Source Current (V_O = 1.5 V)	I_{Source}	40	80	—	μA
Output Voltage Swing High State (I_{Source} = 0 μA) Low State (I_{Sink} = 500 μA)	 V_{OH} V_{OL}	 1.75 —	 1.96 0.1	 2.25 0.15	V

Note 1. T_{low} = 0°C for MC34129
= −40°C for MC33129
T_{high} = +70°C for MC34129
= +85°C for MC33129

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1] unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR					
Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	150	275	400	mV
Input Bias Current	I_{IB}	—	−120	−250	μA
Propagation Delay, Ramp Input to Drive Output	$t_{PLH(IN/DRV)}$	—	250	—	ns
SOFT-START					
Capacitor Charge Current (Pin 12 = 0 V)	I_{chg}	0.75	1.2	1.50	μA
Buffer Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	—	15	40	mV
Buffer Output Voltage (I_{Sink} = 100 μA)	V_{OL}	—	0.15	0.225	V
FAULT TIMER					
Restart Delay Time	t_{DLY}	200	400	600	μs
START/RUN COMPARATOR					
Threshold Voltage (Pin 12)	V_{th}	—	2.0	—	V
Threshold Hysteresis Voltage (Pin 12)	V_H	—	350	—	mV
Output Voltage (I_{Sink} = 500 μA)	V_{OL}	9.0	10	10.3	V
Output Off-State Leakage Current (V_{OH} = 15 V)	$I_{S/R(leak)}$	—	0.4	2.0	μA
Output Zener Voltage (I_Z = 10 mA)	V_Z	—	(V_{CC} + 7.6)	—	V
OSCILLATOR					
Frequency (R_T = 25.5 kΩ, C_T = 390 pF)	f_{OSC}	80	100	120	kHz
Capacitor C_T Discharge Current (Pin 5 = 1.2 V)	I_{dischg}	240	350	460	μA
Sync Input Current High State (V_{in} = 2.0 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 — —	 40 15	 125 35	μA
Sync Input Resistance	R_{in}	12.5	32	50	kΩ
DRIVE OUTPUT					
Output Voltage High State (I_{Source} = 200 mA) Low State (I_{Sink} = 200 mA)	 V_{OH} V_{OL}	 8.3 —	 8.9 1.4	 — 1.8	V
Low State Holding Current	I_H	—	225	—	μA
Output Voltage Rise Time (C_L = 500 pF)	t_r	—	100	—	ns
Output Voltage Fall Time (C_L = 500 pF)	t_f	—	30	—	ns
Output Pull-Down Resistance	R_{PD}	100	225	350	kΩ
UNDERVOLTAGE LOCKOUT					
Start-Up Threshold	V_{th}	3.0	3.6	4.2	V
Hysteresis	V_H	5.0	10	15	%
TOTAL DEVICE					
Power Supply Current R_T = 25.5 kΩ, C_T = 390 pF, C_L = 500 pF	I_{CC}	1.0	2.5	4.0	mA
Power Supply Zener Voltage (I_Z = 10 mA)	V_Z	12	14.3	—	V

Note 1. T_{low} = 0°C for MC34129 = −40°C for MC33129 T_{high} = +70°C for MC34129 = +85°C for MC33129

FIGURE 1 — TIMING RESISTOR versus OSCILLATOR FREQUENCY

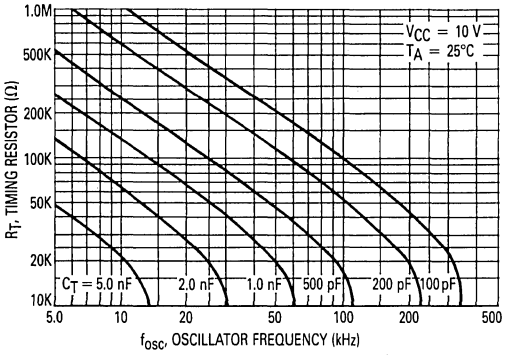


FIGURE 2 — OUTPUT DEAD-TIME versus OSCILLATOR FREQUENCY

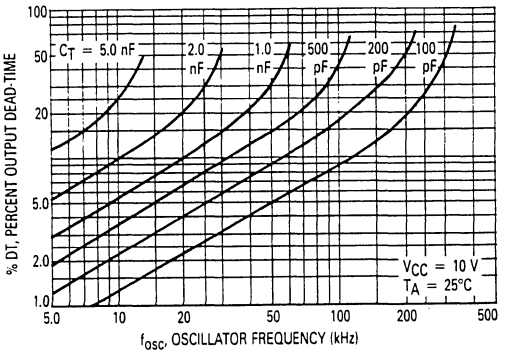


FIGURE 3 — OSCILLATOR FREQUENCY CHANGE versus TEMPERATURE

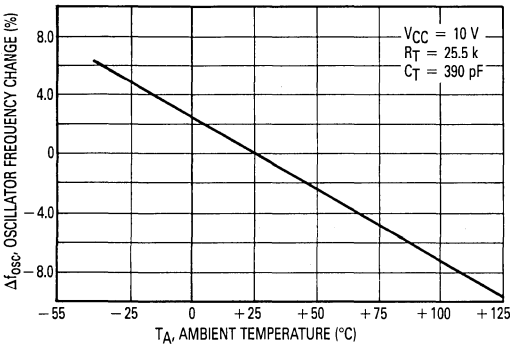


FIGURE 4 — ERROR AMP OPEN-LOOP GAIN AND PHASE versus FREQUENCY

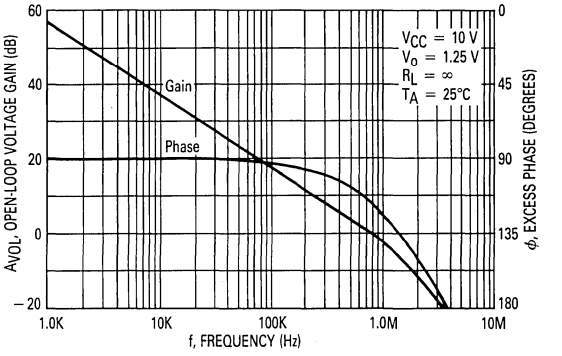


FIGURE 5 — ERROR AMP SMALL-SIGNAL TRANSIENT RESPONSE

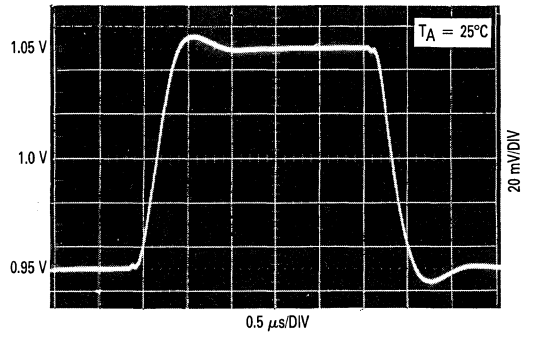


FIGURE 6 — ERROR AMP LARGE-SIGNAL TRANSIENT RESPONSE

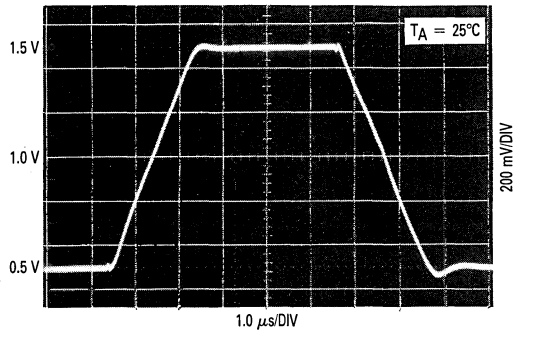


FIGURE 7 — ERROR AMP OPEN-LOOP DC GAIN versus LOAD RESISTANCE

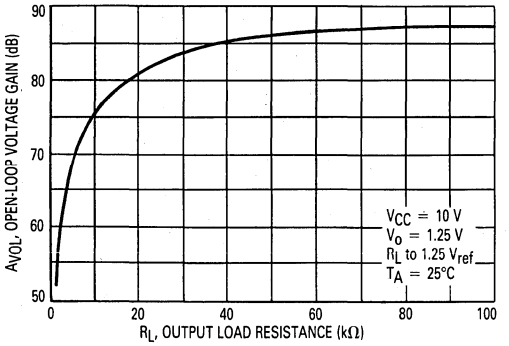


FIGURE 8 — ERROR AMP OUTPUT SATURATION versus SINK CURRENT

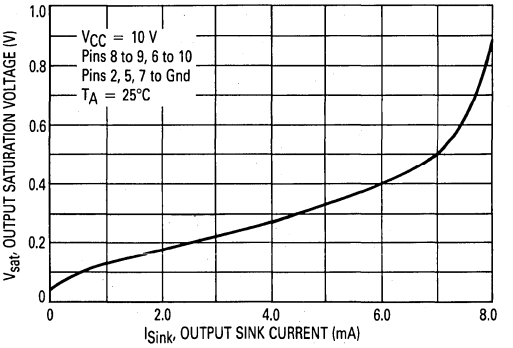


FIGURE 9 — SOFT-START BUFFER OUTPUT SATURATION versus SINK CURRENT

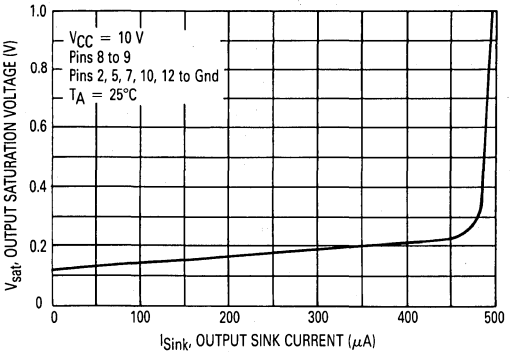


FIGURE 10 — REFERENCE OUTPUT VOLTAGE versus SUPPLY VOLTAGE

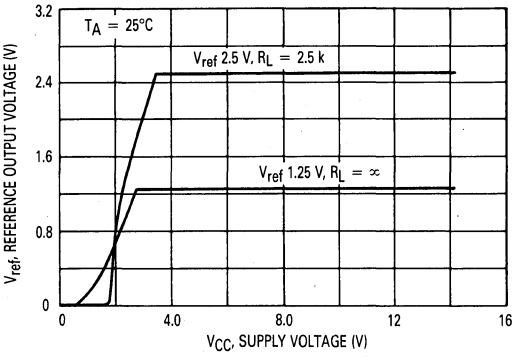


FIGURE 11 — 1.25 V REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

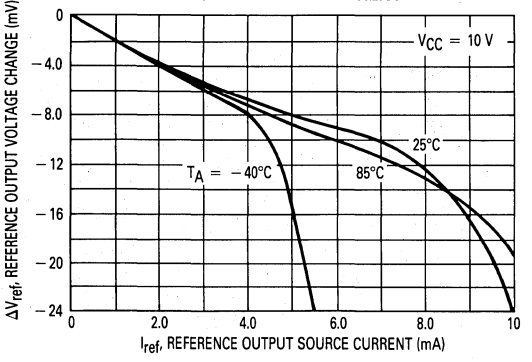


FIGURE 12 — 2.5 V REFERENCE OUTPUT VOLTAGE CHANGE versus SOURCE CURRENT

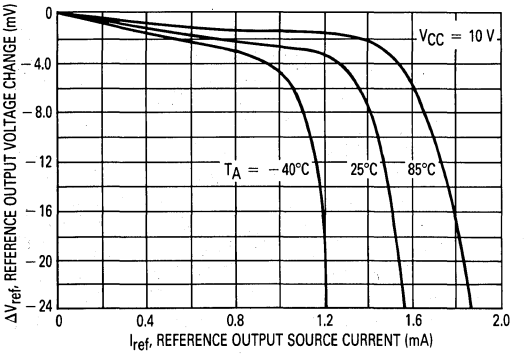


FIGURE 13 — 1.25 V REFERENCE OUTPUT VOLTAGE versus TEMPERATURE

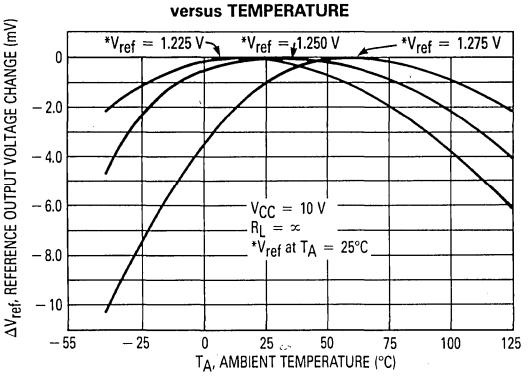


FIGURE 14 — 2.5 V REFERENCE OUTPUT VOLTAGE versus TEMPERATURE

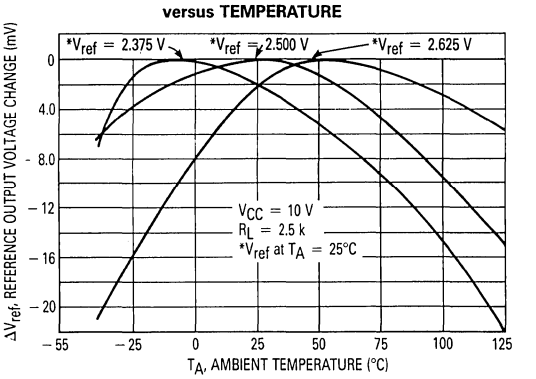


FIGURE 15 — DRIVE OUTPUT SATURATION versus LOAD CURRENT

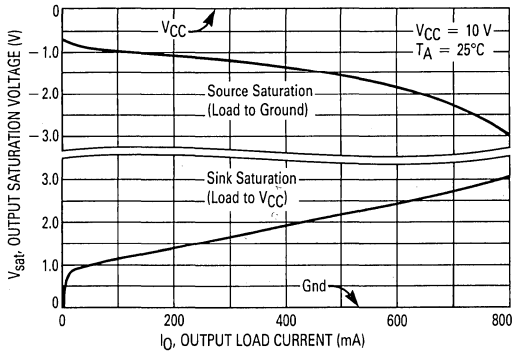


FIGURE 16 — DRIVE OUTPUT WAVEFORM

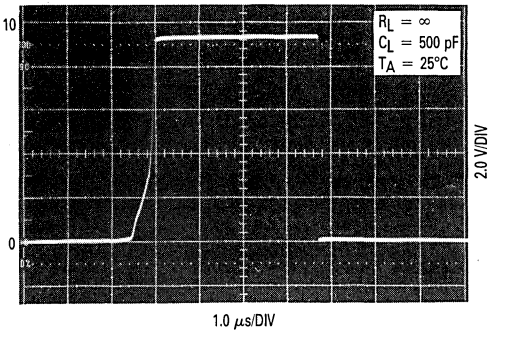
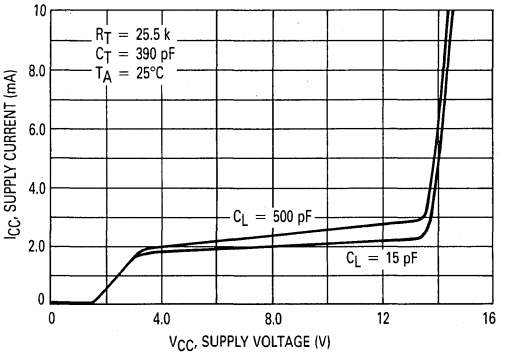


FIGURE 17 — SUPPLY CURRENT versus SUPPLY VOLTAGE



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	Drive Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sinked by this pin.
2	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
3	Ramp Input	A voltage proportional to the inductor current is connected to this input. The PWM uses this information to terminate output switch conduction.
4	Sync/Inhibit Input	A rectangular waveform applied to this input will synchronize the Oscillator and limit the maximum Drive Output duty cycle. A dc voltage within the range of 2.0 V to V_{CC} will inhibit the controller.
5	R_T/C_T	The free-running Oscillator frequency and maximum Drive Output duty cycle are programmed by connecting resistor R_T to V_{ref} 2.5 V and capacitor C_T to Ground. Operation to 300 kHz is possible.
6	V_{ref} 2.50 V	This output is derived from V_{ref} 1.25 V. It provides charging current for capacitor C_T through resistor R_T.
7	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
8	V_{ref} 1.25 V	This output furnishes a voltage reference for the Error Amplifier Non-Inverting Input.
9	Error Amp Non-Inverting Input	This is the non-inverting input of the Error Amplifier. It is normally connected to the 1.25 V reference.
10	Error Amp Inverting Input	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
11	Feedback/PWM Input	This pin is available for loop compensation. It is connected to the Error Amplifier and Soft-Start Buffer outputs, and the Pulse Width Modulator input.
12	$C_{Soft\text{-}Start}$	A capacitor $C_{Soft\text{-}Start}$ is connected from this pin to Ground for a controlled ramp-up of peak inductor current during start-up.
13	Start/Run Output	This output controls the state of an external bootstrap transistor. During the start mode, operating bias is supplied by the transistor from V_{in}. In the run mode, the transistor is switched off and bias is supplied by an auxiliary power transformer winding.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 4.2 V to 12 V.

OPERATING DESCRIPTION

The MC34129 series are high performance current mode switching regulator controllers specifically designed for use in low power telecommunication applications. Implementation will allow remote digital telephones and terminals to shed their power cords and derive operating power directly from the twisted pair used for data transmission. Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in a wide range of converter applications. A representative block diagram is shown in Figure 18.

OSCILLATOR

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 2.5 V reference through resistor R_T to approximately 1.25 V and discharged by an internal current sink to ground. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the lower input of the NOR gate high. This causes the Drive Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows Oscillator Frequency versus R_T and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. In many noise sensitive applications it may be desirable to frequency-lock one or more switching regulators to an external system clock. This can be accomplished by applying the clock signal to the Sync/Inhibit Input. For reliable locking, the free-running oscillator frequency should be about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 19, the rising edge of the clock signal applied to the Sync/Inhibit Input, terminates charging of C_T and Drive Output conduction. By tailoring the clock waveform, accurate duty cycle clamping of the Drive Output can be achieved. A circuit method is shown in Figure 20. The Sync/Inhibit Input may also be used as a means for system shutdown by applying a dc voltage that is within the range of 2.0 V to V_{CC}.

PWM COMPARATOR AND LATCH

The MC34129 operates as a current mode controller whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches a threshold level established by the output of the Error Amp or Soft-Start Buffer (Pin 11). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The PWM Comparator-Latch configuration used, ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground-referenced resistor R_S in series with the source of output switch Q_1. The Ramp Input adds an offset of 275 mV to this voltage to guarantee that no pulses appear at the Drive Output when Pin 11 is at its lowest state. This occurs at the beginning of the soft-start interval or when the power supply is operating and the load is removed. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 11 where:

$$I_{pk} = \frac{V_{(Pin\ 11)} - 0.275\ V}{R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the voltage at Pin 11 will be internally clamped to 1.95 V by the output of the Soft-Start Buffer. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.95\ V - 0.275}{R_S} = \frac{1.675\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method which adjusts this voltage in discrete increments is shown in Figure 22. This method is possible because the Ramp Input bias current is always negative (typically $-120\ \mu A$). A positive temperature coefficient equal to that of the diode string will be exhibited by $I_{pk(max)}$. An adjustable method that is more precise and temperature stable is shown in Figure 23. Erratic operation due to noise pickup can result if there is an excessive reduction of the clamp voltage. In this situation, high frequency circuit layout techniques are imperative.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 25.

ERROR AMP AND SOFT-START BUFFER

A fully-compensated Error Amplifier with access to both inputs and output is provided for maximum design flexibility. The Error Amplifier output is common with that of the Soft-Start Buffer. These outputs are open-collector (sink only) and are ORed together at the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the loop. Soft-start is mandatory for stable start-up when power is provided through a high source impedance such as the long twisted pair used in telecommunications. It effectively removes the load from the output of the switching power supply upon initial start-up. The Soft-Start Buffer is configured as a unity gain follower with the non-inverting input connected to Pin 12. An internal 1.0 μA

FIGURE 18 — REPRESENTATIVE BLOCK DIAGRAM

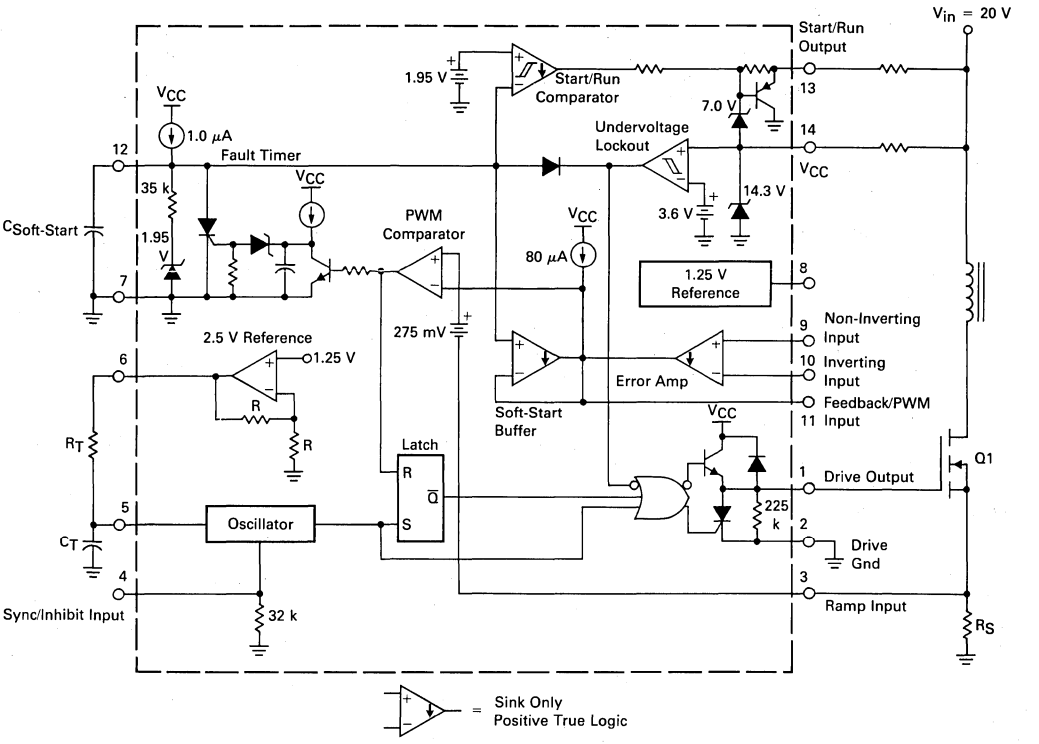
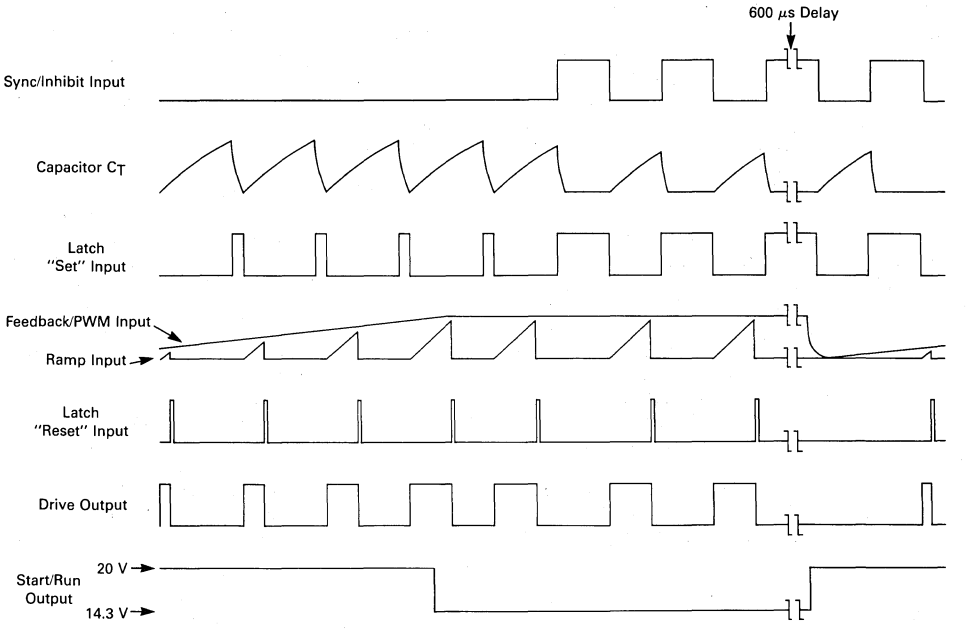


FIGURE 19 — TIMING DIAGRAM



OPERATING DESCRIPTION (continued)

current source charges the soft-start capacitor ($C_{Soft-Start}$) to an internally clamped level of 1.95 V. The rate of change of peak inductor current, during start-up, is programmed by the capacitor value selected. Either the Fault Timer or the Undervoltage Lockout can discharge the soft-start capacitor.

FAULT TIMER

This unique circuit prevents sustained operation in a lockout condition. This can occur with conventional switching control IC's when operating from a power source with a high series impedance. If the power required by the load is greater than that available from the source, the input voltage will collapse, causing the lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions, the output of the PWM Comparator will reset the Latch and discharge the internal Fault Timer capacitor on a cycle-by-cycle basis. Under operating conditions where the required power into the load is greater than that available from the source (V_{in}), the Ramp Input voltage (plus offset) will not reach the comparator threshold level (Pin 11), and the output of the PWM Comparator will remain low. If this condition persists for more than 600 μs, the Fault Timer will activate, discharging $C_{Soft-Start}$ and initiating a soft-start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load power or source impedance is reduced. The minimum fault timeout is 200 μs, which limits the useful switching frequency to a minimum of 5.0 kHz.

START/RUN COMPARATOR

A bootstrap start-up circuit is included to improve system efficiency when operating from a high input voltage. The output of the Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 21. While $C_{Soft-Start}$ is charging, start-up bias is supplied to V_{CC} (Pin 14) from V_{in} through transistor Q2. When $C_{Soft-Start}$ reaches the 1.95 V clamp level, the Start-Run output switches low (V_{CC} – 50 mV), turning off Q2. Operating bias is now derived from the auxiliary bootstrap winding of the transformer, and all drive power is efficiently converted down from V_{in}. The start time must be long enough for the power supply output to reach regulation. This will ensure that there is sufficient bias voltage at the auxiliary bootstrap winding for sustained operation.

$$t_{Start} = \frac{1.95\ V\ C_{Soft-Start}}{1.0\ \mu A} = 1.95\ C_{Soft-Start\ in\ \mu F}$$

The Start/Run Comparator has 350 mV of hysteresis. The output off-state is clamped to V_{CC} + 7.6 V by the internal zener and PNP transistor base-emitter junction.

DRIVE OUTPUT AND DRIVE GROUND

The MC34129 contains a single totem-pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem-pole stage consists of an NPN transistor for turn-on drive and a high speed SCR for turn-off. The SCR design requires less average supply current (I_{CC}) when compared to conventional switching control IC's that use an all NPN totem-pole. The SCR accomplishes this during turn-off of the MOSFET, by utilizing the gate charge as regenerative on-bias, whereas the conventional all transistor design requires continuous base current. Conversion efficiency in low power applications is greatly enhanced with this reduction of I_{CC}. The SCR's low-state holding current (I_H) is typically 225 μA. An internal 225 kΩ pull-down resistor is included to shunt the Drive Output off-state leakage to ground when the Undervoltage Lockout is active. A separate Drive Ground is provided to reduce the effects of switching transient noise imposed on the Ramp Input. This feature becomes particularly useful when the $I_{pk(max)}$ clamp level is reduced. Figure 24 shows the proper implementation of the MC34129 with a current sensing power MOSFET.

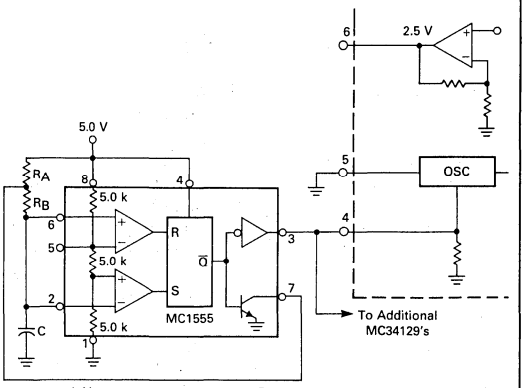
UNDERVOLTAGE LOCKOUT

The Undervoltage Lockout comparator holds the Drive Output and $C_{Soft-Start}$ pins in the low state when V_{CC} is less than 3.6 V. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft-start cycle begins. A built-in hysteresis of 350 mV prevents erratic output behavior as V_{CC} crosses the comparator threshold voltage. A 14.3 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the MOSFET gate from excessive drive voltage during system start-up. An external 9.1 V zener is required when driving low threshold MOSFETs. Refer to Figure 21. The minimum operating voltage range of the IC is 4.2 V to 12 V.

REFERENCES

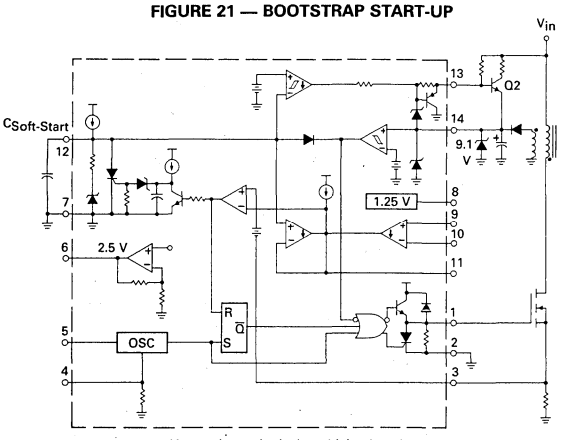
The 1.25 V bandgap reference is trimmed to ±2.0% tolerance at T_A = 25°C. It is intended to be used in conjunction with the Error Amp. The 2.50 V reference is derived from the 1.25 V reference by an internal op amp with a fixed gain of 2.0. It has an output tolerance of ±5.0% at T_A = 25°C and its primary purpose is to supply charging current to the oscillator timing capacitor.

FIGURE 20 — EXTERNAL DUTY CYCLE CLAMP AND MULTI UNIT SYNCHRONIZATION



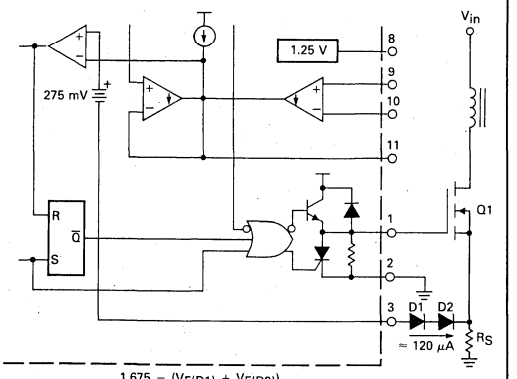
$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

FIGURE 21 — BOOTSTRAP START-UP



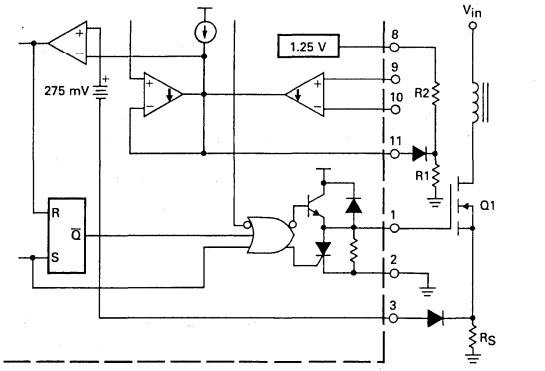
The external 9.1 V zener is required when driving low threshold MOSFETs.

FIGURE 22 — DISCRETE STEP REDUCTION OF CLAMP LEVEL



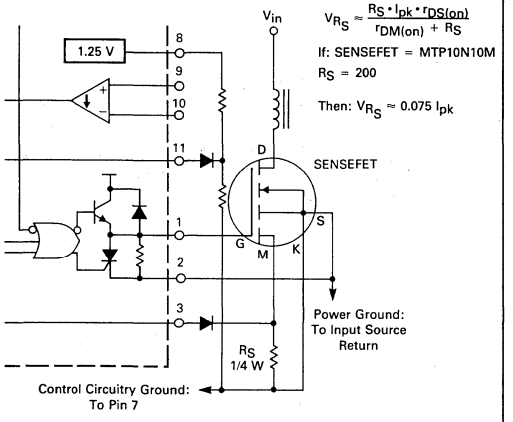
$$I_{pk(max)} = \frac{1.675 - (V_{F(D1)} + V_{F(D2)})}{R_S}$$

FIGURE 23 — ADJUSTABLE REDUCTION OF CLAMP LEVEL



If: $\frac{1.25\ V}{R1 + R2} \geq 1.0\ mA$ Then: $I_{pk(max)} \approx \frac{\frac{1.25}{\left(\frac{R2}{R1} + 1\right)} - 0.275}{R_S}$

FIGURE 24 — CURRENT SENSING POWER MOSFET



$$V_{R_S} \approx \frac{R_S \cdot I_{pk} \cdot r_{DS(on)}}{r_{DM(on)} + R_S}$$

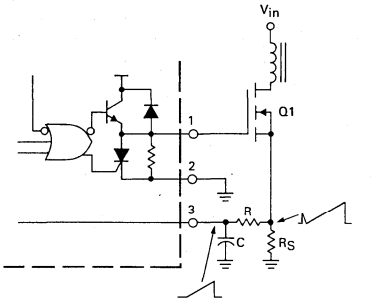
If: SENSEFET = MTP10N10M

R_S = 200

Then: $V_{R_S} \approx 0.075\ I_{pk}$

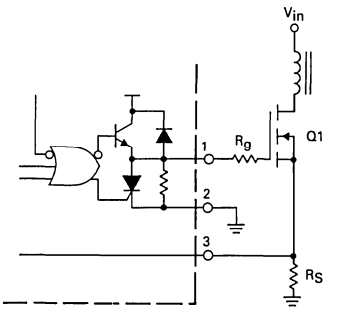
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch.

FIGURE 25 — CURRENT WAVEFORM SPIKE SUPPRESSION



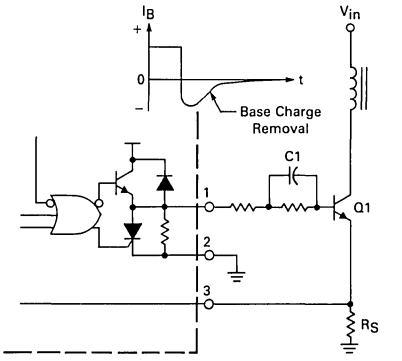
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

FIGURE 26 — MOSFET PARASITIC OSCILLATIONS



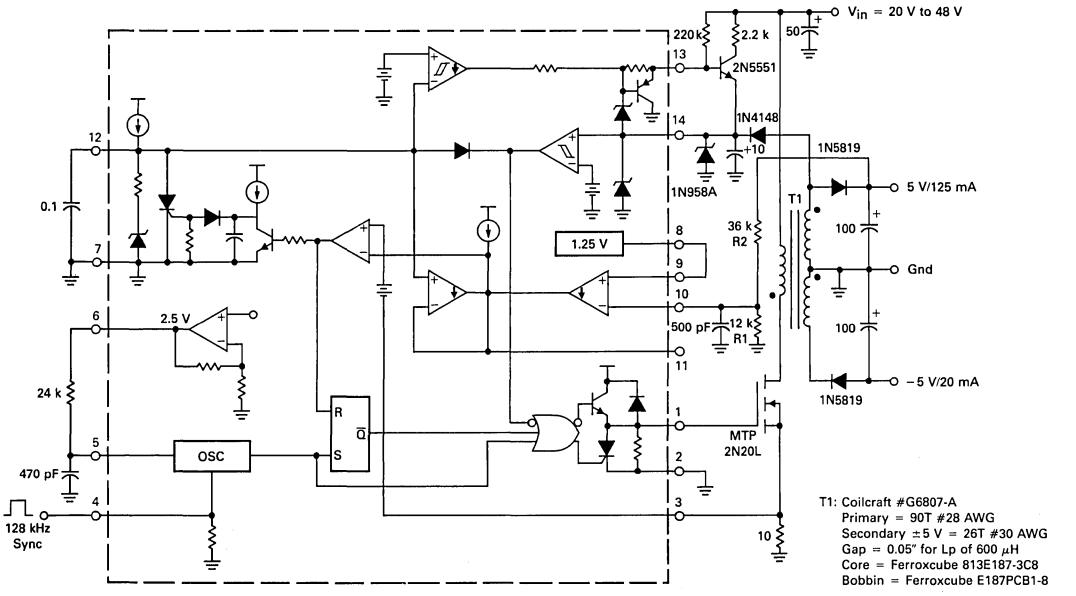
Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

FIGURE 27 — BIPOLAR TRANSISTOR DRIVE



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C1.

FIGURE 28 — NON-ISOLATED 725 mW FLYBACK REGULATOR

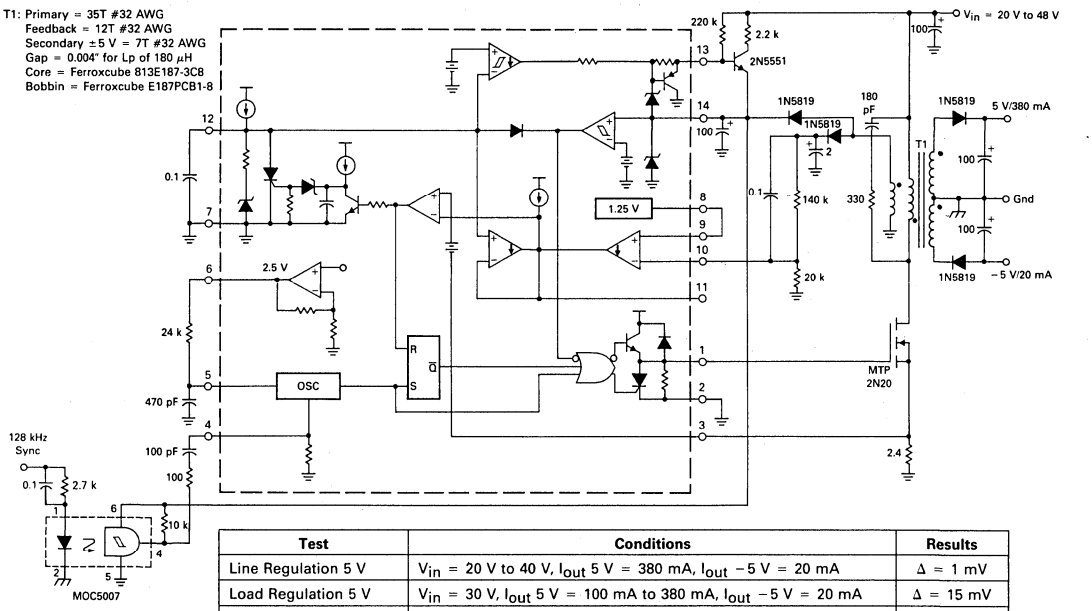


T1: Coilcraft #G6807-A
Primary = 90T #28 AWG
Secondary ±5 V = 26T #30 AWG
Gap = 0.05" for Lp of 600 μH
Core = Ferroxcube 813E187-3C8
Bobbin = Ferroxcube E187PCB1-8

Test	Conditions	Results
Line Regulation 5 V	V_{in} = 20 V to 40 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	Δ = 1.0 mV
Load Regulation 5 V	V_{in} = 30 V, I_{out} 5 V = 0 mA to 150 mA, I_{out} −5 V = 20 mA	Δ = 2.0 mV
Output Ripple 5 V	V_{in} = 30 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	150 mVp-p
Efficiency	V_{in} = 30 V, I_{out} 5 V = 125 mA, I_{out} −5 V = 20 mA	77%

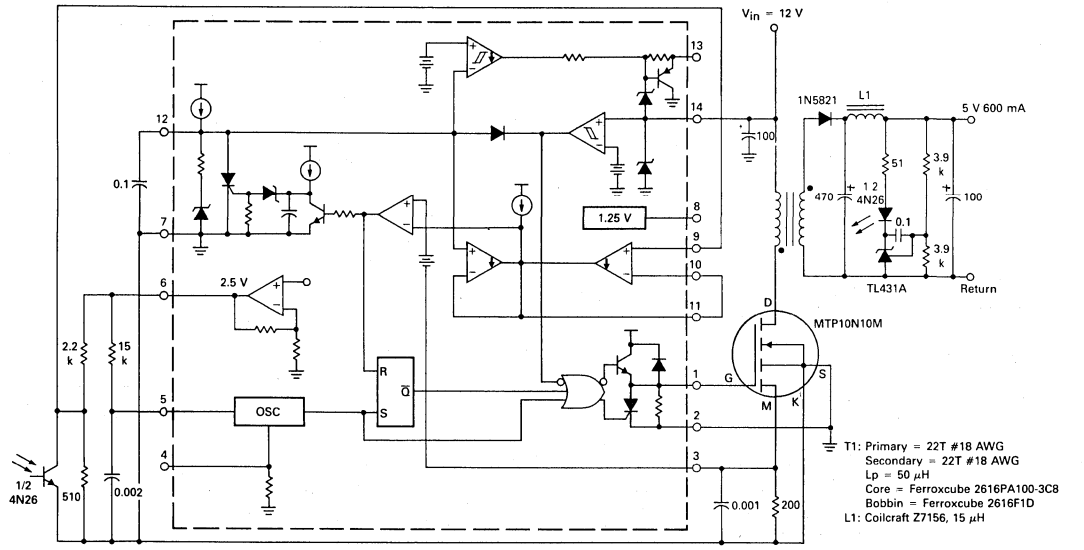
$$V_{out} = 1.25\left(\frac{R2}{R1} + 1\right)$$

FIGURE 29 — ISOLATED 2.0 W FLYBACK REGULATOR



Test	Conditions	Results
Line Regulation 5 V	V_{in} = 20 V to 40 V, I_{out} 5 V = 380 mA, I_{out} −5 V = 20 mA	Δ = 1 mV
Load Regulation 5 V	V_{in} = 30 V, I_{out} 5 V = 100 mA to 380 mA, I_{out} −5 V = 20 mA	Δ = 15 mV
Output Ripple 5 V	V_{in} = 30 V, I_{out} 5 V = 380 mA, I_{out} −5 V = 20 mA	150 mVp-p
Efficiency	V_{in} = 30 V, I_{out} 5 V = 380 mA, I_{out} −5 V = 20 mA	73%

FIGURE 30 — ISOLATED 3.0 W FLYBACK REGULATOR WITH SECONDARY SIDE SENSING



Test	Conditions	Results
Line Regulation	V_{in} = 8 V to 12 V, I_{out} 600 mA	Δ = 1 mV
Load Regulation	V_{in} = 12 V, I_{out} = 100 mA to 600 mA	Δ = 8 mV
Output Ripple	V_{in} = 12 V, I_{out} = 600 mA	20 mVp-p
Efficiency	V_{in} = 12 V, I_{out} = 600 mA	81%

An economical method of achieving secondary sensing is to combine the TL431A with a 4N26 optocoupler.

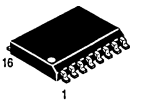
MC142100
MC145100

4 × 4 Crosspoint Switch with Control Memory

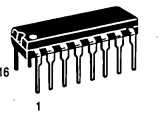
The MC142100 and MC145100 consist of 16 crosspoint switches (analog transmission gates) organized in 4 rows and 4 columns. Both devices have 16 latches, each of which controls the state of a particular switch. Any of the 16 switches can be selected by applying its address to the device and a pulse to the strobe input. The selected crosspoint will turn on if during strobe, D_{in} was a 1 and will turn off if during strobe, D_{in} was a 0. In addition the MC145100 will reset all non-selected switches in the same row as the selected switch. Other switches are unaffected. In the MC145100, an internal power-on reset turns off all switches as power is applied.

- Internal Latches Control State of Switches
- Power-On Reset (MC145100 Only)
- Low On Resistance — Typically on 110 Ω @ 10 Vdc
- Large Analog Range (V_{DD}–V_{SS})
- All Pins are Diode Protected
- Matched Switch Characteristics
- High CMOS Noise Immunity
- MC142100 Pin-for-Pin Replacement for CD22100

NOT RECOMMENDED FOR NEW DESIGN



DW SUFFIX
SOG
CASE 751G

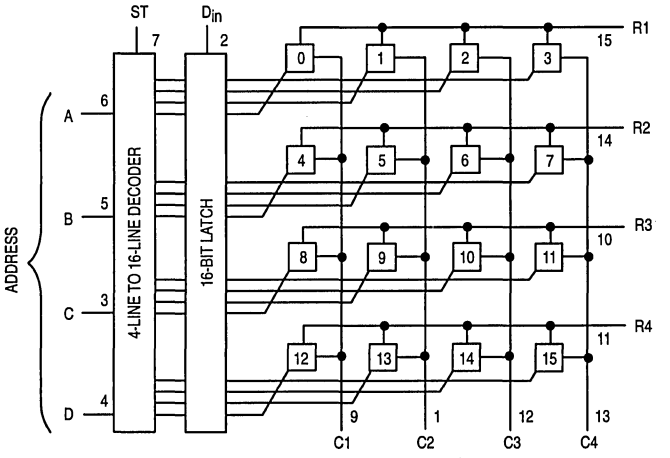


P SUFFIX
PLASTIC
CASE 648

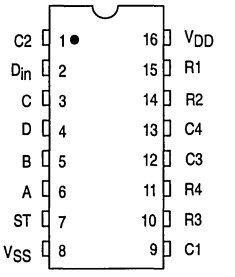
ORDERING INFORMATION

MC14XXXX	SUFFIX	DENOTES
	DW	SOG Package **MC142100 ONLY**
	P	Plastic DIP
	C	Limited Operating Temperature Range
	A	Extended Operating Temperature Range

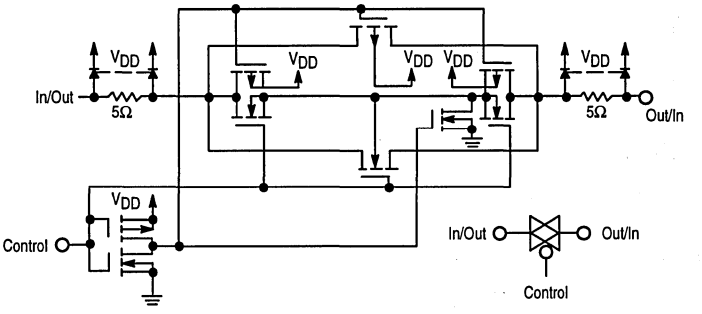
BLOCK DIAGRAM

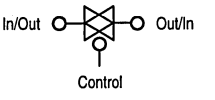


PIN ASSIGNMENTS



ANALOG TRANSMISSION GATE (CROSSPOINT) SCHEMATIC





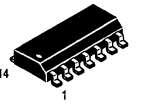
MC143403
MC143404

Quad Line Driver
CMOS

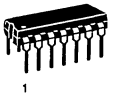
The MC143403 and MC143404 are low-power, quad line drivers with true differential inputs. The device has electrical characteristics similar to the popular LM324 and MC3403. However, the MC143403 has several distinct advantages over standard operational amplifier types. The low-power, quad line driver MC143403, draws only 1.5 mA (typ) and the micropower, quad line driver MC143404, draws only 400 µA (typ) and provides high output drive capabilities. The common mode rejection ratio is typically 60 dB.

These units are excellent building blocks for communications, consumer industrial and instrument applications where low power is required, particularly in telecommunications equipment. These units are useful in both battery operated communications systems and phone line powered equipment.

- Low-Power and Micropower Communication Devices
- True Differential Input Stage
- Single or Split Supply Operation
- High Input Impedance
- Very Low Input Bias Current: 1 nA
- Four Drivers per Package
- Pinout Compatible with LM324 and MC3403
- Wide Input Voltage Range
- High Output Current Drive, MC143403
- Typical Input Offset Voltage: 10 mV



D SUFFIX
SOG
CASE 751A



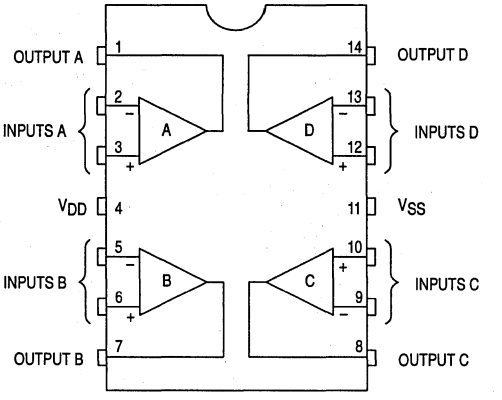
P SUFFIX
PLASTIC
CASE 646

ORDERING INFORMATION

MC14XXXX	SUFFIX	DENOTES
	P	Plastic DIP
	D	SOG Package

NOT RECOMMENDED
FOR NEW DESIGN

PIN ASSIGNMENT



MC145026
MC145027
MC145028
SC41343
SC41344

Encoder and Decoder Pairs
CMOS

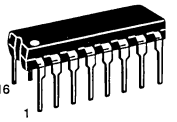
These devices are designed to be used as encoder/decoder pairs in remote control applications.

The MC145026 encodes nine lines of information and serially sends this information upon receipt of a transmit enable ($\overline{TE}$) signal. The nine lines may be encoded with trinary data (low, high, or open) or binary data (low or high). The words are transmitted twice per encoding sequence to increase security.

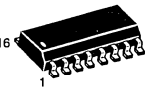
The MC145027 decoder receives the serial stream and interprets five of the trinary digits as an address code. Thus, 243 addresses are possible. If binary data is used at the encoder, 32 addresses are possible. The remaining serial information is interpreted as four bits of binary data. The valid transmission (VT) output goes high on the MC145027 when two conditions are met. First, two addresses must be consecutively received (in one encoding sequence) which both match the local address. Second, the 4 bits of data must match the last valid data received. The active VT indicates that the information at the Data output pins has been updated.

The MC145028 decoder treats all nine trinary digits as an address which allows 19,683 codes. If binary data is encoded, 512 codes are possible. The VT output goes high on the MC145028 when two addresses are consecutively received (in one encoding sequence) which both match the local address.

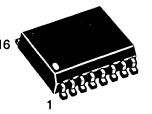
- Operating Temperature Range: −40 to +85°C
- Very-Low Standby Current for the Encoder: 300 nA Maximum @ 25°C
- Interfaces with RF, Ultrasonic, or Infrared Modulators and Demodulators
- RC Oscillator, No Crystal Required
- High External Component Tolerance; Can Use ±5% Components
- Internal Power-On Reset Forces All Decoder Outputs Low
- For Infrared Applications, See Applications Notes AN1016 and AN1126
- Operating Voltage Range: MC145026 = 2.5 to 18 V*
  MC145027, MC145028 = 4.5 to 18 V
- Low-Voltage Versions Available:
  SC41343 = 2.8 to 10 V Version of the MC145027
  SC41344 = 2.8 to 10 V Version of the MC145028



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG
CASE 751B

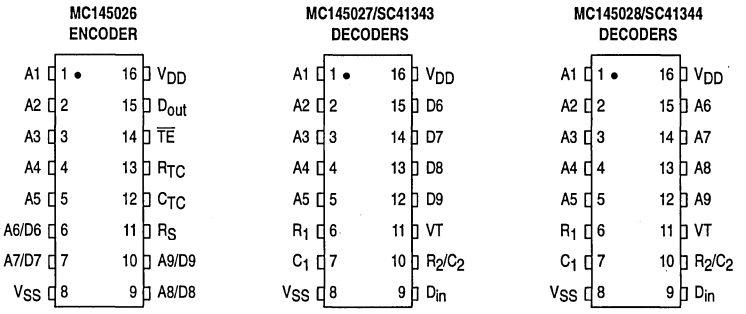


DW SUFFIX
SOG
CASE 751G

ORDERING INFORMATION

MC145026P	Plastic DIP
MC145026D	SOG
MC145027P, SC41343P	Plastic DIP
MC145027DW, SC41343DW	SOG
MC145028P, SC41344P	Plastic DIP
MC145028DW, SC41344DW	SOG

PIN ASSIGNMENTS



* All MC145026 devices manufactured after date code 9314 or 314 are guaranteed over this wider voltage range. All previous designs using the low-voltage SC41342 should convert to the MC145026, which is a drop-in replacement. The SC41342 part number will be discontinued.

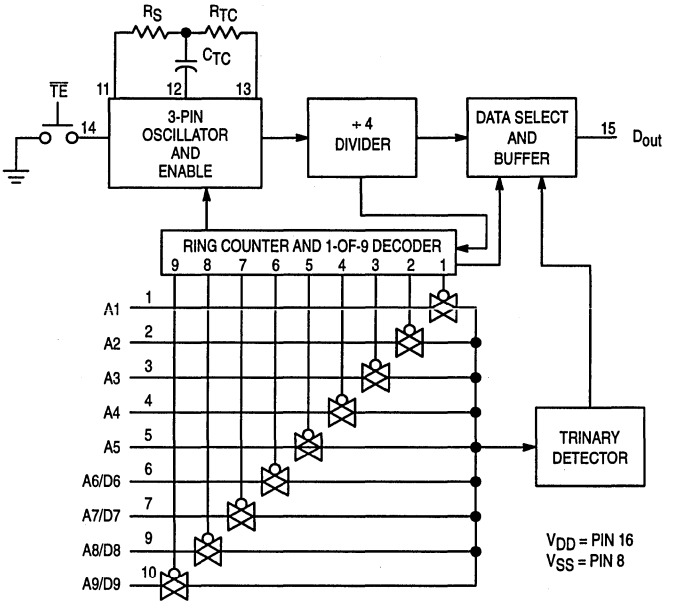


Figure 1. MC145026 Encoder Block Diagram

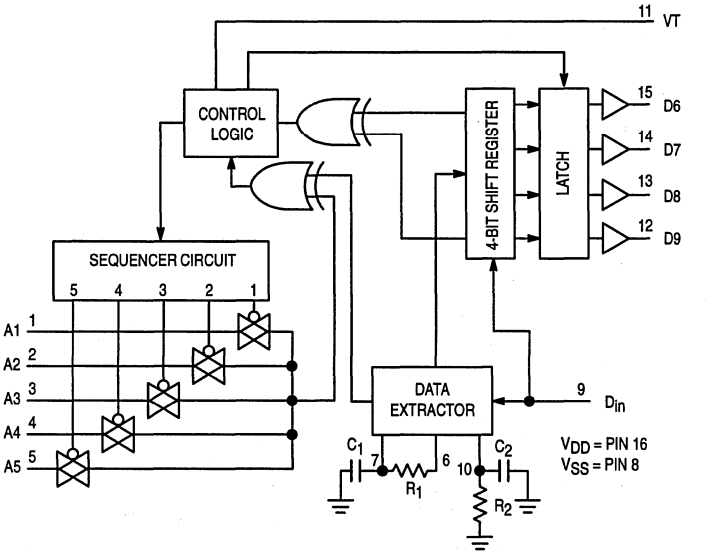


Figure 2. MC145027 Decoder Block Diagram

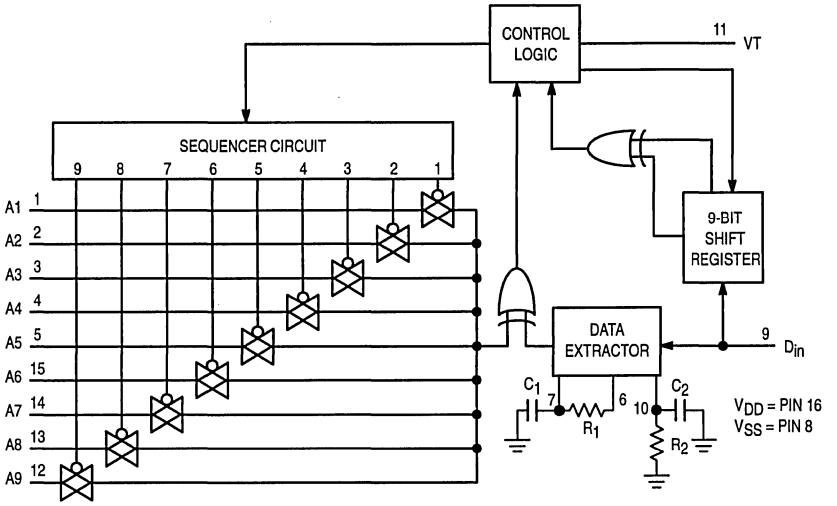


Figure 3. MC145028 Decoder Block Diagram

MAXIMUM RATINGS* (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (except SC41343, SC41344)	−0.5 to +18	V
V_{DD}	DC Supply Voltage (SC41343, SC41344 only)	−0.5 to +10	V
V_{in}	DC Input Voltage	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD} +0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±10	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS — MC145026*, MC145027, and MC145028 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			−40°C		25°C		+85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low-Level Output Voltage (V_{in} = V_{DD} or 0)	5.0	—	0.05	—	0.05	—	0.05	V
		10	—	0.05	—	0.05	—	0.05	
		15	—	0.05	—	0.05	—	0.05	
V_{OH}	High-Level Output Voltage (V_{in} = 0 or V_{DD})	5.0	4.95	—	4.95	—	4.95	—	V
		10	9.95	—	9.95	—	9.95	—	
		15	14.95	—	14.95	—	14.95	—	
V_{IL}	Low-Level Input Voltage								V
	(V_{out} = 4.5 or 0.5 V)	5.0	—	1.5	—	1.5	—	1.5	
	(V_{out} = 9.0 or 1.0 V)	10	—	3.0	—	3.0	—	3.0	
	(V_{out} = 13.5 or 1.5 V)	15	—	4.0	—	4.0	—	4.0	
V_{IH}	High-Level Input Voltage								V
	(V_{out} = 0.5 or 4.5 V)	5.0	3.5	—	3.5	—	3.5	—	
	(V_{out} = 1.0 or 9.0 V)	10	7.0	—	7.0	—	7.0	—	
	(V_{out} = 1.5 or 13.5 V)	15	11	—	11	—	11	—	
I_{OH}	High-Level Output Current								mA
	(V_{out} = 2.5 V)	5.0	−2.5	—	−2.1	—	−1.7	—	
	(V_{out} = 4.6 V)	5.0	−0.52	—	−0.44	—	−0.36	—	
	(V_{out} = 9.5 V)	10	−1.3	—	−1.1	—	−0.9	—	
	(V_{out} = 13.5 V)	15	−3.6	—	−3.0	—	−2.4	—	
I_{OL}	Low-Level Output Current								mA
	(V_{out} = 0.4 V)	5.0	0.52	—	0.44	—	0.36	—	
	(V_{out} = 0.5 V)	10	1.3	—	1.1	—	0.9	—	
	(V_{out} = 1.5 V)	15	3.6	—	3.0	—	2.4	—	
I_{in}	Input Current — $\overline{TE}$	5.0	—	—	3.0	11	—	—	µA
	(MC145026, Pull-up Device)	10	—	—	16	60	—	—	
		15	—	—	35	120	—	—	
I_{in}	Input Current	15	—	±0.3	—	±0.3	—	±1.0	µA
	R_S (MC145026), D_{in} (MC145027, MC145028)								
I_{in}	Input Current								µA
	A1–A5, A6/D6–A9/D9 (MC145026),	5.0	—	—	—	±110	—	—	
	A1–A5 (MC145027),	10	—	—	—	±500	—	—	
	A1–A9 (MC145028)	15	—	—	—	±1000	—	—	
C_{in}	Input Capacitance (V_{in} = 0)	—	—	—	—	7.5	—	—	pF
I_{DD}	Quiescent Current — MC145026	5.0	—	—	—	0.1	—	—	µA
		10	—	—	—	0.2	—	—	
		15	—	—	—	0.3	—	—	
I_{DD}	Quiescent Current — MC145027, MC145028	5.0	—	—	—	50	—	—	µA
		10	—	—	—	100	—	—	
		15	—	—	—	150	—	—	
I_{dd}	Dynamic Supply Current — MC145026 (f_c = 20 kHz)	5.0	—	—	—	200	—	—	µA
		10	—	—	—	400	—	—	
		15	—	—	—	600	—	—	
I_{dd}	Dynamic Supply Current — MC145027, MC145028	5.0	—	—	—	400	—	—	µA
	(f_c = 20 kHz)	10	—	—	—	800	—	—	
		15	—	—	—	1200	—	—	

*Also see next Electrical Characteristics table for 2.5 V specifications.

ELECTRICAL CHARACTERISTICS — MC145026 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			−40°C		25°C		+85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low-Level Output Voltage (V_{in} = 0 V or V_{DD})	2.5	—	0.05	—	0.05	—	0.05	V
V_{OH}	High-Level Output Voltage (V_{in} = 0 V or V_{DD})	2.5	2.45	—	2.45	—	2.45	—	V
V_{IL}	Low-Level Input Voltage (V_{out} = 0.5 V or 2.0 V)	2.5	—	0.3	—	0.3	—	0.3	V
V_{IH}	High-Level Input Voltage (V_{out} = 0.5 V or 2.0 V)	2.5	2.2	—	2.2	—	2.2	—	V
I_{OH}	High-Level Output Current (V_{out} = 1.25 V)	2.5	0.28	—	0.25	—	0.2	—	mA
I_{OL}	Low-Level Output Current (V_{out} = 0.4 V)	2.5	0.22	—	0.2	—	0.16	—	mA
I_{in}	Input Current ($\overline{TE}$ — Pull-Up Device)	2.5	—	—	0.09	1.8	—	—	µA
I_{in}	Input Current (A1–A5, A6/D6–A9/D9)	2.5	—	—	—	±25	—	—	µA
I_{DD}	Quiescent Current	2.5	—	—	—	0.05	—	—	µA
I_{dd}	Dynamic Supply Current (f_c = 20 kHz)	2.5	—	—	—	40	—	—	µA

ELECTRICAL CHARACTERISTICS — SC41343 and SC41344 (Voltage Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	Guaranteed Limit						Unit
			−40°C		25°C		+85°C		
			Min	Max	Min	Max	Min	Max	
V_{OL}	Low-Level Output Voltage (V_{in} = 0 V or V_{DD})	2.8	—	0.05	—	0.05	—	0.05	V
		5.0	—	0.05	—	0.05	—	0.05	
		10	—	0.05	—	0.05	—	0.05	
V_{OH}	High-Level Output Voltage (V_{in} = 0 V or V_{DD})	2.8	2.75	—	2.75	—	2.75	—	V
		5.0	4.95	—	4.95	—	4.95	—	
		10	9.95	—	9.95	—	9.95	—	
V_{IL}	Low-Level Input Voltage								V
	(V_{out} = 2.3 V or 0.5 V)	2.8	—	0.84	—	0.84	—	0.84	
	(V_{out} = 4.5 V or 0.5 V)	5.0	—	1.5	—	1.5	—	1.5	
	(V_{out} = 9.0 V or 1.0 V)	10	—	3.0	—	3.0	—	3.0	
V_{IH}	High-Level Input Voltage								V
	(V_{out} = 0.5 V or 2.3 V)	2.8	1.96	—	1.96	—	1.96	—	
	(V_{out} = 0.5 V or 4.5 V)	5.0	3.5	—	3.5	—	3.5	—	
	(V_{out} = 1.0 V or 9.0 V)	10	7.0	—	7.0	—	7.0	—	
I_{OH}	High-Level Output Current								mA
	(V_{out} = 1.4 V)	2.8	−0.73	—	−0.7	—	−0.55	—	
	(V_{out} = 4.5 V)	5.0	−0.59	—	−0.5	—	−0.41	—	
	(V_{out} = 9.0 V)	10	−1.3	—	−1.1	—	−0.9	—	
I_{OL}	Low-Level Output Current								mA
	(V_{out} = 0.4 V)	2.8	0.35	—	0.3	—	0.24	—	
	(V_{out} = 0.5 V)	5.0	0.8	—	0.6	—	0.4	—	
	(V_{out} = 1.0 V)	10	3.5	—	2.9	—	2.3	—	
I_{in}	Input Current — D_{in}	10	—	±0.3	—	±0.3	—	±1.0	µA
I_{in}	Input Current	2.8	—	—	—	±30	—	—	µA
	A1–A5 (SC41343)	5.0	—	—	—	±140	—	—	
	A1–A9 (SC41344)	10	—	—	—	±600	—	—	
C_{in}	Input Capacitance (V_{in} = 0)	—	—	—	—	7.5	—	—	pF
I_{DD}	Quiescent Current	2.8	—	—	—	60	—	—	µA
		5.0	—	—	—	75	—	—	
		10	—	—	—	150	—	—	
I_{dd}	Dynamic Supply Current (f_c = 20 kHz)	2.8	—	—	—	300	—	—	µA
		5.0	—	—	—	500	—	—	
		10	—	—	—	1000	—	—	

SWITCHING CHARACTERISTICS — MC145026*, MC145027, and MC145028 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure #	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4, 8	5.0 10 15	— — —	200 100 80	ns
t_r	D_{in} Rise Time — Decoders	5	5.0 10 15	— — —	15 15 15	µs
t_f	D_{in} Fall Time — Decoders	5	5.0 10 15	— — —	15 5.0 4.0	µs
f_{osc}	Encoder Clock Frequency	6	5.0 10 15	0.001 0.001 0.001	2.0 5.0 10	MHz
f	Decoder Frequency — Referenced to Encoder Clock	12	5.0 10 15	1.0 1.0 1.0	240 410 450	kHz
t_W	$\overline{TE}$ Pulse Width — Encoders	7	5.0 10 15	65 30 20	— — —	ns

*Also see next Switching Characteristics table for 2.5 V specifications.

SWITCHING CHARACTERISTICS — MC145026 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure #	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4, 8	2.5	—	450	ns
f_{osc}	Encoder Clock Frequency	6	2.5	1.0	250	kHz
t_W	$\overline{TE}$ Pulse Width	7	2.5	1.5	—	µs

SWITCHING CHARACTERISTICS — SC41343 and SC41344 (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	Figure #	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}, t_{THL}	Output Transition Time	4, 8	2.8 5.0 10	— — —	320 200 100	ns
t_r	D_{in} Rise Time	5	2.8 5.0 10	— — —	15 15 15	µs
t_f	D_{in} Fall Time	5	2.8 5.0 10	— — —	15 15 5.0	µs
f	Decoder Frequency — Referenced to Encoder Clock	12	2.8 5.0 10	1.0 1.0 1.0	100 240 410	kHz

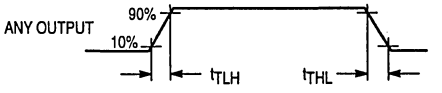


Figure 4.

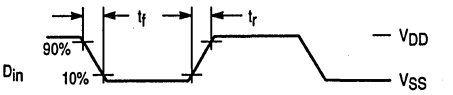


Figure 5.

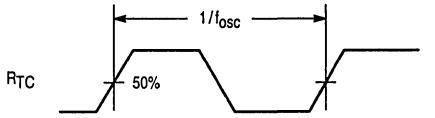


Figure 6.

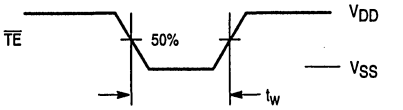
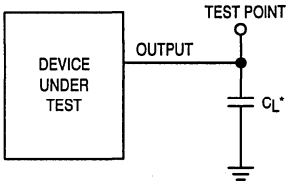


Figure 7.



*INCLUDES ALL PROBE AND JIG CAPACITANCE.

Figure 8. Test Circuit

OPERATING CHARACTERISTICS

MC145026

The encoder serially transmits trinary data as defined by the state of the A1–A5 and A6/D6–A9/D9 input pins. These pins may be in either of three states (low, high, or open) allowing 19,683 possible codes. The transmit sequence is initiated by a low level on the $\overline{TE}$ input pin. Upon power up, the MC145026 can continuously transmit as long as $\overline{TE}$ remains low (also, the device can transmit two-word sequences by pulsing $\overline{TE}$ low). However, no MC145026 application should be designed to rely upon the first data word transmitted immediately after power up because this word may be invalid. Between the two data words, no signal is sent for three data periods (see Figure 10).

Each transmitted trinary digit is encoded into pulses (see Figure 11). A logic 0 (low) is encoded as two consecutive short pulses, a logic 1 (high) as two consecutive long pulses, and an open (high impedance) as a long pulse followed by a short pulse. The input state is determined by using a weak "output" device to try to force each input high then low. If only a high state results from the two tests, the input is assumed to be hardwired to V_{DD}. If only a low state is obtained, the input is assumed to be hardwired to V_{SS}. If both a high and a low can be forced at an input, an open is assumed and is encoded as such. The "high" and "low" levels are 70% and 30% of the supply voltage as shown in the Electrical Characteristics Table. The weak "output" device sinks/sources up to 110 µA at a 5-V supply level, 500 µA at 10 V, and 1 mA at 15 V.

The $\overline{TE}$ input has an internal pull-up device so that a simple switch may be used to force the input low. While $\overline{TE}$ is high, the encoder is completely disabled, the oscillator is inhibited, and the current drain is reduced to quiescent current. When $\overline{TE}$ is brought low, the oscillator is started and the transmit sequence begins. The inputs are then sequentially selected, and determinations are made as to the input logic states. This information is serially transmitted via the D_{out} pin.

MC145027

This decoder receives the serial data from the encoder and outputs the data, if it is valid. The transmitted data, consisting of two identical words, is examined bit by bit during reception. The first five trinary digits are assumed to be the address. If the received address matches the local address, the next four (data) bits are internally stored, but are not transferred to the output data latch. As the second encoded word is received, the address must again match. If a match occurs, the new data bits are checked against the previously stored data bits. If the two nibbles of data (four bits each) match, the data is transferred to the output data latch by VT and remains until new data replaces it. At the same time, the VT output pin is brought high and remains high until an error is received or until no input signal is received for four data periods (see Figure 10).

Although the address information may be encoded in trinary, the data information must be either a 1 or 0. A trinary (open) data line is decoded as a logic 1.

MC145028

This decoder operates in the same manner as the MC145027 except that nine address lines are used and no data output is available. The VT output is used to indicate that a valid address has been received. For transmission security, two identical transmitted words must be consecutively received before a VT output signal is issued.

The MC145028 allows 19,683 addresses when trinary levels are used. 512 addresses are possible when binary levels are used.

PIN DESCRIPTIONS

MC145026 ENCODER

A1–A5, A6/D6–A9/D9
Address, Address/Data Inputs (Pins 1–7, 9, and 10)

These address/data inputs are encoded and the data is sent serially from the encoder via the D_{out} pin.

R_S, C_{TC}, R_{TC}
(Pins 11, 12, and 13)

These pins are part of the oscillator section of the encoder (see Figure 9).

If an external signal source is used instead of the internal oscillator, it should be connected to the R_S input and the R_{TC} and C_{TC} pins should be left open.

$\overline{TE}$
Transmit Enable (Pin 14)

This active-low transmit enable input initiates transmission when forced low. An internal pull-up device keeps this input normally high. The pull-up current is specified in the Electrical Characteristics table.

D_{out}
Data Out (Pin 15)

This is the output of the encoder that serially presents the encoded data word.

V_{SS}
Negative Power Supply (Pin 8)

The most-negative supply potential. This pin is usually ground.

V_{DD}
Positive Power Supply (Pin 16)

The most-positive power supply pin.

MC145027 AND MC145028 DECODERS

A1–A5, A1–A9
Address Inputs (Pins 1–5) — MC145027,
Address Inputs (Pins 1–5, 15, 14, 13, 12) — MC145028

These are the local address inputs. The states of these pins must match the appropriate encoder inputs for the VT pin to go high. The local address may be encoded with trinary or binary data.

D6–D9
Data Outputs (Pins 15, 14, 13, 12) — MC145027 ONLY

These outputs present the binary information that is on encoder inputs A6/D6 through A9/D9. Only binary data is acknowledged; a trinary open at the MC145026 encoder is decoded as a high level (logic 1).

D_{in}
Data In (Pin 9)

This pin is the serial data input to the decoder. The input voltage must be at CMOS logic levels. The signal source driving this pin must be dc coupled.

R_1, C_1
Resistor 1, Capacitor 1 (Pins 6, 7)

As shown in Figures 2 and 3, these pins accept a resistor and capacitor that are used to determine whether a narrow pulse or wide pulse has been received. The time constant $R_1 \times C_1$ should be set to 1.72 encoder clock periods:

$$R_1 C_1 = 3.95 R_{TC} C_{TC}$$

R_2/C_2
Resistor 2/Capacitor 2 (Pin 10)

As shown in Figures 2 and 3, this pin accepts a resistor and capacitor that are used to detect both the end of a received word and the end of a transmission. The time constant $R_2 \times C_2$ should be 33.5 encoder clock periods (four data periods per Figure 11): $R_2 C_2 = 77 R_{TC} C_{TC}$. This time constant is used to determine whether the D_{in} pin has remained low for four data periods (end of transmission). A separate on-chip comparator looks at the voltage-equivalent two data periods ($0.4 R_2 C_2$) to detect the dead time between received words within a transmission.

VT
Valid Transmission Output (Pin 11)

This valid transmission output goes high after the second word of an encoding sequence when the following conditions are satisfied:

1. the received addresses of both words match the local decoder address, and
2. the received data bits of both words match

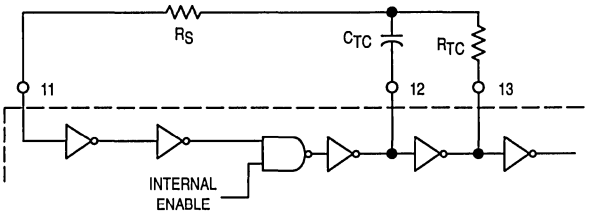
VT remains high until either a mismatch is received or no input signal is received for four data periods.

V_{SS}
Negative Power Supply (Pin 8)

The most-negative supply potential. This pin is usually ground.

V_{DD}
Positive Power Supply (Pin 16)

The most-positive power supply pin.



This oscillator operates at a frequency determined by the external RC network; i.e.,

$$f \approx \frac{1}{2.3\ R_{TC}\ C_{TC'}} \text{ (Hz)}$$

for 1 kHz ≤ f ≤ 400 kHz

where: $C_{TC'} = C_{TC} + C_{layout} + 12$ pF

$R_S \approx 2\ R_{TC}$

$R_S \geq 20$ k

$R_{TC} \geq 10$ k

400 pF < C_{TC} < 15 µF

The value for R_S should be chosen to be ≥ 2 times R_{TC}. This range ensures that current through R_S is insignificant compared to current through R_{TC}. The upper limit for R_S must ensure that R_S x 5 pF (input capacitance) is small compared to R_{TC} x C_{TC}.

For frequencies outside the indicated range, the formula is less accurate. The minimum recommended oscillation frequency of this circuit is 1 kHz. Susceptibility to externally induced noise signals may occur for frequencies below 1 kHz and/or when resistors utilized are greater than 1 MΩ.

Figure 9. Encoder Oscillator Information

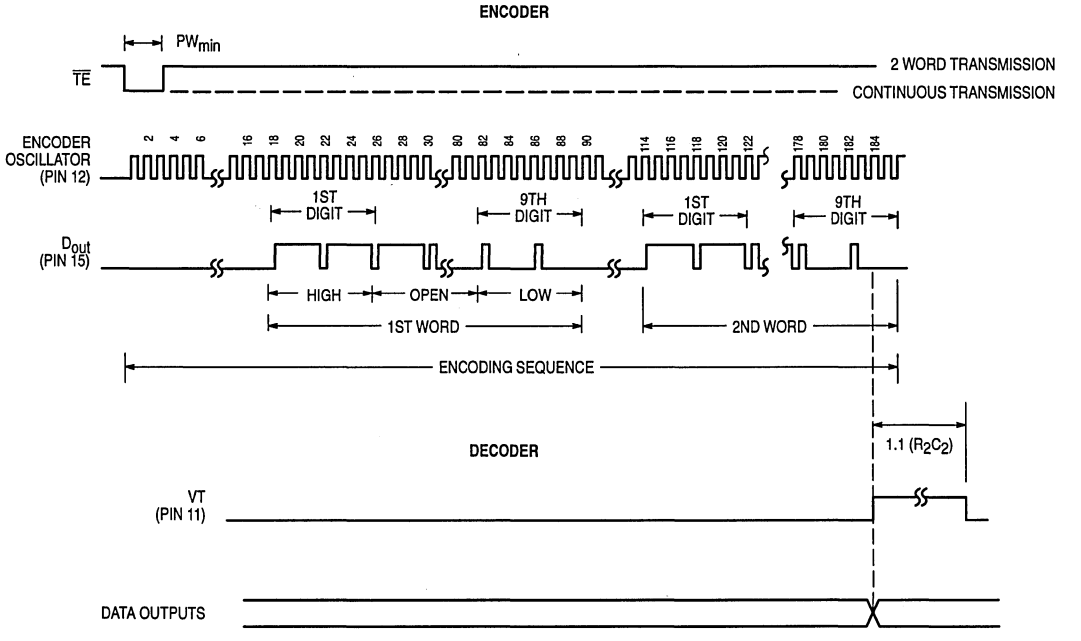


Figure 10. Timing Diagram

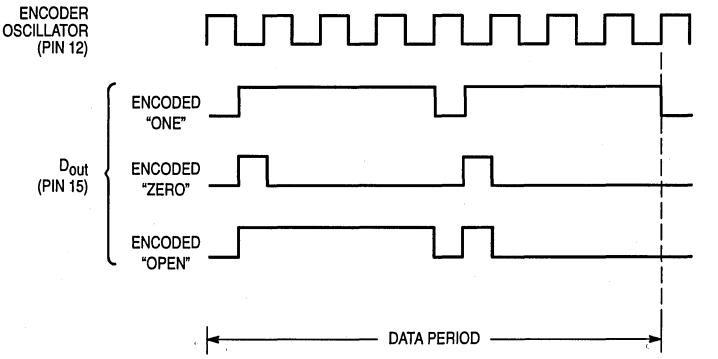


Figure 11. Encoder Data Waveforms

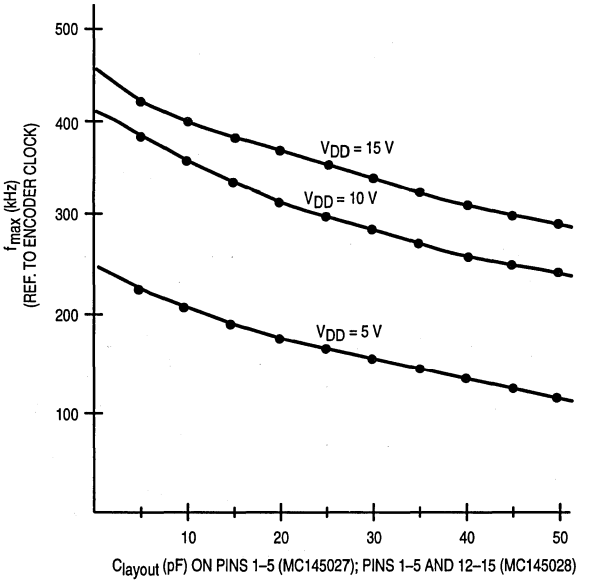


Figure 12. f_{max} vs C_{layout} — Decoders Only

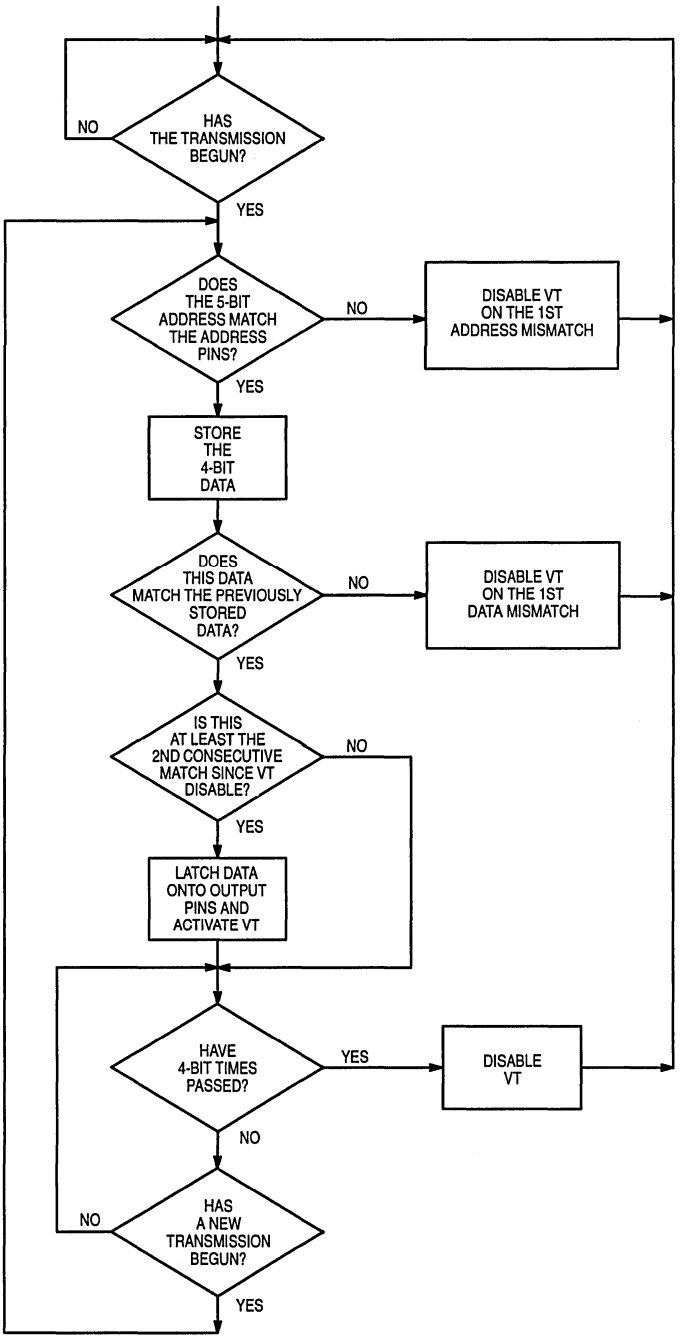


Figure 13. MC145027 Flowchart

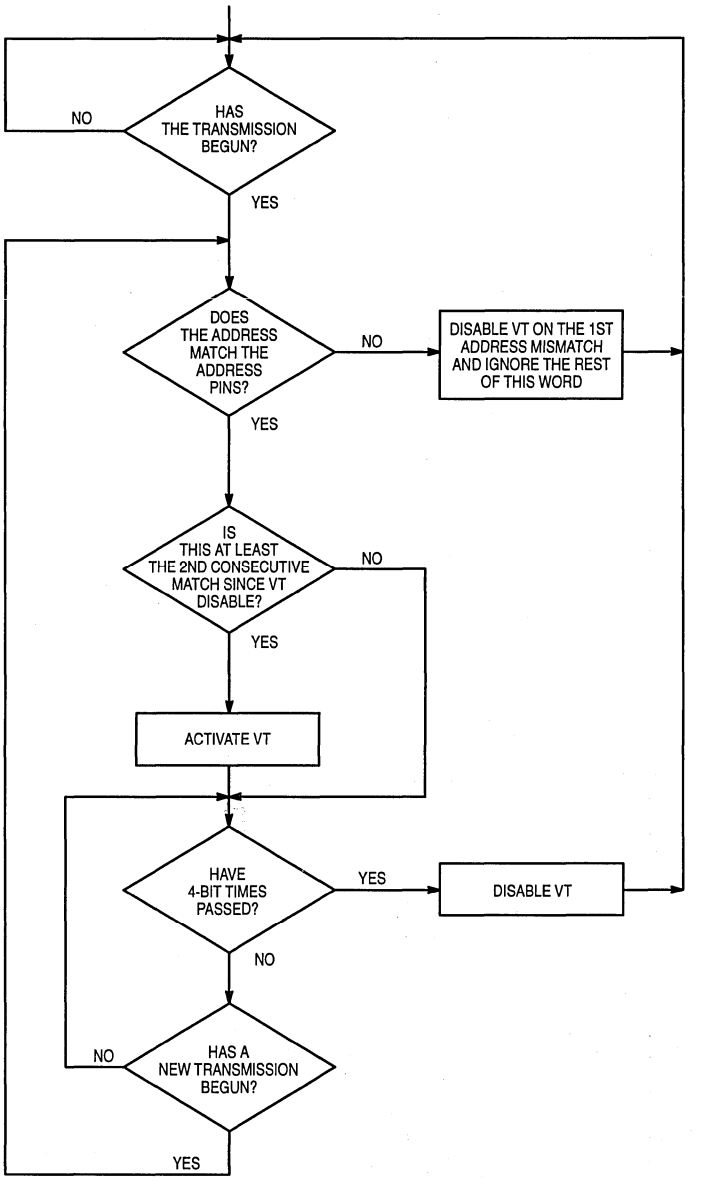


Figure 14. MC145028 Flowchart

MC145027 AND MC145028 TIMING

To verify the MC145027 or MC145028 timing, check the waveforms on C1 (Pin 7) and R2/C2 (Pin 10) as compared to the incoming data waveform on D_{in} (Pin 9).

The R-C decay seen on C1 discharges down to 1/3 V_{DD} before being reset to V_{DD}. This point of reset (labelled "DOS" in Figure 15) is the point in time where the decision is made whether the data seen on D_{in} is a 1 or 0. DOS should not be too close to the D_{in} data edges or intermittent operation may occur.

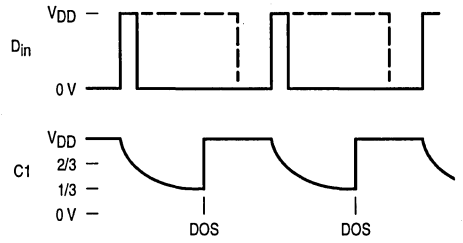


Figure 15. R-C Decay on Pin 7 (C1)

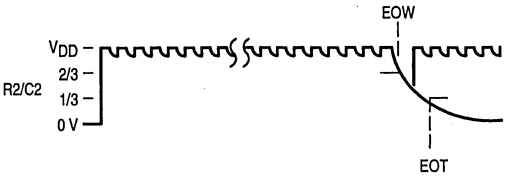
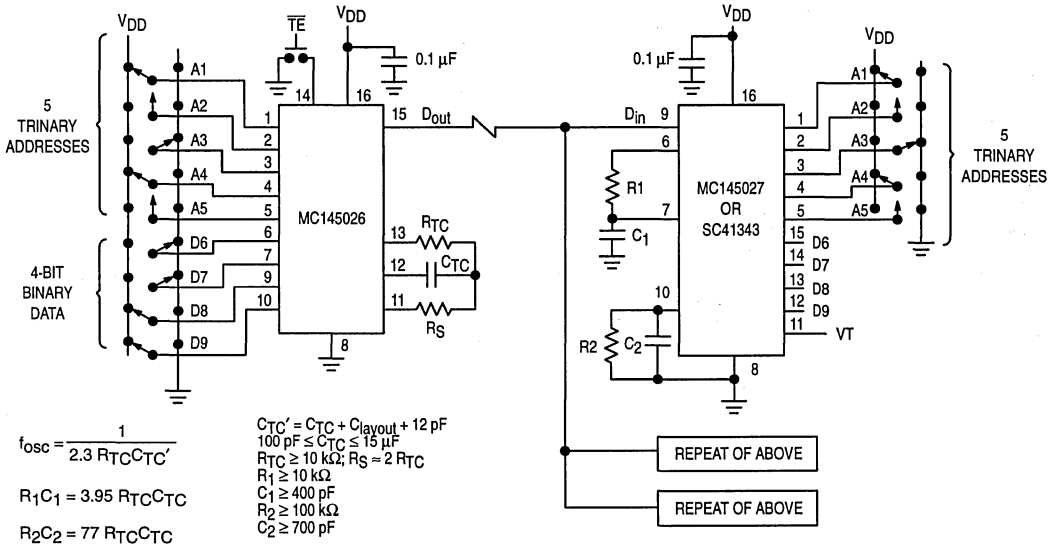


Figure 16. R-C Decay on Pin 10 (R2/C2)

The other timing to be checked on the MC145027 and MC145028 is on R2/C2 (see Figure 16). The R-C decay is continually reset to V_{DD} as data is being transmitted. Only between words and after the end-of-transmission (EOT) does R2/C2 decay significantly from V_{DD}. R2/C2 can be used to identify the internal end-of-word (EOW) timing edge which is generated when R2/C2 decays to 2/3 V_{DD}. The internal EOT timing edge occurs when R2/C2 decays to 1/3 V_{DD}. When the waveform is being observed, the R-C decay should go down between the 2/3 and 1/3 V_{DD} levels, but not too close to either level before data transmission on D_{in} resumes.

Verification of the timing described above should insure a good match between the MC145026 transmitter and the MC145027 and MC145028 receivers.



$$f_{osc} = \frac{1}{2.3\ R_{TC}C_{TC}'}$$

$R_1C_1 = 3.95\ R_{TC}C_{TC}$

$R_2C_2 = 77\ R_{TC}C_{TC}$

$C_{TC}' = C_{TC} + C_{layout} + 12$ pF
100 pF ≤ C_{TC} ≤ 15 µF
R_{TC} ≥ 10 kΩ; $R_S \approx 2\ R_{TC}$
R_1 ≥ 10 kΩ
C_1 ≥ 400 pF
R_2 ≥ 100 kΩ
C_2 ≥ 700 pF

Example R/C Values (All Resistors and Capacitors are ±5%)

($C_{TC}' = C_{TC}$ + 20 pF)

f_{osc} (kHz)	R_{TC}	C_{TC}'	R_S	R_1	C_1	R_2	C_2
362	10 k	120 pF	20 k	10 k	470 pF	100 k	910 pF
181	10 k	240 pF	20 k	10 k	910 pF	100 k	1800 pF
88.7	10 k	490 pF	20 k	10 k	2000 pF	100 k	3900 pF
42.6	10 k	1020 pF	20 k	10 k	3900 pF	100 k	7500 pF
21.5	10 k	2020 pF	20 k	10 k	8200 pF	100 k	0.015 µF
8.53	10 k	5100 pF	20 k	10 k	0.02 µF	200 k	0.02 µF
1.71	50 k	5100 pF	100 k	50 k	0.02 µF	200 k	0.1 µF

Figure 17. Typical Application

APPLICATIONS INFORMATION

INFRARED TRANSMITTER

In Figure 18, the MC145026 encoder is set to run at an oscillator frequency of about 4 to 9 kHz. Thus, the time required for a complete two-word encoding sequence is about 20 to 40 ms. The data output from the encoder gates an RC oscillator running at 50 kHz; the oscillator shown starts rapidly enough to be used in this application. When the "send" button is not depressed, both the MC145026 and oscillator are in a low-power standby state. The RC oscillator has to be trimmed for 50 kHz and has some drawbacks for frequency stability. A superior system uses a ceramic resonator oscillator running at 400 kHz. This oscillator feeds a divider as shown in Figure 19. The unused inputs of the MC14011UB must be grounded.

The MLED81 IRED is driven with the 50-kHz square wave at about 200 to 300 mA to generate the carrier. If desired, two IREDs wired in series can be used (see Application Note AN1016 for more information). The bipolar IRED switch, shown in Figure 18, offers two advantages over a FET. First, a logic FET has too much gate capacitance for the MC14011UB to drive without waveform distortion. Second, the bipolar drive permits lower supply voltages, which are an advantage in portable battery-powered applications.

The configuration shown in Figure 18 operates over a supply range of 4.5 to 18 V. A low-voltage system which operates down to 2.5 V could be realized if the oscillator section of a MC74HC4060 is used in place of the MC14011UB. The data output of the MC145026 is inverted and fed to the RESET pin of the MC74HC4060. Alternately, the MC74HCU04 could be used for the oscillator.

Information on the MC14011UB is in book number DL131/D. The MC74HCU04 and MC74HC4060 are found in book number DL129/D.

INFRARED RECEIVER

The receiver in Figure 20 couples an IR-sensitive diode to input preamp A1, followed by band-pass amplifier A2 with a gain of about 10. Limiting stage A3 follows, with an output of about 800 mVp-p. The limited 50 kHz burst is detected by comparator A4 that passes only positive pulses, and peak-detected and filtered by a diode/RC network to extract the data envelope from the burst. Comparator A5 boosts the signal to logic levels compatible with the MC145027/28 data input. The D_{in} pin of these decoders is a standard CMOS high-impedance input which must ***not*** be allowed to float. Therefore, direct coupling from A5 to the decoder input is utilized.

Shielding should be used on at least A1 and A2, with good ground and high-sensitivity circuit layout techniques applied.

For operation with supplies higher than +5 V, limiter A4's positive output swing needs to be limited to 3 to 5 V. This is accomplished via adding a zener diode in the negative feedback path, thus avoiding excessive system noise. The biasing resistor stack should be adjusted such that V3 is 1.25 to 1.5 V.

This system works up to a range of about 10 meters. The gains of the system may be adjusted to suit the individual design needs. The 100 Ω resistor in the emitter of the first 2N5088 and the 1 kΩ resistor feeding A2 may be altered if different gain is required. In general, more gain does not necessarily result in increased range. This is due to noise floor limitations. The designer should increase transmitter power and/or increase receiver aperature with fresnal lensing to greatly improve range. See applications note AN1016 for additional information.

Information on the MC34074 is in data book DL128/D.

TRINARY SWITCH MANUFACTURERS

Midland Ross–Electronic Connector Div.
617/491-5400
Greyhill
312/354-1040
Augat/Alcoswitch
617/685-4371
Aries Electronics
201/996-6841

The above companies may not have the switches in a DIP. For more info, call them or consult EEM or Gold Book. ***Ask for SPDT with center OFF.***

Alternative: A SPST can be placed in series between a SPDT and the Encoder or Decoder to achieve trinary action.

Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of trinary switch manufacturers.

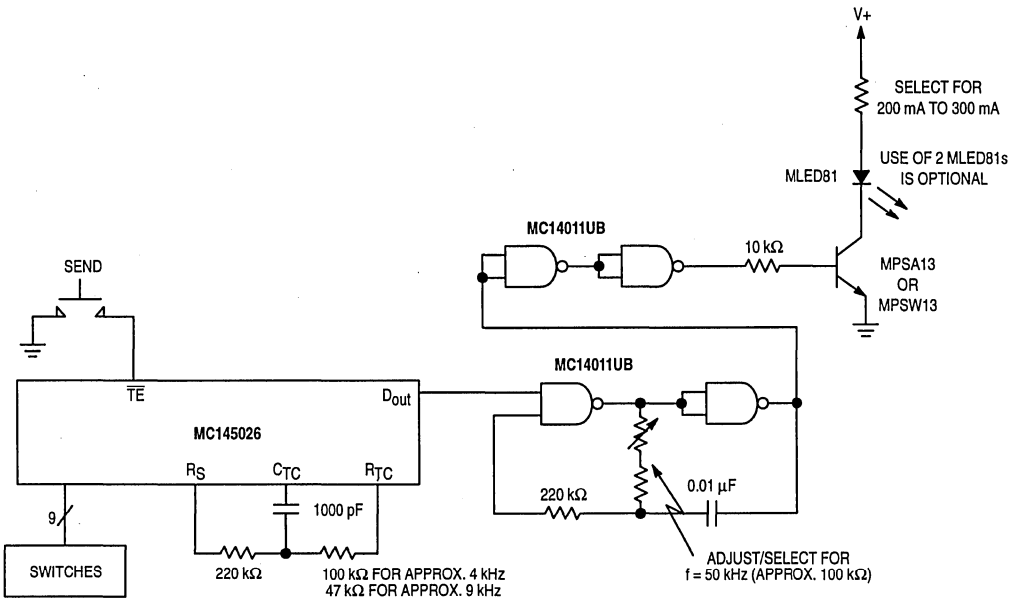


Figure 18. IRED Transmitter Using RC Oscillator to Generate Carrier Frequency

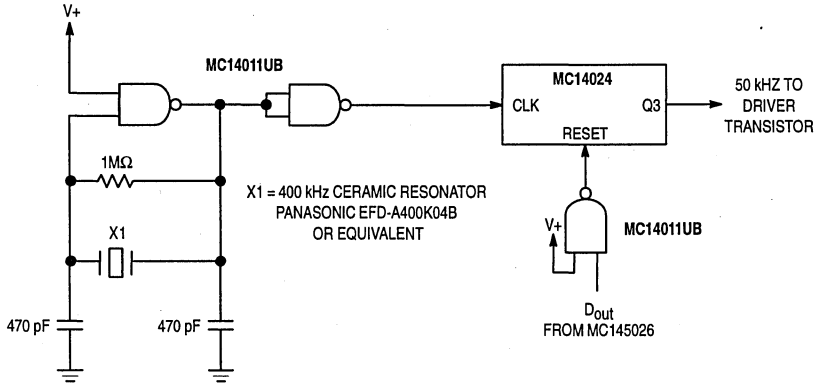


Figure 19. Using a Ceramic Resonator to Generate Carrier Frequency

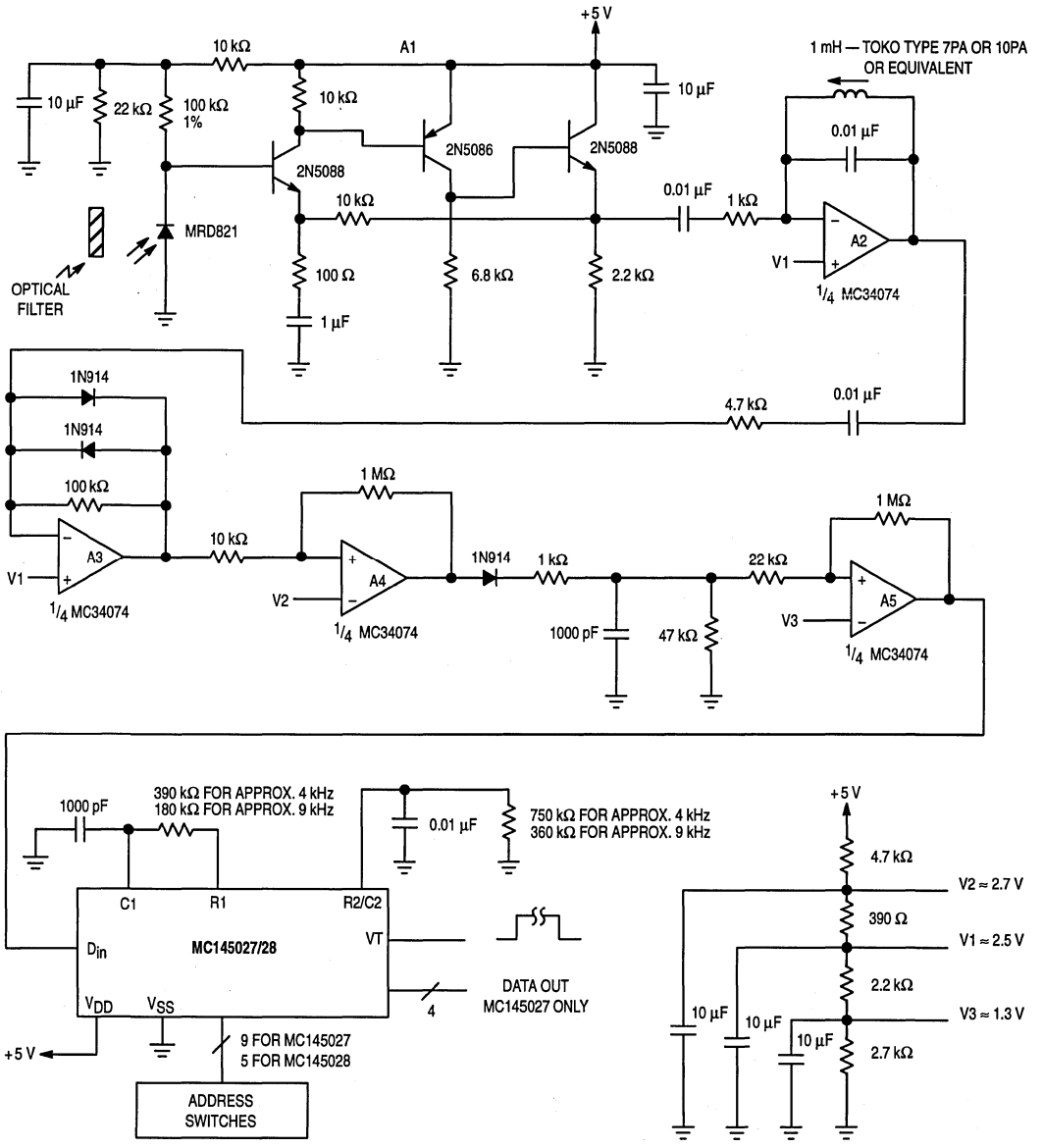


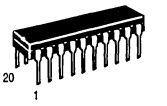
Figure 20. Infrared Receiver

MC145030

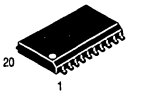
Advance Information

Remote Control Encoder/ Decoder

CMOS



P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG
CASE 751D

ORDERING INFORMATION

MC145030P	Plastic DIP
MC145030DW	SOG Package

The MC145030 encodes and decodes nine bits of information, which allows 512 different codes.

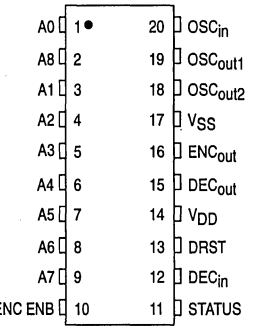
The encoder section samples the 9-bit parallel address input, encodes the bits into Manchester Code, and sends the serial information via the ENC_{out} pin. The address is issued twice per encoding sequence; initialization occurs with a rising edge on ENC ENB.

The decoder accepts serial information at the DEC_{in} pin, and decodes the Manchester information. The decoded address is compared with the local address. If a match occurs, DEC_{out} toggles once per sequence. The active-high DRST input is used to clear DEC_{out}.

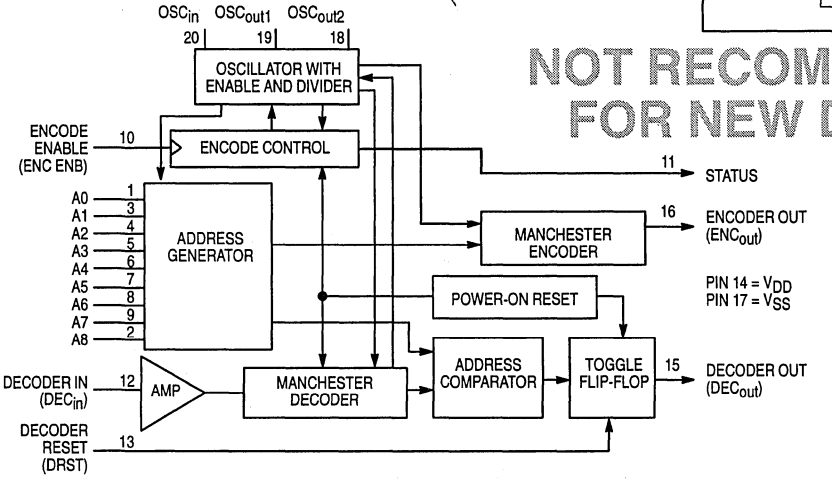
The Status pin, when high, indicates the device is encoding. During decoding or standby, Status is low.

- Applications:
  Cordless Phones and Half-Duplex Remote Control
- Interfaces with RF, Ultrasonic, or Infrared Modulators and Demodulators
- Operating Temperature Range: – 40 to 85°C
- Operating Voltage Range: 2 to 6 V
- Standby Supply Current: 20 µA Maximum @ 2.0 V
- Operating Supply Current: 700 µA Maximum @ 2.5 V
- Address Inputs Have On-Chip Pull-Up Devices
- RC Oscillator, No Crystal Required
- On-Chip Amplifier in Decode Section
- Power-On Reset Forces DEC_{out} Low and Initializes the Decoder and Encoder Sections
- See Application Notes AN1016 and AN1126 and Article Reprint AR255

PIN ASSIGMENT



BLOCK DIAGRAM



NOT RECOMMENDED FOR NEW DESIGN

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to V_{DD} + 0.5	V
V_{out}	DC Output Voltage	– 0.5 to V_{DD} + 0.5	V
I_{in}	DC Input Current, per Pin	± 10	mA
I_{out}	DC Output Current, per Pin	± 10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (10-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

† Power Dissipation Temperature Derating: – 12 mW/°C from 65 to 85°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Except for the Address Inputs, unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). The Address inputs may be left open; see Pin Descriptions. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	2.0 to 6.0	V
V_{IL}	Maximum Low-Level Input Voltage (Except DEC_{in})		2.5 6.0	0.3 1.2	V
V_{IH}	Minimum High-Level Input Voltage (Except DEC_{in})		2.5 6.0	1.9 4.5	V
V_{sig}	Minimum Output Voltage of Signal Source Driving DEC_{in}	Square-Wave Source See Figure 1	2.5 6.0	200 200	mV_{p-p}
V_{OL}	Maximum Low-Level Output Voltage	I_{out} = 0 µA I_{out} = 0.4 mA	2.5	0.15 0.4	V
		I_{out} = 0 µA I_{out} = 1.0 mA	6.0	0.15 0.4	
V_{OH}	Minimum High-Level Output Voltage	I_{out} = 0 µA I_{out} = – 0.4 mA	2.5	2.35 2.0	V
		I_{out} = 0 µA I_{out} = – 1.0 mA	6.0	5.85 5.5	
I_{in}	Maximum Input Current DEC_{in} ENC ENB, DRST, OSC_{in}	$V_{in} = V_{DD}$ or V_{SS}	6.0	± 60 ± 0.3	µA
I_{IH}	Maximum High-Level Input Leakage Current A0–A8	$V_{in} = V_{DD}$	6.0	0.3	µA
I_{IL}	Maximum Low-Level Pull-Up Current A0–A8	$V_{in} = V_{SS}$	6.0	– 100	µA
I_{OZ}	Maximum Three-State Leakage Current ENC_{out}	$V_{out} = V_{DD}$ or V_{SS}	6.0	± 500	nA
I_{DD}	Maximum Quiescent Supply Current	Device in Standby Mode $V_{in} = V_{SS}$ or V_{DD} for ENC ENB, DEC_{in}, DRST, OSC_{in} $V_{in} = V_{SS}$, V_{DD}, or Open for A0–A8 I_{out} = 0 µA	2.0 6.0	20 100	µA
I_{dd}	Maximum RMS Operating Supply Current	Oscillator Frequency = 500 kHz $V_{in} = V_{SS}$ or V_{DD} for ENC ENB, DEC_{in}, DRST, OSC_{in} $V_{in} = V_{SS}$, V_{DD}, or Open for A0–A8 I_{out} = 0 µA	2.5 6.0	700 2500	µA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, C_L = 50 pF, V_{DD} = 2.5 to 6 V unless otherwise stated)

Symbol	Parameter	Figure #	V_{DD} V	Guaranteed Limit	Unit
f_{osc}	Maximum Oscillator Frequency (≈ 50% Duty Cycle)*	2	—	500	kHz
t_{PLH}, t_{PHL}	System Propagation Delay, ENC ENB (of an encoding device) to DEC_{out} (of a decoding device)	3, 5	—	384–608	OSC Cycles
t_d	Debounce Time, ENC ENB (guarantees 1 encoding sequence)		—	608	OSC Cycles
t_w	Minimum Input Pulse Width, ENC ENB or DRST	4	2.5 6.0	200 80	ns
C_{in}	Maximum Input Capacitance		—	10	pF

*See Pin Descriptions and Application Example for component tolerances.

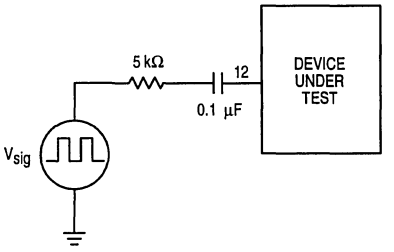


Figure 1. Decoder Input Sensitivity Test

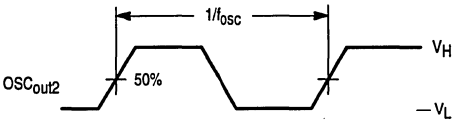


Figure 2. Switching Waveform

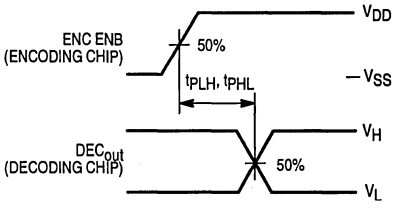


Figure 3. Switching Waveforms

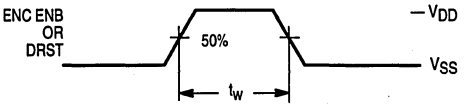
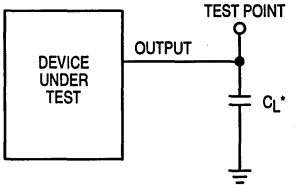


Figure 4. Switching Waveform



*Includes all probe and fixture capacitance.

Figure 5. Test Circuit

PIN DESCRIPTIONS

INPUT PINS

A0–A8
Local Address Inputs (Pins 1, 3–9, 2)

These binary inputs provide the address for both the encoder and decoder; 512 addresses are possible. The local address is sent serially from ENC_{out} with 2 sync bits appearing first, followed by A0. The decoder compares the local address with the received address stream.

On-chip pullup devices are provided on the address inputs to facilitate interface to SPST switches or jumpers to V_{SS}. During standby, A0–A8 are in the high-impedance state (i.e., the pull-up devices are inactive to minimize standby power consumption).

The inputs are left open (or tied to V_{DD}) for a high level and tied to V_{SS} for a low level.

ENC ENB
Edge-Sensitive Encode Enable (Pin 10)

A low-to-high transition on this pin aborts any decoding sequence in progress and initiates an encoding sequence. This input is debounced 608 oscillator cycles. See Figures 8 and 9.

DEC_{in}
Decoder In (Pin 12)

Decoder In is the input to the on-chip amplifier. The incoming signal is usually capacitively-coupled to this pin. Direct coupling may be used if the signal level is rail-to-rail (V_{SS} to V_{DD}).

DRST
Level-Sensitive Decoder Reset (Pin 13)

When this input is taken high, DEC_{out} is cleared to a low level. This pin may be used to override a response from a DEC_{in} data stream.

OUTPUT PINS

STATUS
Encode/Decode Status (Pin 11)

This pin is high during the encoding sequence and low during decoding or idle.

When Status is low, the ENC_{out} pin is in the high-impedance state.

DEC_{out}
Toggle Flip-Flop Decoder Output (Pin 15)

The encoder sends the same address twice to complete a sequence. If one or both of the decoded addresses matches the local address, DEC_{out} toggles once per sequence (unless overridden by DRST). See Figures 6 and 7.

ENC_{out}
Three-State Encoder Output (Pin 16)

This is the serial output of the Manchester-encoded local address. A0 appears before A8 in the bit stream. The local address is sent twice to complete a sequence which is initialized by ENC ENB. When a sequence is complete, ENC_{out} returns to the high-impedance state. See Figures 8 and 9.

OSCILLATOR PINS

OSC_{in}, OSC_{out1}, OSC_{out2}
Oscillator Input, Oscillator Outputs 1/2 (Pins 20, 19, 18)

As shown in Figure 10, these pins are used in conjunction with external resistors and a capacitor to form an oscillator. Polystyrene or mylar capacitors are recommended. Susceptibility to externally induced noise signals may occur if resistors utilized are greater than 1 MΩ. See Figure 10 for component tolerances.

When the on-chip oscillator is used, the frequency may be up to 500 kHz. The oscillator is active only during encoding or decoding.

When an external frequency source is used to drive OSC_{in}, OSC_{out1} and OSC_{out2} may be left floating. The signal applied to OSC_{in} should swing rail-to-rail and may be dc to 500 kHz.

POWER SUPPLY PINS

V_{SS}
Negative Power Supply (Pin 17)

This pin is the negative supply potential and is usually ground.

V_{DD}
Positive Power Supply (Pin 14)

This pin is the positive supply potential and may range from + 2 to + 6 V with respect to V_{SS}.

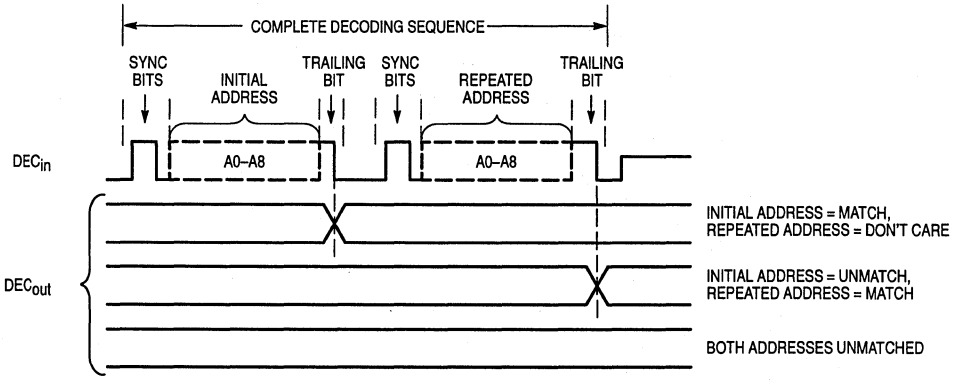


Figure 6. Decoder Timing Diagram

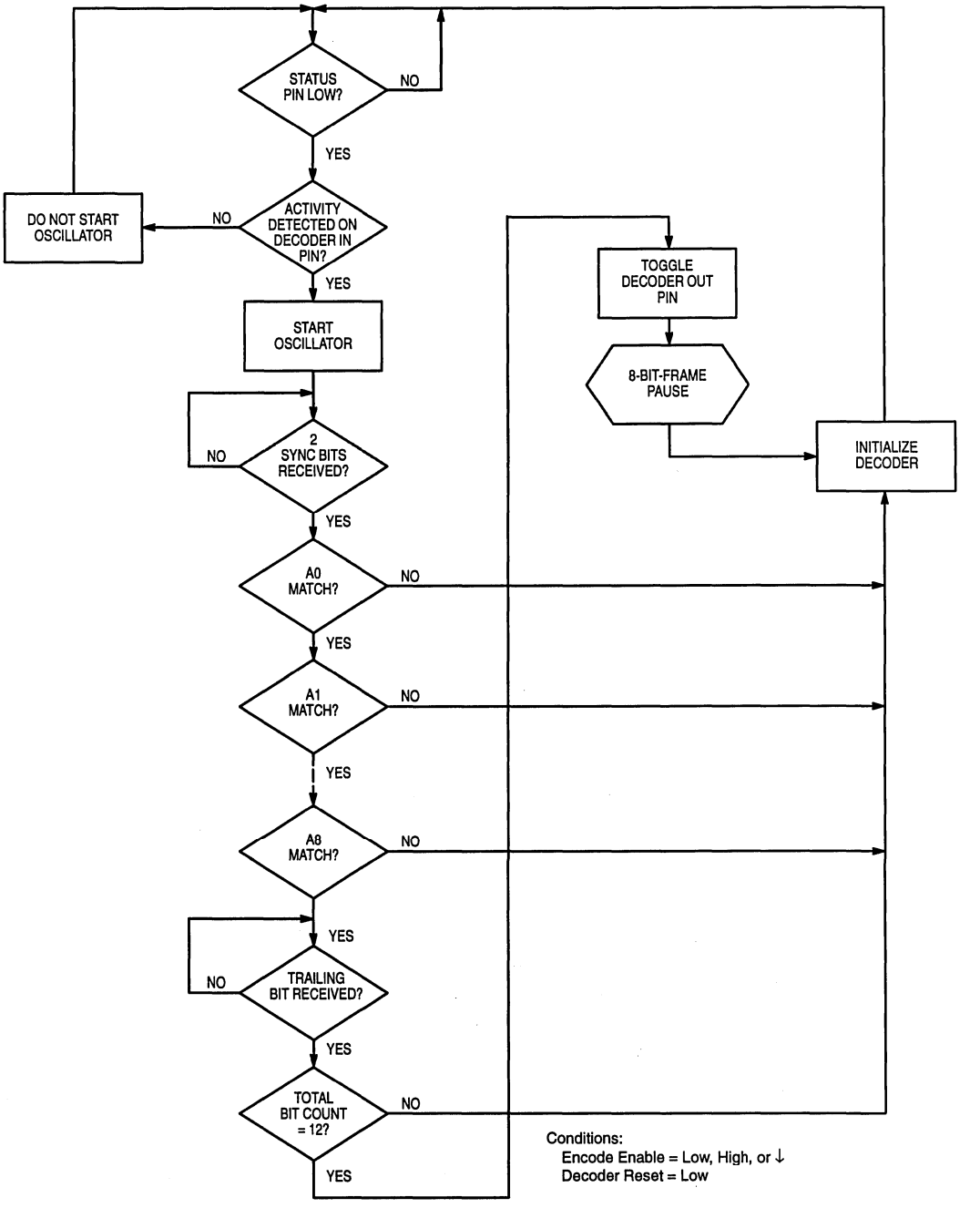


Figure 7. Decoder Flowchart

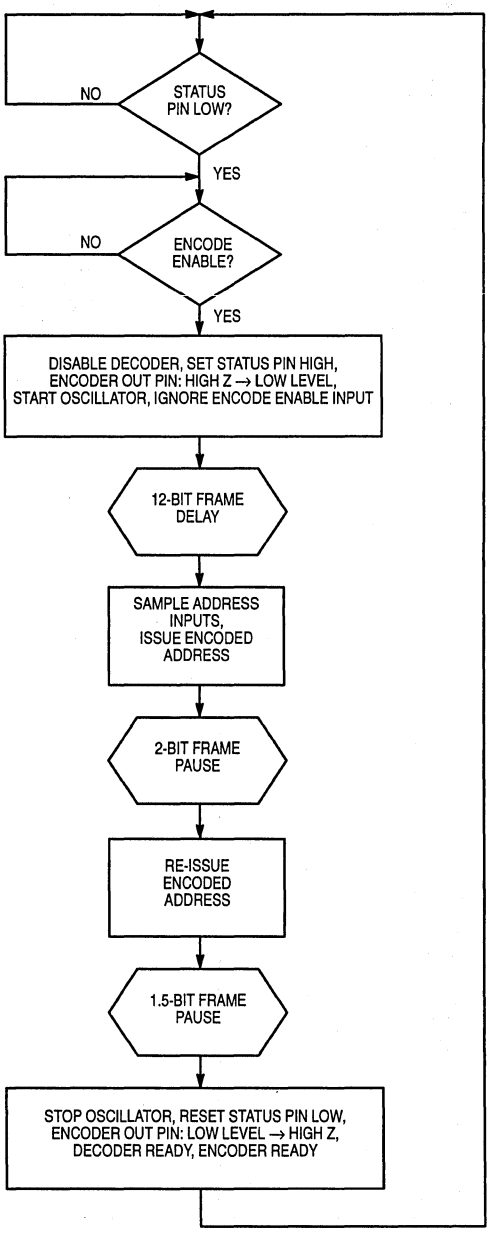


Figure 8. Encoder Flowchart

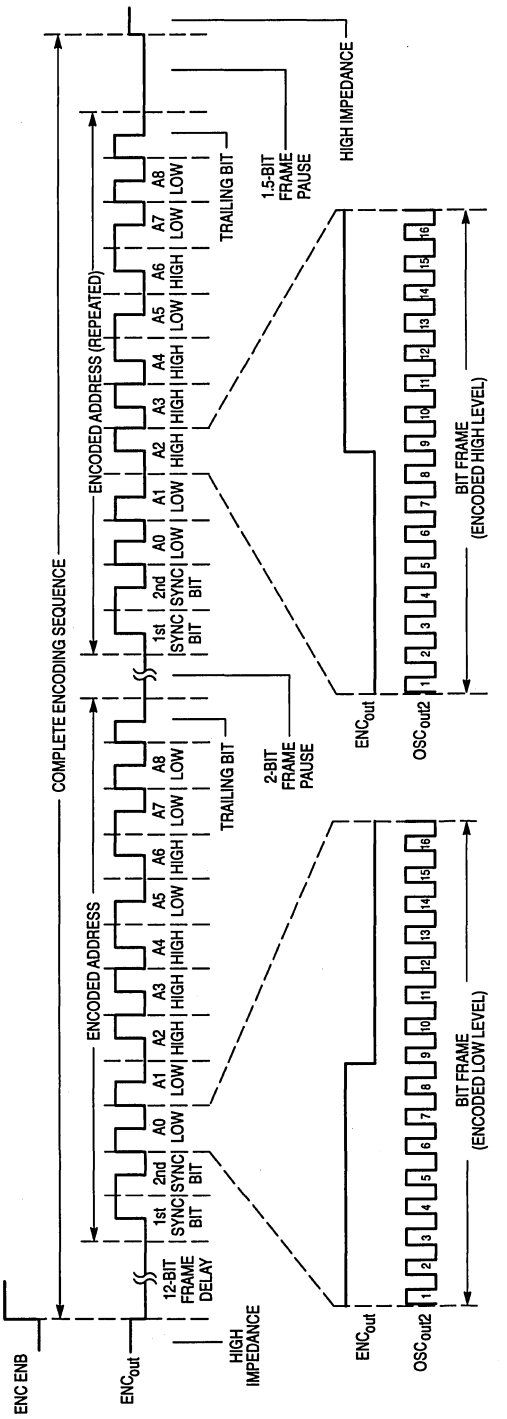
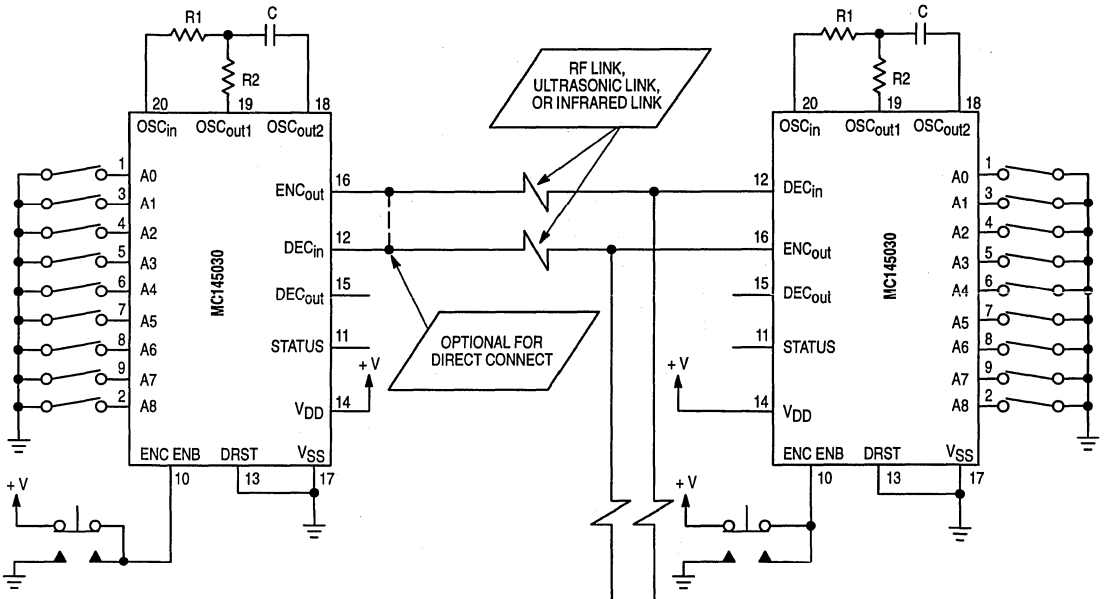


Figure 9. Encoder Timing Diagram



EXAMPLE R/C VALUES

f_{OSC} (APPROX.)	R1	R2	C	ENCODE ENABLE SWITCH DEBOUNCE TIME (APPROX.)
452 kHz	30 kΩ	5.6 kΩ	100 pF	1.3 ms
220 kHz	47 kΩ	10 kΩ	100 pF	2.8 ms
70 kHz	47 kΩ	10 kΩ	510 pF	8.7 ms
4.1 kHz	330 kΩ	47 kΩ	2200 pF	148 ms

GUIDELINES: 100 pF ≤ C ≤ 0.1 μF
2 (R2) < R1 < 10 (R2)
10 kΩ ≤ R2 ≤ 500 kΩ
R1 ≤ 1 MΩ

The maximum oscillator frequency difference allowable from encoding IC to decoding IC is ± 11%. The ambient temperature and supply voltage differences between ICs affect this frequency difference. Therefore, the tolerances of the frequency-determining components R2 and C are determined by the rule of thumb:

$$[\Delta R2 + \Delta C + \Delta f_{IC} + \Delta f_{temp} + \Delta f_{sup}] \leq \pm 11\%,$$

where

R2 = tolerance of R2 in percent
C = tolerance of C in percent
f_{IC} = IC frequency variation from part to part (expected value: ± 4%)
f_{temp} = IC frequency variation over temperature (expected value: ± 2% @ 25°C ± 40°)
f_{sup} = IC frequency variation with supply (expected value: ± 2% @ 5 V ± 0.5 V)

For the above variances: $[\Delta R2 + \Delta C + (\pm 4\%) + (\pm 2\%) + (\pm 2\%)] \leq \pm 11\%$
$[\Delta R2 + \Delta C] \leq \pm 3\%$

Choose R2 with a ± 1% tolerance and C2 with a ± 2% tolerance. R1 may be ± 5%.

Figure 10. Application Example

MC145031
MC145032
MC145033
MC145034
MC145035

Advance Information

Encoders and Decoders

CMOS

For remote control devices, the MC145031/34 function as encoders and the MC145032/35 function as decoders. The MC145033 functions as both an encoder and a decoder.

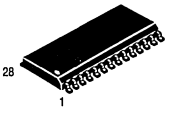
The encoders convert parallel address and data inputs into the Manchester code format and output the information serially via the D0–D3 pins.

The decoders revert the serial Manchester-coded input back into binary and compare the incoming address with local one. If both addresses match, a valid data output (VD) signal is asserted and the proper data appears at the D_{out} pin.

The difference between the MC145031/2 and MC145034/5 is the VD output pin. The VD output of the MC145031/2 is a toggle function while the MC145034/5 is a "one shot" valid address output pulse if a correct data sequence and matched address are received.

The MC145033 encoder/decoder has a status output. The status pin, when high, indicates the device is encoding. During decoding or standby, status is low.

- Typical Applications: Remote Control, Security Systems, and Keyless Entry
- Manchester Coding
- RC Oscillator, No Crystal Required
- Binary Address and Data Inputs
- Two-Word Transmit Sequence
- Built-In Input Data Amplifier
- Schmitt-Trigger Serial Input for Excellent Noise Immunity
- Code Break Output with Adjustable Error Code Transmission Time Window
- Operating Voltage Range: 2 to 6 V
- Operating Temperature Range: −40 to +85°C
- MC145031 Encoder/MC145032 Decoder Pair: 13 Address and 4 Data Lines or 17 Address Lines
- MC145033 Encoder/Decoder: 15 Address Lines
- MC145034 Encoder/MC145035 Decoder Pair: 13 Address and 4 Data Lines or 17 Address Lines
- Address/Data Inputs have On-Chip Pull-Up Devices
- See Application Note AN1126



DW SUFFIX
SOG
CASE 751F

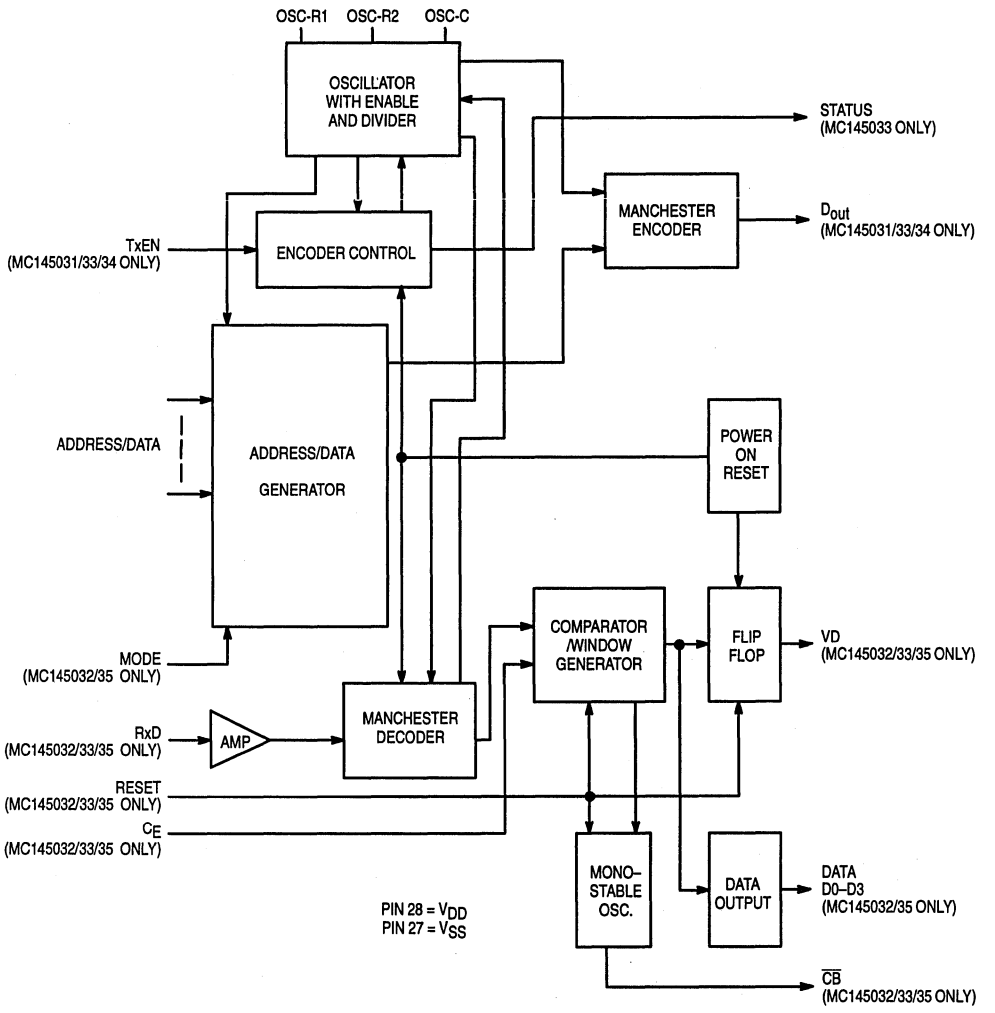
ORDERING INFORMATION

MC145031DW	SOG Package
MC145032DW	SOG Package
MC145033DW	SOG Package
MC145034DW	SOG Package
MC145035DW	SOG Package

NOT RECOMMENDED
FOR NEW DESIGN

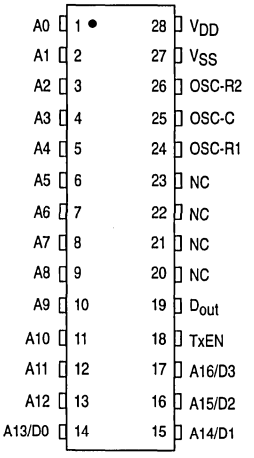
This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM OF MC145031/32/33/34/35

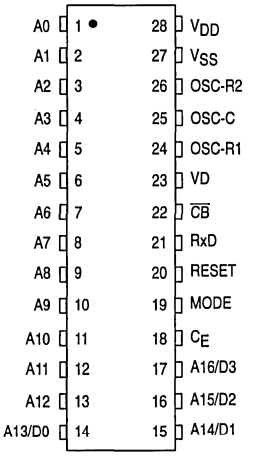


PIN ASSIGNMENTS

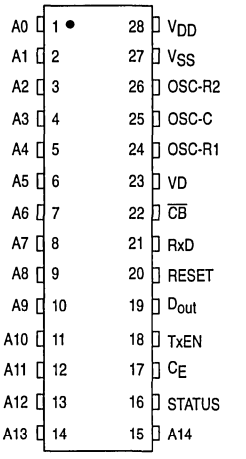
MC145031 ENCODER



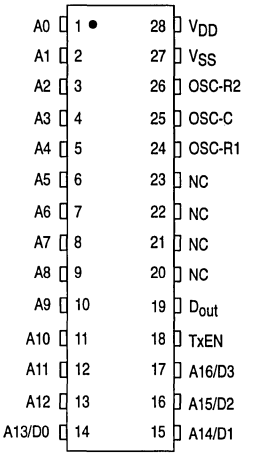
MC145032 DECODER



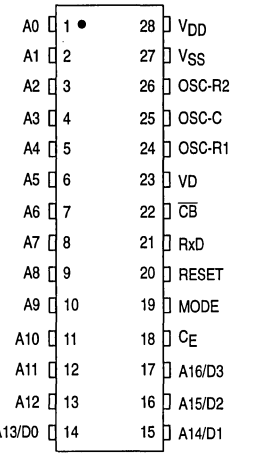
MC145033 ENCODER/DECODER



MC145034 ENCODER



MC145035 DECODER



NC = No Connection

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +0.7	V
V_{in}	DC Input Voltage	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD} +0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-second soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
† Power Dissipation Temperature Derating: −12 mW/°C from 65°C to 85°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Except for the Address inputs, unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). The Address inputs may be left open, see Pin Descriptions. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (T_A = −40 to +85°C, C_L = 50 pF, V_{DD} = 2.5 to 6 V unless otherwise stated)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	2.0 to 6.0	V
V_{IL}	Maximum Low-Level Input Voltage Except RxD		2.5 6.0	0.3 1.2	V
V_{IH}	Minimum High-Level Input Voltage Except RxD		2.5 6.0	1.9 4.5	V
V_{OL}	Maximum Low-Level Output Voltage	I_{out} = 0 µA I_{out} = 0.4 mA	2.5	0.15 0.4	V
		I_{out} = 0 µA I_{out} = 1.0 mA	6.0	0.15 0.4	
V_{OH}	Minimum High-Level Output Voltage	I_{out} = 0 µA I_{out} = −0.4 mA	2.5	2.35 2.0	V
		I_{out} = 0 µA I_{out} = −1.0 mA	6.0	5.85 5.5	
I_{in}	Maximum Input Current RxD TxEN, RESET, OSC-R2	V_{in} = V_{DD} or V_{SS}	6.0	±80 ±0.3	µA
I_{IH}	Maximum High-Level Input Leakage Current A0–A16	V_{in} = V_{DD}	6.0	0.3	µA
I_{IL}	Maximum Low-Level Pull-Up Current A0–A16	V_{in} = V_{SS}	6.0	−100	µA
I_{OZ}	Maximum Three-State Leakage Current D_{out}	V_{out} = V_{DD} or V_{SS}	6.0	±500	nA
I_{DD}	Maximum Quiescent Supply Current (per Package)	Device in Standby mode, V_{in} = V_{DD} or V_{SS} for TxEN, Decoder in, RESET, OSC-R2. V_{in} = V_{SS}, V_{DD}, or open for A0–A16. I_{out} = 0 µA	2.5 6.0	25 100	µA
I_{dd}	Maximum RMS Operating Supply Current (per Package)	Oscillator Frequency = 500 kHz. V_{in} = V_{SS} or V_{DD} for TxEN, RESET, OSC-R2. V_{in} = V_{SS}, V_{DD}, or open for A0–A16. I_{out} = 0 µA	2.5 6.0	700 2500	µA
I_{OL}	Code Break Sink Current $\overline{CB}$			5	mA
V_{in}	Minimum RxD Input Level For Decoder	Square wave, see Figure 1	6.0	200	mVp-p

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, C_L = 50 pF, V_{DD} = 2.5 to 6 V unless otherwise stated)

Symbol	Parameter	Figure #	V_{DD} V	Guaranteed Limit	Unit
f_{OSC}	Maximum Oscillator Frequency (50% Duty Cycle)	2	—	500	kHz
t_d	Debounce Time, TxEN (guarantees 1 encoding sequence)		—	500	OSC cycles
t_w	Minimum Input Pulse Width, TxEN or RESET	3	2.5 6.0	200 80	ns
C_{in}	Maximum Input Capacitance		—	10	pF

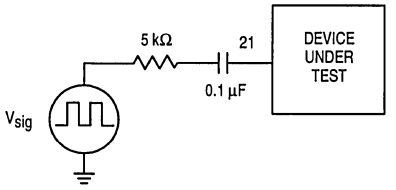


Figure 1. Decoder In Sensitivity Test

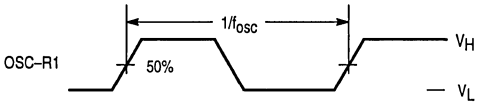


Figure 2. Switching Waveform

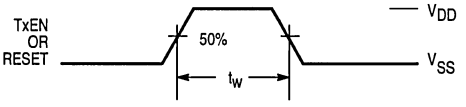


Figure 3. Switching Waveform

GENERAL DESCRIPTION

ENCODER

The encoder circuit encodes the parallel binary input address/data into Manchester code and outputs the information serially.

Each transmitted word is preceded by a two-bit dead time interval. Once the TxEN (transmit enable) pin is triggered by a high level, a two-word transmit sequence following a 12-bit preamble is serially output at the D_{out} terminal. The transmit sequences repeat continuously if TxEN remains high. The minimum is one complete sequence; if TxEN goes low, the transmission continues until the end of the current transmit sequence.

The data rate is set at one eighth of the system clock, which is an RC oscillator.

One transmission cycle comprises:

1. 12-bit preamble
2. 2-bit dead time interval
3. First word
4. 2-bit dead time interval
5. Second word

One transmitted word consists of:

1. 2 start bits
2. The address/data bits
3. 2 stop bits

DECODER

The decoder circuit accepts a serial Manchester-coded input at the RxD pin. The data stream is then decoded and compared with the local address set by the parallel address inputs. When a correct transmit sequence (two identical words) is received and the incoming address matches the local one, the valid data (VD) output on the MC145035 goes high and the decoded data may then be read at the Data outputs (D0–D3) if the Mode pin is high (see the **Mode** pin description). VD remains high unless an erroneous address/data is detected or the transmit sequence is terminated.

For the MC145032 and MC145033, the VD output is a toggle function. That is, VD changes state once each time a valid sequence of bits is received. If needed, VD can be reset to a low level via the Reset pin.

If the decoder detects an error in the incoming transmit sequence, a time window is opened at the end of that sequence. If two consecutive erroneous transmit sequences are received within that window, the code break ($\overline{CB}$) output goes low until the window's duration is over. During the opened window, the $\overline{CB}$ output can be reset by either the reset input or a correct transmit sequence that follows. The window duration is controlled by an external capacitor connected to pin C_E. The duration of the $\overline{CB}$ output is equal to TB, which is half of error window time constant TE.

PIN DESCRIPTIONS

V_{DD}
Power Supply (Pin 28)
Power supply. This pin may range from +2 to +6 V with respect to V_{SS}.

V_{SS}
Ground (Pin 27)
Power supply ground.

TxEN
Transmit Enable (Pin 18)—*MC145031/33/34 Only*
A low-to-high transition on the Transmit Enable pin initiates a transmit sequence. Transmission is continuous if TxEN remains high.

D_{out}
Data Out (Pin 19)—*MC145031/33/34 Only*
Three-state encoder output. It serially outputs the Manchester-coded transmit data, when initiated by TxEN.

VD
Valid Address Output (Pin 23)
MC145032/33 Only: This "toggle" output changes state whenever a correct transmit sequence is received and the address matches the local one (see Figure 4). A high level on VD can be cleared by either a correct transmit sequence that follows or the RESET input.

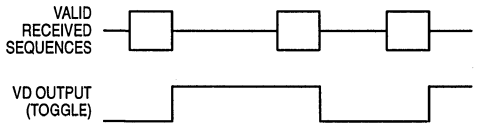


Figure 4. Valid Address Output Timing (MC145032 and MC145033)

MC145035 Only: VD goes high if, and only if, a correct transmit sequence is received and the address matches the local one. The VD output remains high unless an erroneous address/data is detected or the transmit sequence is terminated. The minimum duration of VD is guaranteed by an external RC. See Figures 5 and 7.

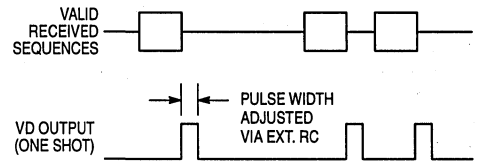


Figure 5. Valid Address Output Timing (MC145035)

RESET
Reset (Pin 20)
MC145032/33 Only: A positive pulse on this pin resets the $\overline{CB}$ output and VD output.
MC145035 Only: A positive pulse on this pin resets the $\overline{CB}$ output and the VD output. Its resets VD only when there is no RxD received (see Figure 7).

$\overline{CB}$
Code Break (Pin 22)—*MC145032/33/35 Only*
Decoder code-break open-drain output. $\overline{CB}$ goes low if two additional consecutive erroneous transmit sequences following the 1st error have been received within the window set by external capacitor C_E. While in an active state, it can be cleared by the RESET input.

An external PNP transistor may be utilized to charge up the C_E (timing capacitor) to disable the low frequency oscillator. As a result, the TB counter stops. In this case, the $\overline{CB}$ output remains activated until a "reset" signal is applied to reset the C_E flip-flop (see Figures 6 and 7).

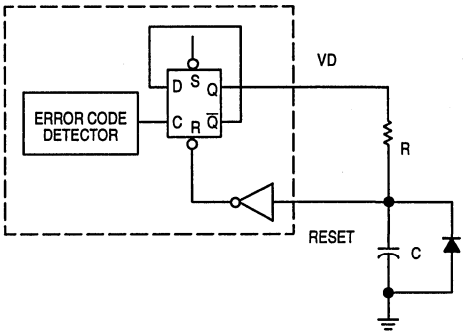


Figure 6. One Shot VD Output Circuit (MC145035)

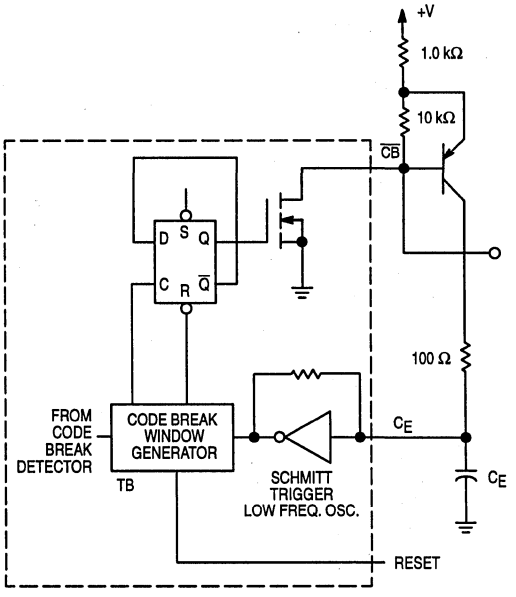


Figure 7. Code Break Window Control

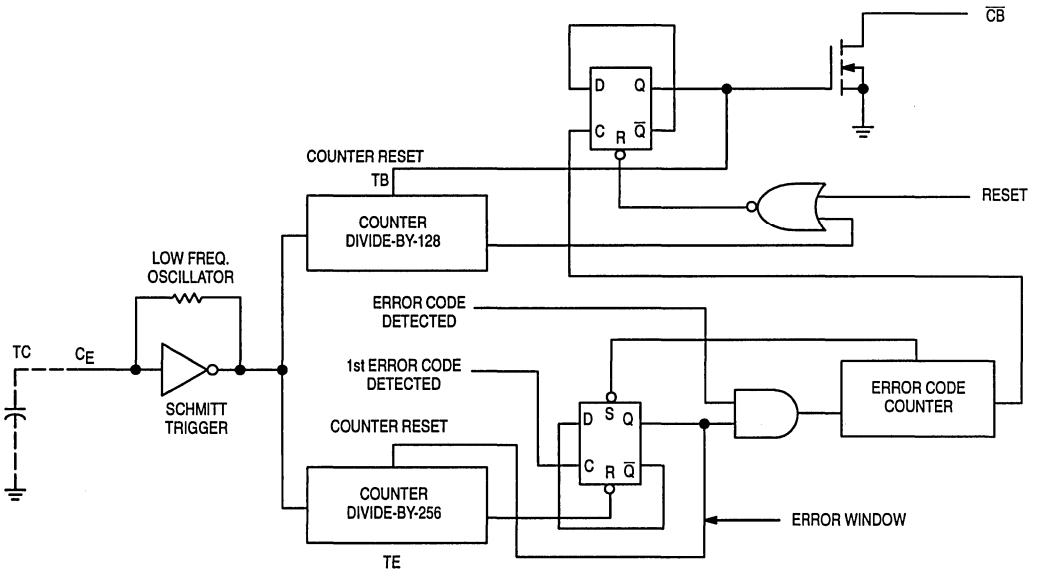


Figure 8. Error Window TE and Code Break Window Generator TB

A0–A12 and A13/D0–A16/D3
Address Inputs (Pins 1–17)
MC145031/31/34/35 Only: Bidirectional address/data pins. These pins form a binary input port during encoding. The pins become a three-state data output during decoding if the Mode pin is tied to V_{DD}.
MC145033 Only: Binary address inputs. These pins form a binary input port during the encoding sequence. These inputs become the local address during the decoding sequence.

STATUS
Encode/Decode Status (Pin 16)
MC145033 Only: This pin is high during the encoding sequence and low during decoding or idle. When Status is low, the D_{out} pin is in a high-impedance state.

RxD
Serial Data Input (Pin 21)
MC145032/33/35 Only: Serial data input to the Manchester decoder. Minimum encoded data signal level is 200 mVp-p (see Figure 9).

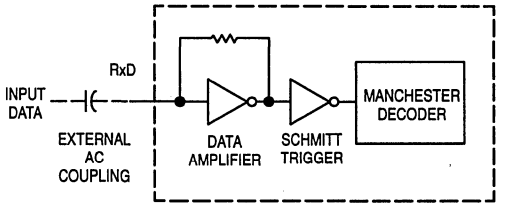
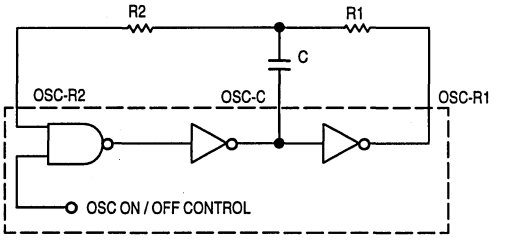


Figure 9. RxD Pin Coupling

OSC-R2, OSC-R1, OSC-C
Oscillator (Pins 26, 24, and 25)
The oscillator frequency is determined by the external RC network (see Figure 10). There is only a 4% change in system oscillating frequency as the supply voltage varies from 2 to 6 V.

The encoder system oscillating frequency can be varied ±10% with reference to decoder system oscillator frequency for valid detection.



$$f = \frac{0.38}{R1C} \text{ (Hz)}$$

for f ≤ 150 kHz where R2=2R1
The system oscillating frequency is eight times the encoded data rate.

Figure 10. RC Oscillator

MODE
Mode Select Input (Pin 19)
MC145032/35 Only: This pin defines the A13/D0–A16/D3 lines to be address or data lines. It is internally pulled high.
L=Address Lines
H=Data Lines

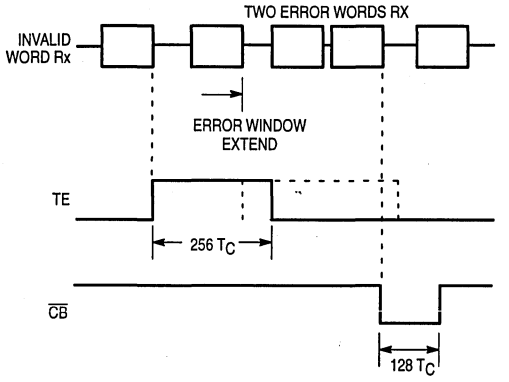


Figure 11. Error Window and $\overline{CB}$ Output Timing

C_E
External Capacitor
(Pin 18—MC145032/35; Pin 17—MC145033)

Error window duration control input. The built-in Schmitt trigger oscillator frequency is controlled by external capacitor C_E. The error window (TE) is equal to 256 times the internal oscillator cycle.

If an unmatched data word (error code) is detected, an internal window TE is generated. If two or more errors are detected within the TE period, the $\overline{CB}$ signal is activated, signaling that an outsider is trying to break the code of this system (noise cannot activate the code break output).

If only one error code is detected within the window, the window period is automatically extended from the last invalid word to check if there are two or more error codes. If so, the $\overline{CB}$ signal is activated; if not, TE is closed after a defined period. See Figures 8 and 11.

TE and TB are generated from a Schmitt-trigger low frequency oscillator of which the period (TC) is controlled by C_E. The period of this low frequency oscillator is defined as TC as indicated in Figure 8.

TE is generated by an 8-stage counter.

TB is generated by a 7-stage counter.

TE = 256 TC and TB = 128 TC.

The relation between TC and C_E is listed below with a 5.0-V supply.

Timing Capacitor (C_E)	Cycle Time (TC)
4.7 µF	1430 ms
1.0 µF	330 ms
0.1 µF	26 ms
0.047 µF	12 ms
0.022 µF	5.6 ms
0.01 µF	2.5 ms
0.0047 µF	1.0 ms
0.001 µF	0.3 ms

In order to minimize false $\overline{CB}$ triggers, one error code is allowed for every TE period (256 TC).

Suppose C_E = 4.7 µF, TC = 1430 ms, and TE = 256 TC. On an average, it takes 2^{10} trials in order to succeed in breaking the system coding. Total time taken in breaking the system coding = # of trials x TC x 256.

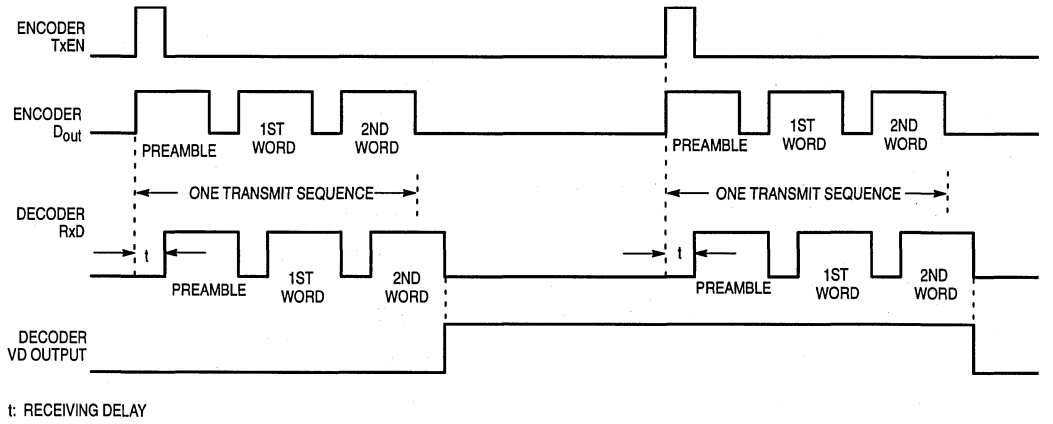
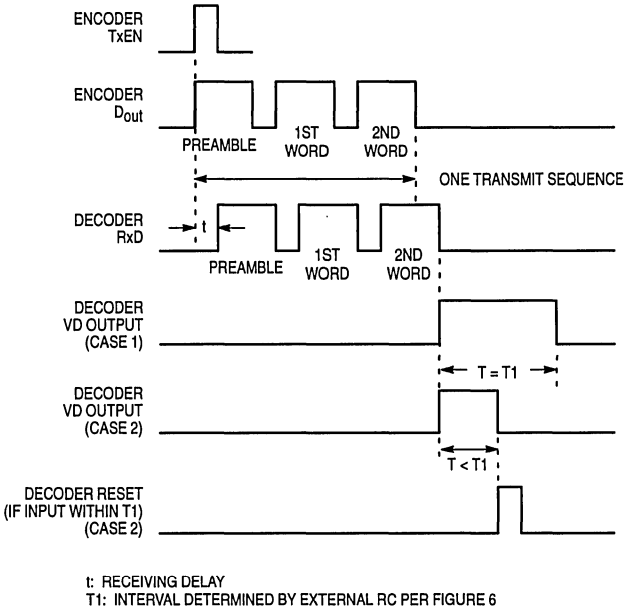
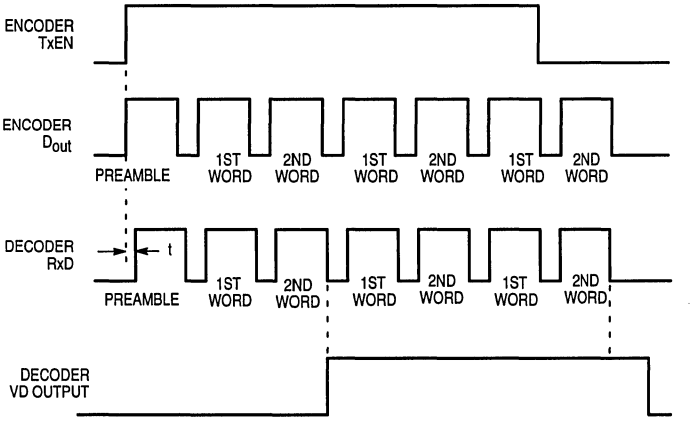


Figure 12. MC145031/32/33 Encoding and Decoding Timing Diagram



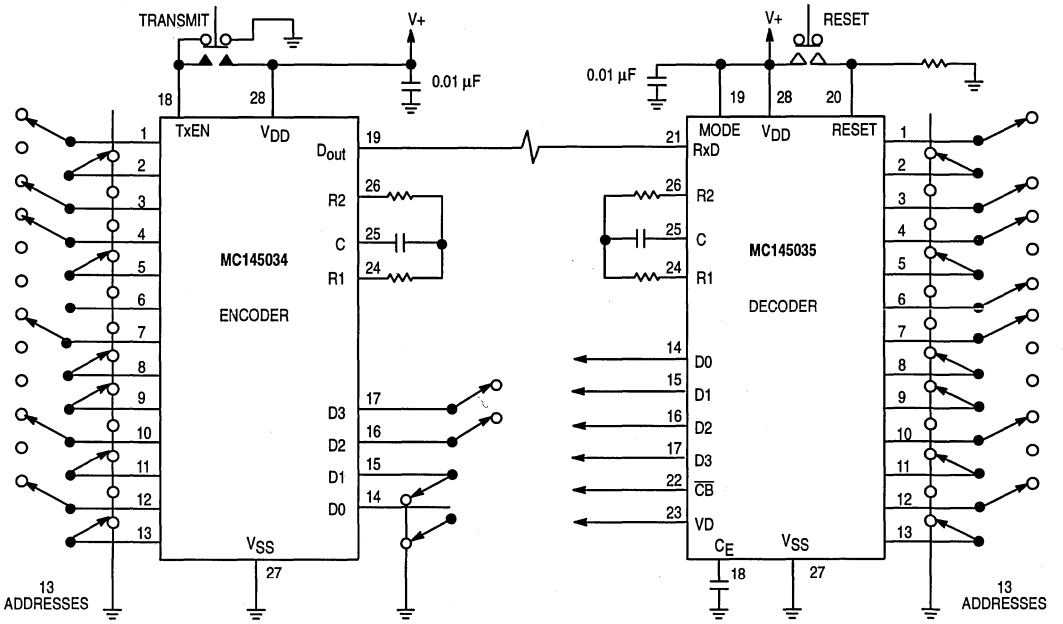
t: RECEIVING DELAY
T1: INTERVAL DETERMINED BY EXTERNAL RC PER FIGURE 6

Figure 13. MC145034/35 Encoding and Decoding Timing Diagram — Single Transmission



t: RECEIVING DELAY

Figure 14. MC145034/5 Encoding and Decoding Timing Diagram — Continuous Transmissions



FOR DATA RATE = 500 BAUD
OSC. FREQ = 4 kHz
R1 = 10 kΩ
R2 = 22 kΩ
C = 0.01 µF

Figure 15. Typical Application

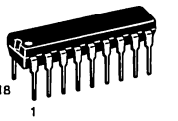
MC145106

PLL Frequency Synthesizer
CMOS

The MC145106 is a phase locked loop (PLL) frequency synthesizer constructed in CMOS on a single monolithic structure. This synthesizer finds applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 2^{10} or 2^{11} divider chain for the oscillator signal, a programmable divider chain for the input signal and a phase detector. The MC145106 has circuitry for a 10.24-MHz oscillator or may operate with an external signal. The circuit provides a 5.12-MHz output signal, which can be used for frequency tripling. A 2^9 programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground-to-supply binary signals. Pull-down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

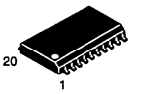
The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out-of-lock signal is provided from the on-chip lock detector with a "0" level for the out-of-lock condition.

- Single Power Supply
- Wide Supply Range: 4.5 to 12 V
- Provision for 10.24-MHz Crystal Oscillator
- 5.12-MHz Output
- Programmable Division Binary Input Selects up to 2^9
- On-Chip Pull Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2^{10} or 2^{11} (including ÷ 2)
- Three-State Phase Detector
- See Application Note AN535 and Article Reprint AR254
- Chip Complexity: 880 FETs or 220 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 707

FN SUFFIX
PLCC
CASE 775



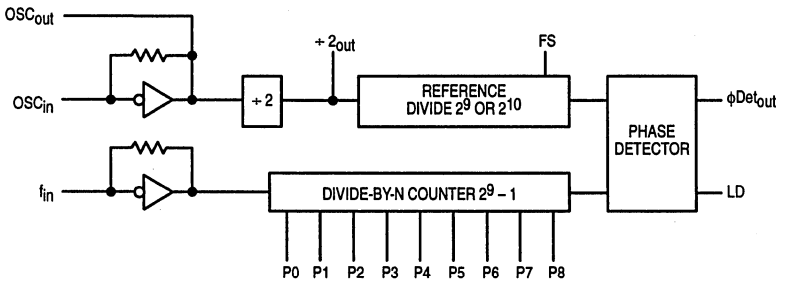
DW SUFFIX
SOG
CASE 751D

ORDERING INFORMATION

MC145106P	Plastic DIP
MC145106FN	PLCC
MC145106DW	SOG

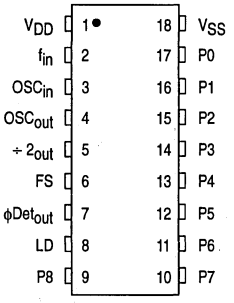
The PLCC (FN suffix) package will be phased out for this device and is NOT RECOMMENDED FOR NEW DESIGNS.

BLOCK DIAGRAM

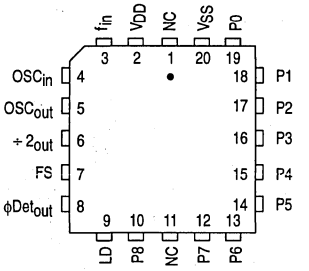


PIN ASSIGNMENTS

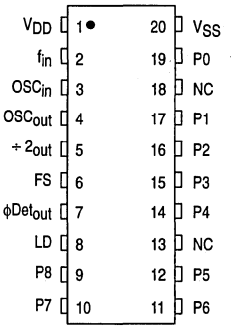
PLASTIC DIP



PLCC PACKAGE



SOG PACKAGE



NC = NO CONNECTION

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	− 0.5 to + 12	V
Input Voltage, All Inputs	V_{in}	− 0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I	± 10	mA
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless Otherwise Stated, Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	All Types			Unit
				Min	Typ*	Max	
Power Supply Voltage Range		V_{DD}	—	4.5	—	12	V
Supply Current		I_{DD}	5.0	—	6	10	mA
			10	—	20	35	
			12	—	28	50	
Input Voltage	"0" Level	V_{IL}	5.0	—	—	1.5	V
			10	—	—	3.0	
			12	—	—	3.6	
	"1" Level	V_{IH}	5.0	3.5	—	—	
			10	7.0	—	—	
			12	8.4	—	—	
Input Current FS, Pull-Up Resistor Source Current)	"0" Level	I_{in}	5.0	−5.0	−20	−50	µA
			10	−15	−60	−150	
			12	−20	−80	−200	
(P0–P8)			5.0	—	—	−0.3	
			10	—	—	−0.3	
			12	—	—	−0.3	
(FS)	"1" Level		5.0	—	—	0.3	
			10	—	—	0.3	
			12	—	—	0.3	
(P0–P8, Pull-Down Resistor Sink Current)			5.0	7.5	30	75	
			10	22.5	90	225	
			12	30	120	300	
(OSC_{in}, f_{in})	"0" Level		5.0	−2.0	−6.0	−15	
			10	−6.0	−25	−62	
			12	−9.0	−37	−92	
(OSC_{in}, f_{in})	"1" Level		5.0	2.0	6.0	15	
			10	6.0	25	62	
			12	9.0	37	92	
Output Drive Current		I_{OH}					mA
(V_O = 4.5 V)	Source		5.0	−0.7	−1.4	—	
(V_O = 9.5 V)			10	−1.1	−2.2	—	
(V_O = 11.5 V)			12	−1.5	−3.0	—	
(V_O = 0.5 V)	Sink	I_{OL}					
(V_O = 0.5 V)			5.0	0.9	1.8	—	
(V_O = 0.5 V)			10	1.4	2.8	—	
			12	2.0	4.0	—	
Input Amplitude		—					V p-p
(f_{in} @ 4.0 MHz)			—	1.0	0.2	—	Sine
(OSC_{in} @ 10.24 MHz)			—	1.5	0.3	—	
Input Resistance		R_{in}					MΩ
(OSC_{in}, f_{in})			5.0	—	1.0	—	
			10	—	0.5	—	
			12	—	—	—	
Input Capacitance (OSC_{in}, f_{in})		C_{in}	—	—	6.0	—	pF
Three-State Leakage Current (ϕDet_{out})		I_{OZ}	5.0	—	—	1.0	µA
			10	—	—	1.0	
			12	—	—	1.0	
Input Frequency (− 40 to + 85°C)		f_{in}	4.5	0	—	4.0	MHz
			12	0	—	4.0	
Oscillator Frequency (− 40 to + 85°C)		OSC_{in}	4.5	0.1	—	10.24	MHz
			12	0.1	—	10.24	

*Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TYPICAL CHARACTERISTICS*

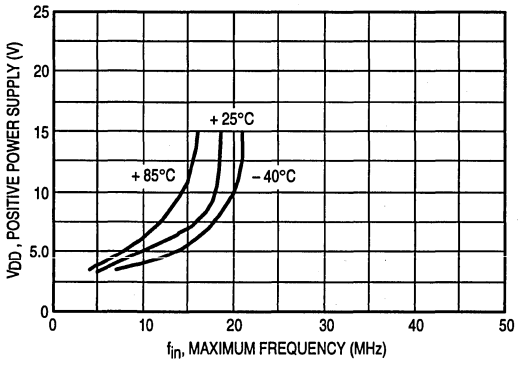


Figure 1. Maximum Divider Input Frequency versus Supply Voltage

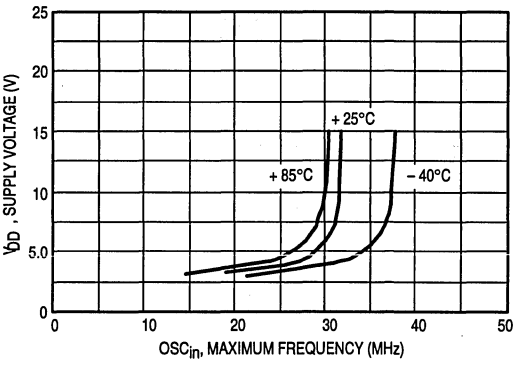


Figure 2. Maximum Oscillator Input Frequency versus Supply Voltage

*Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TRUTH TABLE

Selection									
P8	P7	P6	P5	P4	P3	P2	P1	P0	Divide by N
0	0	0	0	0	0	0	0	0	2*
0	0	0	0	0	0	0	0	1	3*
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	1	0	0	4
•	•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	1	255
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	511

1: Voltage level = V_{DD}.
0: Voltage level = 0 or open circuit input.
* The binary setting of 00000000 and 00000001 on P8 to P0 results in a 2 and 3 division which is not in the $2^N - 1$ sequence. When pin is not connected the logic signal on that pin can be treated as a "0".

PIN DESCRIPTIONS

P0–P8
Programmable Inputs
Programmable divider inputs (binary).

f_{in}
Frequency Input
Frequency input to programmable divider (derived from VCO).

OSC_{in}, OSC_{out}
Oscillator Input and Oscillator Output
Oscillator/amplifier input and output terminals.

LD
Lock Detector
LD is high when loop is locked, pulses low when out-of-lock.

ϕDet_{out}
Signal for control of external VCO, output high when f_{in}/N is less than the reference frequency; output low when f_{in}/N is greater than the reference frequency. Reference frequency is the divided down oscillator — input frequency typically 5.0 or 10 kHz.

FS
Reference Oscillator Frequency Division Select
When using 10.24 MHz OSC frequency, this control selects 10 kHz, a "0" selects 5.0 kHz.

$\div 2_{out}$
Reference OSC frequency divided by 2 output; when using 10.24 MHz OSC frequency, this output is 5.12 MHz for frequency tripling applications.

V_{DD}
Positive Power Supply

V_{SS}
Ground

NOTE
Phase Detector Gain = $V_{DD}/4\pi$

PLL SYNTHESIZER APPLICATIONS

The MC145106 is well suited for applications in CB radios because of the channelized frequency requirements. A typical 40 channel CB transceiver synthesizer, using a single crystal reference, is shown in Figure 3 for receiver IF values of 10.695 MHz and 455 kHz.

In addition to applications in CB radios, the MC145106 can be used as a synthesizer for several other systems. Various frequency spectrums can be achieved through the use of proper offset, prescaling, and loop programming techniques. In general, 300–400 channels can be synthesized using a single loop, with many additional channels available when multiple loop approaches are employed. Figures 4 and 5 are examples of some possibilities.

In the aircraft synthesizer of Figure 5, the VHF loop (top) will provide a 50 kHz, 360 channel system with 10.7 MHz R/T offset when only the 11.0500 MHz (transmit) and 12.1200 MHz (receive) frequencies are provided to mixer #1. When these signals are provided with crystal oscillators, the result is a three crystal 360 channel, 50 kHz step synthesizer. When using the offset loop (bottom) in Figure 5 to provide the indicated injection frequencies for mixer #1 (two for transmit and two for receive) 360 additional channels are possible. This results in a 720 channel, 25 kHz step synthesizer which requires only two crystals and provides R/T offset capability. The receive offset value is determined by the 11.31 MHz crystal frequency and is 10.7 MHz for the example.

The VHF marine synthesizer in Figure 4 depicts a single loop approach for FM transceivers. The VCO operates on frequency during transmit and is offset downward during receive. The offset corresponds to the receive IF (10.7 MHz) for channels having identical receive/transmit frequencies (simplex), and is (10.7 – 4.6 = 6.1) MHz for duplex channels. Carrier modulation is introduced in the loop during transmit.

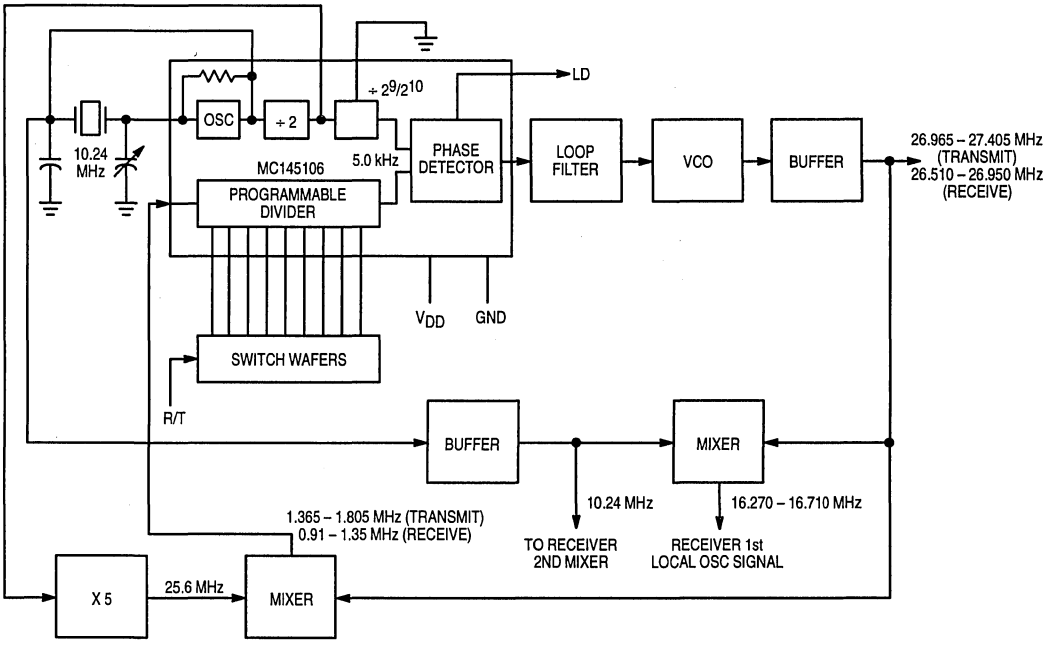
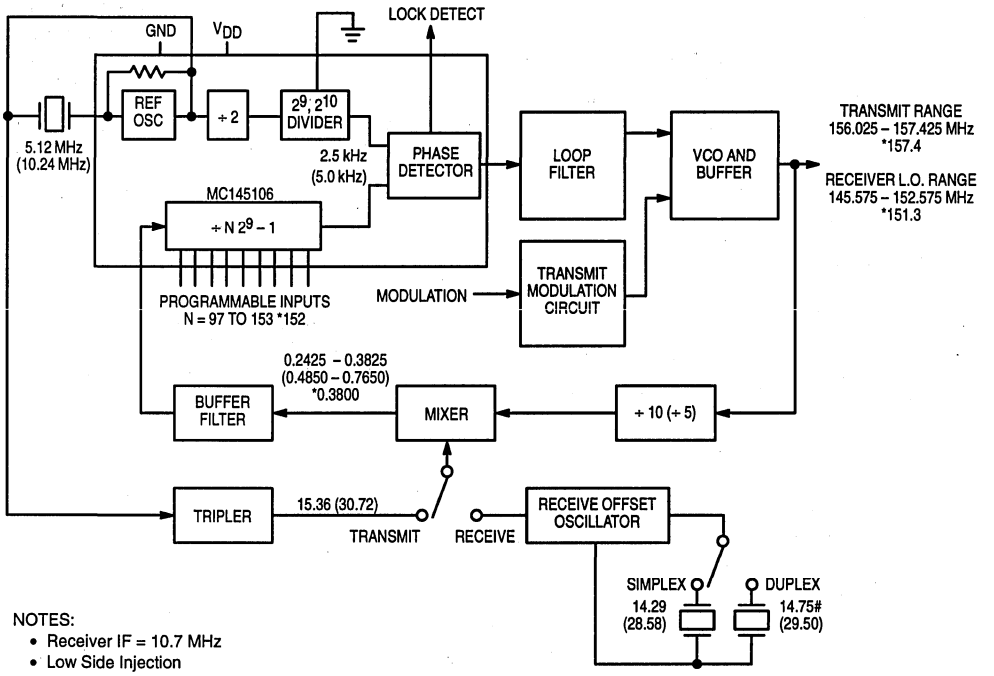


Figure 3. Single Crystal CB Synthesizer Featuring On-Frequency VCO During Transmit



NOTES:
- Receiver IF = 10.7 MHz
- Low Side Injection
- Duplex Offset = 4.6 MHz
- Step Size = 25 kHz
- Frequencies in MHz unless noted.
- Values in parentheses are for a 5.0 kHz reference frequency.
- Example frequencies for Channel 28 shown by *

#Can be eliminated by adding 184 to ÷ N for Duplex Channels.

Figure 4. VHF Marine Transceiver Synthesizer

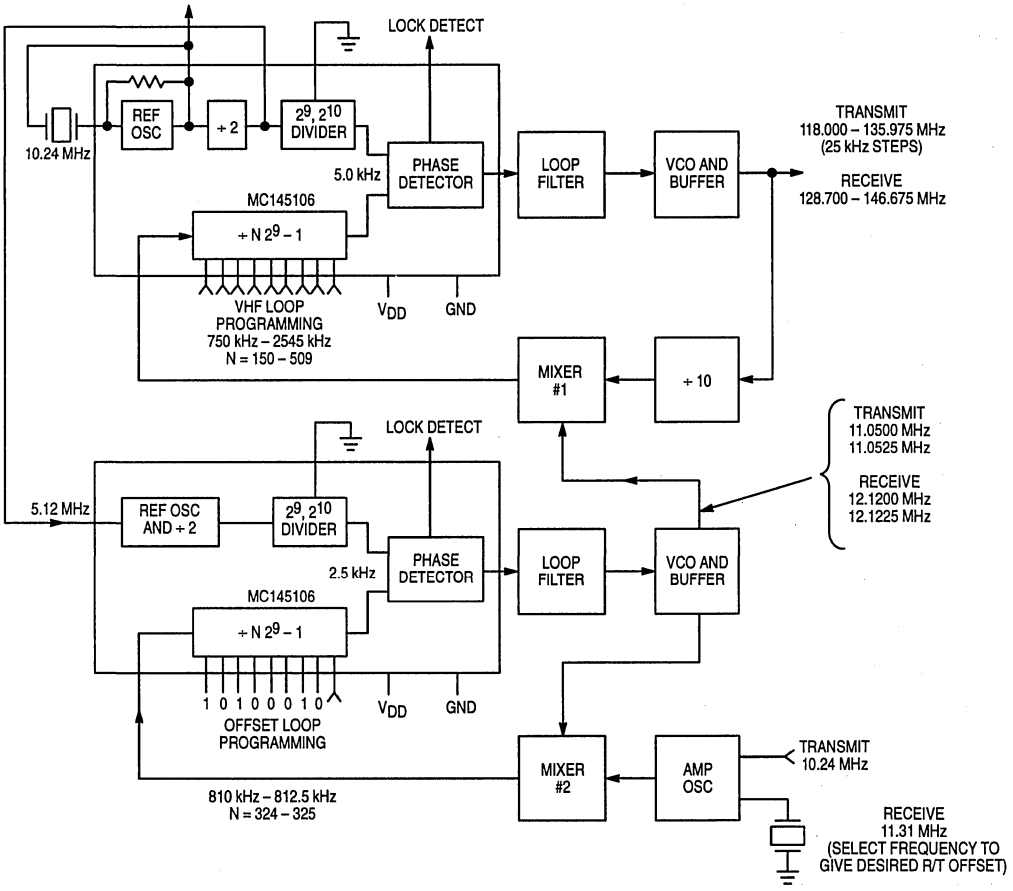


Figure 5. VHF Aircraft 720 Channel Two Crystal Frequency Synthesizer

MC145145-2

Advance Information

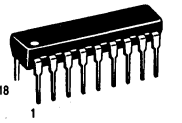
4-Bit Data Bus Input PLL Frequency Synthesizer

Interfaces with Single-Modulus Prescalers

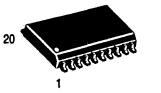
The MC145145-2 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, 12-bit programmable reference divider, digital phase detector, 14-bit programmable divide-by-N counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145145-2 can provide all of the remaining functions for a PLL frequency synthesizer operating up to the device frequency limit. For higher VCO frequency operation, a down mixer or a fixed divide prescaler can be used between the VCO and the MC145145-2.

The MC145145-2 is an improved performance drop-in replacement for the MC145145-1. Power consumption has decreased and ESD and latch-up performance have improved.

- General Purpose Applications
  - CATV — TV Tuning
  - AM/FM Radios — Scanning Receivers
  - Two Way Radios — Amateur Radio
- Low Power Consumption Through the Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Single Modulus 4-Bit Data Bus Programming
- On- or Off-Chip Reference Oscillator Operation
- +N Range = 3 to 16,383, +R Range = 3 to 4,095
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  - Single Ended (Three-State)
  - Double Ended
- Chip Complexity: 5,692 FETs or 1,423 Equivalent Gates



P SUFFIX
PLASTIC DIP
CASE 707



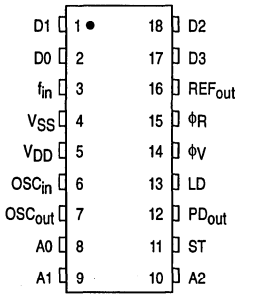
DW SUFFIX
SOG
CASE 751D

ORDERING INFORMATION

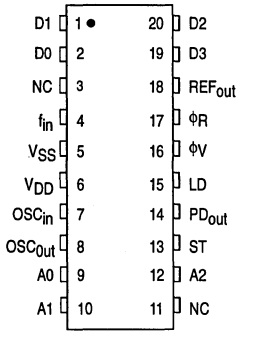
MC145145P2	Plastic DIP
MC145145DW2	SOG Package

PIN ASSIGNMENTS

PLASTIC DIP

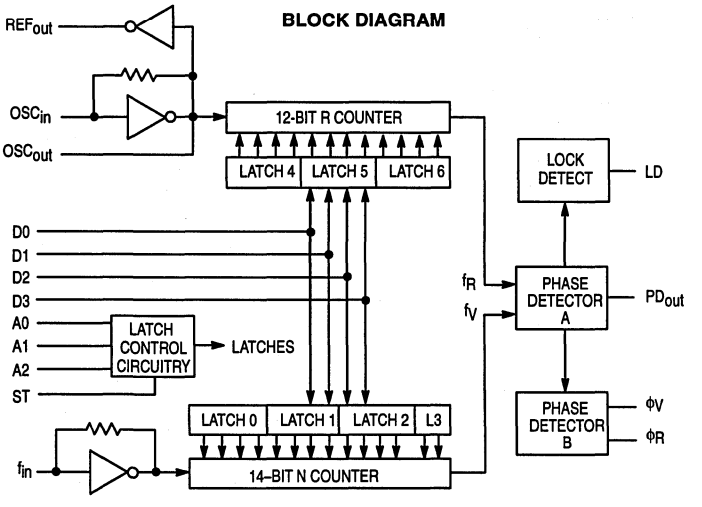


SOG PACKAGE



NC = NO CONNECTION

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

† Power Dissipation Temperature:
Plastic DIP: −12 mW/°C from 65 to 85°C
SOG Package: −7.0 mW/°C from 65 to 85°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high-impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull-up devices. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Conditions	V_{DD}	−40°C		25°C		+85°C		Unit
			V	Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage Range		—	3.0	9.0	3.0	9.0	3.0	9.0	V
I_{ss}	Dynamic Supply Current	$f_{in} = OSC_{in}$ = 10 MHz, 1 Vp-p ac-coupled sine wave R = 128, A = 32, N = 128	3.0 5.0 9.0	— — —	3.5 10 30	— — —	3.0 7.5 24	— — —	3.0 7.5 24	mA
I_{SS}	Quiescent Supply Current	$V_{in} = V_{DD}$ or V_{SS} I_{out} = 0 µA	3.0 5.0 9.0	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	µA
V_{in}	Input Voltage — f_{in}, OSC_{in}	Input ac-coupled sine wave	—	500	—	500	—	500	—	mVp-p
V_{IL}	Low-Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \ge 2.1$ V Input $V_{out} \ge 3.5$ V dc-coupled $V_{out} \ge 6.3$ V square wave	3.0 5.0 9.0	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
V_{IH}	High-Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \le 0.9$ V Input $V_{out} \le 1.5$ V dc-coupled $V_{out} \le 2.7$ V square wave	3.0 5.0 9.0	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
V_{IL}	Low-Level Input Voltage — except f_{in}, OSC_{in}		3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}	High-Level Input Voltage — except f_{in}, OSC_{in}		3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
I_{in}	Input Current (f_{in}, OSC_{in})	$V_{in} = V_{DD}$ or V_{SS}	9.0	±2.0	±50	±2.0	±25	±2.0	±22	µA
I_{IL}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{SS}$	9.0	—	−0.3	—	−0.1	—	−1.0	µA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{DD}$	9.0	—	0.3	—	0.1	—	1.0	µA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF
V_{OL}	Low-Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{DD}$	3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High-Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{SS}$	3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
V_{OL}	Low-Level Output Voltage — Other Outputs	$I_{out} \approx 0$ µA	3.0 5.0 9.0	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V

(continued)

ELECTRICAL CHARACTERISTICS (continued) (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Conditions	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Max	+85°C Min	+85°C Max	Unit
V_{OH}	High-Level Output Voltage—Other Outputs	$I_{out} \approx 0$ µA	3.0 5.0 9.0	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
I_{OL}	Low-Level Sinking Current—Lock Detect	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	3.0 5.0 9.0	0.25 0.64 1.3	— — —	0.2 0.51 1.0	— — —	0.15 0.36 0.7	— — —	mA
I_{OH}	High-Level Sourcing Current—Lock Detect	V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	3.0 5.0 9.0	−0.25 −0.64 −1.3	— — —	−0.2 −0.51 −1.0	— — —	−0.15 −0.36 −0.7	— — —	mA
I_{OL}	Low-Level Sinking Current—Other Outputs	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	3.0 5.0 9.0	0.44 0.64 1.3	— — —	0.35 0.51 1.0	— — —	0.22 0.36 0.7	— — —	mA
I_{OH}	High-Level Sourcing Current—Other Outputs	V_{out} = 2.7 V V_{out} = 4.6 V V_{out} = 8.5 V	3.0 5.0 9.0	−0.44 −0.64 −1.3	— — —	−0.35 −0.51 −1.0	— — —	−0.22 −0.36 −0.7	— — —	mA
I_{OZ}	Output Leakage Current—PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9.0	—	±0.3	—	±0.1	—	±1.0	µA
C_{out}	Output Capacitance—PD_{out}	PD_{out}—Three-State	—	—	10	—	10	—	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	Figure #	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit −40 to +85°C	Unit
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V	1, 5	3.0 5.0 9.0	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, LD	2, 5	3.0 5.0 9.0	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs	2, 5	3.0 5.0 9.0	160 80 60	175 100 65	ns
t_{su}	Minimum Setup Time, Data to ST	3	3.0 5.0 9.0	10 10 10	TBD TBD TBD	ns
t_{su}	Minimum Setup Time, Address to ST	3	3.0 5.0 9.0	25 20 15	TBD TBD TBD	ns
t_h	Minimum Hold Time, Address to ST	3	3.0 5.0 9.0	10 10 10	TBD TBD TBD	ns
t_h	Minimum Hold Time, Data to ST	3	3.0 5.0 9.0	25 20 15	TBD TBD TBD	ns
t_w	Minimum Input Pulse Width, ST	4	3.0 5.0 9.0	40 30 20	TBD TBD TBD	ns

SWITCHING WAVEFORMS

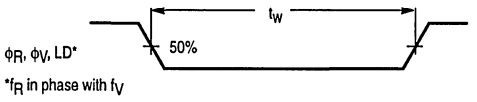


Figure 1.

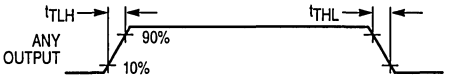


Figure 2.

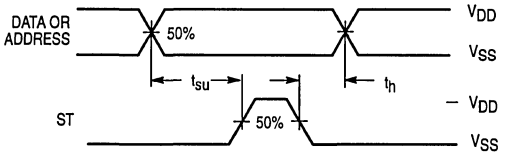


Figure 3.

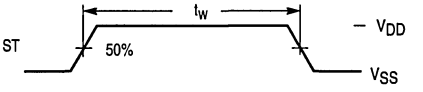
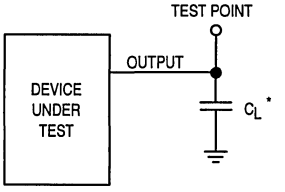


Figure 4.

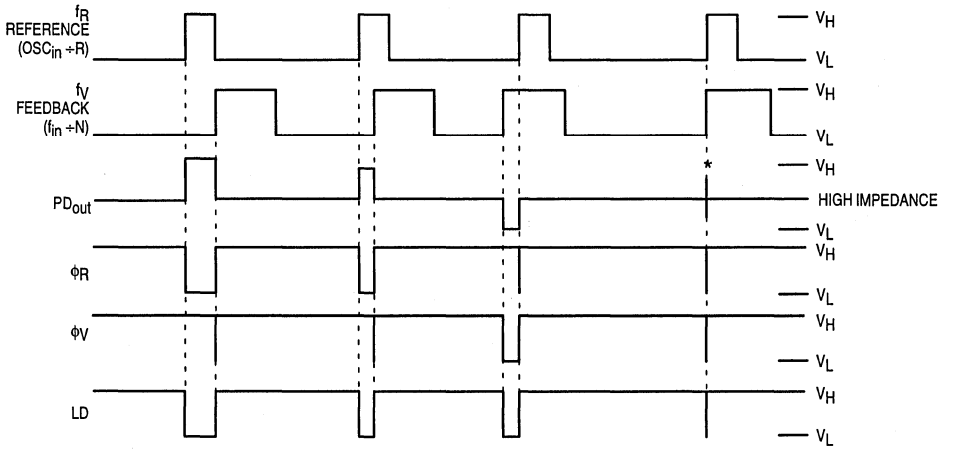


*Includes all probe and jig capacitance.

Figure 5. Test Circuit

FREQUENCY CHARACTERISTICS (Voltages Referenced to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD}	−40°C		25°C		+85°C		Unit
			V	Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mVp-p ac-coupled sine wave	3.0 5.0 9.0	— — —	6.0 15 15	— — —	6.0 15 15	— — —	6.0 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 1.0 Vp-p ac-coupled sine wave	3.0 5.0 9.0	— — —	12 22 25	— — —	12 20 22	— — —	7.0 20 22	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = V_{DD} to V_{SS} dc-coupled square wave	3.0 5.0 9.0	— — —	13 25 25	— — —	12 22 25	— — —	8.0 22 25	MHz



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.
Note: The PD_{out} generates error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor.

Figure 6. Phase/Frequency Detectors and Lock Detector Output Waveforms

PIN DESCRIPTIONS

D0–D3
Data Inputs
Information at these inputs is transferred to the internal latches when the ST input is in the high state. D3 is most significant bit.

f_{in}
Frequency Input
Input to ÷N portion of synthesizer. f_{in} is typically derived from the loop VCO and is ac coupled. For larger amplitude signals (standard CMOS-logic levels) dc coupling may be used.

V_{SS}
Ground
Circuit Ground.

V_{DD}
Positive Power Supply
The positive supply voltage may range from 3.0 to 9.0 V with respect to V_{SS}.

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output
These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal is typically ac-coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

A0–A2
Address Inputs
A0, A1, and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

A2	A1	A0	Selected	Function	D0	D1	D2	D3
0	0	0	Latch 0	÷N Bits	0	1	2	3
0	0	1	Latch 1	÷N Bits	4	5	6	7
0	1	0	Latch 2	÷N Bits	8	9	10	11
0	1	1	Latch 3	÷N Bits	12	13	—	—
1	0	0	Latch 4	Reference Bits	0	1	2	3
1	0	1	Latch 5	Reference Bits	4	5	6	7
1	1	0	Latch 6	Reference Bits	8	9	10	11
1	1	1	—	—	—	—	—	—

ST
Strobe Transfer
The rising edge of strobe transfers data into the addressed latch, the falling edge of strobe latches data into the latch. This pin should normally be held low to avoid loading latches with invalid data.

PD_{out}
Single-Ended Phase Detector Output
Three-state output of phase detector for use as loop error signal.
Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence:
High-Impedance State

LD
Lock Detector Signal
High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

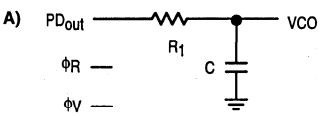
ϕV, ϕR
Phase Detector Outputs
These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).
If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.
If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.
If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

REF_{out}
Buffered Reference Output
Buffered output of on-chip reference oscillator or externally provided reference-input signal.

DESIGN CONSIDERATIONS

PHASE-LOCKED LOOP — LOW-PASS FILTER DESIGN

A)

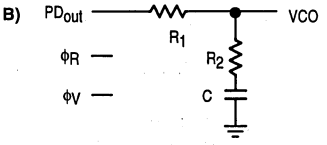


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC+1}$$

B)

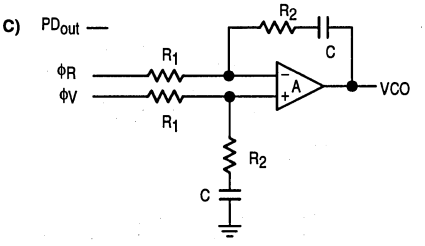


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1+R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2sC+1}{(R_1+R_2)\,sC+1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC+1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley-Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley-Interscience, 1980.

Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York, Wiley-Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley-Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice-Hall, 1983.

Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off-Chip Reference

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 7.

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_o + \frac{C1 \cdot C2}{C1 + C2}$$

where

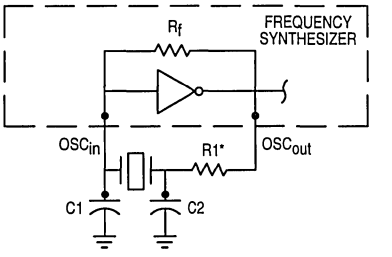
C_{in} = 5.0 pF (see Figure 8)
C_{out} = 6.0 pF (see Figure 8)
C_a = 1.0 pF (see Figure 8)
C_O = the crystal's holder capacitance (see Figure 9)
C1 and C2 = external capacitors (see Figure 7)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 9. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damaging or excessive shift in frequency. R1 in Figure 7 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1=0 Ω).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. (see Table 1).



*May be deleted in certain cases. See text.

Figure 7. Pierce Crystal Oscillator Circuit

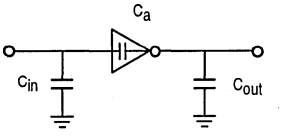
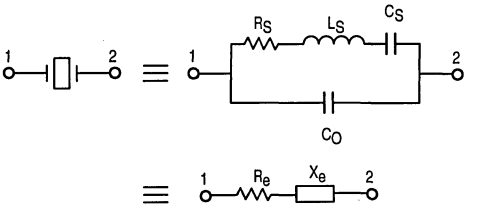


Figure 8. Parasitic Capacitances of the Amplifier



Note: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 9. Equivalent Crystal Networks

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

Note: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

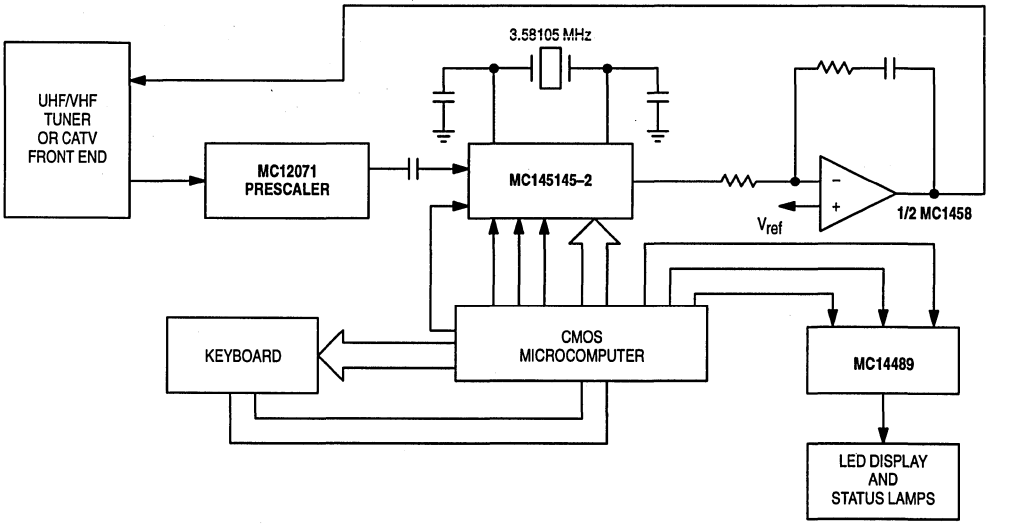


Figure 10. TV/CATV Tuning System

RECOMMENDED READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June, 1969.

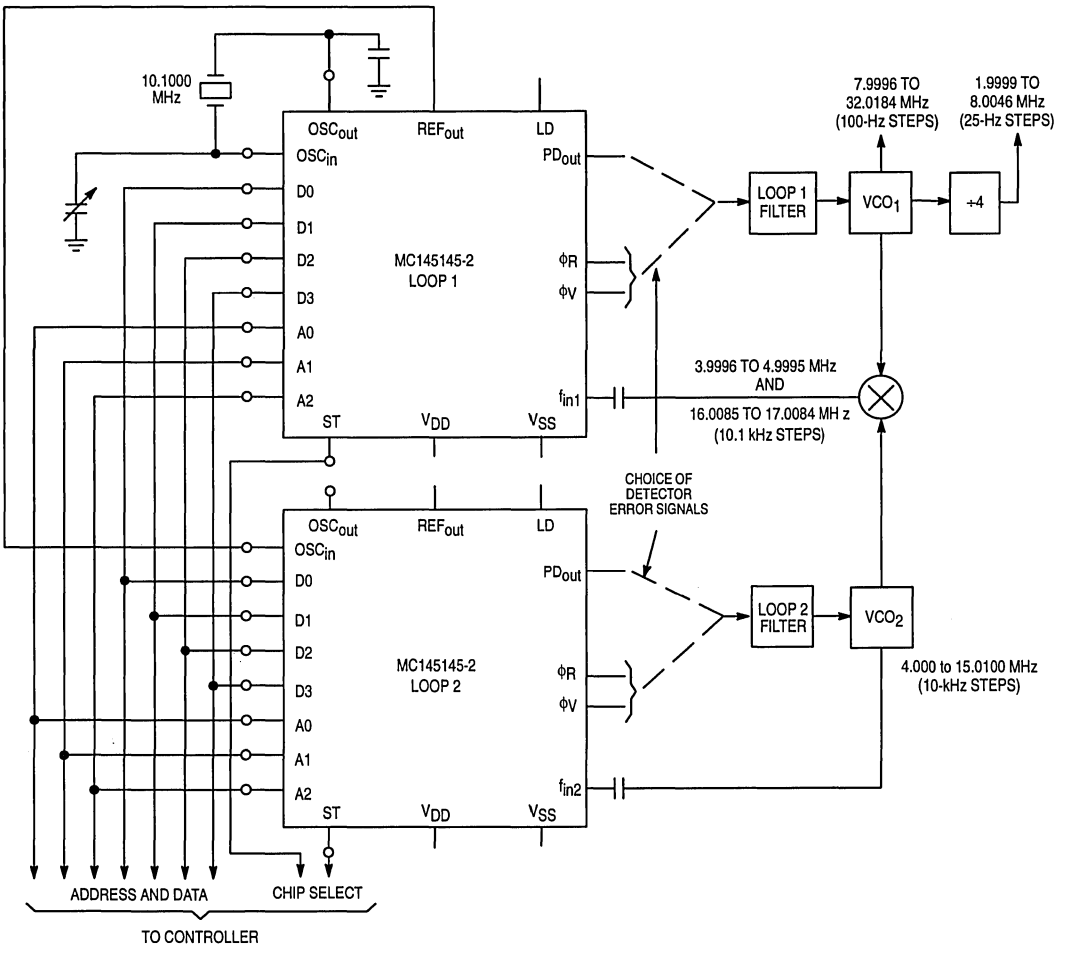
P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

APPLICATIONS

The features of the MC145145-2 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor-controlled system this strobe input is accessed when the PLL is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

The ÷R programmability is used to advantage in Figure 10. Here, the nominal ÷R value is 3667, but by programming small changes in this value, fine tuning is accomplished. Better tuning resolution is achievable with this method than by changing the ÷N, due to the use of the large fixed prescaling value of ÷256 provided by the MC12071.

The two loop synthesizer, in Figure 11, takes advantage of these features to control the phase locked loop with a minimum of dedicated lines while preserving optimal loop performance. Both 25-Hz and 100-Hz steps are provided while the relatively large reference frequencies of 10 kHz or 10.1 kHz are maintained.



NOTES:
1. Table 2 provides program sequence for the ÷N1 (Loop 1) and ÷N2 (Loop 2) Counters.
2. ÷R1 = 1000, f_{R1} = 10.1 kHz, ÷R2 = 1010, f_{R2} = 10 kHz.
3. $f_{VCO1} = N1(f_{R1}) + N2(f_{R2}) = N1(f_{R2} + \Delta f) + N2(f_{R2})$ where $\Delta f = 100$ Hz
4. Other f_{R1} and f_{R2} values may be used with appropriate ÷N1 and ÷N2 changes.

Figure 11. Two Loop Synthesizer Provides 25- and 100-Hz Frequency Steps While Maintaining High Detector Comparison Frequencies of 10 and 10.1 kHz

Table 2. Programming Sequence for Two-Loop Synthesizer of Figure 11

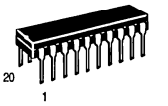
÷N1	f_{in1} (MHz)	÷N2	f_{VCO2} (MHz)	f_{VCO1} (MHz)
"A" 396 ↑ 397 ↓ 495	"B" 3.9996 ↑ 4.0097 ↓ 4.9995	400 ↑ 399 ↓ 301	4.0000 ↑ 3.9900 ↓ 3.0100	7.9996 ↑ 7.9997 ↓ 8.0095
"A"	"B"	401 ↑ 400 ↓ 303	4.0100 ↑ 4.0000 ↓ 3.0200	8.0096 ↑ 8.0097 ↓ 8.0195
"A"	"B"	"C" 402 ↑ 401 ↓ 303	"D" 4.0200 ↑ 4.0100 ↓ 3.0300	8.0196 ↑ 8.0197 ↓ 8.0295
"A"	"B"	↓ 1500	↓ 15.0000	Increasing In 100-Hz Steps ↓ 19.9995
"A"	"B"	1600 ↑ 1599 ↓ 1501	16.0000 ↑ 15.9900 ↓ 15.0100	19.9996 ↑ 19.9997 ↓ 20.0095
"E" 1585 ↑ 1586 ↓ 1684	"F" 16.0085 ↑ 16.0186 ↓ 17.0084	↑	↑	20.0085 ↑ 20.0086 ↓ 20.0184
"E"	"F"	"C"	"D"	20.0185 ↑ 20.0186 ↓ 20.0284
				Increasing In 100-Hz Steps ↓ 32.0084
"E"	"F"			32.0085 ↑ 32.0086 ↓ 32.0184

MC145146-2

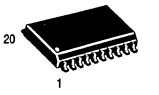
Advance Information

4-Bit Data Bus Input PLL Frequency Synthesizer

Interfaces with Dual-Modulus Prescalers



P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG
CASE 751D

ORDERING INFORMATION

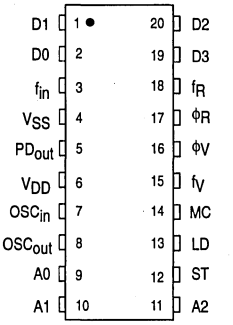
MC145146P2	Plastic DIP
MC145146DW2	SOG Package

The MC145146-2 is programmed by a 4-bit input, with strobe and address lines. The device features consist of a reference oscillator, 12-bit programmable reference divider, digital phase detector, 10-bit programmable divide-by-N counter, 7-bit divide-by-A counter and the necessary latch circuitry for accepting the 4-bit input data. When combined with a loop filter and VCO, the MC145146-2 can provide all of the remaining functions for a PLL frequency synthesizer operating up to the device frequency limit. For higher VCO frequency operation, a down mixer or a dual-modulus prescaler can be used between the VCO and the MC145146-2.

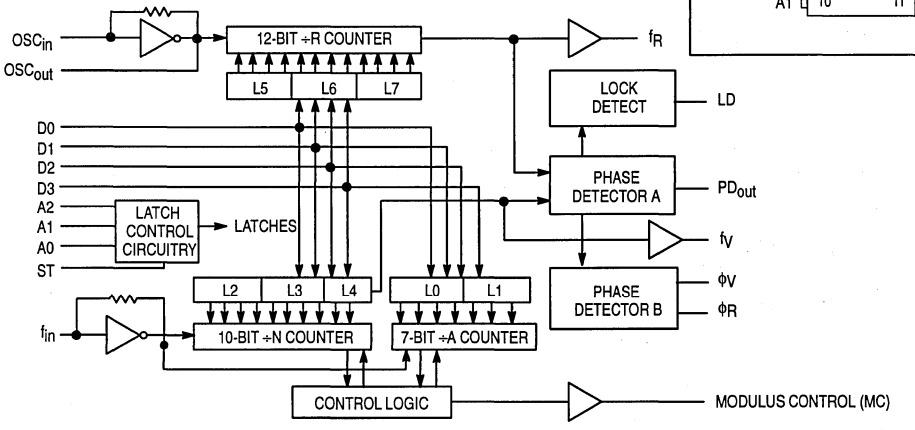
The MC145146-2 is an improved performance drop-in replacement for the MC145146-1. Power consumption has decreased and ESD and latch-up performance have improved.

- General Purpose Applications
  - CATV — TV Tuning
  - AM/FM Radios — Scanning Receivers
  - Two Way Radios — Amateur Radio
- Low Power Consumption Through the Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Programmable Reference Divider for Values Between 3 and 4095
- On- or Off-Chip Reference Oscillator Operation
- Dual-Modulus 4-Bit Data Bus Programming
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options:
  - Single Ended (Three State)
  - Double Ended
- Chip Complexity: 5,692 FETs or 1,423 Equivalent Gates

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descrip-
† tions section.

Power Dissipation Temperature Derating:
Plastic DIP: −12 mW/°C from 65 to 85°C
SOG Package: −7.0 mW/°C from 65 to 85°C

These devices contain protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high-impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull-up devices. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD}	−40°C		25°C		+85°C		Unit
			V	Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage Range		—	3.0	9.0	3.0	9.0	3.0	9.0	V
I_{ss}	Dynamic Supply Current	f_{in}=OSC_{in}=10 MHz, 1 Vp-p ac-coupled sine wave R=128, A=32, N=128	3.0 5.0 9.0	— — —	3.5 10 30	— — —	3.0 7.5 24	— — —	3.0 7.5 24	mA
I_{SS}	Quiescent Supply Current	V_{in}=V_{DD} or V_{SS} I_{out}=0 µA	3.0 5.0 9.0	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	µA
V_{in}	Input Voltage — f_{in}, OSC_{in}	Input ac-coupled sine wave	—	500	—	500	—	500	—	mVp-p
V_{IL}	Low-Level Input Voltage — f_{in}, OSC_{in}	V_{out}≥2.1 V Input dc- V_{out}≥3.5 V coupled V_{out}≥6.3 V square wave	3.0 5.0 9.0	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
V_{IH}	High-Level Input Voltage — f_{in}, OSC_{in}	V_{out}≤0.9 V Input dc- V_{out}≤1.5 V coupled V_{out}≤2.7 V square wave	3.0 5.0 9.0	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
V_{IL}	Low-Level Input Voltage — except f_{in}, OSC_{in}		3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}	High-Level Input Voltage — except f_{in}, OSC_{in}		3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
I_{in}	Input Current (f_{in}, OSC_{in})	V_{in}=V_{DD} or V_{SS}	9.0	±2.0	±50	±2.0	±25	±2.0	±22	µA
I_{IL}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	V_{in}=V_{SS}	9.0	—	−0.3	—	−0.1	—	−1.0	µA
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	V_{in}=V_{DD}	9.0	—	0.3	—	0.1	—	1.0	µA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF

(continued)

ELECTRICAL CHARACTERISTICS—continued (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD}	−40°C		25°C		+85°C		Unit
			V	Min	Max	Min	Max	Min	Max	
V_{OL}	Low-Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{DD}$	3.0 5.0 9.0	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High-Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{SS}$	3.0 5.0 9.0	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
V_{OL}	Low-Level Output Voltage — Other Outputs	$I_{out} \approx 0$ µA	3.0 5.0 9.0	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	High-Level Output Voltage — Other Outputs	$I_{out} \approx 0$ µA	3.0 5.0 9.0	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
I_{OL}	Low-Level Sinking Current — Modulus Control (MC)	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3.0 5.0 9.0	1.3 1.9 3.8	— — —	1.1 1.7 3.3	— — —	0.66 1.08 2.1	— — —	mA
I_{OH}	High-Level Sourcing Current — Modulus Control (MC)	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3.0 5.0 9.0	−0.6 −0.9 −1.5	— — —	−0.5 −0.75 −1.25	— — —	−0.3 −0.5 −0.8	— — —	mA
I_{OL}	Low-Level Sinking Current — Lock Detect (LD)	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3.0 5.0 9.0	0.25 0.64 1.3	— — —	0.2 0.51 1.0	— — —	0.15 0.36 0.7	— — —	mA
I_{OH}	High-Level Sourcing Current — Lock Detect (LD)	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3.0 5.0 9.0	−0.25 −0.64 −1.3	— — —	−0.2 −0.51 −1.0	— — —	−0.15 −0.36 −0.7	— — —	mA
I_{OL}	Low-Level Sinking Current — Other Outputs	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3.0 5.0 9.0	0.44 0.64 1.3	— — —	0.35 0.51 1.0	— — —	0.22 0.36 0.7	— — —	mA
I_{OH}	High-Level Sourcing Current — Other Outputs	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3.0 5.0 9.0	−0.44 −0.64 −1.3	— — —	−0.35 −0.51 −1.0	— — —	−0.22 −0.36 −0.7	— — —	mA
I_{OZ}	Output Leakage Current — PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9.0	—	±0.3	—	±0.1	—	±1.0	µA
C_{out}	Output Capacitance — PD_{out}	PD_{out} — Three-State	—	—	10	—	10	—	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	Figure #	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit −40°C to +85°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, f_{in} to MC	1, 6	3.0 5.0 9.0	110 60 35	120 70 40	ns
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V	2, 6	3.0 5.0 9.0	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}	Maximum Output Transition Time, MC	3, 6	3.0 5.0 9.0	115 60 40	115 75 60	ns
t_{THL}	Maximum Output Transition Time, MC	3, 6	3.0 5.0 9.0	60 34 30	70 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, LD	3, 6	3.0 5.0 9.0	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs	3, 6	3.0 5.0 9.0	160 80 60	175 100 65	ns
t_{su}	Minimum Set-Up Time, Data to ST	4	3.0 5.0 9.0	10 10 10	TBD TBD TBD	ns
t_{su}	Minimum Set-Up Time, Address to ST	4	3.0 5.0 9.0	25 20 15	TBD TBD TBD	ns
t_h	Minimum Hold Time, Address to ST	4	3.0 5.0 9.0	10 10 10	TBD TBD TBD	ns
t_h	Minimum Hold Time, Data to ST	4	3.0 5.0 9.0	25 20 15	TBD TBD TBD	ns
t_w	Minimum Input Pulse Width, ST	5	3.0 5.0 9.0	40 30 20	TBD TBD TBD	ns

SWITCHING WAVEFORMS

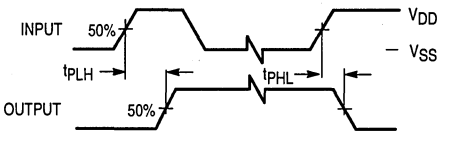


Figure 1.

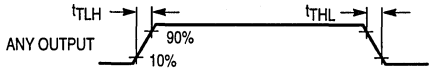


Figure 3.

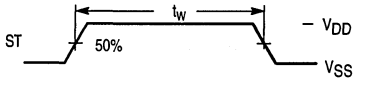


Figure 5.

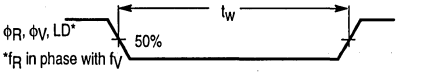


Figure 2.

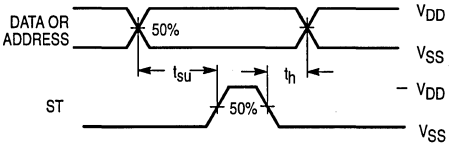
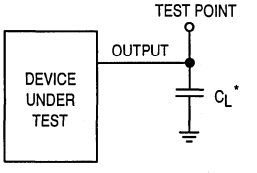


Figure 4.

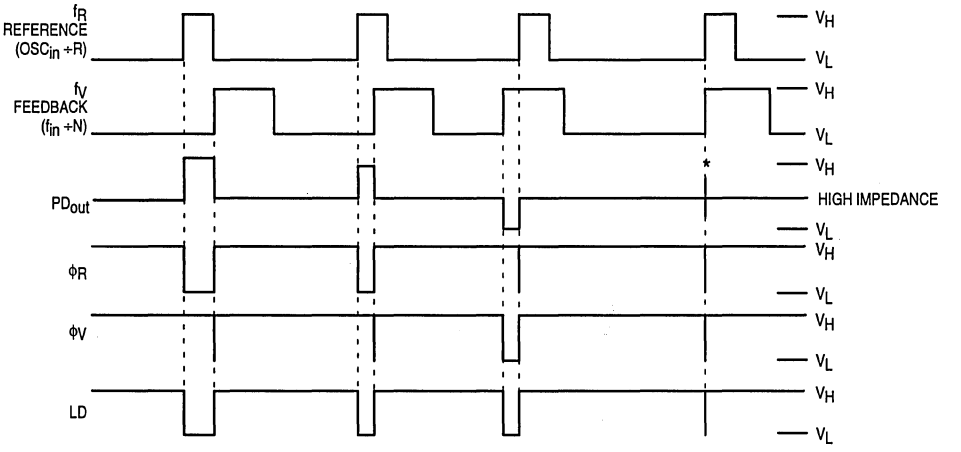


*Includes all probe and jig capacitance.

Figure 6. Test Circuit

FREQUENCY CHARACTERISTICS (Voltages Referenced to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise specified)

Symbol	Parameter	Test Condition	V_{DD}	−40°C		25°C		+ 85°C		Unit
			V	Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R≥8, A≥0, N≥8 V_{in} = 500 mVp-p ac-coupled sine wave	3.0 5.0 9.0	— — —	6.0 15 15	— — —	6.0 15 15	— — —	6.0 15 15	MHz
		R≥8, A≥0, N≥8 V_{in} = 1.0 Vp-p ac-coupled sine wave	3.0 5.0 9.0	— — —	12 22 25	— — —	12 20 22	— — —	7.0 20 22	MHz
		R≥8, A≥0, N≥8 V_{in} = V_{DD} to V_{SS} dc-coupled square wave	3.0 5.0 9.0	— — —	13 25 25	— — —	12 22 25	— — —	8.0 22 25	MHz



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.
Note: The PD_{out} generates error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor.

Figure 7. Phase/Frequency Detectors and Lock Detector Output Waveforms

PIN DESCRIPTIONS

D0–D3
Data Inputs (Pins 2, 1, 20, 19)
Information at these inputs is transferred to the internal latches when the ST input is in the high state. D3 (Pin 19) is the most significant bit.

f_{in}
Frequency Input (Pin 3)
Input to ÷N Portion of Synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into Pin 3. For larger amplitude signals (standard CMOS-logic levels) dc coupling may be used.

V_{SS}
Ground (Pin 4)
Circuit Ground.

PD_{out}
Single-Ended Phase Detector Output (Pin 5)
Three-state output of phase detector for use as loop error signal.
Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence:
High-Impedance State

V_{DD}
Positive Power Supply (Pin 6)
The positive supply voltage may range from 3.0 to 9.0 V with respect to V_{SS}.

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 7 and 8)
These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS-logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

A0–A2
Address Inputs (Pins 9, 10, 11)
A0, A1, and A2 are used to define which latch receives the information on the data input lines. The addresses refer to the following latches:

A2	A1	A0	Selected	Function	D0	D1	D2	D3
0	0	0	Latch 0	÷A Bits	0	1	2	3
0	0	1	Latch 1	÷A Bits	4	5	6	—
0	1	0	Latch 2	÷N Bits	0	1	2	3
0	1	1	Latch 3	÷N Bits	4	5	6	7
1	0	0	Latch 4	÷N Bits	8	9	—	—
1	0	1	Latch 5	Reference Bits	0	1	2	3
1	1	0	Latch 6	Reference Bits	4	5	6	7
1	1	1	Latch 7	Reference Bits	8	9	10	11

ST
Strobe Transfer (PIn 12)
The rising edge of strobe transfers data into the addressed latch. The falling edge of strobe latches data into the latch. This pin should normally be held low to avoid loading latches with invalid data.

LD
Lock Detector (Pin 13)
High level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

MC
Modulus Control (Pin 14)
Signal generated by the on-chip control logic circuitry for controlling an external dual-modulus prescaler. The modulus control level is low at the beginning of a count cycle and remains low until the ÷A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷N counter has counted the rest of the way down from its programmed value (N–A additional counts since both ÷N and ÷A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P+A where P and P+1 represent the dual-modulus prescaler divide values respectively for high and low modulus control levels; N the number programmed into the ÷N counter and A the number programmed into the ÷A counter.

f_V
÷N Counter Output (Pin 15)
This pin is the output of the ÷N counter that is internally connected to the phase detector input. With this output available, the ÷N counter can be used independently.

ϕV, ϕR
Phase Detector Outputs (Pins 16 and 17)
These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

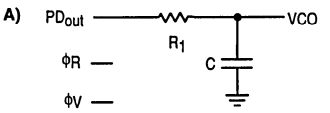
If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

f_R
÷R Counter Output (Pin 18)
This is the output of the ÷R counter that is internally connected to the phase detector input. With this output available, the ÷R counter can be used independently.

DESIGN CONSIDERATIONS

PHASE-LOCKED LOOP — LOW-PASS FILTER DESIGN

A)

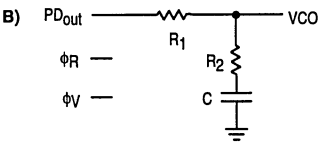


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC+1}$$

B)

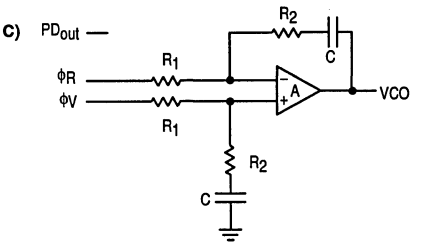


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1+R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2sC+1}{(R_1+R_2)\,sC+1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC+1}{R_1sC}$$

NOTE: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \approx 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley-Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley-Interscience, 1980.

Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York, Wiley-Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley-Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice-Hall, 1983.

Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers. The most desirable is discussed first.

Use Of A Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 µA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design An Off-chip Reference

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

Use Of The On-chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 8.

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_o + \frac{C1 \bullet C2}{C1 + C2}$$

where

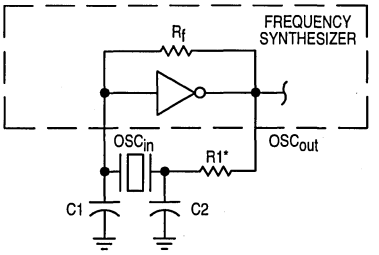
C_{in} = 5.0 pF (see Figure 9)
C_{out} = 6.0 pF (see Figure 9)
C_a = 1.0 pF (see Figure 9)
C_O = the crystal's holder capacitance (see Figure 10)
C1 and C2=external capacitors (see Figure 8)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 10. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damaging or excessive shift in frequency. R1 in Figure 8 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1=0 ohms).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 1.



*May be deleted in certain cases. See text.

Figure 8. Pierce Crystal Oscillator Circuit

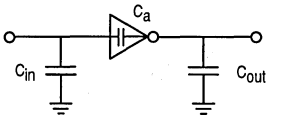
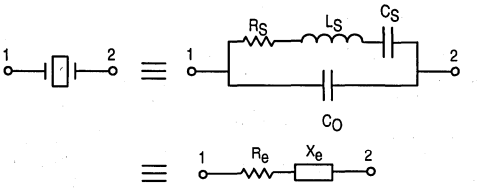


Figure 9. Parasitic Capacitances of the Amplifier



Note: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 10. Equivalent Crystal Networks

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

Note: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

RECOMMENDED READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

DUAL-MODULUS PRESCALING

OVERVIEW

The technique of dual-modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single-modulus) divider is used for the prescaler.

In dual-modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P+1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual-modulus frequency synthesizers contain this feature and can be used with a variety of dual-modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P+1 divide values in the range of ÷3/÷4 to ÷128/÷129 can be controlled by most Motorola frequency synthesizers.

Several dual-modulus prescaler approaches suitable for use with the MC145146-2 are:

MC12009	÷5/÷6	440 MHz
MC12011	÷8/÷9	500 MHz
MC12013	÷10/÷11	500 MHz
MC12015	÷32/÷33	225 MHz
MC12016	÷40/÷41	225 MHz
MC12017	÷64/÷65	225 MHz
MC12018	÷128/÷129	520 MHz
MC12022A	÷64/65 or ÷128/129	1.1 GHz
MC12032A	÷64/65 or ÷128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application, i.e.

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P+A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P+1 are the two selectable divide ratios available in the dual-modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from zero through P−1 for a particular value N in the ÷ N counter. N is then incremented to N+1 and the ÷ A is sequenced from 0 through P−1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters. The constraint $N \geq A$ always applies. If $A_{max} = P-1$, then $N_{min} \geq P-1$. Then $N_{Tmin} = (P-1)P+A$ or $(P-1)P$ since A is free to assume the value of 0.

$$N_{Tmax} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual-modulus prescaler output must go from low to high after each group of P or P+1 input cycles. The prescaler should divide by P when its modulus control line is high and by P+1 when its modulus control is low.

For the maximum frequency into the prescaler (f_{VCO} max), the value used for P must be large enough such that:

1. f_{VCO} max divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual-modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the ÷N and ÷A counters treated in the following manner:

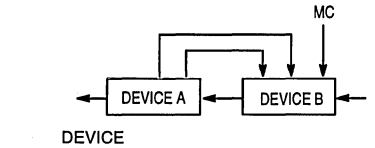
1. Assume the ÷A counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order ÷A counter bits above "a" to 0.
3. Assume the ÷N counter and the ÷A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n+a bits in length (n = number of divider stages in the ÷N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷N and the LSB is to correspond to the LSB of ÷A. The system divide value, N_T, now results when the value of N_T in binary is used to program the "new" n+a bit counter.

By using the two devices, several dual-modulus values are achievable (shown in Figure 11).

APPLICATIONS

The features of the MC145146-2 permit bus operation with a dedicated wire needed only for the strobe input. In a microprocessor-controlled system this strobe input is accessed when the phase lock loop is addressed. The remaining data and address inputs will directly interface to the microprocessor's data and address buses.

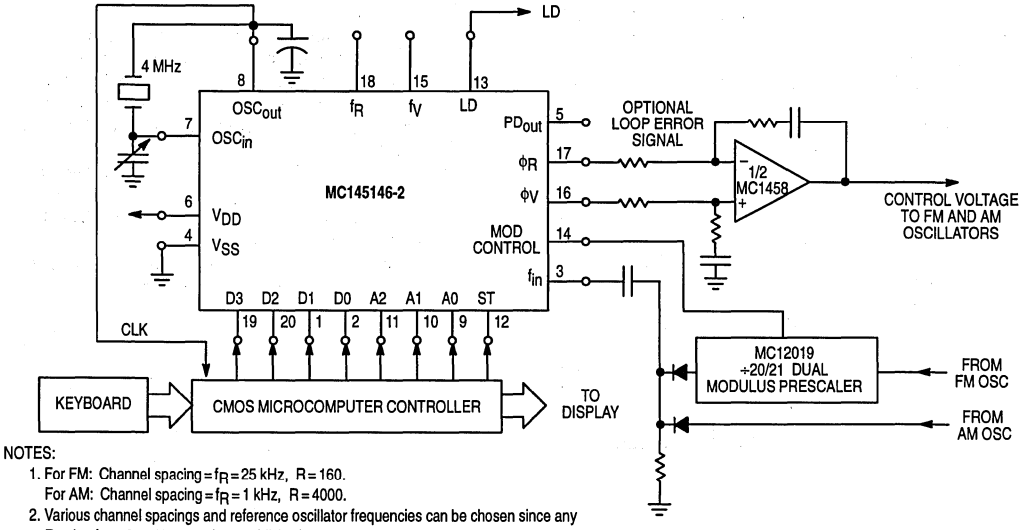
The device architecture allows the user to establish any integer reference divide value between 3 and 4095. The wide selection of +R values permits a high degree of flexibility in choosing the reference oscillator frequency. As a result the reference oscillator can frequently be chosen to serve multiple system functions such as a second local oscillator in a receiver design or a microprocessor system clock. Typical applications that take advantage of these MC145146-2 features including the dual modulus capability are shown in Figures 12, 13, and 14.



DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷20/÷21	÷32/÷33	÷40/÷41
MC10138	÷50/÷51	÷80/÷81	÷100/÷101
MC10154	÷40/÷41 OR ÷80/÷81	÷64/÷65 OR ÷128/÷129	÷80/÷81

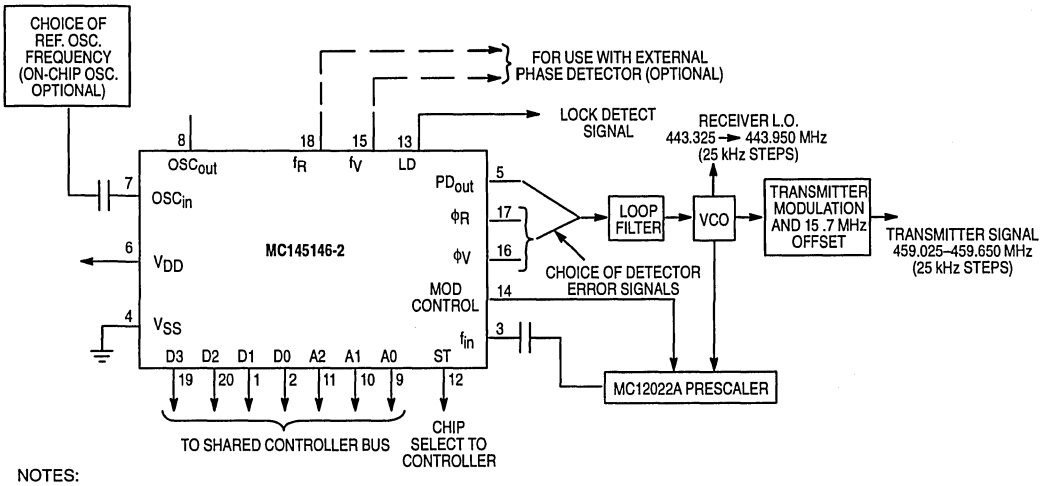
NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

Figure 11. Dual Modulus Values



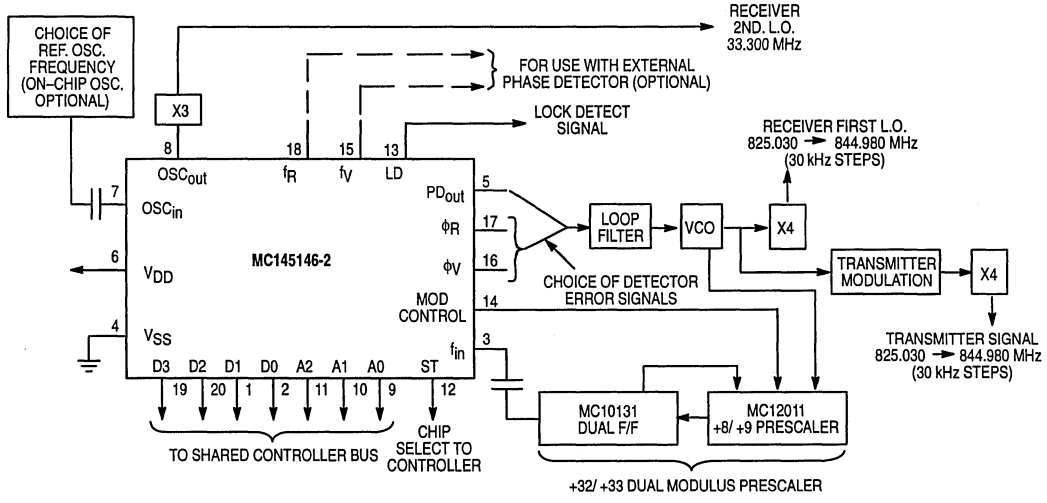
NOTES:
1. For FM: Channel spacing = f_R = 25 kHz, R = 160.
   For AM: Channel spacing = f_R = 1 kHz, R = 4000.
2. Various channel spacings and reference oscillator frequencies can be chosen since any R value from 3 to 4095 can be established.
3. Data and address lines are inactive and high impedance when pin 12 is low. Their interface with the controller may therefore be shared with other system functions if desired.

Figure 12. FM/AM Broadcast Radio Synthesizer



NOTES:
1. Receiver I.F. = 10.7 MHz, low side injection.
2. Duplex operation with 5 MHz receive/transmit separation.
3. f_R = 25 kHz, ÷R chosen to correspond with desired reference oscillator frequency.
4. N_{total} = 17,733 to 17,758 = N . P + A; N = 277, A = 5 to 30 for P = 64.

Figure 13. Synthesizer for UHF Mobile Radio Telephone Channels Demonstrates use of the MC145146-2 in Microprocessor/Microcomputer Controlled Systems Operating to Several Hundred MHz



NOTES:
1. Receiver 1st I.F. = 45 MHz, low side injection; Receiver 2nd I.F. = 11.7 MHz , low side injection.
2. Duplex operation with 45 MHz receive/transmit separation.
3. f_R = 7.5 kHz, ÷R = 1480.
4. N_{total} = N . 32 + A = 27,501 to 28,166; N = 859 to 880; A = 0 to 31.
5. Only one implementation is shown. Various other configurations and dual modulus prescaling values to ÷128/÷129 are possible.

Figure 14. 666 Channel, Computer Controlled, Mobile Radio Telephone Synthesizer for 800-MHz Cellular Radio Systems

MC145149

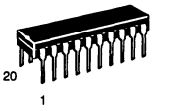
Dual PLL Frequency Synthesizer

Interfaces with Dual-Modulus Prescalers

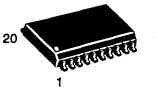
The MC145149 contains two PLL Frequency Synthesizers which share a common serial data port and common reference oscillator. The device contains two 14-stage R counters, two 10-stage N counters, and two 7-stage A counters. All six counters are fully programmable through a serial port. The divide ratios are latched into the appropriate counter latch according to the last data bits (control bits) entered.

When combined with external low-pass filters and voltage controlled oscillators (VCOs), the MC145149 can provide all the remaining functions for two PLL frequency synthesizers operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or dual-modulus prescaler can be used between the VCO and the synthesizer IC.

- Low Power Consumption Through Use of CMOS Technology
- Wide Operating Voltage Range: 3 to 9 V
- Operating Temperature Range: – 40 to + 85°C
- ÷ R Range = 3 to 16,383
- ÷ N Range = 3 to 1023
- ÷ A Range = 0 to 127
- Two "Linearized" Three-State Digital Phase Detectors with No Dead Zone
- Two Lock Detect Signals (LD1 and LD2)
- Two Open-Drain Port Expander Outputs (SW1 and SW2)
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs



P SUFFIX
PLASTIC DIP
CASE 738

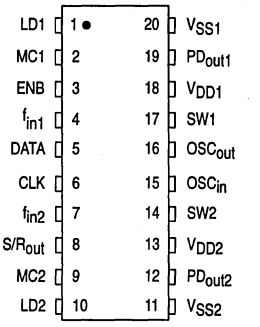


DW SUFFIX
SOG
CASE 751D

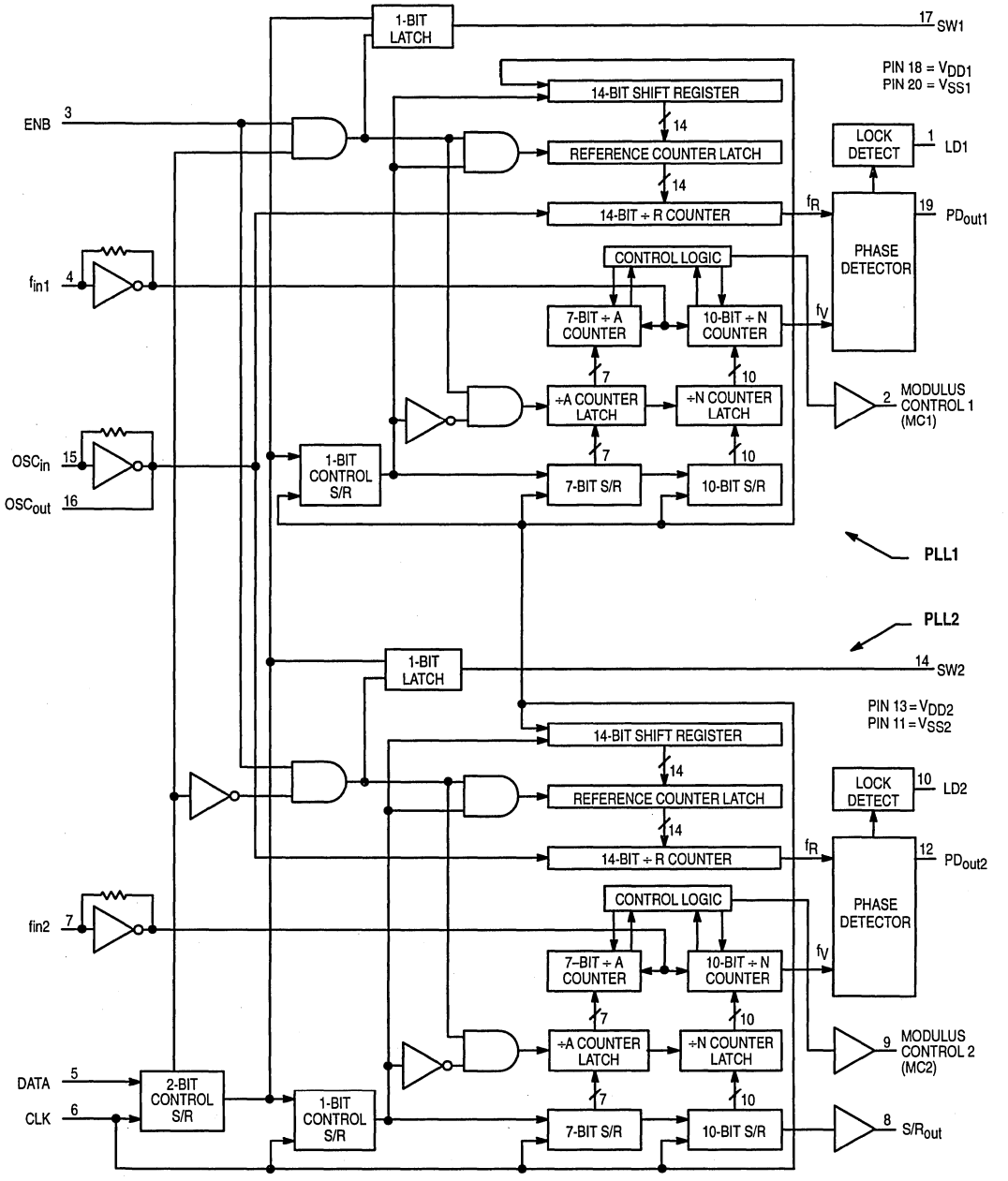
ORDERING INFORMATION

MC145149P	Plastic DIP
MC145149DW	SOG Package

PIN ASSIGNMENT



BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +10	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) except SW1, SW2	−0.5 to V_{DD}+0.5	V
V_{out}	Output Voltage (DC or Transient)—SW1, SW2	−0.5 to 15	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Power Dissipation Temperature Derating:
Plastic DIP: −12 mW/°C from 65 to 85°C
SOG Package: −7 mW/°C from 65 to 85°C

This device contains circuitry to protect against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$ except SW1 and SW2 which may range up to 15 V.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs should be left floating.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Characteristic		V_{DD}	−40°C		25°C		+85°C		Unit
			V	Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage Range		—	3	9	3	9	3	9	V
V_{OL}	Output Voltage V_{in}=0 V or V_{DD} I_{out}=0 µA	0 Level	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}		1 Level	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	
V_{IL}	Input Voltage V_{out}=0.5 V or V_{DD}−0.5 V (All Outputs Except OSC_{out})	0 Level	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}		1 Level	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	
I_{OH}	Output Current—MC1, MC2 V_{out}=2.7 V V_{out}=4.6 V V_{out}=8.5 V	Source	3 5 9	−0.60 −0.90 −1.50	— — —	−0.50 −0.75 −1.25	— — —	−0.30 −0.50 −0.80	— — —	mA
I_{OL}	V_{out}=0.3 V V_{out}=0.4 V V_{out}=0.5 V	Sink	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	
I_{OL}	Output Current—SW1, SW2 V_{out}=0.3 V V_{out}=0.4 V V_{out}=0.5 V	Sink	3 5 9	0.80 1.50 3.50	— — —	0.48 0.90 2.10	— — —	0.24 0.45 1.50	— — —	mA
I_{OH}	Output Current—Other Outputs V_{out}=2.7 V V_{out}=4.6 V V_{out}=8.5 V	Source	3 5 9	−0.44 −0.64 −1.30	— — —	−0.35 −0.51 −1.00	— — —	−0.22 −0.36 −0.70	— — —	mA
I_{OL}	V_{out}=0.3 V V_{out}=0.4 V V_{out}=0.5 V	Sink	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	
I_{in}	Input Current—DATA, CLK, ENB		9	—	±0.3	—	±0.1	—	±1.0	µA
I_{in}	Input Current—f_{in}, OSC_{in}		9	—	±50	—	±25	—	±22	µA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF
C_{out}	Three-State Output Capacitance—PD_{out}		—	—	10	—	10	—	10	pF

(continued)

ELECTRICAL CHARACTERISTICS — continued (Voltages Referenced to V_{SS})

Symbol	Characteristic	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Max	+85°C Min	+85°C Max	Unit
I_{DD}	Quiescent Current V_{in}=0 V or V_{DD} I_{out}=0 µA	3 5 9	— — —	800 1200 1600	— — —	800 1200 1600	—	1600 2400 3200	µA
I_{OZ}	Three-State Leakage Current—PD_{out} V_{out}=0 V or 9 V	9	—	±0.3	—	±0.1	—	±3.0	µA
I_{OZ}	Off-State Leakage Current—SW1, SW2 V_{out}=9 V	9	—	0.3	—	0.1	—	3.0	µA

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic	Figure #	V_{DD} V	Min	Max	Unit
t_{TLH}	Output Rise Time, MC1 and MC2	1, 6	3 5 9	— — —	115 60 40	ns
t_{THL}	Output Fall Time, MC1 and MC2	1, 6	3 5 9	— — —	60 34 30	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time, LD and S/R_{out}	1, 6	3 5 9	— — —	140 80 60	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, f_{in} to MC1 or MC2	2, 6	3 5 9	— — —	125 80 50	ns
t_{su}	Setup Time, DATA to CLK	3	3 5 9	30 20 18	— — —	ns
t_{su}	Setup Time, CLK to ENB	3	3 5 9	70 32 25	— — —	ns
t_h	Hold Time, CLK to DATA	3	3 5 9	12 12 15	— — —	ns
t_{rec}	Recovery Time, ENB to CLK	3	3 5 9	5 10 20	— — —	ns
t_r, t_f	Input Rise and Fall Times, Any Input	4	3 5 9	— — —	5 2 0.5	µs
t_w	Input Pulse Width, ENB and CLK	5	3 5 9	40 35 25	— — —	ns

FREQUENCY CHARACTERISTICS (Voltages Referenced to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Test Conditions	V_{DD}	−40°C		25°C		+85°C		Unit
			V	Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R≥8, A≥0, N≥8 V_{in} = 500 mVp-p ac-coupled sine wave	3 5 9	— — —	6 15 15	— — —	6 15 15	— — —	6 15 15	MHz
		R≥8, A≥0, N≥8 V_{in} = V_{DD} to V_{SS} dc-coupled square wave	3 5 9	— — —	6 15 15	— — —	6 15 15	— — —	6 15 15	MHz

SWITCHING WAVEFORMS

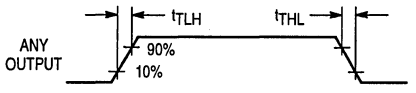


Figure 1.

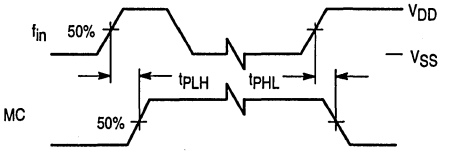


Figure 2.

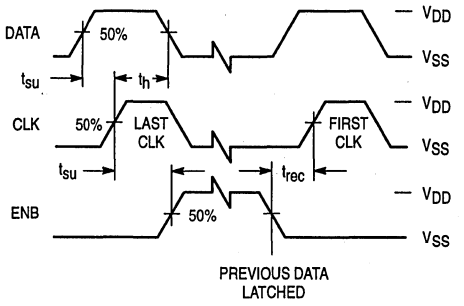


Figure 3.

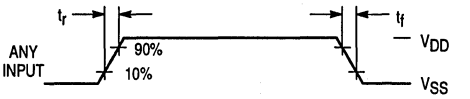


Figure 4.

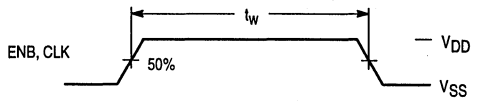


Figure 5.

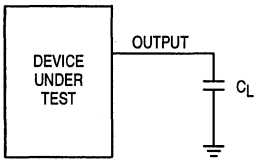


Figure 6.

PIN DESCRIPTIONS

INPUTS

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 15, 16)

These pins form a reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate value must be connected from OSC_{in} and OSC_{out} to ground.

OSC_{in} may also serve as input for an externally-generated reference signal. The signal is typically ac-coupled to OSC_{in}, but for signals with CMOS logic levels, dc coupling may be used. When used with an external reference, OSC_{out} should be left open.

f_{in1}, f_{in2}
Frequency Inputs (Pins 4, 7)

Input frequency from an external VCO output. Each rising-edge signal on f_{in1} decrements the N counter, and when appropriate, the A counter of PLL 1. Similarly, f_{in2} decrements the counters of PLL 2.

These inputs have inverters biased on the linear region which allows ac coupling for signals as low as 500 mVp-p. With square wave signals which swing from V_{SS} to V_{DD}, dc coupling may be used.

DATA, CLK
Data, Clock Inputs (Pins 5, 6)

Shift register data and clock inputs. Each low-to-high transition on the clock pin shifts one bit of data into the on-chip shift registers. Refer to Figure 7 for the following discussion.

The last bit entered is a steering bit that determines which set of latches are activated. A logic high selects the latches for PLL 1. A logic low selects PLL 2.

The second-to-last bit controls the appropriate port expander output, SW1 or SW2. A logic low forces the output low. A logic high forces the output to the high-impedance state.

The third-to-last bit determines which storage latch is activated. A logic low selects the ÷A and ÷N counter latches. A logic high selects the reference counter latch.

When writing to either set of ÷A and ÷N counter latches, 20 clock cycles are typically used. However, if a byte-oriented MCU is utilized, 24 clock cycles may be used with the first 4 bits being "Don't Care."

When writing to either reference counter latch, 17 clock cycles are typically used. However, if a byte-oriented MCU is utilized, 24 clock cycles may be used with the first 7 bits being "Don't Care".

ENB
Latch Enable Input (Pin 3)

A positive pulse on this input transfers data from the shift registers to the selected latches, as determined by the control and steering data bits. A logic low level on this pin allows the user to shift data into the shift registers without affecting the data in the latches or counters. Enable is normally held low and is pulsed high to transfer data into the latches.

OUTPUTS

PD_{out1}, PD_{out2}
Single-Ended Phase Detector Outputs (Pins 19, 12)

Each single-ended (three–state) phase detector output produces a loop error signal that is used with a loop filter to control a VCO (see Figure 8).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

S/R_{out}
Shift Register Output (Pin 8)

This output can be connected to an external shift register to provide band switching or control information. S/R_{out} may also be used to check the counter programming bit stream.

MC1, MC2
Modulus Control Outputs (Pins 2, 9)

Each output generates a signal by the on-chip control logic circuitry for controlling an external dual–modulus prescaler. The modulus control level is low at the beginning of a count cycle and remains low until the ÷A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷N counter has counted the rest of the way down from its programmed value (N-A additional counts since both ÷N and ÷A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters are preset to their respective programmed values, and the above sequence is repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual–modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷N counter, and A the number programmed into the ÷A counter.

Note that when a prescaler is needed, the dual-modulus version offers a distinct advantage. The dual-modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

LD1, LD2
Lock Detect Signals (Pins 1, 10)

Each output is essentially at a high logic level when the corresponding loop is locked (f_R and f_V of the same phase and frequency). Each output pulses low when the corresponding loop is out of lock (see Figure 8).

SW1, SW2
Latched Open-Drain Switch Outputs (Pins 17, 14)

The state of each output is controlled by the "SW STATE" bit shown in Figure 7. If the bit is a logic high, the corresponding SW output assumes the high-impedance state. If the bit is low, the SW output goes low.

To control output SW1, steering bit PLL 1/PLL 2 shown in Figure 7 must be high. To control SW2, bit PLL 1/PLL 2 must be low.

These outputs have an output voltage range of V_{SS} to 15 V.

POWER SUPPLY

V_{DD1}, V_{DD2}
Positive Power Supply (Pins 18, 13)

The most positive power supply potentials. Both of these pins are connected to the substrate of the chip. Therefore, both must be tied to the same voltage potential. This potential may range from 3 to 9 V with respect to the V_{SS} pins.

For optimum performance, V_{DD1} should be bypassed to V_{SS1} and V_{DD2} bypassed to V_{SS2}. That is, two separate bypass capacitors should be utilized.

V_{SS1}, V_{SS2}
Negative Power Supply (Pins 20, 11)

The most negative power supply potentials. Both of these pins should be tied to ground.

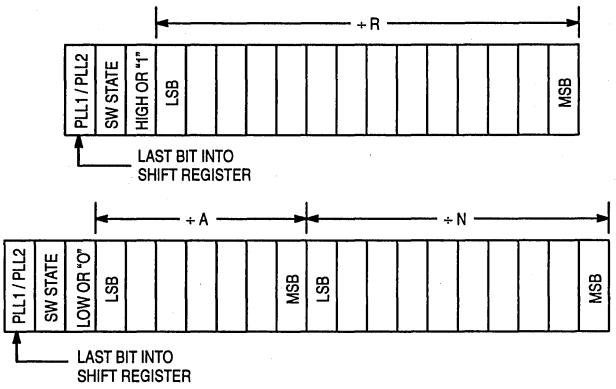
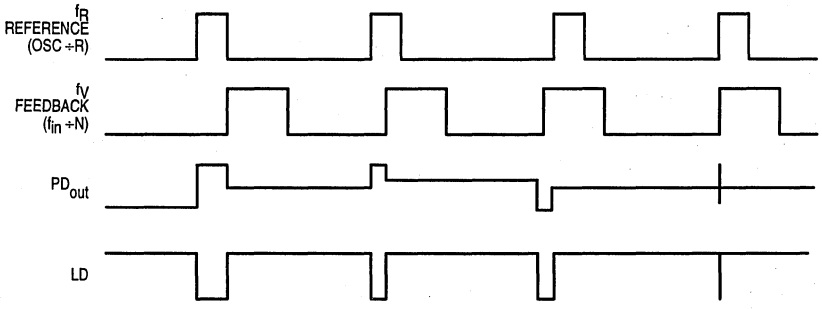
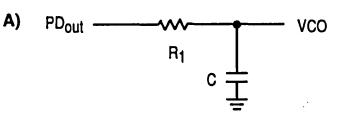


Figure 7. Bit Stream Formats



Note: The PD output state is equal to either V_{DD} or V_{SS} when active. When not active, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor.

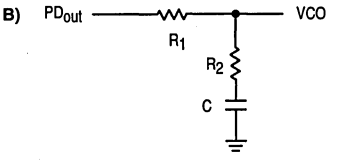
Figure 8. Phase Detector/Lock Detector Output Waveforms



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC+1}$$



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1+R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}} \right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1+R_2)\,sC + 1}$$

DEFINITIONS:

N=Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain)=$V_{DD}/4\pi$ for PD_{out}

K_{VCO} (VCO Gain)= $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design ω_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \approx 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

Figure 9. Phase-Locked Loop Low-Pass Filter Design

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use Of A Hybrid Crystal Oscillator

Commercially available temperature-compensate crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 µA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design An Off-chip Reference

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

Use Of The On-chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_o + \frac{C1 \bullet C2}{C1+C2}$$

where

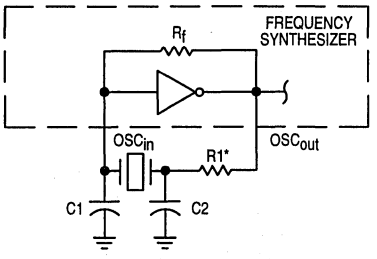
C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C_O = the crystal's holder capacitance (see Figure 12)
C1 and C2 = external capacitors (see Figure 10)

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damaging or excessive shift in frequency. R1 in Figure 10 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1=0 Ω).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize load-ing.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 1).



*May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

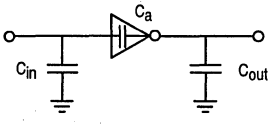
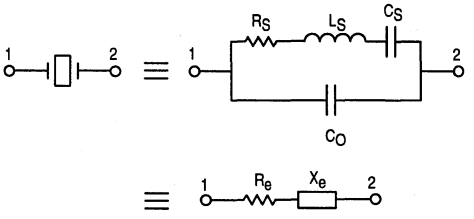


Figure 11. Parasitic Capacitances of the Amplifier



Note: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
Unites States Crystal Corp.	3605 McCart St. Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr. Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St. Orange, CA 92668	(714) 639-7810

Note: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

RECOMMENDED READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

DUAL-MODULUS PRESCALING

OVERVIEW

The technique of dual-modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single-modulus) divider is used for the prescaler.

In dual-modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P+1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual-modulus frequency synthesizers contain this feature and can be used with a variety of dual-modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P+1 divide values in the range of ÷3/÷4 to ÷128/÷129 can be controlled by most Motorola frequency synthesizers.

Several dual-modulus prescaler approaches suitable for use with the MC145149 are:

MC12009	÷5/÷6	440 MHz
MC12011	÷8/÷9	500 MHz
MC12013	÷10/÷11	500 MHz
MC12015	÷32/÷33	225 MHz
MC12016	÷40/÷41	225 MHz
MC12017	÷64/÷65	225 MHz
MC12018	÷128/÷129	520 MHz
MC12022A	÷64/65 or ÷128/129	1.1 GHz
MC12032A	÷64/65 or ÷128/129	2.0 GHz

DESIGN GUIDELINES

The system total divide value, N_{total} (N_T) will be dictated by the application, i.e.,

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \bullet P + A$$

N is the number programmed into the ÷N counter, A is the number programmed into the ÷A counter, P and P+1 are the two selectable divide ratios available in the dual-modulus prescalers. To have a range of N_T values in sequence, the ÷A counter is programmed from 0 through P–1 for a particular value N in the ÷N counter. N is then incremented to N+1 and the ÷A is sequenced from 0 through P–1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷N and ÷A counters.

The constraint $N \geq A$ always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P - 1)\ P + A$ or $(P - 1)\ P$ since A is free to assume the value of 0.

$$N_{Tmax} = N_{max} \bullet P + A_{max}$$

To maximize system frequency capability, the dual-modulus prescaler output must go from low to high after each group of P or P+1 input cycles. The prescaler should divide by P when its modulus control line is high and by P+1 when its modulus control is low.

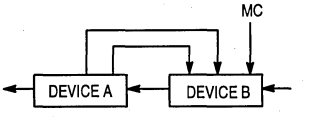
For the maximum frequency into the prescaler (f_{VCOmax}), the value used for P must be large enough such that:

1. f_{VCO} max divided by P may not exceed the frequency capability of f_{in} (input to the ÷N and ÷A counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual-modulus prescaler.
   b. Prescaler setup or release time relative to its modulus control signal.
   c. Propagation time from f_{in} to the modulus control output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the ÷N and ÷A counters treated in the following manner:

1. Assume the ÷A counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order ÷A counter bits above "a" to 0.
3. Assume the ÷N counter and the ÷A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n+a bits in length (n=number of divider stages in the ÷N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷N and the LSB is to correspond to the LSB of ÷A. The system divide value, N_T, now results when the value of N_T in binary is used to program the "new" n+a bit counter.

By using the two devices, several dual-modulus values are achievable:



DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷20/÷21	÷32/÷33	÷40/÷41
MC10138	÷50/÷51	÷80/÷81	÷100/÷101
MC10154	÷40/÷41 OR ÷80/÷81	÷64/÷65 OR ÷128/÷129	÷80/÷81

NOTE: MC12009, MC12011, and MC12013 are pin equivalent. MC12015, MC12016, and MC12017 are pin equivalent.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

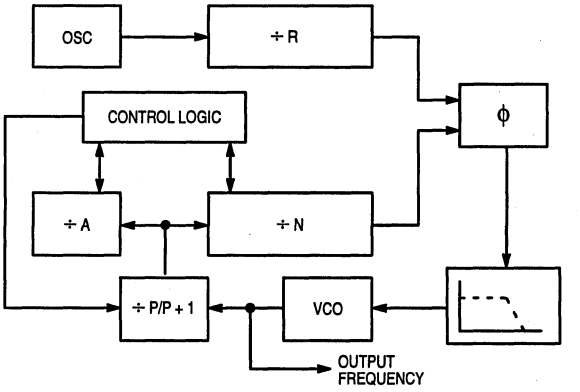
MC145151-2
MC145152-2
MC145155-2
MC145156-2
MC145157-2
MC145158-2

PLL Frequency Synthesizers
CMOS

The devices described in this document are typically used as low-power, phase-locked loop frequency synthesizers. When combined with an external low-pass filter and voltage-controlled oscillator, these devices can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a prescaler can be used between the VCO and the synthesizer IC.

These frequency synthesizer chips can be found in the following and other applications:

CATV	TV Tuning
AM/FM Radios	Scanning Receivers
Two-Way Radios	Amateur Radio



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MC145151-2

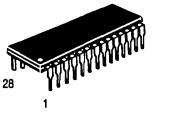
Parallel-Input PLL Frequency Synthesizer

Interfaces with Single-Modulus Prescalers

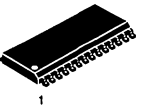
The MC145151-2 is programmed by 14 parallel-input data lines for the N counter and 3 input lines for the R counter. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, and 14-bit programmable divide-by-N counter.

The MC145151-2 is an improved-performance drop-in replacement for the MC145151-1. The power consumption has decreased and ESD and latch-up performance have improved.

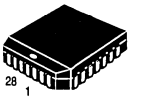
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- ÷ N Counter Output Available
- Single Modulus/Parallel Programming
- 8 User-Selectable ÷ R Values: 8, 128, 256, 512, 1024, 2048, 2410, 8192
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single Ended (Three-State) or Double Ended
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates



P SUFFIX
PLASTIC
CASE 710



DW SUFFIX
SOG
CASE 751F



FN SUFFIX
PLCC
CASE 776

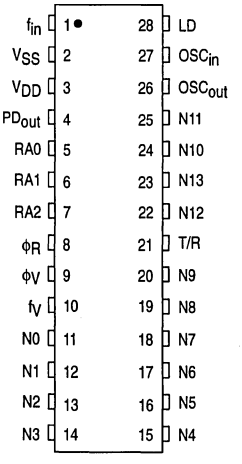
ORDERING INFORMATION

MC145151P2	Plastic DIP
MC145151DW2	SOG Package
MC145151FN2	PLCC Package

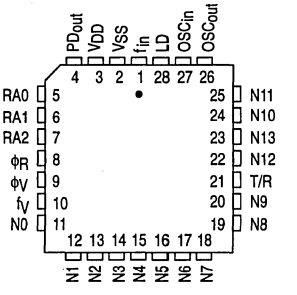
The PLCC (FN suffix) package will be phased out for this device and is NOT RECOMMENDED FOR NEW DESIGNS.

PIN ASSIGNMENTS

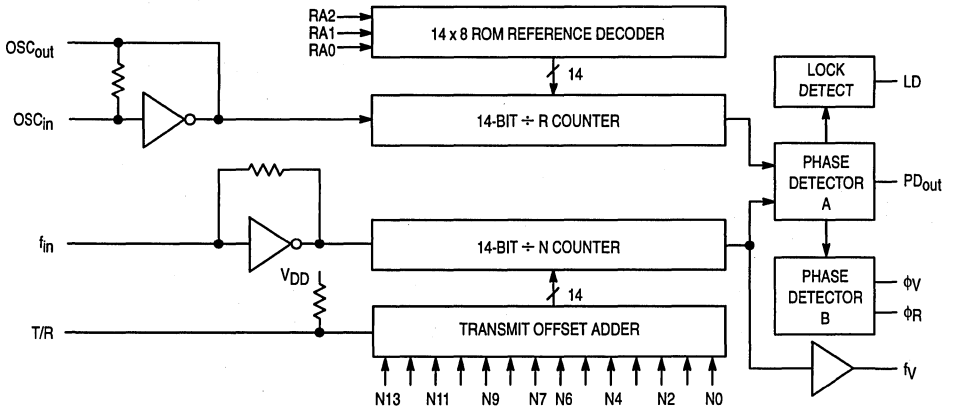
PLASTIC DIP and SOG PACKAGE



PLCC



BLOCK DIAGRAM



NOTE: N0–N13 inputs and inputs RA0, RA1, and RA2 have pull-up resistors that are not shown.

PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 1)

Input to the ÷ N portion of the synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0–RA2
Reference Address Inputs (Pins 5, 6, 7)

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Pull-up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

N0–N11
N Counter Programming Inputs (Pins 11–20, 22–25)

These inputs provide the data that is preset into the ÷ N counter when it reaches the count of zero. N0 is the least significant and N13 is the most significant. Pull-up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

T/R
Transmit/Receive Offset Adder Input (Pin 21)

This input controls the offset added to the data provided at the N inputs. This is normally used for offsetting the VCO frequency by an amount equal to the IF frequency of the transceiver. This offset is fixed at 856 when T/R is low and gives no offset when T/R is high. A pull-up resistor ensures that no connection will appear as a logic 1 causing no offset addition.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output (Pin 4)

Three-state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕV and ϕR).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕ_R, ϕ_V
Phase Detector B Outputs (Pins 8, 9)

These phase detector outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_V
N Counter Output (Pin 10)

This is the buffered output of the ÷ N counter that is internally connected to the phase detector input. With this output available, the ÷ N counter can be used independently.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS

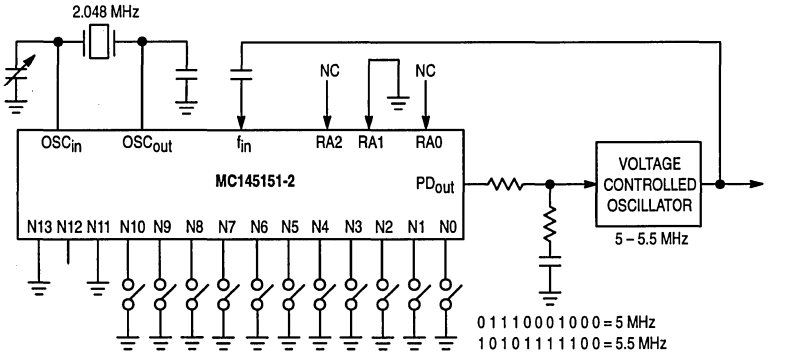
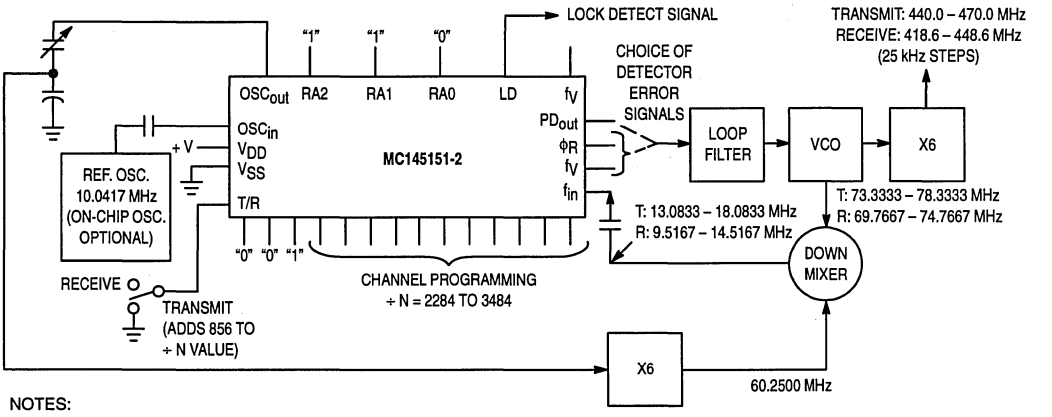


Figure 1. 5 MHz to 5.5 MHz Local Oscillator Channel Spacing = 1 kHz



NOTES:
1. f_R = 4.1667 kHz; ÷ R = 2410; 21.4-MHz low side injection during receive.
2. Frequency values shown are for the 440–470 MHz band. Similar implementation applies to the 406–440 MHz band. For 470–512 MHz, consider reference oscillator frequency X9 for mixer injection signal (90.3750 MHz).

Figure 2. Synthesizer for Land Mobile Radio UHF Bands

Data Sheet Continued on Page 2-556

MC145152-2

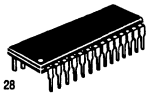
Parallel-Input PLL Frequency Synthesizer

Interfaces with Dual-Modulus Prescalers

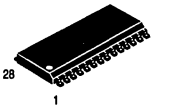
The MC145152-2 is programmed by sixteen parallel inputs for the N and A counters and three input lines for the R counter. The device features consist of a reference oscillator, selectable-reference divider, two-output phase detector, 10-bit programmable divide-by-N counter, and 6-bit programmable ÷ A counter.

The MC145152-2 is an improved-performance drop-in replacement for the MC145152-1. Power consumption has decreased and ESD and latch-up performance have improved.

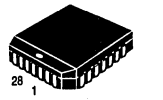
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Lock Detect Signal
- Dual Modulus/Parallel Programming
- 8 User-Selectable ÷ R Values: 8, 64, 128, 256, 512, 1024, 1160, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 63
- Chip Complexity: 8000 FETs or 2000 Equivalent Gates



P SUFFIX
PLASTIC
CASE 710



DW SUFFIX
SOG
CASE 751F



FN SUFFIX
PLCC
CASE 776

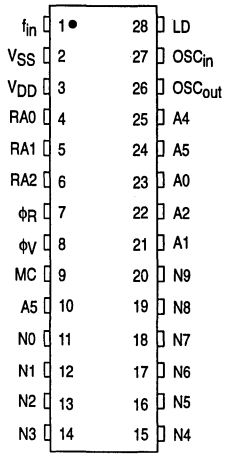
ORDERING INFORMATION

MC145152P2	Plastic DIP
MC145152DW2	SOG Package
MC145152FN2	PLCC Package

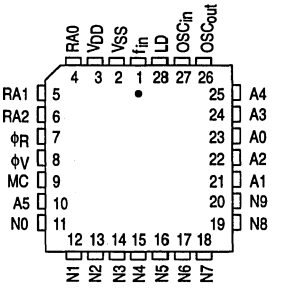
The PLCC (FN suffix) package will be phased out for this device and is NOT RECOMMENDED FOR NEW DESIGNS.

PIN ASSIGNMENTS

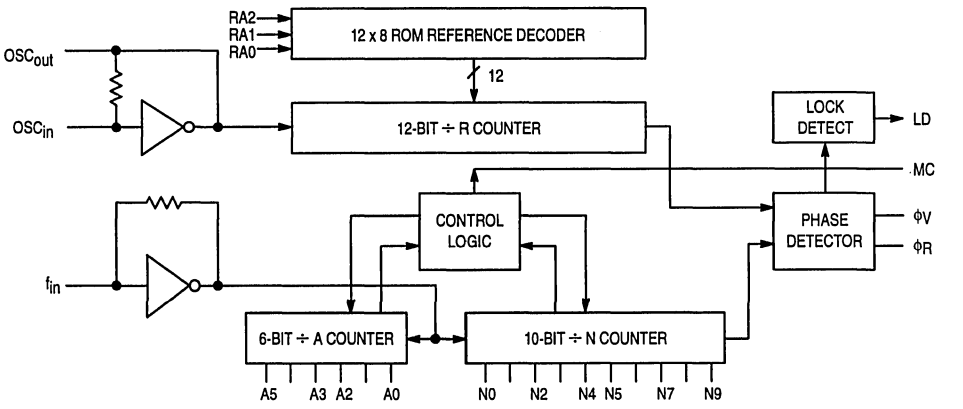
PLASTIC DIP and SOG PACKAGE



PLCC



BLOCK DIAGRAM



NOTE: N0–N9, A0–A5, and RA0–RA2 have pull-up resistors that are not shown.

PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 1)

Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual-modulus prescaler and is ac-coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

RA0, RA1, RA2
Reference Address Inputs (Pins 4, 5, 6)

These three inputs establish a code defining one of eight possible divide values for the total reference divider. The total reference divide values are as follows:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	512
1	0	1	1024
1	1	0	1160
1	1	1	2048

N0–N9
N Counter Programming Inputs (Pins 11–20)

The N inputs provide the data that is preset into the ÷ N counter when it reaches the count of 0. N0 is the least significant digit and N9 is the most significant. Pull-up resistors ensure that inputs left open remain at a logic 1 and require only a SPST switch to alter data to the zero state.

A0–A5
A Counter Programming Inputs
(Pins 23, 21, 22, 24, 25, 10)

The A inputs define the number of clock cycles of f_{in} that require a logic 0 on the MC output (see ***Dual-Modulus Prescaling*** section). The A inputs all have internal pull-up resistors that ensure that inputs left open will remain at a logic 1.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 27, 26)

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

ϕR, ϕV
Phase Detector B Outputs (Pins 7, 8)

These phase detector outputs can be combined externally for a loop-error signal.

If the frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

MC
Dual-Modulus Prescale Control Output (Pin 9)

Signal generated by the on-chip control logic circuitry for controlling an external dual-modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first

portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual-modulus prescaler divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

LD
Lock Detector Output (Pin 28)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). Pulses low when loop is out of lock.

POWER SUPPLY PINS

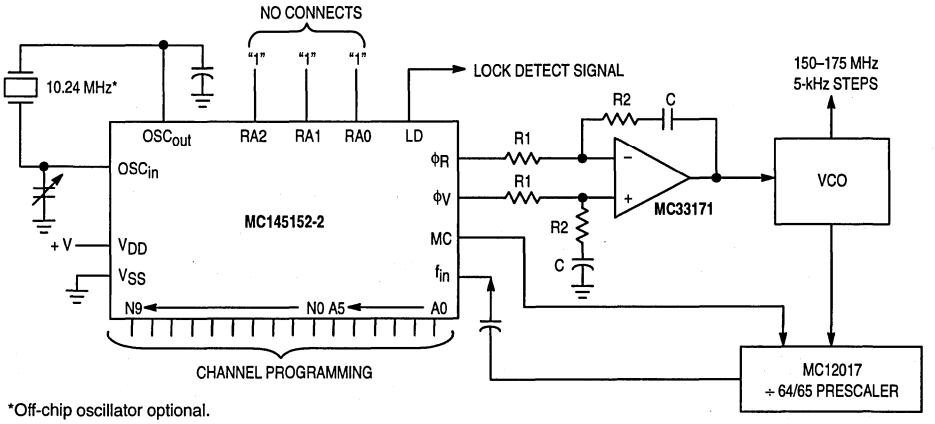
V_{DD}
Positive Power Supply (Pin 3)

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply (Pin 2)

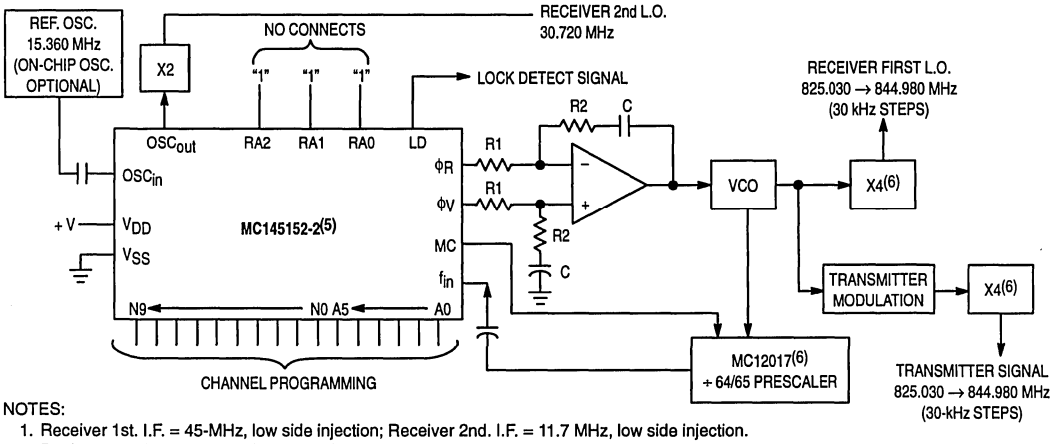
The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



*Off-chip oscillator optional.

Figure 1. Synthesizer for Land Mobile Radio VHF Bands



NOTES:

1. Receiver 1st. I.F. = 45-MHz, low side injection; Receiver 2nd. I.F. = 11.7 MHz, low side injection.
2. Duplex operation with 45-MHz receiver/transmit separation.
3. f_R = 7.5 kHz; ÷ R = 2048.
4. N_{total} = N • 64 + A = 27501 to 28166; N = 429 to 440; A = 0 to 63.
5. MC145158-2 may be used where serial data entry is desired.
6. High frequency prescalers (e.g., MC12018 [520 MHz] and MC12022 [1 GHz]) may be used for higher frequency VCO and f_{ref} implementations.

Figure 2. 666-Channel, Computer-Controlled, Mobile Radiotelephone Synthesizer for 800-MHz Cellular Radio Systems

Data Sheet Continued on Page 2-556

MC145155-2

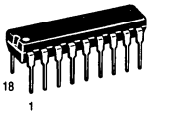
Serial-Input PLL Frequency Synthesizer

Interfaces with Single-Modulus Prescalers

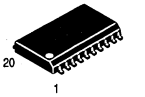
The MC145155-2 is programmed by a clocked, serial input, 16-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 14-bit programmable divide-by-N counter, and the necessary shift register and latch circuitry for accepting serial input data.

The MC145155-2 is an improved-performance drop-in replacement for the MC145155-1. Power consumption has decreased and ESD and latch-up performance have improved.

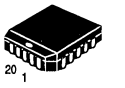
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- 8 User-Selectable ÷ R Values: 16, 512, 1024, 2048, 3668, 4096, 6144, 8192
- Single Modulus/Serial Programming
- ÷ N Range = 3 to 16383
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single Ended (Three-State) or Double Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC
CASE 707



DW SUFFIX
SOG
CASE 751D



FN SUFFIX
PLCC
CASE 775

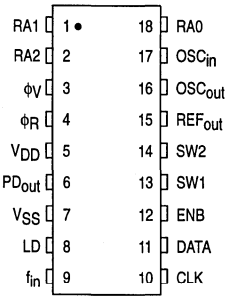
ORDERING INFORMATION

MC145155P2	Plastic DIP
MC145155DW2	SOG Package
MC145155FN2	PLCC Package

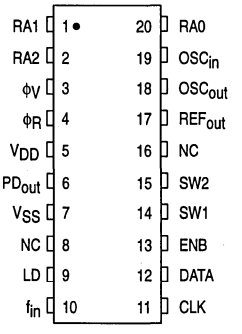
The PLCC (FN suffix) package will be phased out for this device and is NOT RECOMMENDED FOR NEW DESIGNS.

PIN ASSIGNMENTS

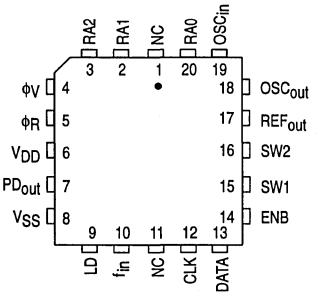
PLASTIC DIP



SOG PACKAGE

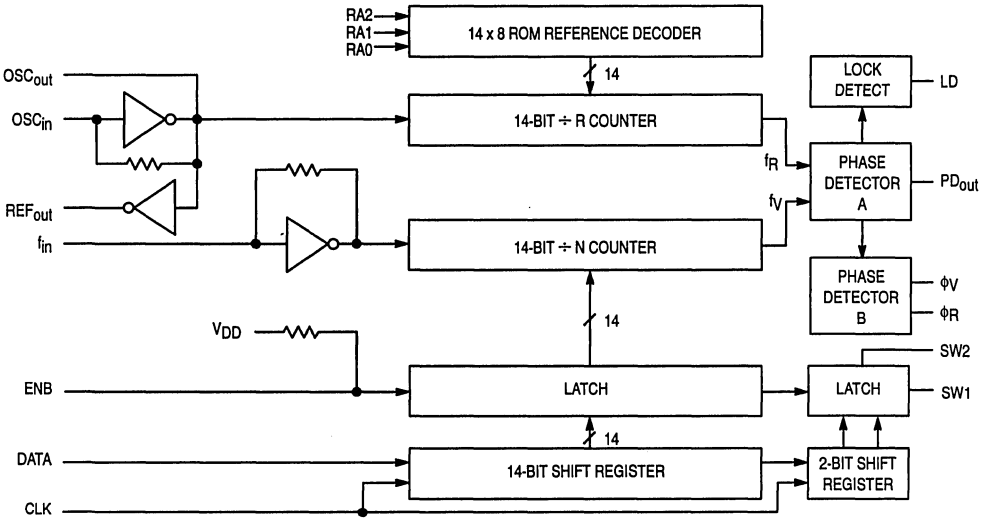


PLCC PACKAGE



NC = NO CONNECTION

BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input

Input to the ÷ N portion of the synthesizer. f_{in} is typically derived from loop VCO and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

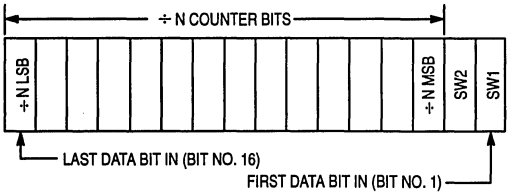
RA0, RA1, RA2
Reference Address Inputs

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	16
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	3668
1	0	1	4096
1	1	0	6144
1	1	1	8192

CLK, DATA
Shift Register Clock, Serial Data Inputs

Each low-to-high transition clocks one bit into the on-chip 16-bit shift register. The Data input provides programming information for the 14-bit ÷ N counter and the two switch signals SW1 and SW2. The entry format is as follows:



ENB
Latch Enable Input

When high (1), ENB transfers the contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low (0), ENB inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on-chip pull-up establishes a continuously high level for ENB when no external signal is applied. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output

Three-state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕV and ϕR).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence:
High-Impedance State

ϕR, ϕV
Phase Detector B Outputs

These phase detector outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

LD
Lock Detector Output

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). LD pulses low when loop is out of lock.

SW1, SW2
Band Switch Outputs

SW1 and SW2 provide latched open-drain outputs corresponding to data bits numbers one and two. These outputs can be tied through external resistors to voltages as high as 15 Vdc, independent of the V_{DD} supply voltage. These are typically used for band switch functions. A logic 1 causes the output to assume a high-impedance state, while a logic 0 causes the output to be low.

REF_{out}
Buffered Reference Oscillator Output

Buffered output of on-chip reference oscillator or externally provided reference-input signal.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply

The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS

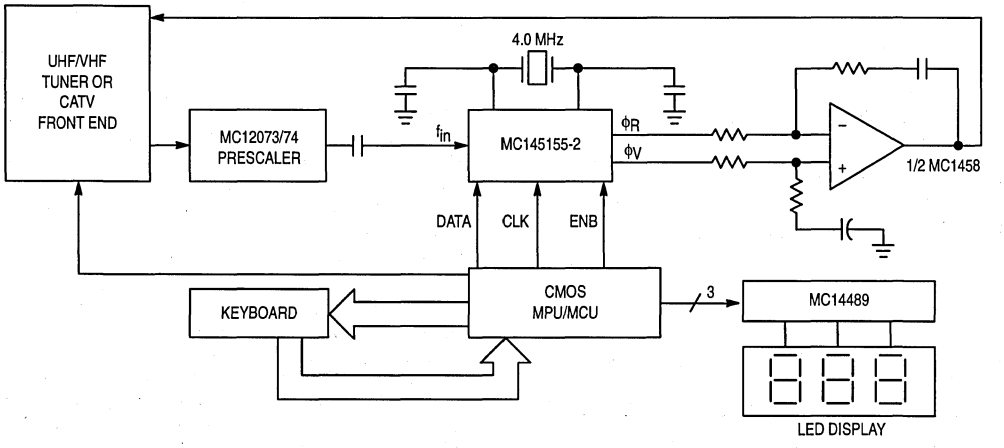


Figure 1. Microprocessor-Controlled TV/CATV Tuning System with Serial Interface

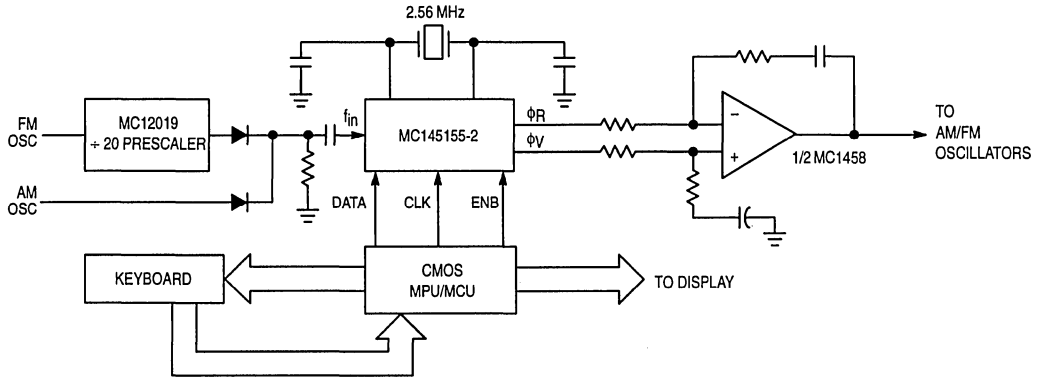


Figure 2. AM/FM Radio Synthesizer

Data Sheet Continued on Page 2-556

MC145156-2

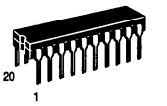
Serial-Input PLL Frequency Synthesizer

Interfaces with Dual-Modulus Prescalers

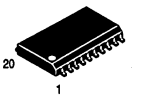
The MC145156-2 is programmed by a clocked, serial input, 19-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit programmable divide-by-A counter, and the necessary shift register and latch circuitry for accepting serial input data.

The MC145156-2 is an improved-performance drop-in replacement for the MC145156-1. Power consumption has decreased and ESD and latch-up performance have improved.

- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Dual Modulus/Serial Programming
- 8 User-Selectable ÷ R Values: 8, 64, 128, 256, 640, 1000, 1024, 2048
- ÷ N Range = 3 to 1023, ÷ A Range = 0 to 127
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single Ended (Three-State) or Double Ended
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOG
CASE 751D

FN SUFFIX
PLCC
CASE 775

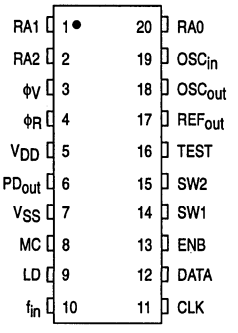
ORDERING INFORMATION

MC145156P2	Plastic DIP
MC145156DW2	SOG Package
MC145156FN2	PLCC Package

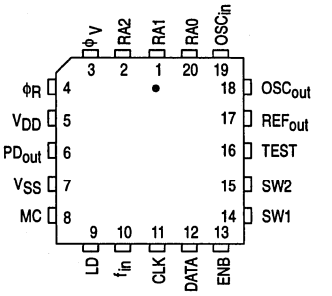
The PLCC (FN suffix) package will be phased out for this device and is NOT RECOMMENDED FOR NEW DESIGNS.

PIN ASSIGNMENTS

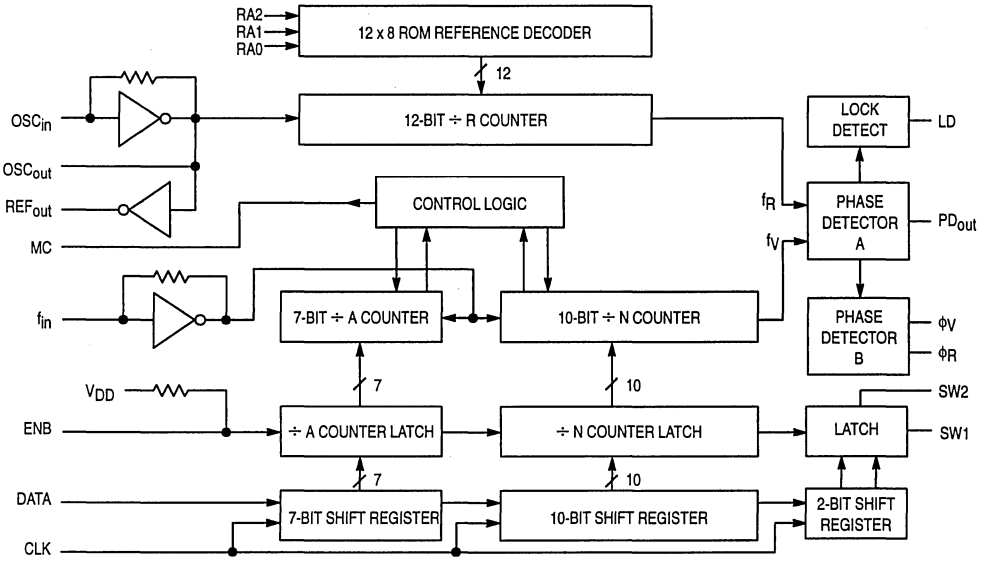
PLASTIC DIP and SOG PACKAGE



PLCC PACKAGE



BLOCK DIAGRAM



PIN DESCRIPTIONS

INPUT PINS

f_{in}
Frequency Input (Pin 10)

Input to the positive edge triggered ÷ N and ÷ A counters. f_{in} is typically derived from a dual-modulus prescaler and is ac coupled into the device. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

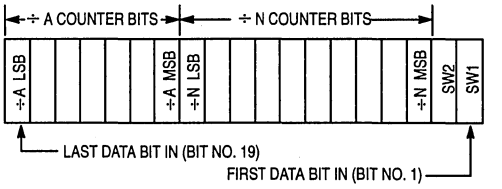
RA0, RA1, RA2
Reference Address Inputs (Pins 20, 1, 2)

These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below:

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	640
1	0	1	1000
1	1	0	1024
1	1	1	2048

CLK, DATA
Shift Register Clock, Serial Data Inputs (Pins 11, 12)

Each low-to-high transition clocks one bit into the on-chip 19-bit shift register. The Data input provides programming information for the 10-bit ÷ N counter, the 7-bit ÷ A counter, and the two switch signals SW1 and SW2. The entry format is as follows:



ENB
Latch Enable Input (Pin 13)

When high (1), ENB transfers the contents of the shift register into the latches, and to the programmable counter inputs, and the switch outputs SW1 and SW2. When low (0), ENB inhibits the above action and thus allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on-chip pull-up establishes a continuously high level for ENB when no external signal is applied. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output (Pins 19, 18)

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

TEST

Factory Test Input (Pin 16)

Used in manufacturing. Must be left open or tied to V_{SS}.

OUTPUT PINS

PD_{out}

Phase Detector A Output (Pin 6)

Three-state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ϕ_V and ϕ_R).

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕR, ϕV

Phase Detector B Outputs (Pins 4, 3)

These phase detector outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

MC

Dual-Modulus Prescale Control Output (Pin 8)

Signal generated by the on-chip control logic circuitry for controlling an external dual-modulus prescaler. The MC level will be low at the beginning of a count cycle and will remain low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T) = N • P + A where P and P + 1 represent the dual-modulus prescaler divide values respectively for high and low MC levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter.

LD

Lock Detector Output (Pin 9)

Essentially a high level when loop is locked (f_R, f_V of same phase and frequency). LD pulses low when loop is out of lock.

SW1, SW2

Band Switch Outputs (Pins 14, 15)

SW1 and SW2 provide latched open-drain outputs corresponding to data bits numbers one and two. These outputs can be tied through external resistors to voltages as high as 15 Vdc, independent of the V_{DD} supply voltage. These are typically used for band switch functions. A logic 1 causes the output to assume a high-impedance state, while a logic 0 causes the output to be low.

REF_{out}

Buffered Reference Oscillator Output (Pin 17)

Buffered output of on-chip reference oscillator or externally provided reference-input signal.

POWER SUPPLY PINS

V_{DD}

Positive Power Supply (Pin 5)

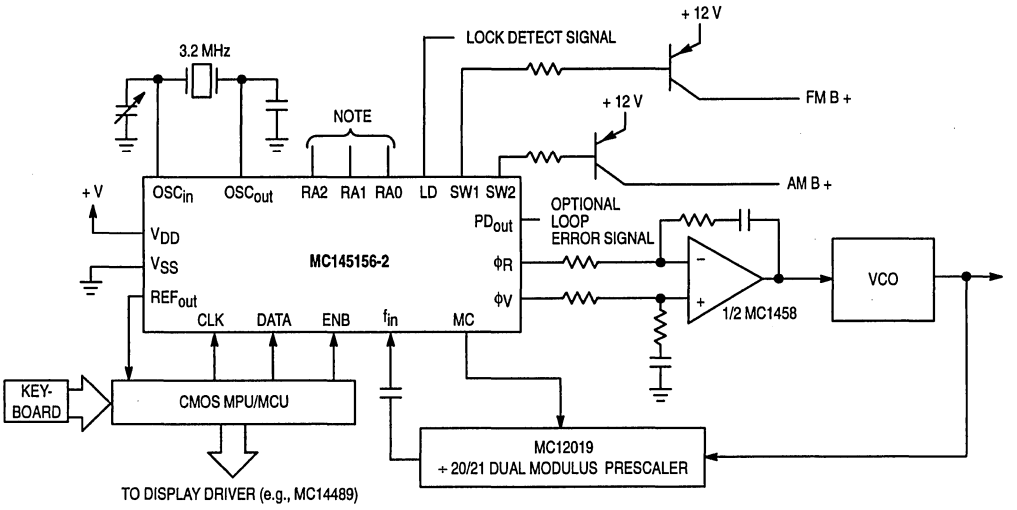
The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

V_{SS}

Negative Power Supply (Pin 7)

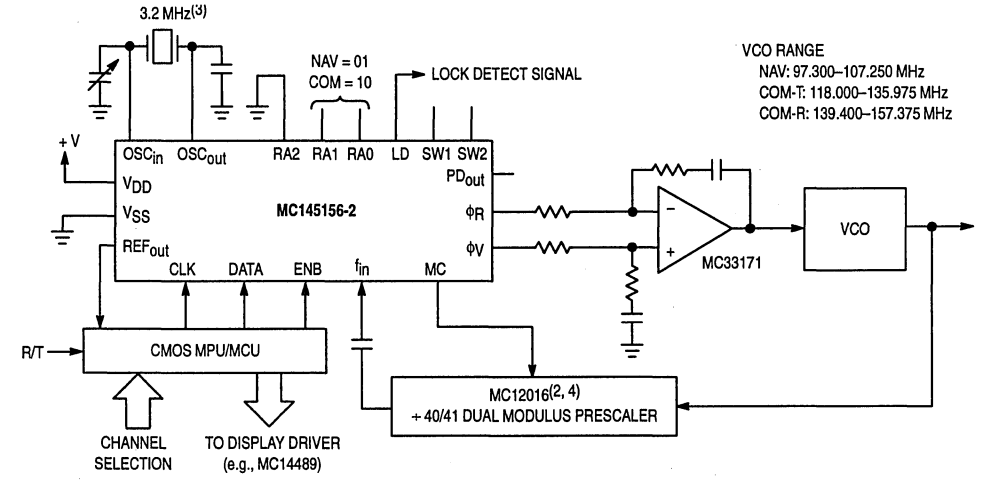
The most negative supply potential. This pin is usually ground.

TYPICAL APPLICATIONS



NOTE:
For AM: channel spacing = 5 kHz, ÷ R = ÷ 640 (code 100)
For FM: channel spacing = 25 kHz, ÷ R = ÷ 128 (code 010)

Figure 1. AM/FM Radio Broadcast Synthesizer



NOTES:
1. For NAV: f_R = 50 kHz, ÷ R = 64 using 10.7-MHz lowside injection, N_{total} = 1946–2145.
   For COM-T: f_R = 25 kHz, ÷ R = 128, N_{total} = 4720–5439.
   For COM-R: f_R = 25 kHz, ÷ R = 128, using 21.4-MHz highside injection, N_{total} = 5576–6295.
2. A ÷ 32/33 dual modulus approach is provided by substituting an MC12015 for the MC12016. The devices are pin equivalent.
3. A 6.4-MHz oscillator crystal can be used by selecting ÷ R = 128 (code 010) for NAV and ÷ R = 256 (code 011) for COM.
4. MC12013 + MC10131 combination may also be used to form the ÷ 40/41 prescaler.

Figure 2. Avionics Navigation or Communication Synthesizer

Data Sheet Continued on Page 2-556

MC145157-2

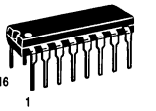
Serial-Input PLL Frequency Synthesizer

Interfaces with Single-Modulus Prescalers

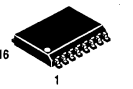
The MC145157-2 has a fully programmable 14-bit reference counter, as well as a fully programmable ÷ N counter. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145157-2 is an improved-performance drop-in replacement for the MC145157-1. Power consumption has decreased and ESD and latch-up performance have improved.

- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 16383
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single-Ended (Three-State) or Double-Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOG
CASE 751G

FN SUFFIX
PLCC
CASE 775

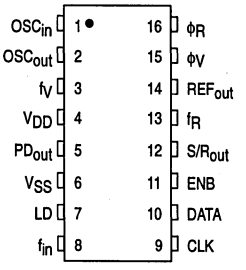
ORDERING INFORMATION

MC145157P2	Plastic DIP
MC145157DW2	SOG Package
MC145157FN2	PLCC Package

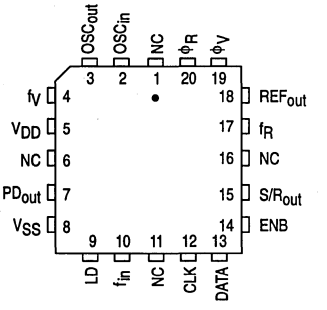
The PLCC (FN suffix) package will be phased out for this device and is NOT RECOMMENDED FOR NEW DESIGNS.

PIN ASSIGNMENTS

PLASTIC DIP and SOG PACKAGE

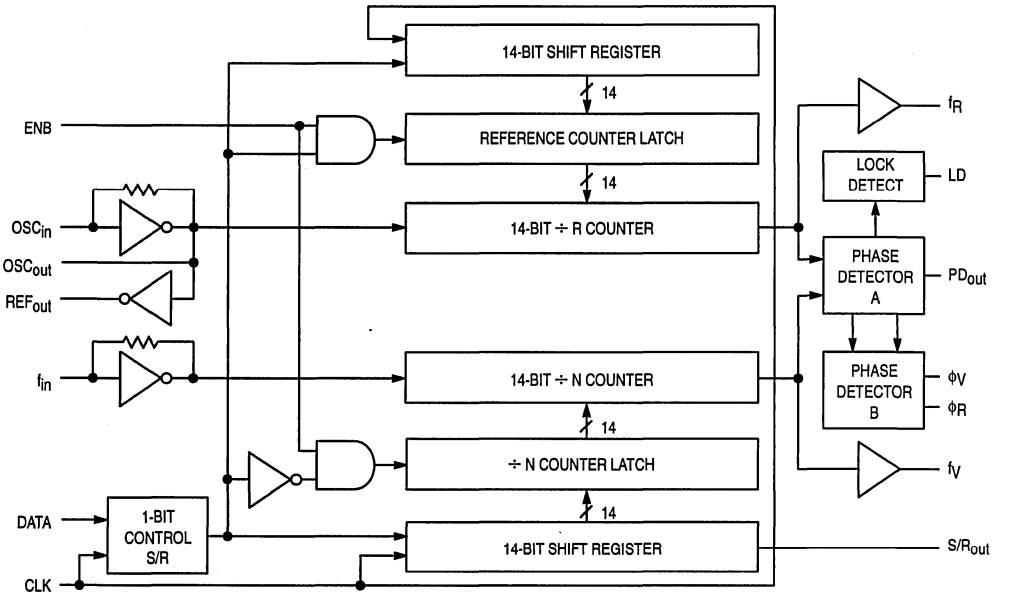


PLCC PACKAGE



NC = NO CONNECTION

BLOCK DIAGRAM



PIN DESCRIPTIONS

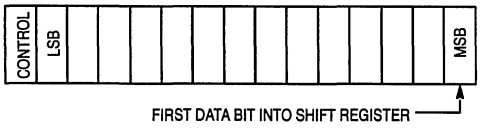
INPUT PINS

f_{in}
Frequency Input

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ N counter. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mVp-p. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

CLK, DATA
Shift Clock, Serial Data Inputs

Each low-to-high transition of the clock shifts one bit of data into the on-chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the ÷ N counter latch. The entry format is as follows:



ENB
Latch Enable Input

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Single-Ended Phase Detector A Output

This single-ended (three-state) phase detector output produces a loop error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕ_R, ϕ_V
Double-Ended Phase Detector B Outputs

These outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕ_V and ϕ_R remain high except for a small minimum time period when both pulse low in phase.

f_R, f_V
R Counter Output, N Counter Output

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD
Lock Detector Output

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}
Buffered Reference Oscillator Output

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

S/R_{out}
Shift Register Output

This output can be connected to an external shift register to provide band switching, control information, and counter programming code checking.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply

The positive power supply potential. This pin may range from +3 to +9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply

The most negative supply potential. This pin is usually ground.

Data Sheet Continued on Page 2-556

MC145158-2

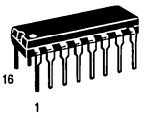
Serial-Input PLL Frequency Synthesizer

Interfaces with Dual-Modulus Prescalers

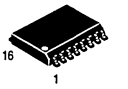
The MC145158-2 has a fully programmable 14-bit reference counter, as well as fully programmable ÷ N and ÷ A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

The MC145158-2 is an improved-performance drop-in replacement for the MC145158-1. Power consumption has decreased and ESD and latch-up performance have improved.

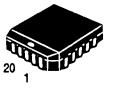
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- Fully Programmable Reference and ÷ N Counters
- ÷ R Range = 3 to 16383
- ÷ N Range = 3 to 1023
- Dual Modulus Capability; ÷ A Range = 0 to 127
- f_V and f_R Outputs
- Lock Detect Signal
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- "Linearized" Digital Phase Detector
- Single-Ended (Three-State) or Double-Ended Phase Detector Outputs
- Chip Complexity: 6504 FETs or 1626 Equivalent Gates



P SUFFIX
PLASTIC
CASE 648



DW SUFFIX
SOG
CASE 751G



FN SUFFIX
PLCC
CASE 775

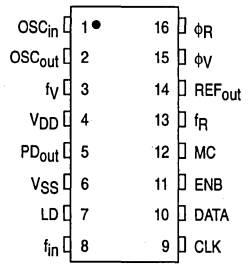
ORDERING INFORMATION

MC145158P2	Plastic DIP
MC145158DW2	SOG Package
MC145158FN2	PLCC Package

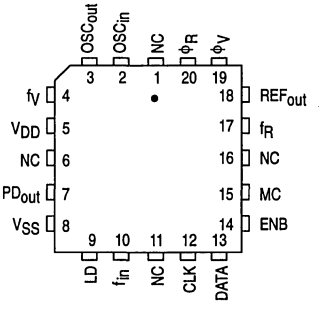
The PLCC (FN suffix) package will be phased out for this device and is NOT RECOMMENDED FOR NEW DESIGNS.

PIN ASSIGNMENTS

PLASTIC DIP and SOG PACKAGE

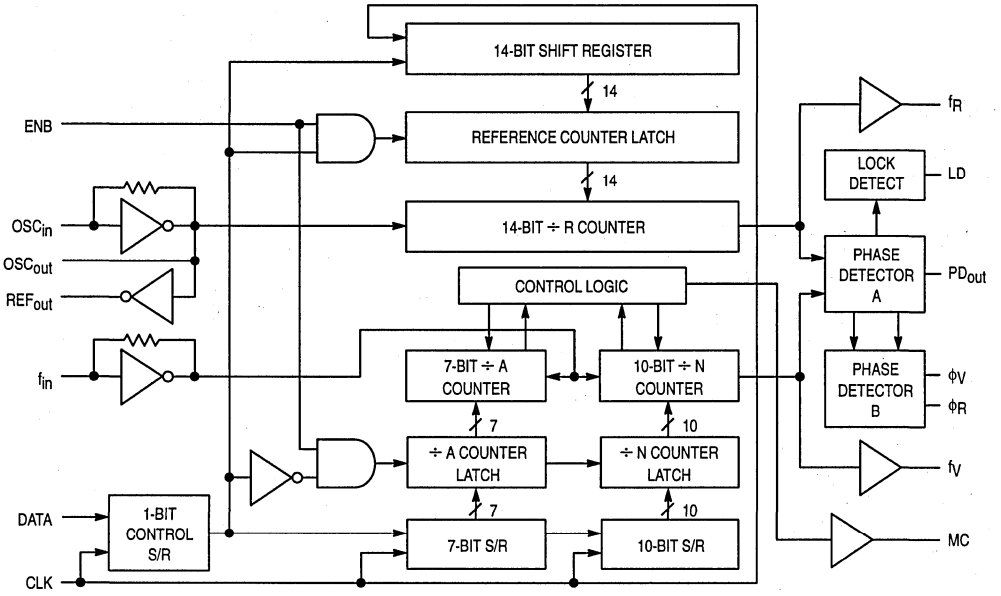


PLCC PACKAGE



NC = NO CONNECTION

BLOCK DIAGRAM



PIN DESCRIPTIONS

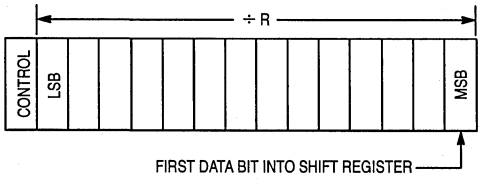
INPUT PINS

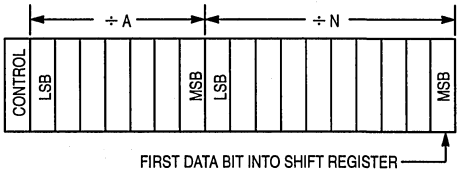
f_{in}
Frequency Input

Input frequency from VCO output. A rising edge signal on this input decrements the ÷ A and ÷ N counters. This input has an inverter biased in the linear region to allow use with ac coupled signals as low as 500 mVp-p. For larger amplitude signals (standard CMOS logic levels) dc coupling may be used.

CLK, DATA
Shift Clock, Serial Data Inputs

Each low-to-high transition of the CLK shifts one bit of data into the on-chip shift registers. The last data bit entered determines which counter storage latch is activated; a logic 1 selects the reference counter latch and a logic 0 selects the ÷ A, ÷ N counter latch. The data entry format is as follows:





ENB
Latch Enable Input

A logic high on this pin latches the data from the shift register into the reference divider or ÷ N, ÷ A latches depending on the control bit. The reference divider latches are activated if the control bit is at a logic high and the ÷ N, ÷ A latches are activated if the control bit is at a logic low. A logic low on this pin allows the user to change the data in the shift registers without affecting the counters. ENB is normally low and is pulsed high to transfer data to the latches.

OSC_{in}, OSC_{out}
Reference Oscillator Input/Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as the input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

OUTPUT PINS

PD_{out}
Phase Detector A Output

This single ended (three-state) phase detector output produces a loop error signal that is used with a loop filter to control a VCO.

Frequency $f_V > f_R$ or f_V Leading: Negative Pulses
Frequency $f_V < f_R$ or f_V Lagging: Positive Pulses
Frequency $f_V = f_R$ and Phase Coincidence: High-Impedance State

ϕR, ϕV
Phase Detector B Outputs

Double-ended phase detector outputs. These outputs can be combined externally for a loop-error signal. A single-ended output is also available for this purpose (see **PD_{out}**).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ϕV pulsing low. ϕR remains essentially high.

If the frequency f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ϕR pulsing low. ϕV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, then both ϕV and ϕR remain high except for a small minimum time period when both pulse low in phase.

MC
Dual-Modulus Prescale Control Output

This output generates a signal by the on-chip control logic circuitry for controlling an external dual-modulus prescaler. The MC level is low at the beginning of a count cycle and remains low until the ÷ A counter has counted down from its programmed value. At this time, MC goes high and remains high until the ÷ N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷ N and ÷ A are counting down during the first portion of the cycle). MC is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value $(N_T) = N \bullet P + A$ where P and P + 1 represent the dual-modulus prescaler divide values respectively for high and low modulus control levels, N the number programmed into the ÷ N counter, and A the number programmed into the ÷ A counter. Note that when a prescaler is needed, the dual-modulus version offers a distinct advantage. The dual-modulus prescaler allows a higher reference frequency at the phase detector input, increasing system performance capability, and simplifying the loop filter design.

f_R, f_V
R Counter Output, N Counter Output

Buffered, divided reference and f_{in} frequency outputs. The f_R and f_V outputs are connected internally to the ÷ R and ÷ N counter outputs respectively, allowing the counters to be used independently, as well as monitoring the phase detector inputs.

LD
Lock Detector Output

This output is essentially at a high level when the loop is locked (f_R, f_V of same phase and frequency), and pulses low when loop is out of lock.

REF_{out}
Buffered Reference Oscillator Output

This output can be used as a second local oscillator, reference oscillator to another frequency synthesizer, or as the system clock to a microprocessor controller.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply

The positive power supply potential. This pin may range from + 3 to + 9 V with respect to V_{SS}.

V_{SS}
Negative Power Supply

The most negative supply potential. This pin is usually ground.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 10.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) except SW1, SW2	– 0.5 to V_{DD} + 0.5	V
V_{out}	Output Voltage (DC or Transient), SW1, SW2 ($R_{pull\text{-}up}$ = 4.7 kΩ)	– 0.5 to + 15	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature , 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

† Power Dissipation Temperature Derating:
Plastic DIP: – 12 mW/°C from 65 to 85°C
PLCC Package: – 12 mW/°C from 65 to 85°C
SOG Package: – 7 mW/°C from 65 to 85°C

These devices contain protection circuitry to protect against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to these high-impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ except for SW1 and SW2.

SW1 and SW2 can be tied through external resistors to voltages as high as 15 V dc, independent of the supply voltage.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pull-up devices. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C Min	– 40°C Max	25°C Min	25°C Max	+ 85°C Min	+ 85°C Max	Unit
V_{DD}	Power Supply Voltage Range		—	3	9	3	9	3	9	V
I_{ss}	Dynamic Supply Current	f_{in} = OSC_{in} = 10 MHz, 1 Vp-p ac-coupled sine wave R = 128, A = 32, N = 128	3 5 9	— — —	3.5 10 30	— — —	3 7.5 24	— — —	3 7.5 24	mA
I_{SS}	Quiescent Supply Current (not including pull-up current component)	V_{in} = V_{DD} or V_{SS} I_{out} = 0 µA	3 5 9	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	µA
V_{in}	Input Voltage — f_{in}, OSC_{in}	Input ac-coupled sine wave	—	500	—	500	—	500	—	mVp-p
V_{IL}	Low-Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \ge 2.1$ V Input dc-coupled square wave $V_{out} \ge 3.5$ V $V_{out} \ge 6.3$ V	3 5 9	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
V_{IH}	High-Level Input Voltage — f_{in}, OSC_{in}	$V_{out} \le 0.9$ V Input dc-coupled square wave $V_{out} \le 1.5$ V $V_{out} \le 2.7$ V	3 5 9	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
V_{IL}	Low-Level Input Voltage — except f_{in}, OSC_{in}		3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{IH}	High-Level Input Voltage — except f_{in}, OSC_{in}		3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
I_{in}	Input Current (f_{in}, OSC_{in})	V_{in} = V_{DD} or V_{SS}	9	± 2	± 50	± 2	± 25	± 2	± 22	µA
I_{IL}	Input Leakage Current (Data, CLK, ENB — without pull-ups)	V_{in} = V_{SS}	9	—	– 0.3	—	– 0.1	—	– 1.0	µA

(continued)

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Max	+85°C Min	+85°C Max	Unit
I_{IH}	Input Leakage Current (all inputs except f_{in}, OSC_{in})	$V_{in} = V_{DD}$	9	—	0.3	—	0.1	—	1.0	µA
I_{IL}	Pull-up Current (all inputs with pull-ups)	$V_{in} = V_{SS}$	9	−20	−400	−20	−200	−20	−170	µA
C_{in}	Input Capacitance		—	—	10	—	10	—	10	pF
V_{OL}	Low-Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{DD}$	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
V_{OH}	High-Level Output Voltage — OSC_{out}	$I_{out} \approx 0$ µA $V_{in} = V_{SS}$	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	V
V_{OL}	Low-Level Output Voltage — Other Outputs	$I_{out} \approx 0$ µA	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
V_{OH}	High-Level Output Voltage — Other Outputs	$I_{out} \approx 0$ µA	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	V
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage — SW1, SW2	$R_{pull\text{-}up} = 4.7$ kΩ	—	15	—	15	—	15	—	V
I_{OL}	Low-Level Sinking Current — MC	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	mA
I_{OH}	High-Level Sourcing Current — MC	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	−0.60 −0.90 −1.50	— — —	−0.50 −0.75 −1.25	— — —	−0.30 −0.50 −0.80	— — —	mA
I_{OL}	Low-Level Sinking Current — LD	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.25 0.64 1.30	— — —	0.20 0.51 1.00	— — —	0.15 0.36 0.70	— — —	mA
I_{OH}	High-Level Sourcing Current — LD	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	−0.25 −0.64 −1.30	— — —	−0.20 −0.51 −1.00	— — —	−0.15 −0.36 −0.70	— — —	mA
I_{OL}	Low-Level Sinking Current — SW1, SW2	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.80 1.50 3.50	— — —	0.48 0.90 2.10	— — —	0.24 0.45 1.05	— — —	mA
I_{OL}	Low-Level Sinking Current — Other Outputs	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	mA
I_{OH}	High-Level Sourcing Current — Other Outputs	$V_{out} = 2.7$ V $V_{out} = 4.6$ V $V_{out} = 8.5$ V	3 5 9	−0.44 −0.64 −1.30	— — —	−0.35 −0.51 −1.00	— — —	−0.22 −0.36 −0.70	— — —	mA
I_{OZ}	Output Leakage Current — PD_{out}	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	—	±0.3	—	±0.1	—	±1.0	µA
I_{OZ}	Output Leakage Current — SW1, SW2	$V_{out} = V_{DD}$ or V_{SS} Output in Off State	9	—	±0.3	—	±0.1	—	±3.0	µA
C_{out}	Output Capacitance — PD_{out}	PD_{out} — Three-State	—	—	10	—	10	—	10	pF

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 10 ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit – 40 to 85°C	Unit
t_{PLH}, t_{PHL}	Maximum Propagation Delay, f_{in} to MC (Figures 1 and 4)	3 5 9	110 60 35	120 70 40	ns
t_{PHL}	Maximum Propagation Delay, ENB to SW1, SW2 (Figures 1 and 5)	3 5 9	160 80 50	180 95 60	ns
t_W	Output Pulse Width, ϕ_R, ϕ_V, and LD with f_R in Phase with f_V (Figures 2 and 4)	3 5 9	25 to 200 20 to 100 10 to 70	25 to 260 20 to 125 10 to 80	ns
t_{TLH}	Maximum Output Transition Time, MC (Figures 3 and 4)	3 5 9	115 60 40	115 75 60	ns
t_{THL}	Maximum Output Transition Time, MC (Figures 3 and 4)	3 5 9	60 34 30	70 45 38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, LD (Figures 3 and 4)	3 5 9	180 90 70	200 120 90	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Other Outputs (Figures 3 and 4)	3 5 9	160 80 60	175 100 65	ns

SWITCHING WAVEFORMS

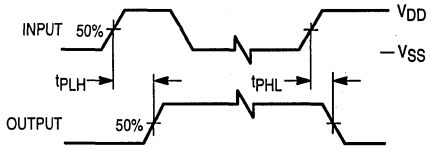
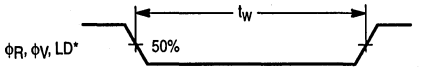


Figure 1.



*f_R in phase with f_V.

Figure 2.

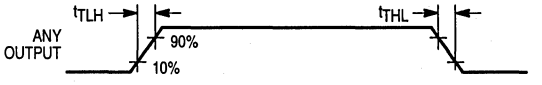
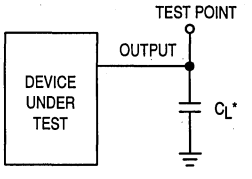
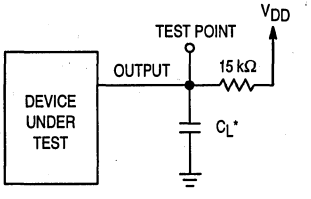


Figure 3.



*Includes all probe and jig capacitance.

Figure 4. Test Circuit



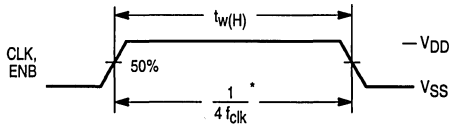
*Includes all probe and jig capacitance.

Figure 5. Test Circuit

TIMING REQUIREMENTS (Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit 25°C	Guaranteed Limit – 40 to 85°C	Unit
f_{clk}	Serial Data Clock Frequency, Assuming 25% Duty Cycle NOTE: Refer to CLK $t_{w(H)}$ below (Figure 6)	3 5 9	dc to 5.0 dc to 7.1 dc to 10	dc to 3.5 dc to 7.1 dc to 10	MHz
t_{su}	Minimum Setup Time, Data to CLK (Figure 7)	3 5 9	30 20 18	30 20 18	ns
t_h	Minimum Hold Time, CLK to Data (Figure 7)	3 5 9	40 20 15	40 20 15	ns
t_{su}	Minimum Setup Time, CLK to ENB (Figure 7)	3 5 9	70 32 25	70 32 25	ns
t_{rec}	Minimum Recovery Time, ENB to CLK (Figure 7)	3 5 9	5 10 20	5 10 20	ns
$t_{w(H)}$	Minimum Pulse Width, CLK and ENB (Figure 6)	3 5 9	50 35 25	70 35 25	ns
t_r, t_f	Maximum Input Rise and Fall Times — Any Input (Figure 8)	3 5 9	5 4 2	5 4 2	µs

SWITCHING WAVEFORMS



*Assumes 25% Duty Cycle.

Figure 6.

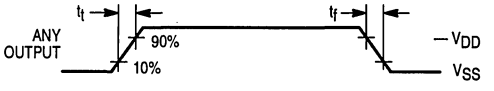


Figure 8.

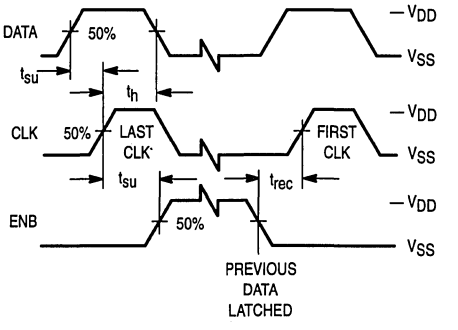
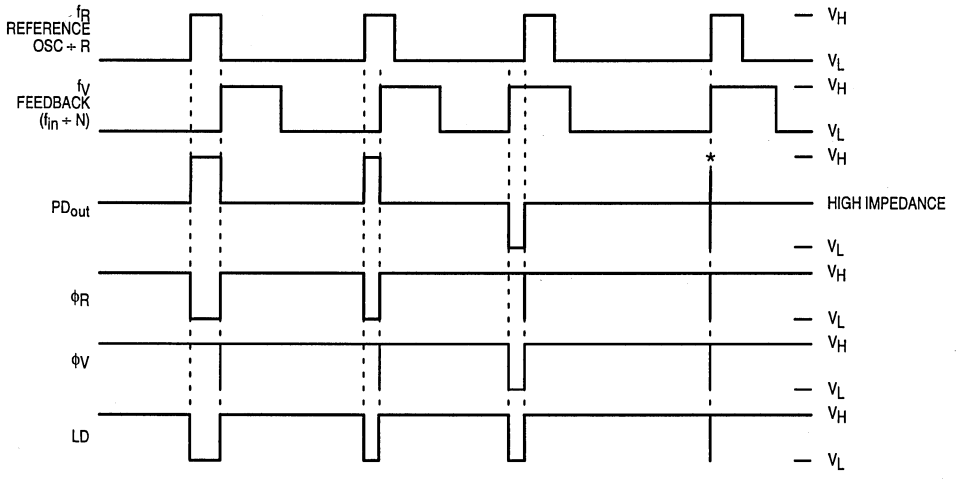


Figure 7.

FREQUENCY CHARACTERISTICS (Voltages References to V_{SS}, C_L = 50 pF, Input $t_r = t_f$ =10 ns unless otherwise indicated)

Symbol	Parameter	Test Condition	V_{DD} V	– 40°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
f_i	Input Frequency (f_{in}, OSC_{in})	R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 500 mVp-p ac-coupled sine wave	3 5 9	— — —	6 15 15	— — —	6 15 15	— — —	6 15 15	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = 1 Vp-p ac-coupled sine wave	3 5 9	— — —	12 22 25	— — —	12 20 22	— — —	7 20 22	MHz
		R ≥ 8, A ≥ 0, N ≥ 8 V_{in} = V_{DD} to V_{SS} dc-coupled square wave	3 5 9	— — —	13 25 25	— — —	12 22 25	— — —	8 22 25	MHz

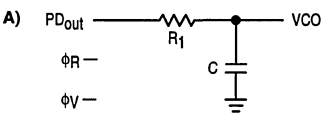


V_H = High Voltage Level
V_L = Low Voltage Level
*At this point, when both f_R and f_V are in phase, the output is forced to near mid-supply.
NOTE: The PD_{out} generates error pulses during out-of-lock conditions. When locked in phase and frequency the output is high and the voltage at this pin is determined by the low-pass filter capacitor.

Figure 9. Phase Detector/Lock Detector Output Waveforms

PHASE-LOCKED LOOP—LOW-PASS FILTER DESIGN

A)

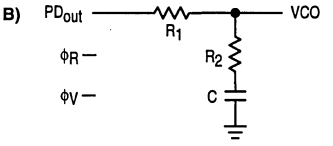


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

B)

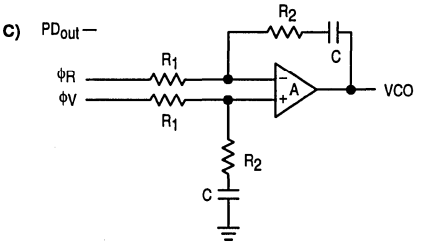


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1+R_2)\,sC + 1}$$

C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

Note: Sometimes R_1 is split into two series resistors each $R_1 \div 2$. A capacitor C_C is then placed from the midpoint to ground to further filter ϕ_V and ϕ_R. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in feedback loop

K_ϕ (Phase Detector Gain) = $V_{DD}/4\pi$ for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ for ϕ_V and ϕ_R

K_{VCO} (VCO Gain) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$

for a typical design w_n (Natural Frequency) $\approx \frac{2\pi fr}{10}$ (at phase detector input).

Damping Factor: $\zeta \cong 1$

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley-Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley-Interscience, 1980.

Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York, Wiley-Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley-Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice-Hall, 1983.

Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

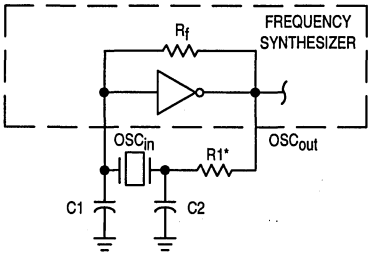
For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off-Chip Reference

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.



*May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

For V_{DD} = 5.0 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8.0 MHz, 20 pF for frequencies in the area of 8.0 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. The shunt load capacitance, C_L, presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_O + \frac{C1 \cdot C2}{C1 + C2}$$

where:

C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C_O = the crystal's holder capacitance (see Figure 12)
C1 and C2 = external capacitors (see Figure 10)

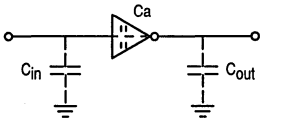
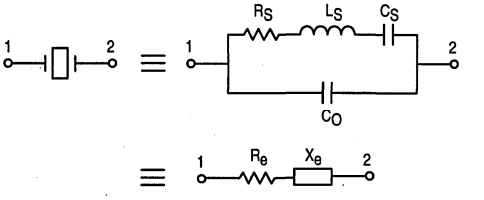


Figure 11. Parasitic Capacitances of the Amplifier



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. In some cases, stray capacitance should be added to the value for C_{in} and C_{out}.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The drive level specified by the crystal manufacturer is the maximum stress that a crystal can withstand without damaging or excessive shift in frequency. R1 in Figure 10 limits the drive level. The use of R1 may not be necessary in some cases (i.e., R1 = 0 Ω).

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 1).

Recommended Reading

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

Table 1. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

DUAL-MODULUS PRESCALING

Overview

The technique of dual-modulus prescaling is well established as a method of achieving high performance frequency synthesizer operation at high frequencies. Basically, the approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that results if a fixed (single-modulus) divider is used for the prescaler.

In dual-modulus prescaling, the lower speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P + 1 in the prescaler for the required amount of time (see modulus control definition). Motorola's dual-modulus frequency synthesizers contain this feature and can be used with a variety of dual-modulus prescalers to allow speed, complexity and cost to be tailored to the system requirements. Prescalers having P, P + 1 divide values in the range of ÷ 3/÷ 4 to ÷ 128/÷ 129 can be controlled by most Motorola frequency synthesizers.

Several dual-modulus prescaler approaches suitable for use with the MC145152-2, MC145156-2, or MC145158-2 are:

MC12009	÷ 5/÷ 6	440 MHz
MC12011	÷ 8/÷ 9	500 MHz
MC12013	÷ 10/÷ 11	500 MHz
MC12015	÷ 32/÷ 33	225 MHz
MC12016	÷ 40/÷ 41	225 MHz
MC12017	÷ 64/÷ 65	225 MHz
MC12018	÷ 128/÷ 129	520 MHz
MC12022A	÷ 64/65 or ÷ 128/129	1.1 GHz
MC12032A	÷ 64/65 or ÷ 128/129	2.0 GHz

Design Guidelines

The system total divide value, N_{total} (N_T) will be dictated by the application:

$$N_T = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N \cdot P + A$$

N is the number programmed into the ÷ N counter, A is the number programmed into the ÷ A counter, P and P + 1 are the two selectable divide ratios available in the dual-modulus prescalers. To have a range of N_T values in sequence, the ÷ A counter is programmed from zero through P – 1 for a particular value N in the ÷ N counter. N is then incremented to N + 1 and the ÷ A is sequenced from 0 through P – 1 again.

There are minimum and maximum values that can be achieved for N_T. These values are a function of P and the size of the ÷ N and ÷ A counters.

The constraint $N \geq A$ always applies. If $A_{max} = P - 1$, then $N_{min} \geq P - 1$. Then $N_{Tmin} = (P - 1)\ P + A$ or $(P - 1)\ P$ since A is free to assume the value of 0.

$$N_{Tmax} = N_{max} \cdot P + A_{max}$$

To maximize system frequency capability, the dual-modulus prescaler output must go from low to high after each group of P or P + 1 input cycles. The prescaler should divide by P when its modulus control line is high and by P + 1 when its MC is low.

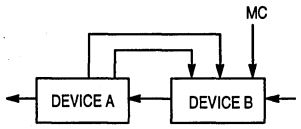
For the maximum frequency into the prescaler (f_{VCOmax}), the value used for P must be large enough such that:

1. f_{VCOmax} divided by P may not exceed the frequency capability of f_{in} (input to the ÷ N and ÷ A counters).
2. The period of f_{VCO} divided by P must be greater than the sum of the times:
   a. Propagation delay through the dual-modulus prescaler.
   b. Prescaler setup or release time relative to its MC signal.
   c. Propagation time from f_{in} to the MC output for the frequency synthesizer device.

A sometimes useful simplification in the programming code can be achieved by choosing the values for P of 8, 16, 32, or 64. For these cases, the desired value of N_T results when N_T in binary is used as the program code to the ÷ N and ÷ A counters treated in the following manner:

1. Assume the ÷ A counter contains "a" bits where $2^a \geq P$.
2. Always program all higher order ÷ A counter bits above "a" to 0.
3. Assume the ÷ N counter and the ÷ A counter (with all the higher order bits above "a" ignored) combined into a single binary counter of n + a bits in length (n = number of divider stages in the ÷ N counter). The MSB of this "hypothetical" counter is to correspond to the MSB of ÷ N and the LSB is to correspond to the LSB of ÷ A. The system divide value, N_T, now results when the value of N_T in binary is used to program the "new" n + a bit counter.

By using the two devices, several dual-modulus values are achievable (shown in Figure 13).



DEVICE A \ DEVICE B	MC12009	MC12011	MC12013
MC10131	÷ 20/÷ 21	÷ 32/÷ 33	÷ 40/÷ 41
MC10138	÷ 50/÷ 51	÷ 80/÷ 81	÷ 100/÷ 101
MC10154	÷ 40/÷ 41 or ÷ 80/÷ 81	÷ 64/÷ 65 or ÷ 128/÷ 129	÷ 80/÷ 81

NOTE: MC12009, MC12011, and MC12013 are pin equivalent.
MC12015, MC12016, and MC12017 are pin equivalent.

Figure 13.

MC145159-1

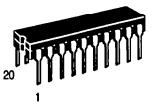
Serial-Input PLL Frequency Synthesizer with Analog Phase Detector

Interfaces with Dual-Modulus Prescalers

The MC145159-1 has a programmable 14-bit reference counter, as well as fully programmable divide-by-N/divide-by-A counters. The counters are programmed serially through a common data input and latched into the appropriate counter latch, according to the last data bit (control bit) entered.

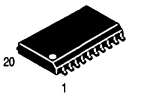
When combined with a loop filter and VCO, this device can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operations, a down mixer or a dual modulus prescaler can be used between the VCO and the PLL.

- General Purpose Applications:
  - CATV
  - TV Tuning
  - AM/FM Radios
  - Scanning Receivers
  - Two Way Radios
  - Amateur Radio
- Low Power Consumption Through Use of CMOS Technology
- 3.0 to 9.0 V Supply Range
- On- or Off-Chip Reference Oscillator Operation
- Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs
- ÷ R Range = 3 to 16383
- ÷ N Range = 16 to 1023, ÷ A Range = 0 to 127
- High-Gain Analog Phase Detector
- See Application Note AN969



P SUFFIX
PLASTIC
CASE 738

FN SUFFIX
PLCC
CASE 775



DW SUFFIX
SOG
CASE 751D

VF SUFFIX
SSOP
CASE TBD

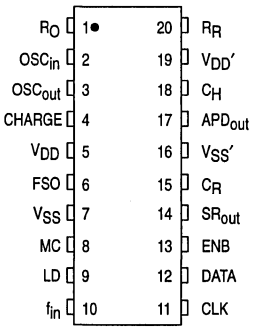
ORDERING INFORMATION

MC145159P1	Plastic DIP
MC145159FN1	PLCC
MC145159DW1	SOG
MC145159VF1	SSOP

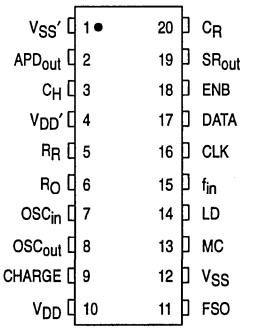
The PLCC (FN suffix) package will be phased out for this device and is NOT RECOMMENDED FOR NEW DESIGNS.

PIN ASSIGNMENTS

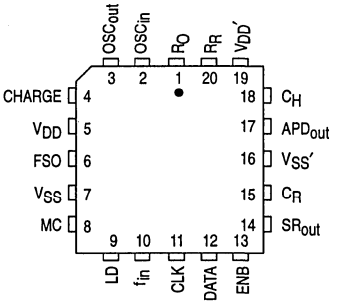
PLASTIC DIP and SOG PACKAGE



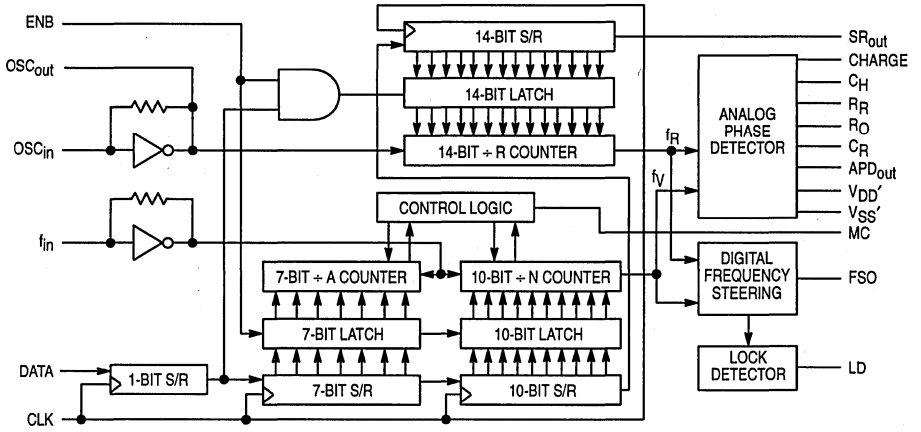
SSOP PACKAGE



PLCC PACKAGE



BLOCK DIAGRAM



*FSO is not and cannot be used as a digital phase detector output.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 10.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
I_{DD}, I_{SS}	Supply Current, V_{DD} or V_{SS} Pins	± 30	mA
P_D	Power Dissipation, per Package	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS} except I_{CR} and I_{APD} which are referenced to V_{SS}')

Characteristic	Symbol	V_{DD}	−40°C Min	−40°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
Power Supply Voltage Range	V_{DD}	—	3	9	3	9	3	9	V
Output Voltage 0 Level V_{in} = 0 V or V_{DD} I_{out} = 0 μA (Except OSC_{out} and APD_{out})	V_{OL}	3 5 9	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	— — —	0.05 0.05 0.05	V
1 Level	V_{OH}	3 5 9	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	2.95 4.95 8.95	— — —	
Output Voltage 0 Level OSC_{out} V_{in} = 0 V or V_{DD}	V_{OL}	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
1 Level	V_{OH}	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	
ΔVoltage, $V_{CH} - V_{APDout}$, I_{APDout} = 0 μA	ΔV	—	—	—	—	1.05	—	—	V
Input Voltage 0 Level V_{out} = 0.5 V or V_{DD} − 0.5 V (All Outputs Except OSC_{out})	V_{IL}	3 5 9	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	— — —	0.9 1.5 2.7	V
1 Level	V_{IH}	3 5 9	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	2.1 3.5 6.3	— — —	
Input Voltage* — OSC_{in} V_O = 2.1 V or 0.9 V 0 Level V_O = 3.5 V or 1.5 V V_O = 6.3 V or 2.7 V	V_{IL}	3 5 9	— — —	0 0 0	— — —	0 0 0	— — —	0 0 0	V
V_O = 0.9 V or 2.1 V 1 Level V_O = 1.5 V or 3.5 V V_O = 2.7 V or 6.3 V	V_{IH}	3 5 9	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	3.0 5.0 9.0	— — —	V
Output Current — MC V_{out} = 2.7 V Source V_{out} = 4.6 V V_{out} = 8.5 V	I_{OH}	3 5 9	−0.60 −0.90 −1.50	— — —	−0.50 −0.75 −1.25	— — —	−0.30 −0.50 −0.80	— — —	mA
V_{out} = 0.3 V Sink V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	3 5 9	1.30 1.90 3.80	— — —	1.10 1.70 3.30	— — —	0.66 1.08 2.10	— — —	
Output Current, C_R, V_{CR} = 4.5 V, R_R = 240 k	I_{CR}	9	—	—	−90	−110	—	—	μA
Output Current, APD_{out} R_O = 240 k, V_{CH} = 0 V, V_{APDout} = 4.5 V	I_{APD}	9	—	—	170	350	—	—	μA
Output Current — Other Outputs V_{out} = 2.7 V Source V_{out} = 4.6 V V_{out} = 8.5 V	I_{OH}	3 5 9	−0.44 −0.64 −1.30	— — —	−0.35 −0.51 −1.00	— — —	−0.22 −0.36 −0.70	— — —	mA
V_{out} = 0.3 V Sink V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	3 5 9	0.44 0.64 1.30	— — —	0.35 0.51 1.00	— — —	0.22 0.36 0.70	— — —	
Input Current — Data, CLK, ENB	I_{in}	9	—	±0.3	—	±0.1	—	±1.0	μA
Input Current — f_{in}, OSC_{in}	I_{in}	9	±2	±50	±2	±25	±2	±22	μA
Input Capacitance	C_{in}	—	—	10	—	10	—	10	pF
Three-State Output Capacitance — FSO	C_{out}	—	—	10	—	10	—	10	pF
Quiescent Current V_{in} = 0 V or V_{DD} I_{out} = 0 μA	I_{DD}	3 5 9	— — —	800 1200 1600	— — —	800 1200 1600	— — —	1600 2400 3200	μA
Three-State Leakage Current, V_{out} = 0 V or 9 V	I_{OZ}	9	—	±0.3	—	±0.1	—	±3.0	μA

*DC-coupled square wave.

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Characteristic	Figure #	Symbol	V_{DD}	Min	Max	Unit
Output Rise Time — MC	4, 9	t_{TLH}	3 5 9	— — —	115 60 40	ns
Output Fall Time — MC	4, 9	t_{THL}	3 5 9	— — —	60 34 30	ns
Output Rise and Fall Time — LD and SR_{out}	4, 9	t_{TLH}, t_{THL}	3 5 9	— — —	140 80 60	ns
Propagation Delay Time — f_{in} to MC	5, 9	t_{PLH}, t_{PHL}	3 5 9	— — —	125 80 50	ns
Setup Times — Data to CLK	6	t_{su}	3 5 9	30 20 18	— — —	ns
CLK to ENB	6		3 5 9	70 32 25	— — —	
Hold Time — CLK to Data	6	t_h	3 5 9	12 12 15	— — —	ns
Recovery Time — ENB to CLK	6	t_{rec}	3 5 9	5 10 20	— — —	ns
Input Rise and Fall Times — CLK, OSC_{in}, f_{in}	7	t_r, t_f	3 5 9	— — —	5 2 0.5	µs
Input Pulse Width — ENB and CLK	8	t_w	3 5 9	40 35 25	— — —	ns

NOTE: Refer to the graphs and text in application note AN969 for maximum frequency information.

PIN DESCRIPTIONS

INPUT PINS

OSC_{in}, OSC_{out}
Oscillator Input and Oscillator Output

These pins form an on-chip reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate value must be connected from OSC_{in} to V_{SS} and OSC_{out} to V_{SS}. OSC_{in} may also serve as input for an externally-generated reference signal. This signal will typically be ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels), dc coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

f_{in}
Frequency Input

Input to the positive edge triggered divide-by-N and divide-by-A counters. f_{in} is typically derived from a dual modulus prescaler and is ac coupled. This input has an inverter biased in the linear region to allow use with ac-coupled signals as low as 500 mV peak-to-peak or direct- coupled signals swinging from V_{DD} to V_{SS}.

DATA
Serial Data Input

Counter and control information is shifted into this input. The last data bit entered goes into the one-bit control shift register. A logic 1 allows the reference counter information to be loaded into its 14-bit latch when Enable goes high. A logic 0 entered as the control bit disables the reference counter latch. The divide-by-A/divide-by-N counter latch is loaded, regardless of the contents of the control register, when ENB goes high. The data entry format is shown in Figure 1.

ENB
Transparent Latch Enable

A logic high on this input allows data to be entered into the divide-by-A/divide-by-N latch and, if the control bit is high, into the reference counter latch. Counter programming is unaffected when ENB is low. ENB should be kept normally low and pulsed high to transfer data to the latches.

CLK
Shift Register Clock

A low-to-high transition on this input shifts data from the serial data input into the shift registers.

COMPONENT PINS

C_R
Ramp Capacitor

The capacitor connected from this pin to V_{SS}' is charged linearly, at a rate determined by R_R. The voltage on this capacitor is proportional to the phase difference of the frequencies present at the internal phase detector inputs. A polystyrene or mylar capacitor is recommended.

R_R
Ramp Current Bias Resistor

A resistor connected from this pin to V_{SS}' determines the rate at which the ramp capacitor is charged, thereby affecting the phase detector gain (see Figure 2).

C_H
Hold Capacitor

The charge stored on the ramp capacitor is transferred to the capacitor connected from this pin to either V_{DD}' or V_{SS}'. The ratio of C_R to C_H should be large enough to have no affect on the phase detector gain (C_R > 10 C_H). A low-leakage capacitor should be used.

R_O
Output Bias Current Resistor

A resistor connected from this pin to V_{SS}' biases the output N-Channel transistor, thereby setting a current sink on the analog phase detector output. This resistor adjusts the APD_{out} bias current (see Figure 3).

OUTPUT PINS

APD_{out}
Analog Phase Detector Output

This output produces a voltage that controls an external VCO. The voltage range of this output (V_{DD} = + 9 V) is from below + 0.5 V to + 8 V or more. The source impedance of this output is the equivalent of a source follower with an externally variable source resistor. The source resistor depends upon the output bias current controlled by the output bias current resistor, R_O. The bias current is adjustable from 0.01 mA to 0.5 mA. The output voltage is not more than 1.05 V below the sampled point on the ramp. With a constant sample of the ramp voltage at 9 V and the hold capacitor of 50 pF, the instantaneous output ripple is about 5 mV peak-to-peak.

CHARGE
Ramp Charge Indicator

This output is high from the time f_R goes high to the time f_V goes high (f_R and f_V are the frequencies at the phase detector inputs). This high voltage indicates that the ramp capacitor, C_R, is being charged.

FSO
Three-State Frequency Steering Output

If the counted down input frequency on f_{in} is higher than the counted down reference frequency of OSC_{in}, this output goes low. If the counted down VCO frequencies is lower than that of the counted down OSC_{in}, this output goes high.

The repetition rate of the frequency steering output pulses is approximately equal to the difference of the frequencies

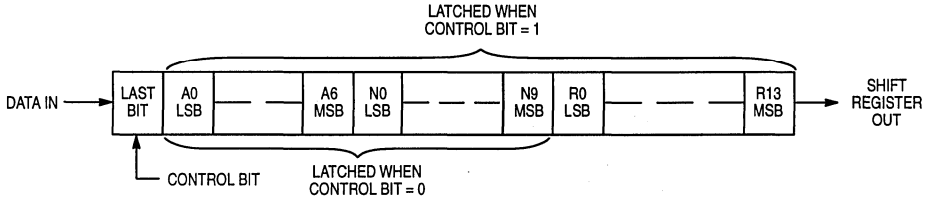


Figure 1. Data Entry Format

The repetition rate of the frequency steering output pulses is approximately equal to the difference of the frequencies of the two counted down inputs from the VCO and OSC_{in}. See Application Note AN969 for further information.

LD
Lock Detector Indicator

This output is high during lock and goes low to indicate a non-lock condition. The frequency and duration of the non-lock pulses will be the same as either polarity of the frequency steering output.

MC
Dual Modulus Prescaler Control

The modulus control level is low at the beginning of a count cycle and remains low until the divide-by-A counter has counted down from its programmed value. At that time, the modulus control goes high and remains high until the divide-by-N counter has counted the rest of the way down from its programmed value (N – A additional counts since both divide-by-N and divide-by-A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value of $N_T = N \bullet P + A$, where P and P + 1 represent the dual modulus prescaler divide values respectively for high and low modulus control levels, N is the number programmed into the divide-by-N counter, and A is the number programmed into the divide-by-A counter.

SR_{out}
Shift Register Output

This pin is the non-inverted output of the last stage of the 32-bit serial data shift register. It is not latched by the ENB line. If unused, SR_{out} should be floated.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply

Positive power supply input for all sections of the device except the analog phase detector. V_{DD} and V_{DD}' should be powered up at the same time to avoid damage to the MC145159-1. V_{DD} must be tied to the same potential as V_{DD}'.

V_{SS}
Negative Power Supply

Circuit ground for all sections of the MC145159-1 except the analog phase detector. V_{SS} must be tied to the same potential as V_{SS}'.

V_{SS}'
Analog Phase Detector Circuit Ground

Separate power supply and ground inputs are provided to help reduce the effects in the analog section of noise coming from the digital sections of this device and the surrounding circuitry.

V_{DD}'
Analog Power Supply

Separate power supply and ground inputs are provided to help reduce the effects in the analog section of noise coming from the digital sections of this device and the surrounding circuitry.

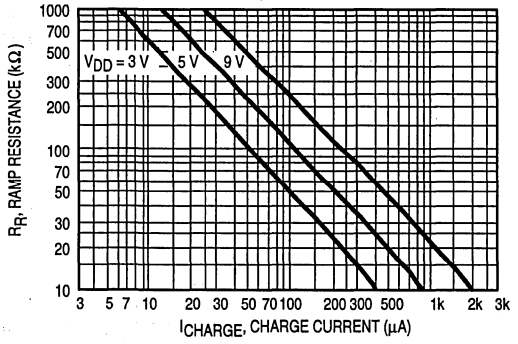


Figure 2. Charge Current versus Ramp Resistance

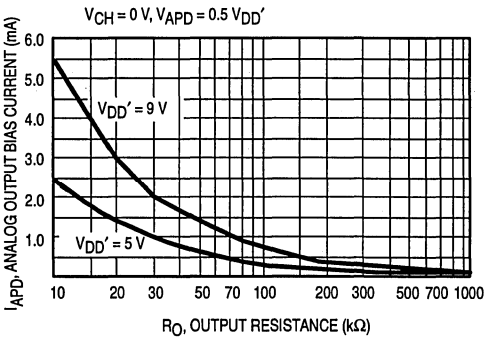


Figure 3. APD_{out} Bias Current vs Output Resistance

DESIGN EQUATION

$$K_\phi = \frac{I_{CHARGE}}{2\pi f_R C_R}$$

where
K_ϕ = phase detector gain, I_{CHARGE} is from Figure 2
f_R = reference frequency
C_R = ramp capacitor (in farads)

SWITCHING WAVEFORMS

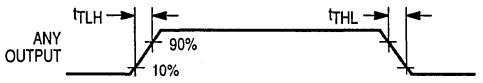


Figure 4.

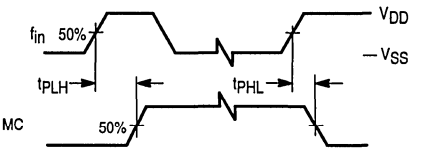


Figure 5.

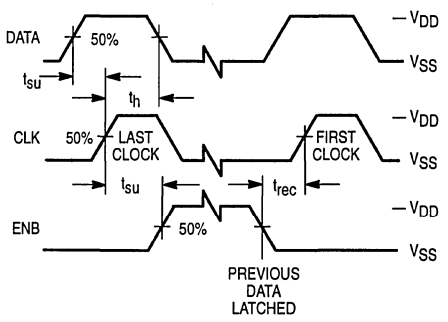


Figure 6.

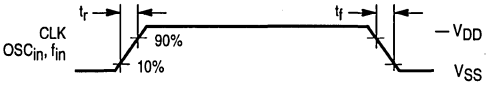


Figure 7.

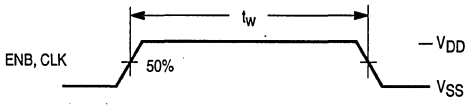


Figure 8.

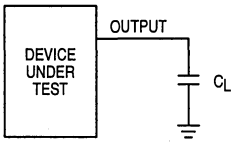


Figure 9. Test Circuit

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use Of A Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of sinking and sourcing 50 μA at CMOS logic levels may be direct or dc coupled to OSC_{in}. In general, the highest frequency capability is obtained utilizing a direct-coupled square wave having a rail-to-rail (V_{DD} to V_{SS}) voltage swing. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used. OSC_{out}, an unbuffered output, should be left floating.

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

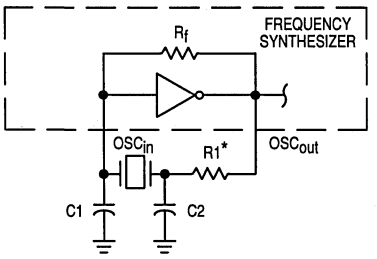
Design An Off-chip Reference

The user may design an off-chip crystal oscillator using ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in}. For large amplitude signals (standard CMOS logic levels), dc coupling is used. OSC_{out}, an unbuffered output, should be left floating. In general, the highest frequency capability is obtained with a direct-coupled square wave having rail-to-rail voltage swing.

Use Of The On-chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 10.

For V_{DD} = 5 V, the crystal should be specified for a loading capacitance, C_L, which does not exceed 32 pF for frequencies to approximately 8 MHz, 20 pF for frequencies in the area of 8 to 15 MHz, and 10 pF for higher frequencies. These are guidelines that provide a reasonable compromise between IC capacitance, drive capability, swamping variations in stray and IC input/output capacitance, and realistic C_L values. Assuming R1 = 0 Ω. the shunt load capacitance, C_L, presented across the crystal can be estimated to be: where



*May be deleted in certain cases. See text.

Figure 10. Pierce Crystal Oscillator Circuit

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

C_{in} = 5 pF (see Figure 11)
C_{out} = 6 pF (see Figure 11)
C_a = 1 pF (see Figure 11)
C1 and C2 = external capacitors (see Figure 10)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

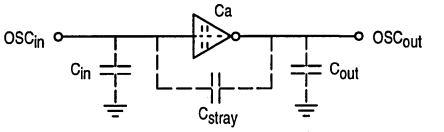
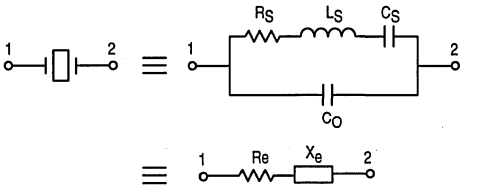


Figure 11. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 12. Equivalent Crystal Networks

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes zero in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 12. The maximum drive level specified by the crystal manufacturer represents the maximum stress that a crystal can withstand without damaging or excessive shift in operating frequency. R1 in Figure 10 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not overdrive the crystal, monitor the output frequency as a function of voltage at OSC_{out}. (Care should be taken to minimize loading.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal will decrease in frequency or become unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful. See Table 1.

RECOMMENDED READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit – Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2 Feb., 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June, 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May, 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

Table 2. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart St., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

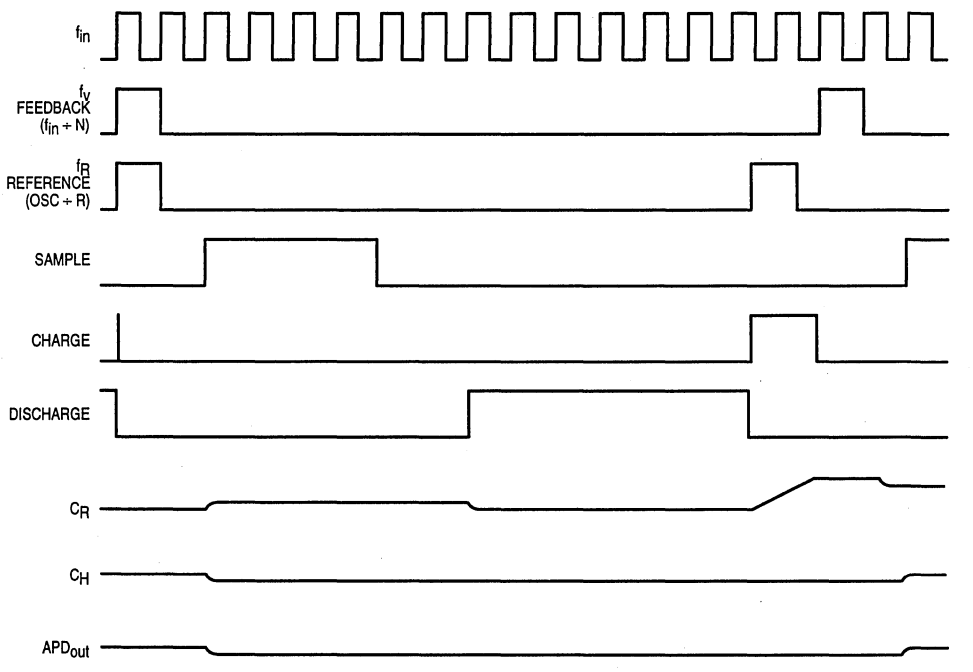


Figure 13. Timing Diagram for Minimum Divide Value (N = 16)

MC145160
MC145166
MC145167

Advance Information

Dual PLLs for 46/49 MHz Cordless Telephones

CMOS

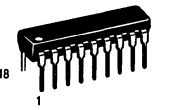
These devices are dual phase-locked loop (PLL) frequency synthesizers intended for use primarily in 46/49 MHz cordless phones with up to 10 channels. These parts contain two mask-programmable counter ROMs for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are shared by the receive and transmit circuits.

Frequency selection is accomplished via a 4-bit parallel input for the MC145160 and MC145166. The MC145167 utilizes a serial interface.

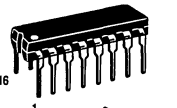
Other features include a lock detect circuit for the transmit loop, illegal code default, and a 5 kHz tone output.

- Synthesizes Up to Ten Channel Pairs
- Maximum Operating Frequency: 60 MHz @ V_{in} = 200 mVp-p
- Operating Temperature Range: −40 to +75°C
- Operating Voltage Range: 2.5 to 5.5 V
- On-Chip Oscillator Circuit Supports External Crystal
- Lock Detect Signal
- Operating Power Consumption: 3.0 mA @ 3.0 V
- Standby Mode for Power Savings: 1.5 mA @ 3.0 V

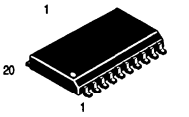
Part Number	4.0 kHz Output	Transmit Frequency	Channel Programming
MC145160	Yes	Half of Fundamental	BCD
MC145166	No	Fundamental	BCD
MC145167	No	Fundamental	Serial



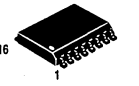
P SUFFIX
PLASTIC DIP
CASE 707



P SUFFIX
PLASTIC DIP
CASE 648



DW SUFFIX
SOG
CASE 751D



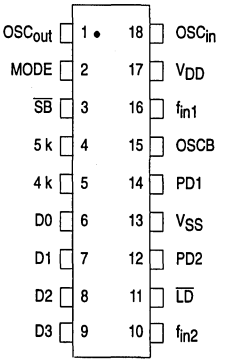
DW SUFFIX
SOG
CASE 751G

ORDERING INFORMATION

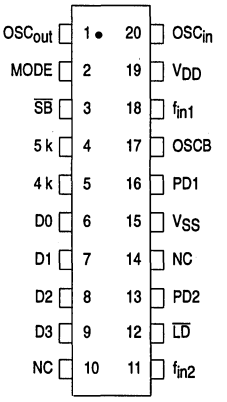
MC145160P	Plastic DIP
MC145160DW	SOG Package
MC145166P	Plastic DIP
MC145166DW	SOG Package
MC145167P	Plastic DIP
MC145167DW	SOG Package

PIN ASSIGNMENTS

MC145160P

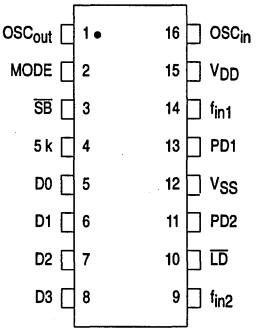


MC145160DW

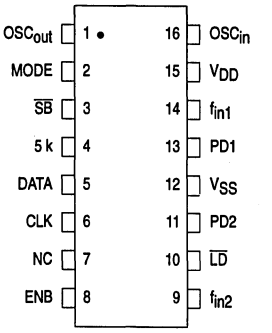


NC = NO CONNECTION

MC145166P
MC145166DW



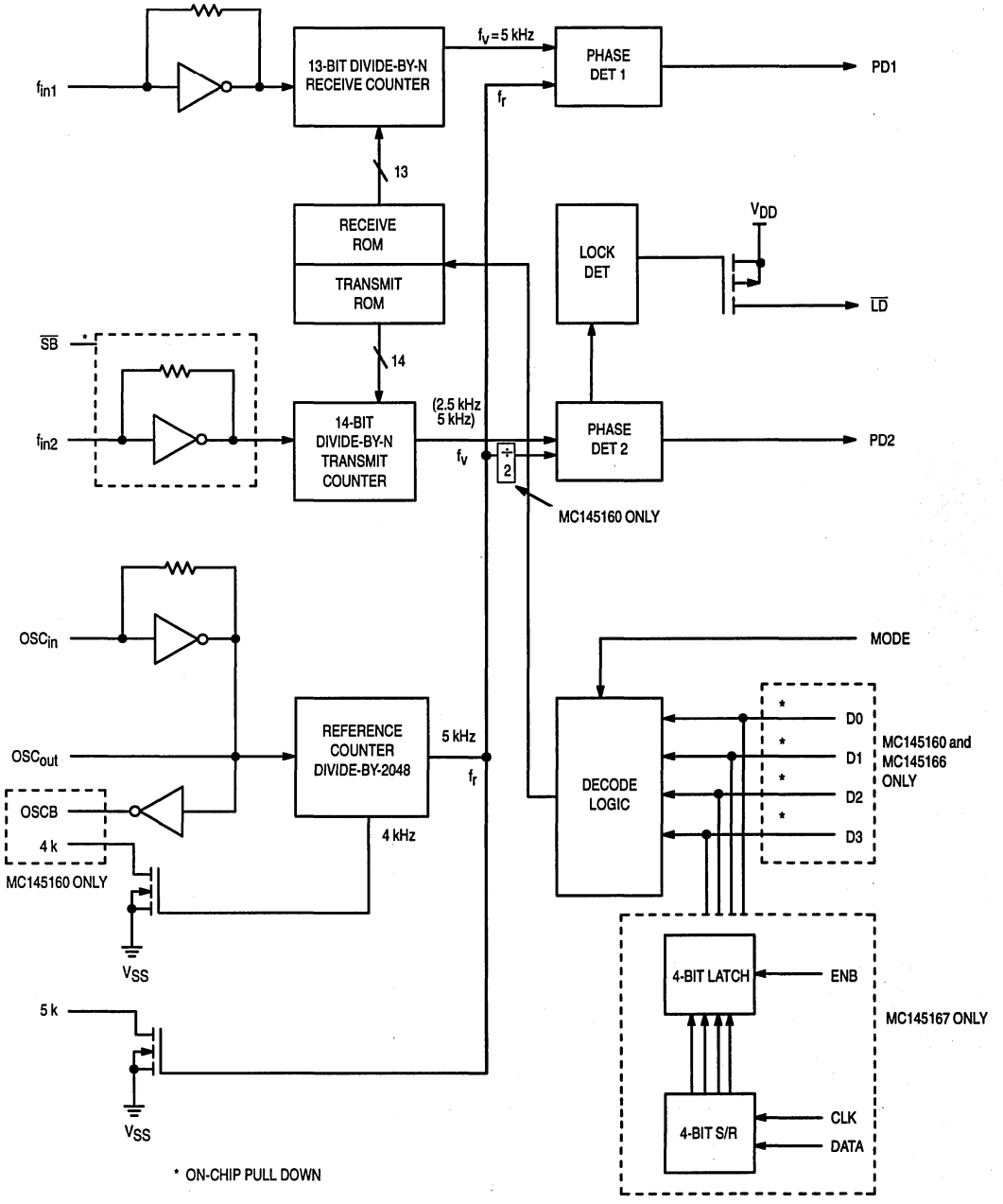
MC145167P
MC145167DW



NC = NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM OF THE MC145160, MC145166, AND MC145167



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +6.0	V
V_{in}	Input Voltage, All Inputs	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	−65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A=25°C)

Symbol	Characteristic		V_{DD}	Guaranteed Limit Min	Guaranteed Limit Max	Unit
V_{DD}	Power Supply Voltage Range		—	2.5	5.5	V
V_{OL}	Output Voltage (I_{out}=0)	0 Level	2.5 5.5	— —	0.05 0.05	V
V_{OH}	(V_{in}=V_{DD} or 0)	1 Level	2.5 5.5	2.45 5.45	— —	
V_{IL}	Input Voltage (V_{out}=0.5 V or V_{DD}−0.5 V)	0 Level	2.5 5.5	— —	0.75 1.65	V
V_{IH}		1 Level	2.5 5.5	1.75 3.85	— —	
I_{OH}	Output Current (V_{out}=2.2 V) (V_{out}=5.0 V)	Source	2.5 5.5	−0.18 −0.55	— —	mA
I_{OL}	(V_{out}=0.3 V) (V_{out}=0.5 V)	Sink	2.5 5.5	0.18 0.55	— —	
I_{IL}	Input Current (V_{in}=0)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	−30 −66	µA
		DATA, $\overline{SB}$, Mode	2.5 5.5	— —	−0.05 −0.11	
I_{IH}	(V_{in}=V_{DD}−0.5)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	30 66	µA
		DATA, $\overline{SB}$, Mode	2.5 5.5	— —	50 121	
C_{in}	Input Capacitance		—	—	8.0	pF
C_{out}	Output Capacitance		—	—	8.0	pF
I_{DD}	Standby Current, $\overline{SB}$=V_{SS} or Open		2.5 5.5	— —	1.4 3.6	mA
I_{dd}	Operating Current (200 mVp-p input at f_{in1} and f_{in2}, $\overline{SB}$=V_{DD})		2.5 5.5	— —	2.8 6.2	mA
I_{OZ}	Three-State Leakage Current (V_{out}=0 or 5.5 V)		5.5	—	±1.0	µA

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic	Figure #	V_{DD}	Guaranteed Limit Min	Guaranteed Limit Max	Unit
t_{TLH}	Output Rise Time	1, 5	3.0 5.0	— —	200 100	ns
t_{THL}	Output Fall Time	1, 5	3.0 5.0	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time, OSC_{in}	2	3.0 5.0	— —	5.0 4.0	µs
f_{max}	Input Frequency OSC_{in} Input = Sine Wave 200 mVp-p f_{in1} f_{in2}		3.0–5.0 3.0–5.0 3.0–5.0	— — —	12 60 60	MHz
t_{su}	Setup Time (MC145167) DATA to CLK	3	3.0 5.0	100 50	— —	ns
	ENB to CLK		3.0 5.0	200 100	— —	
t_h	Hold Time (MC145167), CLK to DATA	3	3.0 5.0	80 40	— —	ns
t_{rec}	Recovery Time (MC145167), ENB to CLK	3	3.0 5.0	80 40	— —	ns
t_w	Input Pulse Width (MC145167), CLK and ENB	4	3.0 5.0	80 60	— —	ns

SWITCHING WAVEFORMS

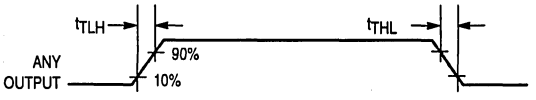


Figure 1.

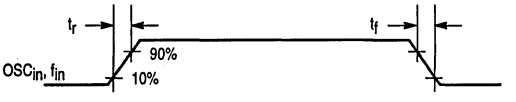


Figure 2.

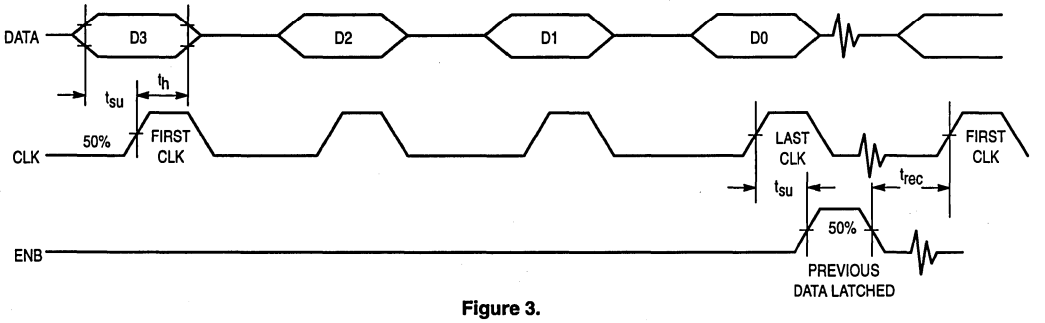


Figure 3.

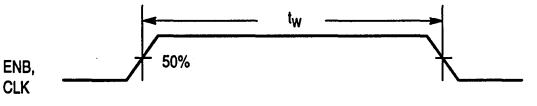


Figure 4.

PIN DESCRIPTIONS

INPUTS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output
These pins form a reference oscillator when connected to an external parallel-resonant crystal. For a 46/49 MHz cordless phone application, a 10.24-MHz crystal is needed. OSC_{in} may also serve as input for an externally generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required for OSC_{out}.

MODE
Mode is for determining whether the part is to be used in the base or handset of a cordless phone. Internally, this pin is used in the decoding logic for selecting the ROM address. When high, the device is set in the base mode, and when low, it is set in the handset mode. This input has an internal pull-down device.

$\overline{SB}$
Standby Input
The standby pin is used to save power when not transmitting. When high, both the transmit and receive loops are in operation. When low, the transmit loop is disabled, thereby reducing power consumption. This input has an internal pull-down device.

D0–D3
Data Inputs
These inputs provide the BCD code for selecting the one of ten channels to be locked in both the transmit and receive loop. When address data other than 1–10 are input, the decoding logic defaults to channel 10. The frequency assignments with reference to Mode and D0–D3 are shown in Table 1. These inputs have internal pull-down devices.

f_{in1}, f_{in2}
Frequency Inputs
f_{in1} and f_{in2} are inputs to the divide-by-N receive and transmit counters, respectively. These signals are typically derived from the loop VCO and are ac coupled. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used. The minimum input level is 200 mVp-p.

CLK, DATA
Clock, Data
These pins provide the BCD input by using serial channel programming instead of parallel. Logical high represents a 1. Each low-to-high transition of the clock shifts one bit of data into the on-chip shift register.

ENB
Enable
The enable pin controls the data transfer from the shift register to the 4-bit latch. A positive pulse latches the data.

OUTPUTS

5k, 4k
5-kHz and 4-kHz Tone Signals
These are 5-kHz and 4-kHz tone signals derived from the reference oscillator, these are N-channel open-drain outputs.

$\overline{LD}$
Lock Detect Signal
The lock detect signal is associated with the transmit loop. The lock output goes high to indicate an out-of-lock condition. This is a P-channel open-drain output.

PD1, PD2
Phase Detector Outputs
These are three-state outputs of the transmit and receive phase detectors for use as loop error signals.
Frequency $f_V > f_r$ or f_V leading: Output = Negative pulses
Frequency $f_V < f_r$ or f_V lagging: Output = Positive pulses
Frequency $f_V = f_r$ and phase coincidence:
Output = High-impedance state

OSCB
Buffered Reference Oscillator
Buffered output of the on-chip reference oscillator or externally provided reference. This output is available on the MC145160 only.

POWER SUPPLY

V_{SS}
Negative Power Supply
This pin is the negative supply potential and is usually ground.

V_{DD}
Positive Power Supply
This pin is the positive supply potential and may range from + 2.5 to + 5.5 V with respect to V_{SS}.

Table 1. MC145166/67 Divide Ratios and VCO Frequencies

Channels					Handset (Mode=0)				Base (Mode=1)			
					f_{in2}—Transmit		f_{in1}—Receive		f_{in2}—Transmit		f_{in1}—Receive	
D3	D2	D1	D0	CH#	F_{VCO} (MHz)	÷N	F_{VCO} (MHz)	÷N	F_{VCO} (MHz)	÷N	F_{VCO} (MHz)	÷N
0	0	0	1	1	49.670	9934	35.915	7183	46.610	9322	38.975	7795
0	0	1	0	2	49.845	9969	35.935	7187	46.630	9326	39.150	7830
0	0	1	1	3	49.860	9972	35.975	7195	46.670	9334	39.165	7833
0	1	0	0	4	49.770	9954	36.015	7203	46.710	9342	39.075	7815
0	1	0	1	5	49.875	9975	36.035	7207	46.730	9346	39.180	7836
0	1	1	0	6	49.830	9966	36.075	7215	46.770	9354	39.135	7827
0	1	1	1	7	49.890	9978	36.135	7227	46.830	9366	39.195	7839
1	0	0	0	8	49.930	9986	36.175	7235	46.870	9374	39.235	7847
1	0	0	1	9	49.990	9998	36.235	7247	46.930	9386	39.295	7859
1	0	1	0	10	49.970	9994	36.275	7255	46.970	9394	39.275	7855

NOTES:
1. Other input combinations will be defaulted to channel 10
2. Half the frequency of f_{in2} for MC145160
3. 0 = logic low, 1 = logic high.

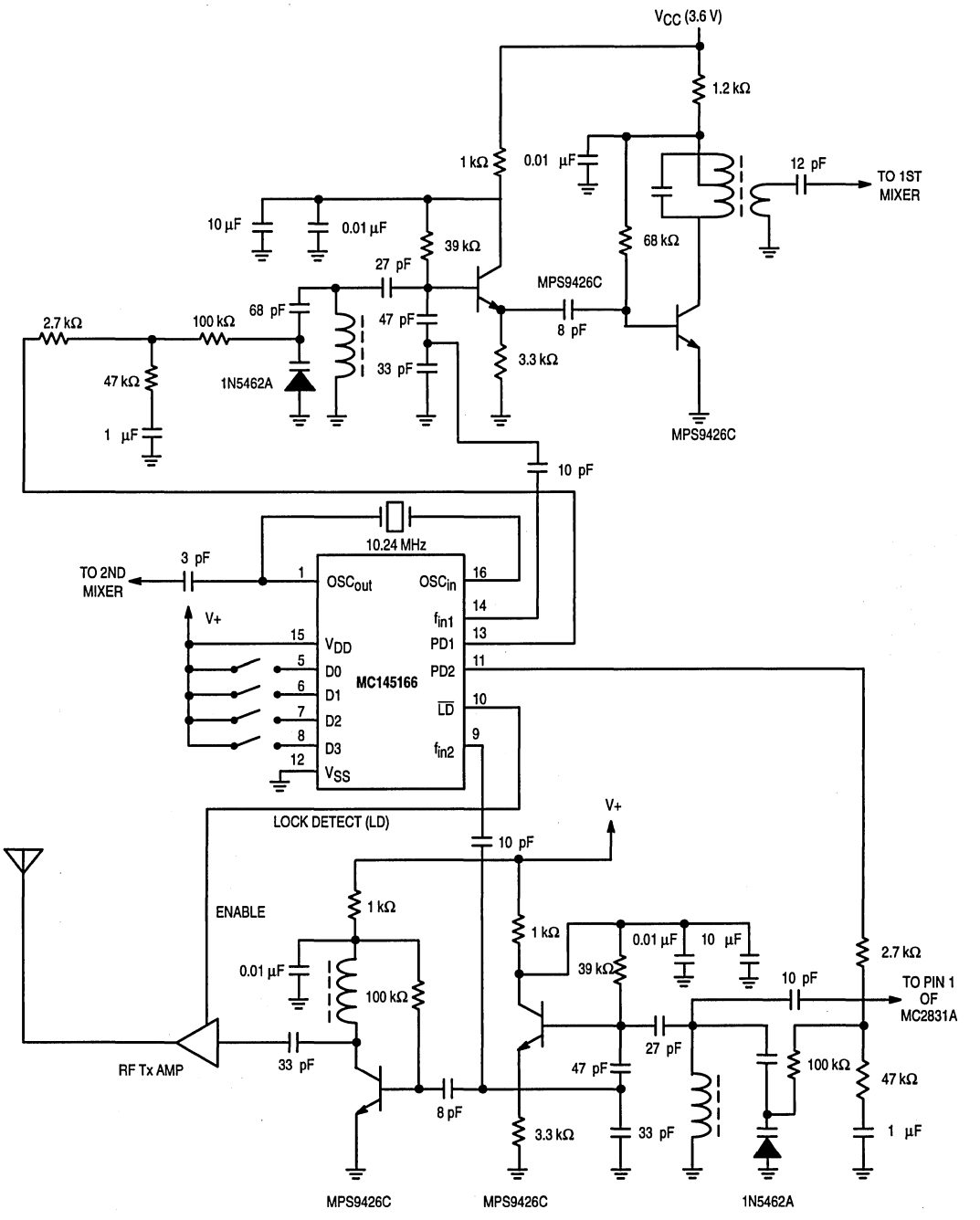


Figure 5. MC145166 Circuit Example

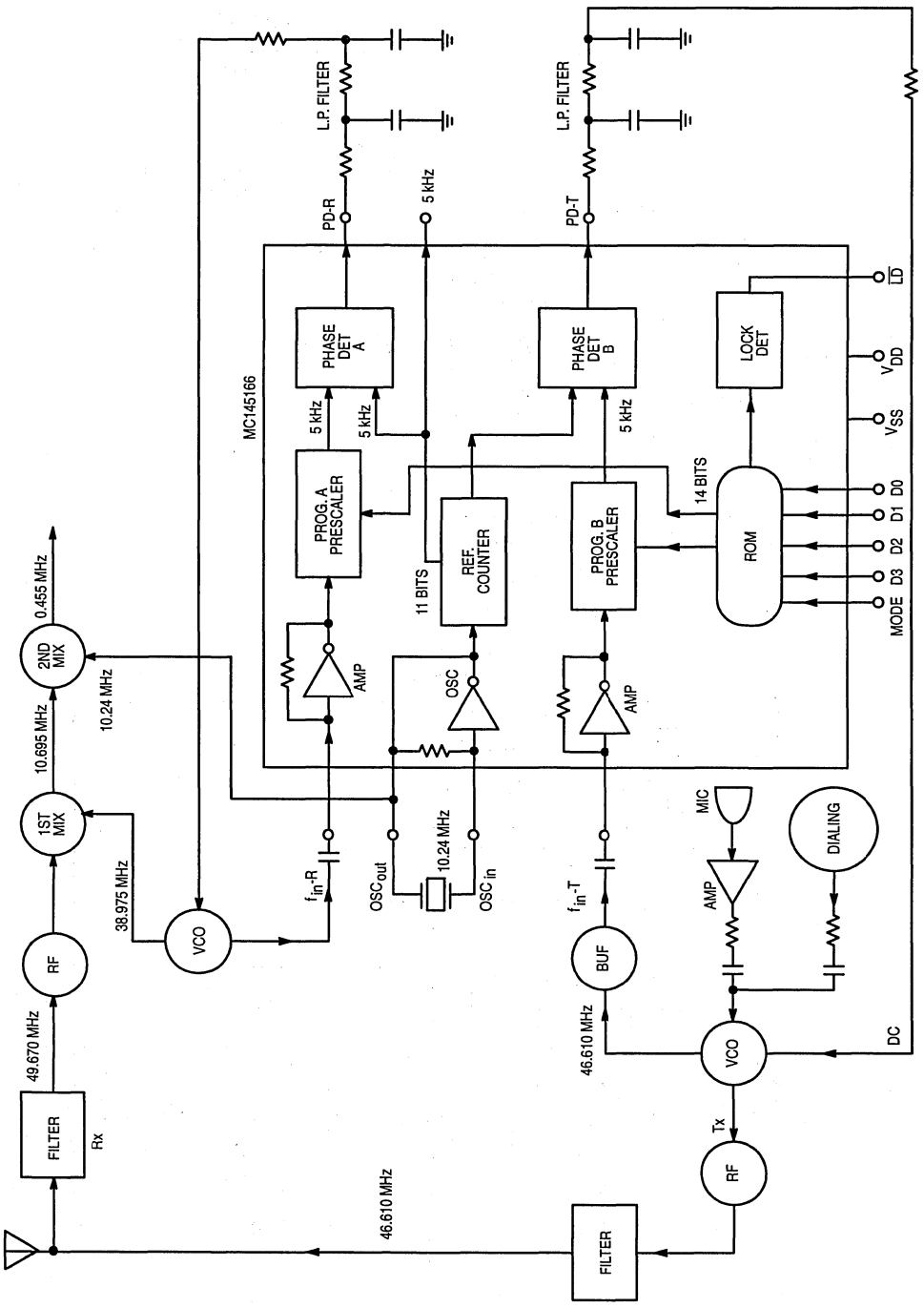


Figure 6. DPLL Application in 46/49 MHz Cordless Phone

MC145161

Advance Information

Dual PLL for 30/39 MHz Cordless Telephones

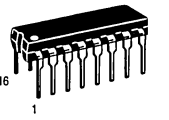
CMOS

The MC145161 is a dual phase-locked loop (PLL) frequency synthesizer intended for use primarily in 30/39 MHz cordless phones with up to 10 channels. This part contains two mask-programmable counter ROMs for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are shared by the receive and transmit circuits.

Frequency selection is accomplished via a 4-bit serial input.

Other features include a lock detect circuit for the transmit loop, illegal code default, and a 5-kHz tone output.

- Applications: Bases and Handsets of Cordless Phones for the Australian Market
- Synthesizes Up to Ten Channel Pairs
- Maximum Operating Frequency: 60 MHz @ V_{in} = 200 mVp-p
- Operating Temperature Range: −40 to +75°C
- Operating Voltage Range: 2.5 to 5.5 V
- On-Chip Oscillator Circuit Supports External Crystal
- Lock Detect Signal
- Operating Power Consumption: 3.0 mA @ 3.0 V
- Standby Mode for Power Savings: 1.5 mA @ 3.0 V



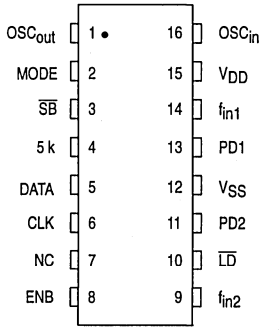
P SUFFIX
PLASTIC DIP
CASE 648

DW SUFFIX
SOG
CASE 751G

ORDERING INFORMATION

MC145161P	Plastic DIP
MC145161DW	SOG Package

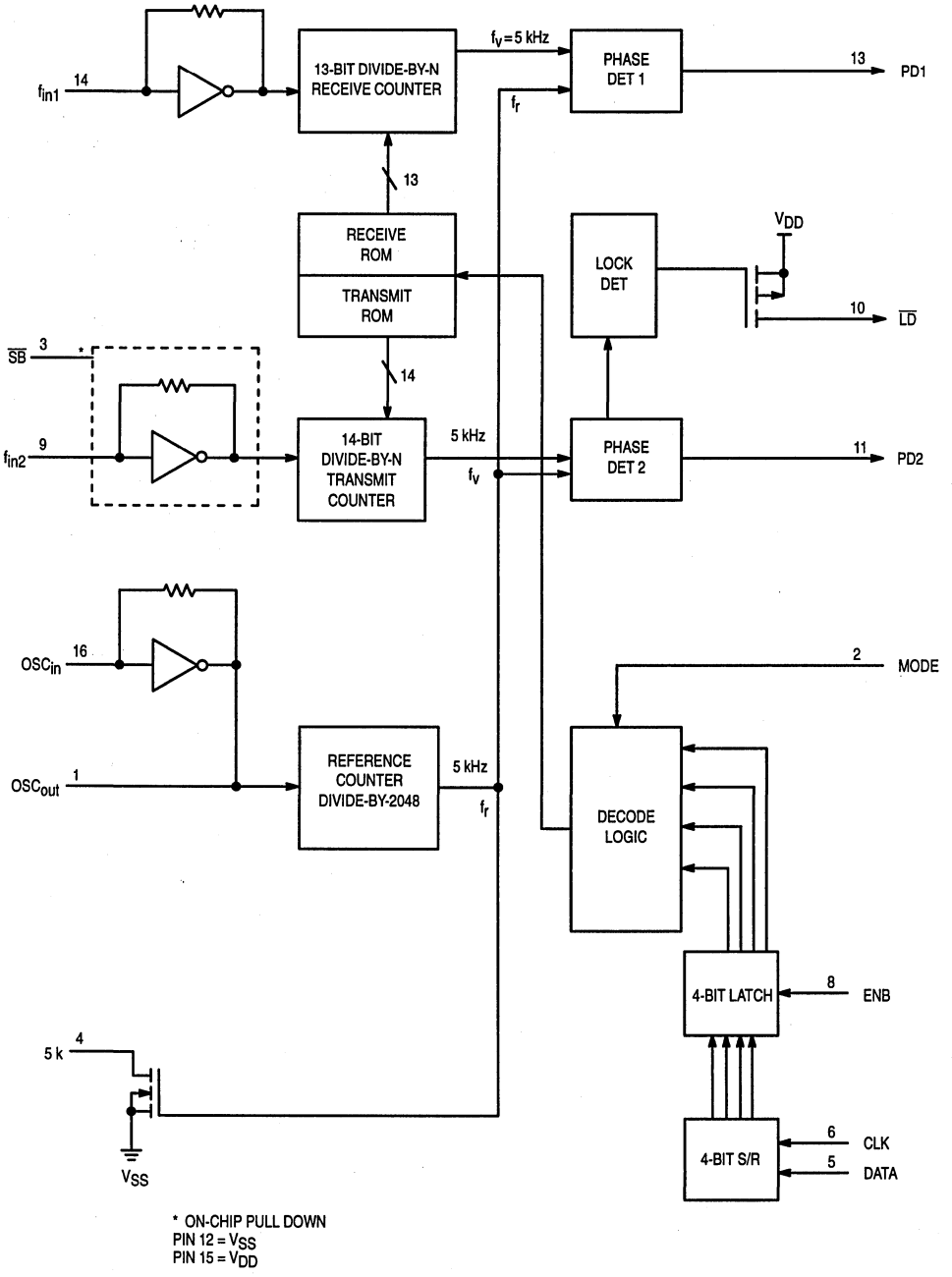
PIN ASSIGNMENT



NC = NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM OF THE MC145161



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +6.0	V
V_{in}	Input Voltage, All Inputs	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	−65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A=25°C)

Symbol	Characteristic		V_{DD}	Guaranteed Limit		Unit
				Min	Max	
V_{DD}	Power Supply Voltage Range		—	2.5	5.5	V
V_{OL}	Output Voltage (I_{out}=0)	0 Level	2.5 5.5	— —	0.05 0.05	V
V_{OH}	(V_{in}=V_{DD} or 0)	1 Level	2.5 5.5	2.45 5.45	— —	
V_{IL}	Input Voltage (V_{out}=0.5 V or V_{DD}−0.5 V)	0 Level	2.5 5.5	— —	0.75 1.65	V
V_{IH}		1 Level	2.5 5.5	1.75 3.85	— —	
I_{OH}	Output Current (V_{out}=2.2 V) (V_{out}=5.0 V)	Source	2.5 5.5	−0.18 −0.55	— —	mA
I_{OL}	(V_{out}=0.3 V) (V_{out}=0.5 V)	Sink	2.5 5.5	0.18 0.55	— —	
I_{IL}	Input Current (V_{in}=0)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	−30 −66	µA
		Data, $\overline{SB}$, Mode	2.5 5.5	— —	−0.05 −0.11	
I_{IH}	(V_{in}=V_{DD}−0.5)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	30 66	µA
		Data, $\overline{SB}$, Mode	2.5 5.5	— —	50 121	
C_{in}	Input Capacitance		—	—	8.0	pF
C_{out}	Output Capacitance		—	—	8.0	pF
I_{DD}	Standby Current, $\overline{SB}$=V_{SS} or Open		2.5 5.5	— —	1.4 3.6	mA
I_{dd}	Operating Current (200 mVp-p input at f_{in1} and f_{in2}, $\overline{SB}$=V_{DD})		2.5 5.5	— —	2.8 6.2	mA
I_{OZ}	Three-State Leakage Current (V_{out}=0 or 5.5 V)		5.5	—	±1.0	µA

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic	Figure #	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}	Output Rise Time	1, 5	3.0 5.0	— —	200 100	ns
t_{THL}	Output Fall Time	1, 5	3.0 5.0	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time, OSC_{in}	2	3.0 5.0	— —	5.0 4.0	µs
f_{max}	Input Frequency OSC_{in} Input = Sine Wave 200 mVp-p f_{in1} f_{in2}		3.0–5.0 3.0–5.0 3.0–5.0	— — —	12 60 60	MHz
t_{su}	Setup Time DATA to CLK	3	3.0 5.0	100 50	— —	ns
	ENB to CLK		3.0 5.0	200 100	— —	
t_h	Hold Time, CLK to DATA	3	3.0 5.0	80 40	— —	ns
t_{rec}	Recovery Time, ENB to CLK	3	3.0 5.0	80 40	— —	ns
t_W	Input Pulse Width, CLK and ENB	4	3.0 5.0	80 60	— —	ns

SWITCHING WAVEFORMS

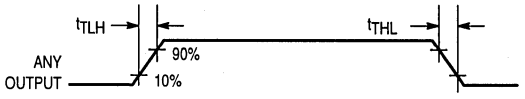


Figure 1.

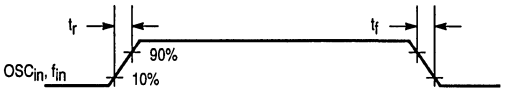


Figure 2.

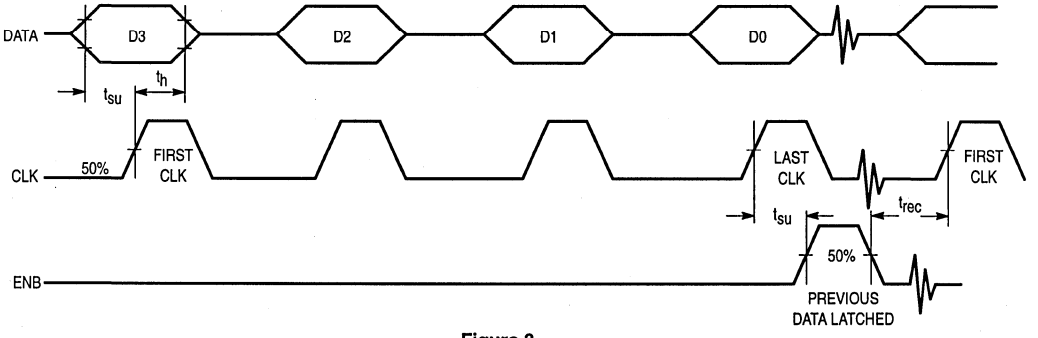


Figure 3.

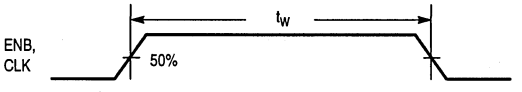


Figure 4.

PIN DESCRIPTIONS

INPUTS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 16, 1)
These pins form a reference oscillator when connected to an external parallel-resonant crystal. For a 30/39 MHz cordless phone application, a 10.24-MHz crystal is needed. OSC_{in} may also serve as input for an externally generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required for OSC_{out}.

MODE
(Pin 2)
Mode is for determining whether the part is to be used in the base or handset of a cordless phone. Internally, this pin is used in the decoding logic for selecting the ROM address. When high, the device is set in the base mode, and when low, it is set in the handset mode. This input has an internal pull-down device.

$\overline{SB}$
Standby Input (Pin 3)
The standby pin is used to save power when not transmitting. When high, both the transmit and receive loops are in operation. When low, the transmit loop is disabled, thereby reducing power consumption. This input has an internal pull-down device.

f_{in1}, f_{in2}
Frequency Inputs (Pins 14, 9)
f_{in1} and f_{in2} are inputs to the divide-by-N receive and transmit counters, respectively. These signals are typically derived from the loop VCO and are ac coupled. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used. The minimum input level is 200 mVp-p.

CLK, DATA
Clock, Data (Pins 6, 5)
These pins provide the BCD input by using serial channel programming. Logical high represents a 1. Each low-to-high transition of the clock shifts one bit of data into the on-chip shift register.

ENB
Enable (Pin 8)
The enable pin controls the data transfer from the shift register to the 4-bit latch. A positive pulse latches the data.

OUTPUTS

5 k
5-kHz Tone Signal (Pin 4)
This 5-kHz tone signal is derived from the reference oscillator; this is an N-channel open-drain output.

$\overline{LD}$
Lock Detect Signal (Pin 10)
The lock detect signal is associated with the transmit loop. The lock output goes high to indicate an out-of-lock condition. This is a P-channel open-drain output.

PD1, PD2
Phase Detector Outputs (Pins 13, 11)
These are three-state outputs of the transmit and receive phase detectors for use as loop error signals.
Frequency $f_V > f_r$ or f_V leading: Output=Negative pulses
Frequency $f_V < f_r$ or f_V lagging: Output=Positive pulses
Frequency $f_V = f_r$ and phase coincidence: Output High-Impedance state

POWER SUPPLY

V_{SS}
Negative Power Supply (Pin 12)
This pin is the negative supply potential and is usually ground.

V_{DD}
Positive Power Supply (Pin 15)
This pin is the positive supply potential and may range from +2.5 to +5.5 V with respect to V_{SS}.

Table 1. Divide Ratios and VCO Frequencies (used for the Australian Market)

Channels					Handset (Mode=0)				Base (Mode=1)			
					f_{in2}—Transmit		f_{in1}—Receive		f_{in2}—Transmit		f_{in1}—Receive	
D3	D2	D1	D0	CH#	F_{VCO} (MHz)	÷N	F_{VCO} (MHz)	÷N	F_{VCO} (MHz)	÷N	F_{VCO} (MHz)	÷N
0	0	0	1	1	39.775	7955	19.380	3876	30.075	6015	29.080	5816
0	0	1	0	2	39.825	7965	19.430	3886	30.125	6025	29.130	5826
0	0	1	1	3	39.875	7975	19.480	3896	30.175	6035	29.180	5836
0	1	0	0	4	39.925	7985	19.530	3906	30.225	6045	29.230	5846
0	1	0	1	5	39.975	7995	19.580	3916	30.275	6055	29.280	5856
0	1	1	0	6	39.800	7960	19.405	3881	30.100	6020	29.105	5821
0	1	1	1	7	39.850	7970	19.455	3891	30.150	6030	29.155	5831
1	0	0	0	8	39.900	7980	19.505	3901	30.200	6040	29.205	5841
1	0	0	1	9	39.950	7990	19.555	3911	30.250	6050	29.255	5851
1	0	1	0	10	40.000	8000	19.605	3921	30.300	6060	29.305	5861

NOTES:
1. Other input combinations will be defaulted to channel 10
2. 0 = logic low, 1 = logic high
3. First IF = 10.695 MHz

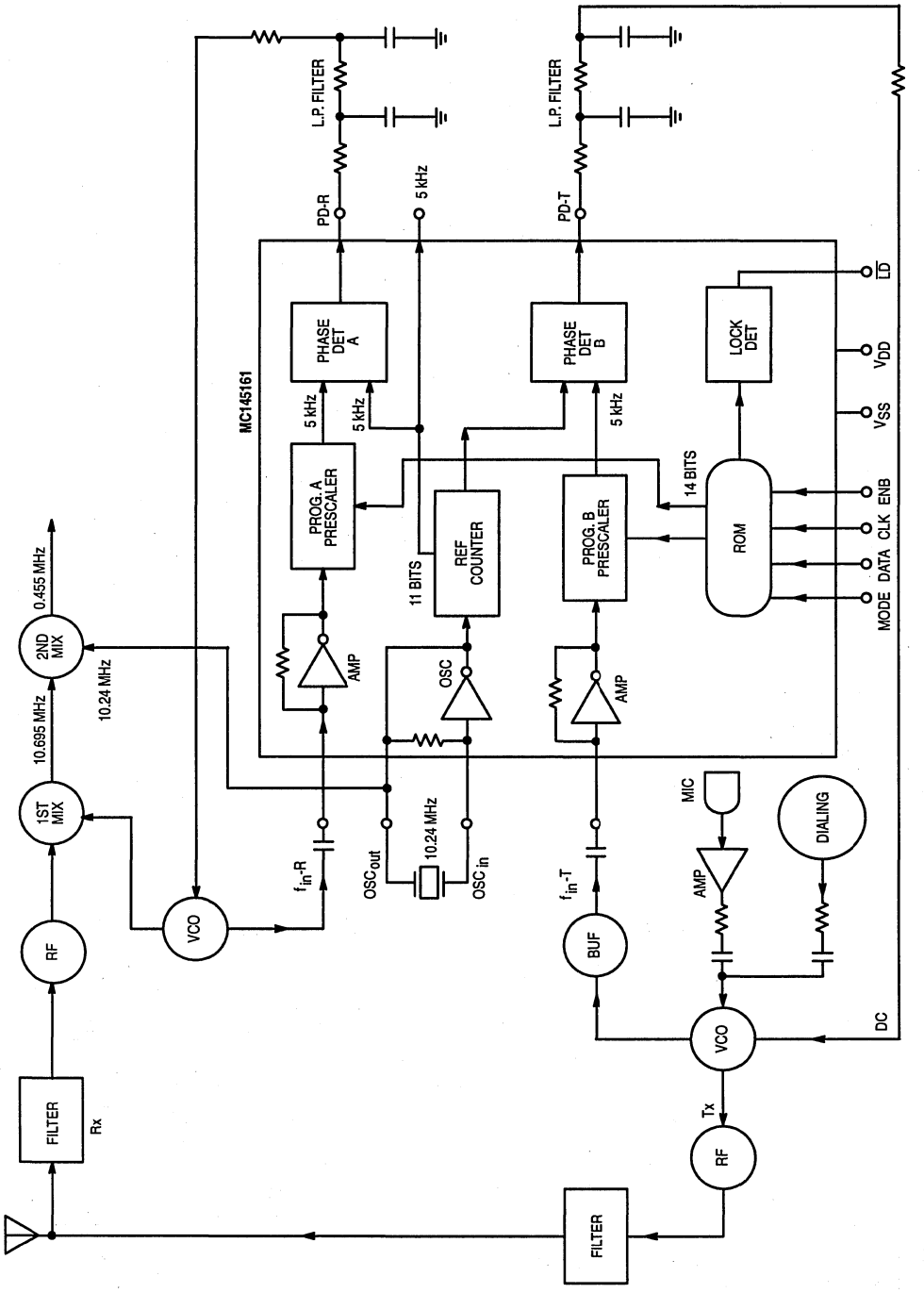


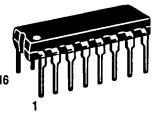
Figure 5. DPLL Application in 30/39 MHz Cordless Phone

MC145162

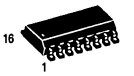
Advance Information

60 MHz Universal Programmable Dual PLL Frequency Synthesizer

CMOS



P SUFFIX
PLASTIC DIP
CASE 648



D SUFFIX
SOG
CASE 751B

ORDERING INFORMATION

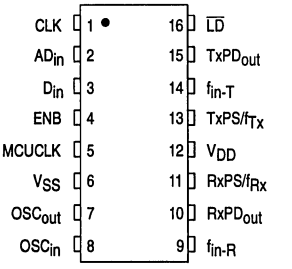
MC145162P	Plastic DIP
MC145162D	SOG

The MC145162 is a dual phase-locked loop (PLL) frequency synthesizer especially designed for CT-1 cordless phone applications worldwide. This frequency synthesizer is also for any products with frequency operation at 60 MHz or below.

The device features fully programmable receive, transmit, reference, and auxiliary reference counters accessed through an MCU serial interface. This feature allows this device to operate in any CT–1 cordless phone application. The device consists of two independent phase detectors for transmit and receive loops. A common reference oscillator, driving two independent reference frequency counters, provides independent reference frequencies for transmit and receive loops. The auxiliary reference counter allows the user to select an additional reference frequency for receive and transmit loops if required.

- Operating Voltage Range: 2.5 to 5.5 V
- Operating Temperature Range: – 40 to +75°C
- Operating Power Consumption: 3.0 mA @ 2.5 V
- Maximum Operating Frequency: 60 MHz @ 200 mVp-p, V_{DD} = 2.5 V
- 3 or 4 Pins Used for Serial MCU Interface
- Built-In MCU Clock Output with Frequency of Reference Oscillator ÷ 3/÷ 4
- Power Saving Mode Controlled by MCU
- Lock Detect Signal
- On-Chip Reference Oscillator Supports External Crystals to 16.0 MHz
- Reference Frequency Counter Division Range: 16 to 4095
- Auxiliary Reference Frequency Counter Division Range: 16 to 16,383
- Transmit Counter Division Range: 16 to 65,535
- Receive Counter Division Range: 16 to 65,535

PIN ASSIGNMENT



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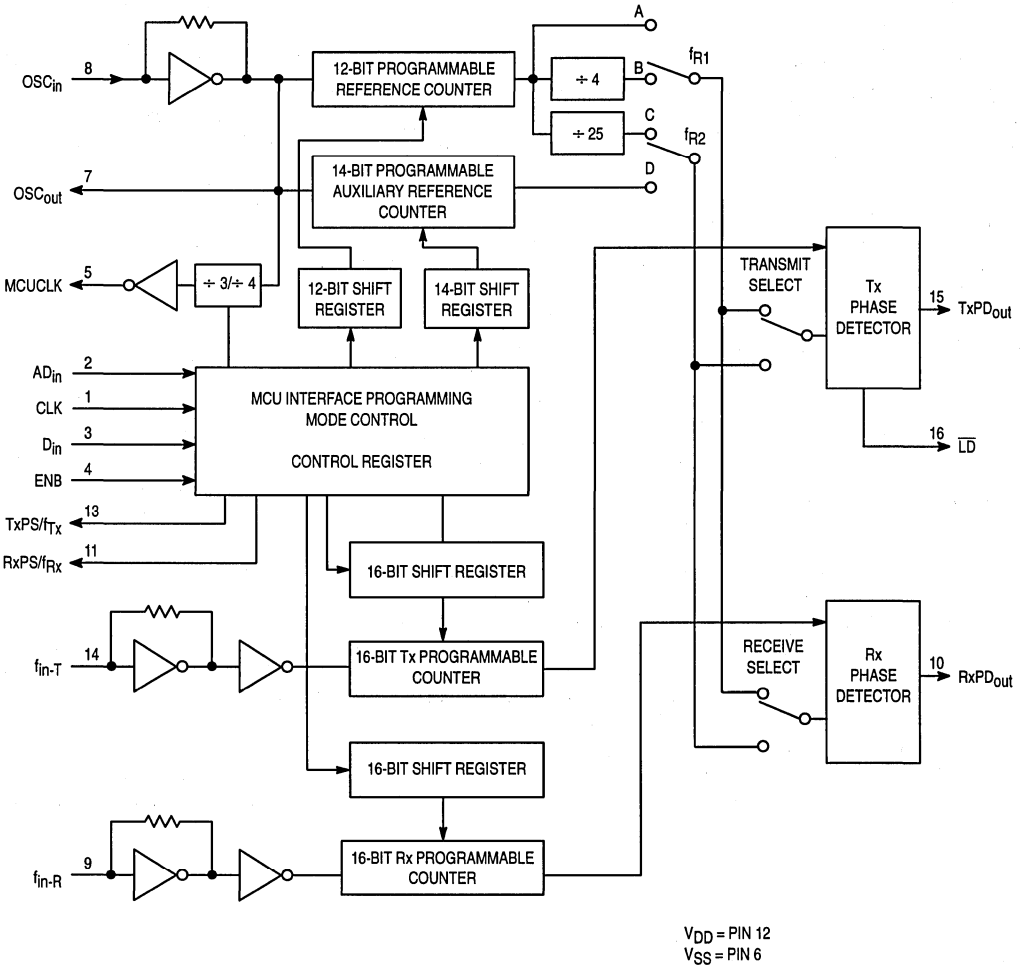
REV. 1

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	− 0.5 to + 6.0	V
V_{in}	Input Voltage, All Inputs	− 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	−65 to + 150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused pins must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C)

Symbol	Characteristic		V_{DD}	Guaranteed Limit Min	Guaranteed Limit Max	Unit
V_{DD}	Power Supply Voltage Range		—	2.5	5.5	V
V_{OL}	Output Voltage (I_{out} = 0)	0 Level	2.5 5.5	— —	0.1 0.1	
V_{OH}	(V_{in} = V_{DD} or 0)	1 Level	2.5 5.5	2.45 5.45	— —	V
V_{IL}	Input Voltage (V_{out} = 0.5 V or V_{DD} − 0.5 V)	0 Level	2.5 5.5	— —	0.75 1.65	V
V_{IH}		1 Level	2.5 5.5	1.75 3.85	— —	
I_{OH}	Output Current (V_{out} = 2.2 V) (V_{out} = 5.0 V)	Source	2.5 5.5	−0.18 −0.55	— —	mA
I_{OL}	(V_{out} = 0.3 V) (V_{out} = 0.5 V)	Sink	2.5 5.5	0.18 0.55	— —	
I_{IL}	Input Current (V_{in} = 0)	OSC_{in}, f_{in-T}, f_{in-R}	2.5 5.5	— —	−30 −66	µA
		AD_{in}, CLK, D_{in}, ENB	2.5 5.5	— —	−1.0 −1.0	
I_{IH}	(V_{in} = V_{DD} − 0.5)	OSC_{in}, f_{in-T}, f_{in-R}	2.5 5.5	— —	30 66	µA
		AD_{in}, CLK, D_{in}, ENB	2.5 5.5	— —	5.0 5.0	
I_{OZ}	Three-State Leakage Current (V_{out} = 0 V or 5.5 V)		5.5	—	±100	nA
C_{in}	Input Capacitance		—	—	8.0	pF
C_{out}	Output Capacitance		—	—	8.0	pF
$I_{DD(stdby)}$	Standby Current (All Counters are in Power-Down Mode with Oscillator On)		2.5 5.5	— —	0.3 1.5	mA
I_{DD}	Operating Current (200 mVp-p input at f_{in-T} = 60 MHz and f_{in-R} = 60 MHz, OSC = 10.24 MHz)		2.5 5.5	— —	3.0 10	mA

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic	Figure #	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}	Output Rise Time	1	2.5 5.5	— —	200 100	ns
t_{THL}	Output Fall Time	1	2.5 5.5	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time, OSC_{in}	2	2.5 5.5	— —	5.0 4.0	µs
t_w	Input Pulse Width, CLK and ENB	3	2.5 5.5	80 60	— —	ns
f_{max}	Input Frequency (OSC_{in}) (Input = Sine Wave @ ≥ 200 mVp-p (f_{in-T}) (f_{in-R})		2.5–5.5 2.5–5.5 2.5–5.5	— — —	16 60 60	MHz
t_{su}	Setup Time Data to CLK ENB to CLK	5	2.5–5.5 2.5–5.5	100 200	— —	ns
t_h	Hold Time, CLK to Data	5	2.5 5.5	80 40	— —	ns
t_{rec}	Recovery Time, ENB to CLK	5	2.5 5.5	80 40	— —	ns
t_{su1}	Setup Time, ENB to CLK	4	2.5–5.5	80	—	ns
t_{h1}	Hold Time, CLK to ENB	4	2.5–5.5	600	—	ns

SWITCHING WAVEFORMS

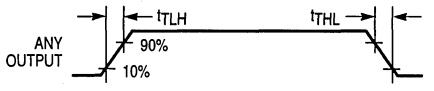


Figure 1.

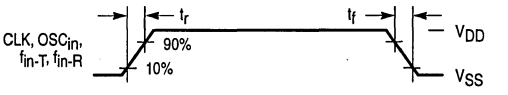


Figure 2.

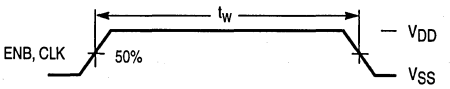


Figure 3.

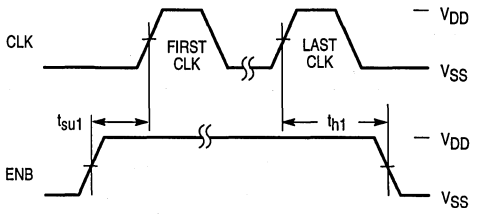


Figure 4. ENB High During Serial Transfer

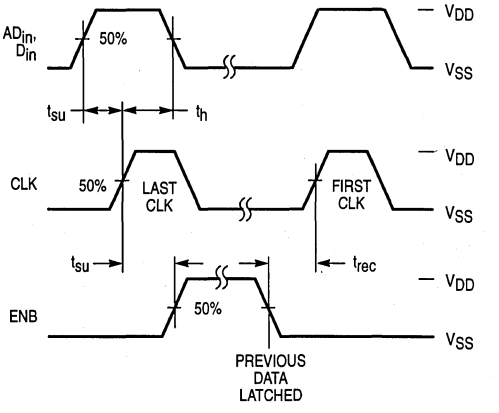


Figure 5. ENB Low During Serial Transfer

PIN DESCRIPTIONS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 8, 7)

These pins form a reference oscillator when connected to an external parallel-resonant crystal. Figure 6 shows the relationship of different crystal frequencies and reference frequencies for cordless phone applications in various countries. OSC_{in} may also serve as input for an externally generated reference signal which is typically ac coupled.

MCUCLK
System Clock (Pin 5)

This output pin provides a signal of the crystal frequency (OSC_{out}) divided by 3 or 4 that is controlled by a bit in the control register.

This signal can be a clock source for the MCU or other system clocks.

AD_{in}, D_{in}, CLK, ENB
Auxiliary Data In, Data In, Clock, Enable (Pins 2, 3, 1, 4)

These four pins provide an MCU serial interface for programming the reference counter, the transmit-channel counter, and the receive-channel counter. They also provide various controls of the PLL including the power saving mode and the programming format.

$TxPS/f_{Tx}$, $RxPS/f_{Rx}$
Transmit Power Save, Receive Power Save (Pins 13, 11)

For a normal application, these output pins provide the status of the internal power saving mode operation. If the transmit-channels counter circuitry is in power down mode, $TxPS/f_{Tx}$ outputs a high state. If the receive-channels counter circuitry is in power down mode, $RxPS/f_{Rx}$ is set high. These outputs can be applied for controlling the external power switch for the transmitter and the receiver to save MCU control pins.

In the Tx/Rx channel counter test mode, the $TxPS/f_{Tx}$ and $RxPS/f_{Rx}$ pins output the divided value of the transmit channel counter (f_{Tx}) and the receive channel counter (f_{Rx}), respectively. This test mode operation is controlled by the control register. Details of the counter test mode are in the **Tx/Rx Channel Counter Test** section of this data sheet.

f_{in-T}/f_{in-R}
Transmit/Receive Counter Inputs (Pins 14, 9)

f_{in-T} and f_{in-R} are inputs to the transmit and the receive counters, respectively. These signals are typically driven from the loop VCO and ac-coupled. The minimum input signal level is 200 mVp-p @ 60.0 MHz.

$TxPD_{out}/RxPD_{out}$
Transmit/Receive Phase Detector Outputs (Pins 15, 10)

These are three-state outputs of the transmit and receive phase detectors for use as loop error signals (see Figure 7 for phase detector output waveforms).

Frequency $f_V > f_R$ or f_V leading: output = negative pulse.

Frequency $f_V < f_R$ or f_V lagging: output = positive pulse.

Frequency $f_V = f_R$ and phase coincidence: output = high-impedance state.

f_R is the divided-down reference frequency at the phase detector input and f_V is the divided-down VCO frequency at the phase detector input.

$\overline{LD}$
Lock Detect (Pin 16)

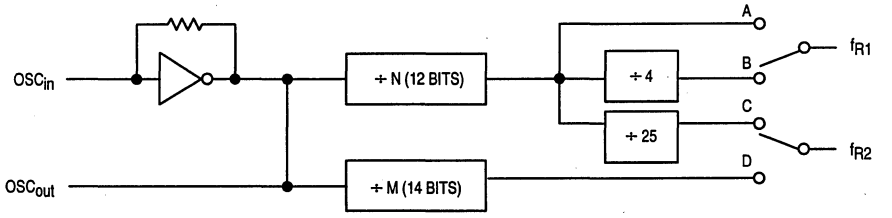
The lock detect signal is associated with the transmit loop. The output at a high level indicates an out-of-lock condition (see Figure 7 for the $\overline{LD}$ output waveform).

V_{DD}
Positive Power Supply (Pin 12)

V_{DD} is the most positive power supply potential ranging from 2.5 to 5.5 V with respect to V_{SS}.

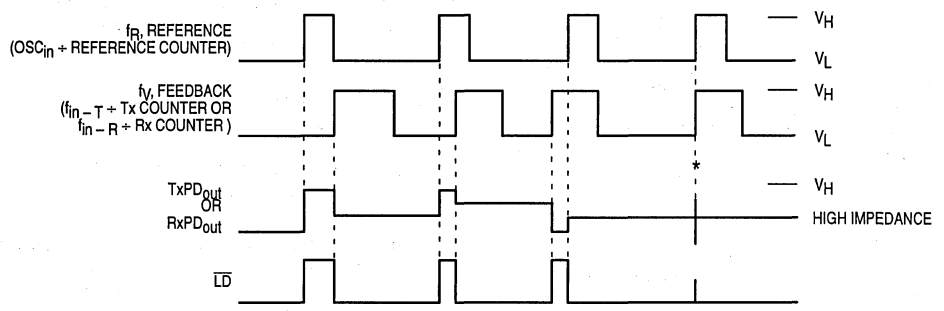
V_{SS}
Negative Power Supply (Pin 6)

V_{SS} is the most negative supply potential and is usually connected to ground.



Crystal	÷ N Value	$f_{R1 \rightarrow B}$	$f_{R2 \rightarrow C}$
11.150 MHz	446	6.25 kHz	1.0 kHz
11.150 MHz	223	12.5 kHz	
10.240 MHz	512	5.0 kHz	
12.000 MHz	600	5.0 kHz	

Figure 6. Reference Frequencies for Cordless Phone Applications of Various Countries



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output is forced to near mid supply.
Note: The $TxPD_{out}$ and $RxPD_{out}$ generate error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor.

Figure 7. Phase Detector/Lock Detector Output Waveforms

MCU PROGRAMMING SCHEME

The MCU programming scheme is defined in two formats controlled by the ENB input. If the enable signal is high during the serial data transfer, control register/reference frequency programming is selected. If the ENB is low, programming of the transmit and receive counters is selected. During programming of the transmit and receive counters, both AD_{in} and D_{in} pins can input the data to the transmit and receive counters. Both counters' data is clocked into the PLL internal shift register at the leading edge of the CLK signal. It is not necessary to reprogram the reference frequency counter/control register when using the enable signal to program the transmit/receive channels.

In programming the control register/reference frequency scheme, the most significant bit (MSB) of the programming word identifies whether the input data is the control word or the reference frequency data word. If the MSB is 1, the input data is the control word (Figure 8). Also see Figure NO TAG and Table 1 for control register and bit function. If the MSB is 0, the input data is the reference frequency (Figure 9).

The reference frequency data word is a 32-bit word containing the 12-bit reference frequency data, the 14-bit auxiliary reference frequency counter information, the reference frequency selection plus, the auxiliary reference frequency counter enable bit (Figure 9).

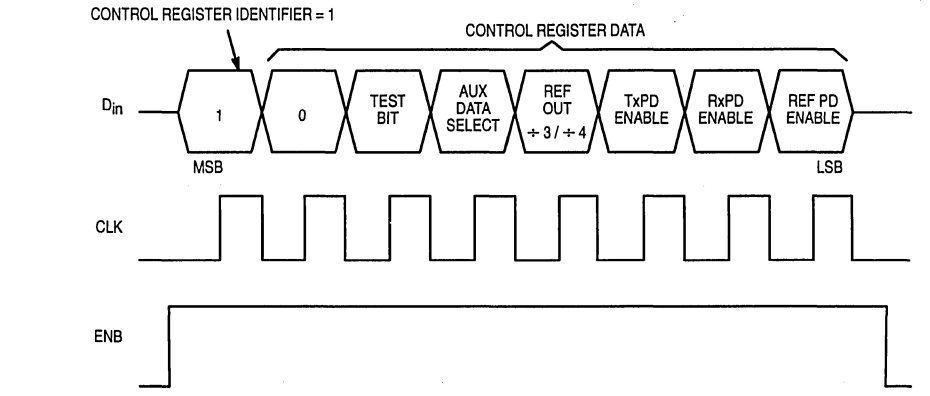
If the AUX REF ENB bit is high, the 14-bit auxiliary reference frequency counter provides an additional phase reference frequency output for the loops. If AUX REF ENB bit is low, the auxiliary reference frequency counter is forced into power-down mode for current saving. (Other power down modes are also provided through the control register per Table 2 and Figure 8.) At the falling edge of the ENB signal, the data is stored in the registers.

There are two interfacing schemes for the universal channel mode: the three-pin and the four-pin interfacing schemes. The three-pin interfacing scheme is suited for use with the MCU SPI (serial peripheral interface) (Figure 10), while the four-pin interfacing scheme is commonly used for general I/O port connection (Figure 11).

For the three-pin interfacing scheme, the auxiliary data select bit is set to 0. All 32 bits of data, which define both the 16-bit transmit counter and the 16-bit receive counter, latch into the PLL internal register through the data in pins at the leading edge of CLK. See Figures 12 and 13.

For the four-pin interfacing scheme, the auxiliary data select bit is set to 1. In this scheme, the 16-bit transmit counter's data enters into the AD_{in} pin at the same time as the 16-bit receive counter's data enters into the D_{in} pin. This simultaneous entry of the transmit and receive counters causes the programming period of the four-pin scheme to be half that of the three-pin scheme (see Figures 14 and 15).

While programming Tx/Rx Channel Counter, the ENB pin must be pulsed to provide falling edge to latch the shifted data after the rising edge of the last clock. Maximum data transfer rate is 500 kbps.



Note: ENB must be high during the serial transfer.

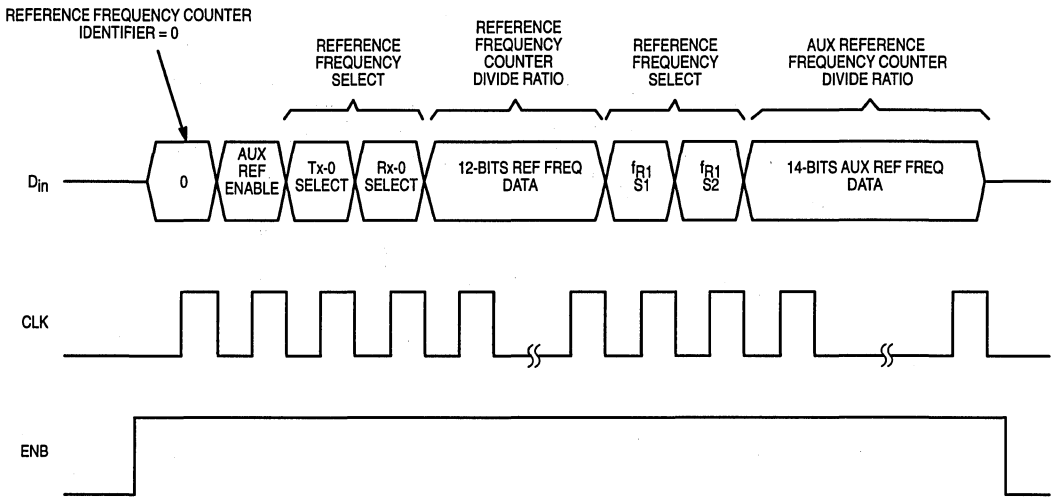
Figure 8. Programming Format of the Control Register

Table 1. Control Register Function Bits Description

Test Bit	Set to 1 for Tx/Rx channel counter test mode Set to 0 for normal application
Aux Data Select	Set to 1 for both AD_{in} and D_{in} pins inputting the transmit 16-bits data and receive 16-bits data respectively. Set to 0 for normal application interfacing with MCU serial peripheral interface. Does not use AD_{in} pin; tie AD_{in} to V_{SS}.
REF_{out} ÷ 3/÷ 4	If set to 1, REF_{out} output frequency is equal to OSC_{out} ÷ 3. If set to 0, REF_{out} output is OSC_{out} ÷ 4.
TxPD Enable	If set to 1, the transmit counter, transmit phase detector, and the associated circuitry is in power-down mode. Tx PS/f_{Tx} is set "High".
RxPD Enable	If set to 1, the receive counter, receive phase detector, and the associated circuitry is in power-down mode. Rx PS/f_{Rx} is set "High".
Ref PD Enable	If set to 1, both 12-bit and 14-bit reference frequency counters are in power-down mode.

Table 2. Control Register Power Down Bits Function

TxPD Enable	RxPD Enable	REF PD Enable	Tx-Channel Counter	Rx-Channel Counter	Reference Frequency Counter
0	0	0	—	—	—
0	0	1	—	—	Power Down
0	1	0	—	Power Down	—
0	1	1	—	Power Down	Power Down
1	0	0	Power Down	—	—
1	0	1	Power Down	—	Power Down
1	1	0	Power Down	Power Down	—
1	1	1	Power Down	Power Down	Power Down



Note: ENB must be high during the serial transfer.

Figure 9. Programming Format of the Auxiliary/Reference Frequency Counters

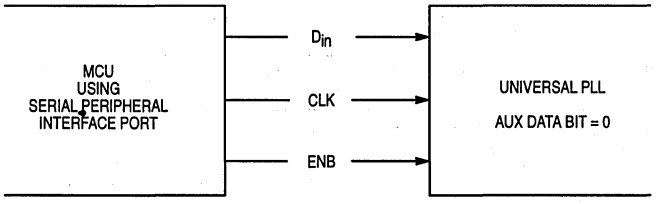


Figure 10. MCU Interface Using SPI

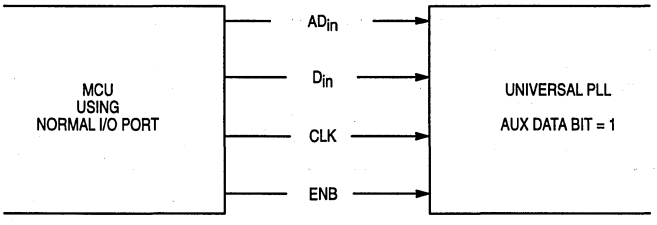
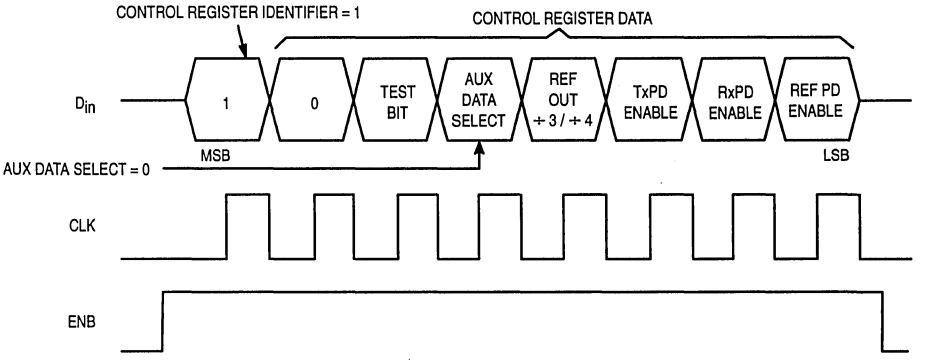
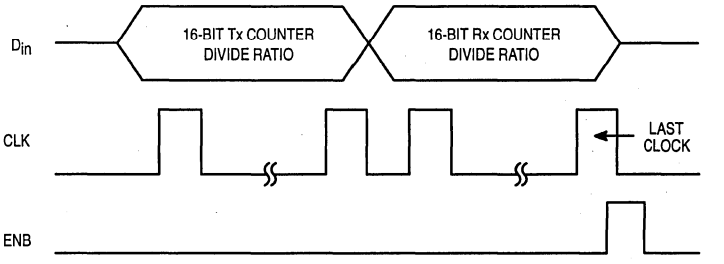


Figure 11. MCU Interface Using Normal I/O Ports with Both D_{in} and AD_{in} for Faster Programming Time



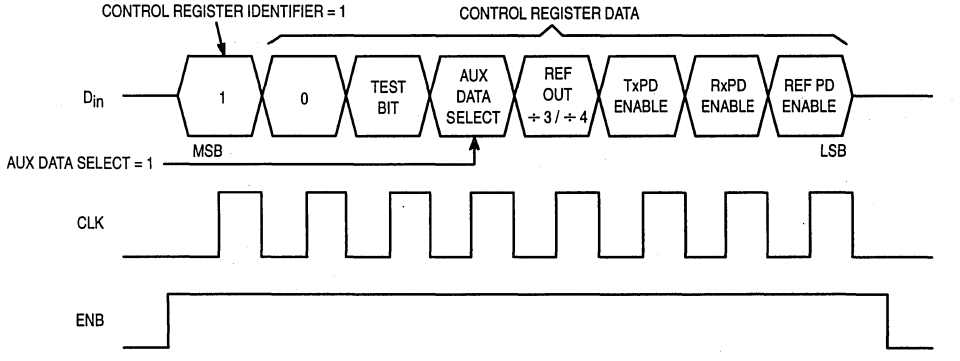
Note: ENB must be high during the serial transfer.

Figure 12. Programming Format for Control Register (3-Pin Interfacing Scheme)



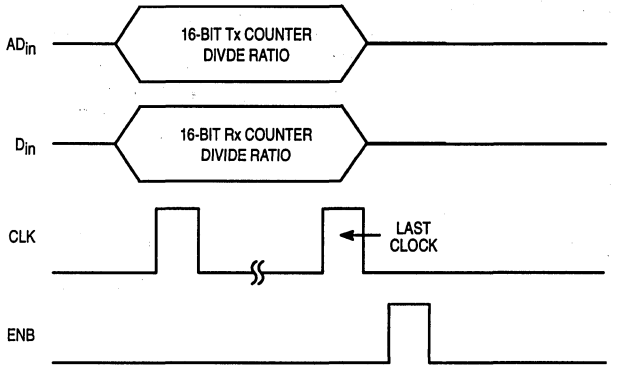
Note: ENB must be low during the serial transfer.

Figure 13. Programming Format for Transmit and Receive Counters (3-Pin Interfacing Scheme)



Note: ENB must be high during the serial transfer.

Figure 14. Programming Format for Control Register (4-Pin Interfacing Scheme)



Note: ENB must be low during the serial transfer.

Figure 15. Programming Format for Transmit and Receive Counters (4-Pin Interfacing Scheme)

Table 3. Global CT–1 Reference Frequency Setting vs Channel Frequencies

Country	Channels Frequency	f_{R1}	f_{R2}
U.S.A.	46/49 MHz (10, 15, 25 Channels)	5.0 kHz	—
France	26/41 MHz	6.25 kHz/12.5 kHz	—
Spain	31/41 MHz	5.0 kHz	—
Australia	30/39 MHz	5.0 kHz	—
U.K.	1.7/47 MHz	6.25 kHz	1.0 kHz
New Zealand	1.7/34/40 MHz	6.25 kHz	1.0 kHz

REFERENCE FREQUENCY SELECTION AND PROGRAMMING

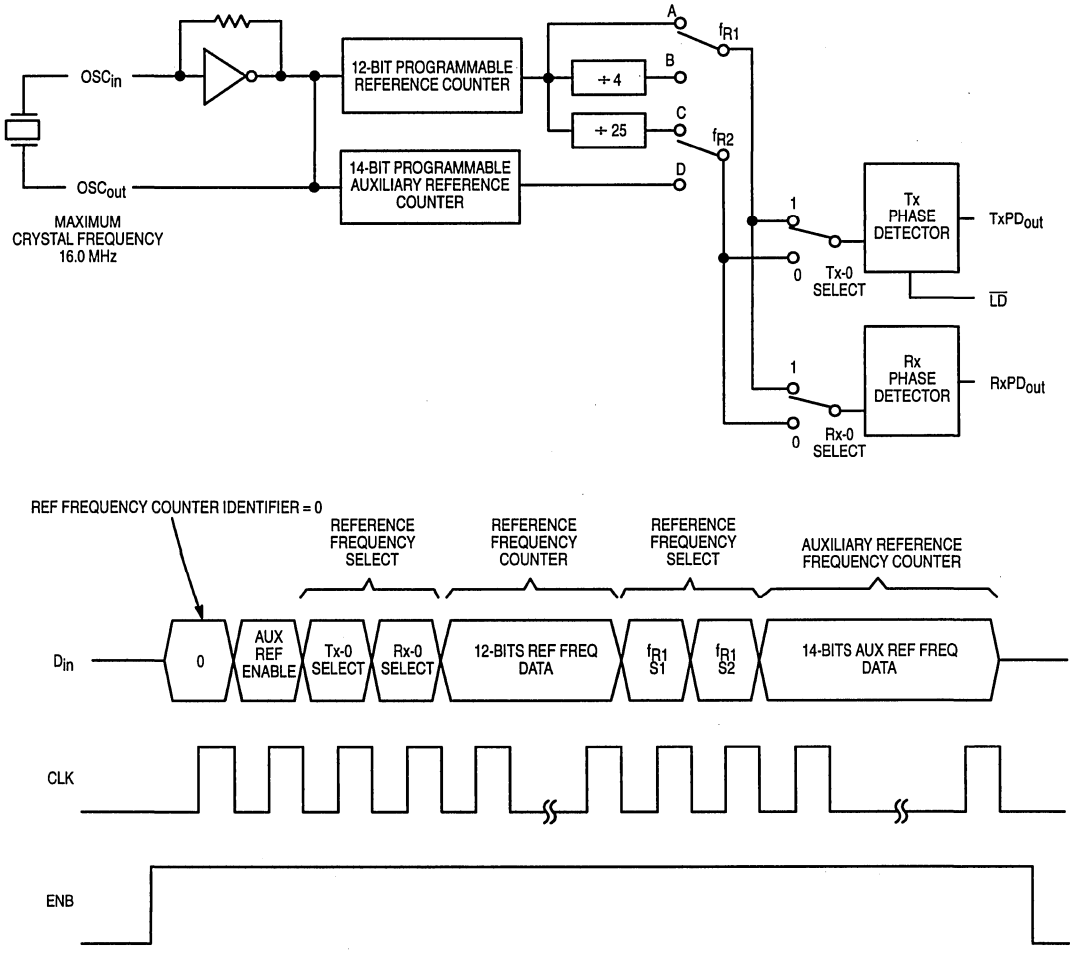
Figure 16 shows the bit function of the reference frequency programming word. The user can either select the "fixed" reference frequency for all channels accordingly or provide a specific reference frequency for a particular channel by using two reference frequency counters (e.g., for an application in France, the base set transmit channel common fixed reference frequency is 6.25 kHz or 12.5 kHz). (See Table 3 and Figure 6 for reference frequencies for various countries.) However, transmit channels 6, 8, and 14 can be set to 25 kHz, and channel 8 reference frequency can be set to 50 kHz. But this reference frequency may not be applied to the receiving side; therefore, the receiving side reference frequency must be generated by another reference frequency counter. The higher the reference frequency, the better the phase noise performance and faster the lock time, but the PLL consumes more current if both reference frequency counters are in operation.

In general, the 12-bit reference frequency counter plus the ÷ 4 and ÷ 25 module can offer all the reference frequencies for global CT–1 transmit and receive channel requirements. Users can select their own reference frequency by introducing the additional 14-bit auxiliary reference frequency counter.

Again, the 14-bit auxiliary reference frequency counter can be shut down by the auxiliary reference enable bit in the reference counter programming word by setting the bit to 0. At this state, the f_{R2} is automatically connected to point C (the ÷ 25 block output), and f_{R1} can be connected to point A or B by setting the f_{R1}-S1 and f_{R1}-S2 bits in the reference counter program word. The 14-bit auxiliary reference frequency counter data will be in "Don't Care" state.

If the 14-bit auxiliary reference frequency counter is enabled (auxiliary reference enable = 1), then f_{R2} is automatically connected to point D (14-bit counter output), and f_{R1} can be selected to connect to point A, B, or C, depending on the bit setting of f_{R1}-S1 and f_{R1}-S2.

Table 4 and Figure 16 describe the functions of the auxiliary reference enable bit and the f_{R1}-S1 and f_{R1}-S2 bits selection.



Note: ENB must be high during the serial transfer.

Figure 16. Reference Frequency Counter/Selection Programming Mode

Table 4. Bit Function and the Reference Frequency Selection Bit Setting of the Reference Frequency Counter Programming Word

AUX REF Enable	Auxiliary Reference Frequency Counter Mode	Module Select	f_{R1} S1	f_{R1} S2	f_{R1} Routing
0	14-Bit Auxiliary Reference Frequency Counter Disable	$f_{R2} \rightarrow C$	0 0 1 1	0 1 0 1	N/A $f_{R1} \rightarrow A$ $f_{R1} \rightarrow B$ N/A
1	14-Bit Auxiliary Reference Frequency Counter Enable	$f_{R2} \rightarrow D$	0 0 1 1	0 1 0 1	N/A $f_{R1} \rightarrow A$ $f_{R1} \rightarrow B$ $f_{R1} \rightarrow C$

N/A = Not Applicable

POWER SAVING OPERATION

This PLL has a programmable power-saving scheme. The transmit and receive counters and the reference frequency counter can be powered down individually by setting the TxPD enable, RxPD enable, and Ref PD enable bits of the control register. The functions of the power down control bits are explained in Table 2 and the programming format is in Figure 8.

The output pins TxPS/f_{Tx} and RxPS/f_{Rx} output the status of the internal power saving setting. If the bit TxPD enable is set "high" (transmit counter is set to power-down mode), then the TxPS/f_{Tx} pin will also output a "high" state. This TxPS/f_{Tx} output can control an external power switch to switch off the transmitter, as shown in Figure 17. This scheme can be applied to the RxPS/f_{Rx} output to control the receiver power saving operation as required.

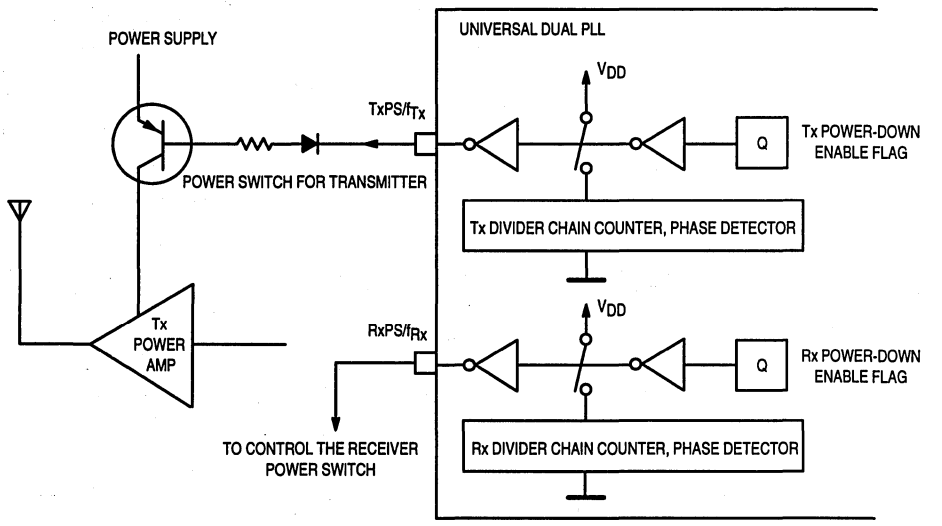


Figure 17. TxPS/f_{Tx} and RxPS/f_{Rx} Outputs to Control Power Switches of the Transmitter and the Receiver

TX/RX CHANNEL COUNTER TEST

In normal applications, the TxPS/f_{Tx} and the RxPS/f_{Rx} output pins indicate the power saving mode status. However, the user can examine the Tx and Rx channel counter outputs by setting the Test bit in the control register to 1. The final value of the transmit-channel counter and the receive-channel counter multiplex out to TxPS/f_{Tx} and RxPS/f_{Rx} respectively. The user can verify the divided-down output waveform associated with the RF input level in the PLL circuitry implementation (Figure 18).

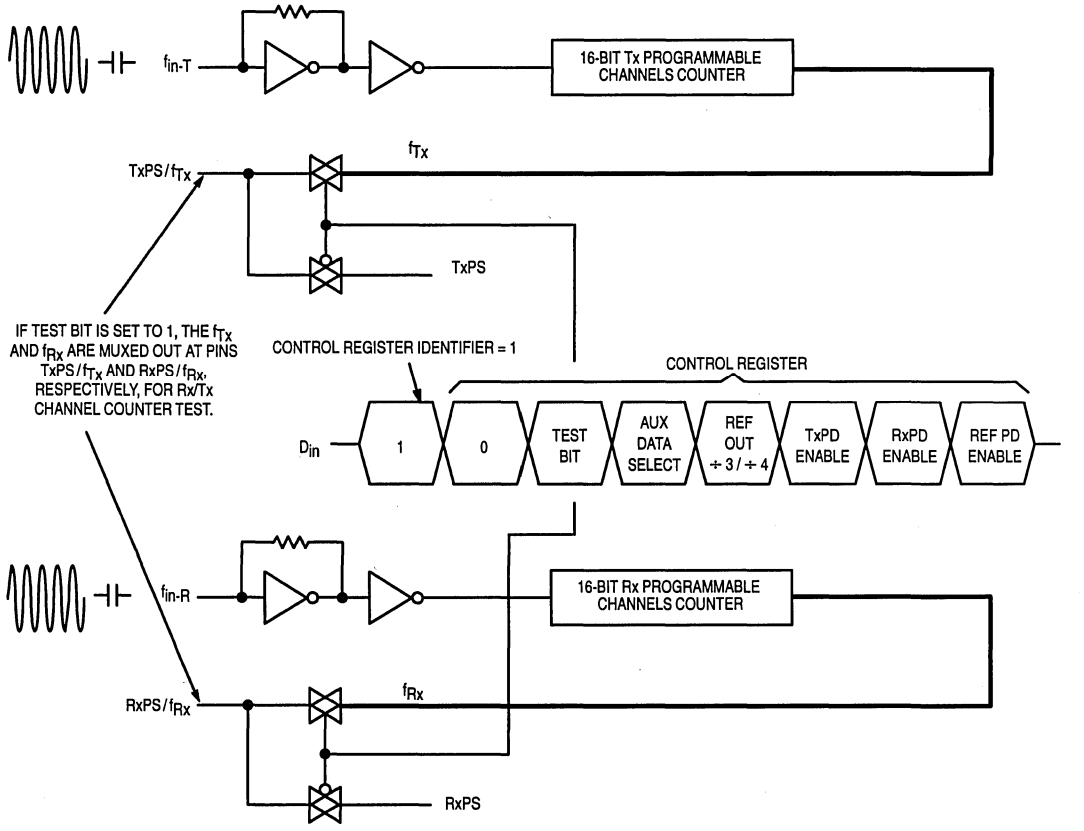


Figure 18. RF Buffer Sensitivity

Table 5. France CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in-R} Input Frequency (MHz) [1st IF=10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	26.4875	4238	30.7875	4926
2	26.4750	4236	30.7750	4924
3	26.4625	4234	30.7625	4922
4	26.4500	4232	30.7500	4920
5	26.4375	4230	30.7375	4918
6	26.4250	4228	30.7250	4916
7	26.4125	4226	30.7125	4914
8	26.4000	4224	30.7000	4912
9	26.3875	4222	30.6875	4910
10	26.3750	4220	30.6750	4908
11	26.3625	4218	30.6625	4906
12	26.3500	4216	30.6500	4904
13	26.3375	4214	30.6375	4902
14	26.3250	4212	30.6250	4900
15	26.3125	4210	30.6125	4898

Table 6. France CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in-R} Input Frequency (MHz) [1st IF=10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	41.4875	6638	37.1875	5950
2	41.4750	6636	37.1750	5948
3	41.4625	6634	37.1625	5946
4	41.4500	6632	37.1500	5944
5	41.4375	6630	37.1375	5942
6	41.4250	6628	37.1250	5940
7	41.4125	6626	37.1125	5938
8	41.4000	6624	37.1000	5936
9	41.3875	6622	37.0875	5934
10	41.3750	6620	37.0750	5932
11	41.3625	6618	37.0625	5930
12	41.3500	6616	37.0500	5928
13	41.3375	6614	37.0375	5926
14	41.3250	6612	37.0250	5924
15	41.3125	6610	37.0125	5922

Table 7. Spain CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in-R} Input Frequency (MHz) [1st IF=10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	31.0250	6205	29.2300	5846
2	31.0500	6210	29.2550	5851
3	31.0750	6215	29.2800	5856
4	31.1000	6220	29.3050	5861
5	31.1250	6225	29.3300	5866
6	31.1500	6230	29.3550	5871
7	31.1750	6235	29.3800	5876
8	31.2000	6240	29.4050	5881
9	31.2500	6250	29.4550	5891
10	31.2750	6255	29.4800	5896
11	31.3000	6260	29.5050	5901
12	31.3250	6265	29.5300	5906

Table 8. Spain CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in-R} Input Frequency (MHz) [1st IF=10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	39.9250	7985	20.3300	4066
2	39.9500	7990	20.3550	4071
3	39.9750	7995	20.3800	4076
4	40.0000	8000	20.4050	4081
5	40.0250	8005	20.4300	4086
6	40.0500	8010	20.4550	4091
7	40.0750	8015	20.4800	4096
8	40.1000	8020	20.5050	4101
9	40.1500	8030	20.5550	4111
10	40.1750	8035	20.5800	4116
11	40.2000	8040	20.6050	4121
12	40.2250	8045	20.6300	4126

Table 9. New Zealand CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value		f_{in-R} Input Frequency (MHz) [1st IF=10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	1.7820	1782		29.7625	4762
2	1.7620	1762		29.7500	4760
3	1.7420	1742	Ref Freq = 1.0 kHz	29.7375	4758
4	1.7220	1722		29.7250	4756
5	1.7020	1702		29.7125	4754
6	34.3500	5496		29.7000	4752
7	34.3625	5498		29.6875	4750
8	34.3750	5500	Ref Freq = 6.25 kHz	29.6750	4748
9	34.3875	5502		29.6625	4746
10	34.4000	5504		29.6500	4744

Table 10. New Zealand CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in-R} Input Frequency (MHz)	Rx Counter Value
1	40.4625	6474	2.2370	2237
2	40.4500	6472	2.2170	2217
3	40.4375	6470	2.1970	2197
4	40.4250	6468	2.1770	2177
5	40.4125	6466	2.1570	2157
6	40.4000	6464	23.6500	3784
7	40.3875	6462	23.6625	3786
8	40.3750	6460	23.6750	3788
9	40.3625	6458	23.6875	3790
10	40.3500	6456	23.7000	3792

Ref Freq = 455 kHz

Ref Freq = 1.0 kHz

Ref Freq = 10.7 kHz

Ref Freq = 6.25 kHz

Table 11. Australia CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in-R} Input Frequency (MHz) [1st IF=10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	30.0750	6015	29.0800	5816
2	30.1250	6025	29.1300	5826
3	30.1750	6035	29.1800	5836
4	30.2250	6045	29.2300	5846
5	30.2750	6055	29.2800	5856
6	30.1000	6020	29.1050	5821
7	30.1500	6030	29.1550	5831
8	30.2000	6040	29.2050	5841
9	30.2500	6050	29.2550	5851
10	30.3000	6060	29.3050	5861

Table 12. Australia CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in-R} Input Frequency (MHz) [1st IF=10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	39.7750	7955	19.3800	3876
2	39.8250	7965	19.4300	3886
3	39.8750	7975	19.4800	3896
4	39.9250	7985	19.5300	3906
5	39.9750	7995	19.5800	3916
6	39.8000	7960	19.4050	3881
7	39.8500	7970	19.4550	3891
8	39.9000	7980	19.5050	3901
9	39.9500	7990	19.5550	3911
10	40.0000	8000	19.6050	3921

Table 13. U.K. CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 1.00 kHz)	f_{in-R} Input Frequency (MHz) [1st IF=10.7 MHz]	Rx Counter Value (Ref. Freq. = 6.25 kHz)
1	1.6420	1642	36.75625	5881
2	1.6620	1662	36.76875	5883
3	1.6820	1682	36.78125	5885
4	1.7020	1702	36.79375	5887
5	1.7220	1722	36.80625	5889
6	1.7420	1742	36.81875	5891
7	1.7620	1762	36.83125	5893
8	1.7820	1782	36.84375	5895

Table 14. U.K. CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 6.25 kHz)	f_{in-R} Input Frequency (MHz) [1st IF=455 kHz]	Rx Counter Value (Ref. Freq. = 1.00 kHz)
1	47.45625	7593	2.097	2097
2	47.46875	7595	2.117	2117
3	47.48125	7597	2.137	2137
4	47.49375	7599	2.157	2157
5	47.50625	7601	2.177	2177
6	47.51875	7603	2.197	2197
7	47.53125	7605	2.217	2217
8	47.54375	7607	2.237	2237

Table 15. U.S.A. CT–1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in-R} Input Frequency (MHz) [1st IF=10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	46.610	9322	38.975	7795
2	46.630	9326	38.150	7830
3	46.670	9334	38.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855

Table 16. U.S.A. CT–1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in-R} Input Frequency (MHz) [1st IF=10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255

Table 17. Korea CT-1 Base Set Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in-R} Input Frequency (MHz) [1st IF=10.695 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	46.610	9322	38.975	7795
2	46.630	9326	38.150	7830
3	46.670	9334	38.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855
11	46.510	9302	39.000	7800
12	46.530	9306	39.015	7803
13	46.550	9310	39.030	7806
14	46.570	9314	39.045	7809
15	46.590	9318	39.060	7812

Table 18. Korea CT-1 Handset Frequency

Channel Number	Tx Channel Frequency (MHz)	Tx Counter Value (Ref. Freq. = 5.00 kHz)	f_{in-R} Input Frequency (MHz) [1st IF=10.7 MHz]	Rx Counter Value (Ref. Freq. = 5.00 kHz)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255
11	49.695	9939	35.815	7163
12	49.710	9942	35.835	7167
13	49.725	9945	35.855	7171
14	49.740	9948	35.875	7175
15	49.755	9951	35.895	7179

MC145168
MC145169

Advance Information

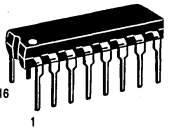
Dual PLLs for 46/49 MHz Cordless Telephones

CMOS

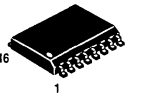
These devices are dual phase-locked loop frequency synthesizers intended for use primarily in 46/49 MHz cordless phones with up to 15 channels. These parts contain two mask-programmable counter ROMs for receive and transmit loops with two independent phase detect circuits. A common reference oscillator and reference divider are shared by the receive and transmit circuits.

Other features include a lock detect circuit for the transmit loop, illegal code default, a buffered oscillator output for mixing purposes in the system, and a 5.0-kHz tone output.

- Maximum Operating Frequency: 60 MHz @ V_{in}=200 mVp-p
- Operating Temperature Range: −40 to +75°C
- Operating Voltage Range: 2.5 to 5.5 V
- On-Chip Oscillator Circuit Supports External Crystal
- Operating Power Consumption: 3.0 mA @ 3.0 V
- Lock Detect Signal
- Standby Mode for Power Savings: 1.5 mA @ 3.0 V
- Two Versions:
  - MC145168 — Up to 15-Channel ROM with 4-Bit Binary Code Input for Channel Pair Selection
  - MC145169 — Up to 15-Channel ROM with Serial Interface for Channel Pair Selection
- Custom 20-Channel ROM Versions of the MC145169 are Possible; Consult Factory



P SUFFIX
PLASTIC DIP
CASE 648

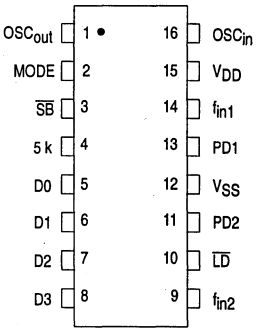


DW SUFFIX
SOG
CASE 751G

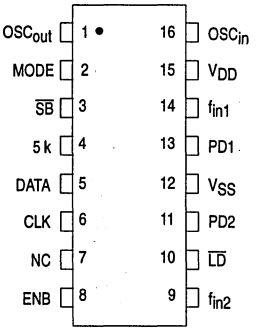
ORDERING INFORMATION

MC145168P	Plastic DIP
MC145168DW	SOG Package
MC145169P	Plastic DIP
MC145169DW	SOG Package

MC145168



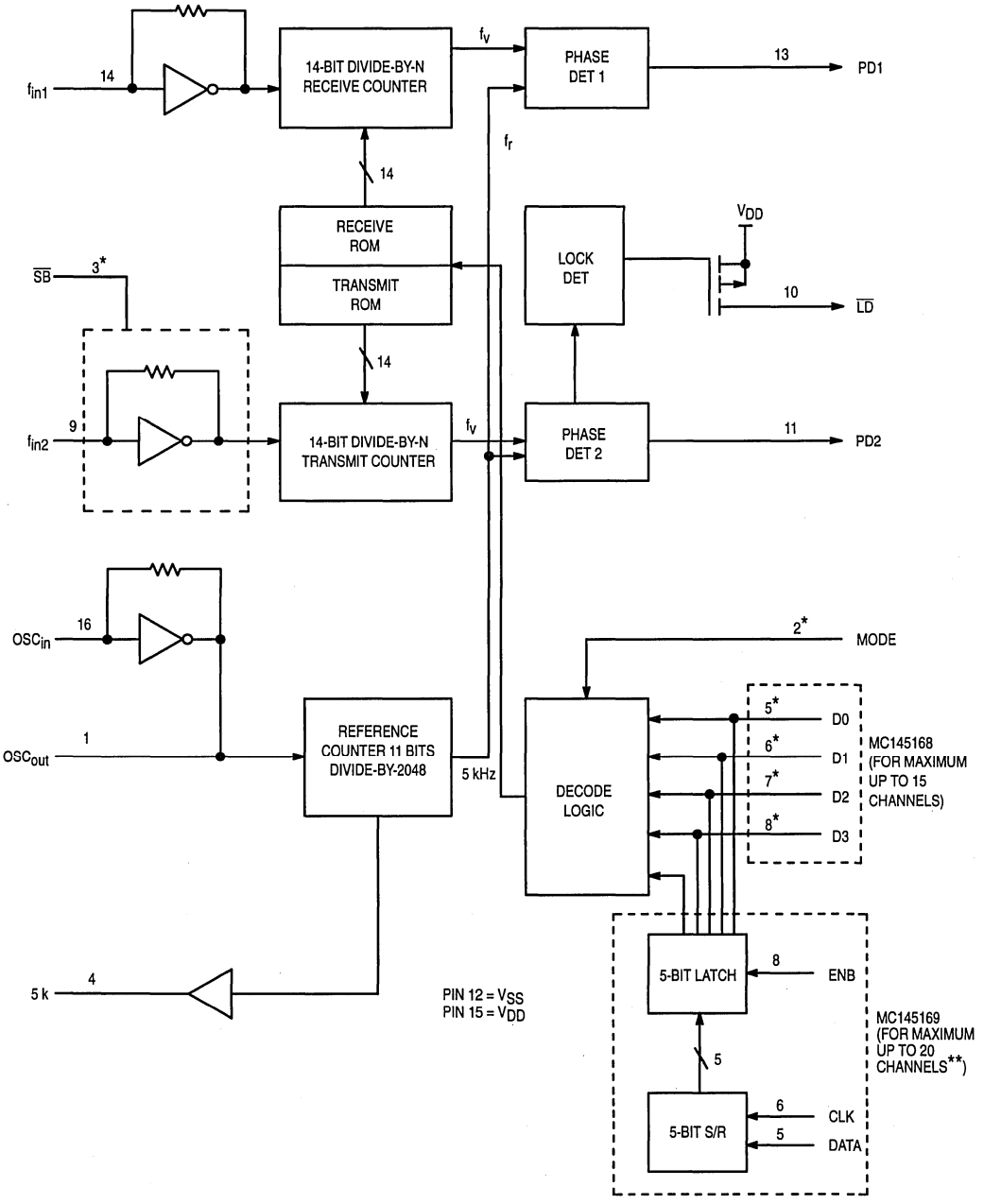
MC145169



NC = NO CONNECTION

This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM



*On chip pull-down.

**The standard MC145169 is 15 channels; see Tables 1 and 2. Custom versions up to 20 channels are possible.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Rating	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +6.0	V
V_{in}	Input Voltage, All Inputs	−0.5 to V_{DD}+0.5	V
I_{in}, I_{out}	DC Current Drain Per Pin	10	mA
I_{DD}, I_{SS}	DC Current Drain V_{DD} or V_{SS} Pins	30	mA
T_{stg}	Storage Temperature Range	−65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, T_A = 25°C)

Symbol	Characteristic		V_{DD}	Guaranteed Limit		Unit
				Min	Max	
V_{DD}	Power Supply Voltage Range		—	2.5	5.5	V
V_{OL}	Output Voltage (I_{out} = 0)	0 Level	2.5 5.5	— —	0.05 0.05	V
V_{OH}	(V_{in} = V_{DD} or 0)	1 Level	2.5 5.5	2.45 5.45	— —	
V_{IL}	Input Voltage (V_{out} = 0.5 V or V_{DD} − 0.5 V)	0 Level	2.5 5.5	— —	0.75 1.65	V
V_{IH}		1 Level	2.5 5.5	1.75 3.85	— —	
I_{OH}	Output Current (V_{out} = 2.2 V) (V_{out} = 5.0 V)	Source	2.5 5.5	−0.18 −0.55	— —	mA
I_{OL}	(V_{out} = 0.3 V) (V_{out} = 0.5 V)	Sink	2.5 5.5	0.18 0.55	— —	
I_{IL}	Input Current (V_{in} = 0)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	−30 −66	µA
		DATA, $\overline{SB}$, Mode	2.5 5.5	— —	−0.05 −0.11	
I_{IH}	(V_{in} = V_{DD} − 0.5)	OSC_{in}, f_{in1}, f_{in2}	2.5 5.5	— —	30 66	µA
		DATA, $\overline{SB}$, Mode	2.5 5.5	— —	50 121	
C_{in}	Input Capacitance		—	—	8.0	pF
C_{out}	Output Capacitance		—	—	8.0	pF
I_{DD}	Standby Current, $\overline{SB}$ = V_{SS} or Open		2.5 5.5	— —	1.4 3.6	mA
I_{dd}	Operating Current (200 mVp-p input at f_{in1}, f_{in2}, $\overline{SB}$ = V_{DD})		2.5 5.5	— —	2.8 6.2	mA
I_{OZ}	Three-State Leakage Current (V_{out} = 0 V or 5.5 V)		5.5	—	±1.0	µA

SWITCHING CHARACTERISTICS (T_A = 25°C, C_L = 50 pF)

Symbol	Characteristic	Figure #	V_{DD}	Guaranteed Limit		Unit
				Min	Max	
t_{TLH}	Output Rise Time	1, 5	3.0 5.0	— —	200 100	ns
t_{THL}	Output Fall Time	1, 5	3.0 5.0	— —	200 100	ns
t_r, t_f	Input Rise and Fall Time, OSC_{in}	2	3.0 5.0	— —	5.0 4.0	µs
f_{max}	Input Frequency OSC_{in} Input=Sine Wave 200 mVp-p f_{in1} f_{in2}		3.0–5.0 3.0–5.0 3.0–5.0	— — —	12 60 60	MHz
t_{su}	Setup Time (MC145169) DATA to CLK	3	3.0 5.0	100 50	— —	ns
	ENB to CLK	3	3.0 5.0	200 100	— —	
t_h	Hold Time (MC145169), CLK to DATA	3	3.0 5.0	80 40	— —	ns
t_{rec}	Recovery Time (MC145169), ENB to CLK	3	3.0 5.0	80 40	— —	ns
t_w	Input Pulse Width (MC145169), CLK and ENB	4	3.0 5.0	80 60	— —	ns

SWITCHING WAVEFORMS

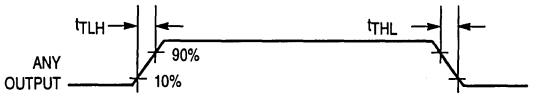


Figure 1.

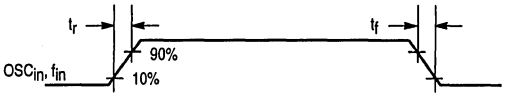


Figure 2.

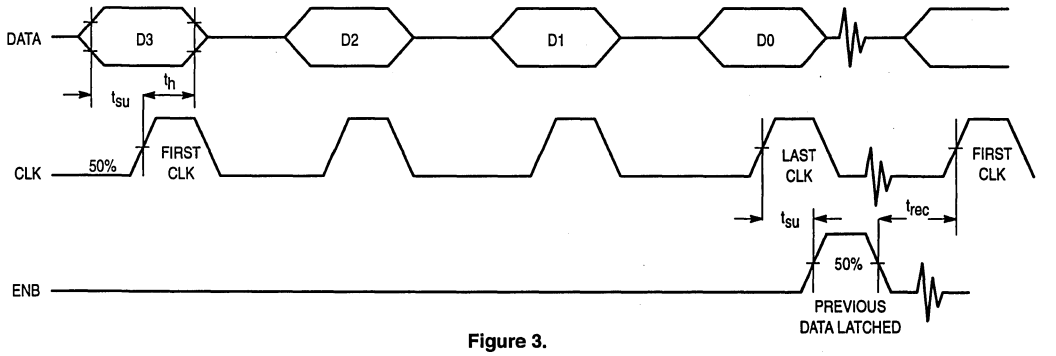


Figure 3.

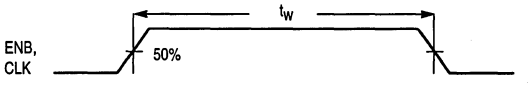


Figure 4.

PIN DESCRIPTIONS

INPUTS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 16, 1)

These pins form a reference oscillator when connected to an external parallel-resonant crystal. For a 46/49 MHz cordless phone application, a 10.24 MHz crystal is needed. OSC_{in} may also serve as input for an externally generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) dc coupling may also be used. In the external reference mode, no connection is required for OSC_{out}.

MODE
Mode Select (Pin 2)

Mode is for determining whether the part is to be used in the base or handset of a cordless phone. Internally, this pin is used in the decoding logic for selecting the ROM address. When high, the device is set in the base mode, and when low, it is set in the handset mode. This input has an internal pull-down device.

$\overline{SB}$
Standby (Pin 3)

The standby pin is used to save power when not transmitting. When high, both the transmit and receive loops are in operation. When low, the transmit loop is disabled, thereby reducing power consumption. This input has an internal pull-down device.

D0–D3 (MC145168 ONLY)
Data Inputs (Pins 5, 6, 7, 8)

These inputs provide the 4-bit binary code for selecting the one of 15 channels for the transmit and receive loops. When address data other than 1–15 are input, the decoding logic defaults to channel 1. The frequency assignments, with reference to Mode and D0–D3, are shown in Tables 1 and 2. These inputs have internal pull-down devices.

f_{in1}, f_{in2}
Frequency Inputs (Pins 14, 9)

f_{in1} and f_{in2} are inputs to the divide-by-N receive and transmit counters, respectively. These signals are typically derived from the loop VCO and are ac coupled. The minimum input level is 200 mVp-p. For larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

DATA, CLK (MC145169 ONLY)
Data, Clock (Pins 5, 6)

These pins provide the binary input by using serial channel programming. A logic high represents a 1. Each low-to-high transition of the clock shifts one bit of data into the on-chip shift register. Data is entered MSB first (see Figure 3).

ENB (MC145169 ONLY)
Enable (Pin 8)

The enable pin controls the data transfer from the shift register to the latch. A positive pulse transfers the data. This pin should normally be held low to avoid loading erroneous data into the latch.

OUTPUTS

5 k
5-kHz Tone Signal (Pin 4)

This is a 5 kHz tone signal derived from the reference oscillator. This pin is a push-pull output.

$\overline{LD}$
Lock Detect Signal (Pin 10)

The lock detect signal is associated with the transmit loop. The lock output goes high to indicate an out-of-lock condition. This is a P-channel open-drain output.

PD1/PD2
Transmit/Receive Phase Detector Outputs (Pins 13, 11)

These are three-state outputs of the transmit and receive phase detectors for use as loop error signals.

Frequency $f_V > f_r$ or f_V leading: Negative pulses
Frequency $f_V < f_r$ or f_V lagging: Positive pulses
Frequency $f_V = f_r$ and phase coincidence: High-impedance state

NOTE: f_V is the output of the N counter. f_r is the output of the reference counter.

POWER SUPPLY

V_{DD} (Pin 15)

This pin is the positive supply potential and may range from +2.5 to +5.5 V with respect to V_{SS}.

V_{SS} (Pin 12)

This pin is the negative supply potential and is usually ground.

Table 1. Handset Frequencies of Each Corresponding Channel in a 46/49 MHz Cordless Phone for the Korean Market

Channels					RX Freq.	Receive (Note 3)		TX Freq.	Transmit		
D3	D2	D1	D0	CH#	(MHz)	f_{in1} (MHz)	÷N	(MHz)	f_{in2} (MHz)	÷N	Mode
0	0	0	1	1	46.610	35.915	7183	49.670	49.670	9934	0
0	0	1	0	2	46.630	35.935	7187	49.845	49.845	9969	0
0	0	1	1	3	46.670	35.975	7195	49.860	49.860	9972	0
0	1	0	0	4	46.710	36.015	7203	49.770	49.770	9954	0
0	1	0	1	5	46.730	36.035	7207	49.875	49.875	9975	0
0	1	1	0	6	46.770	36.075	7215	49.830	49.830	9966	0
0	1	1	1	7	46.830	36.135	7227	49.890	49.890	9978	0
1	0	0	0	8	46.870	36.175	7235	49.930	49.930	9986	0
1	0	0	1	9	46.930	36.235	7247	49.990	49.990	9998	0
1	0	1	0	10	46.970	36.275	7255	49.970	49.970	9994	0
1	0	1	1	11	46.510	35.815	7163	49.695	49.695	9939	0
1	1	0	0	12	46.530	35.835	7167	49.710	49.710	9942	0
1	1	0	1	13	46.550	35.855	7171	49.725	49.725	9945	0
1	1	1	0	14	46.570	35.875	7175	49.740	49.740	9948	0
1	1	1	1	15	46.590	35.895	7179	49.755	49.755	9951	0

NOTES:
1. 0 = logic low, 1 = logic high.
2. Power-up and illegal inputs are defaulted to channel 1 in the MC145169. Illegal inputs are defaulted to channel 1 in MC145168.
3. First IF frequency of receive is 10.695 MHz; Second IF is 455 kHz.
4. $\div N = \frac{f_{in}}{f_{ref}}$ where f_{in} is the VCO frequency and f_{ref} is the reference frequency (5.0 kHz).

Table 2. Base Frequencies of Each Corresponding Channel in a 46/49 MHz Cordless Phone for the Korean Market

Channels					RX Freq.	Receive (Note 3)		TX Freq.	Transmit		
D3	D2	D1	D0	CH#	(MHz)	f_{in1} (MHz)	÷N	(MHz)	f_{in2} (MHz)	÷N	Mode
0	0	0	1	1	49.670	38.975	7795	46.610	46.610	9322	1
0	0	1	0	2	49.845	39.150	7830	46.630	46.630	9326	1
0	0	1	1	3	49.860	39.165	7833	46.670	46.670	9334	1
0	1	0	0	4	49.770	39.075	7815	46.710	46.710	9342	1
0	1	0	1	5	49.875	39.180	7836	46.730	46.730	9346	1
0	1	1	0	6	49.830	39.135	7827	46.770	46.770	9354	1
0	1	1	1	7	49.890	39.195	7839	46.830	46.830	9366	1
1	0	0	0	8	49.930	39.235	7847	46.870	46.870	9374	1
1	0	0	1	9	49.990	39.295	7859	46.930	46.930	9386	1
1	0	1	0	10	49.970	39.275	7855	46.970	46.970	9394	1
1	0	1	1	11	49.695	39.000	7800	46.510	46.510	9302	1
1	1	0	0	12	49.710	39.015	7803	46.530	46.530	9306	1
1	1	0	1	13	49.725	39.030	7806	46.550	46.550	9310	1
1	1	1	0	14	49.740	39.045	7809	46.570	46.570	9314	1
1	1	1	1	15	49.755	39.060	7812	46.590	46.590	9318	1

NOTES:
1. 0 = logic low, 1 = logic high.
2. Power-up and illegal inputs are defaulted to channel 1 in the MC145169. Illegal inputs are defaulted to channel 1 in MC145168.
3. First IF frequency of receive is 10.695 MHz; Second IF is 455 kHz.
4. $\div N = \frac{f_{in}}{f_{ref}}$ where f_{in} is the VCO frequency and f_{ref} is the reference frequency (5.0 kHz).

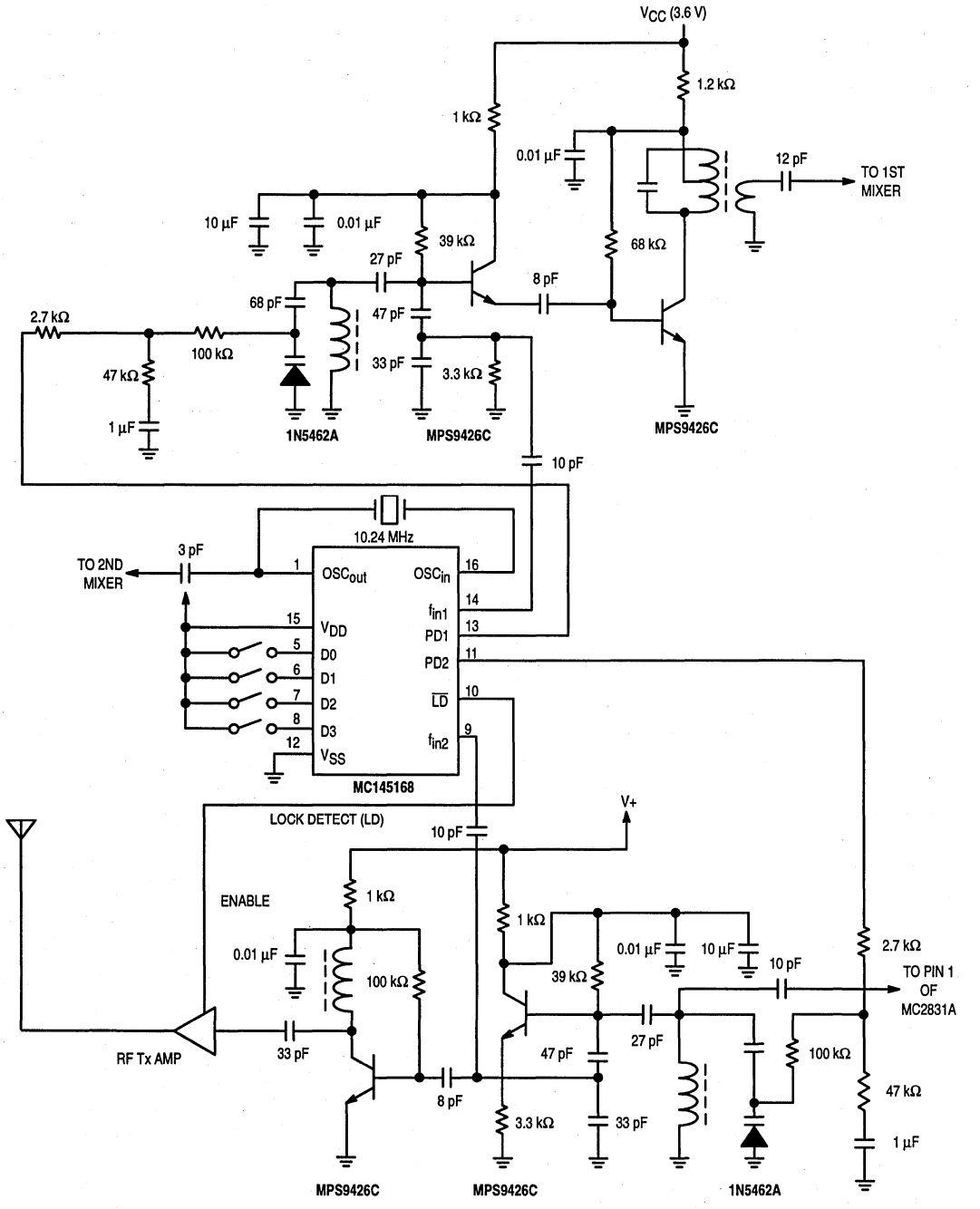


Figure 5. MC145168 Circuit Example

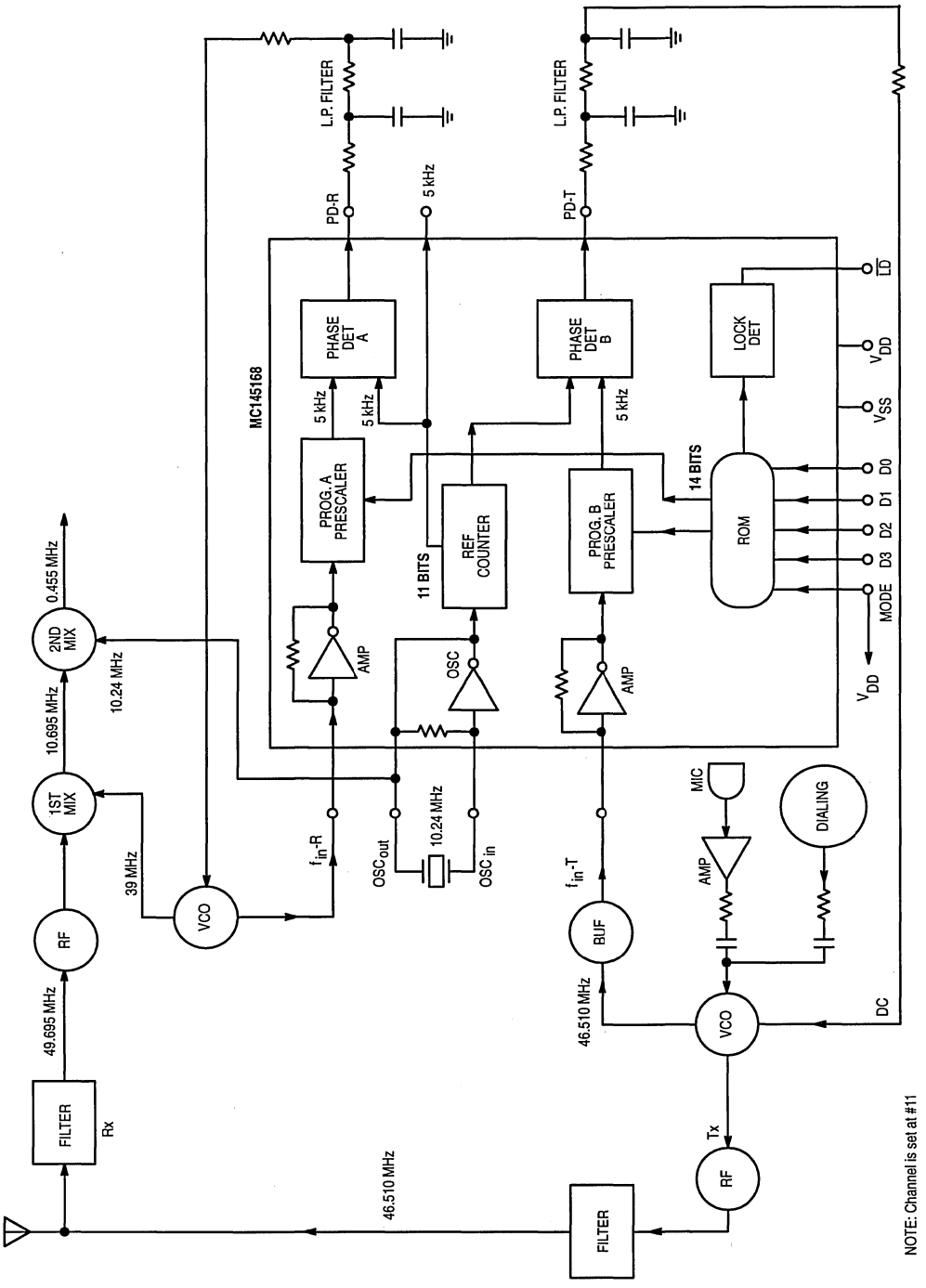


Figure 6. DPLL Application in 46/49 MHz Cordless Phone 15-Channel Base

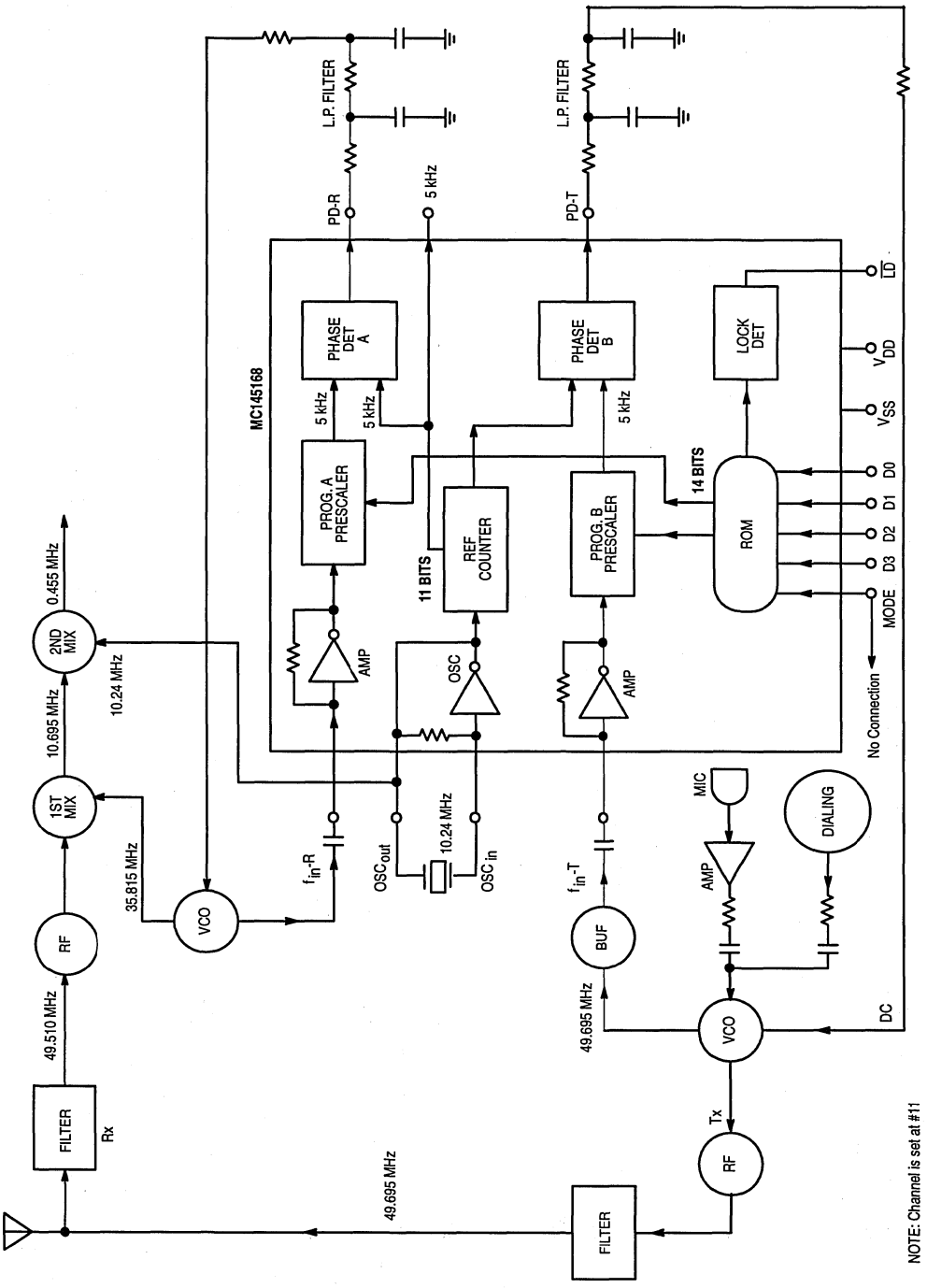


Figure 7. DPLL Application in 46/49 MHz Cordless Phone 15-Channel Handset

MC145170

Advance Information

PLL Frequency Synthesizer with Serial Interface

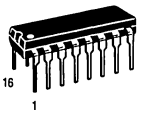
CMOS

The MC145170 is a single-chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL the easiest to program in the industry. Either a bit- or byte-oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2-byte serial transfer to the 16-bit N register.

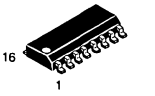
The device features fully programmable R and N counters, an amplifier at the f_{in} pin, on-chip support of an external crystal, a programmable reference output, and both single- and double-ended phase detectors with linear transfer functions. A new feature on the MC145170 is the C register (configuration register). The C register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam-load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.5 to 6.0 V
- Maximum Operating Frequency:
  160 MHz @ V_{in} = 500 mVp-p, 4.5-V Minimum Supply
  100 MHz @ V_{in} = 500 mVp-p, 3.0-V Minimum Supply
- Operating Temperature Range: – 40 to 85°C
- R Counter Division Range: 5 to 32,767 Plus Direct Access to Phase Detector Input
- N Counter Division Range: 40 to 65,535
- Direct Interface to Motorola SPI and National MICROWIRE™ Serial Data Ports
- 180 MHz Versions Available (Part Numbers MC145170P1 and MC145170D1), Consult Factory*
- Chip Complexity: 4800 FETs or 1200 Equivalent Gates
- See Application Note AN1207



P SUFFIX
PLASTIC DIP
CASE 648

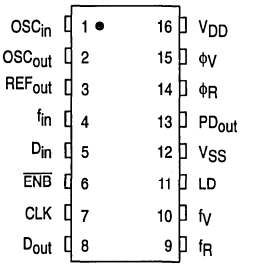


D SUFFIX
SOG
CASE 751B

ORDERING INFORMATION

MC145170P	Plastic DIP
MC145170D	SOG Package

PIN ASSIGNMENT



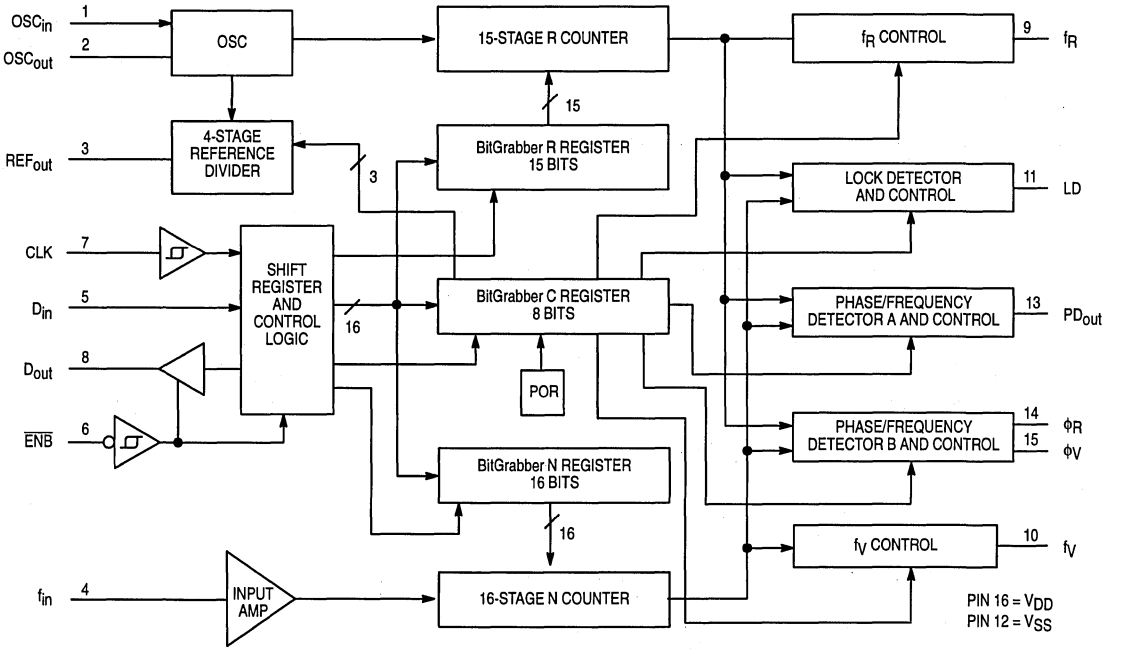
*The functional voltage range for the suffix-1 devices is 2.7 to 5.5 V. 180 MHz operation is with a 4.5 V minimum supply.

BitGrabber is a trademark of Motorola, Inc. MICROWIRE is a trademark of National Semiconductor Corp.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV. 1

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +6.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD} +0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±20	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS}, $T_A = -40$ to $+85°C$)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	2.5 to 6.0	V
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		2.5 4.5 6.0	0.50 1.35 1.80	V
V_{IH}	Minimum High-Level Input Voltage (D_{in}, CLK, $\overline{ENB}$)		2.5 4.5 6.0	2.00 3.15 4.20	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		2.5 6.0	0.15 0.20	V
V_{OL}	Maximum Low-Level Output Voltage (Any Output)	$I_{out} = 20\ \mu A$	2.5 6.0	0.1 0.1	V
V_{OH}	Minimum High-Level Output Voltage (Any Output)	$I_{out} = -20\ \mu A$	2.5 6.0	2.4 5.9	V
I_{OL}	Minimum Low-Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	$V_{out} = 0.3$ V $V_{out} = 0.4$ V $V_{out} = 0.5$ V	2.5 4.5 6.0	0.12 0.36 0.50	mA
I_{OH}	Minimum High-Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	$V_{out} = 2.2$ V $V_{out} = 4.1$ V $V_{out} = 5.5$ V	2.5 4.5 6.0	−0.12 −0.36 −0.50	mA
I_{OL}	Minimum Low-Level Output Current (D_{out})	$V_{out} = 0.4$ V	4.5	1.6	mA
I_{OH}	Minimum High-Level Output Current (D_{out})	$V_{out} = 4.1$ V	4.5	−1.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, OSC_{in})	$V_{in} = V_{DD}$ or V_{SS}	6.0	±1.0	µA
I_{in}	Maximum Input Current (f_{in})	$V_{in} = V_{DD}$ or V_{SS}	6.0	±120	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	$V_{in} = V_{DD}$ or V_{SS}, Output in High-Impedance State	6.0	±100	nA
	(D_{out})		6.0	±5	µA
I_{DD}	Maximum Quiescent Supply Current	$V_{in} = V_{DD}$ or V_{SS}; Outputs Open; Excluding f_{in} Amp Input Current Component	6.0	100	µA
I_{dd}	Maximum Operating Supply Current	$f_{in} = 160$ MHz @ 500 mVp-p; $OSC_{in} = 10$ MHz @ 1 Vp–p; f_R, f_V, REF_{out} = Inactive and No Connect; OSC_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, ENB, CLK = V_{DD} or V_{SS}	5.0	*	mA

* The nominal value is 7 mA. This is not a guaranteed limit.
Current consumption is reduced at lower frequencies and/or lower supply voltages (i.e., at 100 MHz with a 3-V supply, the device draws about 2.5 mA).

AC INTERFACE CHARACTERISTICS (T_A = – 40 to + 85°C, C_L = 50 pF, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure #	V_{DD} V	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	2.5 4.5 6.0	dc to TBD dc to 4.0 dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to D_{out}	1, 5	2.5 4.5 6.0	TBD 85 85	ns
t_{PLZ}, t_{PHZ}	Maximum Disable Time, D_{out} Active to High Impedance	2, 6	2.5 4.5 6.0	TBD 200 200	ns
t_{PZL}, t_{PZH}	Access Time, D_{out} High Impedance to Active	2, 6	2.5 4.5 6.0	TBD 0 to 100 0 to 100	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, D_{out} CL = 50 pF	1, 5	2.5 4.5 6.0	TBD 50 50	ns
	CL = 200 pF	1, 5	2.5 4.5 6.0	TBD 150 150	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK,		—	10	pF
C_{out}	Maximum Output Capacitance – D_{out}		—	15	pF

TIMING REQUIREMENTS (T_A = – 40 to + 85°C, Input $t_r = t_f$ = 10 ns unless otherwise indicated)

Symbol	Parameter	Figure #	V_{DD} V	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	2.5 4.5 6.0	TBD 40 40	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold, and Recovery Times, $\overline{ENB}$ vs CLK	4	2.5 4.5 6.0	TBD 100 100	ns
$t_{w(H)}$	Minimum Inactive-High Pulse Width, $\overline{ENB}$	4	2.5 4.5 6.0	TBD 300 300	ns
t_w	Minimum Pulse Width, CLK	1	2.5 4.5 6.0	TBD 125 125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	2.5 4.5 6.0	100 100 100	µs

SWITCHING WAVEFORMS

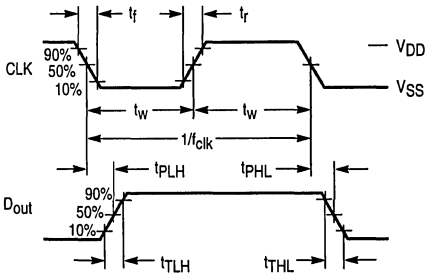


Figure 1.

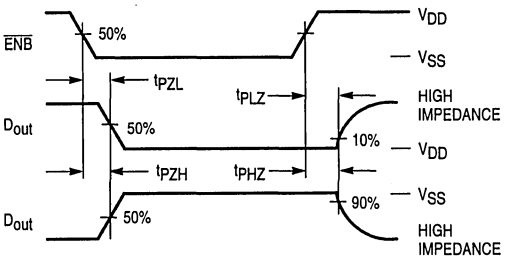


Figure 2.

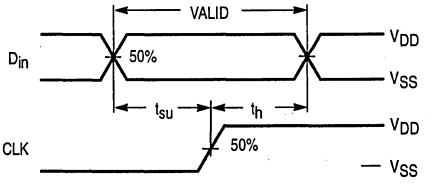


Figure 3.

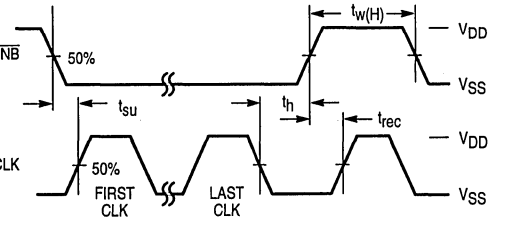
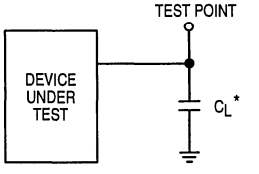
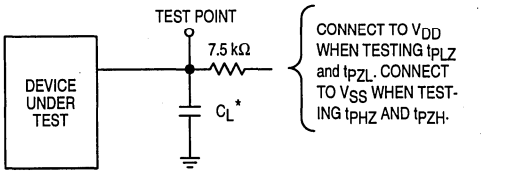


Figure 4.



*Includes all probe and fixture capacitance.

Figure 5. Test Circuit



*Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS ($T_A = -40$ to $+85°C$)

Symbol	Parameter	Test Condition	Fig #	V_{DD} V	Guaranteed Range Min	Guaranteed Range Max	Unit
f	Input Frequency, f_{in}	$V_{in} \geq 500$ mVp–p Sine Wave, N Counter set to divide ratio such that $f_V \leq 2$ MHz	7	2.5 3.0 4.5 6.0	TBD TBD TBD TBD	TBD 100 160 160	MHz
f	Input Frequency, OSC_{in} Externally Driven with ac-coupled signal	$V_{in} \geq 1$ Vp–p Sine Wave, OSC_{out} = No Connect, R Counter set to divide ratio such that $f_R \leq 2$ MHz	8	2.5 3.0 4.5 6.0	1 1 1 1	12 14 20 20	MHz
f_{XTAL}	Crystal Frequency, OSC_{in} and OSC_{out}	C1 ≤ 30 pF C2 ≤ 30 pF Includes Stray Capacitance	9	2.5 3.0 4.5 6.0	2 2 2 2	12 12 15 15	MHz
f_{out}	Output Frequency, REF_{out}	$C_L = 30$ pF	10, 12	2.5 3.0 4.5 6.0	dc dc dc dc	TBD TBD 10 10	MHz
f	Operating Frequency of the Phase Detectors			2.5 3.0 4.5 6.0	dc dc dc dc	TBD TBD 2 2	MHz
t_w	Output Pulse Width, ϕ_R, ϕ_V, and LD	f_R in Phase with f_V $C_L = 50$ pF	11, 12	2.5 3.0 4.5 6.0	TBD TBD 20 16	TBD TBD 100 90	ns
t_{TLH}, t_{THL}	Output Transition Times, ϕ_R, ϕ_V, LD, f_R, and f_V	$C_L = 50$ pF	11, 12	2.5 3.0 4.5 6.0	— — — —	TBD TBD 65 60	ns
C_{in}	Input Capacitance	f_{in} OSC_{in}		— —	— —	5 5	pF

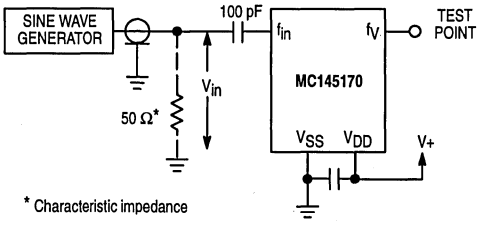


Figure 7. Test Circuit

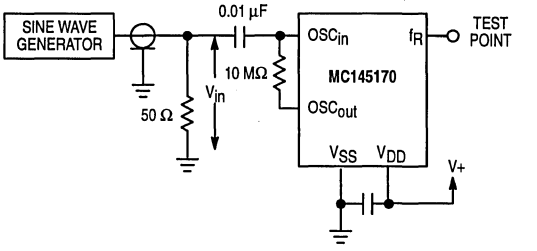


Figure 8. Test Circuit

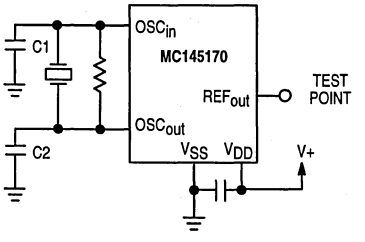


Figure 9. Test Circuit

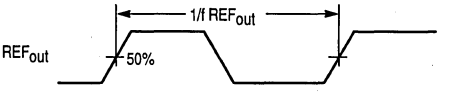


Figure 10. Switching Waveform

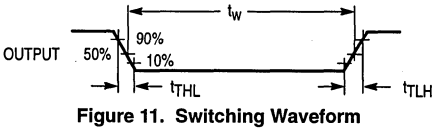


Figure 11. Switching Waveform

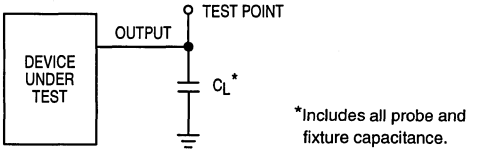


Figure 12. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 5)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low-to-high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Optionally, the R register can be accessed with a 15-bit transfer (see Table 1). The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.5 to 6.0 V. The formats are shown in Figures 13, 14, and 15.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull-up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access
(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	N Register	N15, N14, N13, . . ., N0
15 or 24	R Register	R14, R13, R12, . . ., R0
Other Values ≤ 32	None	
Values > 32	TBD	

CLK
Serial Data Clock Input (Pin 7)

Low-to-high transitions on Clock shift bits available at D_{in}, while high-to-low transitions shift bits from D_{out}. The chip's 16-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 1 and Figures 13, 14, and 15).

CLK typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

CAUTION

To guarantee proper operation of the power-on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. Do ***not*** float or toggle the CLK input during power up.

$\overline{ENB}$
Active Low Enable Input (Pin 6)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited, D_{out} is forced to the high-impedance state, and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low-to-high transition on $\overline{ENB}$ transfers data to the C, N, or R register depending on the data stream length per Table 1.

CAUTION

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt-triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

D_{out}
Three-State Serial Data Output (Pin 8)

Data is transferred out of the 16-1/2 stage shift register through D_{out} on the high-to-low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

D_{out} could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in-line QA test during board manufacturing.

Finally, D_{out} facilitates troubleshooting a system.

REFERENCE PINS

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form a reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1 to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The MC145170 is designed to operate with crystals up to 15 MHz with a 4.5 to 6.0 V supply. With supplies less than 4.5 V, up to 12-MHz crystals may be used. (See Figure 9.)

If desired, an external clock source can be ac coupled to OSC_{in}. A 0.01-μF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications. An external feedback resistor of approximately 10 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac-coupled case (see Figure 8). *OSC_{out} is an internal node on the device and should not be used to drive any loads* (i.e., OSC_{out} is unbuffered). However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 Vp-p; the maximum frequencies are given in the **Loop Specifications** table. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz when the internal phase/frequency detectors are used (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz).

If an external source is available which swings from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table, then dc coupling can be used. In the dc-coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the MC145170, as noted above. For frequencies below 1 MHz, dc coupling must be used. The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

REF_{out}
Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal-generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 13).

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on-chip power-on-initialize circuit forces REF_{out} to the OSC_{in} divided-by-8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

COUNTER OUTPUT PINS

f_R
R Counter Output (Pin 9)

This signal is the buffered output of the 15-stage R counter. f_R can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of 1 (see Figure 14). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz unless an external phase detector is used. The maximum frequency for driving external phase detectors is TBD.

When activated, the f_R signal appears as normally low and pulses high.

f_V
N Counter Output (Pin 10)

This signal is the buffered output of the 16-stage N counter. f_V can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz unless an external phase detector is used. The maximum frequency for driving external phase detectors is TBD.

When activated, the f_V signal appears as normally low and pulses high.

LOOP PINS

f_{in}
Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on-chip amplifier which drives the N counter. This signal is normally sourced from an external voltage-controlled oscillator (VCO), and is ac-coupled into f_{in}. A 100-pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 7). The frequency capability of this input is dependent on the supply voltage as listed in the **Loop Specifications** table. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz when the internal phase/frequency detectors are used (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz).

For signals which swing from at least the V_{IL} to V_{IH} levels listed in the **Electrical Characteristics** table, dc coupling may be used. Also, for low frequency signals, dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the f_{in} pin.

Each rising edge on the f_{in} pin causes the N counter to decrement by 1.

PD_{out}
Single-Ended Phase/Frequency Detector Output (Pin 13)

This is a three-state output for use as a loop error signal when combined with an external low-pass filter. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (C7) in the C register = low (see Figure 13)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high-impedance state by utilization of the disable feature in the C register (patented).

ϕ_R and ϕ_V
Double-Ended Phase/Frequency Detector Outputs (Pins 14, 15)

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by

a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 16.

POL bit (C7) in the C register = low (see Figure 13)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

LD
Lock Detector Output (Pin 11)

This output is essentially at a high level with narrow low-going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies (see Figure 16).

This output can be enabled and disabled via the C register (patented). Upon power up, on-chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

POWER SUPPLY

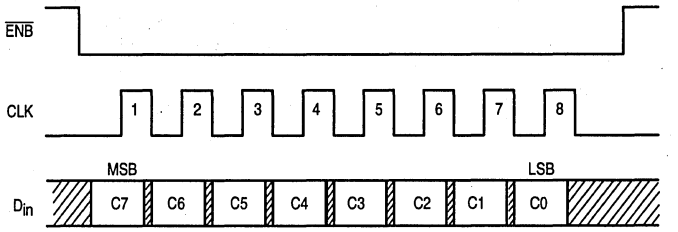
V_{DD}
Most Positive Supply Potential (Pin 16)

This pin may range from +2.5 to 6.0 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using low-inductance capacitor(s) mounted very close to the MC145170. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

V_{SS}
Most Negative Supply Potential (Pin 12)

This pin is usually ground. For measurement purposes, the V_{SS} pin is tied to a ground plane.



C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 16. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high-impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4–C2, OSC2–OSC0: Reference output controls which determine the REF_{out} characteristics as shown below. Upon power up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

C1 — f_VE: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power up.

C0 — f_RE: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power up.

Figure 13. C Register Access and Format (8 Clock Cycles are Used)

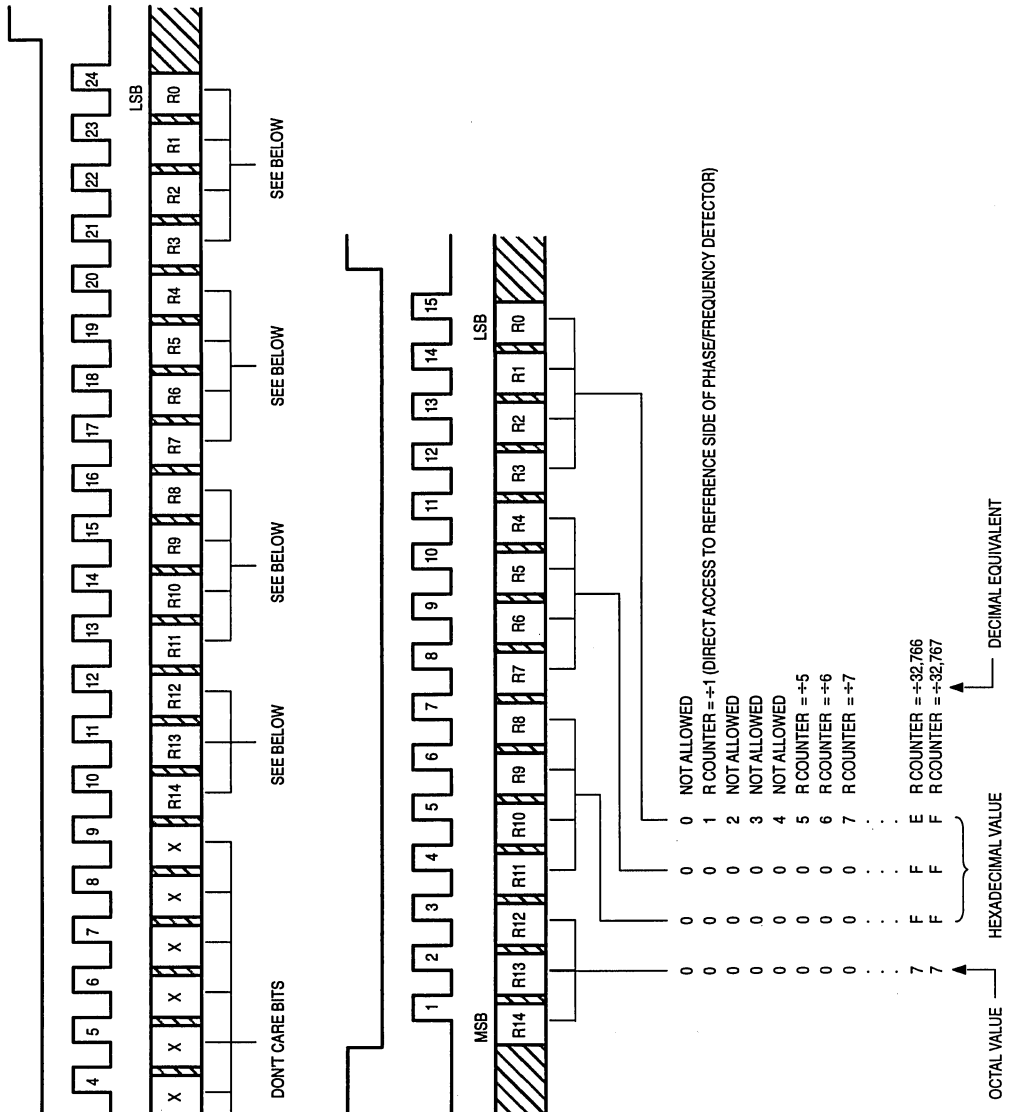


Figure 14. R Register Access and Formats (Either 24 or 15 Clock Cycles Can Be Used)

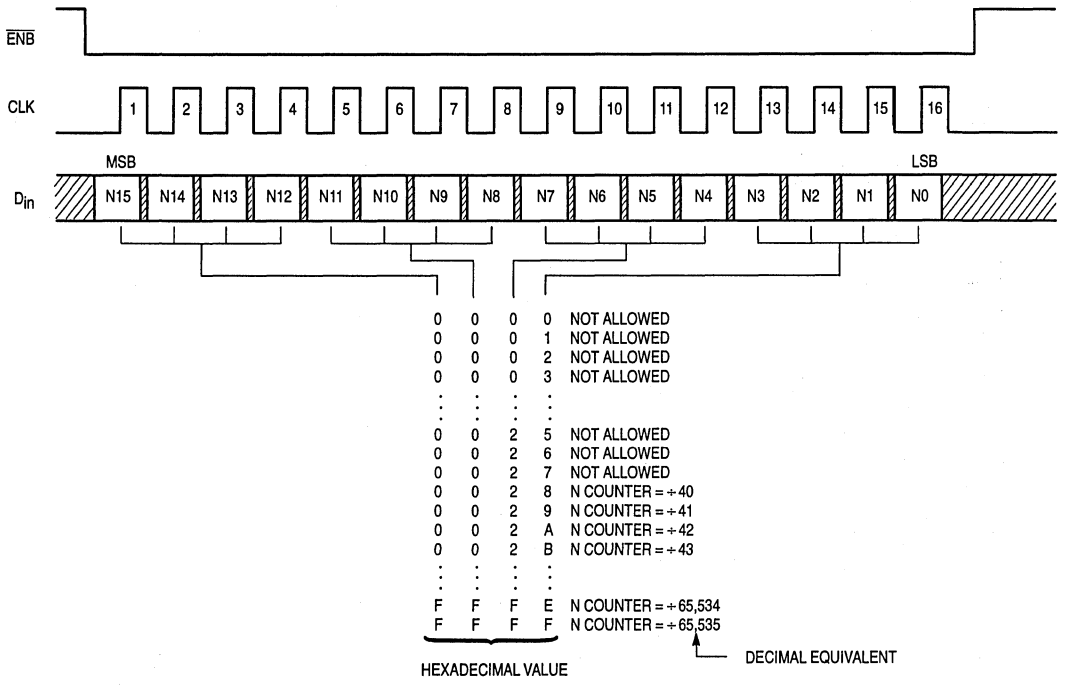
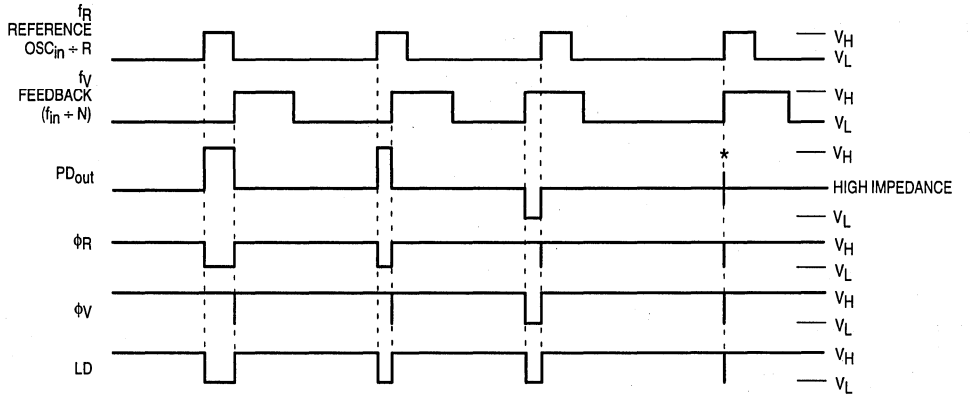


Figure 15. N Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source is forced to near mid-supply.
NOTE: The PD_{out} generates error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 13 for POL.

Figure 16. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off-Chip Reference

The user may design an off-chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to OSC_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling is used.

Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 17.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequency. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1 + C2}$$

where

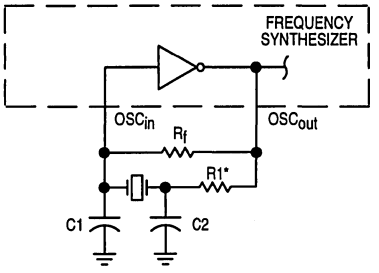
C_{in} = 5 pF (see Figure 18)
C_{out} = 6 pF (see Figure 18)
C_a = 1 pF (see Figure 18)
C1 and C2 = external capacitors (see Figure 17)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 19. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 17 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF_{out} pin (OSC_{out} is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 2).



*May be needed in certain cases. See text.

Figure 17. Pierce Crystal Oscillator Circuit

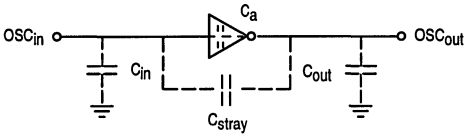
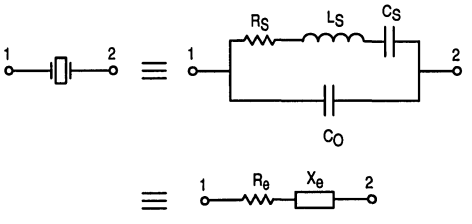


Figure 18. Parasitic Capacitances of the Amplifier and C_{stray}



Note: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 19. Equivalent Crystal Networks

Recommended Reading

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design,* March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design,* April 25, 1985.

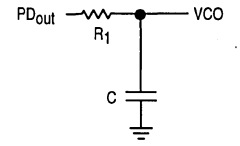
Table 2. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693-0099

Note: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE-LOCKED LOOP—LOW PASS FILTER DESIGN

(A)

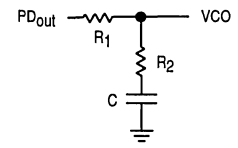


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

(B)

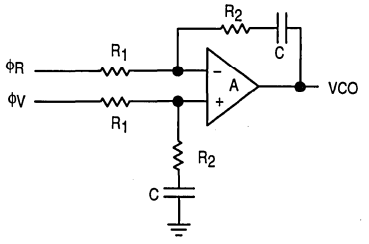


$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\,\omega_n \left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

(C)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTE:

For (C), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $V_{DD}/ 4\pi$ V/radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{DD}/2\pi$ V/radian for ϕ_V and ϕ_R

$$K_{VCO}\ (\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R-related VCO sidebands.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley-Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley-Interscience, 1980.

Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York, Wiley-Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley-Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice-Hall, 1983.

Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

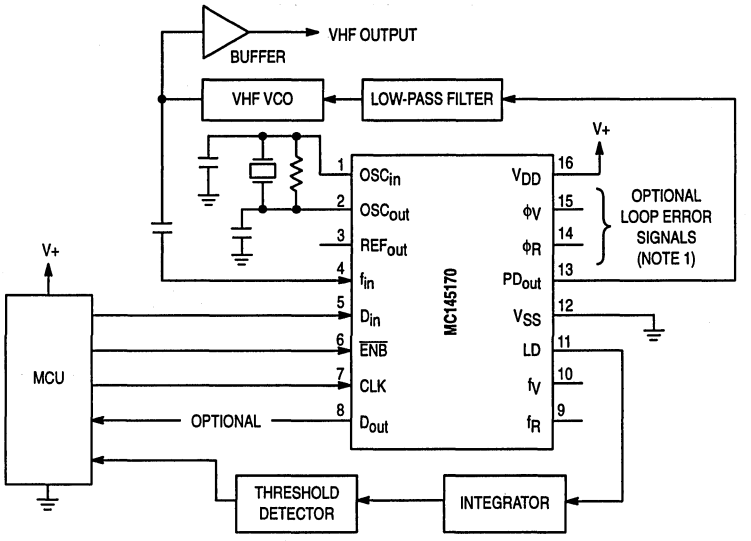
Seidman, Arthur H., *Integrated Circuits Applications Handbook,* Chapter 17, pp. 538-586. New York, John Wiley & Sons.

Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.

AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.

AN1207, The MC145170 in Basic HF and VHF Oscillators, Motorola Semiconductor Products, Inc., 1992



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop — Low-Pass Filter Design page for additional information.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} (GND) with one or more low-inductance capacitors.
3. The R counter is programmed for a divide value = OSC_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by f_R = N, where N is the divide value of the N counter.

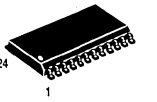
Figure 20. Example Application

MC145173

Technical Summary

Dual-Band PLL Frequency Synthesizer with ADC and Frequency Counter

CMOS

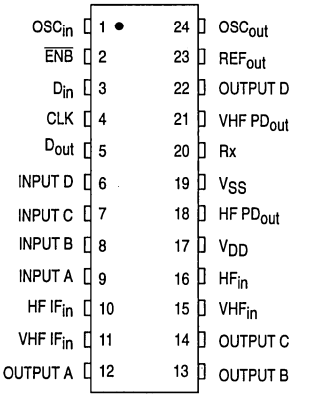


DW SUFFIX
SOG
CASE 751E

ORDERING INFORMATION

MC145173DW SOG Package

PIN ASSIGNMENT



The MC145173 is a single-chip CMOS synthesizer with a four-wire serial interface for primary use in AM-FM broadcast receivers. The device also finds use in LW (long-wave) and SW (short-wave) receivers. Two inputs to the high-speed N counter are provided along with 2 phase detectors: one for a VHF loop up to 130 MHz and another for an HF loop up to 30 MHz. The VHF phase detector has a current source/sink output and both detectors feature linear transfer functions. An external crystal ties across on-chip circuitry which drives a reference counter that is completely programmable. Thus, a broad range of tuning resolution is possible. The crystal oscillator is buffered and fed to an open-drain output which is active in the HF mode only.

Due to the patented BitGrabber™ registers, there are no address or steering bits in the serial data stream for random access of the registers. The serial port is byte-oriented to facilitate control via an MCU. Tuning across a band is accomplished with a two-byte transfer to the N register.

The 6-bit analog-to-digital converter (ADC) has two input channels. The converter is read via a one-byte transfer which includes an end-of-conversion (EOC) bit.

A 22-stage frequency counter is provided and accepts two IF (intermediate fre- quency) signals. Primary use for the frequency counter is for the seek-and-scan function on broadcast radio receivers. Reading the count is accomplished with a three-byte serial transfer which includes a count-complete (CC) bit.

Four general purpose digital outputs are included. One of the outputs is open-drain; the others are totem-pole (push-pull). Two general purpose digital inputs are provided also. One input has a comparator with a switch point at 33% of V_{DD}.

- Operating Voltage Range: 4.5 to 5.5 V
- Maximum Operating Frequency: VHF_{in} = 130 MHz @ 210 mVp-p
  HF_{in} = 30 MHz @ 210 mVp-p
- Maximum Frequency of Reference Counter: 15 MHz
- Maximum Frequency of Frequency Counter: 25 MHz
- Maximum Supply Current: Operating Mode = 25 mA
  Standby Mode = 100 µA
- Approximate ADC Conversion Time: 325 µs
- Operating Temperature Range: −40 to +85°C
- R Counter Division Range: 1 and 5 to 16,383
- N Counter Division Range: 40 to 32,767
- Direct Interface to Motorola SPI Data Port
- Order complete document as MC145173/D

BitGrabber is a trademark of Motorola, Inc.

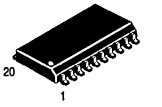
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC145190
MC145191

Advance Information

1.1 GHz PLL Frequency Synthesizers

Include On-Board 64/65 Prescalers



F SUFFIX
SOG
CASE 751J

ORDERING INFORMATION

MC145190F	SOG Package
MC145191F	SOG Package

The MC145190 and MC145191 are single-package synthesizers with serial interfaces capable of direct usage up to 1.1 GHz. A special architecture makes these PLLs very easy to program because a byte-oriented format is utilized. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 3-byte serial transfer to the 24-bit A register. The interface is both SPI and MICROWIRE™ compatible.

Each device features a single-ended current source/sink phase detector output and a double-ended phase detector output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single-ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

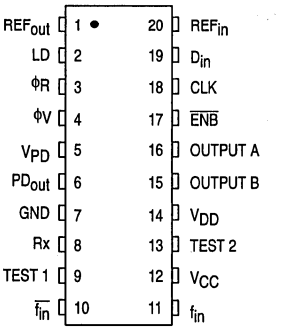
The MC145190 features logic-level converters and high-voltage phase/frequency detectors; the detector supply may range up to 9.5 V. The MC145191 has lower-voltage phase/frequency detectors optimized for single-supply systems of 5 V ±10%.

Each part includes a differential RF input which may be operated in a single-ended mode. Also featured are on-board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the parts to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on-board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

The double-buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

PIN ASSIGNMENT

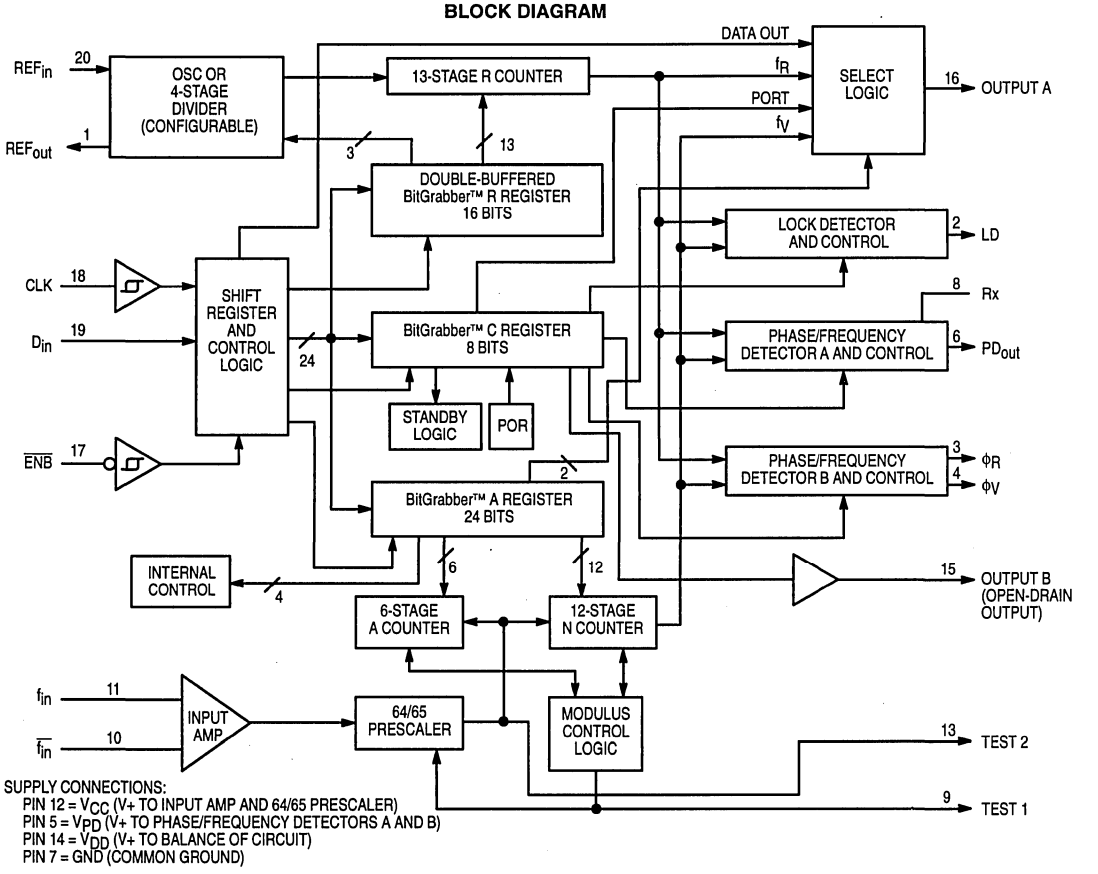


- Maximum Operating Frequency: 1100 MHz @ V_{in} = 200 mVp-p
- Operating Supply Current: 7 mA Nominal
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 4.5 to 5.5 V
- Operating Supply Voltage Range of Phase Detectors (V_{PD} Pin) —
  MC145190: 8.0 to 9.5 V
  MC145191: 4.5 to 5.5 V
- Current Source/Sink Phase Detector Output Capability: 2 mA Maximum
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: −40 to +85°C
- R Counter Division Range: 5 to 8191 plus Direct Access to Phase Detector Input
- Dual-Modulus Capability Provides Total Division up to 262,143
- High-Speed Serial Interface: 4 Mbps
- OUTPUT A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General-Purpose Digital Outputs — OUTPUT A: Totem-Pole (Push-Pull)
  OUTPUT B: Open-Drain
- Patented Power-Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 50 μA
- The MC145190EVK is the evaluation platform for the MC145190
- The MC145191EVK is the evaluation platform for the MC145191

This document contains information on a new product. Specifications and information herein are subject to change without notice.
BitGrabber is a trademark of Motorola Inc. MICROWIRE is a trademark of National Semiconductor Corp.

REV. 2

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	−0.5 to +6.0	V
V_{PD}	DC Supply Voltage (Pin 5) MC145190 MC145191	V_{DD} −0.5 to +9.5 V_{DD} −0.5 to +6.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (except OUTPUT B, PD_{out}, φR, φV)	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (OUTPUT B, PD_{out}, φR, φV)	−0.5 to V_{PD} +0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	±10	mA
I_{out}	DC Output Current, per Pin	±20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	±30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = 4.5 to 5.5 V, Voltages Referenced to GND, T_A = −40 to +85°C, unless otherwise stated; MC145190: V_{PD} = 8.0 to 9.5 V; MC145191: V_{PD} = 4.5 to 5.5 V with $V_{DD} \leq V_{PD}$.

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode	0.3 × V_{DD}	V
V_{IH}	Minimum High-Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode	0.7 × V_{DD}	V
V_{hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		300	mV
V_{OL}	Maximum Low-Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = 20 μA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High-Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = −20 μA, Device in Reference Mode	V_{DD} − 0.1	V
I_{OL}	Minimum Low-Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = 0.4 V	0.36	mA
I_{OH}	Minimum High-Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = V_{DD} − 0.4 V for REF_{out}, LD V_{out} = V_{PD} − 0.4 V for ϕ_R, ϕ_V	−0.36	mA
I_{OL}	Minimum Low-Level Output Current (OUTPUT A, OUTPUT B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High-Level Output Current (OUTPUT A, Only)	V_{out} = V_{DD} − 0.4 V	−0.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V_{DD} or GND, Device in XTAL Mode	±1.0	μA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V_{DD} or GND, Device in Reference Mode	±150	μA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{out} = V_{PD} − 0.5 V or 0.5 V, Output in High-Impedance State — MC145190 MC145191	±150 ±200	nA
I_{OZ}	Maximum Output Leakage Current (OUTPUT B)	V_{out} = V_{PD} or GND, Output in High-Impedance State	±10	μA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	V_{in} = V_{DD} or GND; Outputs Open; Device in Standby Mode, Shut-Down Crystal Mode or REF_{out}-Static-Low Reference Mode; OUTPUT B Controlling V_{CC} per Figure 21	50*	μA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static Low or High, Bit C4 = Low Which is ***not*** Standby, I_{Rx} = 113 μA	600*	μA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is ***not*** Standby	30*	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 1.1 GHz; REF_{in} = 13 MHz @ 1 Vp-p; OUTPUT A = Inactive and No Connect; REF_{out} ÷ 8; ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, $\overline{ENB}$, CLK = V_{DD} or GND, Phase Detector B Selected (Bit C6 = Low)	**	mA

*MC145191 only

**The nominal value = 7 mA. This is not a guaranteed limit.

ANALOG CHARACTERISTICS—CURRENT SOURCE/SINK OUTPUT—PD_{out}
($I_{out} \leq 2$ mA, $V_{DD} = V_{CC} = 4.5$ to 5.5 V, $V_{DD} \leq V_{PD}$. Voltages Referenced to GND)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation (Part-to-Part)	MC145190: $V_{out} = 0.5 \times V_{PD}$	8.0	±20	%
		9.5	±20	
	MC145191: $V_{out} = 0.5 \times V_{PD}$	4.5	±20	%
		5.5	±20	
Maximum Sink-vs-Source Mismatch (Note 3)	MC145190: $V_{out} = 0.5 \times V_{PD}$	8.0	12	%
		9.5	12	
	MC145191: $V_{out} = 0.5 \times V_{PD}$	4.5	12	%
		5.5	12	
Output Voltage Range (Note 3)	MC145190: I_{out} variation ≤ 20%	8.0	0.5 to 7.5	V
		9.5	0.5 to 9.0	
	MC145191: I_{out} variation ≤ 20%	4.5	0.5 to 4.0	V
		5.5	0.5 to 5.0	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for any specific temperature within –40 to +85°C.
4. The analog characteristics for PD_{out} are preliminary and subject to change for the MC145190.

AC INTERFACE CHARACTERISTICS ($V_{DD} = 4.5$ to 5.5 V, $T_A = -40$ to +85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns; MC145190: $V_{PD} = 8.0$ to 9.5 V; MC145191: $V_{PD} = 4.5$ to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Figure #	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to OUTPUT A (Selected as Data Out)	1, 5	105	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT A (Selected as Port)	2, 5	100	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT B	2, 6	120	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, OUTPUT A and OUTPUT B; t_{THL} ONLY, on OUTPUT B	1, 5, 6	100	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK		10	pF

TIMING REQUIREMENTS
($V_{DD} = V_{CC} = 4.5$ to 5.5 V, $T_A = -40$ to +85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Figure #	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	20	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{ENB}$ vs CLK	4	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	4	*	cycles
t_w	Minimum Pulse Width, CLK	1	125	ns
t_r, t_f	Maximum Input Rise and Fall Times – CLK, $\overline{ENB}$	1	100	µs

*The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

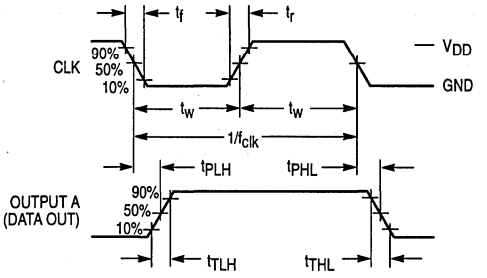


Figure 1.

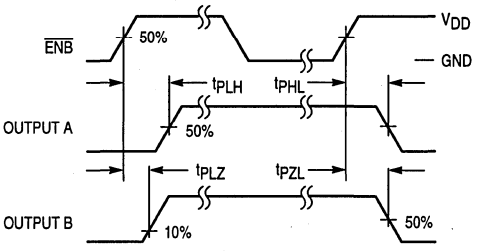


Figure 2.

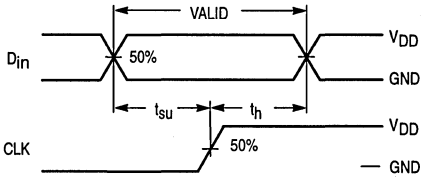


Figure 3.

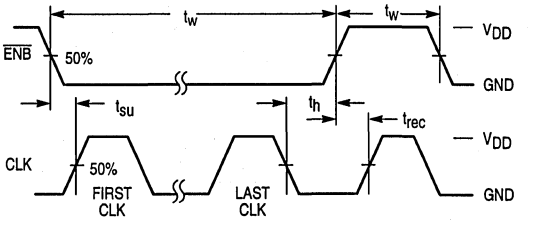
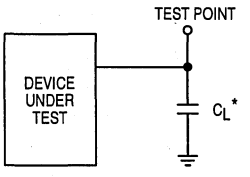
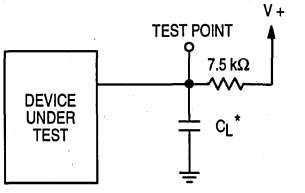


Figure 4.



*Includes all probe and fixture capacitance.

Figure 5. Test Circuit



*Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 4.5 to 5.5 V unless otherwise indicated, T_A = −40 to +85°C)

Symbol	Parameter	Test Condition	Figure #	Guaranteed Operating Range		Unit
				Min	Max	
V_{in}	Input Voltage Range, f_{in}	100 MHz ≤ f_{in} < 250 MHz 250 MHz ≤ f_{in} ≤ 1100 MHz	7	400 200	1500 1500	mVp-p
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode	V_{in} = 400 mVp-p V_{in} = 1 Vp-p R Counter set to divide ratio such that f_R ≤ 2 MHz; REF Counter set to divide ratio such that REF_{out} ≤ 10 MHz	8	12 4.5*	27 27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance; R Counter and REF Counter same as above	9	2	15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 30 pF	10, 12	dc	10	MHz
f	Operating Frequency of the Phase Detectors			dc	2	MHz
t_W	Output Pulse Width, ϕ_R, ϕ_V, LD — MC145191	f_R in Phase with f_V, C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	20	100	ns
t_{TLH}, t_{THL}	Output Transition Times, LD, ϕ_V, ϕ_R — MC145191	C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	—	65	ns
C_{in}	Input Capacitance, REF_{in}			—	5	pF

*If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal.

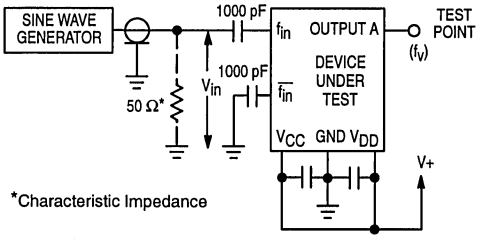


Figure 7. Test Circuit

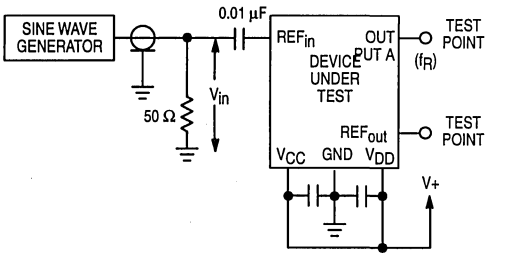


Figure 8. Test Circuit–Reference Mode

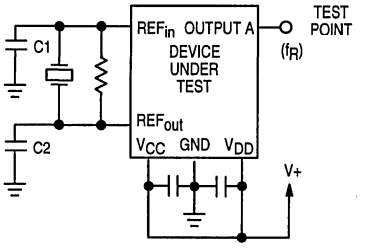


Figure 9. Test Circuit–Crystal Mode

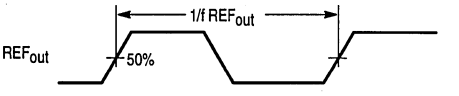


Figure 10. Switching Waveform

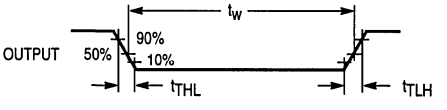


Figure 11. Switching Waveform

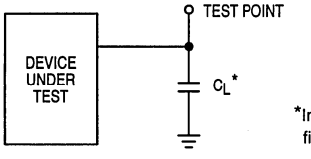


Figure 12. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 19)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low-to-high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 1). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

CAUTION

The value programmed for the N-counter must be greater than or equal to the value of the A-counter.

The 13 least significant bits (LSBs) of the R register are double-buffered. As indicated above, data is latched into the first buffer on a 16-bit transfer. (The 3 MSBs are not double-buffered and have an immediate effect after a 16-bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24-bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16-bit transfer may be followed by pulsing $\overline{ENB}$ low with no signal on the CLK pin. This is an alternate method of transferring data to the second buffer of the R register (see Figure 16).

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 4.5 to 5.5 V. The formats are shown in Figures 13, 15, and 16.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull-up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access
(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 22–25	

CLK
Serial Data Clock Input (Pin 18)

Low-to-high transitions on CLK shift bits available at the D_{in} pin, while high-to-low transitions shift bits from OUTPUT A (when configured as Data Out, see Pin 16). The 24-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty-four cycles are used to access the A register. See Table 1 and Figures 13, 15, and 16. The number of clocks required for cascaded devices is shown in Figures 23 through 25.

CLK typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

CAUTION

To guarantee proper operation of the Power-On Reset (POR) circuit, the CLK pin must be grounded or held low during power up.

$\overline{ENB}$
Active Low Enable Input (Pin 17)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low-to-high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt-triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

CAUTION

$\overline{ENB}$ must not be floated or toggled during power up. It is preferable to hold $\overline{ENB}$ at the potential of the V_{DD} pin during power up to guarantee proper operation of the POR circuit.

OUTPUT A
Configurable Digital Output (Pin 16)

OUTPUT A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 15.

If A23 = A22 = high, OUTPUT A is configured as f_R. This signal is the buffered output of the 13-stage R counter. The f_R signal appears as normally low and pulses high, and can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0–R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of 1 (see Figure 16). The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R should not exceed 2 MHz.

If A23 = high and A22 = low, OUTPUT A is configured as f_V. This signal is the buffered output of the 12-stage N counter. The f_V signal appears as normally low and pulses high, and can be used to verify the operation of the prescaler, A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is N × 64 + A. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 15. The maximum frequency at which the phase detectors operate

The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V should not exceed 2 MHz.

If A23 = low and A22 = high, OUTPUT A is configured as Data Out. This signal is the serial output of the 24-1/2-stage shift register. The bit stream is shifted out on the high-to-low transition of the CLK input. Upon power up, OUTPUT A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, OUTPUT A is configured as Port. This signal is a general-purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

OUTPUT B

Open-Drain Digital Output (Pin 15)

This signal is a general-purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, OUTPUT B assumes the high-impedance state. OUTPUT B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. **Note:** the maximum voltage allowed on the V_{PD} pin is 9.5 V for the MC145190 and 5.5 V for the MC145191.

Upon power-up, power-on reset circuitry forces OUTPUT B to a low level.

REFERENCE PINS

REF_{in} and REF_{out}

Reference Input and Reference Output (Pins 20 and 1)

Configurable pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 16.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate values as recommended by the crystal supplier are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The device is designed to operate with crystals up to 15 MHz; the required connections are shown in Figure 9. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary, respectively). This is the active-crystal mode shown in Figure 16. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut-down crystal mode (shown in Figure 16) and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal up to 27 MHz from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. Due to an on-board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 16 shows how to obtain ratios of eight, four, and two. A ratio of one-to-one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 10 MHz. Therefore, for REF_{in} frequencies above 10 MHz, the one-to-one ratio may not be used. Likewise, for REF_{in} frequencies above 20 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in} and $\overline{f_{in}}$

Frequency Inputs (Pins 11 and 10)

These pins are frequency inputs from the VCO. These pins feed the on-board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they usually are used in a single-ended configuration (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out}

Single-Ended Phase/Frequency Detector Output (Pin 6)

This is a three-state current-source/sink output for use as a loop error signal when combined with an external low-pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 13)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current-sinking pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current-sourcing pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current-sourcing pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current-sinking pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high-impedance state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the high-impedance state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)
Double-Ended Phase/Frequency Detector Outputs

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 13)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase
POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD
Lock Detector Output (Pin 2)

This output is essentially at a high level with narrow low-going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V (see Figure 17).

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on-chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx
External Resistor (Pin 8)

A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Tables 2 and 3 for other values of current. To achieve a maximum current of 2 mA, the resistor should be about 47 kΩ when V_{PD} is 9 V or about 18 kΩ when V_{PD} is 5.0 V. See Figure 14 if lower maximum current values are desired.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

TEST POINT PINS

TEST 1
Modulus Control Signal (Pin 9)

This pin may be used in conjunction with the Test 2 pin for access to the on-board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace. There is the possibility that the final production version of the device will have this lead clipped at the body of the package.

TEST 2
Prescaler Output (Pin 13)

This pin may be used to access to the on-board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace. There is the possibility that the final production version of the device will have this lead clipped at the body of the package.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply (Pin 14)

This pin supplies power to the main CMOS digital portion of the device. The voltage range is + 4.5 to + 5.5 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low-inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC}
Positive Power Supply (Pin 12)

This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is +4.5 to +5.5 V with respect to the GND pin. In the standby mode, the V_{CC} pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 21.

For optimum performance, V_{CC} should be bypassed to GND using a low-inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{PD}
Positive Power Supply (Pin 5)

This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin must be no less than the potential applied to the V_{DD} pin. The maximum voltage can be +9.5 V with respect to the GND pin for the MC145190 and +5.5 V for the MC145191.

For optimum performance, V_{PD} should be bypassed to GND using a low-inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

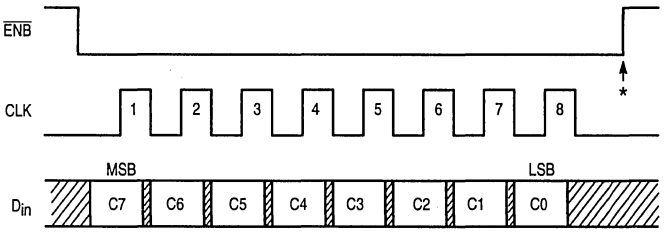
GND
Ground (Pin 7)

Common ground.

can be +9.5 V with respect to the GND pin for the MC145190 and +5.5 V for the MC145191.

For optimum performance, V_{PD} should be bypassed to GND using a low-inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND
Ground (Pin 7)
Common ground.



*At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high-impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output (LD) when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 — STBY: When set, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high-impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.

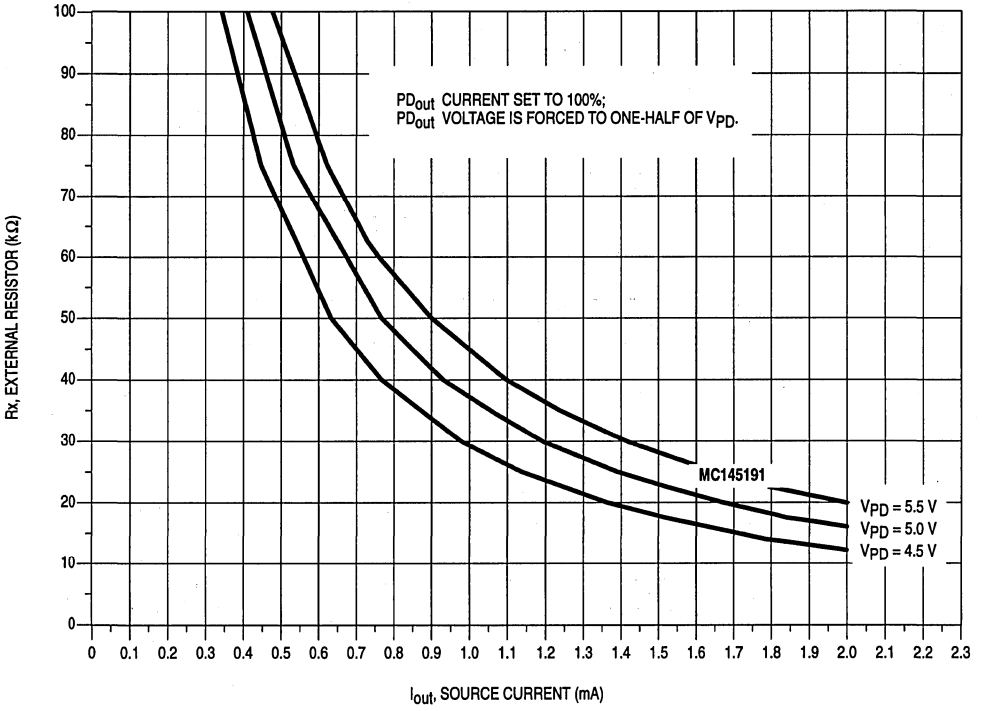
When C4 is reset low, the part is taken out of standby in 2 steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C3, C2 — I2, I1: Controls the PD_{out} source/sink current per Tables 2 and 3. With both bits high, the maximum current (as set by Rx per Figure 14) is available. Also, see C1 bit description.

C1 — Port: When the OUTPUT A pin is selected as "Port" via bits A22 and A23, C1 determines the state of OUTPUT A. When C1 is set high, OUTPUT A is forced high; C1 low forces OUTPUT A low. When OUTPUT A is NOT selected as "Port," C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 2 and 3.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when OUTPUT A is selected as "Port." The Port bit is not affected by the standby mode.

C0 — Out B: Determines the state of OUTPUT B. When C0 is set high, OUTPUT B is high-impedance; C0 low forces OUTPUT B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 13. C Register Access and Format (8 Clock Cycles are Used)



NOTE: The MC145191 is optimized for Rx values in the 18 kΩ to 40 kΩ range. For example, to achieve 0.3 mA of output current, it is preferable to use a 30-kΩ resistor for Rx and bit settings for 25% (as shown in Table 3).

Figure 14. Nominal Source Current for the PD_{out} Pin

Table 2. PD_{out} Current, C1 = Low with OUTPUT A *NOT* Selected as "Port"; Also, Default Mode When OUTPUT A Selected as "Port"

C3	C2	PD_{out} Current
0	0	70%
0	1	80%
1	0	90%
1	1	100%

Table 3. PD_{out} Current, C1 = High with OUTPUT A *NOT* Selected as "Port"

C3	C2	PD_{out} Current
0	0	25%
0	1	50%
1	0	75%
1	1	100%

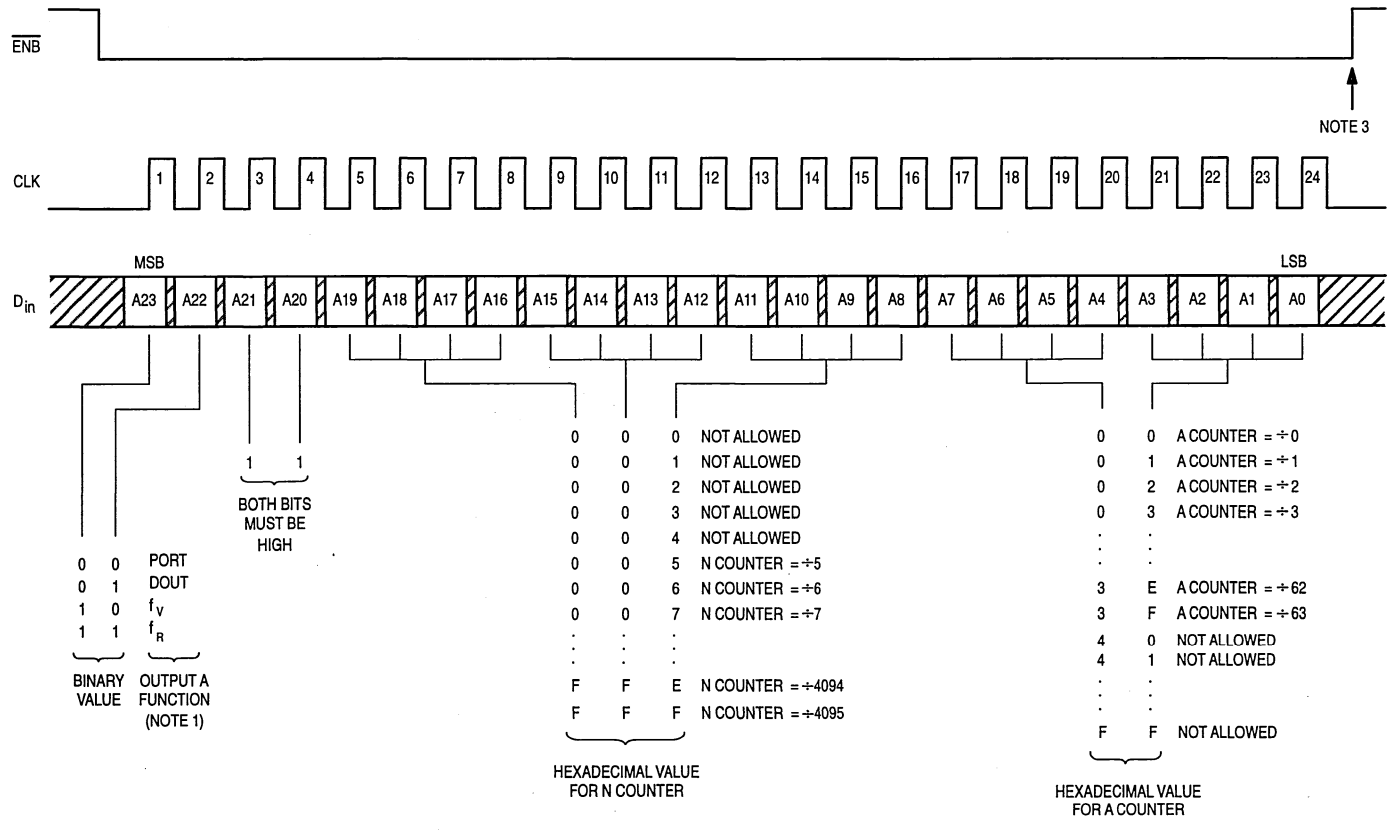
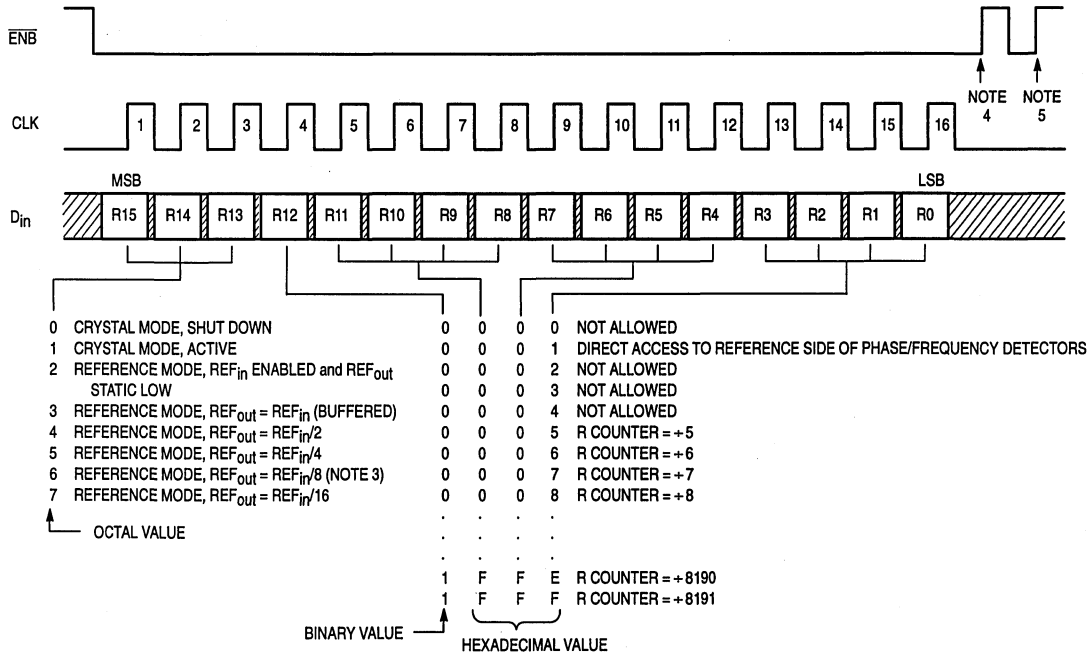


Figure 15. A Register Access and Format (24 Clock Cycles are Used)

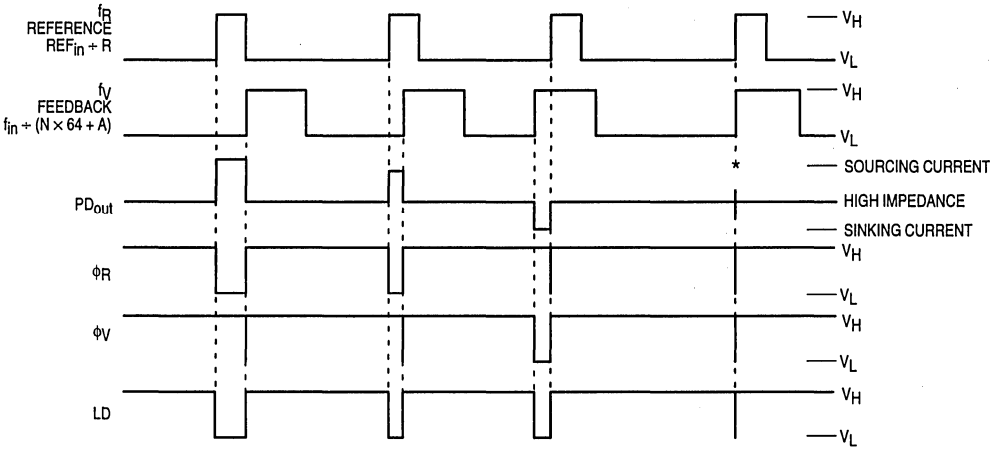
NOTES:
1. A power-on initialize circuit forces the OUTPUT A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.



NOTES:

1. Bits R15 through R13 control the configurable "OSC or 4-stage divider" block (see Block Diagram).
2. Bits R12 through R0 control the "13-stage R counter" block (see Block Diagram).
3. A power-on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4-Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double-buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. At this point, bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note 3 of Figure 15 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

Figure 16. R Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
NOTE: The PD_{out} either sources or sinks current during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor. PD_{out}, ϕR, and ϕV are shown with the polarity bit (POL) = low; see Figure 13 for POL.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off-Chip Reference

The user may design an off-chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C_L) which does not exceed approximately 20 pF when used at the highest operating frequency of 15 MHz. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)

C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at OUTPUT A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 4).

RECOMMENDED READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

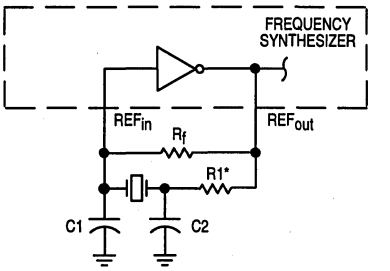
E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE*, Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology*, June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.



*May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

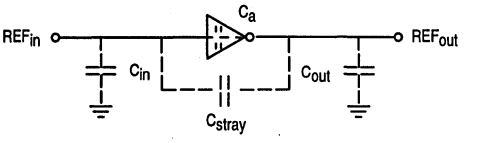
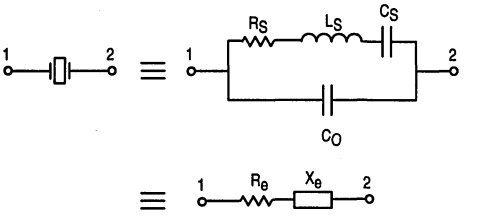


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}



Note: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

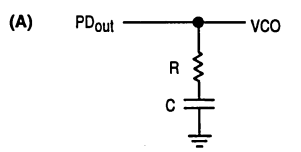
Table 4. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693-0099

Note: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE-LOCKED LOOP—LOW PASS FILTER DESIGN

(A)



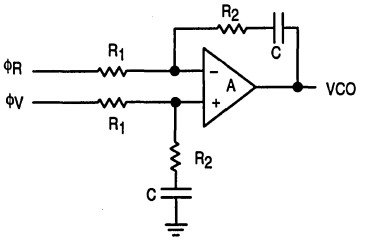
$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:
For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_C = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:
For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}
K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

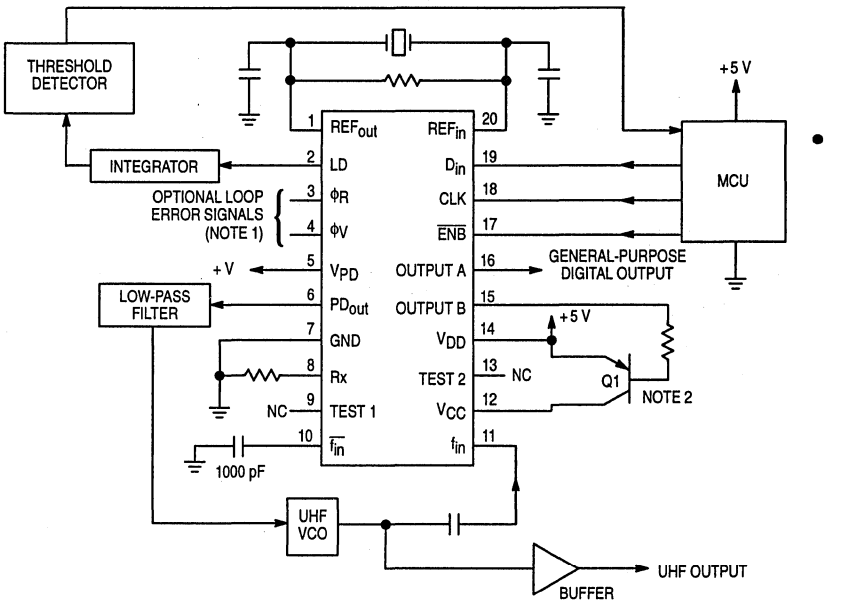
$$K_{VCO}\text{ (VCO Transfer Function)} = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}\text{ radians per volt}$$

For a nominal design starting point, the user might consider a damping factor ζ=0.7 and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R-related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R-related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook,* Chapter 17, pp. 538-586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop — Low-Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general-purpose digital pin, OUTPUT B. If the standby feature is not needed, tie pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low-inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 21. Example Application

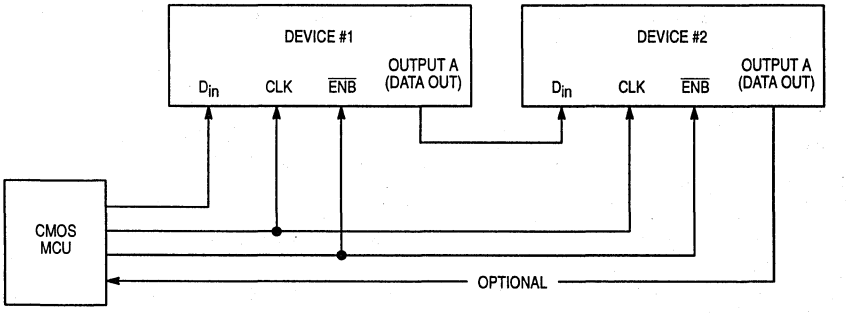
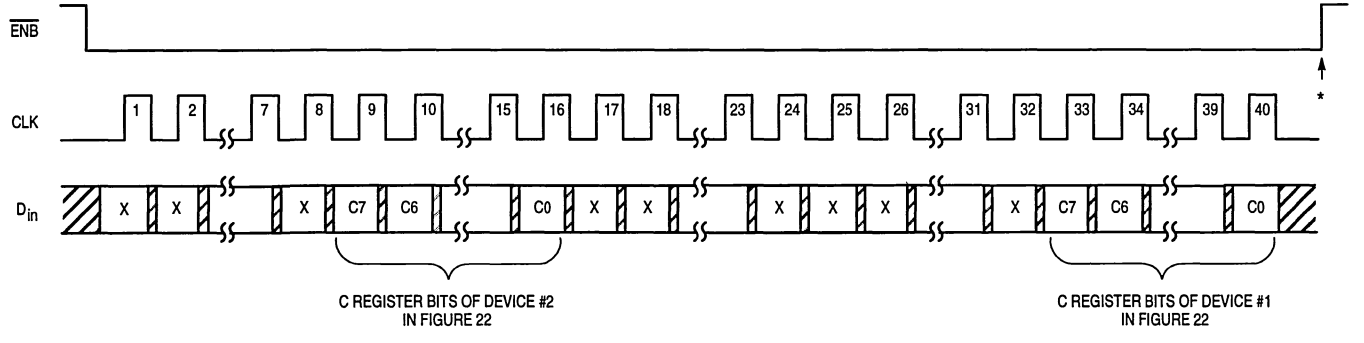
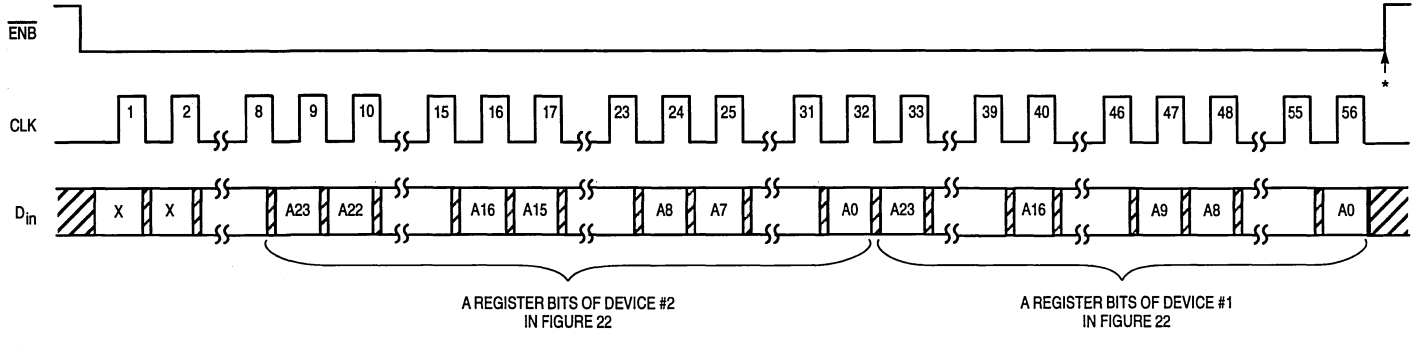


Figure 22. Cascading Two Devices



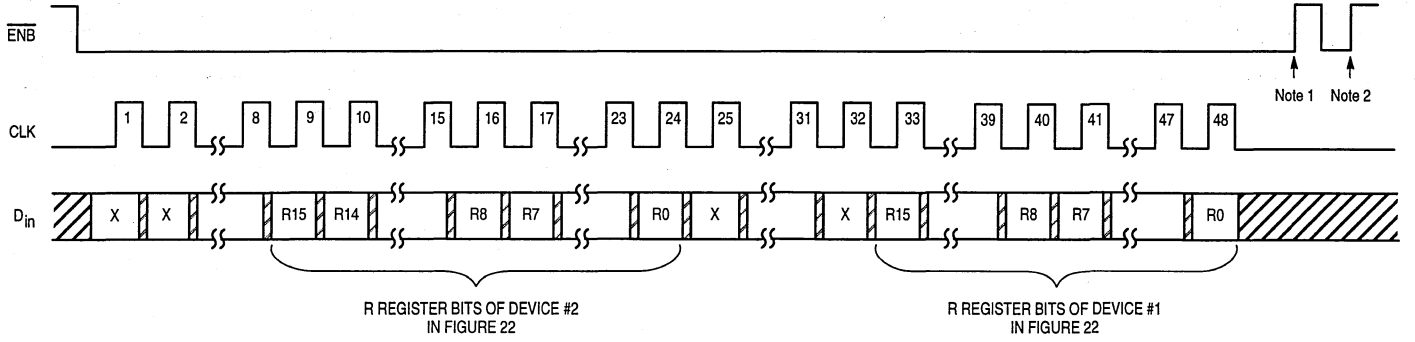
*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

Figure 23. Accessing the C Registers of Two Cascaded Devices



*At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

Figure 24. Accessing the A Registers of Two Cascaded Devices



NOTES APPLICABLE TO EACH DEVICE:

1. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4-Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double-buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. At this point, the bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note of Figure 24 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

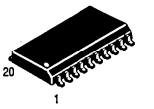
Figure 25. Accessing the R Registers of Two Cascaded Devices

MC145192

Advance Information

Low-Voltage 1.1 GHz PLL Frequency Synthesizer

Includes On-Board 64/65 Prescaler

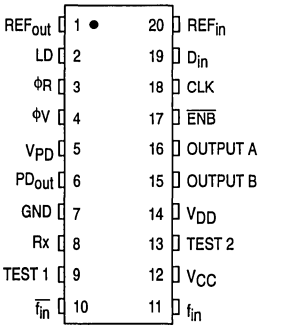


F SUFFIX
SOG
CASE 751J

ORDERING INFORMATION

MC145192F SOG Package

PIN ASSIGNMENT



The MC145192 is a low-voltage single-package synthesizer with serial interface capable of direct usage up to 1.1 GHz. A special architecture makes this PLL very easy to program because a byte-oriented format is utilized. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Tuning can be accomplished via a 3-byte serial transfer to the 24-bit A register. The interface is both SPI and MICROWIRE™ compatible.

The device features a single-ended current source/sink phase detector A output and a double-ended phase detector B output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single-ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

The MC145192 phase/frequency detector B ϕR and ϕV outputs can be powered from 2.7 to 5.5 V. This is optimized for 3-V systems. The phase/frequency detector A PD_{out} output must be powered from 4.5 to 5.5 V, and is optimized for a 5-V supply.

This part includes a differential RF input which may be operated in a single-ended mode. Also featured are on-board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on-board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

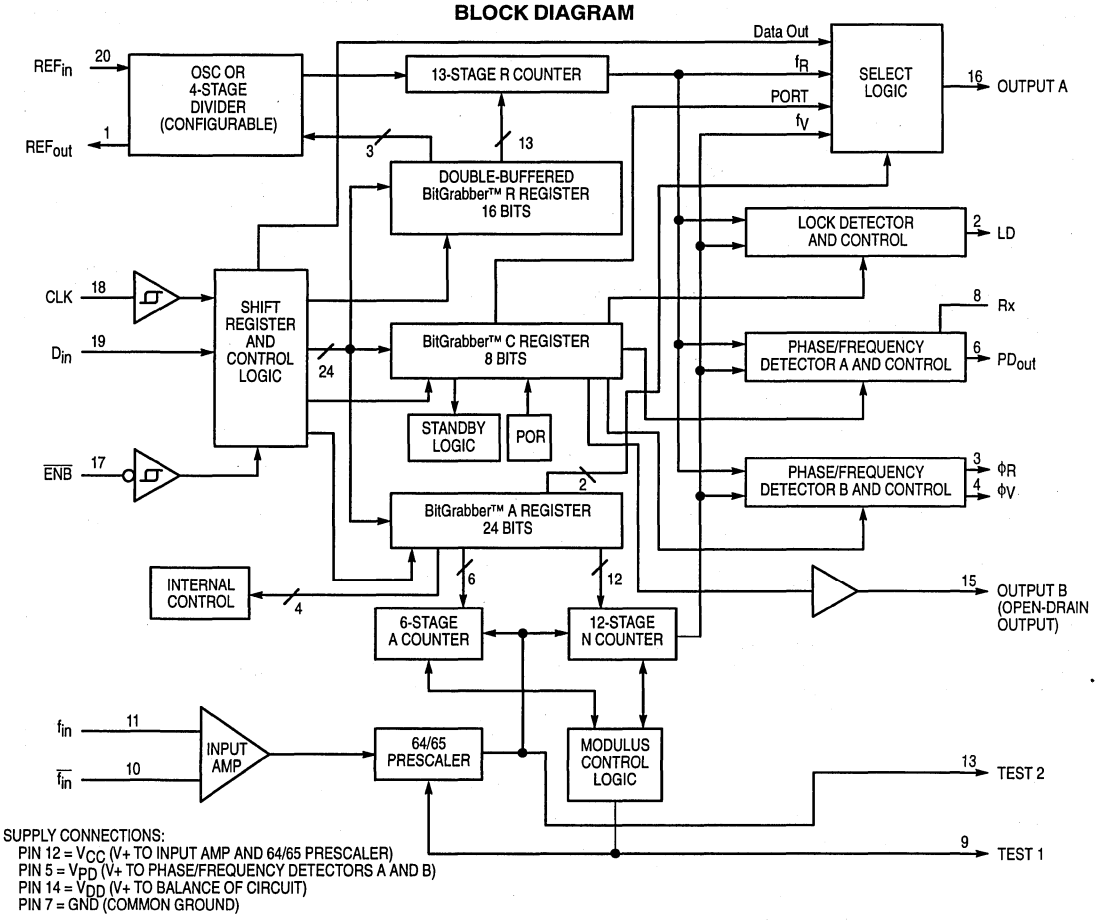
The double-buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 1100 MHz @ V_{in} = 200 mVp-p
- Operating Supply Current: 6 mA Nominal at 2.7 V
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 2.7 to 5.0 V
- Operating Supply Voltage Range of Phase Freq. Detector A (V_{PD} Pin): 4.5 to 5.5 V
- Operating Supply Voltage Range of Phase Detector B (V_{PD} Pin): 2.7 to 5.5 V
- Current Source/Sink Phase Detector Output Capability: 2 mA Maximum
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: −40 to +85°C
- R Counter Division Range: 5 to 8191 Plus Direct Access to Phase Detector Input
- Dual-Modulus Capability Provides Total Division up to 262,143
- High-Speed Serial Interface: 2 Mbps
- OUTPUT A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General-Purpose Digital Outputs — OUTPUT A: Totem-Pole (Push-Pull) with Four Output Modes
  OUTPUT B: Open-Drain
- Patented Power-Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 50 µA

This document contains information on a new product. Specifications and information herein are subject to change without notice.
BitGrabber is a trademark of Motorola Inc. MICROWIRE is a trademark of National Semiconductor Corp.

REV. 1

BLOCK DIAGRAM



SUPPLY CONNECTIONS:
PIN 12 = V_{CC} (V+ TO INPUT AMP AND 64/65 PRESCALER)
PIN 5 = V_{PD} (V+ TO PHASE/FREQUENCY DETECTORS A AND B)
PIN 14 = V_{DD} (V+ TO BALANCE OF CIRCUIT)
PIN 7 = GND (COMMON GROUND)

MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	−0.5 to +6.0	V
V_{PD}	DC Supply Voltage (Pin 5)	V_{DD} −0.5 to +6.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (except OUTPUT B, PD_{out}, ϕR, ϕV)	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (OUTPUT B, PD_{out}, ϕR, ϕV)	−0.5 to V_{PD} +0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	±10	mA
I_{out}	DC Output Current, per Pin	±20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	±30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = 2.7 to 5.0 V, Voltages Referenced to GND, T_A = −40 to +85°C, unless otherwise stated;
Phase/Frequency Detector A V_{PD} = 4.5 to 5.5 V with $V_{DD} \le V_{PD}$; Phase/Frequency Detector B V_{PD} = 2.7 to 5.5 V with $V_{DD} \le V_{PD}$.

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode	0.2 × V_{DD}	V
V_{IH}	Minimum High-Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode	0.8 × V_{DD}	V
V_{Hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)	V_{DD} = 2.7 V V_{DD} = 5.0 V	100 300	mV
V_{OL}	Maximum Low-Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = 20 µA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High-Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = −20 µA, Device in Reference Mode	V_{DD} − 0.1	V
I_{OL}	Minimum Low-Level Output Current (REF_{out}, LD)	V_{out} = 0.4 V	0.25	mA
I_{OL}	Minimum Low-Level Output Current (ϕ_R, ϕ_V)	V_{out} = 0.4 V V_{DD}, V_{PD} = 2.7 V	0.36	mA
I_{OL}	Minimum Low-Level Output Current (OUTPUT A)	V_{out} = 0.4 V	0.6	mA
I_{OL}	Minimum Low-Level Output Current (OUTPUT B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High-Level Output Current (REF_{out}, LD)	V_{out} = V_{DD} − 0.4 V	−0.25	mA
I_{OH}	Minimum High-Level Output Current (ϕ_R, ϕ_V)	V_{out} = V_{PD} − 0.4 V V_{DD}, V_{PD} = 2.7 V	−0.36	mA
I_{OH}	Minimum High-Level Output Current (OUTPUT A Only)	V_{out} = V_{DD} − 0.4 V	−0.35	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V_{DD} or GND, Device in XTAL Mode	±1.0	µA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V_{DD} or GND, Device in Reference Mode	±150	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{out} = V_{PD} − 0.5 V or 0.5 V, Output in High-Impedance State	±200	nA
	(OUTPUT B)	V_{out} = V_{PD} or GND Output in High-Impedance State	±10	µA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	V_{in} = V_{DD} or GND; Outputs Open; Device in Standby Mode, Shut-Down Crystal Mode or REF_{out}-Static-Low Reference Mode; OUTPUT B Controlling V_{CC} per Figure 21	50	µA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static Low or High, Bit C4 = Low Which is ***not*** Standby, I_{Rx} = 113 µA, V_{PD} = 5.5 V	600	µA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is ***not*** Standby	30	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 1.1 GHz; REF_{in} = 13 MHz @ 1 Vp-p; OUTPUT A = Inactive and No Connect; V_{DD} = V_{CC}, REF_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, $\overline{ENB}$, CLK = V_{DD} or GND, Phase Detector B Selected (Bit C6 = Low)	*	mA

* The nominal values are:
6 mA at V_{DD} = 2.7 V and V_{PD} = 2.7 V
9 mA at V_{DD} = 5.0 V and V_{PD} = 5.5 V
These are not guaranteed limits.

ANALOG CHARACTERISTICS—CURRENT SOURCE/SINK OUTPUT—PD_{out}

($I_{out} \leq 2$ mA, $V_{DD} = V_{CC} = 2.7$ to 5.0 V, Voltages Referenced to GND, $V_{DD} = V_{CC} \leq V_{PD}$)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation (Part-to-Part)	$V_{out} = 0.5 \times V_{PD}$	4.5	±20	%
		5.5	±20	
Maximum Sink-vs-Source Mismatch (Note 3)	$V_{out} = 0.5 \times V_{PD}$	4.5	12	%
		5.5	12	
Output Voltage Range (Note 3)	I_{out} variation ≤ 20%	4.5	0.5 to 4.0	V
		5.5	0.5 to 5.0	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within –40 to +85°C.

AC INTERFACE CHARACTERISTICS

($V_{DD} = V_{CC} = 2.7$ to 5.0 V, $T_A = -40$ to +85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns; $V_{PD} = 2.7$ to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Figure #	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	dc to 2.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to OUTPUT A (Selected as Data Out)	1, 5	200	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT A (Selected as Port)	2, 5	200	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT B	2, 6	200	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, OUTPUT A and OUTPUT B; t_{THL} only, on OUTPUT B	1, 5, 6	200	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK,		10	pF

TIMING REQUIREMENTS

($V_{DD} = V_{CC} = 2.7$ to 5.0 V, $T_A = -40$ to +85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Figure #	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	50	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{ENB}$ vs CLK	4	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	4	*	cycles
t_w	Minimum Pulse Width, CLK	1	125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	100	µs

*The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

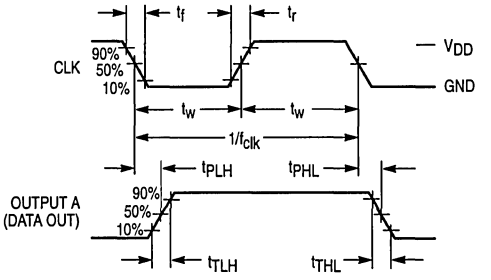


Figure 1.

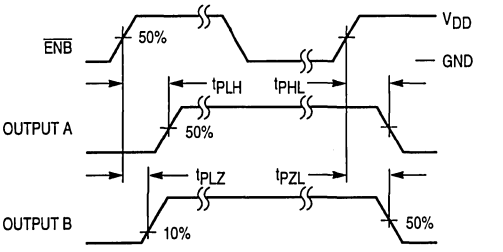


Figure 2.

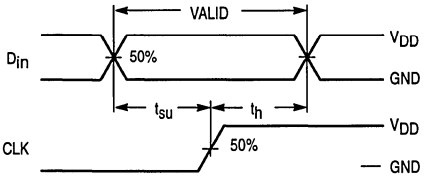


Figure 3.

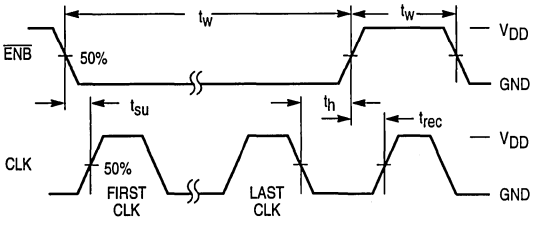
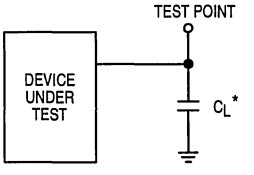
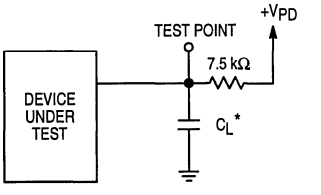


Figure 4.



*Includes all probe and fixture capacitance.

Figure 5. Test Circuit



*Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 2.7 to 5.0 V unless otherwise indicated, T_A = −40 to +85°C)

Symbol	Parameter	Test Condition	Fig #	Guaranteed Operating Range		Unit
				Min	Max	
V_{in}	Input Voltage Range, f_{in}	100 MHz ≤ f_{in} < 250 MHz 250 MHz ≤ f_{in} ≤ 1100 MHz	7	400 200	1500 1500	mVp-p
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode	V_{in} = 400 mVp-p, R Counter set to divide ratio such that f_R ≤ 1 MHz, REF Counter set to divide ratio such that REF_{out} ≤ 5 MHz	8			MHz
		V_{DD} = 2.7 V		1	20	
		V_{DD} = 3.0 V		4.5	20	
		V_{DD} = 3.5 V		5.5	20	
		V_{DD} = 4.5 to 5 V		12	27	
		V_{in} = 1 Vp-p, R Counter set to divide ratio such that f_R ≤ 1 MHz, REF Counter set to divide ratio such that REF_{out} ≤ 5 MHz	8			MHz
		V_{DD} = 2.7 V		1	20	
		V_{DD} = 3.0 V		1.5	20	
		V_{DD} = 3.5 V		2	20	
		V_{DD} = 4.5 to 5 V		4.5	27	
f_{XTAL}	Crystal Frequency, Crystal Mode	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance; R Counter and REF Counter same as above	9	2	10	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 30 pF	10, 12	dc	5	MHz
f	Operating Frequency of the Phase Detectors			dc	1	MHz
t_W	Output Pulse Width (ϕ_R, ϕ_V, and LD)	f_R in Phase with f_V, C_L = 50 pF, V_{PD} = 2.7 V, V_{DD} = V_{CC} = 2.7 V	11, 12	20	140	ns
t_{TLH}, t_{THL}	Output Transition Times (LD, ϕ_V, and ϕ_R)	C_L = 50 pF, V_{PD} = 2.7 V, V_{DD} = V_{CC} = 2.7 V	11, 12	—	80	ns
C_{in}	Input Capacitance, REF_{in}			—	5	pF

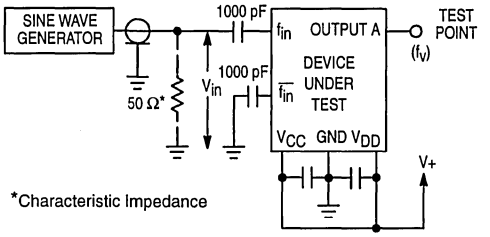


Figure 7. Test Circuit

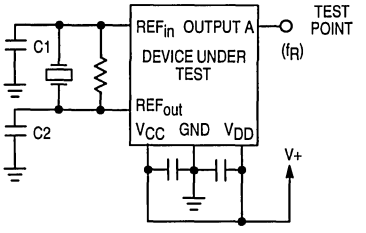


Figure 9. Test Circuit–Crystal Mode

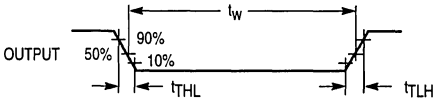


Figure 11. Switching Waveform

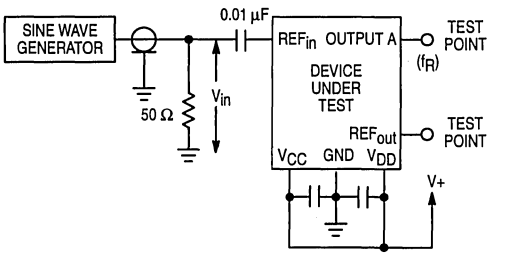


Figure 8. Test Circuit–Reference Mode

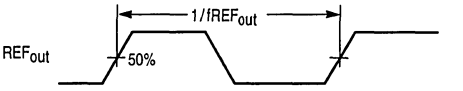


Figure 10. Switching Waveform

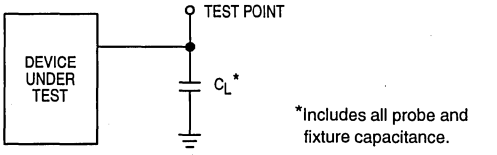


Figure 12. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 19)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low-to-high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 1). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

CAUTION

The value programmed for the N counter must be greater than or equal to the value of the A counter.

The 13 least significant bits (LSBs) of the R register are double-buffered. As indicated above, data is latched into the first buffer on a 16-bit transfer. (The 3 MSBs are not double-buffered and have an immediate effect after a 16-bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24-bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16-bit transfer may be followed by pulsing $\overline{ENB}$ low with no signal on the CLK pin. This is an alternate method of transferring data to the second buffer of the R register (see Figure 16).

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.7 to 5.0 V. The formats are shown in Figures 13, 15, and 16.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull-up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access
(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 22–25	

CLK

Serial Data Clock Input (Pin 18)

Low-to-high transitions on CLK shift bits available at the D_{in} pin, while high-to-low transitions shift bits from OUTPUT A (when configured as Data Out, see Pin 16). The 24-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty-four cycles are used to access the A register. See Table 1 and Figures 13, 15, and 16. The number of clocks required for cascaded devices is shown in Figures 23 through 25.

CLK typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

CAUTION

To guarantee proper operation of the Power-On Reset (POR) circuit, the CLK pin must ***not*** be floating or toggled during power up. It is prefereable to hold the CLK pin low during power up.

$\overline{ENB}$

Active Low Enable Input (Pin 17)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low-to-high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt-triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

CAUTION

$\overline{ENB}$ must not be floated or toggled during power up. It is preferable to hold $\overline{ENB}$ at the potential of the V_{DD} pin during power up to guarantee proper operation of the POR circuit.

OUTPUT A

Configurable Digital Output (Pin 16)

OUTPUT A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 15.

If A23 = A22 = high, OUTPUT A is configured as f_R. This signal is the buffered output of the 13-stage R counter. The f_R signal appears as normally low and pulses high. The f_R signal can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0–R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of 1 (see Figure 16). The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_R should not exceed 1 MHz.

If A23 = high and A22 = low, OUTPUT A is configured as f_V. This signal is the buffered output of the 12-stage N counter. The f_V signal appears as normally low and pulses high. The f_V signal can be used to verify the operation of the prescaler, A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 15. The maximum frequency at which the phase detectors operate is 1 MHz. Therefore, the frequency of f_V should not exceed 1 MHz.

If A23 = low and A22 = high, OUTPUT A is configured as Data Out. This signal is the serial output of the 24-1/2-stage shift register. The bit stream is shifted out on the high-to-low transition of the CLK input. Upon power up, OUTPUT A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, OUTPUT A is configured as Port. This signal is a general-purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

OUTPUT B

Open-Drain Digital Output (Pin 15)

This signal is a general-purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, OUTPUT B assumes the high-impedance state. OUTPUT B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. **Note:** the maximum voltage allowed on the V_{PD} pin is 5.5 V for the MC145192.

Upon power-up, power-on reset circuitry forces OUTPUT B to a low level.

REFERENCE PINS

REF_{in} and REF_{out}

Reference Input and Reference Output (Pins 20 and 1)

Configurable pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 16.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate values, as recommended by the crystal supplier, are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The device is designed to operate with crystals up to 10 MHz; the required connections are shown in Figure 9. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary, respectively). This is the active-crystal mode shown in Figure 16. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut-down crystal mode (shown in Figure 16) and can be engaged whether in standby or not.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 16 shows how to obtain ratios of eight, four, and two. A ratio of one-to-one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 5 MHz for V_{DD} to V_{SS} swing. Therefore, for REF_{in} frequencies above 5 MHz, the one-to-one ratio may not be used for large signal swing requirements. Likewise, for REF_{in} frequencies above 10 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in} and $\overline{f_{in}}$
Frequency Inputs (Pins 11 and 10)

These pins are frequency inputs from the VCO. These pins feed the on-board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they are usually used in a single-ended configuration (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out}
Single-Ended Phase/Frequency Detector Output (Pin 6)

This is a three-state current-source/sink output for use as a loop error signal when combined with an external low-pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 13)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current-sinking pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current-sourcing pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current-sourcing pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current-sinking pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high-impedance state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the high-impedance state when the device is put into standby (STBY bit C4 = high).

The PD_{out} circuit is powered by V_{PD}. The phase detector gain is controllable by bits C3, C2, and C1: gain (in amps per radian) = PD_{out} current divided by 2π.

ϕ_R and ϕ_V (Pins 3 and 4)
Double-Ended Phase/Frequency Detector Outputs

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 13)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
- Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD
Lock Detector Output (Pin 2)

This output is essentially at a high level with narrow low-going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V (see Figure 17).

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on-chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx
External Resistor (Pin 8)

A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Tables 2 and 3 for other current values. To achieve a maximum current of 2 mA, the resistor should be about 18 kΩ when V_{PD} is 5 V. See Figure 14 if lower maximum current values are desired.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

TEST POINT PINS

TEST 1
Modulus Control Signal (Pin 9)

This pin may be used in conjunction with the Test 2 pin for access to the on-board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin must be attached to an isolated pad with no trace. There is the possibility that the final production version of the device will have this lead clipped at the body of the package.

TEST 2
Prescaler Output (Pin 13)

This pin may be used to access to the on-board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and must be floated in an actual application. This pin must be attached to an isolated pad with no trace. There is the possibility that the final production version of the device will have this lead clipped at the body of the package.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply (Pin 14)

This pin supplies power to the main CMOS digital portion of the device. The voltage range is +2.7 to +5.0 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low-inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC}
Positive Power Supply (Pin 12)

This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is +2.7 to +5.0 V with respect to the GND pin. In standby mode, the V_{CC} pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 21.

For optimum performance, V_{CC} should be bypassed to GND using a low-inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

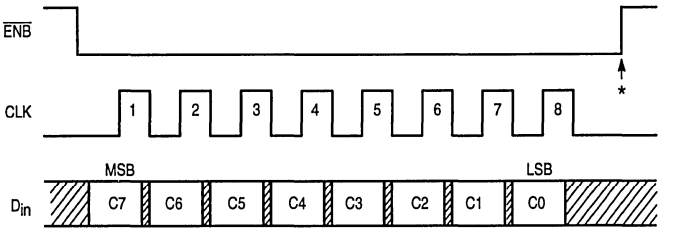
V_{PD}
Positive Power Supply (Pin 5)

This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin must be no less than the potential applied to the V_{DD} pin. The voltage range for V_{PD} is 4.5 to 5.5 V with respect to the GND pin when using PD_{OUT} and 2.7 to 5.5 V when using ϕ_R, ϕ_V outputs.

For optimum performance, V_{PD} should be bypassed to GND using a low-inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND
Ground (Pin 7)

Common ground.



*At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high-impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 — STBY: When set, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high-impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.

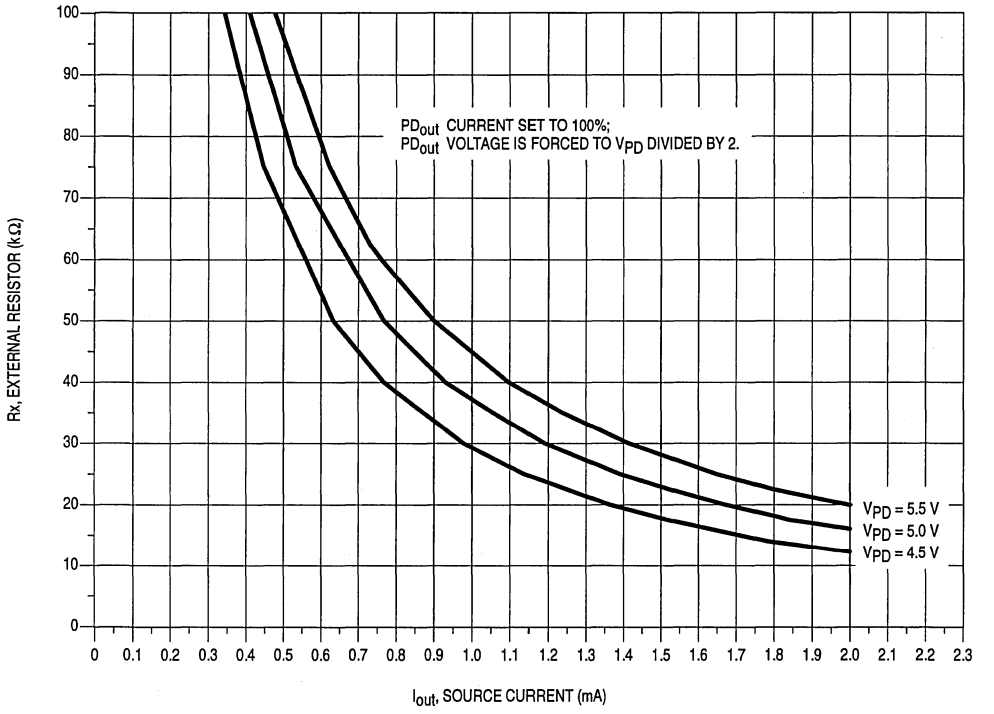
When C4 is reset low, the part is taken out of standby in 2 steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C3, C2 — I2, I1: Controls the PD_{out} source/sink current per Tables 2 and 3. With both bits high, the maximum current (as set by Rx per Figure 14) is available. Also, see C1 bit description.

C1 — Port: When the OUTPUT A pin is selected as "Port" via bits A22 and A23, C1 determines the state of OUTPUT A. When C1 is set high, OUTPUT A is forced high; C1 low forces OUTPUT A low. When OUTPUT A is ***not*** selected as "Port," C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 2 and 3.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when OUTPUT A is selected as "Port." The Port bit is not affected by the standby mode.

C0 — Out B: Determines the state of OUTPUT B. When C0 is set high, OUTPUT B is high-impedance; C0 low forces OUTPUT B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 13. C Register Access and Format (8 Clock Cycles are Used)



NOTE: The MC145192 is optimized for Rx values in the 18 kΩ to 40 kΩ range. For example, to achieve 0.3 mA of output current, it is preferable to use a 30-kΩ resistor for Rx and bit settings for 25% (as shown in Table 3).

Figure 14. Nominal Source Current for the PD_{out} Pin

Table 2. PD_{out} Current, C1 = Low with OUTPUT A *NOT* Selected as "Port"; Also, Default Mode When OUTPUT A Selected as "Port"

C3	C2	PD_{out} Current
0	0	70%
0	1	80%
1	0	90%
1	1	100%

Table 3. PD_{out} Current, C1 = High with OUTPUT A *NOT* Selected as "Port"

C3	C2	PD_{out} Current
0	0	25%
0	1	50%
1	0	75%
1	1	100%

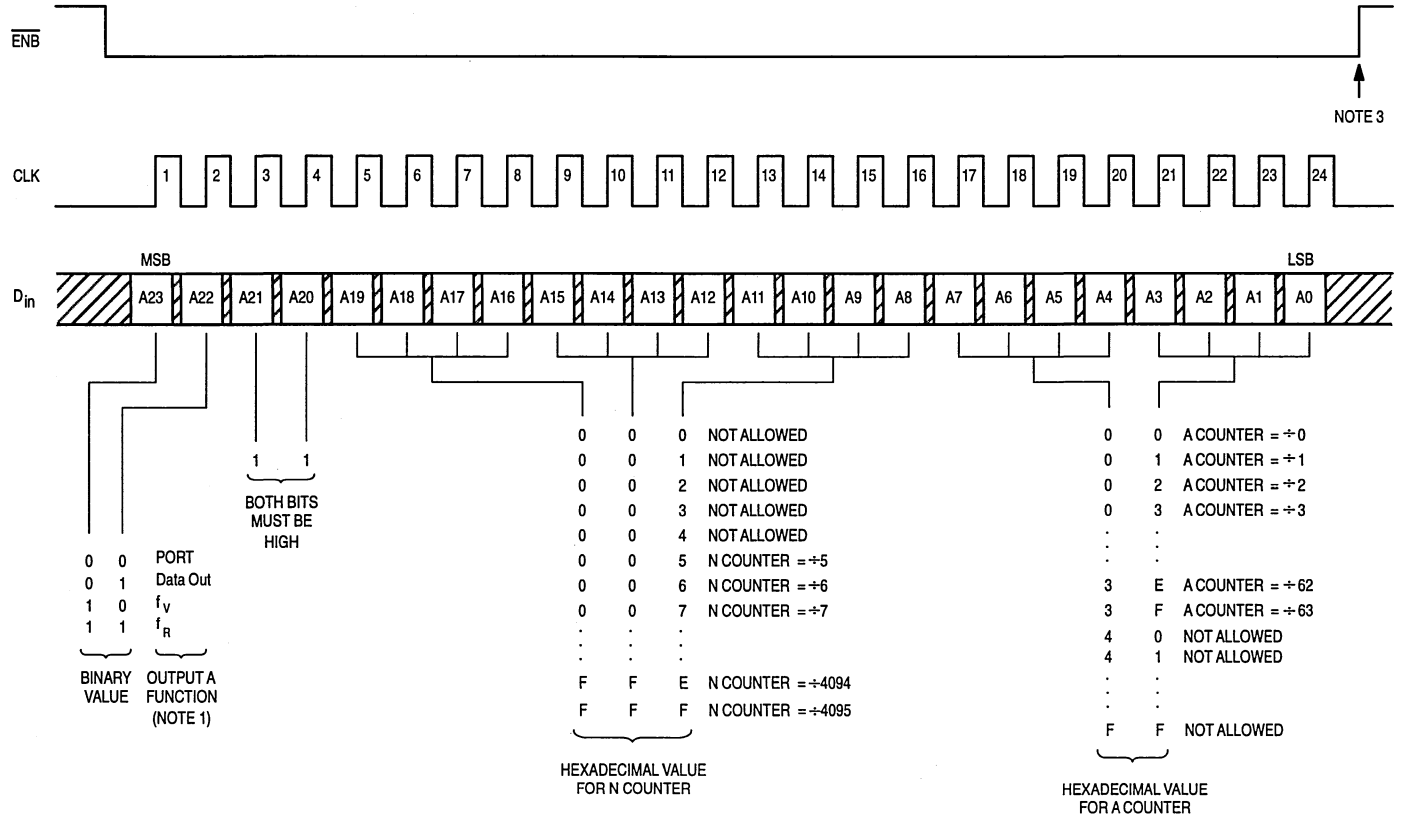
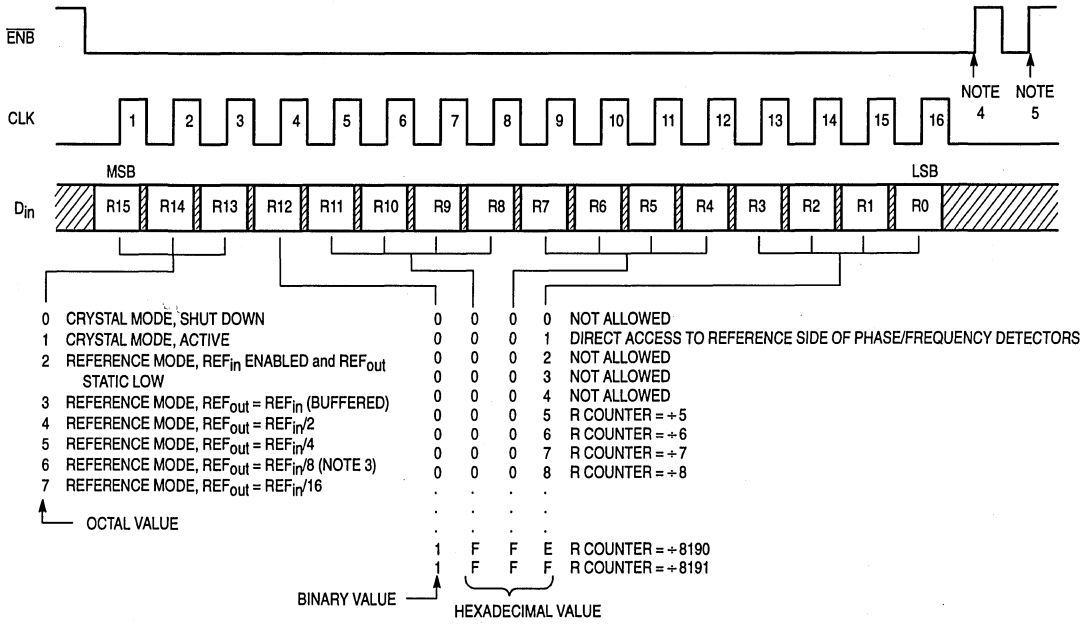


Figure 15. A Register Access and Format (24 Clock Cycles are Used)

Notes:

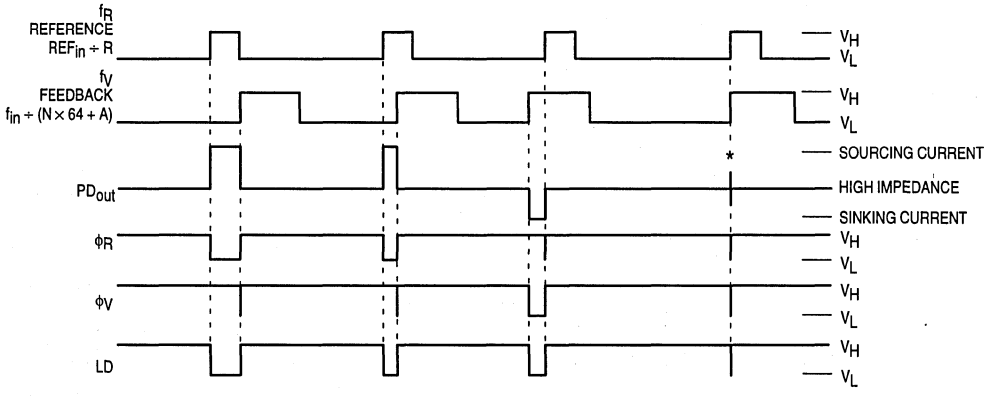
1. A power-on initialize circuit forces the OUTPUT A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.



NOTES:

1. Bits R15 through R13 control the configurable "OSC or 4-stage divider" block (see Block Diagram).
2. Bits R12 through R0 control the "13-stage R counter" block (see Block Diagram).
3. A power-on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4-Stage Divider" block in the Block Diagram. Bits R0–R12 are loaded into the first buffer in the double-buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. At this point, bits R0–R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note 3 of Figure 15 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

Figure 16. R Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
NOTE: The PD_{out} either sources or sinks current during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 13 for POL.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off-Chip Reference

The user may design an off-chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C_L) which does not exceed approximately 20 pF when used at the highest operating frequency of 10 MHz. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \bullet C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)

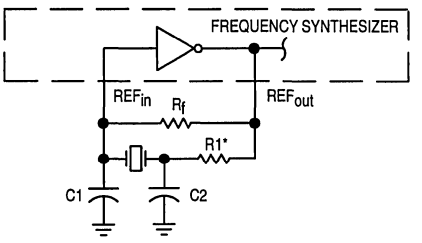
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at OUTPUT A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 4).



*May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

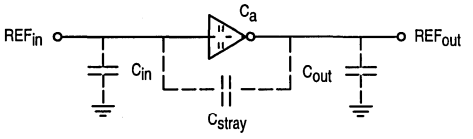
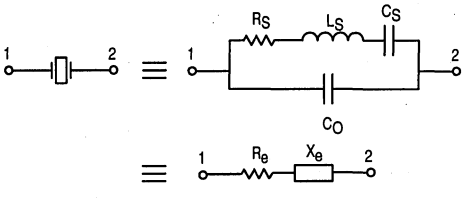


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}



Note: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design,* May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design,* March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design,* April 25, 1985.

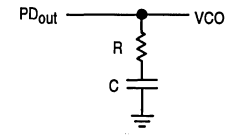
Table 4. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693-0099

Note: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE-LOCKED LOOP—LOW-PASS FILTER DESIGN

(A)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

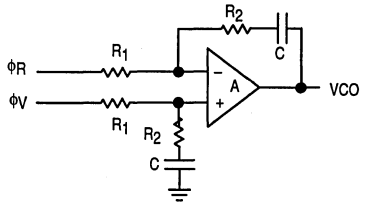
$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:

For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_c = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:

For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:

N = Total Division Ratio in Feedback Loop

K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}

K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R-related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R-related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley-Interscience, 1979.

Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley-Interscience, 1980.

Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York, Wiley-Interscience, 1976.

Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley-Interscience, 1981.

Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice-Hall, 1983.

Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.

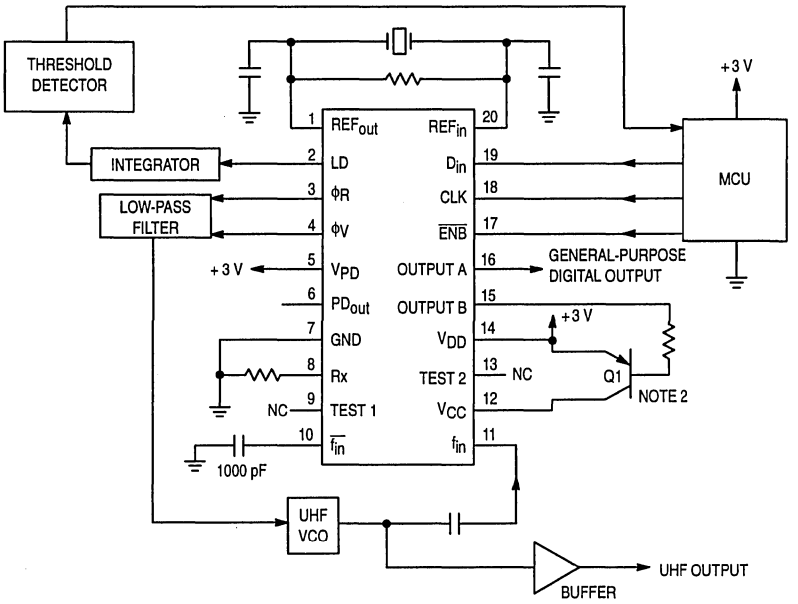
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.

Seidman, Arthur H., *Integrated Circuits Applications Handbook,* Chapter 17, pp. 538-586. New York, John Wiley & Sons.

Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.

AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.

AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop — Low-Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general-purpose digital pin, OUTPUT B. If the standby feature is not needed, tie pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low-inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 21. Example Application

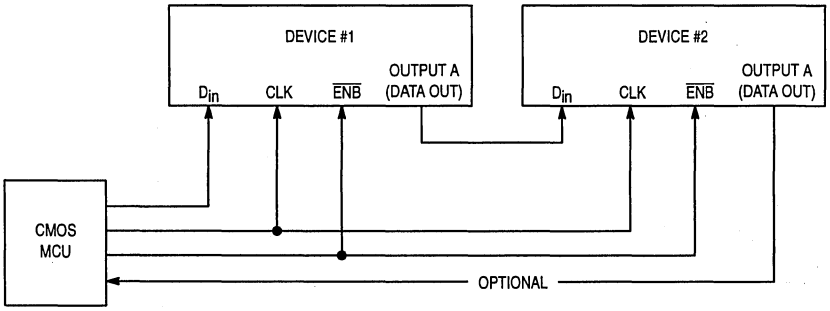
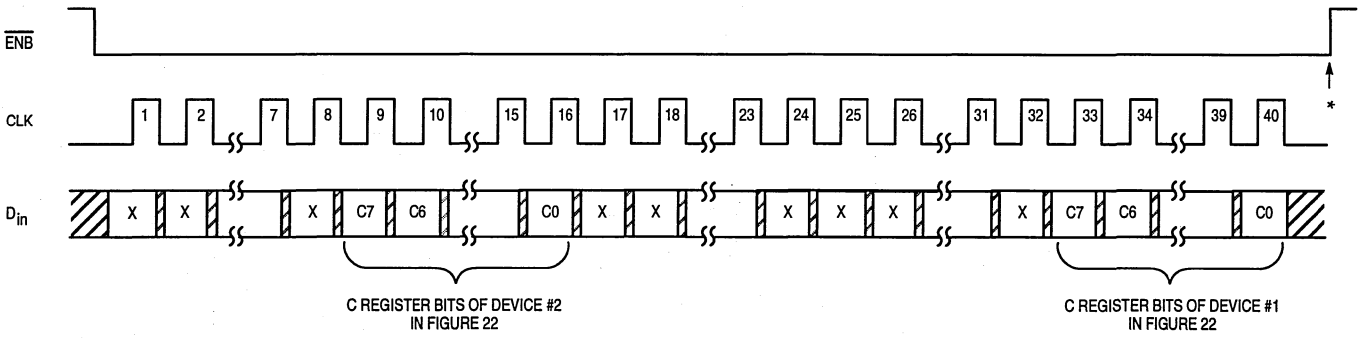
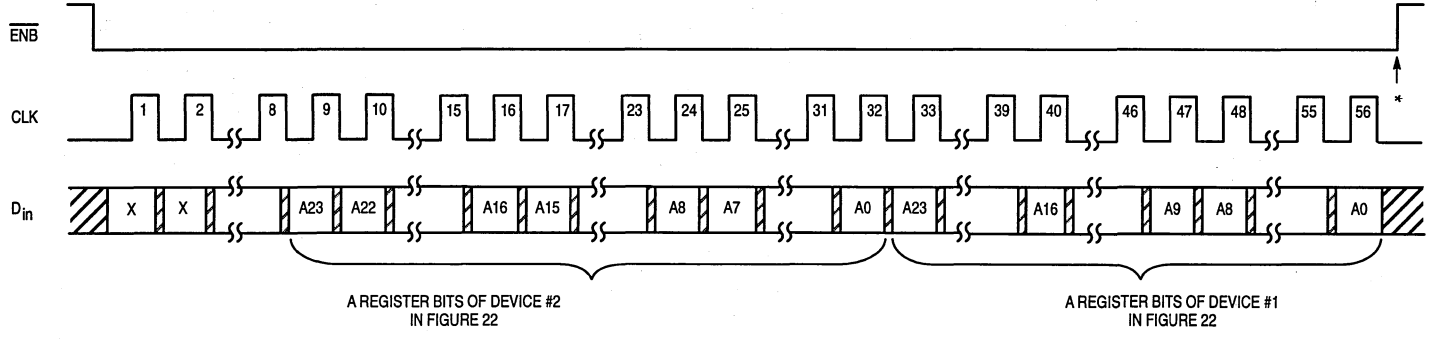


Figure 22. Cascading Two Devices



*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

Figure 23. Accessing the C Registers of Two Cascaded Devices



*At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

Figure 24. Accessing the A Registers of Two Cascaded Devices

Figure 25. Accessing the R Registers of Two Cascaded Devices

Notes Applicable To Each Device:

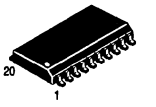
1. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4-Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double-buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. At this point, the bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note of Figure 24 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

MC145200
MC145201

Product Preview

2.0 GHz PLL Frequency Synthesizers

Include On-Board 64/65 Prescalers

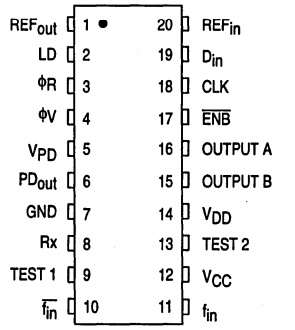


F SUFFIX
SOG PACKAGE
CASE 751J

ORDERING INFORMATION

MC145200F	SOG Package
MC145201F	SOG Package

PIN ASSIGNMENT



The MC145200 and MC145201 are single-package synthesizers with serial interfaces capable of direct usage up to 2.0 GHz. A special architecture makes these PLLs very easy to program because a byte-oriented format is utilized. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 3-byte serial transfer to the 24-bit A register. The interface is both SPI and MICROWIRE™ compatible.

Each device features a single-ended current source/sink phase detector output and a double-ended phase detector output. Both phase detectors have linear transfer functions (no dead zones). The maximum current of the single-ended phase detector output is determined by an external resistor tied from the Rx pin to ground. This current can be varied via the serial port.

The MC145200 features logic-level converters and high-voltage phase/frequency detectors; the detector supply may range up to 9.5 V. The MC145201 has lower-voltage phase/frequency detectors optimized for single-supply systems of 5 V ±10%.

Each part includes a differential RF input which may be operated in a single-ended mode. Also featured are on-board support of an external crystal and a programmable reference output. The R, A, and N counters are fully programmable. The C register (configuration register) allows the parts to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing system noise and interference.

In order to have consistent lock times and prevent erroneous data from being loaded into the counters, on-board circuitry synchronizes the update of the A register if the A or N counters are loading. Similarly, an update of the R register is synchronized if the R counter is loading.

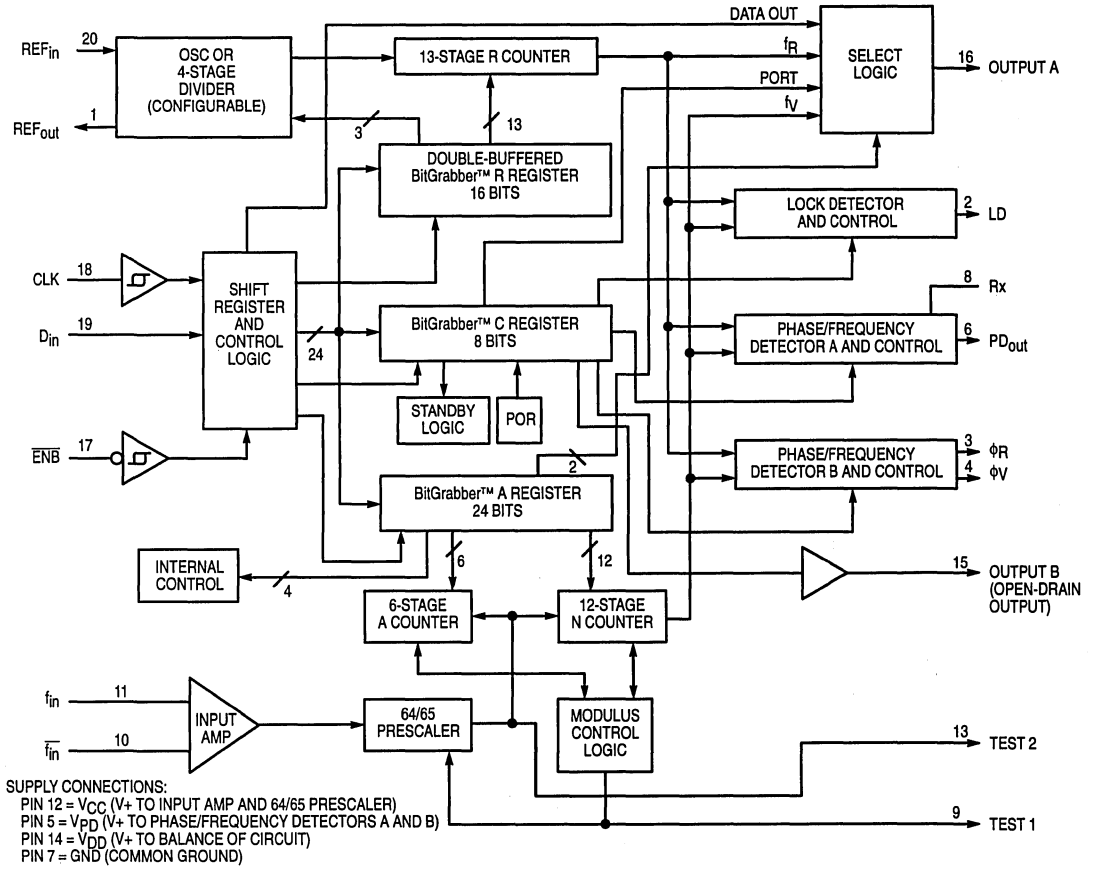
The double-buffered R register allows new divide ratios to be presented to the three counters (R, A, and N) simultaneously.

- Maximum Operating Frequency: 2000 MHz @ V_{in} = 200 mVp-p
- Operating Supply Current: 12 mA Nominal
- Operating Supply Voltage Range (V_{DD} and V_{CC} Pins): 4.5 to 5.5 V
- Operating Supply Voltage Range of Phase Detectors (V_{PD} Pin) —
  MC145200: 8.0 to 9.5 V
  MC145201: 4.5 to 5.5 V
- Current Source/Sink Phase Detector Output Capability: 2 mA Maximum
- Gain of Current Source/Sink Phase/Frequency Detector Controllable via Serial Port
- Operating Temperature Range: – 40 to +85°C
- R Counter Division Range: 5 to 8191 plus Direct Access to Phase Detector Input
- Dual-Modulus Capability Provides Total Division up to 262,143
- High-Speed Serial Interface: 4 Mbps
- OUTPUT A Pin, When Configured as Data Out, Permits Cascading of Devices
- Two General-Purpose Digital Outputs — OUTPUT A: Totem-Pole (Push-Pull)
  OUTPUT B: Open-Drain
- Power-Saving Standby Feature with Orderly Recovery for Minimizing Lock Times, Standby Current: 50 μA

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.
BitGrabber is a trademark of Motorola, Inc. MICROWIRE is a trademark of National Semiconductor Corp.

REV. 1

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to GND, unless otherwise stated)

Symbol	Parameter	Value	Unit
V_{CC}, V_{DD}	DC Supply Voltage (Pins 12 and 14)	−0.5 to +6.0	V
V_{PD}	DC Supply Voltage (Pin 5) MC145200 MC145201	V_{DD} −0.5 to +9.5 V_{DD} −0.5 to +6.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (except OUTPUT B, PD_{out}, ϕR, ϕV)	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage (OUTPUT B, PD_{out}, ϕR, ϕV)	−0.5 to V_{PD} +0.5	V
I_{in}, I_{PD}	DC Input Current, per Pin (Includes V_{PD})	±10	mA
I_{out}	DC Output Current, per Pin	±20	mA
I_{DD}	DC Supply Current, V_{DD} and GND Pins	±30	mA
P_D	Power Dissipation, per Package	300	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 seconds	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = 4.5 to 5.5 V, Voltages Referenced to GND, T_A = −40 to +85°C, unless otherwise stated;
MC145200: V_{PD} = 8.0 to 9.5 V; MC145201: V_{PD} = 4.5 to 5.5 V with $V_{DD} \leq V_{PD}$.

Symbol	Parameter	Test Condition	Guaranteed Limit	Unit
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode	0.3 × V_{DD}	V
V_{IH}	Minimum High-Level Input Voltage (D_{in}, CLK, $\overline{ENB}$, REF_{in})	Device in Reference Mode	0.7 × V_{DD}	V
V_{hys}	Minimum Hysteresis Voltage (CLK, $\overline{ENB}$)		300	mV
V_{OL}	Maximum Low-Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = 20 µA, Device in Reference Mode	0.1	V
V_{OH}	Minimum High-Level Output Voltage (REF_{out}, OUTPUT A)	I_{out} = −20 µA, Device in Reference Mode	V_{DD} − 0.1	V
I_{OL}	Minimum Low-Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = 0.4 V	0.36	mA
I_{OH}	Minimum High-Level Output Current (REF_{out}, LD, ϕ_R, ϕ_V)	V_{out} = V_{DD} − 0.4 V for REF_{out}, LD V_{out} = V_{PD} − 0.4 V for ϕ_R, ϕ_V	−0.36	mA
I_{OL}	Minimum Low-Level Output Current (OUTPUT A, OUTPUT B)	V_{out} = 0.4 V	1.0	mA
I_{OH}	Minimum High-Level Output Current (OUTPUT A Only)	V_{out} = V_{DD} − 0.4 V	− 0.6	mA
I_{in}	Maximum Input Leakage Current (D_{in}, CLK, $\overline{ENB}$, REF_{in})	V_{in} = V_{DD} or GND, Device in XTAL Mode	± 1.0	µA
I_{in}	Maximum Input Current (REF_{in})	V_{in} = V_{DD} or GND, Device in Reference Mode	± 100	µA
I_{OZ}	Maximum Output Leakage Current (PD_{out})	V_{out} = V_{PD} − 0.5 or 0.5 V, Output in High-Impedance State — MC145200	± 150	nA
		MC145201	± 200	
I_{OZ}	Maximum Output Leakage Current (OUTPUT B)	V_{out} = V_{PD} or GND, Output in High-Impedance State	± 10	µA
I_{STBY}	Maximum Standby Supply Current (V_{DD} + V_{PD} Pins)	V_{in} = V_{DD} or GND; Outputs Open; Device in Standby Mode, Shut-Down Crystal Mode or REF_{out}-Static-Low Reference Mode; OUTPUT B Controlling V_{CC} per Figure 21	50*	µA
I_{PD}	Maximum Phase Detector Quiescent Current (V_{PD} Pin)	Bit C6 = High Which Selects Phase Detector A, PD_{out} = Open, PD_{out} = Static Low or High, Bit C4 = Low Which is ***not*** Standby, I_{Rx} = 113 µA	600*	µA
		Bit C6 = Low Which Selects Phase Detector B, ϕ_R and ϕ_V = Open, ϕ_R and ϕ_V = Static Low or High, Bit C4 = Low Which is ***not*** Standby	30*	
I_T	Total Operating Supply Current (V_{DD} + V_{PD} + V_{CC} Pins)	f_{in} = 2.0 GHz; REF_{in} = 13 MHz @ 1 Vp-p; OUTPUT A = Inactive and No Connect; REF_{out}, ϕ_V, ϕ_R, PD_{out}, LD = No Connect; D_{in}, $\overline{ENB}$, CLK = V_{DD} or GND, Phase Detector B Enabled (Bit C6 = Low)	**	mA

*MC145201 ONLY.

**The nominal value = 12 mA. This is not a guaranteed limit.

ANALOG CHARACTERISTICS—CURRENT SOURCE/SINK OUTPUT—PD_{out}
($I_{out} \leq 2$ mA, $V_{DD} = V_{CC} = 4.5$ to 5.5 V, $V_{DD} \leq V_{PD}$. Voltages Referenced to GND)

Parameter	Test Condition	V_{PD}	Guaranteed Limit	Unit
Maximum Source Current Variation	MC145200: $V_{out} = 0.5 \times V_{PD}$	8.0	±20	%
		9.5	±20	
	MC145201: $V_{out} = 0.5 \times V_{PD}$	4.5	±20	%
		5.5	±20	
Maximum Sink-vs-Source Mismatch (Note 3)	MC145200: $V_{out} = 0.5 \times V_{PD}$	8.0	12	%
		9.5	12	
	MC145201: $V_{out} = 0.5 \times V_{PD}$	4.5	12	%
		5.5	12	
Output Voltage Range (Note 3)	MC145200: I_{out} variation ≤ 20%	8.0	0.5 to 7.5	V
		9.5	0.5 to 9.0	
	MC145201: I_{out} variation ≤ 20%	4.5	0.5 to 4.0	V
		5.5	0.5 to 5.0	

NOTES:
1. Percentages calculated using the following formula: (Maximum Value – Minimum Value)/Maximum Value.
2. See Rx Pin Description for external resistor values.
3. This parameter is guaranteed for a given temperature within –40 to +85°C.

AC INTERFACE CHARACTERISTICS ($V_{DD} = 4.5$ to 5.5 V, $T_A = -40$ to +85°C, $C_L = 50$ pF, Input $t_r = t_f = 10$ ns; MC145200: $V_{PD} = 8.0$ to 9.5 V; MC145201: $V_{PD} = 4.5$ to 5.5 V with $V_{DD} \leq V_{PD}$)

Symbol	Parameter	Figure #(s)	Guaranteed Limit	Unit
f_{clk}	Serial Data Clock Frequency (Note: Refer to Clock t_w below)	1	dc to 4.0	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, CLK to OUTPUT A (Selected as Data Out)	1, 5	105	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT A (Selected as Port)	2, 5	100	ns
t_{PZL}, t_{PLZ}	Maximum Propagation Delay, $\overline{ENB}$ to OUTPUT B	2, 6	120	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, OUTPUT A and OUTPUT B; t_{THL} only, on OUTPUT B	1, 5, 6	100	ns
C_{in}	Maximum Input Capacitance – D_{in}, $\overline{ENB}$, CLK,		10	pF

TIMING REQUIREMENTS
($V_{DD} = 4.5$ to 5.5 V, $T_A = -40$ to +85°C, Input $t_r = t_f = 10$ ns unless otherwise indicated)

Symbol	Parameter	Figure #(s)	Guaranteed Limit	Unit
t_{su}, t_h	Minimum Setup and Hold Times, D_{in} vs CLK	3	20	ns
t_{su}, t_h, t_{rec}	Minimum Setup, Hold and Recovery Times, $\overline{ENB}$ vs CLK	4	100	ns
t_w	Minimum Pulse Width, $\overline{ENB}$	4	*	cycles
t_w	Minimum Pulse Width, CLK	1	125	ns
t_r, t_f	Maximum Input Rise and Fall Times, CLK	1	100	µs

*The minimum limit is 3 REF_{in} cycles or 195 f_{in} cycles, whichever is greater.

SWITCHING WAVEFORMS

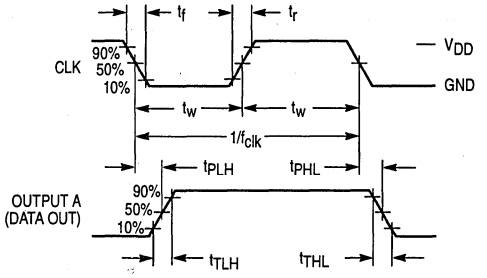


Figure 1.

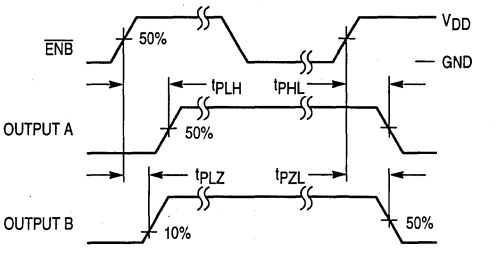


Figure 2.

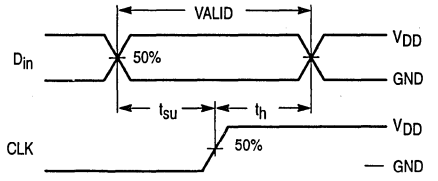


Figure 3.

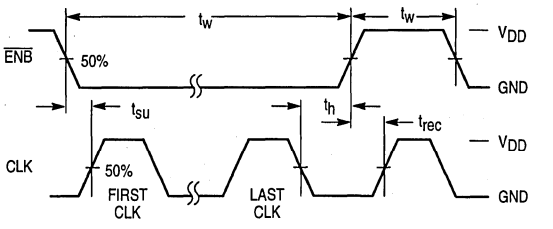
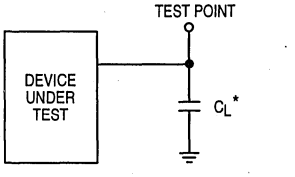
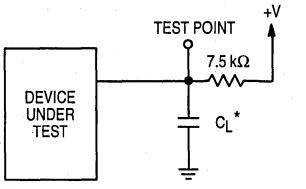


Figure 4.



*Includes all probe and fixture capacitance.

Figure 5. Test Circuit



*Includes all probe and fixture capacitance.

Figure 6. Test Circuit

LOOP SPECIFICATIONS (V_{DD} = V_{CC} = 4.5 to 5.5 V unless otherwise indicated, T_A = −40 to +85°C)

Symbol	Parameter	Test Condition	Fig #	Guaranteed Operating Range		Unit
				Min	Max	
V_{in}	Input Voltage Range, f_{in}	500 MHz ≤ f_{in} ≤ 2000 MHz	7	200	1500	mVp-p
f_{ref}	Input Frequency, REF_{in} Externally Driven in Reference Mode	V_{in} = 400 mVp-p V_{in} = 1 Vp-p R Counter set to divide ratio such that f_R ≤ 2 MHz, REF Counter set to divide ratio such that REF_{out} ≤ 10 MHz	8	12 4.5*	27 27	MHz
f_{XTAL}	Crystal Frequency, Crystal Mode	C1 ≤ 30 pF, C2 ≤ 30 pF, Includes Stray Capacitance; R Counter and REF Counter same as above	9	2	15	MHz
f_{out}	Output Frequency, REF_{out}	C_L = 30 pF	10, 12	dc	10	MHz
f	Operating Frequency of the Phase Detectors			dc	2	MHz
t_W	Output Pulse Width, LD, ϕ_R, and ϕ_V, — MC145201	f_R in Phase with f_V, C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	20	100	ns
t_{TLH}, t_{THL}	Output Transition Times, LD, ϕ_V, and ϕ_R — MC145201	C_L = 50 pF, V_{PD} = 5.5 V, V_{DD} = V_{CC} = 5.0 V	11, 12	—	65	ns
C_{in}	Input Capacitance f_{in} REF_{in}			— —	TBD 5	pF

*If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal.

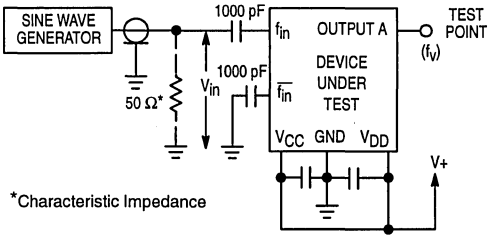


Figure 7. Test Circuit

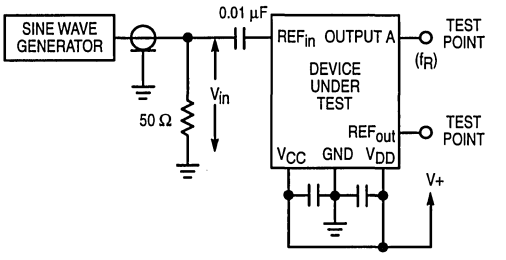


Figure 8. Test Circuit–Reference Mode

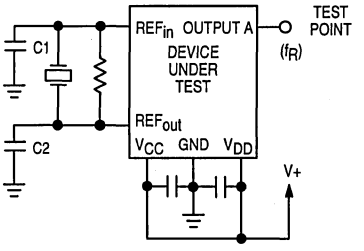


Figure 9. Test Circuit–Crystal Mode

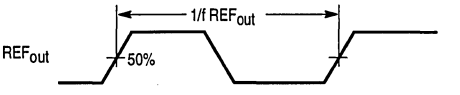


Figure 10. Switching Waveform

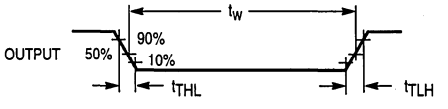


Figure 11. Switching Waveform

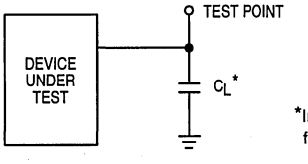


Figure 12. Test Circuit

PIN DESCRIPTIONS

DIGITAL INTERFACE PINS

D_{in}
Serial Data Input (Pin 19)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low-to-high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the first buffer of the R register, or 3 bytes (24 bits) to access the A register (see Table 1). The values in the C, R, and A registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{ENB}$.

CAUTION

The value programmed for the N-counter must be greater than or equal to the value of the A-counter.

The 13 least significant bits (LSBs) of the R register are double-buffered. As indicated above, data is latched into the first buffer on a 16-bit transfer. (The 3 MSBs are not double-buffered and have an immediate effect after a 16-bit transfer.) The second buffer of the R register contains the 13 bits for the R counter. This second buffer is loaded with the contents of the first buffer when the A register is loaded (a 24-bit transfer). This allows presenting new values to the R, A, and N counters simultaneously. If this is not required, then the 16-bit transfer may be followed by pulsing $\overline{ENB}$ low with no signal on the CLK pin. This is an alternate method of transferring data to the second buffer of the R register (see Figure 16).

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 4.5 to 5.5 V. The formats are shown in Figures 13, 15, and 16.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull-up resistor of 1 kΩ to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 1. Register Access
(MSBs are shifted in first; C0, R0, and A0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
8	C Register	C7, C6, C5, . . ., C0
16	R Register	R15, R14, R13, . . ., R0
24	A Register	A23, A22, A21, . . ., A0
Other Values ≤ 32	Not Allowed	
Values > 32	See Figures 22–25	

CLK
Serial Data Clock Input (Pin 18)

Low-to-high transitions on CLK shift bits available at the D_{in} pin, while high-to-low transitions shift bits from OUTPUT A (when configured as Data Out, see Pin 16). The 24-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the first buffer of the R register. Twenty-four cycles are used to access the A register. See Table 1 and Figures 13, 15, and 16. The number of clocks required for cascaded devices is shown in Figures 23 through 25.

CLK typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of **D_{in}** for more information.

CAUTION

To guarantee proper operation of the Power-On Reset (POR) circuit, the CLK pin must be grounded or held low during power up.

$\overline{ENB}$
Active Low Enable Input (Pin 17)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{ENB}$ is in an inactive high state, shifting is inhibited and the port is held in the initialized state. To transfer data to the device, $\overline{ENB}$ (which must start inactive high) is taken low, a serial transfer is made via D_{in} and CLK, and $\overline{ENB}$ is taken back high. The low-to-high transition on $\overline{ENB}$ transfers data to the C or A registers and first buffer of the R register, depending on the data stream length per Table 1.

Transitions on $\overline{ENB}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{ENB}$ is high and CLK is low.

This input is also Schmitt-triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of **D_{in}** for more information.

CAUTION

$\overline{ENB}$ must not be floated or toggled during power up. It is preferable to hold $\overline{ENB}$ at the potential of the V_{DD} pin during power up to guarantee proper operation of the POR circuit.

OUTPUT A
Configurable Digital Output (Pin 16)

OUTPUT A is selectable as f_R, f_V, Data Out, or Port. Bits A22 and A23 in the A register control the selection; see Figure 15.

If A23 = A22 = high, OUTPUT A is configured as f_R. This signal is the buffered output of the 13-stage R counter. The f_R signal appears as normally low and pulses high, and can be used to verify the divide ratio of the R counter. This ratio extends from 5 to 8191 and is determined by the binary value loaded into bits R0 through R12 in the R register. Also, direct access to the phase detectors via the REF_{in} pin is allowed by choosing a divide value of 1 (see Figure 16). The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R should not exceed 2 MHz.

If A23 = high and A22 = low, OUTPUT A is configured as f_V. This signal is the buffered output of the 12-stage N counter. The f_V signal appears as normally low and pulses high, and can be used to verify the operation of the prescaler, A counter, and N counter. The divide ratio between the f_{in} input and the f_V signal is $N \times 64 + A$. N is the divide ratio of the N counter and A is the divide ratio of the A counter. These ratios are determined by bits loaded into the A register. See Figure 15.

The maximum frequency at which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V should not exceed 2 MHz.

If A23 = low and A22 = high, OUTPUT A is configured as Data Out. This signal is the serial output of the 24-1/2-stage shift register. The bit stream is shifted out on the high-to-low transition of the CLK input. Upon power up, OUTPUT A is automatically configured as Data Out to facilitate cascading devices.

If A23 = A22 = low, OUTPUT A is configured as Port. This signal is a general-purpose digital output which may be used as an MCU port expander. This signal is low when the Port bit (C1) of the C register is low, and high when the Port bit is high.

OUTPUT B
Open-Drain Digital Output (Pin 15)

This signal is a general-purpose digital output which may be used as an MCU port expander. This signal is low when the Out B bit (C0) of the C register is low. When the Out B bit is high, OUTPUT B assumes the high-impedance state. OUTPUT B may be pulled up through an external resistor or active circuitry to any voltage less than or equal to the potential of the V_{PD} pin. **Note**: the maximum voltage allowed on the V_{PD} pin is 9.5 V for the MC145200 and 5.5 V for the MC145201.

Upon power-up, power-on reset circuitry forces OUTPUT B to a low level.

REFERENCE PINS

REF_{in} and REF_{out}
Reference Input and Reference Output (Pins 20 and 1)

Configurable pins for a Crystal or an External Reference. This pair of pins can be configured in one of two modes: the crystal mode or the reference mode. Bits R13, R14, and R15 in the R register control the modes as shown in Figure 16.

In crystal mode, these pins form a reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate values as recommended by the crystal supplier are connected from each of the two pins to ground (up to a maximum of 30 pF each, including stray capacitance). An external resistor of 1 MΩ to 15 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The device is designed to operate with crystals up to 15 MHz; the required connections are shown in Figure 8. To turn on the oscillator, bits R15, R14, and R13 must have an octal value of one (001 in binary, respectively). This is the active-crystal mode shown in Figure 16. In this mode, the crystal oscillator runs and the R Counter divides the crystal frequency, unless the part is in standby. If the part is placed in standby via the C register, the oscillator runs, but the R counter is stopped. However, if bits R15 to R13 have a value of 0, the oscillator is stopped, which saves additional power. This is the shut-down crystal mode (shown in Figure 16) and can be engaged whether in standby or not.

In the reference mode, REF_{in} (Pin 20) accepts a signal up to 27 MHz from an external reference oscillator, such as a TCXO. A signal swinging from at least the V_{IL} to V_{IH} levels listed in the Electrical Characteristics table may be directly coupled to the pin. If the signal is less than this level, ac coupling must be used as shown in Figure 8. Due to an on-board resistor which is engaged in the reference modes, an external biasing resistor tied between REF_{in} and REF_{out} is not required.

With the reference mode, the REF_{out} pin is configured as the output of a divider. As an example, if bits R15, R14, and R13 have an octal value of seven, the frequency at REF_{out} is the REF_{in} frequency divided by 16. In addition, Figure 16 shows how to obtain ratios of eight, four, and two. A ratio of one-to-one can be obtained with an octal value of three. Upon power up, a ratio of eight is automatically initialized. The maximum frequency capability of the REF_{out} pin is 10 MHz. Therefore, for REF_{in} frequencies above 10 MHz, the one-to-one ratio may not be used. Likewise, for REF_{in} frequencies above 20 MHz, the ratio must be more than two.

If REF_{out} is unused, an octal value of two should be used for R15, R14, and R13 and the REF_{out} pin should be floated. A value of two allows REF_{in} to be functional while disabling REF_{out}, which minimizes dynamic power consumption and electromagnetic interference (EMI).

LOOP PINS

f_{in} and $\overline{f_{in}}$
Frequency Inputs (Pins 11 and 10)

These pins are frequency inputs from the VCO. These pins feed the on-board RF amplifier which drives the 64/65 prescaler. These inputs may be fed differentially. However, they usually are used in a single-ended configuration (shown in Figure 7). Note that f_{in} is driven while $\overline{f_{in}}$ must be tied to ground via a capacitor.

Motorola does not recommend driving $\overline{f_{in}}$ while terminating f_{in} because this configuration is not tested for sensitivity. The sensitivity is dependent on the frequency as shown in the Loop Specifications table.

PD_{out}
Single-Ended Phase/Freq. Detector Output (Pin 6)

This is a three-state current-source/sink output for use as a loop error signal when combined with an external low-pass filter. The phase/frequency detector is characterized by a linear transfer function. The operation of the phase/ frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 13)
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current-sinking pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current-sourcing pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

POL bit (C7) = high
- Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: current-sourcing pulses from high impedance
- Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: current-sinking pulses from high impedance
- Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high-impedance state by utilization of the disable feature in the C register (bit C6). This is a patented feature. Similarly, PD_{out} is forced to the high-impedance state when the device is put into standby (STBY bit C4 = high).

ϕ_R and ϕ_V (Pins 3 and 4)
Double-Ended Phase/Frequency Detector Outputs

These outputs can be combined externally to generate a loop error signal. Through use of a Motorola patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 17.

POL bit (C7) in the C register = low (see Figure 13)
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase
POL bit (C7) = high
Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high
Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses
Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via C register bits C6 or C4. This is a patented feature. Note that when disabled or in standby, ϕ_R and ϕ_V are forced to their rest condition (high state).

The ϕ_R and ϕ_V output signal swing is approximately from GND to V_{PD}.

LD
Lock Detector Output (Pin 2)

This output is essentially at a high level with narrow low-going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies. LD is the logical ANDing of ϕ_R and ϕ_V (see Figure 17).

This output can be enabled and disabled via the C register. This is a patented feature. Upon power up, on-chip initialization circuitry disables LD to a static low logic level to prevent a false "lock" signal. If unused, LD should be disabled and left open.

The LD output signal swing is approximately from GND to V_{DD}.

Rx
External Resistor (Pin 8)

A resistor tied between this pin and GND, in conjunction with bits in the C register, determines the amount of current that the PD_{out} pin sinks and sources. When bits C2 and C3 are both set high, the maximum current is obtained at PD_{out}; see Tables 2 and 3 for other values of current. To achieve a maximum current of 2 mA, the resistor should be about 47 kΩ when V_{PD} is 9 V or about 18 kΩ when V_{PD} is 5.0 V. See Figure 14 if lower maximum current values are desired.

When the ϕ_R and ϕ_V outputs are used, the Rx pin may be floated.

TEST POINT PINS

TEST 1
Modulus Control Signal (Pin 9)

This pin may be used in conjunction with the Test 2 pin for access to the on-board 64/65 prescaler. When Test 1 is low, the prescaler divides by 65. When high, the prescaler divides by 64.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace. There is the possibility that the final production version of the device will have this lead clipped at the body of the package.

TEST 2
Prescaler Output (Pin 13)

This pin may be used to access to the on-board 64/65 prescaler output.

CAUTION

This pin is an unbuffered output and ***must*** be floated in an actual application. This pin must be attached to an isolated pad with no trace. There is the possibility that the final production version of the device will have this lead clipped at the body of the package.

POWER SUPPLY PINS

V_{DD}
Positive Power Supply (Pin 14)

This pin supplies power to the main CMOS digital portion of the device. The voltage range is + 4.5 to + 5.5 V with respect to the GND pin.

For optimum performance, V_{DD} should be bypassed to GND using a low-inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

V_{CC}
Positive Power Supply (Pin 12)

This pin supplies power to the RF amp and 64/65 prescaler. The voltage range is +4.5 to +5.5 V with respect to the GND pin. In the standby mode, the V_{CC} pin still draws a few milliamps from the power supply. This current drain can be eliminated with the use of transistor Q1 as shown in Figure 21.

For optimum performance, V_{CC} should be bypassed to GND using a low-inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

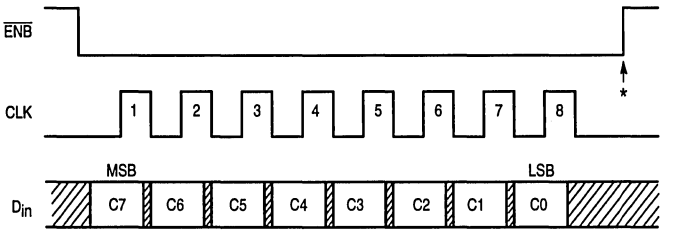
V_{PD}
Positive Power Supply (Pin 5)

This pin supplies power to both phase/frequency detectors A and B. The voltage applied on this pin must be no less than the potential applied to the V_{DD} pin. The maximum voltage can be +9.5 V with respect to the GND pin for the MC145200 and +5.5 V for the MC145201.

For optimum performance, V_{PD} should be bypassed to GND using a low-inductance capacitor mounted very close to these pins. Lead lengths on the capacitor should be minimized.

GND
Ground (Pin 7)

Common ground.



*At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 — POL: Selects the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 17. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 — PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high-impedance state. This bit is cleared low at power up.

C5 — LDE: Enables the lock detector output (LD) when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 — STBY: When set, places the CMOS section of device, which is powered by the V_{DD} and V_{PD} pins, in the standby mode for reduced power consumption: PD_{out} is forced to the high-impedance state, ϕ_R and ϕ_V are forced high, the A, N, and R counters are inhibited from counting, and the Rx current is shut off. In standby, the state of LD is determined by bit C5. C5 low forces LD low (no change). C5 high forces LD static high. During standby, data is retained in the A, R, and C registers. The condition of REF/OSC circuitry is determined by the control bits in the R register: R13, R14, and R15. However, if REF_{out} = static low is selected, the internal feedback resistor is disconnected and the input is inhibited when in standby; in addition, the REF_{in} input only presents a capacitive load. NOTE: Standby does not affect the other modes of the REF/OSC circuitry.

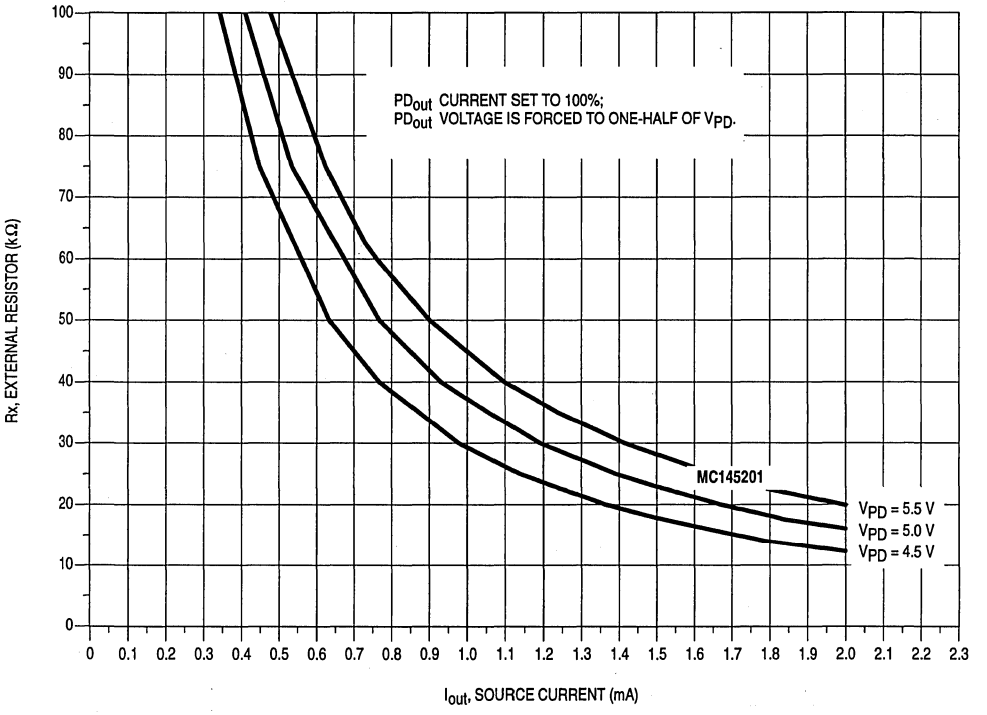
When C4 is reset low, the part is taken out of standby in 2 steps. First, the REF_{in} (only in one mode) resistor is reconnected, all counters are enabled, and the Rx current is enabled. Any f_R and f_V signals are inhibited from toggling the phase/frequency detectors and lock detector. Second, when the first f_V pulse occurs, the R counter is jam loaded, and the phase/frequency and lock detectors are initialized. Immediately after the jam load, the A, N, and R counters begin counting down together. At this point, the f_R and f_V pulses are enabled to the phase and lock detectors. (Patented feature.)

C3, C2 — I2, I1: Controls the PD_{out} source/sink current per Tables 2 and 3. With both bits high, the maximum current (as set by Rx per Figure 14) is available. Also, see C1 bit description.

C1 — Port: When the OUTPUT A pin is selected as "Port" via bits A22 and A23, C1 determines the state of OUTPUT A. When C1 is set high, OUTPUT A is forced high; C1 low forces OUTPUT A low. When OUTPUT A is NOT selected as "Port," C1 controls whether the PD_{out} step size is 10% or 25%. (See Tables 2 and 3.) When low, steps are 10%. When high, steps are 25%. Default is 10% steps when OUTPUT A is selected as "Port." The Port bit is not affected by the standby mode.

C0 — Out B: Determines the state of OUTPUT B. When C0 is set high, OUTPUT B is high-impedance; C0 low forces OUTPUT B low. The Out B bit is not affected by the standby mode. This bit is cleared low at power up.

Figure 13. C Register Access and Format (8 Clock Cycles are Used)



NOTE: The MC145201 is optimized for Rx values in the 18 kΩ to 40 kΩ range. For example, to achieve 0.3 mA of output current, it is preferable to use a 30-kΩ resistor for Rx and bit settings for 25% (as shown in Table 3).

Figure 14. Nominal Source Current for the PD_{out} Pin

Table 2. PD_{out} Current, C1 = Low with OUTPUT A *NOT* Selected as "Port"; Also, Default Mode When OUTPUT A Selected as "Port"

C3	C2	PD_{out} Current
0	0	70%
0	1	80%
1	0	90%
1	1	100%

Table 3. PD_{out} Current, C1 = High with OUTPUT A *NOT* Selected as "Port"

C3	C2	PD_{out} Current
0	0	25%
0	1	50%
1	0	75%
1	1	100%

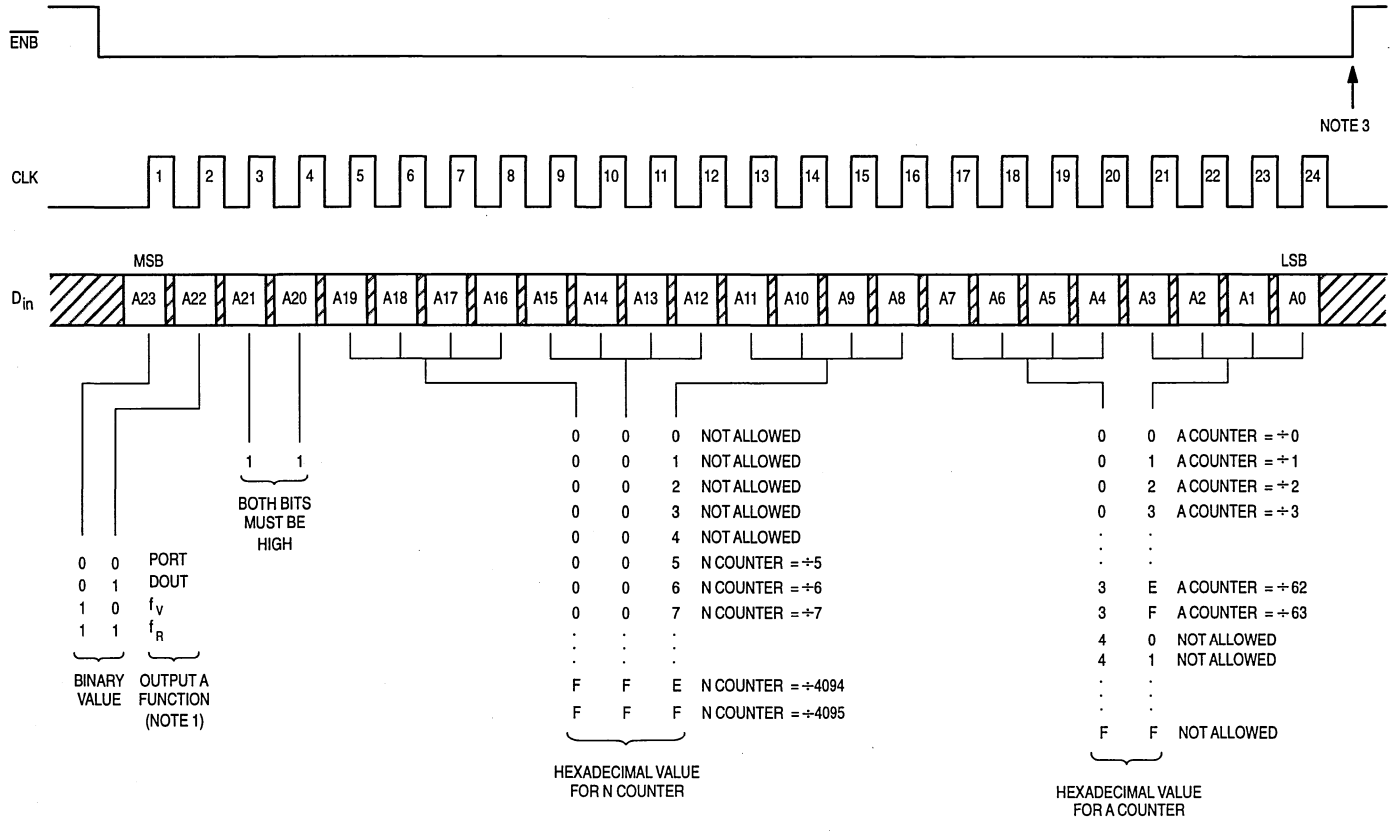
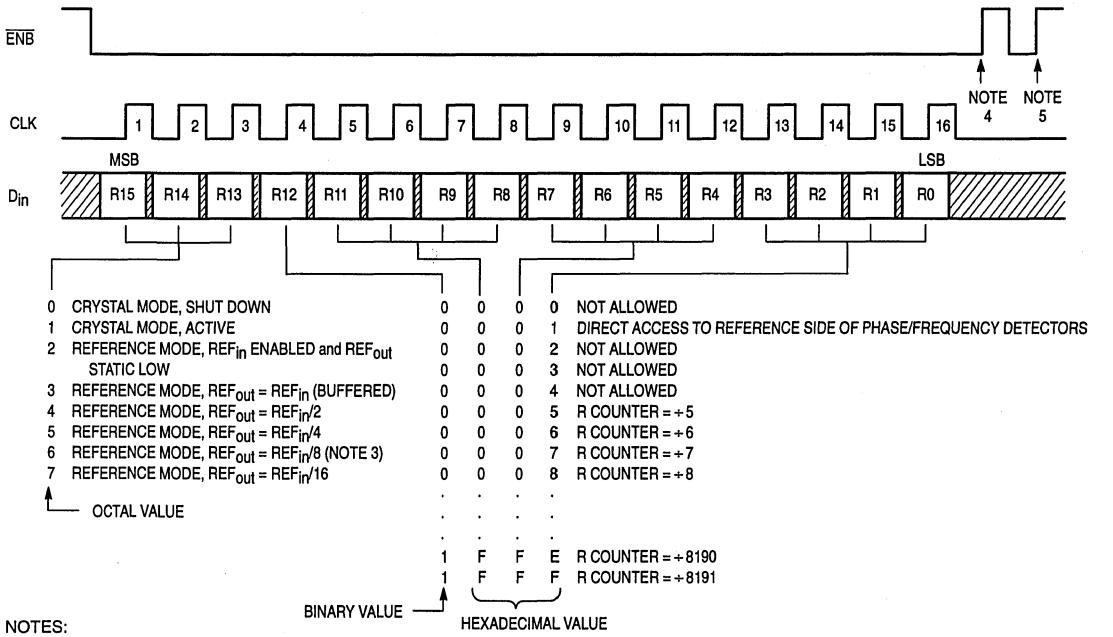


Figure 15. A Register Access and Format (24 Clock Cycles are Used)

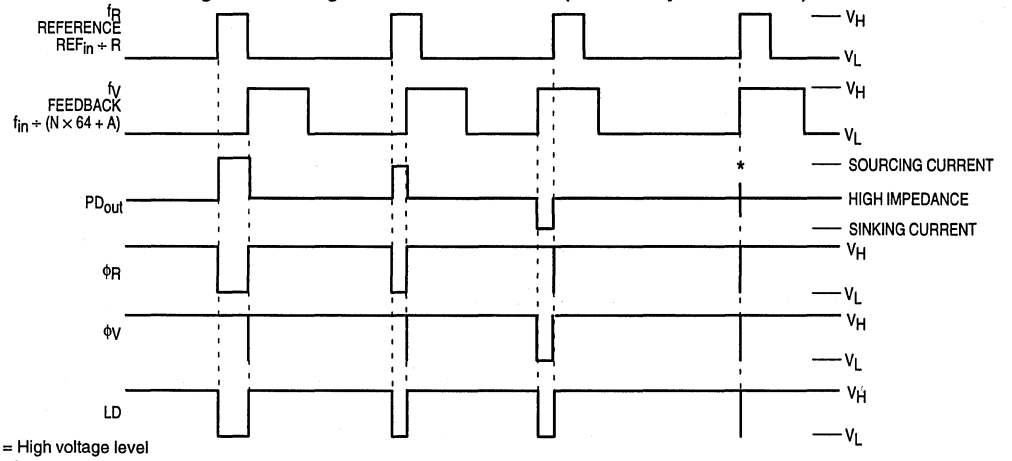
NOTES:
1. A power-on initialize circuit forces the OUTPUT A function to default to Data Out.
2. The values programmed for the N counter must be greater than or equal to the values programmed for the A counter. This results in a total divide value = N x 64 + A.
3. At this point, the three new bytes are transferred to the A register. In addition, the 13 LSBs in the first buffer of the R register are transferred to the R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of the R register is not affected. The C register is not affected.



NOTES:

1. Bits R15 through R13 control the configurable "OSC or 4-stage divider" block (see Block Diagram).
2. Bits R12 through R0 control the "13-stage R counter" block (see Block Diagram).
3. A power-on initialize circuit forces a default REF_{in} to REF_{out} ratio of eight.
4. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4-Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double-buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
5. At this point, bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note 3 of Figure 15 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

Figure 16. R Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, the output source and sink circuits are turned on for a short interval.
NOTE: The PD_{out} either sources or sinks current during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor. PD_{out}, ϕ_R, and ϕ_V are shown with the polarity bit (POL) = low; see Figure 13 for POL.

Figure 17. Phase/Frequency Detectors and Lock Detector Output Waveforms

DESIGN CONSIDERATIONS

CRYSTAL OSCILLATOR CONSIDERATIONS

The following options may be considered to provide a reference frequency to Motorola's CMOS frequency synthesizers.

Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to REF_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to REF_{in} may be used (see Figure 8).

For additional information about TCXOs and data clock oscillators, please consult the latest version of the *eem Electronic Engineers Master Catalog,* the *Gold Book,* or similar publications.

Design an Off-Chip Reference

The user may design an off-chip crystal oscillator using discrete transistors or ICs specifically developed for crystal oscillator applications, such as the MC12061 MECL device. The reference signal from the MECL device is ac coupled to REF_{in} (see Figure 8). For large amplitude signals (standard CMOS logic levels), dc coupling may be used.

Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 18.

The crystal should be specified for a loading capacitance (C_L) which does not exceed approximately 20 pF when used at the highest operating frequency of 15 MHz. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in}+C_{out}} + C_a + C_{stray} + \frac{C1 \cdot C2}{C1 + C2}$$

where

C_{in} = 5 pF (see Figure 19)
C_{out} = 6 pF (see Figure 19)
C_a = 1 pF (see Figure 19)

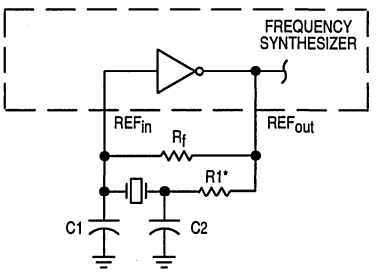
C1 and C2 = external capacitors (see Figure 18)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

The oscillator can be "trimmed" on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the REF_{in} and REF_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 20. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 18 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency (f_R) at OUTPUT A as a function of supply voltage. (REF_{out} is not used because loading impacts the oscillator.) The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful (see Table 4).



*May be needed in certain cases. See text.

Figure 18. Pierce Crystal Oscillator Circuit

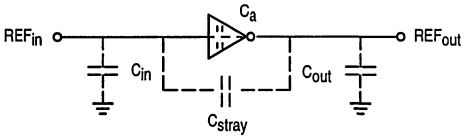
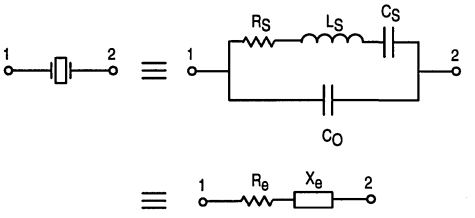


Figure 19. Parasitic Capacitances of the Amplifier and C_{stray}



Note: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 20. Equivalent Crystal Networks

RECOMMENDED READING

Technical Note TN-24, Statek Corp.

Technical Note TN-7, Statek Corp.

E. Hafner, "The Piezoelectric Crystal Unit–Definitions and Method of Measurement", *Proc. IEEE,* Vol. 57, No. 2, Feb. 1969.

D. Kemper, L. Rosine, "Quartz Crystals for Frequency Control", *Electro-Technology,* June 1969.

P. J. Ottowitz, "A Guide to Crystal Selection", *Electronic Design*, May 1966.

D. Babin, "Designing Crystal Oscillators", *Machine Design*, March 7, 1985.

D. Babin, "Guidelines for Crystal Oscillator Design", *Machine Design*, April 25, 1985.

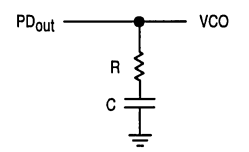
Table 4. Partial List of Crystal Manufacturers

Name	Address	Phone
United States Crystal Corp.	3605 McCart Ave., Ft. Worth, TX 76110	(817) 921-3013
Crystek Crystal	2371 Crystal Dr., Ft. Myers, FL 33907	(813) 936-2109
Statek Corp.	512 N. Main St., Orange, CA 92668	(714) 639-7810
Fox Electronics	5570 Enterprise Parkway, Ft. Myers, FL 33905	(813) 693-0099

Note: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of crystal manufacturers.

PHASE-LOCKED LOOP—LOW PASS FILTER DESIGN

(A)



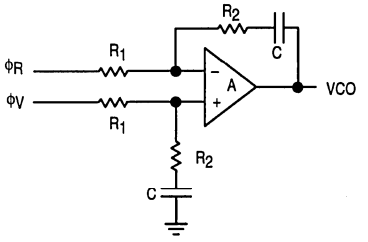
$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC}}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_\phi K_{VCO} C}{N}} = \frac{\omega_n RC}{2}$$

$$Z(s) = \frac{1 + sRC}{sC}$$

NOTE:
For (A), using K_ϕ in amps per radian with the filter's impedance transfer function, Z(s), maintains units of volts per radian for the detector/filter combination. Additional sideband filtering can be accomplished by adding a capacitor C′ across R. The corner $\omega_C = 1/RC'$ should be chosen such that ω_n is not significantly affected.

(B)



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

ASSUMING GAIN A IS VERY LARGE, THEN:

$$F(s) = \frac{R_2 sC + 1}{R_1 sC}$$

NOTE:
For (B), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.

DEFINITIONS:
N = Total Division Ratio in Feedback Loop
K_ϕ (Phase Detector Gain) = $I_{PDout}/2\pi$ amps per radian for PD_{out}
K_ϕ (Phase Detector Gain) = $V_{PD}/2\pi$ volts per radian for ϕ_V and ϕ_R

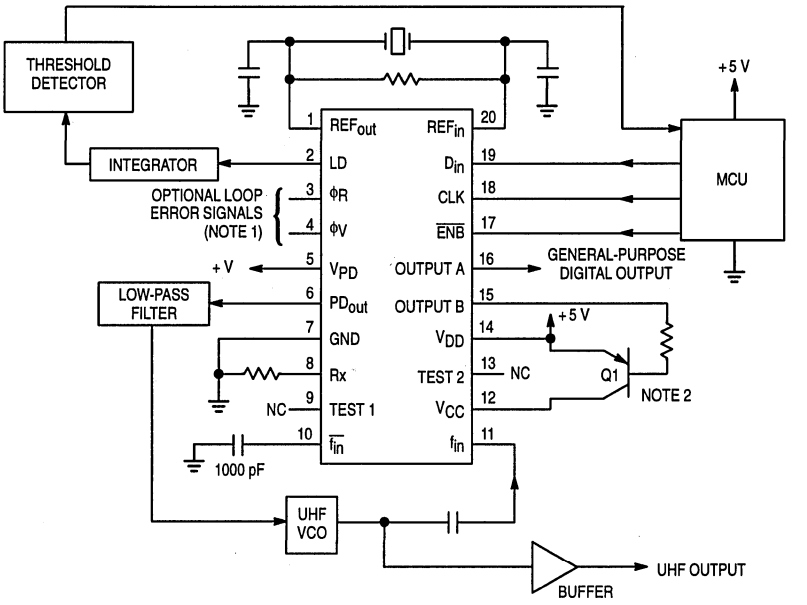
K_{VCO} (VCO Transfer Function) = $\frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$ radians per volt

For a nominal design starting point, the user might consider a damping factor $\zeta \approx 0.7$ and a natural loop frequency $\omega_n \approx (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R-related VCO sidebands.

Either loop filter (A) or (B) is frequently followed by additional sideband filtering to further attenuate f_R-related VCO sidebands. This additional filtering may be active or passive.

RECOMMENDED READING:

Gardner, Floyd M., *Phaselock Techniques (second edition).* New York, Wiley-Interscience, 1979.
Manassewitsch, Vadim, *Frequency Synthesizers: Theory and Design (second edition).* New York, Wiley-Interscience, 1980.
Blanchard, Alain, *Phase-Locked Loops: Application to Coherent Receiver Design.* New York, Wiley-Interscience, 1976.
Egan, William F., *Frequency Synthesis by Phase Lock.* New York, Wiley-Interscience, 1981.
Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design.* Englewood Cliffs, NJ, Prentice-Hall, 1983.
Berlin, Howard M., *Design of Phase-Locked Loop Circuits, with Experiments.* Indianapolis, Howard W. Sams and Co., 1978.
Kinley, Harold, *The PLL Synthesizer Cookbook.* Blue Ridge Summit, PA, Tab Books, 1980.
Seidman, Arthur H., *Integrated Circuits Applications Handbook,* Chapter 17, pp. 538-586. New York, John Wiley & Sons.
Fadrhons, Jan, "Design and Analyze PLLs on a Programmable Calculator," *EDN.* March 5, 1980.
AN535, Phase-Locked Loop Design Fundamentals, Motorola Semiconductor Products, Inc., 1970.
AR254, Phase-Locked Loop Design Articles, Motorola Semiconductor Products, Inc., Reprinted with permission from *Electronic Design,* 1987.



NOTES:

1. When used, the ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop — Low-Pass Filter Design page for additional information.
2. Transistor Q1 is required only if the standby feature is needed. Q1 permits the bipolar section of the device to be shut down via use of the general-purpose digital pin, OUTPUT B. If the standby feature is not needed, tie pin 12 directly to the power supply.
3. For optimum performance, bypass the V_{CC}, V_{DD}, and V_{PD} pins to GND with low-inductance capacitors.
4. The R counter is programmed for a divide value = REF_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by $f_R = N_T = N \times 64 + A$; this determines the values (N, A) that must be programmed into the N and A counters, respectively.

Figure 21. Example Application

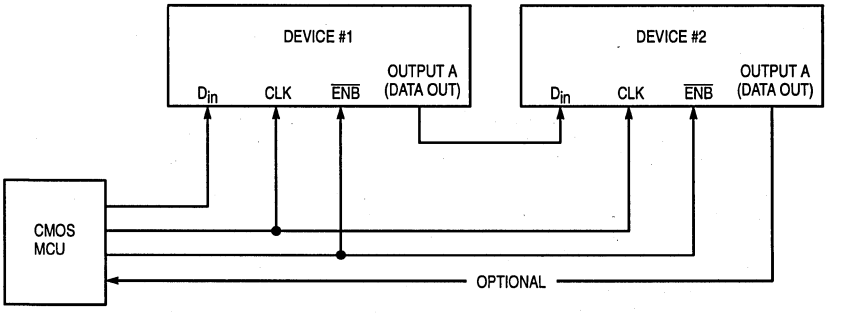
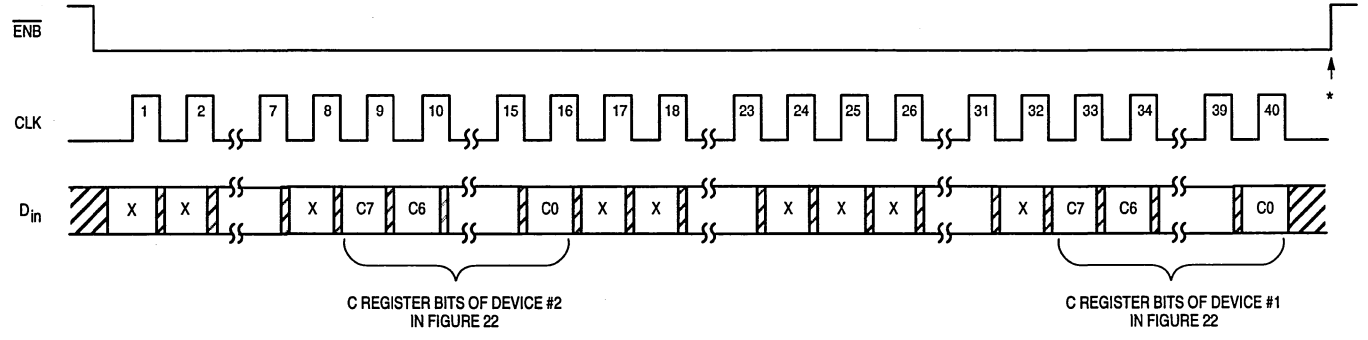
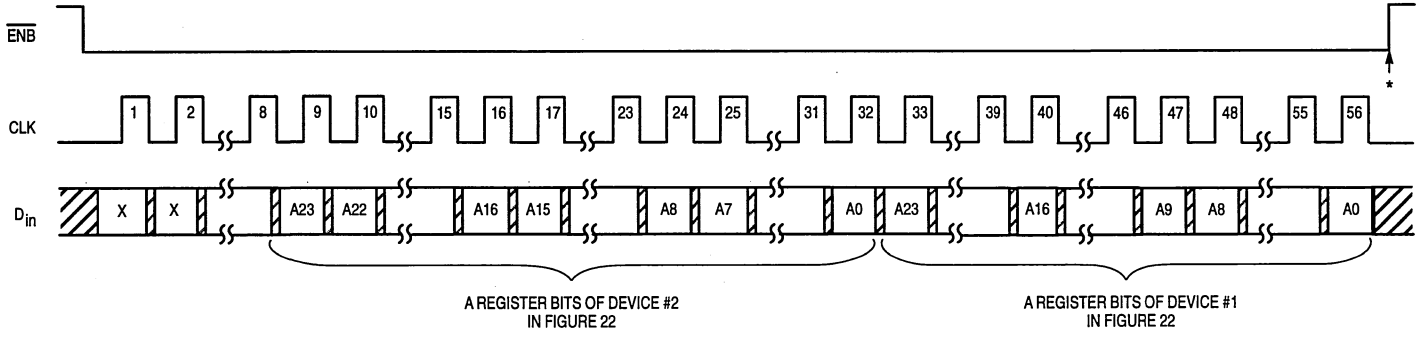


Figure 22. Cascading Two Devices



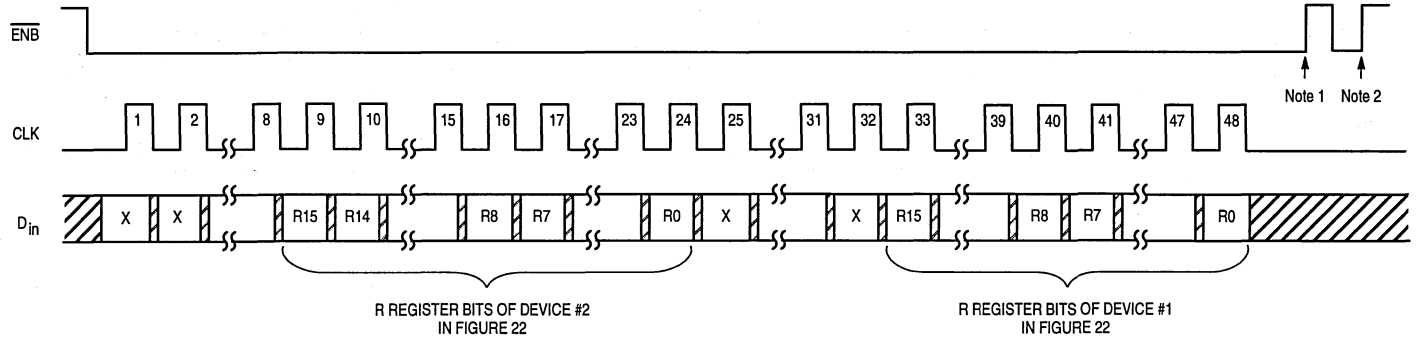
*At this point, the new bytes are transferred to the C registers of both devices and stored. No other registers are affected.

Figure 23. Accessing the C Registers of Two Cascaded Devices



*At this point, the new bytes are transferred to the A registers of both devices and stored. Additionally, for both devices, the 13 LSBs in each of the first buffers of the R registers are transferred to the respective R register's second buffer. Thus, the R, N, and A counters can be presented new divide ratios at the same time. The first buffer of each R register is not affected. Neither C register is affected.

Figure 24. Accessing the A Registers of Two Cascaded Devices



NOTES APPLICABLE TO EACH DEVICE:

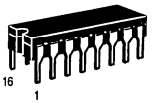
1. At this point, bits R13, R14, and R15 are stored and sent to the "OSC or 4-Stage Divider" block in the Block Diagram. Bits R0 through R12 are loaded into the first buffer in the double-buffered section of the R register. Therefore, the R counter divide ratio is not altered yet and retains the previous ratio loaded. The C and A registers are not affected.
2. At this point, the bits R0 through R12 are transferred to the second buffer of the R register. The R counter begins dividing by the new ratio after completing the rest of the present count cycle. CLK must be low during the $\overline{ENB}$ pulse, as shown. Also, see note of Figure 24 for an alternate method of loading the second buffer in the R register. The C and A registers are not affected. The first buffer of the R register is not affected.

Figure 25. Accessing the R Registers of Two Cascaded Devices

MC145402

Advance Information

Serial 13-Bit Linear Codec (A/D and D/A)

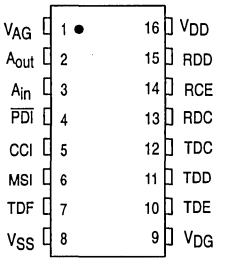


L SUFFIX
CERAMIC
CASE 620

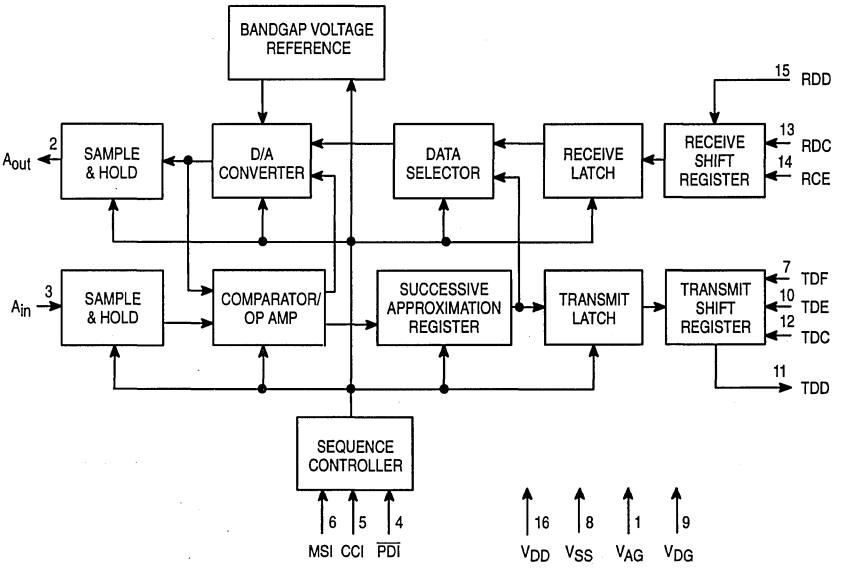
The MC145402 is a 13-bit linear monotonic digital-to-analog and analog-to-digital converter implemented in a single silicon-gate CMOS IC. Potential applications include analog interface for Digital Signal Processor (DSP) applications, high speed modems, telephone systems, SONAR, Adaptive Differential Pulse Code Modulation (ADPCM) converters, echo cancellers, repeaters, voice synthesizers, and music synthesizers.

- 60 dB Signal-to-(Noise Plus Distortion) Ratio Typical
- On-Chip Precision Voltage Reference
- Serial Data Ports
- Two's Complement Coding
- ±5 V Supply Operation
- Sample Rates from 100 Hz to 16 kHz (Both A/D and D/A), 100 Hz to 21.3 kHz (A/D Only), and 100 Hz to 64 kHz (D/A Only)
- Input Sample and Hold Provided On-Chip
- 5 V CMOS Inputs; Outputs Capable of Driving Two LSTTL Loads
- Available in a 16-Pin DIP
- Low Power Consumption: 50 mW Typical, 1 mW Power Down

PIN ASSIGNMENT



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	−0.5 to 11	V
Voltage, Any Pin to VSS	V	−0.5 to V_{DD} + 0.5	V
DC Current Drain per Pin (Exclud ing V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$ on analog inputs/outputs and $V_{DG} \le (V_{in}$ or $V_{out}) \le V_{DD}$ on digital inputs/outputs. Reliability of operation is enhanced if unused digital inputs are tied to an appropriate logic voltage level (e.g., either V_{DG} or V_{DD}) and unused analog Inputs are tied to V_{AG}.

RECOMMENDED OPERATING CONDITIONS

Parameter		Pins	0 to 70°C Min	25°C Typ	0 to 70°C Max	Unit
DC Supply Voltage		V_{DD} to V_{SS}	9.5	10	10.5	V
Power Dissipation, $\overline{PDI}$ = 1		V_{DD} to V_{SS}	—	50	80	mW
Power Dissipation, $\overline{PDI}$ = 0		V_{DD} to V_{SS}	—	1	5	mW
Conversion Rate	Full Cycle A/D and D/A Short Cycle A/D Short Cycle D/A	MSI	0.1 0.1 0.1	— — —	16 21.3 64	kHz
Conversion Sequence Rate		CCI	3.2	—	512	kHz
Date Rate		TDC, RDC	16 x f_{MSI}	—	4096	kHz
Full Scale Analog Levels (Referenced to 600 Ω)		AI, AO	— —	3.27 9.5	— —	Vp dBm

DIGITAL ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, V_{SS} = − 5 V, V_{AG} = V_{DG} = 0 V, T_A = 0 to 70°C)

Characteristic			Symbol	Min	Max	Unit
High Level Input Voltage			V_{IH}	3.5	—	V
Low Level Input Voltage			V_{IL}	—	1.5	V
Input Current			I_{in}	—	±1.0	µA
Input Capacitance			C_{in}	—	10	pF
High Level Output Voltage	TDD	I_{out} = −20 µA I_{out} = −1 mA	V_{OH}	4.9 4.3	— —	V
Low Level Output Voltage	TDD	I_{out} = −20 µA I_{out} = −1 mA	V_{OL}	— —	0.1 0.4	V

CODER AND DECODER PERFORMANCE (V_{DD} = 5 V ± 5%, V_{SS} = −5 V ± 5%, V_{AG} = V_{DG} = 0 V,
0 dBm0 = 1.60 Vrms = 6.30 dBm (600 Ω), T_A = 0 to 70°C, MSI = TDE = RCE = 8 kHz, TDC = RDC = 2.048 MHz, CCI = 256 kHz)

Characteristic		Coder (A/D)			Decoder (D/A)			Unit
		Min	Typ	Max	Min	Typ	Max	
Resolution		13	—	13	13	—	13	Bits
Conversion Time	Full Cycle A/D and D/A	62.5	—	10,000	62.5	—	10,000	µs
	Short Cycle A/D	46.9	—	10,000	—	—	—	
	Short Cycle D/A	—	—	—	15.6	—	10,000	
Differential Nonlinearity		—	—	±1	—	—	±1	LSB
Gain Error		−0.35	—	+0.35	−0.35	—	+0.35	dB
Offset		−15	—	+15	—	—	—	LSB
		—	—	—	−20	—	+20	mV
Idle Channel Noise, 3 kHz Low-Pass		—	−75	—	—	−79	—	dBm0
Signal-to-Noise (Referenced to 1.02 kHz through a f_{MSI}/2 Low-Pass Filter)	3.2 dBm0	—	61	—	—	62	—	dB
	0 dBm0	—	60	—	—	60	—	
	−10 dBm0	—	57	—	—	59	—	
	−20 dBm0	—	50	—	—	52	—	
	−30 dBm0	—	40	—	—	42	—	
	−40 dBm0	—	30	—	—	32	—	
	−50 dBm0	—	20	—	—	22	—	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V ± 5%, V_{SS} = −5 V ± 5%, V_{AG} = V_{DG} = 0 V, 0 dBm0 = 1.60 Vrms = 6.30 dBm (600 Ω), T_A = 0 to 70°C, MSI = TDE = RCE = 8 kHz, TDC = RDC = 2.048 MHz, CCI = 256 kHz)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Input Current	AI	I_{in}	—	0.01	±1	µA
AC Input Impedance	AI	Z_{in}	0.5	—	—	MΩ
Input Capacitance	AI	C_{in}	—	—	15	pF
Output Voltage Range	AO	V_{out}	−3.4	—	3.4	V
Power Supply Rejection Ratio (100 mV RMS on V_{DD} or V_{SS}, 0–50 kHz)	AO, TDD	PSRR	—	40	—	dB
Crosstalk, A_{in} to A_{out} and RDD to TDD referenced to 0 dBm0 @ 1.02 kHz	AO, TDD	—	—	−90	−75	dB
Slew Rate	AO	SR	1.5	3	—	V/µs
Settling Time (Full Scale)	AO	t_{settle}	—	8	—	µs

SWITCHING CHARACTERISTICS

(V_{DD} = + 5 V ± 5%, V_{SS} = − 5 V ± 5%, V_{AG} = V_{DG} = 0 V, T_A = 0 to 70°C, C_L = 50 pF, See Figure 1)

Characteristic		Symbol	Min	Max	Unit
Input Rise Time	RCE, RDC, TDC, TDE, CCI, MSI	t_r	—	100	ns
Input Fall Time	RCE, RDC, TDC, TDE, CCI, MSI	t_f	—	100	ns
Output Rise Time	TDD	t_r	—	80	ns
Output Fall Time	TDD	t_f	—	80	ns
Pulse Width High	RDC, MSI, CCI, TDC, RCE	t_{wH}	100	—	ns
Pulse Width Low	TDE, MSI, TDC, RCE, RDC	t_{wL}	100	—	ns
CCI Pulse Width Low		t_{wL}	500	—	ns
MSI Clock Frequency		f_{MSI}	0.1	64	kHz
CCI Clock Frequency		f_{CCI}	3.2	512	kHz
TDC and RDC Clock Frequency		f_{DC}	16 x f_{MSI}	4.1	MHz
TDC Rising Edge to TDD Data Valid During TDE High		t_{p1}	—	150	ns
TDE Rising Edge to TDD Data Valid During TDC High		t_{p2}	—	150	ns
TDE Rising Edge to TDD Low-Impedance Propagation Delay		t_{p3}	0	100	ns
TDE Falling Edge to TDD High-Impedance Propagation Delay		t_{p4}	—	40	ns
TDE Rising Edge to TDC Falling Edge Setup Time		t_{su1} t_{su2}	20 100	— —	ns
RDC Bit 0 Falling Edge to Last CCI Falling Edge Prior to MSI		t_{su3}	20	—	ns
MSI Rising Edge to CCI Falling Edge Setup Time		t_{su4} t_{su5}	20 100	— —	ns
Last CCI Rising Edge (Prior to MSI) to TDE Rising Edge		t_{su6}	100	—	ns
Last CCI Rising Edge (Prior to MSI) to First TDC Rising Edge		$t_{su6'}$	100	—	ns
First TDC Falling Edge to Last CCI Rising Edge Prior to MSI		t_{su7}	0	—	ns
RCE Rising Edge to RDC Falling Edge Setup Time		t_{su8} t_{su9}	20 100	— —	ns
RDD Valid to RDC Falling Edge Setup Time		t_{su10}	60	—	ns
RDD Hold Time from RDC Falling Edge		t_h	100	—	ns

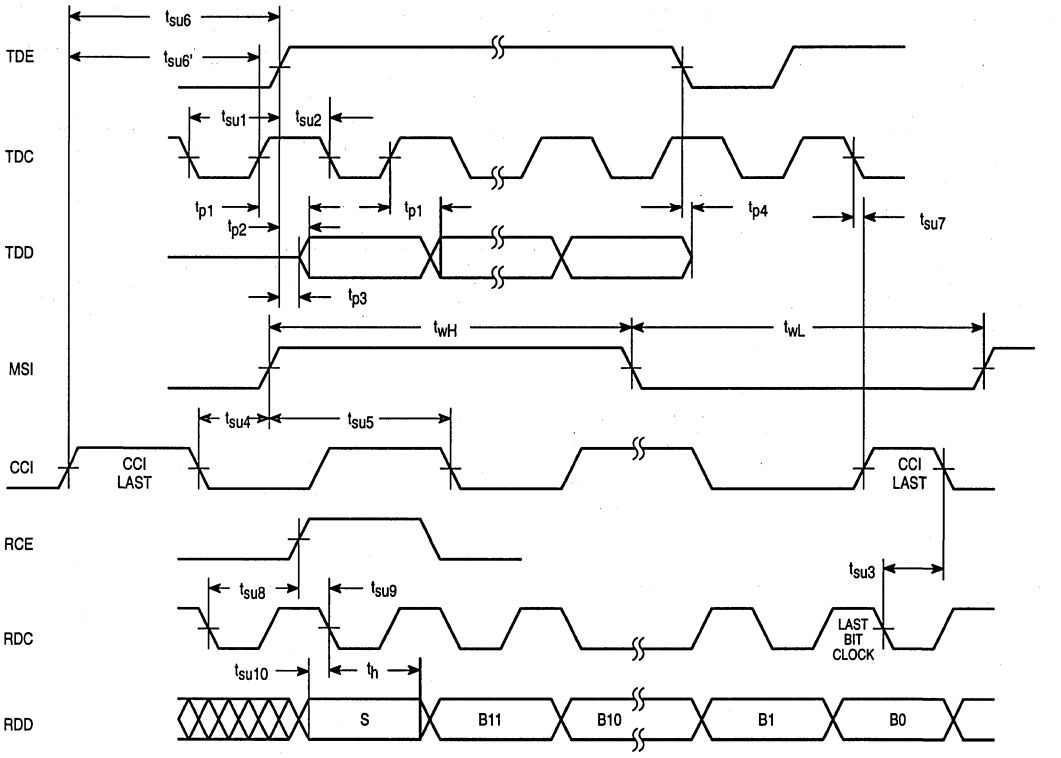


Figure 1. AC Timing Diagram

PIN DESCRIPTIONS

V_{DD}
Positive Supply (Pin 16)
The most positive power supply, typically + 5 V in split power supply configurations or +10 V in single supply systems.

V_{SS}
Negative Supply (Pin 8)
The most negative power supply, typically −5 V in split power supply configurations or 0 V in single supply systems.

V_{AG}
Analog Ground (Pin 1)
This is the analog signal reference point. This pin is normally tied to 0 V in split supply operation or $V_{DD}/2$ in single supply systems.

V_{DG}
Digital Ground (Pin 9)
This is the ground reference for all of the digital input and output pins. CMOS compatible logic signals swing from V_{DG} to V_{DD} where V_{DG} can be established anywhere from V_{DD} −4.75 V to V_{SS}.

A_{out}
Analog Output (Pin 2)
This is the output of the decoder's sample and hold circuit and is a 100% duty cycle analog output of the last digital word received and decoded by the decoder. A_{out} is updated approximately 60 ns after the rising edge of the last CCI prior to MSI (see Figure 2). A_{out} is capable of driving a 10 kΩ, 50 pF load.

A_{in}
Analog Input (Pin 3)
This is the high-impedance input to the coder. An A/D cycle begins on the first falling edge of CCI following the rising edge of MSI. A_{in} is sampled approximately 50 ns after the rising edge of CCI prior to the start of the A/D cycle.

$\overline{PDI}$
Power-Down Input (Pin 4)
In normal operation this Input should be tied high. A logic low on this input puts the device into a minimum power dissipation mode. During power-down, all functions stop. Two complete MSI conversion cycles are required to establish normal operation after leaving the power-down mode.

CCI
Convert Clock Input (Pin 5)

This input controls the complete conversion sequence during one MSI cycle and must receive a clock which is 32 times the frequency of MSI. The only exception to 32 times the frequency of MSI is during short-cycle operation. See ***General Modes of Operation*** section. CCI must be synchronous and approximately rising edge aligned with MSI.

MSI
Master Sync Input (Pin 6)

This pin determines the conversion rate for both the coder and the decoder. One A/D and D/A conversion takes place during each period of the digital clock applied to this input (except in short-cycle operation, see ***General Modes of Operation*** section). MSI must be synchronous and approximately rising edge aligned with CCI.

TDC
Transmit Data Clock (Pin 12)

Digital data from the coder is serially transmitted from TDD on rising TDC edges whenever TDE is a logic high. TDC must be approximately rising edge aligned with TDE. Generally, if TDC is low when TDE rises, the first rising edge of TDC clocks the first data bit. If TDC is high when TDE rises, the first bit will be clocked by TDE and the first rising edge of TDC after TDE rises will clock out the second data bit.

TDE
Transmit Data Enable (Pin 10)

This pin is used to initiate the serial transfer of data from the coder and provides three-state control of the TDD pin. The rising edge of TDE (or TDC if it follows TDE) signals the start of data transfer from the TDD pin. A resulting high logic level on TDE also releases TDD from its high-impedance state. TDE must remain high throughout the data transfer to keep TDD in the low-impedance state and must return to a low state prior to each data transfer. If TDE remains high for more than 16 TDC clocks, the 16 bits of TDD data will be recirculated. (Note: The A/D cycle begins on the first falling edge of CCI after the rising edge of MSI. The internal transmit latch is updated one and one half CCI periods prior to the start of the A/D cycle. A pulse generated by the logical AND of TDE and the first TDC transfers data to the transmit shift register, and this pulse must not occur when the transmit latch is updated. See Figure 2 and see t_{su6}, $t_{su6'}$, and t_{su7} of Figure 1.

TDD
Transmit Digital Data (Pin 11)

This is the three-state output data pin from the coder and is controlled by the TDE and TDC pins. TDD is in the high-impedance state whenever TDE is a logic low. The first data bit is output from TDD on the rising edge of TDE (or TDC if it follows TDE) and each subsequent bit is output on rising edges of TDC. Two output data formats are available as described in the TDF pin description below.

TDF
Transmit Data Format (Pin 7)

The 13-bit digital output of the coder is available in one of two 16-bit two's complement formats as determined by the state of this pin. A logic 0 at this pin causes the data from TDD to be in a 16-bit sign-extended format as follows: SSSSM ... L where S, M, and L represent the sign, most significant bit, and the least significant bit, respectively. A logic 1 on this pin formats the data as follows: SM ... LSSS (see Figure 3). RDD data is not affected by the state of this pin and if a "digital loopback" is needed (TDD data looped back into RDD), this pin should be high.

RDC
Receive Data Clock (Pin 13)

Receive digital data is accepted by the decoder on the first 13 falling edges of RDC after an RCE rising edge.

RCE
Receive Clock Enable (Pin 14)

This pin identifies the beginning of a date transfer into the RDD pin of the decoder. The first 13 falling edges of RDC after an RCE rising edge will clock data into the decoder data input, RDD. RCE must return low prior to each data transfer. Since receive data is latched into the receive latch on the last CCI falling edge prior to MSI, date transfers may not span this falling edge of CCI without loss of data.

RDD
Receive Digital Data (Pin 15)

This pin is the data input to the decoder and is controlled by the RDC and RCE pins described above. Two's complement data are loaded in the following sequence: SM ... L where S, M, and L represent the sign, most significant bit, and the least significant bit, respectively. Only the first 13 bits clocked by RDC after RCE rises will be accepted for decoding. Any additional bits will be ignored (see Figure 3).

GENERAL INFORMATION

GENERAL MODES OF OPERATION

The MC145402 has three modes of operation; a "full" cycle mode and two "short" cycle modes. The full cycle mode allows simultaneous analog-to-digital (A/D) and digital-to-analog (D/A) operation. The short cycle modes allow either A/D only or D/A only operation. Two MSI cycles are required for the MC145402 to detect which operating mode has been selected. See Figure 2 for full versus short cycle clocking.

Full Cycle Operation

When operating in the full cycle mode, the MC145402 performs a 13-bit A/D conversion followed by a 13-bit D/A conversion. Full cycle operation is selected by using a CCI frequency that is 32 times the frequency of MSI. MSI is the sample rate frequency.

Short Cycle Analog to Digital Operation

If CCI is 24 times the frequency of MSI, short cycle analog to digital operation is selected. This allows a 13-bit A/D conversion only. In this mode, the D/A is not operational and any data applied to the RDD input is ignored.

Short Cycle Digital to Analog Operation

Short cycle digital to analog operation is selected by using a CCI clock frequency that is eight times the MSI sample rate. During short cycle D/A operation, A/D operation is disabled and digital data read from TDD is not valid.

CLOCKING RECOMMENDATIONS

For optimum differential nonlinearity performance, all data transitions on TDD and RDD should be limited to the first four CCI cycles following the rising edge of MSI. This may be achieved by setting MSI = TDE = RCE having a duration of 16 data clock cycles, and TDC = RDC $\geq 4 \times$ CCI clock frequency. Figure 6 shows a circuit that generates this clocking configuration; see ***Application Circuits*** section.

SIGNAL TO DISTORTION RATIO

Figures 4 and 5 show graphs of typical signal to distortion ratios versus signal level for the MC145402. The presented data is referenced to a 1020 Hz input sinusoidal frequency with signal levels referenced to 600 Ω and transmission level point adjusted (e.g., 0 dBm0 at 600 Ω with a TLP of 6.30 dB is 4.53 V peak-to-peak). For comparison, ideal signal to noise ratios for 9-, 10-, 11-, 12-, and 13-bit A/D and D/A converters are also shown. The equation used for an ideal RMS to RMS signal to distortion ratio is:

$$S/D = N \times 6\ dB + 1.76\ dB$$

where N is the number of bits of resolution, 6 dB per bit, and $1.76 = 20_{log}\ (\sqrt{3}/\sqrt{2})$.

$(\sqrt{3}/\sqrt{2})$ is approximately the RMS to RMS ratio of a sine wave to white noise.

The signal to noise plus distortion ratio is measured through a brickwall low-pass filter set to the Nyquist frequency of the A/D and D/A sample rate. For an 8 kHz sample rate, the low-pass filter is set to block all signals above 4 kHz.

APPLICATION CIRCUITS

Figure 6 shows a typical circuit for generating the clock frequencies for the MC145402. This circuit uses an MC74HC4040 and a 2.048 MHz crystal to generate the 256 kHz frequency for internal sequencing, 1.024 MHz for the date clocks, and an 8 kHz sample frequency. A 4.096 MHz crystal could be used for a sample rate of 16 kHz.

Figure 7 shows the MC145402 interfaced to the DSP56000 digital signal processor. The DSP56000 can internally generate the clocks for the MC145402 using the SSI serial interface. SCK provides the sequencing and data clocks (non-gated continuous dock) and SC2 (setup as the Frame Sync Out, FSL = 0) provides the sample rate and data enables for the MC145402. The divide-by-four circuit to generate the CCI clock is recommended for optimum MC145402 performance, and allows the DSP56000 to clock data in and out of the MC145402 quickly, leaving time available for processing by the DSP before another sample is available. SC0 and SC1 could be used to gate the enables to select up to four devices on the SSI bus.

TELEPHONE SYSTEM TRANSMISSION LEVEL POINT FOR A LINEAR A/D OR D/A CONVERTER REFERENCED TO MU-LAW COMPANDING

Mu-law companding, as specified by AT&T and CCITT, requires 8159 quantization levels to implement both A/D and D/A conversion schemes. This is to be mirrored about signal ground for the negative part of the wave form.

To implement a 13-bit (± 12-bit) linear converter scheme requires 8192 quantization levels mirrored about signal ground. To specify this converter such that it can be used to interface with, or as an alternative to, telephony based Mu-law applications, the following is an explanation of the gain translation.

A 13-bit linear converter scheme has 8192 quantization levels. The goal is to be able to convert between these two encoding schemes with minimal distortion. This dictates setting the LSBs to the same level. For this to be achieved requires the reference voltage of the linear converter to be 8192/8159 times the reference voltage of the Mu-law converter. The peak amplitude of a Mu-law converter is 3.17 dBm0. The peak level of the linear converter will be 8192/8159 times the peak level of the Mu-law converter, which is 8192/8159 × 3.17 dBm0. However, you cannot multiply a gain factor by a dBm value without using common term units and math (i.e., we must convert this gain factor to a dB equivalent), which is:

$$20 \log_{10} (8192/8159) = 0.03\ dB$$

With the gain factor in dB, we can add it to the Mu-law peak level:

$$3.17\ dBm0 + 0.03\ dB = 3.20\ dBm0$$

Therefore, the linear converter peak level is 3.20 dBm0.

This is another way of saying the 0 dBm0 level for the linear converter is 3.20 dB below the maximum amplitude.

To determine the absolute 0 dBm0 level for the linear converter from the peak level, we calculate the peak level in dBm by:

$$10\ \log_{10} \frac{3.27\ VpK/\sqrt{2})^2/(600\ \Omega)}{1\ mW} = 9.50\ dBm\ (600\ \Omega)$$

and 3.20 dB below this level is the 0 dBm0 absolute amplitude, which is

$$9.50\ dBm - 3.20\ dB = 6.30\ dBm\ (600\ \Omega)$$

Therefore, the calibration level, or transmission level point (TLP), for this part is 6.30 dBm (600 Ω), which is 1.6 Vrms based on the reference voltage of 3.27 V.

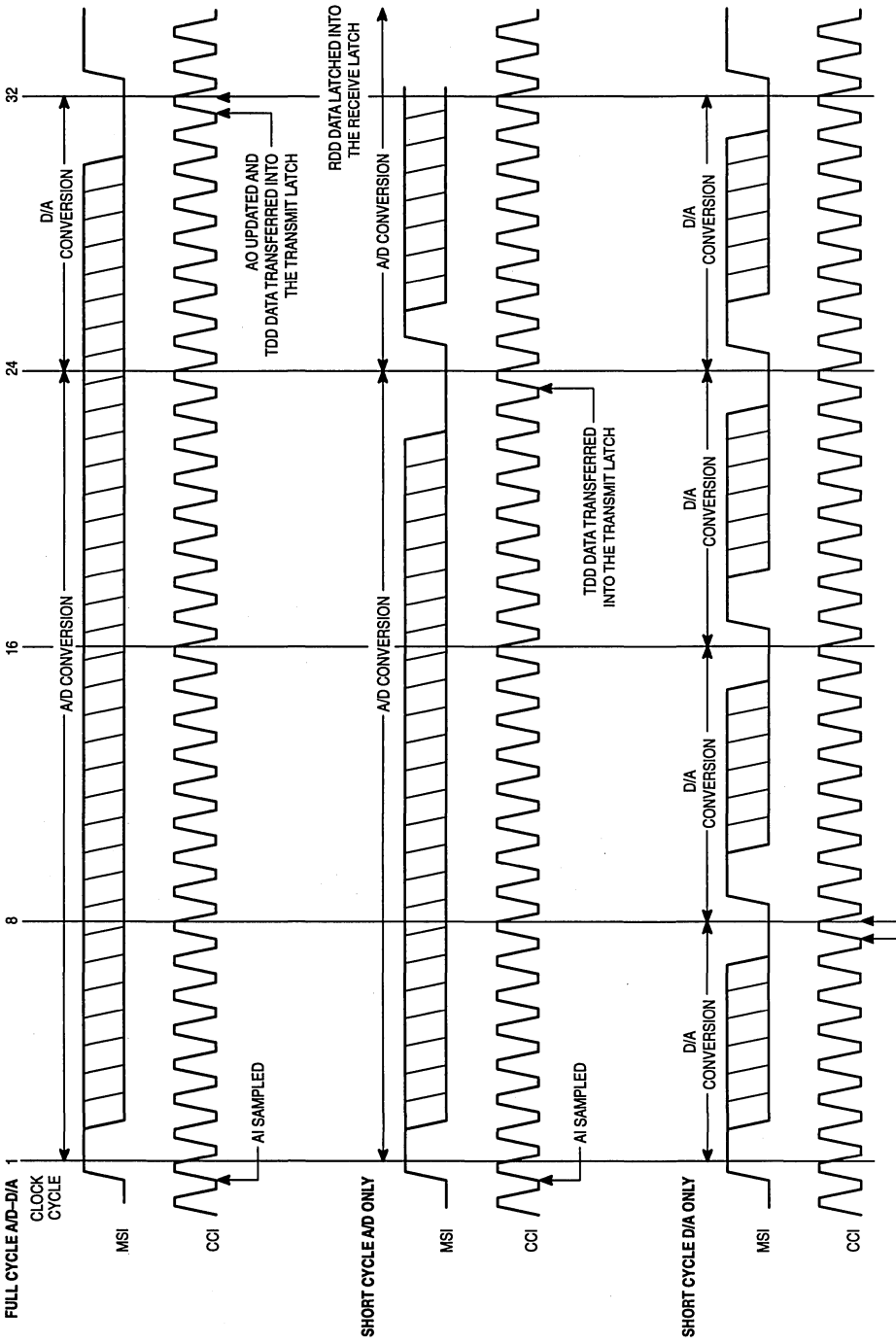


Figure 2. MC145402 Full and Short Cycle Timing

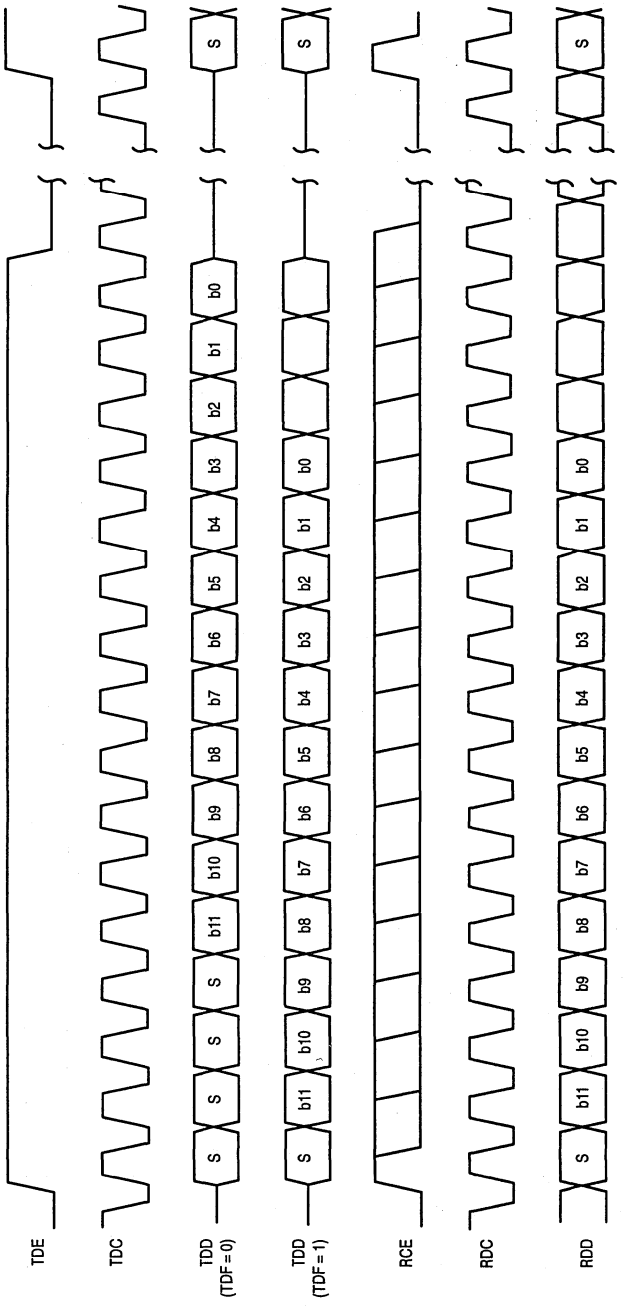


Figure 3. MC145402 Digital Data Timing

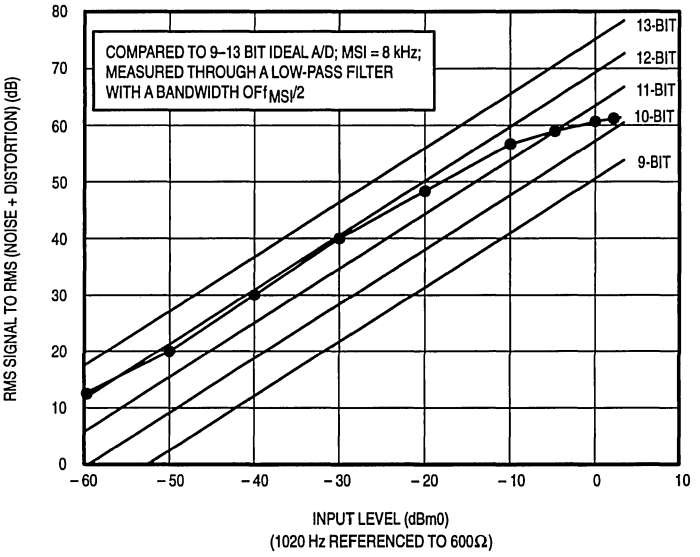


Figure 4. MC145402 Encoder (A/D) Signal to Noise Plus Distortion Ratio

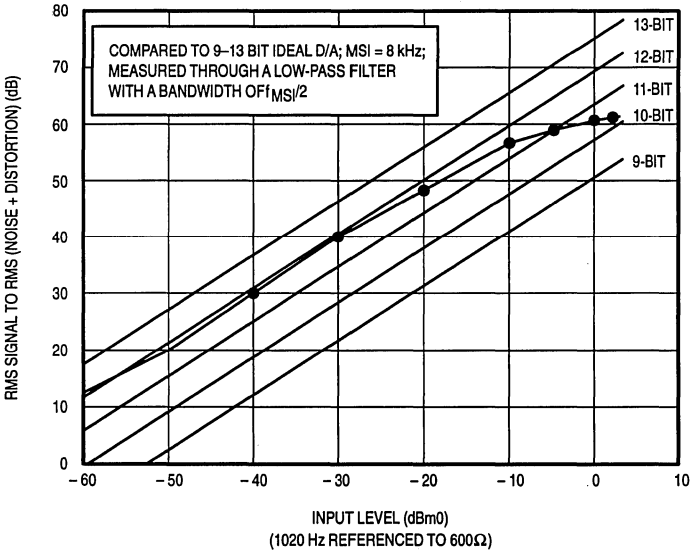


Figure 5. MC145402 Decoder (D/A) Signal to Noise Plus Distortion Ratio

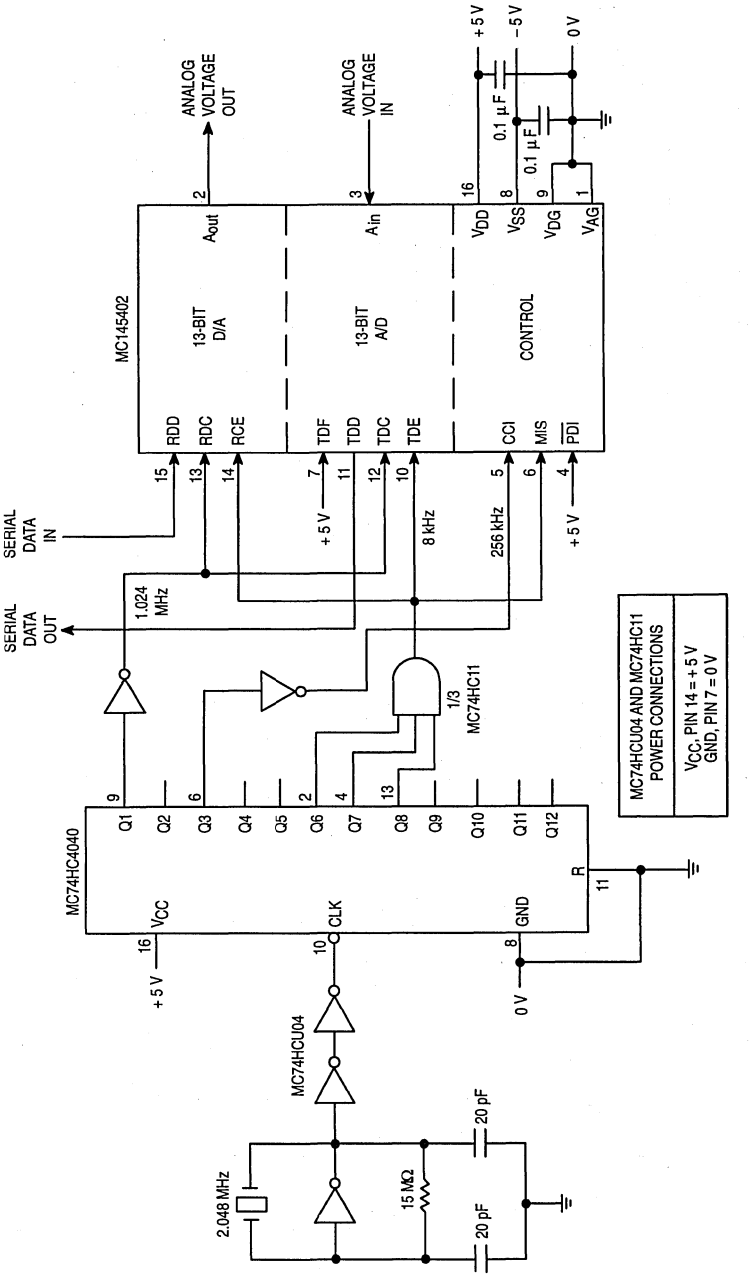


Figure 6. Typical MC145402 Configuration

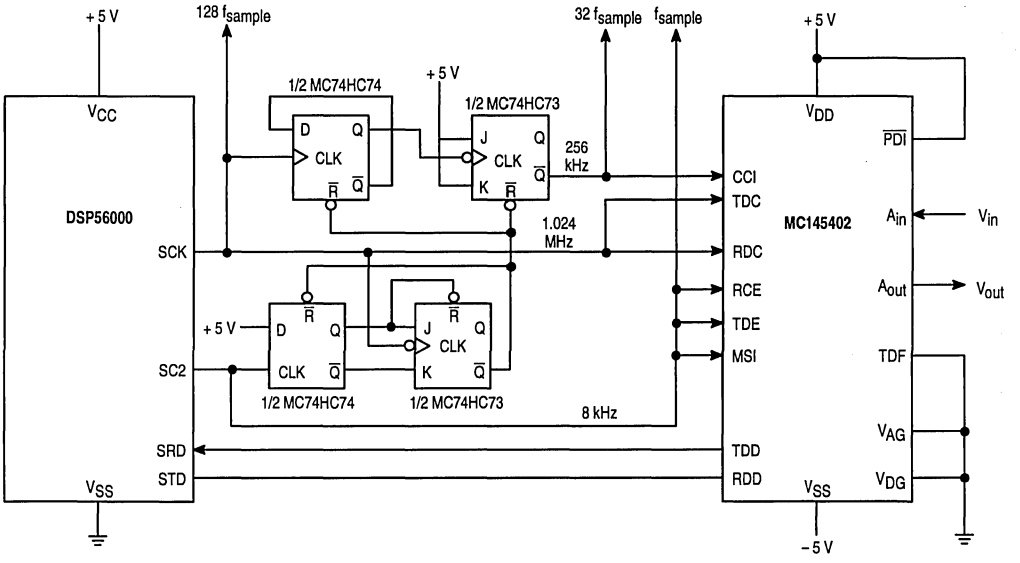


Figure 7. The MC145402, 13-Bit Linear Codec, Interfaced to a Motorola DSP56000, Digital Signal Processor, SSI Port

MC145403
MC145404
MC145405
MC145408

Drivers/Receivers
EIA-232-E and CCITT V.28

These devices are silicon gate CMOS ICs that combine both the transmitter and receiver to fulfill the electrical specifications of EIA Standard 232-E and CCITT V.28. The drivers feature true TTL input compatibility, slew rate limiting outputs, 300-Ω power-off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ±25 V while presenting 3 to 7 kΩ impedance. Hysteresis in the receivers aid in the reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, these devices provide efficient, low-power solutions for both EIA-232-E and V.28 applications.

These devices offer the following performance features:

Drivers

- ±5 to ±12 V Supply Range
- 300-Ω Power-Off Source Impedance
- Output Current Limiting
- TTL and CMOS Compatible Inputs
- Driver Slew Rate Range Limited to 30 V/μs Maximum

Receivers

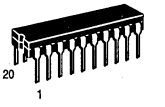
- ±25 V Input Range
- 3 to 7 kΩ Input Impedance
- 0.8 V of Hysteresis for Enhanced Noise Immunity
- TTL and CMOS Compatible Outputs

Available Driver/Receiver Combinations

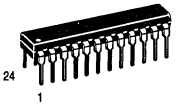
Device	Drivers	Receivers	Figure	No. of Pins
MC145403	3	5	1	20
MC145404	4	4	2	20
MC145405	5	3	3	20
MC145408	5	5	4	24

Alternative EIA-232 devices to consider are:

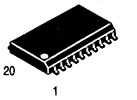
Three Supply	Single Supply
MC145406 (3x3)	MC145407 (3x3)
	MC145705 (2x3) with Power Down
	MC145706 (3x2) with Power Down
	MC145707 (3x3) with Power Down



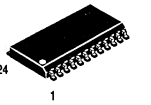
P SUFFIX
PLASTIC
CASE 738



P SUFFIX
PLASTIC
CASE 724



DW SUFFIX
SO
CASE 751D



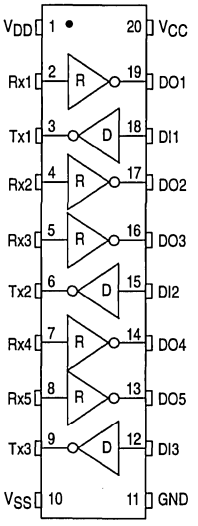
DW SUFFIX
SO
CASE 751E

ORDERING INFORMATION

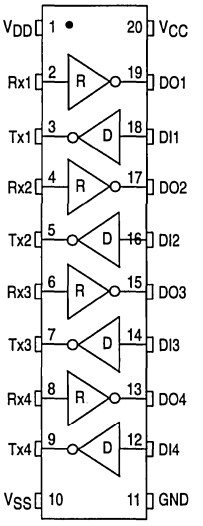
MC145403P
MC145404P
MC145405P
MC145408P
} Plastic DIP

MC145403DW
MC145404DW
MC145405DW
MC145408DW
} SO Package

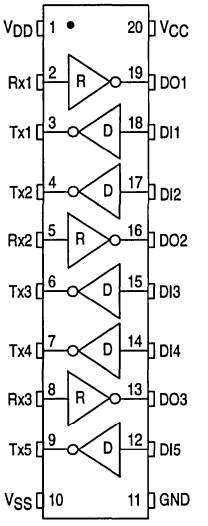
PIN ASSIGNMENTS
(DIP and SO)



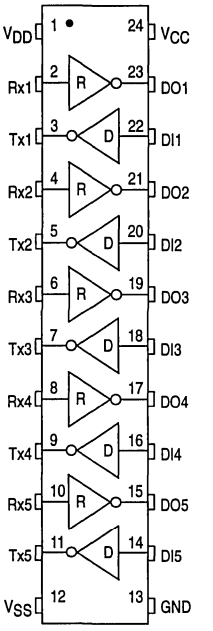
MC145403
3 Drivers/5 Receivers



MC145404
4 Drivers/4 Receivers



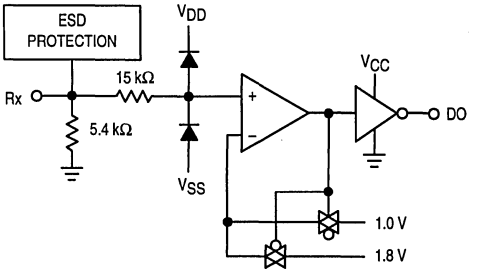
MC145405
5 Drivers/3 Receivers



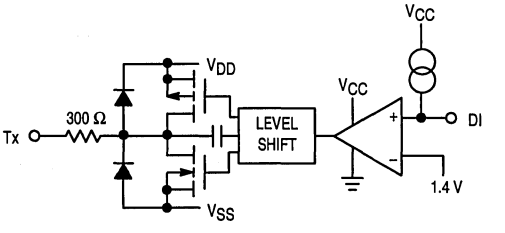
MC145408
5 Drivers/5 Receivers

FUNCTIONAL DIAGRAM

RECEIVER



DRIVER



ABSOLUTE MAXIMUM RATINGS (Voltages referenced to GND, except where noted)

Rating	Symbol	Value	Unit
DC Supply Voltage ($V_{DD} \geq V_{CC}$)	V_{DD} V_{SS} V_{CC}	−0.5 to +13.5 +0.5 to −13.5 −0.5 to +6.0	V
Input Voltage Range Rx1–Rx*n* DI1–DI*n*	V_{IR}	 V_{SS} − 15 to V_{DD} + 15 0.5 to V_{CC} + 15	V
DC Current Drain per Pin	I	± 00	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{out} and V_{in} be constrained to the ranges described as follows:

Digital I/O: Driver Inputs (DI):
($GND \leq V_{DI} \leq V_{CC}$).
Receiver Outputs (DO):
($GND \leq V_{DO} \leq V_{CC}$).
EIA-232 I/O: Driver Outputs (Tx):
($V_{SS} \leq V_{Tx1-Txn} \leq V_{DD}$).
Receiver Inputs (Rx):
V_{SS}−15 V ≤ $V_{Rx1-Rxn}$ ≤ V_{DD} + 15 V).

Reliability of operation is enhanced if unused outputs are tied off to an appropriate logic voltage level (e.g., either GND or V_{CC} for DI, and GND for Rx).

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V, T_A = −40 to +85°C)

Parameter		Symbol	Min	Typ	Max	Unit
DC Supply Voltage		V_{DD} V_{SS} V_{CC}	4.5 −4.5 4.5	5 to 12 −5 to −12 5	13.2 −13.2 5.5	V
Quiescent Supply Current (Outputs Unloaded, Inputs Low)	V_{DD} = +12 V V_{SS} = −12 V V_{CC} = +5 V	I_{DD} I_{SS} I_{CC}	— — —	425 −400 110	635 −600 200	µA

RECEIVER ELECTRICAL SPECIFICATIONS
(Voltage polarities referenced to GND = 0 V, V_{DD} = +12 V, V_{SS} = −12 V, T_A = −40 to +85°C, V_{CC} = +5 V, ±5%)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Turn-on Threshold $V_{DO} = V_{OL}$	Rx1–Rx*n*	V_{on}	1.35	1.8	2.35	V
Input Turn-off Threshold $V_{DO} = V_{OH}$	Rx1–Rx*n*	V_{off}	0.75	1	1.25	V
Input Threshold Hysteresis $\Delta = V_{on} - V_{off}$		V_{hys}	0.6	0.8	—	V
Input Resistance (V_{SS} − 15 V) ≤ V Rx1–Rx*n* ≤ (V_{DD} + 15 V)		R_{in}	3	5.4	7	kΩ
High Level Output Voltage V_{Rx} = −3 to −25 V* (DO1–DO*n*)	I_{out} = −20 µA I_{out} = −1.0 mA	V_{OH}	4.9 3.8	4.9 4.3	— —	V
Low Level Output Voltage V_{Rx} = +3 to +25 V* (DO1–DO*n*)	I_{out} = +2 mA I_{out} = +4 mA	V_{OL}	— —	0.02 0.5	0.5 0.7	V

*This is the range of input voltages as specified by EIA-232-E to cause a receiver to be in the high or low.

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage Polarities Referenced to Gnd = 0 V, V_{dd} = +12 V, V_{ss} = −12 V, T_a = −40 to +85°C, V_{cc} = +5 V, ±5%)

Characteristic		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1–DI*n*					V
Logic 0		V_{IL}	—	—	0.8	
Logic 1		V_{IH}	2	—	—	
Input Current	DI1–DI*n*					μA
V_{DI} = GND		I_{IL}	—	7	—	
V_{DI} = V_{CC}		I_{IH}	—	—	±1.0	
Output High Voltage	Tx1–Tx*n*	V_{OH}				V
V_{DI} = Logic 0, R_L = 3 kΩ						
V_{DD} = +5.0 V, V_{SS} = −5.0 V			3.5	3.9	—	
V_{DD} = +6.0 V, V_{SS} = −6.0 V			4.3	4.7	—	
V_{DD} = +12.0 V, V_{SS} = −12.0 V			9.2	9.5	—	
Output Low Voltage*	Tx1–Tx*n*	V_{OL}				V
V_{DI} = Logic 1, R_L = 3 kΩ						
V_{DD} = +5.0 V, V_{SS} = −5.0 V			−4	−4.3	—	
V_{DD} = +6.0 V, V_{SS} = −6.0 V			−4.5	−5.2	—	
V_{DD} = +12.0 V, V_{SS} = −12.0 V			−10	−10.3	—	
Input Current (Figure 5)	Tx1–Tx*n*	Z_{off}	300	—	—	Ω
Output Short Circuit Current	Tx1–Tx*n*	I_{SC}				mA
V_{DD} = +12 V, V_{SS} = −12 V						
Tx Shorted to GND**			—	±22	±60	
Tx Shorted to ±15 V***			—	±60	±100	

* Voltage specifications are in terms of absolute values.

** Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.

*** This condition could exceed package limitations.

SWITCHING CHARACTERISTICS

(V_{CC} = +5 V, ±5%, V_{DD} = +12 V, V_{SS} = −12 V, T_A = −40 to +85°C; See Figures 2 and 3)

Drivers

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Tx					ns
Low-to-High					
R_L = 3 kΩ, C_L = 50 pF	t_{PLH}	—	500	1000	
High-to-Low					
R_L = 3 kΩ, C_L = 50 pF	t_{PHL}	—	700	1000	
Output Slew Rate	SR				V/μs
Minimum Load					
R_L = 7 kΩ, C_L = 0 pF (V_{DD} = 6 to 12 V, V_{SS} = −6 to −12 V)		—	±6	±30	
Maximum Load					
R_L = 3 kΩ, C_L = 2.5 pF (V_{DD} = 6 to 12 V, V_{SS} = −6 to −12 V)		4	—	—	

Receivers (C_L = 50 pF)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time					ns
Low-to-High	t_{PLH}	—	360	610	
High-to-Low	t_{PHL}	—	130	610	
Output Rise Time	t_r	—	250	400	ns
Output Fall Time	t_f	—	40	100	ns

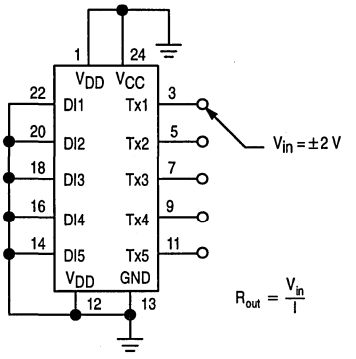


Figure 1. Power Off Source Resistance Illustrated for MC145408

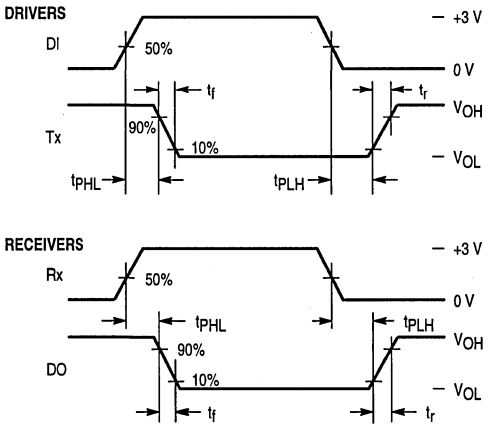


Figure 2. Switching Characteristics

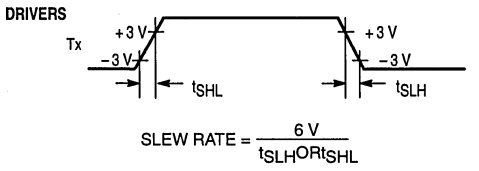


Figure 3. Slew Rate Characteristics

PIN DESCRIPTIONS

V_{CC}
Digital Power Supply
The digital supply pin, which is connected to the logic power supply (+5.5 V maximum).

GND
Ground
Ground return pin is typically connected to the signal ground pin of the EIA-232-E connector (Pin 7) as well as to the logic power supply ground.

V_{DD}
Most Positive Device Pin
The most positive power supply pin, which is typically +5 to +12 V.

V_{SS}
Most Negative Device Pin
The most negative power supply pin, which is typically −5 to −12 V.

Rx1–Rx*n*
Receive Data Input Pins
These are the EIA-232-E receive signal inputs. A voltage between +3 and +25 V is decoded as a space, and causes the corresponding DO pin to swing to ground (0 V). A voltage between −3 and −25 V is decoded as a mark, and causes the corresponding DO pin to swing to V_{CC}.

DO1–DO*n*
Data Output Pins
These are the receiver digital output pins which swing from V_{CC} to GND. Each output pin is capable of driving one LSTTL input load.

DI1–DI*n*
Data Input Pins
These are the high impedance digital input pins to the drivers. Input voltage levels on these pins are LSTTL compatible and must be between V_{CC} and GND. A weak pull-up on each input sets all unused DI pins to V_{CC}, causing the corresponding unused driver outputs to be at V_{SS}.

Tx1–TX*n*
Transmit Data Output Pins
These are the EIA-232-E transmit signal output pins, which swing from V_{DD} to V_{SS}. A logic 1 at the DI input causes the corresponding Tx output to swing to V_{SS}. A logic 0 at the DI input causes the corresponding Tx out to swing to V_{DD}. The actual levels and slew rate achieved will depend on the output loading (R_L || C_L).

APPLICATION INFORMATION

POWER SUPPLY CONSIDERATIONS

Figure 4 shows a technique to guard against excessive device current.

The diode D1 prevents excessive current from flowing through an internal diode from the V_{CC} pin to the V_{DD} pin when $V_{DD} < V_{CC}$ by approximately 0.6 V or greater. This high current condition can exist for a short period of time during power up/down. Additionally, if the + 12 V supply is switched off while the + 5 V is on and the off supply is a low impedance to ground, the diode D1 will prevent current flow through the internal diode.

The diode D2 is used as a voltage clamp, to prevent V_{SS} from drifting positive to V_{CC}, in the event that power is removed from V_{SS} (Pin 12). If V_{SS} power is removed, and the impedance from the V_{SS} pin to ground is greater than approximately 3 kΩ, this pin will be pulled to V_{CC} by internal circuitry causing excessive current in the V_{CC} pin.

If by design, neither of the above conditions are allowed to exist, then the diodes D1 and D2 are not required.

ESD PROTECTION

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply buses of the IC. This coupling will usually occur through the internal ESD protection diodes. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. Figure 4 shows a technique which will clamp the ESD voltage at approximately ±15 V using the MMVZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the capacitors C1–C3. This scheme has provided protection to the interface part up to ±10 kV, using the human body model test.

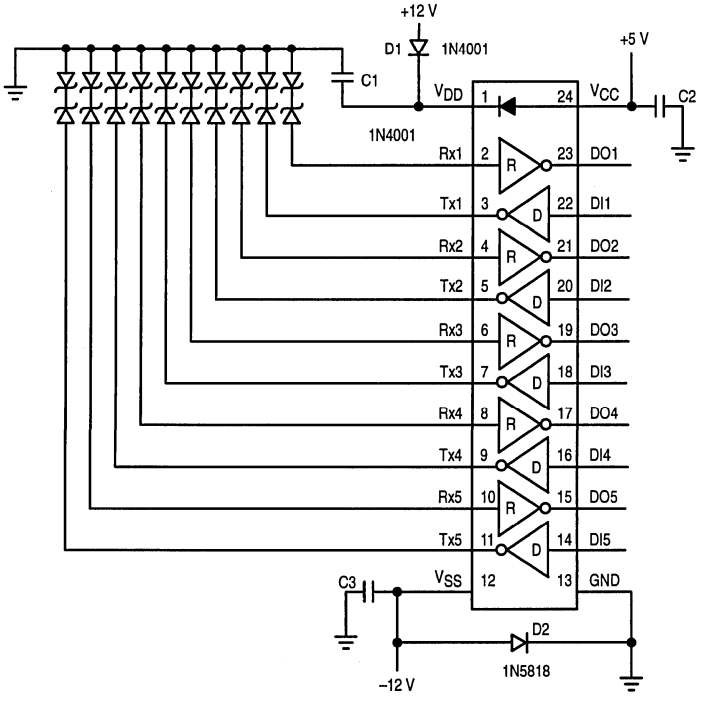


Figure 4.

MC145406

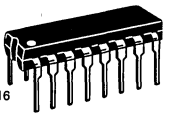
Driver/Receiver

EIA-232-E and CCITT V.28 (Formerly RS-232-D)

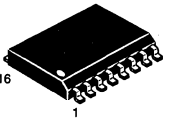
The MC145406 is a silicon-gate CMOS IC that combines three drivers and three receivers to fulfill the electrical specifications of standards EIA-232-E and CCITT V.28. The drivers feature true TTL input compatibility, slew-rate-limited output, 300-Ω power-off source impedance, and output typically switching to within 25% of the supply rails. The receivers can handle up to ±25 V while presenting 3 to 7 kΩ impedance. Hysteresis in the receivers aids reception of noisy signals. By combining both drivers and receivers in a single CMOS chip, the MC145406 provides efficient, low-power solutions for EIA-232-E and V.28 applications.

Drivers
- ±5 V to ±12 V Supply Range
- 300-Ω Power-Off Source Impedance
- Output Current Limiting
- TTL Compatible
- Maximum Slew Rate = 30 V/µs

Receivers
- ±25 V Input Voltage Range When V_{DD} = 12 V, V_{SS} = −12 V
- 3 to 7 kΩ Input Impedance
- Hysteresis on Input Switchpoint

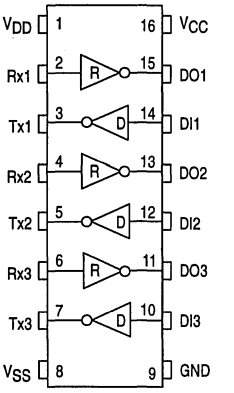


P SUFFIX
PLASTIC
CASE 648



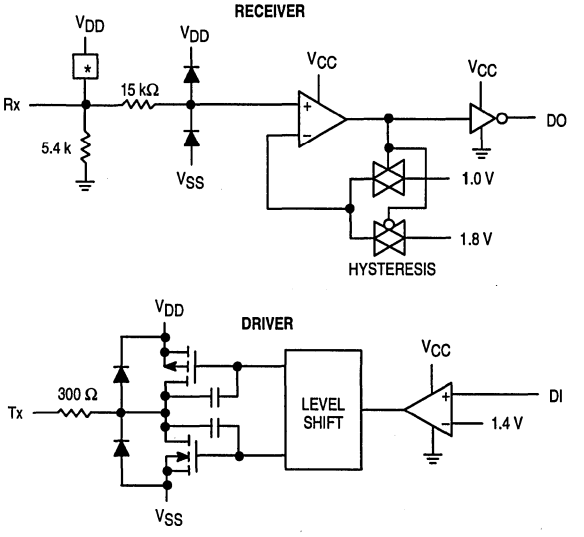
DW SUFFIX
SOG
CASE 751G

PIN ASSIGNMENT



D = DRIVER
R = RECEIVER

FUNCTION DIAGRAM



*Protection circuit

MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltages ($V_{DD} \geq V_{CC}$)	V_{DD} V_{SS} V_{CC}	− 0.5 to + 13.5 + 0.5 to − 13.5 − 0.5 to + 6.0	V
Input Voltage Range Rx1-3 Inputs DI1-3 Inputs	V_{IR}	 (V_{SS} − 15) to (V_{DD} + 15) − 0.5 to (V_{CC} + 0.5)	V
DC Current Per Pin		± 100	mA
Power Dissipation	P_D	1.0	W
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Rate	T_{stg}	− 85 to + 150	°C

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range $GND \leq V_{DI} \leq V_{CC}$ and $GND \leq V_{DO} \leq V_{CC}$. Also, the voltage at the Rx pin should be constrained to $(V_{SS} - 15\ V) \leq V_{Rx1-3} \leq (V_{DD} + 15\ V)$, and Tx should be constrained to $V_{SS} \leq V_{Tx1-3} \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI and Ground for Rx.)

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V, T_A = − 40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage					V
V_{DD}	V_{DD}	4.5	5 to 12	13.2	
V_{SS}	V_{SS}	−4.5	−5 to −12	−13.2	
V_{CC} ($V_{DD} \geq V_{CC}$)	V_{CC}	4.5	5.0	5.5	
Quiescent Supply Current (Outputs unloaded, inputs low)					µA
V_{DD} = +12 V	I_{DD}	—	140	400	
V_{SS} = −12 V	I_{SS}	—	340	600	
V_{CC} = +5 V	I_{CC}	—	300	450	

RECEIVER ELECTRICAL SPECIFICATIONS
(Voltage polarities referenced to GND = 0 V, V_{DD} = +5 to +12 V, V_{SS} = −5 to −12 V, $V_{DD} \geq V_{CC}$, T_A = −40 to +85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Turn-on Threshold $V_{DO1-DO3} = V_{OL}$, V_{CC} = 5.0 V ±5%	Rx1–Rx3	V_{on}	1.35	1.80	2.35	V
Input Turn-off Threshold $V_{DO1-DO3} = V_{OH}$, V_{CC} = 5.0 V ±5%	Rx1–Rx3	V_{off}	0.75	1.00	1.25	V
Input Threshold Hysteresis V_{CC} = 5.0 V ±5%	Rx1–Rx3	V_{on}–V_{off}	0.6	0.8	—	V
Input Resistance (V_{SS} −15 V) ≤ $V_{Rx1-Rx3}$ ≤ (V_{DD} + 15 V)	Rx1–Rx3	R_{in}	3.0	5.4	7.0	kΩ
High-Level Output Voltage ($V_{Rx1-Rx3}$ = −3 V to (V_{SS} − 15 V))*	DO1–DO3	V_{OH}				V
I_{OH} = −20 µA, V_{CC} = +5.0 V			4.9	4.9	—	
I_{OH} = −1 mA, V_{CC} = +5.0 V			3.8	4.3	—	
Low-Level Output Voltage ($V_{Rx1-Rx3}$ = +3 V to (V_{DD} + 15 V))*	DO1–DO3	V_{OL}				V
I_{OL} = +20 µA, V_{CC} = +5.0 V			—	0.01	0.1	
I_{OL} = +2 mA, V_{CC} = +5.0 V			—	0.02	0.5	
I_{OL} = +4 mA, V_{CC} = +5.0 V			—	0.5	0.7	

*This is the range of input voltages as specified by EIA-232-E to cause a receiver to be in the high or low logic state.

ELECTRICAL SPECIFICATIONS (Voltage polarities referenced to GND = 0 V, V_{CC} = + 5 V ± 5%, T_A = − 40 to +85°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Digital Input Voltage DI1–DI3					V
Logic 0	V_{IL}	—	—	0.8	
Logic 1	V_{IH}	2.0	—	—	
Input Current DI1–DI3	I_{in}	—	—	±1.0	μA
$V_{DI1-DI3} = V_{CC}$					
Output High Voltage (V_{DI1-3} = Logic 0, R_L = 3.0 kΩ) Tx1–Tx3	V_{OH}				V
V_{DD} = +5.0 V, V_{SS} = −5.0 V		3.5	3.9	—	
V_{DD} = +6.0 V, V_{SS} = −6.0		4.3	4.7	—	
V_{DD} = +12.0 V, V_{SS} = −12.0 V		9.2	9.5	—	
Output Low Voltage* (V_{DI1-3} = Logic 1, R_L = 3.0 kΩ) Tx1–Tx3	V_{OL}				V
V_{DD} = +5.0 V, V_{SS} = −5.0 V		−4.0	−4.3	—	
V_{DD} = +6.0 V, V_{SS} = −6.0 V		−4.5	−5.2	—	
V_{DD} = +12.0 V, V_{SS} = −12.0 V		−10.0	−10.3	—	
Off Source Resistance (Figure 1) Tx1–Tx3		300	—	—	Ω
$V_{DD} = V_{SS}$ = GND = 0 V, $V_{Tx1-Tx3}$ = ±2.0 V					
Output Short-Circuit Current (V_{DD} = +12.0 V, V_{SS} = −12.0 V) Tx1–Tx3	I_{SC}				mA
Tx1–Tx3 shorted to GND**		—	±22	±60	
Tx1–Tx3 shorted to ±15.0 V***		—	±60	±100	

* The voltage specifications are in terms of absolute values.

** Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits will be exceeded.

*** This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = +5 V ±5%, T_A = −40 to +85°C; See Figures 2 and 3)

Drivers

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Tx1–Tx3					ns
Low-to-High					
R_L = 3 kΩ, C_L = 50 pF	t_{PLH}	—	300	500	
High-to-Low	t_{PHL}				
R_L = 3 kΩ C_L = 50 pF		—	300	500	
Output Slew Rate Tx1–Tx3	SR				V/μs
Minimum Load					
R_L = 7 kΩ, C_L = 0 pF, V_{DD} = +6 to +12 V, V_{SS} = −6 to −12 V		—	±9	±30	
Maximum Load					
R_L = 3 kΩ, C_L = 2500 pF					
V_{DD} = +12 V, V_{SS} = −12 V		4	—	—	
V_{DD} = +5 V, V_{SS} = −5 V		—	—	—	

Receivers (C_L = 50 pF)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time DO1–DO3					ns
Low-to-High	t_{PLH}	—	150	425	
High-to-Low	t_{PHL}	—	150	425	
Output Rise Time DO1–DO3	t_r	—	250	400	ns
Output Fall Time DO1–DO3	t_f	—	40	100	ns

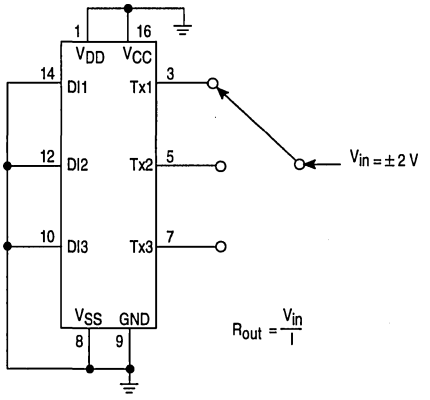


Figure 1. Power-Off Source Resistance (Drivers)

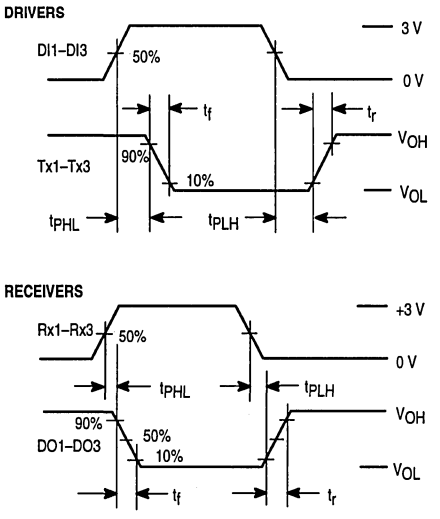


Figure 2. Switching Characteristics

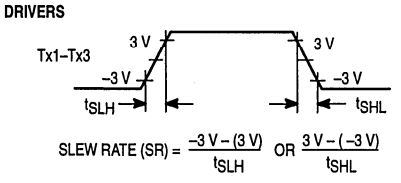


Figure 3. Slew Rate Characterization

PIN DESCRIPTIONS

V_{DD}
Positive Power Supply (Pin 1)
The most positive power supply pin, which is typically +5 to +12V.

V_{SS}
Negative Power Supply (Pin 8)
The most negative power supply pin, which is typically –5 to –12 V.

V_{CC}
Digital Power Supply (Pin 16)
The digital supply pin, which is connected to the logic power supply (maximum +5.5 V). V_{CC} ***must*** be less than or equal to V_{DD}.

GND
Ground (Pin 9)
Ground return pin is typically connected to the signal ground pin of the EIA-232-E connector (Pin 7) as well as to the logic power supply ground.

Rx1, Rx2, Rx3
Receive Data Input (Pins 2, 4, 6)
These are the EIA-232-E receive signal inputs whose voltages can range from (V_{DD} + 15 V) to (V_{SS} – 15 V). A voltage between +3 and (V_{DD} + 15 V) is decoded as a space and causes the corresponding DO pin to swing to ground (0 V); a voltage between –3 and (V_{DD} – 15 V) is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8 V above ground, and includes 800mV of hysteresis for noise rejection. The nominal input impedance is 5 kΩ. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.

DO1, DO2, DO3
Data Output (Pins 11, 13, 15)
These are the receiver digital output pins, which swing from V_{CC} to GND. A space on the Rx pin causes DO to produce a logic 0; a mark produces a logic 1. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3
Data Input (Pins 10, 12,14)
These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4 V above GND. However, 5-V CMOS compatibility is maintained as well. Input voltage levels on these pins must be between V_{CC} and GND.

Tx1, Tx2, Tx3
Transmit Data Output(Pins 3, 5, 7)
These are the EIA-232-E transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic 1 at a DI input causes the corresponding Tx output to swing toward V_{SS}. A logic 0 causes the output to swing toward V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30 V per µs. When the MC145406 is off (V_{DD} = V_{SS} = V_{CC} = GND), the minimum output impedance is 300 Ω.

APPLICATIONS INFORMATION

The MC145406 has been designed to meet the electrical specifications of standards EIA-232-E and CCITT V.28. EIA-232-E defines the electrical and physical interface between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). A DCE is connected to a DTE using a cable that typically carries up to 25 leads. These leads, referred to as interchange circuits, allow the transfer of timing, data, control, and test signals. Electrically this transfer requires level shifting between the TTL/CMOS logic levels of the computer or modem and the high voltage levels of EIA-232-E, which can range from ±3 to ±25 V. The MC145406, provides the necessary level shifting as well as meeting other aspects of the EIA-232-E specification.

DRIVERS

As defined by the specification, an EIA-232-E driver presents a voltage of between ±5 to ±15 V into a load of between 3 to 7 kΩ. A logic 1 at the driver input results in a voltage of between −5 to −15 V. A logic 0 results in a voltage between +5 to +15 V. When operating V_{DD} and V_{SS} at ±7 to ±12 V, the MC145406 meets this requirement. When operating at ±5 V, the MC145406 drivers produce less than ±5 V at the output (when terminated), which does not meet EIA-232-E specification. However, the output voltages when using a ±5 V power supply are high enough (around ±4 V) to permit proper reception by an EIA-232-E receiver, and can be used in applications where strict compliance to EIA-232-E is not required.

Another requirement of the MC145406 drivers is that they withstand a short to another driver in the EIA-232-E cable. The worst-case condition that is permitted by EIA-232-E is a ±15 V source that is current limited to 500 mA. The MC145406 drivers can withstand this condition momentarily. In most short circuit conditions the source driver will have a series 300 Ω output impedance needed to satisfy the EIA-232-E driver requirements. This will reduce the short circuit current to under 40 mA which is an acceptable level for the MC145406 to withstand.

Unlike some other drivers, the MC145406 drivers feature an internally-limited output slew rate that does not exceed 30 V per μs.

RECEIVERS

The job of an EIA-232-E receiver is to level-shift voltages in the range of −25 to +25 V down to TTL/CMOS logic levels (0 to +5 V). A voltage of between −3 and −25 V on Rx1 is defined as a mark and produces a logic 1 at DO1. A voltage between +3 and +25 V is a space and produces a logic zero. While receiving these signals, the Rx inputs must present a resistance between 3 and 7 kΩ. Nominally, the input resistance of the Rx1–Rx3 inputs is 5.4 kΩ.

The input threshold of the Rx1–Rx3 inputs is typically biased at 1.8 V above ground (GND) with typically 800 mV of hysteresis included to improve noise immunity. The 1.8 V bias forces the appropriate DO pin to a logic 1 when its Rx input is open or grounded as called for in the EIA-232-E specification. Notice that TTL logic levels can be applied to the Rx inputs in lieu of normal EIA-232-E signal levels. This might be helpful in situations where access to the modem or computer through the EIA-232-E connector is necessary with TTL devices. However, it is important not to connect the EIA-232-E outputs (Tx1–Tx3) to TTL inputs since TTL operates off +5 V only, and may be damaged by the high output voltage of the MC145406.

The DO outputs are to be connected to a TTL or CMOS input (such as an input to a modem chip). These outputs will swing from V_{CC} to ground, allowing the designer to operate the DO and DI pins from digital power supply. The Tx and Rx sections are independently powered by V_{DD} and V_{SS} so that one may run logic at +5 V and the EIA-232-E signals at ±12 V.

POWER SUPPLY CONSIDERATIONS

Figure 4 shows a technique to guard against excessive device current.

The diode D1 prevents excessive current from flowing through an internal diode from the V_{CC} pin to the V_{DD} pin when $V_{DD} < V_{CC}$ by approximately 0.6 V. This high current condition can exist for a short period of time during power up/down. Additionally, if the +12 V supply is switched off while the +5 V is on and the off supply is a low impedance to ground, the diode D1 will prevent current flow through the internal diode.

The diode D2 is used as a voltage clamp, to prevent V_{SS} from drifting positive to V_{CC}, in the event that power is removed from V_{SS} (Pin 12). If V_{SS} power is removed, and the impedance from the V_{SS} pin to ground is greater than approximately 3 kΩ, this pin will be pulled to V_{CC} by internal circuitry causing excessive current in the V_{CC} pin.

If by design, neither of the above conditions are allowed to exist, then the diodes D1 and D2 are not required.

ESD PROTECTION

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply buses of the IC. This coupling will usually occur through the internal ESD protection diodes. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. Figure 4 shows a technique which will clamp the ESD voltage at approximately ±15 V using the MMVZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the capacitors C1–C3. This scheme has provided protection to the interface part up to ±10 kV, using the human body model test.

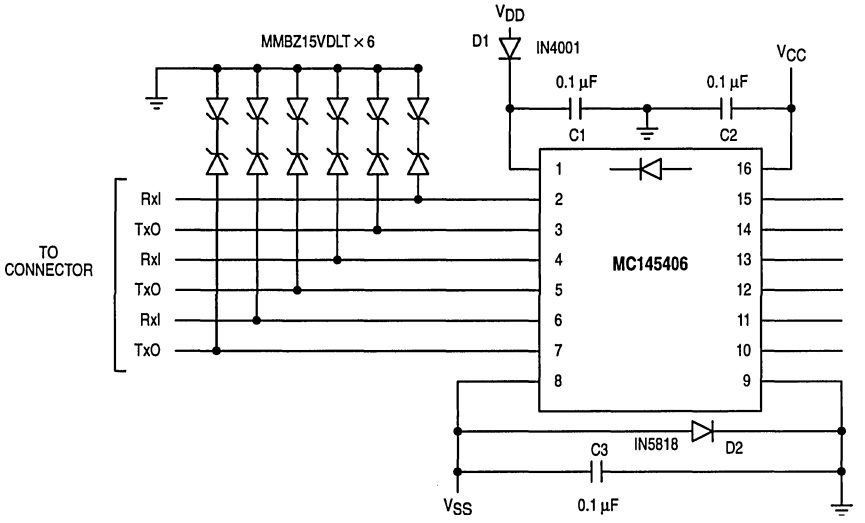


Figure 4. ESD and Power Supply Networks

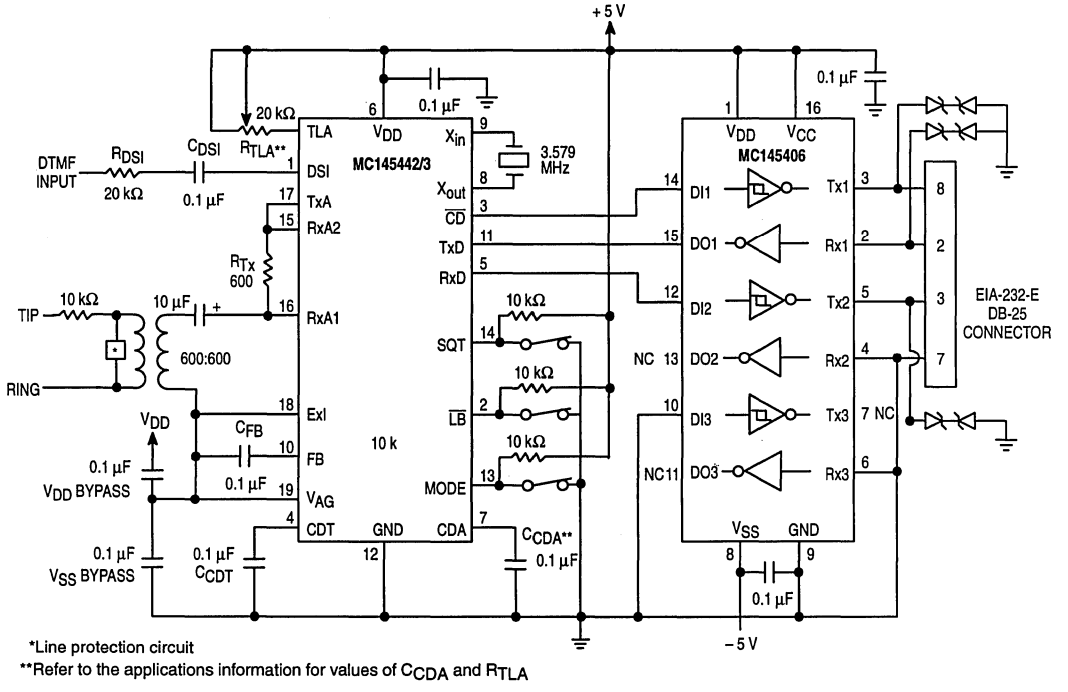


Figure 5. 5-V 300-Baud Modem with EIA-232-E Interface

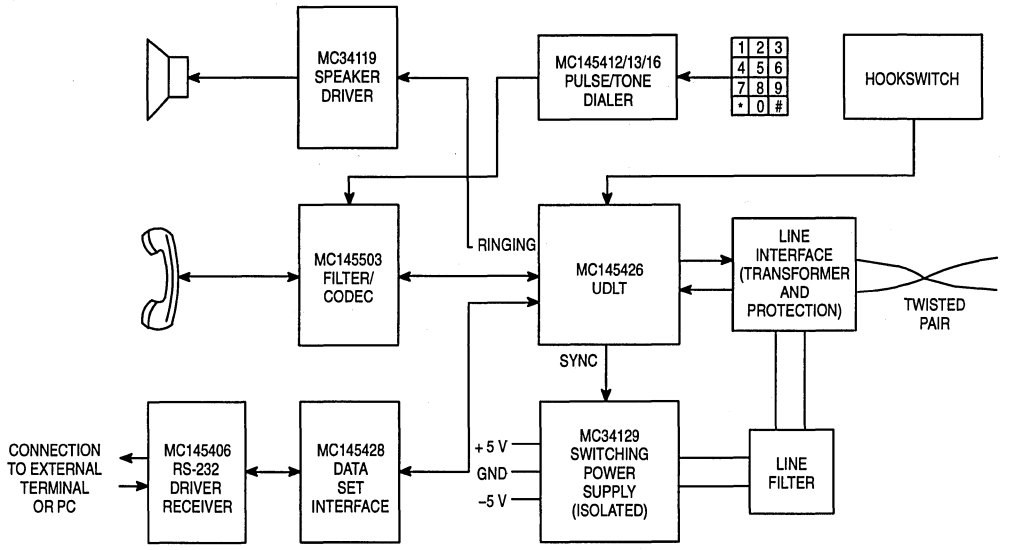


Figure 6. Line-Powered Voice/Data Telephone with Electrically Isolated EIA-232-E Interface

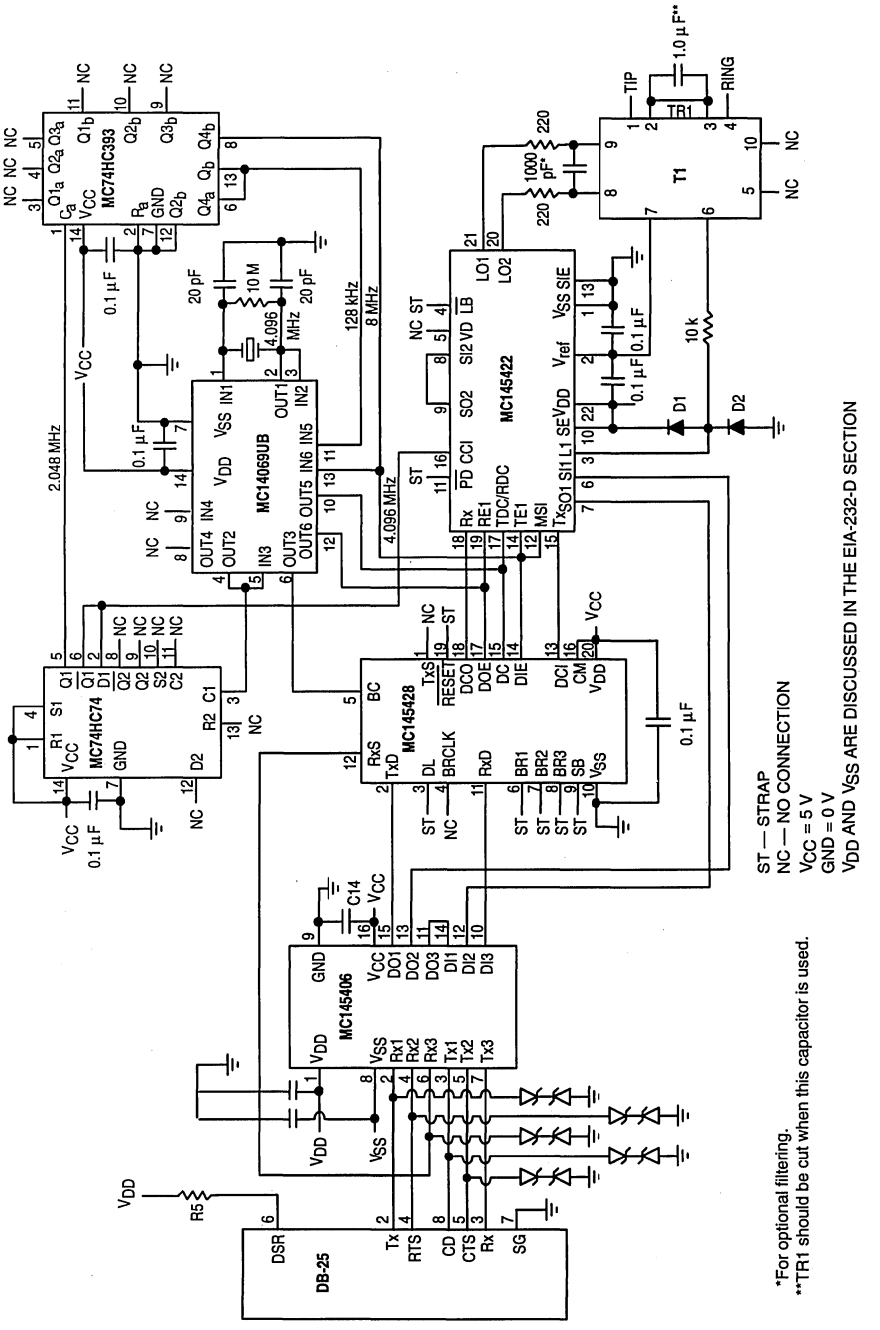


Figure 7. 80-kbps Limited Distance Modem with EIA-232-E Interface (Master)

MC145407

Advance Information

5-Volt-Only Driver/Receiver

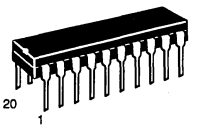
EIA-232-E and CCITT V.28

The MC145407 is a silicon-gate CMOS IC that combines three drivers and three receivers to fulfill the electrical specifications of EIA-232-E and CCITT V.28 while operating from a single +5 V power supply. A voltage doubler and inverter convert the +5 V to ±10 V. This is accomplished through an on-board 20-kHz oscillator and four inexpensive external electrolytic capacitors. The three drivers and three receivers of the MC145407 are virtually identical to those of the MC145406. Therefore, for applications requiring more than three drivers and/or three receivers, an MC145406 can be powered from an MC145407, since the MC145407 charge pumps have been designed to guarantee ± 5 V at the output of up to six drivers. Thus, the MC145407 provides a high-performance, low- power, stand-alone solution or, with the MC145406, a +5 V only, high-performance two-chip solution.

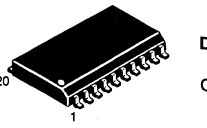
Drivers
- ±7.5 V Output Swing
- 300-Ω Power-Off Impedance
- Output Current Limiting
- TTL and CMOS Compatible Inputs
- Slew Rate Range Limited from 4 V/µs to 30 V/µs

Receivers
- +25 V Input Range
- 3 to 7 kΩ Input Impedance
- 0.8-V Hysteresis for Enhanced Noise Immunity

Charge Pumps
- +5 V to ±10 V Dual Charge Pump Architecture
- Supply Outputs Capable of Driving Three On-Chip Drivers and Three Drivers on the MC145406 Simultaneously
- Requires Four Inexpensive Electrolytic Capacitors
- On-Chip 20-kHz Oscillator

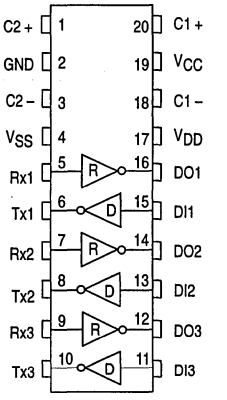


P SUFFIX
PLASTIC
CASE 738



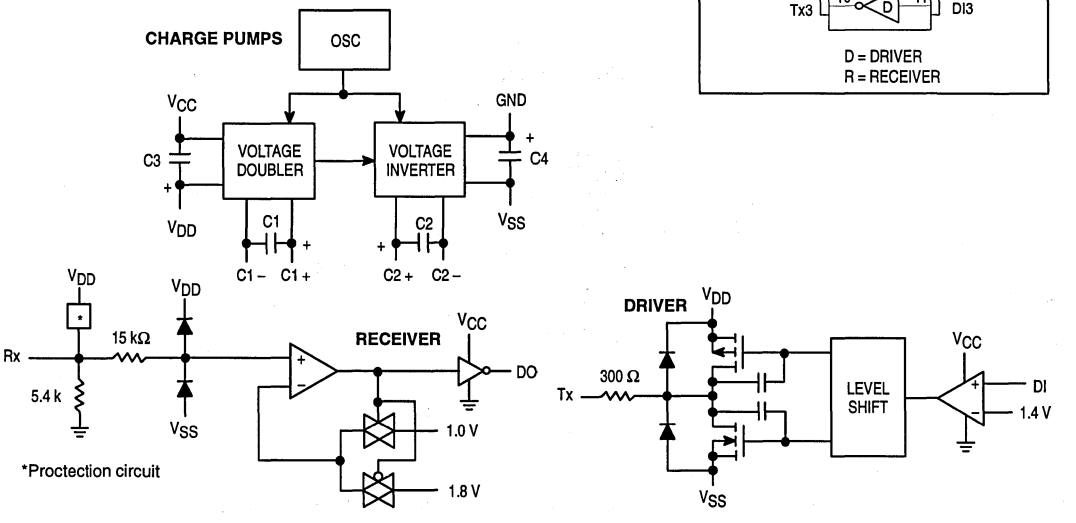
DW SUFFIX
SOG
CASE 751D

PIN ASSIGNMENT



D = DRIVER
R = RECEIVER

FUNCTION DIAGRAM



This document contains information on a new product. Specification and information herein are subject to change without notice.

MAXIMUM RATINGS (Voltage polarities referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltages	V_{CC}	−0.5 to 6.0	V
Input Voltage Range Rx1-Rx3 Inputs DI1–DI3 Inputs	V_{IR}	 V_{SS} − 15 to V_{DD} + 15 −0.5 to (VCC + 0.5)	V
DC Current Per Pin	I	± 100	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−85 to +150	°C

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that the voltages at the DI and DO pins be constrained to the range GND ≤ V_{DI} ≤ V_{CC} and GND ≤ V_{DO} ≤ V_{CC}. Also, the voltage at the Rx pin should be constrained to (V_{SS} − 15 V) ≤ $V_{Rx1-Rx3}$ ≤ (V_{DD} + 15 V), and Tx should be constrained to V_{SS} ≤ $V_{Tx1-Tx3}$ ≤ V_{DD}.

Unused inputs must always be tied to appropriate logic voltage level (e.g., GND or V_{CC} for DI, and GND for Rx.)

DC ELECTRICAL CHARACTERISTICS (All polarities referenced to GND = 0 V; C1, C2, C3, C4 = 10 µF; T_A = −40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{CC}	4.5	5	5.5	V
Quiescent Supply Current (Outputs unloaded, inputs low)	I_{CC}	—	1.2	3.0	mA
Output Voltage I_{load} = 0 mA	V_{DD}	8.5	10	11	V
I_{load} = 5 mA		7.5	9.5	—	
I_{load} = 10 mA		6	9	—	
I_{load} = 0 mA	V_{SS}	−8.5	−10	−11	
I_{load} = 5 mA		−7.5	−9.2	—	
I_{load} = 10 mA		−6	−8.6	—	

RECEIVER ELECTRICAL SPECIFICATIONS
(Voltage polarities referenced to GND = 0 V; V_{CC} = +5 V ±10%; C1, C2, C3, C4 = 10 µF; T_A = −40 to +85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Turn-on Threshold $V_{DO1-DO3} = V_{OL}$	Rx1–Rx3	V_{on}	1.35	1.8	2.35	V
Input Turn-off Threshold $V_{DO1-DO3} = V_{OH}$	Rx1–Rx3	V_{off}	0.75	1.0	1.25	V
Input Threshold Hysteresis ($V_{on} - V_{off}$)	Rx1–Rx3	V_{hys}	0.6	0.8	—	V
Input Resistance	Rx1–Rx3	R_{in}	3.0	5.4	7.0	kΩ
High-Level Output Voltage $V_{Rx1-Rx3}$ = −3 V to −25 V	DO1–DO3	V_{OH}				V
I_{OH} = −20 µA			V_{CC} − 0.1	—	—	
I_{OH} = −1 mA			V_{CC} − 0.7	4.3	—	
Low-Level Output Voltage $V_{Rx1-Rx3}$ = +3 V to +25 V	DO1–DO3	V_{OL}				V
I_{OL} = +20 µA			—	0.01	0.1	
I_{OL} = +1.6 mA			—	0.5	0.7	

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V: V_{CC} = +5 V ±10%; C1, C2, C3, C4 = 10 µF; T_A = −40 to +85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Digital Input Voltage	DI1–DI3					V
Logic 0		V_{IL}	—	—	0.8	
Logic 1		V_{IH}	2.0	—	—	
Input Current GND ≤ $V_{DI1-DI3}$ ≤ V_{CC}	DI1–DI3	I_{in}	—	—	±1.0	µA
Output High Voltage	Tx1–Tx3	V_{OH}	6	7.5	—	V
$V_{DI1-DI3}$ = Logic 0, R_L = 3.0 kΩ	Tx1–Tx6*		5	6.5	—	
Output Low Voltage	Tx1–Tx3	V_{OL}	−6	−7.5	—	V
$V_{DI1-DI3}$ = Logic 1, R_L = 3.0 kΩ	Tx1–Tx6*		−5	−6.5	—	
Off Source Impedance (Figure 1)	Tx1–Tx3	Z_{off}	300	—	—	Ω
Output Short-Circuit Current V_{CC} = +5.5 V	Tx1–Tx3	I_{SC}				mA
Tx1–Tx3 shorted to GND**			—	—	±60	
Tx1–Tx3 shorted to ± 15 V***			—	—	±100	

* Specifications for an MC145407 powering an MC145406 with three additional drivers/receivers.

** Specification is for one Tx output pin to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits could be exceeded.

*** This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = +5 V ±10%; C1, C2, C3, C4 = 10 µF; T_A = −40 to +85°C; See Figures 2 and 3)

Drivers

Characteristic		Symbol	Min	Typ	Max	Unit
Propagation Delay Time	Tx1–Tx3					µs
Low-to-High R_L = 3 kΩ, C_L = 50 pF or 2500 pF		t_{PLH}	—	0.5	1	
High-to-Low R_L = 3 kΩ, C_L = 50 pF or 2500 pF		t_{PHL}	—	0.5	1	
Output Slew Rate	Tx1–Tx3	SR				V/µs
Minimum Load: R_L = 7 kΩ, C_L = 0 pF			—	9.0	±30	
Maximum Load: R_L = 3 kΩ, C_L = 2500 pF			4.0	—	—	

Receivers (C_L = 50 pF)

Characteristic		Symbol	Min	Typ	Max	Unit
Propagation Delay Time	DO1–DO3					µs
Low-to-High		t_{PLH}	—	—	1	
High-to-Low		t_{PHL}	—	—	1	
Output Rise Time	DO1–DO3	t_r	—	250	400	ns
Output Fall Time	DO1–DO3	t_f	—	40	100	ns

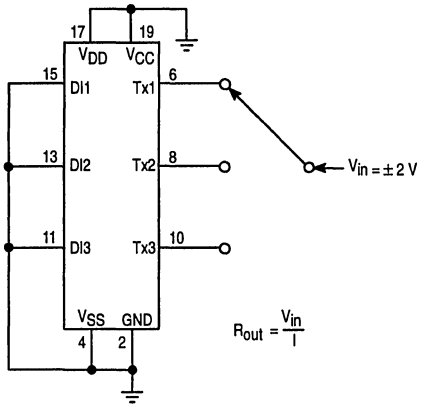


Figure 1. Power-Off Source Resistance

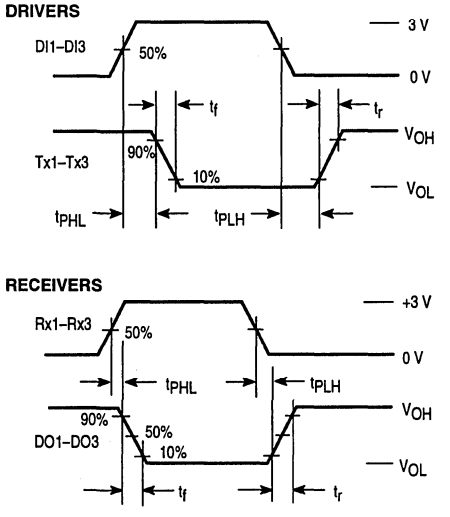


Figure 2. Switching Characteristics

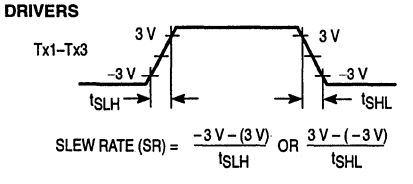


Figure 3. Slew Rate Characterization

PIN DESCRIPTIONS

V_{CC}
Digital Power Supply (Pin 19)

The digital supply pin, which is connected to the logic power supply. This pin should have a 0.33-µF capacitor to ground.

GND
Ground (Pin 2)

Ground return pin is typically connected to the signal ground pin of the EIA-232-E connector (Pin 7) as well as to the logic power supply ground.

V_{DD}
Positive Power Supply (Pin 17)

This is the positive output of the on-chip voltage doubler and the positive power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

V_{SS}
Negative Power Supply (Pin 4)

This is the negative output of the on-chip voltage doubler/ inverter and the negative power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

C2+, C2–, CI–, C1+
Voltage Doubler and Inverter (Pins 1, 3, 18, 20)

These are the connections to the internal voltage doubler and inverter, which generate the V_{DD} and V_{SS} voltages.

Rx1, Rx2, Rx3
Receive Data Input (Pins 5, 7, 9)

These are the EIA-232-E receive signal inputs. A voltage between +3 and +25 V is decoded as a space and causes the corresponding DO pin to swing to ground (0 V). A voltage between –3 and –25 V is decoded as a mark, and causes the DO pin to swing up to V_{CC}.

DO1, DO2, DO3
Data Output (Pins 16,14,12)

These are the receiver digital output pins, which swing from V_{CC} to GND. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3
Data Input (Pins 16,13,11)

These are the high-impedance digital input pins to the drivers. Input voltage levels on these pins must be between V_{CC} and GND.

Tx1, Tx2, Tx3
Transmit Data Output (Pins 6, 8, 10)

These are the EIA-232-E transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic 1 at a DI input causes the corresponding Tx output to swing toward V_{SS}. A logic 0 causes the output to swing toward V_{DD}. The actual levels and slew rate achieved will depend on the output loading (R_L || C_L).

APPLICATIONS INFORMATION

ESD CONSIDERATIONS

ESD protection on IC devices that have their pins accessible to the outside world is essential. High static voltages applied to the pins when someone touches them either directly or indirectly can cause damage to gate oxides and transistor junctions by coupling a portion of the energy from the I/O pin to the power supply busses of the IC. This coupling will usually occur through the internal ESD protection diodes. The key to protecting the IC is to shunt as much of the energy to ground as possible before it enters the IC. Figure 7 shows a technique which will clamp the ESD voltage at approximately + 15 V using the MMVZ15VDLT1. Any residual voltage which appears on the supply pins is shunted to ground through the 0.1-μF capacitors.

OPERATION WITH SMALLER VALUE CHARGE PUMP CAPS

The MC145407 is characterized in the electrical tables using 10-μF charge pump caps to illustrate its capability in driving a companion MC145406 or MC145403. If there is no requirement to support a second interface device and/or the charge pump is not being used to power any other components, the MC145407 is capable of complying with EIA–232-E and V.28 with smaller value charge pump caps. Table 1 summarizes driver performance with both 2.2-μF and 1.0-μF charge pump caps.

Table 1. Typical Performance

Parameter	2.2 μF	1.0 μF
Tx V_{OH} @ 25°C	7.3	7.2
Tx V_{OH} @ 85°C	7.2	7.1
Tx V_{OL} @ 25°C	– 6.5	– 6.4
Tx V_{OL} @ 85°C	– 6.1	– 6.0
Tx Slew Rate @ 25°C	8.0 V/μs	8.0 V/μs
Tx Slew Rate @ 85°C	7.0 V/μs	7.0 V/μs

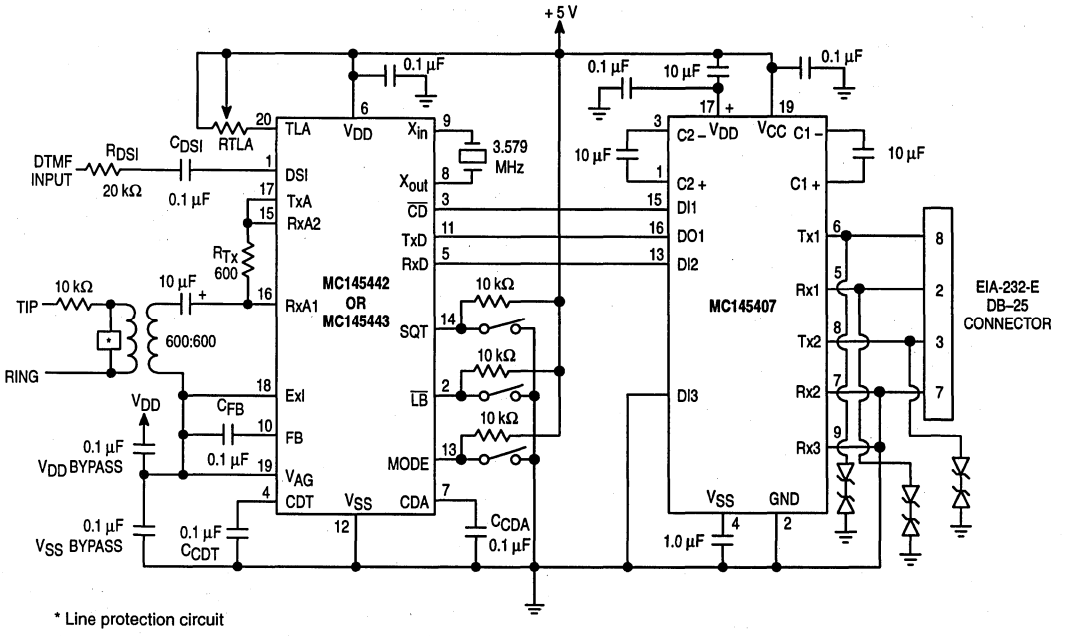


Figure 4. 5-V, 300-Baud Modem with EIA-232-E Interface

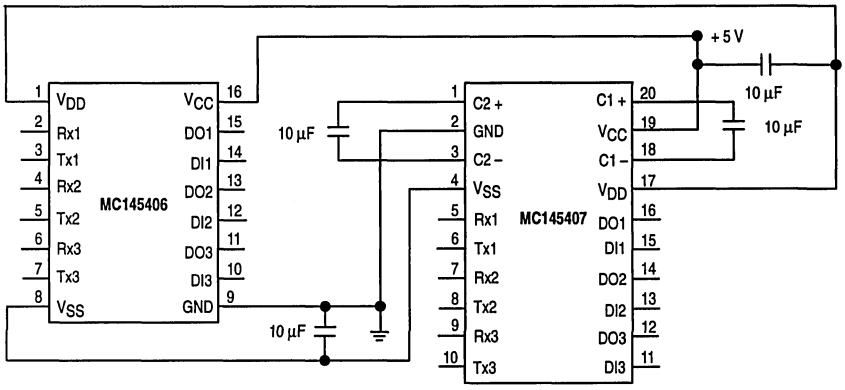


Figure 5. MC145406/MC145407 5-V Only Solution for up to Six EIA-232-E Drivers and Receivers

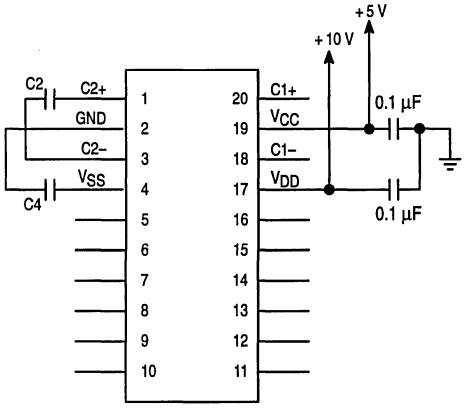


Figure 6. Two Supply Configuration (MC145407 Generates V_{SS} Only)

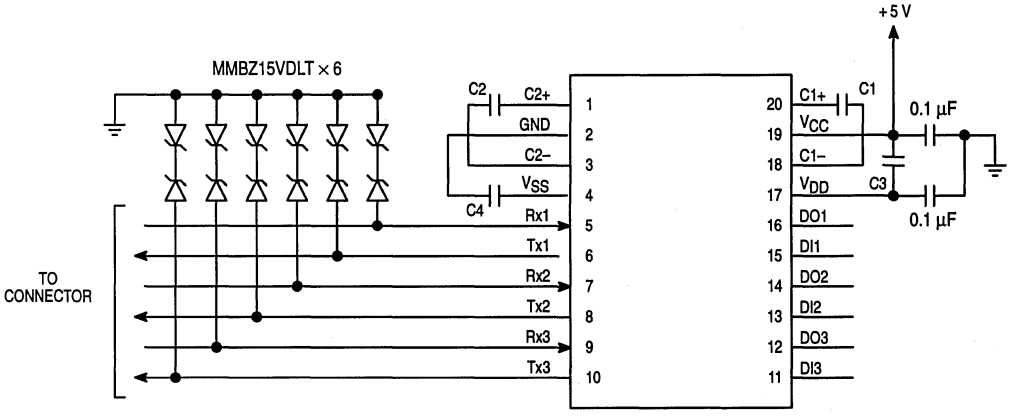
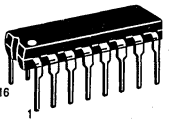


Figure 7. ESD Protection Scheme

MC145411

Bit Rate Generator



P SUFFIX
PLASTIC
CASE 648

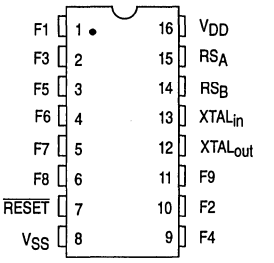
The MC145411 bit rate generator is constructed with complementary MOS enhancement mode devices. It utilizes a frequency divider network to provide a wide range of output frequencies.

A crystal controlled oscillator is the clock source for the network. A two-bit address is provided to select one of four multiple output clock rates.

Applications include a selectable frequency source for equipment in the data communications market, such as teleprinters, printers, CRT terminals, and microprocessor systems.

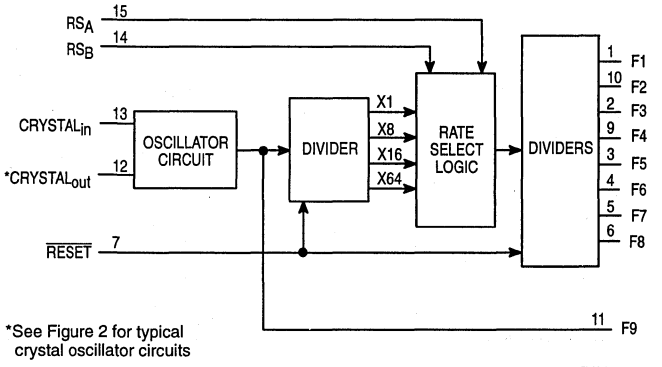
- Single 5-V (±5%) Power Supply
- Internal Oscillator Crystal Controlled for Stability (to 4 MHz)
- 21 Different Bit Rates
- 9 Different Bit Rate Output Pins
- Programmable Time Bases for One of Four Multiple Output Rates
- 50% Output Duty Cycle
- Buffered Outputs Compatible with Low Power TTL
- Noise Immunity = 45% of V_{DD} Typical
- Diode Protection on All Inputs
- External Clock May be Applied to Pin 13
- Internal Pull-up Resistor on Reset Input

PIN ASSIGNMENT



NOT
RECOMMENDED
FOR NEW DESIGN

BLOCK DIAGRAM



*See Figure 2 for typical crystal oscillator circuits

**When Reset = 0, outputs F1–F8 = 0, output F9 = 1.

V_{DD} = PIN 16
V_{SS} = PIN 8

MC145412
MC145413
MC145512

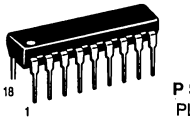
Advance Information

Pulse/Tone Repertory Dialer

Low Power Silicon-Gate CMOS

The MC145412/13 and MC145512 are silicon gate, monolithic CMOS intergrated circuits which convert keyboard inputs into either pulse or DTMF outputs. They are packaged in a standard 18-pin (0.3″ wide) plastic DIP.

- 3 × 4 or 4 × 4 Keyboard Compatibility Which Allows the Use of 2-of-7, 2-of-8, or Form A Type Keyboards
- MC145413 Adds Keyboard Selectable Pause Switch Function
- Single Pin Switchable Between DTMF, 10 pps and 20 pps
- 500-Hz Tone Signal Output in the Pulse Dialing Mode
- Memory Storage for Ten 18-Digit Numbers, Including Last Number Redial
- Uses 3.579545-MHz Colorburst Crystal
- Telephone Line Powered
- Silicon Gate CMOS Technology for 1.7 to 5.5 V Low Power Operation
- Stand Alone DTMF Dialer/Stand Alone Pulse Dialer
- Mute Output Used to Isolate Receiver from Dialing Output
- Memory Programming Options by Keyboard Configuration

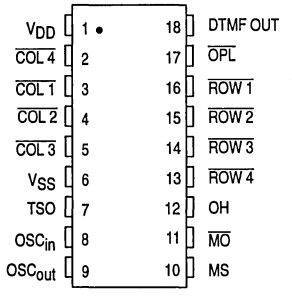


P SUFFIX
PLASTIC
CASE 707

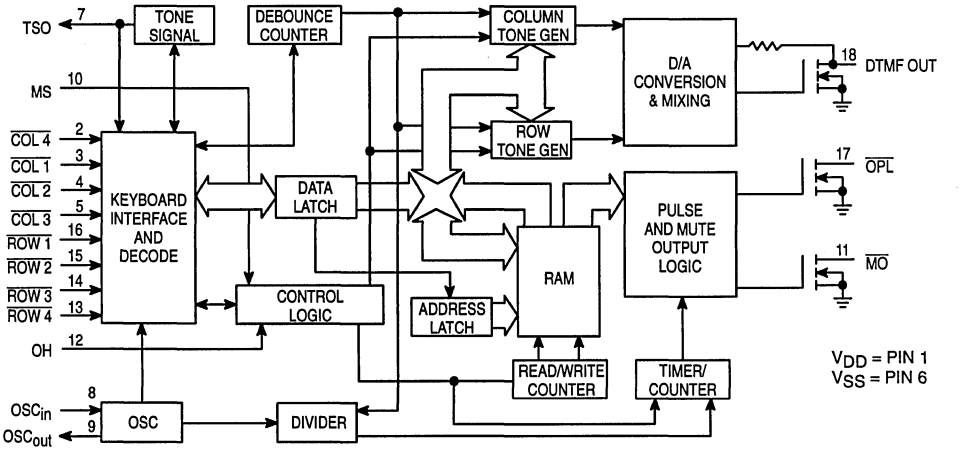
ORDERING INFORMATION

MC1454XX_	Suffix	Denotes
	P	Plastic DIP
	4	40/60 M/B Ratio
	5	32/68 M/B Ratio

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specification and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 8.0	V
Operating Temperature	T_A	– 30 to + 60	°C
Storage Temperature	T_{stg}	– 65 to + 150	°C
DC Current Drain Per Pin	I	10	mA
Maximum Voltage On Any Pin Relative to V_{SS} On Any Pin Relative to V_{DD}	 V_{in1} V_{in2}	 – 0.5 + 0.5	V

ELECTRICAL CHARACTERISTICS (T_A= –30 to +60°C, V_{DD} = 2.5 V, V_{SS} = 0 V, Unless Otherwise Noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DC Supply Voltage	Pulse Mode DTMF Mode	V_{DD}	2.0 2.5	— —	5.5 5.5	V
Operating Current	Pulse Mode (MS = V_{DD}) DTMF Mode (MS = V_{SS})	I_{DD}	— —	0.25 1.0	0.7 2.0	mA
Memory Retention Voltage		V_{stby}	1.7	—	—	V
Memory Retention Current	(V_{DD} = 1.7 V) (V_{DD} = 2.5 V)	I_{stby}	— —	1.0 1.2	2.0 2.5	µA
Input Voltage, Row/Column/OH	"0" Level "1" Level	V_{IL} V_{IH}	— 0.8 V_{DD}	— —	0.2 V_{DD} —	V
Row Column Input Impedance	To V_{DD} To V_{SS}	Z_{in}	— —	100 2	— —	kΩ
OH Pull-Up Resistance		R	—	50	—	kΩ
Input Capacitance (All Inputs)		C_{in}	—	10	—	pF
MS Pin Input Impedance		Z_{in}	50	200	—	kΩ
Output Sink Current	(V_{DD} = 2.5 V) TSO Pin $\overline{MO}$ Pin $\overline{OPL}$ Pin (V_{DD} = 4.0) $\overline{MO}$ Pin $\overline{OPL}$ Pin	I_{OL}	0.5 1.0 1.0 3.0 4.5	0.7 2.0 2.0 — —	— — — — —	mA
TSO Output Source Current (V_{out} = 2.0 V)		I_{OH}	0.5	0.7	—	mA
Output Leakage Current	$\overline{MO}$, $\overline{OPL}$ Pins	I_{lkg}	—	—	1.0	µA
DTMF Output Level Referenced to V_{DD}/2 (V_{DD} = 2.5 to 4.0 V, R_L= 600 Ω to V_{DD})	Row Tone Column Tone	V_{out}	260 330	310 390	370 460	mVrms
DTMF Output Tone Leakage (V_{DD} = 3.5, R_L = 600 Ω, 300 to 4000 Hz)			—	—	–80	dBm
DTMF Output Tone Distortion (V_{DD} = 3.5, R_L = 600 Ω, 300 to 4000 Hz)			—	—	5	%
Pre-Emphasis			1	2	2.5	dB
DTMF Output Leakage Current While Not Dialing Tones (V_{DD} = 2.5 V)			—	—	1.0	µA
DTMF Output Sink Current While Dialing Tones			20	—	—	µA

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{DD} = 2.5 V, Osc. Freq.= 3.579545 MHz, Unless Otherwise Noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Row/Column Scan Frequency		f	—	250	—	Hz
Key Debounce Time		t_{DB}	16	—	20	ms
DTMF Tone Duration for Keypad Dialing		t_{w1}	60	78	—	ms
DTMF Tone Duration for Memory Dialing		t_{w2}	90	102	110	ms
Inter-Digit Pause Time	DTMF (Memory Dialing)	t_{ID}	90	98	110	ms
	Pulse 10 pps		0.8	1.0	1.2	s
	20 pps		0.4	0.5	0.6	
MS Pin Scan Rate		t_{rms}	—	1	—	kHz
Make/Break Ratio	MC145412/13	MBR	—	40/60	—	%
(MC = Open or V_{DD})	MC145512		—	32/68	—	
Outpulsing Rate	MS = Open	f_{OPL}	—	10	—	pps
	MS = V_{DD}		—	20	—	
MUTE Output ($\overline{MO}$) Overlap Time		t_{MO}	—	2	—	ms
TSO Output Frequency		f_{TSO}	—	500	—	Hz
TSO Output Duration		t_{TSO}	35	—	40	ms
DTMF Cycle Time	(Memory Dialing		—	5	—	tones/s
	(Keypad Dialing)		—	10	—	
DTMF Frequency Deviation			—	—	+1.0	%
Predigit Mute		t_d				ms
MC145412/13	Pulse 10 pps		—	40	—	
	20 pps		—	20	—	
MC145512	Pulse 10 pps		—	32	—	
	20 pps		—	16	—	
	DTMF		—	1	—	

PIN DESCRIPTIONS

V_{DD}, V_{SS}
Power Supply (Pins 1, 6)

DC power is supplied to the part on these two pins, with V_{DD} being the most positive. Permissible ranges are from 1.7 to 5.5 V.

MS
Mode Select (Pin 10)

The MS pin is a three-state input for switching between DTMF, 10 pps, and 20 pps dialing modes. Mode selection is done during the first key entry debounce period after the dialer has completed a dialing sequence or has just come off hook. When this pin is not scanned it is high impedance.

This pin is a combination input and weak output. The input circuitry has the capability to determine each of these three states. When the pin is open, the weak driver will be able to clock the pin at 1 kHz. The relationship between pin input voltage and operating mode is shown in Table 1.

Table 1. Mode Select Options

MS	Dialing Mode
V_{DD}	20 pps Pulse Dialing
Open	10 pps Pulse Dialing
V_{SS}	DTMF Dialing

OH
On-Hook (Pin 12)

Connecting the OH pin to V_{DD} or allowing it to float sets the device in the On-hook mode. Connecting this pin to V_{SS} selects the Off-hook mode. When in the On-hook mode, repertory memory can be programmed without a dialing output.

TSO
Tone Signal Output (Pin 7)

TSO emits 500-Hz tone signals after valid key inputs are accepted providing audio feedback for key depressions (except when DTMF tones are generated). This pin also outputs a tone during on-hook programming.

DTMF OUT
Dual Tone Multifrequency Output (Pin 18)

When the MS pin is set to V_{SS} the DTMF OUT pin outputs tones corresponding to the row and column of the key depressed. Simultaneously depressing two or more keys in a single row (or column) will generate the corresponding row (or column) tone on 4 x 4 keypad mode only.

In pulse dialing mode (MS = V_{DD} or float) and during on-hook programming this pin is high impedance. While outputting tones, this pin has a dc bias at $(V_{DD} - V_{SS})/2$. DTMF OUT is an open-drain output requiring an external pull-up to V_{DD}. This pull-up resistor must satisfy the instantaneous current requirements of the internal feedback network in addition to the load applied to the pin.

$\overline{OPL}$
Outpulsing (Pin 17)

This pin outputs pulses at 10 pps (MS is open) or 20 pps (MS = V_{DD}). The MC145412/13 have a make/break ratio of 40/60, while the MC145512 has a make/break ratio of 32/68. In the DTMF dialing mode (MS = V_{SS}), this output is high impedance. During on-hook programming this pin will not outpulse. This pin is an open drain N-channel output which pulls low to break the loop current.

$\overline{MO}$
Mute Output (Pin 11)

The Mute Output is an open drain N-channel output that pulls to V_{SS} during $\overline{OPL}$ outpulsing and during off-hook key depressions and memory dialing in DTMF mode.

$\overline{COL\ 1}$–$\overline{COL\ 4}$ and $\overline{ROW\ 1}$–$\overline{ROW\ 4}$
KEYBOARD INPUTS (Pins 2, 3, 4, 5, 13, 14, 15, 16)

The keyboard inputs allow either a single contact (Class A) keyboard, or a standard 2-of-8 or 2-of-7 keyboard with V_{SS} tied to common. A valid key entry occurs when either a single row is tied to a single column, or a single row and column are simultaneously connected to V_{SS}. Connecting pin 2, $\overline{COL\ 4}$, to V_{DD} sets the part to 3 x 4 keyboard mode. Keyboard mode selection is performed during application of power.

Typical keyboard configurations are shown in Figure 1.

OSC_{in}, OSC_{out}
Oscillator Input and Oscillator Output (Pins 8, 9)

A 3.579545-MHz crystal is required as the frequency reference for the on-chip oscillator. Crystal biasing is accomplished by an internal resistor and capacitors.

GENERAL DEVICE DESCRIPTION

The MC145412/MC145512 and the MC145413 provide users with switchable pulse and DTMF dialing functions. The MC145412/MC145512 change dialing modes via the MS pin. The MC145413 allows users to switch dialing modes via the keyboard in addition to the MS pin. All devices have 10 memories, LNR (last number redial) inclusive, each 18 digits long.

On application of power, there is a 64-ms initialization period during which the oscillator is enabled and the keyboard inputs are disabled. During initialization $\overline{COL\ 4}$ is scanned to set the keyboard mode. If the $\overline{COL\ 4}$ input is high (V_{DD}), the dialer is set to the 3 × 4 keypad mode; otherwise, the 4 × 4 keypad mode is selected. Changing modes is not possible after this initialization period.

During normal dialing, the oscillator starts when a key is depressed. The key input is debounced for 32 ms. During this debounce period the RAM and dialing circuits are disabled and the mode select pin is scanned to determine the dialing mode (either 10 pps, 20 pps, or DTMF). After debounce, the keypad entry is checked and the input is latched into LNR memory followed by a stop code. This process continues until 18 digits have been entered. If a 19th digit is entered, it will over-write the first digit and will be followed by a stop code. When dialing, the device fetches data from memory until a stop code is encountered or 18 digits have been dialed.

During manual DTMF dialing, a minimum tone duration of 60-ms DTMF is output and will continuously output in 32-ms increments as long as the key is depressed. The DTMF OUT pin is designed to drive an external PNP transistor which can be used to modulate tip and ring voltage at the DTMF frequencies.

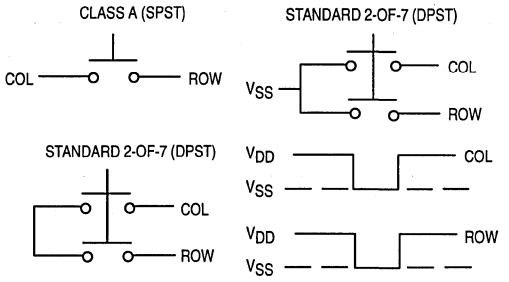


Figure 1. Keyboard Configurations

If the first key is for redial or recall, the device will respond accordingly, either redialing the last number entered, or recalling and dialing the number selected by a subsequent key depression. Responses to dialing sequences for 4 × 4 key-boards are shown in Figure 2, and 3 × 4 keyboard responses are shown in Figure 3.

The MC145412 series can be configured with an external battery to provide memory retention power and allow on-hook programming of the repertory memory. If the part is in the on-hook mode and a key is depressed, the oscillator will start and the key entry will be stored in the last number redial memory. Dialing outputs will not be activated while the device is in the on-hook condition. Dialing inputs will be stored in last number redial memory, as during off-hook operation. After the number has been entered in the on-hook mode, it can be stored in repertory memory. For the 4 × 4 keyboard, pressing the STORE key (* for 3 × 4 keyboard), followed by a digit (1 through 9) will store the number in the repertory memory location specified by the digit.

The RECALL key for the 4 × 4 keypad is used to recall and dial numbers stored in the repertory memory. The digit immediately following the RECALL key designates the memory location of the number to be auto-dialed. For the 4 × 4 keyboard, a last number redial can be accomplished if the RED/P key ($\overline{COL\ 4}$, $\overline{ROW\ 1}$) is the first key depressed after an on-hook to off-hook transition. Otherwise the RED/P key will effect a 4 second pause. If the pulse mode is selected, redial can be accomplished if the first key depressed on a transition to off-hook is #. For the 3 × 4 keyboard, redial occurs if the first key depressed is *,0.

The PAUSE key ($\overline{COL\ 4}$, $\overline{ROW\ 2}$) for the MC145412/MC145512 will cause a 4 second pause. The PAUSE/S key ($\overline{COL\ 4}$, $\overline{ROW\ 2}$) is a feature offered on the MC145413. Depressing this key will cause a 4 second delay, and will switch dialing modes, PAUSE (and PAUSE/S) is stored in memory for pauses (and mode switching) during auto-dialing.

1. **MANUAL DIALING — OFF-HOOK** (PULSE OF DTMF MODE)

D1 D2 D3 — — — — DN

ALL DIGITS ENTERED WILL BE STORED IN THE LAST NUMBER REDIAL REGISTER. PRESSING * OR # WILL DIAL OUT THE DTMF SIGNAL IN TONE MODE ONLY.

2. **MANUAL DIALING WITH AUTO ACCESS PAUSE — OFF-HOOK** (PULSE OR DTMF MODE)

D1 ▪▪▪▪▪ DN RED/P DX ▪▪▪▪▪ DY

D1 ▪▪▪▪▪ DN PAUSE DX ▪▪▪▪▪ DY MC145412/MC145512 ONLY

D1 ▪▪▪▪▪ DN * DX ▪▪▪▪▪ DY PULSE MODE ONLY

THE AUTO ACCESS PAUSE WILL NOT OCCUR DURING MANUAL DIALING IN DTMF MODE. IT IS RETRIEVED DURING RECALL OR REDIAL.

3. **STORING NUMBERS INTO MEMORY — ON-HOOK/OFF-HOOK** (PULSE OR DTMF MODE)

D1 ▪▪▪▪▪ DN STORE A A = 1–9 MEMORY ADDRESS

THIS OPERATION TRANSFERS THE DIGITS D1 TO DN FROM THE LAST NUMBER REDIAL REGISTER TO AN ADDRESS SPACE SPECIFIED BY "A". DIALING OUTPUTS ARE NOT ACTIVATED DURING ON-HOOK PROGRAMING

4. **MEMORY REDIAL — OFF-HOOK** (PULSE OR DTMF MODE)

RECALL A A = 1–9 MEMORY ADDRESS

5. **LAST NUMBER REDIAL — OFF-HOOK** (PULSE OR DTMF MODE)

RED/P

OR

PULSE MODE ONLY

REDIALS THE NUMBER THAT WAS PREVIOUSLY ENTERED INTO THE LAST NUMBER REDIAL REGISTER.

6. **PULSE-TO-TONE MODE SWITCH — OFF-HOOK** (PULSE OR DTMF MODE)

D1 ▪▪▪▪▪ DN PAUSE/S DX ▪▪▪▪▪ DY MC145413 ONLY

7. **CASCADED DIALING — OFF-HOOK** (PULSE OR DTMF MODE)

D1 ▪▪▪▪▪ DN //// RECALL A — CASCADE MANUAL DIALING WITH RECALL
A = 1–9 MEMORY ADDRESS

RECALL A1 //// RECALL A2 — CASCADE MEMORY RECALLS
A1, A2 = 1–9 MEMORY ADDRESSES

RED/P //// RECALL A — CASCADE LAST NUMBER REDIAL WITH MEMORY RECALL
A = 1–9 MEMORY ADDRESS

//// WAIT UNTIL PREVIOUS REDIAL OR RECALL SIGNALS HAVE BEEN SENT BEFORE SUBSEQUENT ENTRIES ARE MADE.

8. **SIGNALING * AND # TONES — OFF-HOOK** (DTMF MODE ONLY)

* OUTPUTS * TONE

\# OUTPUTS # TONE

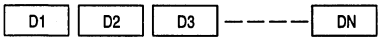
4 X 4 KEY MATRIX

	COL 1	COL 2	COL 3	COL 4	
697 Hz	1	2	3	RED/P	ROW 1
770 Hz	4	5	6	PAUSE	ROW 2
852 Hz	7	8	9	STORE	ROW 3
941 Hz	*	0	#	RECALL	ROW 4
	1209 Hz	1336 Hz	1477 Hz		

MC145413 PAUSE/S KEY FOR PAUSE & SWITCHING DIALING MODES

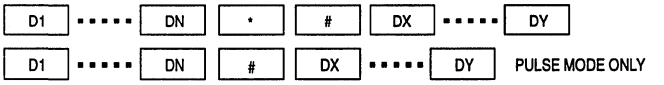
Figure 2. 4 × 4 Keyboard Dialing Sequences

1. **MANUAL DIALING — OFF-HOOK** (PULSE OF DTMF MODE)



ALL KEY ENTRIES EXCEPT * AND # WILL BE STORED IN THE LAST NUMBER REDIAL REGISTER. PRESSING * OR # WILL NOT DIAL OUT THE DTMF SIGNAL IN TONE MODE. FOR SIGNALING, * OR # SHOULD BE PRESSED TWICE.

2. **MANUAL DIALING WITH AUTO ACCESS PAUSE — OFF-HOOK** (PULSE OR DTMF MODE)

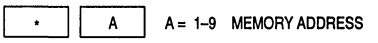


THE AUTO ACCESS PAUSE WILL NOT OCCUR ON MANUAL DIALING IN DTMF MODE. IT IS RETRIEVED DURING RECALL OR REDIAL.

3. **STORING NUMBERS INTO MEMORY — ON-HOOK** (PULSE OR DTMF MODE)

THIS OPERATION TRANSFERS THE DIGITS D1 TO DN FROM THE LAST NUMBER REDIAL REGISTER TO AN ADDRESS SPACE SPECIFIED BY "A".

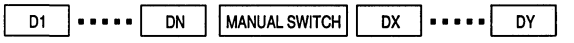
4. **MEMORY REDIAL — OFF-HOOK** (PULSE OR DTMF MODE)



5. **LAST NUMBER REDIAL — OFF-HOOK** (PULSE OR DTMF MODE)

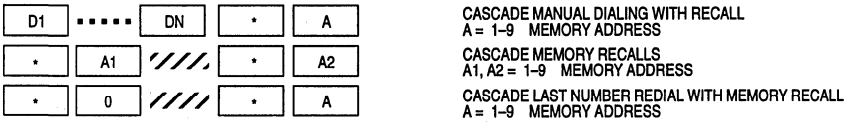
THIS OPERATION REDIALS THE LAST NUMBER ENTERED OFF-HOOK AND RETRIEVES DATA FROM MEMORY ADDRESS 0.

6. **PULSE-TO-TONE MODE SWITCH — OFF-HOOK** (PULSE OR DTMF MODE)



MODE SELECT (MS) PIN HAS TO BE MANUALLY SWITCHED TO DETERMINE THE DIALING MODE. DIALING MODE SELECTION WITH MANUAL SWITCH IS NOT PROGRAMMED INTO THE LAST NUMBER REDIAL MEMORY.

7. **CASCADED DIALING — OFF-HOOK** (PULSE OR DTMF MODE)



WAIT UNTIL PREVIOUS REDIAL OR RECALL SIGNALS HAVE BEEN SENT BEFORE SUBSEQUENT ENTRIES ARE MADE.

8. **SIGNALING * AND # TONES — OFF-HOOK** (DTMF MODE ONLY)

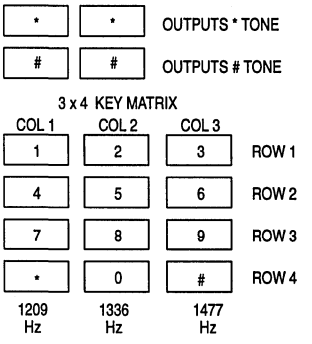


Figure 3. 3 × 4 Keyboard Dialing Sequences

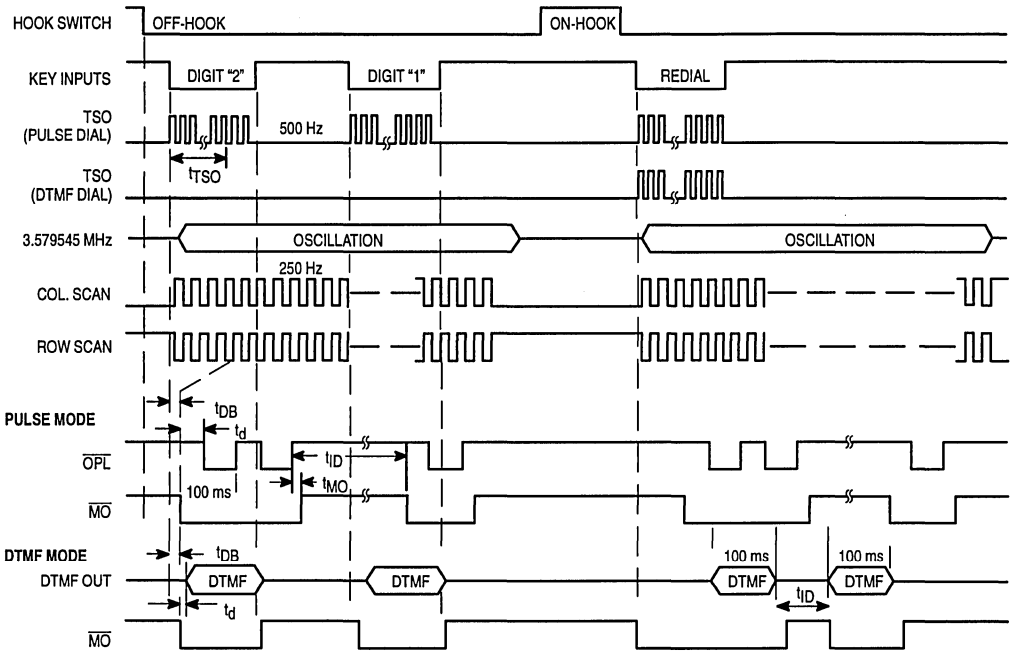


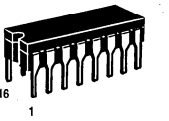
Figure 4. Timing Diagram

MC145414

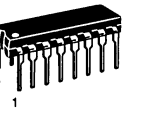
Dual Tunable Low-Pass Sampled Data Filters

The MC145414 is sampled data, switched capacitor filter IC intended to provide band limiting and signal restoration filtering. It is capable of operating from either a single or split power supply and can be powered-down when not in use. Included on the IC are two totally uncommitted op amps for use elsewhere in the system as I-to-V converters, gain adjust buffers, etc.

- Two General Purpose 5th Order Elliptic Low-Pass Filters
- Low Operating Power Consumption — 30 mW (Typical)
- Power Down Capability — 1 mW (Maximum)
- ±5 to ±8 V Power Supply Ranges
- TTL or CMOS Compatible Inputs Using V_{LS} Pin
- Two Operational Amplifiers Available to Reduce Component Count
- Useful in LPC or CVSD Speech Applications
- Passband Edges Tunable With Clock Frequency From 1.25 kHz to 10 kHz

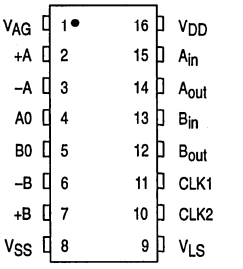


L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

PIN ASSIGNMENT

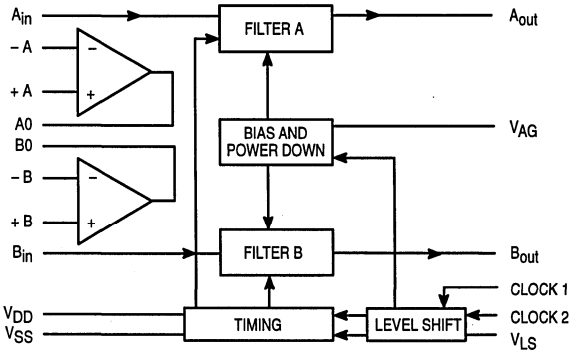


ORDERING INFORMATION

MC145414 — Suffix Denotes
- L Ceramic Package
- P Plastic Package

NOT
RECOMMENDED
FOR NEW DESIGN

BLOCK DIAGRAM



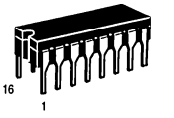
MC145415

Dual Tunable Linear Phase Low-Pass Sampled Data Filters

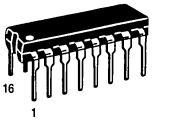
The MC145415 is sampled data, switched capacitor filter IC intended to provide band limiting and signal restoration filtering. It is capable of operating from either a single or split power supply and can be powered-down when not in use. Included on the IC are two uncommitted comparators for use elsewhere in the system.

- Two Linear Phase, 5th Order Low-Pass Filters
- Low Operating Power Consumption — 20 mW (Typical)
- ± 2.5 to ± 8 V Power Supply Ranges
- CMOS Compatible Inputs Using V_{DG} Pin
- Two Comparators Available to Reduce Component Count
- Useful in High Speed Data Modem Applications
- Pass-Band Edges Tunable With Clock Frequency from 1.25 kHz to 10 kHz

NOT RECOMMENDED FOR NEW DESIGN

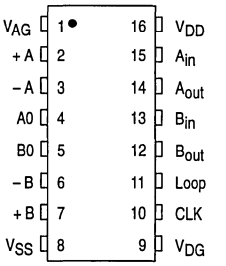


L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

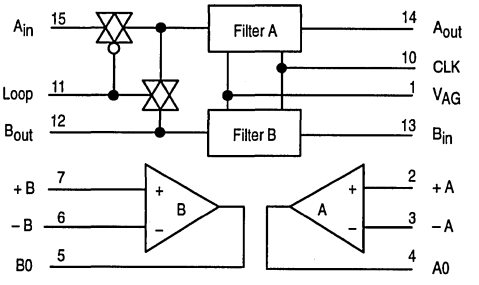
PIN ASSIGNMENT



ORDERING INFORMATION

MC145415 — Suffix	Denotes
L	Ceramic Package
P	Plastic Package

BLOCK DIAGRAM



V_{DG} = PIN 9
V_{DD} = PIN 16
V_{SS} = PIN 8

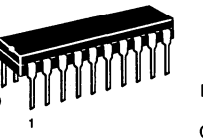
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

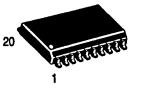
MC145416

Tone/Pulse Dialer with 10 Number Memory Plus 3 Emergency Numbers

Low-Power, Silicon-Gate CMOS



P SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOG
CASE 751D

The MC145416 is a member of the Motorola HCMOS dialer family. In addition to the necessary basic features of pulse, tone, or mixed dialing, and 10 × 18 digit memories inclusive of LNR, it provides the advanced features of flash, 3 × 18 dedicated memories, signal output inhibited during memory storage, note pad programming, and convenient operation sequence by 5 × 4 keyboard interface.

The power-on memory reset has the highest priority if the voltage drops below the minimum voltage level, regardless of hook switch status, to ensure no wrong data in memory content.

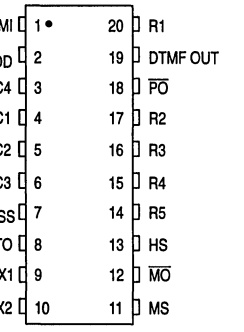
The pin-out is compatible with other members of dialer family except the additional two pins at one end of the device (pins 1 and 20).

Options: MC145416-1 40/60 make-break ratio with indefinite pause
MC145416-2 33/67 make-break ratio with 4-ms pause

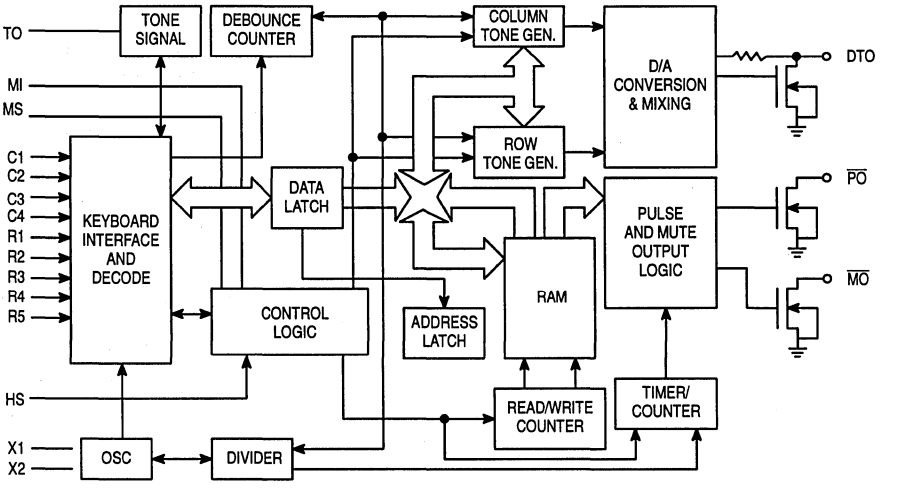
The MC145416 offers the following performance features:

- Stand-Alone Pulse, DTMF, or Mixed Dialing
- Pacifier Tone Output at Pulse Dialing
- Dialing Mode, Pin Selectable, and Changed by Keyboard Entry
- Uses Low Cost 3.57954-MHz TV Color Burst Crystal
- PABX Pause Storage
- Cascaded Memory Redial and Dialing Mode Storage
- Dialing Mode Indication Output for Driving an LED
- 10 × 8 Digit Memory Storage Inclusive of LNR plus 3 × 8 Digit Dedicated Memory
- 40/60 Make Break Ratio, 33/67 in Metal Option #
- Flash Function for Transfer Call in a PABX Environment

PIN ASSIGNMENT



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Voltages referenced to GND, except where noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +8.0	V
Input Voltage (All Pins)	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin	I	±10	mAdc
Power Dissipation	P_d	30	mW
Operating Temperature Range	T_A	−30 to +70	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS (All polarities referenced to V_{SS} = 0 V, V_{DD} = 2.5 V, Unless Otherwise Noted)

Parameter		Symbol	Min	Typ	Max	Unit
DC Supply Voltage	Pulse Mode DTMF Mode	V_{DD}	2.0 2.5	— —	6 6	V
Supply Current	Pulse Mode (V_{DD} = 1.7 V) DTMF MODE (V_{DD} = 2.5 V)	I_{DD}	— —	200 0.5	500 2.0	µA mA
Memory Retention Voltage (On-Hook)		V_{stby}	1.7	—	—	V
Memory Retention Current (On-Hook)	(V_{DD} = 2.5 V) (V_{DD} = 1.7 V)	I_{stby}	— —	— 0.05	2.5 2.0	µA
Row/Column (Pins 3, 4, 5, 6, 14, 15, 16, 17, 20) Input Voltage	"0" Level "1" Level	V_{IL} V_{IH}	— 0.8 × V_{DD}	— —	0.2 × V_{DD} —	V
Row/Column Input Impedance (Pins 3, 4, 5, 6, 14, 15, 16, 17, 20)	To V_{DD} To V_{SS}	R_{in}	— —	100 5	— —	kΩ
Mode Select Input Impedance (Pin 11)	To V_{DD} To V_{SS}	R_{in}	— —	100 100	— —	kΩ
OH Pull-Up Resistance (Pin 13)		R	—	50	—	kΩ
Input Current MS, HS (Pins 11, 13)		I_{in}	—	—	100	µA
Output Sink Current (V_O = 0.5 V)	$\overline{MO}$ (Pin 12) $\overline{PO}$ (Pin 18) MI (Pin 1)	I_{OL} I_{OL} I_{OH}	0.5 1.0 0.25	1.0 2.0 1.5	— — —	mA
Output Leakage Current (Pins 12, 18)		I_{out}	—	—	1.0	µA
Input Capacitance (All Pins)		C_{in}	—	10	—	pF
DTO Output Tone Level (Pin 19)	Row Tone (R_L = 600 Ω to V_{DD}) Column Tone (V_{DD} = 3.5 V)	V_O	260 327	309 389	367 462	mVrms
DTO Output Tone Leakage (Pin 19)	(V_{DD} = 3.5 V, RL = 600 Ω)	D_{bm}	—	—	−80	dBm
DTO Output Tone Distortion (Pin 19) (300 Hz–4 kHz, V_{DD} = 3.5 V, R_L = 600 Ω)			—	5	7	%
Output Ratio Column/Row Tone (Pins 3, 4, 5, 6, 14, 15, 16, 17, 20)	V_{DD} = 3.5 V	D_b	1.5	—	3.0	dB
DTO DC Level (Pin 19)		V_{tDC}	−10%	1/2 V_{DD}	+10%	

SWITCHING CHARACTERISTICS (V_{DD} = 2.5 V, C_L = 50 pF, t_A = 25°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Row/Column Scan Frequency		f	—	250	—	Hz
Key Debounce Time		t_{DB}	—	12 to 26		ms
HS Reset Time		t_R	—	160	—	ms
DTO Duration	Normal Redial	t_{DO}	80 80	— —	— —	ms
Flash Output Duration		t_{FO}	—	600	—	ms
DTO Interdigit Duration (Normal and Redial)		t_{ID}	60	—	—	ms
$\overline{MO}$ Output Predeigit (DTMF Mode)		t_{PDP}	—	40	—	ms
Pacifier Tone Frequency		f_{TSO}	—	800	—	Hz
Pacifier Tone Duration		t_{TSO}	30	—	—	ms
Pulse Interdigit Duration		t_{IDP}	—	800	—	ms
Make/Break	($\overline{P}$/$\overline{DW}$) ($\overline{P2}$/$\overline{DW2}$)	MBR	42/58	40/60 33/67	37/63	%
$\overline{MO}$ Overlap (Pulse Mode/Redial)		t_{MO}	—	800	—	ms
$\overline{MO}$ Output Predigit (Pulse Mode)		t_{MOP}	—	40	—	ms
Pause		t_P	3	—	5	s

PIN DESCRIPTIONS

V_{DD}
Positive Power Supply (Pin 2)
The digital supply pin is connected to the positive side of the system power supply.

V_{SS}
Ground (Pin 7)
Ground return pin is typically connected to the system ground.

MS
Mode Select (Pin 11)
This is a three-state input. A logic 0 selects Tone mode, a logic 1 selects the Pulse mode at 20 pps, and an open connection selects Pulse mode at 10 pps. If the input is changed while dialing is in progress, the mode change will occur after the last interdigit pause for the previous dial mode.

PTO
Pacifier Tone Output (Pin 8)
Recognition of any valid key input in Pulse mode will cause an 800-Hz square wave to be output from this pin. The minimum output time is 30 ms or as long as valid key depression lasts. This pin is high impedance when no signal is output.

HS
Hook Status (Pin 13)
A logic 1 or open condition sets the device on on-hook status. A logic 0 is an off-hook condition.

$\overline{PO}$
Pulse and Flash Output (Pin 18)
This is an N-channel open-drain output. It outputs dialing pulses at a 10-pps or 20-pps rate. The flash output from this pin is a 600-ms pulse. This pin is high impedance when no signal is output.

$\overline{MO}$
Mute Output (Pin 12)
This is an N-channel open-drain output. In the manual tone dialing mode this output goes low for the period of the tone duration. It will remain low until the end of the mute overlap time.

In manual pulse dialing, this output will go low for the period of break and make time, and will remain low until completion of the mute overlap time.

When redialing from LNR, or memory, this pin will go low starting with first digit signal output with predigit period, and will remain low until the last digit is output plus the overlap mute period. This pin remains high (1) during memory store.

R1–R5/C1–C4
Row/Column Inputs (Pins 3–6, 14–17, and 20)
A logic 0 simultaneously presented to a single row and a single column is defined as a valid key entry. The keypad starts to be sampled and the input accepted if it is still valid after 12 to 26 ms debounce time. Depression of multiple keys is an invalid entry.

X1/X2
OSC_{IN} and OSC_{OUT} (Pins 9 and 10)
An inverter works as an on-board oscillator when connected to a parallel mode 3.5795-MHz crystal. The frequency accuracy of the crystal directly affects the accuracy of the DTMF frequency. Crystal biasing is accomplished by an internal resistor and capacitors.

DTO
DTMF Output (Pin 19)
When the MS pin is set to a logic 0 (V_{SS}) the DTMF output pin will output tones corresponding to the row and column of the key depressed. The tone out duration will last as long as a valid key is pressed, with a minimum of 80 ms guaranteed.

In LNR the tone output and interdigit pause are of a fixed duration. When the MS pin is logic 1 or open for pulse dialing, the DTO pin is high impedance.

MI
Mode Indicator Output (Pin 1)
This pin will be at a logic 0 when dialing in the DTMF mode and a logic 1 when dialing in the Pulse mode. The pin remains in the logic state determined by the last dial mode.

OPERATIONAL INFORMATION

The MC145416 allows the use of either a single contact (Class A) keyboard, or a standard 2-of-8 keyboard with V_{SS} tied to common. A valid key entry occurs when either a single row is tied to a single column or a single row and column are simultaneously connected to V_{SS}.

Figure 1 illustrates the two types of keying methods.

Figure 2 illustrates the 4 × 5 functional keyboard layout and the standard row and column frequencies.

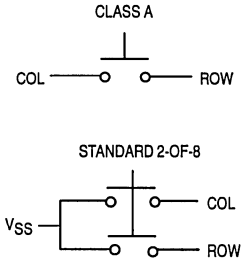


Figure 1. Keyboard Configurations

ROW FREQ.	COL1	COL2	COL3	COL4	
	N1	N2	N3	MR	ROW 1
697	1	2	3	MS	ROW 2
770	4	5	6	PS/S	ROW 3
852	7	8	9	FLASH	ROW 4
941	*	0	#	LNR/PS	ROW 5
	1209	1336	1477		

COLUMN FREQ.

MR = MEMORY RECALL
MS = MEMORY STORE
PS/S = MODE CHANGE/PAUSE
FLASH = 600 ms at PO PIN
LNR/PS = LAST NUMBER REDIAL/PAUSE

Figure 2. 4 × 5 Keyboard Matrix

FUNCTIONAL INFORMATION

A. **MANUAL DIALING — OFF-HOOK** [D1] ———— [DN]

1) Dialing Tone (DTMF) output will continue as long as a valid key is depressed.
2) Mode change can be set on- or off-hook before keyboard entry.
3) In Tone Mode
   a) All digits, including * and #, will have DTMF output.
   b) All digits, including * and #, and Pause will be stored in the LNR register.
   c) Flash, PS/S, MS (Memory Store), and MR (Memory Recall) will cause a PTO output to be generated as long as a key remains pressed.
4) In Pulse Mode (10 or 20 pps)
   a) Numeric Input 0–9, Pause, and PS/S will be stored in the LNR register.
   b) Numeric inputs 0–9, * and #, Flash, LNR, PS/S, MS, and MR will cause a PTO output to be generated for as long as the key remains pressed.

B. **LAST NUMBER REDIAL — OFF-HOOK** [LNR/PS]

1) When this is the first key depressed after off-hook, exluding Mode Select Switch, it causes the last number entered from the keypad to be dialed out.
2) Mixed dialing from the keypad can be stored and redialed with pulse to tone mixed dial out or can be converted to all tone with the Mode Select Switch, retaining the four second pause.

ENTERED ...
Mode Select Switch to Pulse Mode, ENTER: [D1] ▪▪▪▪▪ [D] [PS/S] [D] ▪▪▪▪▪ [DN]
PULSE INPUT | MODE | DTMF INPUT
Change With Pause

REDIALED ...
ON-HOOK to OFF-HOOK
Mode Select Switch in Pulse Mode, ENTER: [LNR/PS], Dial out is the same as original entry.

REDIALED ...
ON-HOOK to OFF-HOOK
Mode Select Switch in Tone Mode, ENTER: [LNR/PS], Dial out changes to:
[D1] ▪▪▪▪▪ [D] [D] ▪▪▪▪▪ [DN]
DTMF OUTPUT | PAUSE | DTMF OUTPUT

3) Numbers dialed from memory 1–9, and N1, N2, and N3 will not be stored in the LNR register.
4) Numbers stored with the MS pin set to DTMF cannot be converted to pulse with the PS/S key because the part does not know to go to 10 or 20 pps.

C. **DIALING WITH AUTO ACCESS PAUSE — OFF-HOOK**

ENTERED ...
Mode Switch in either Pulse or Tone Mode [D1] ▪▪▪▪▪ [D] [LNR/PS] [D] ▪▪▪▪▪ [DN]

REDIALED ...
ON-HOOK to OFF-HOOK
Mode Select Switch Unchanged, ENTER: [LNR/PS], Dial out is the same as original entry.
[D1] ▪▪▪▪▪ [D] PAUSE [D] ▪▪▪▪▪ [DN]

1) A pause is stored in a data number sequence by pressing the LNR/PS key during keypad entry.
2) More than one pause can be entered in sequence for extended pauses.
3) An indefinite pause duration can be provided with a custom metal option.
   a) The indefinite pause will not occur during normal tone or pulse dialing.
   b) On redial, this pause can be terminated by pressing any other key.

D. **DIALING WITH AUTO ACCESS PAUSE AND MODE CHANGE — OFF-HOOK**

ENTERED ...
Mode Select Switch in Pulse Mode (10 or 20 pps) [D1] ▪▪▪▪▪ [D] [PS/S] [D] ▪▪▪▪▪ [DN]
PULSE DIALING | MODE | TONE DIALING
Change With Pause

ENTERED ...
Mode Switch in Tone Mode [D1] ▪▪▪▪▪ [D] [PS/S] [D] ▪▪▪▪▪ [DN]
TONE DIALING | PAUSE | TONE DIALING
Change With Pause

1) Dialing in the Pulse Mode and depressing the PS/S key will initiate a four second auto access pause with the mode change to DTMF.
2) Starting in the Tone Mode, depressing the PS/S key will not cause a mode change to occur, but will insert a four second pause in the dial sequence.

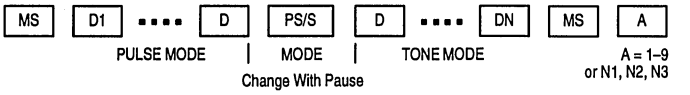
E. MEMORY STORAGE AND RECALL — OFF-HOOK

1) A total of 18 digits can be stored.
2) Pause and Mode Switch (PS/S) key each count as one digit.
3) After pressing MS (Memory Store) key, all outputs are inhibited except the PTO output. Succeeding numeric inputs including PS/S, are counted as data. Following the second MS (Memory Store) key input, the first numeric input is counted as address (A = 1–9 or N1, N2, or N3). Any non-numeric key entered, including 0, will be ignored, and the part will wait for another entry.

ENTERED ...

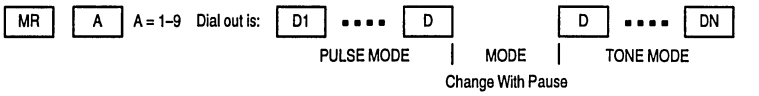
a) Mode Select Switch in Pulse Mode (10 or 20 pps)

Memory Store Sequence ...



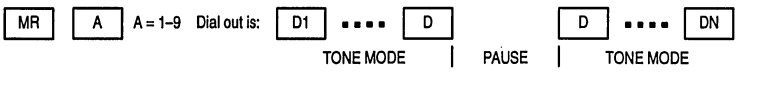
ON-HOOK to OFF-HOOK ENTERED ...

Memory Recall Sequence ...



b) Mode Select Switch to DTMF

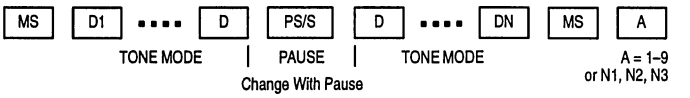
Memory Recall Sequence ...



ENTERED ...

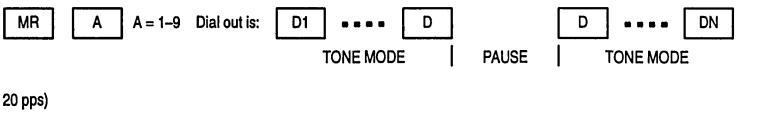
a) Mode Select Switch in Tone Mode

Memory Store Sequence ...



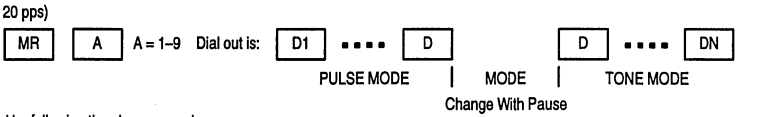
ON-HOOK to OFF-HOOK ENTERED ...

Memory Recall Sequence ...



b) Mode Select Switch in Pulse Mode (10 or 20 pps)

Memory Recall Sequence ...



4) Number storage during conversation is allowed by following the above procedure.
5) Memory registers can be programmed sequentially without going on-hook between each entry.

F. CASCADED DIALING — OFF-HOOK

1) Memory Cascaded ...

a) Numbers stored with the Mode Select Switch set to pulse (10 or 20 pps) can be dialed out as follows:

ENTERED ...	N1	N2		Both N1 and N2 will dial out as originally stored.
ENTERED ...	N1	PS/S	N2	N1 will dial out as stored, N2 will convert to DTMF. PTO output will remain active during the dial out of N2.
ENTERED ...	PS/S	N1	N2	Both N1 and N2 will dial out in DTMF, with PTO active.

b) Numbers stored with the Mode Select Switch set to pulse (10 or 20 pps) can also be dialed out in DTMF by switching the Mode Select Switch to the Tone Mode, on- or off-hook. By using the Mode Select Switch instead of PS/S, PTO will not be active. A dial out conversion back to pulse cannot be accomplished with the use of PS/S when the Mode Select Switch is in the Tone Mode.

c) In cascade operation, the keyboard is inhibited upon pressing the first key (i.e., N1 key). The out pulsing must be completed before acceptance of the next key input.

2) Cascade dialing can be accomplished from any memory location in any order, including LNR ...

a) Numbers stored with the Mode Select Switch set to pulse (10 or 20 pps)

ENTERED ...	MR	A	LNR	Both MR A and LNR dial out in pulse.
ENTERED ...	LNR	MR	A	Both LNR and MR A dial out in pulse

b) Since a redial from any memory location will not distrub the content of the LNR register, it is not necessary to re-enter the last dialed number again.

c) In cascade operation, the keyboard is inhibited upon pressing the first control key (i.e., MR key). The out pulsing must be completed before acceptance of the next control key input.

3) The second control key, or number input, has to be entered after completion of the previous dialing.

G. FLASH — OFF-HOOK FLH

1) Pressing the FLH key will cause a 600-ms pulse to be generated at the pulse output pin. This pulse ***will not*** be stored in either the LNR register or the memory registers. The mute output will go low for 600 ms and the PTO output will be active for as long as this key is depressed.

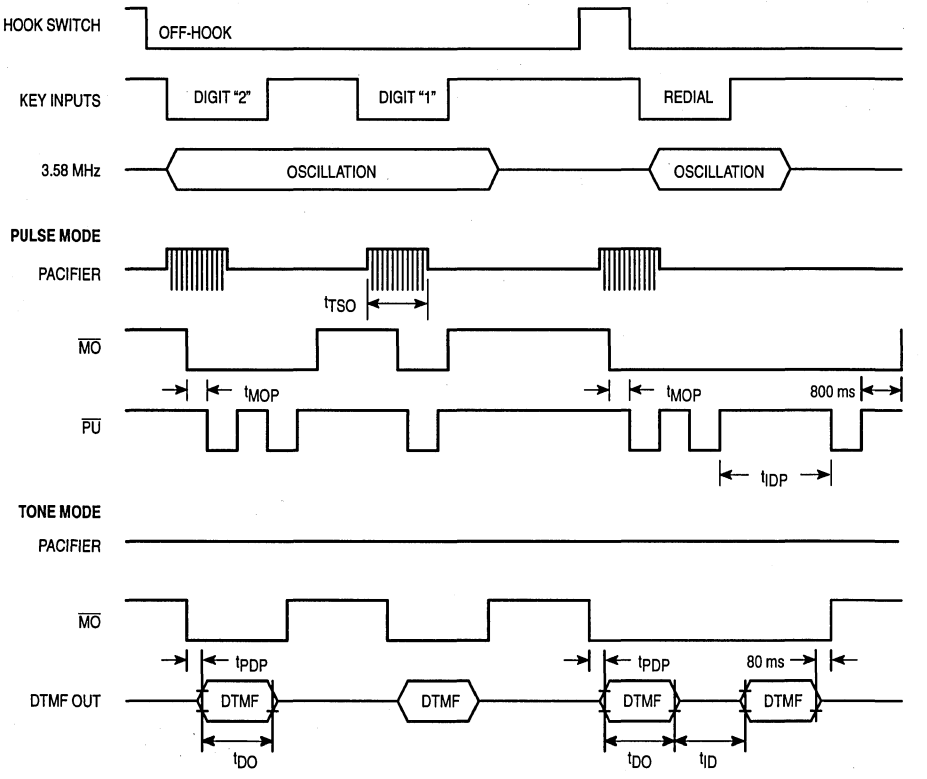
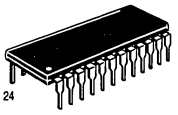


Figure 3. Timing Diagram

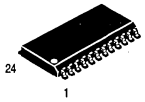
MC145421
MC145425

Advance Information

ISDN Universal Digital Loop Transceivers II
(UDLT II)



P SUFFIX
PLASTIC
CASE 709



DW SUFFIX
SOG
CASE 751F

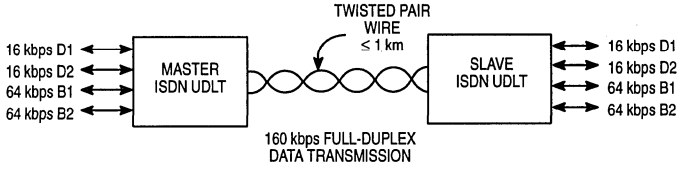
The MC145421 and MC145425 UDLTs are high-speed data transceivers capable of providing 160 kbps full-duplex data communication over 26 AWG and larger twisted-pair cable up to 1 km in length. These devices are primarily used in digital subscriber voice and data telephone systems. In addition, the devices meet and exceed the CCITT recommendations for data transfer rates of ISDNs on a single twisted pair. The devices utilize a 512 kbaud MDPSK burst modulation technique to supply the 160 kbps full-duplex data transfer rates. The 160 kbps rate is provided through four channels. There are two B channels, which are 64 kbps each. In addition, there are two D channels which are 16 kbps each.

The MC145421 and MC145425 UDLTs are designed for upward compatibility with the existing MC145422 and MC145426 80 kbps UDLTs, as well as compatibility with existing and evolving telephone switching hardware and software architectures.

The MC145421 (MASTER) UDLT is designed for use at the telephone switch line card while the MC145425 (SLAVE) UDLT is designed for use at the remote digital telset or data terminal.

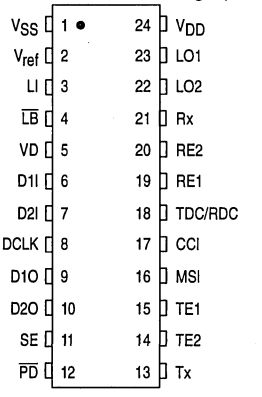
- Employs CMOS Technology, in Order to Take Advantage of Its Proven Capability for Complex Analog and Digital LSI Functions
- Provides Synchronous Full Duplex 160 kbps Voice and Data Communication in a 2B+2D Format for ISDN Compatibility
- Provides the CCITT Basic Access Data Transfer Rate (2B+D) for ISDNs on a Single Twisted Pair up to 1 km
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signalling Schemes
- Protocol Independent
- Single +5 V Power Supply

NOT RECOMMENDED FOR NEW DESIGN



PIN ASSIGNMENT

MC145421—Master
(Plastic and SOG Packages)



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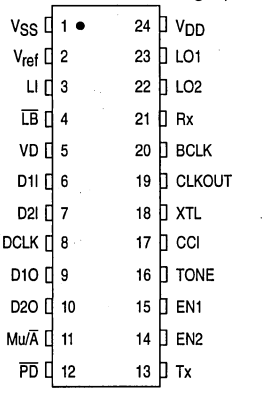
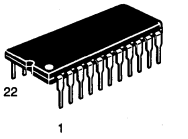


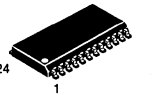
MC145422
MC145426

Advance Information

Universal Digital-Loop Transceivers (UDLT)



P SUFFIX
PLASTIC
CASE 708



DW SUFFIX
SOG
CASE 751E

ORDERING INFORMATION

MC145422P, MC145426P	Plastic
MC145422DW, MC145426DW	SOG

The MC145422 and MC145426 UDLTs are high-speed data transceivers that provide 80-kbps full-duplex data communication over 26 AWG and larger twisted pair cable up to two kilometers in distance. Intended primarily for use in digital subscriber voice/data telephone systems, these devices can also be used In remote data acquisition and control systems. These devices utilize a 256 kilobaud modified differential phase shift keying burst modulation technique for transmission to minimize RFI/EMI and crosstalk. Simultaneous power distribution and duplex data communication can be obtained using a single twisted pair wire.

These devices are designed for compatibility with existing, as well as evolving, telephone switching hardware and software architectures.

The UDLT chip-set consists of the MC145422 master UDLT for use at the telephone switch linecard and the MC145426 slave UDLT for use at the remote digital telset and/or data terminal.

The devices employ CMOS technology in order to take advantage of its reliable low-power operation and proven capability for complex analog/digital LSI functions.

- Provides Full Duplex Synchronous 64 kpbs Voice/Data Channel and Two 8 kbps Signaling Data Channels Over One 26 AWG Wire Pair Up to Two Kilometers
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signaling Schemes
- Automatic Detection Threshold Adjustment for Optimum Performance Over Varying Signal Attenuations
- Protocol Independent
- Single 5 V Power Supply
- 22-Pin Package
- Application Notes AN943, AN949, AN968, AN946, and AN948

NOT RECOMMENDED FOR NEW DESIGN

MC145422 Master UDLT

- Pin Controlled Power-Down and Loop-Back Features
- Signaling and Control I/O Capable of Sharing Common Bus Wiring with Other UDLTs
- Variable Data Clock — 64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of 8 kbps Channel into LSB of 64 kbps Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145426 Slave UDLT

- Compatible with MC145500 Series PCM Codec-Filters
- Pin Controlled Loop-Back Feature
- Automatic Power-Up/Down Feature
- On-Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications

This document contains information on a new product. Specifications and information herein are subject to change without notice.

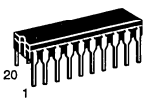
MC145428

Data Set Interface

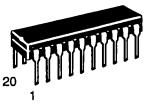
Asynchronous-to-Synchronous and Synchronous-to-Asynchronous Converter

The MC145428 Data Set Interface provides asynchronous-to-synchronous and synchronous-to-asynchronous data conversion. It is ideally suited for voice/data digital telsets supplying an EIA-232 compatible data port into a synchronous transmission link. Other applications include: data multiplexers, concentrators, data-only switching, and PBX-based local area networks. This low-power CMOS device directly interfaces with either the 64 kbps or 8 kbps channel of Motorola's MC145422 and MC145426 Universal Digital Loop Transceivers (UDLTs), as well as the MC145421 and MC145425 Second Generation Universal Digital Loop Transceivers (UDLT II).

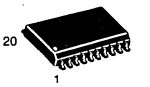
- Provides the Interface Between Asynchronous Data Ports and Synchronous Transmission Links
- Up to 128 kbps Asynchronous Data Rate Operation
- Up to 2.1 Mbps Synchronous Data Rate Operation
- On-Board Bit Rate Clock Generator with Pin Selectable Bit Rates of 300, 1200, 2400, 4800, 9600, 19200, and 38400 bps or an Externally Supplied 16 Times Bit Rate Clock
- Accepts Asynchronous Data Words of 8 or 9 Bits in Length
- False Start Detection Provided
- Automatic Sync Insertion and Checking
- Single 5 V Power Supply
- Low Power Consumption of 5 mW Typical
- Application Notes AN943 and AN946



L SUFFIX
CERAMIC
CASE 732

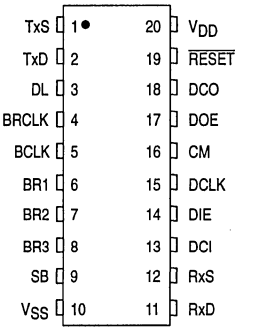


P SUFFIX
PLASTIC
CASE 738



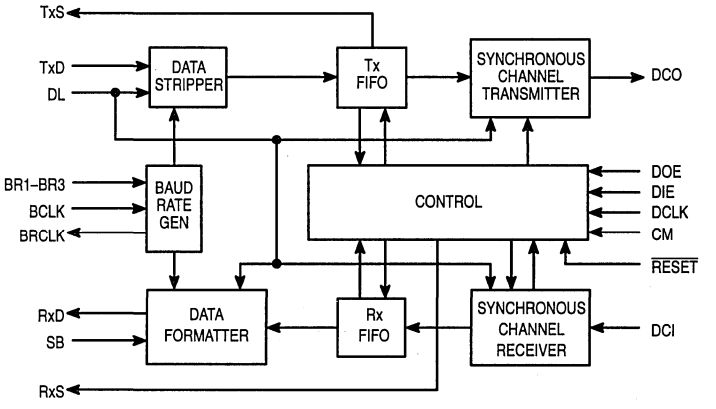
DW SUFFIX
SOG
CASE 751D

PIN ASSIGNMENT



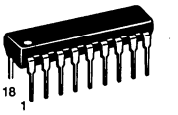
NOT
RECOMMENDED
FOR NEW DESIGN

BLOCK DIAGRAM

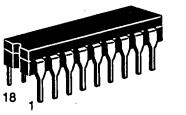


MC145429

Telset Audio Interface Circuit



P SUFFIX
PLASTIC
CASE 707

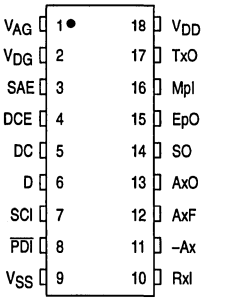


L SUFFIX
CERAMIC
CASE 726

The MC145429 is a silicon-gate CMOS Telset Audio Interface Circuit (TAIC) intended for microcomputer controlled digital or analog telset applications. The device provides the interface between a codec/filter or analog speech network and the telset mouthpiece, earpiece, ringer/speaker amplifier, and an auxiliary input and output. The configuration of the device is programmed via a serial digital data port. Features provided on the device include:

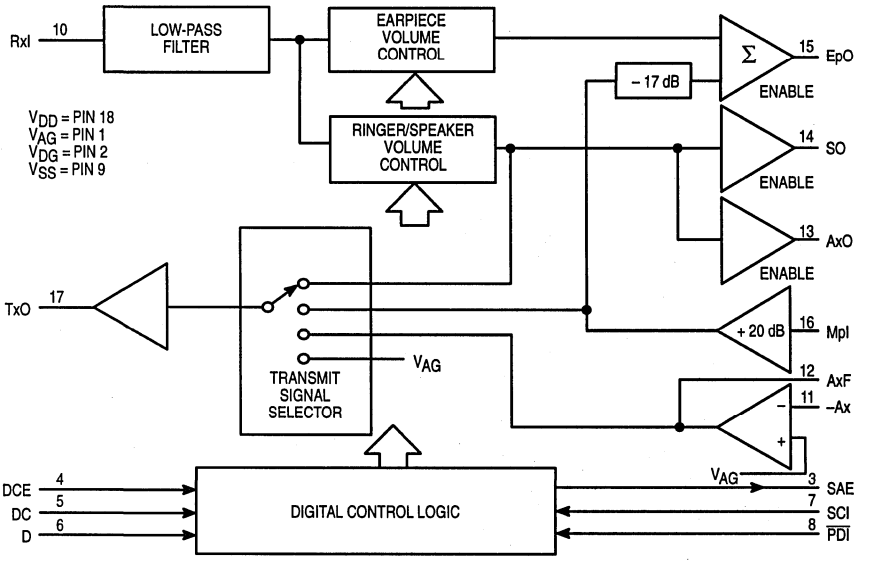
- Independent Adjustment of Earpiece, Speaker, and Ringer Volume
- Transient Suppression Circuitry to Prevent Acoustic "Pops"
- Receive Low-Pass Filter for 8-kHz Attenuation
- Sixteen Possible Audio Configurations
- Power-Down Mode with Data Retention
- 20-dB Mouthpiece Input Gain
- Receive to Transmit Loopback Test Mode
- Provision for Auxiliary Input and Output
- Externally Adjustable Auxiliary Input Gain
- PCM Mono-Circuit Compatible Power Supply
- Digital Output for Speaker Amplifier Control
- Versatile Logic Input Levels
- 18-Pin Package

PIN ASSIGNMENT



NOT RECOMMENDED FOR NEW DESIGN

SIMPLIFIED BLOCK DIAGRAM



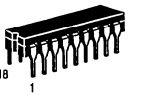
This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC145432

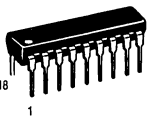
2600 Hz Tone Signaling Filter

This device contains a bypassable 6-pole, 2600 Hz notch filter, a 2-pole 2600 Hz band-pass filter, and a 2600 Hz sine wave generator for SF signaling/ detection applications.

- ±5 V to ±8 V Single or Split Supply Operation
- Low Power Consumption: 80 mW @ 10 V
  200 mW @ 15 V
- On-Board Crystal Oscillator or External Clocks
- Notch Filter Gain Adjustable
- Uncommitted Op Amp Capable of Driving 600 Ω Loads
- TTL or CMOS Compatible Inputs
- 18-Pin Package

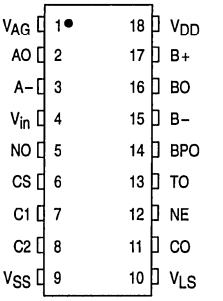


L SUFFIX
CERAMIC
CASE 726



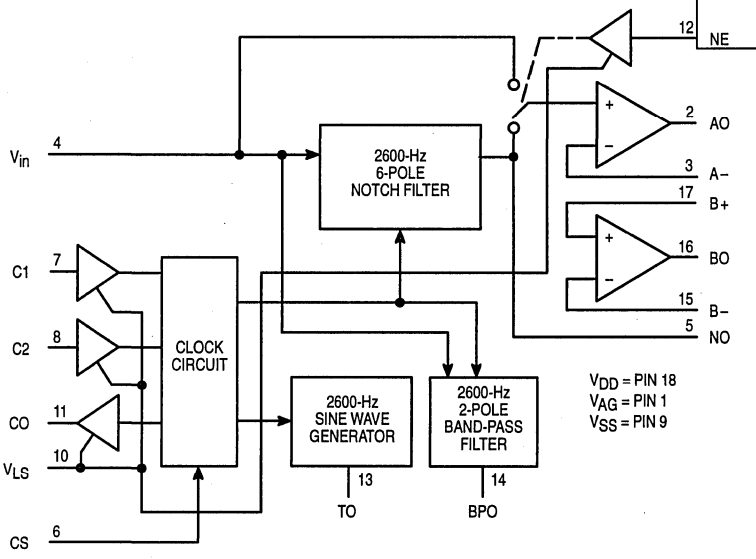
P SUFFIX
PLASTIC
CASE 707

PIN ASSIGNMENT



NOT
RECOMMENDED
FOR NEW DESIGN

BLOCK DIAGRAM



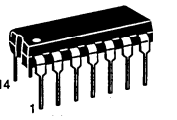
MC145436

Dual Tone Multiple Frequency Receiver

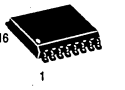
The MC145436 is a silicon gate CMOS LSI device containing the filter and decoder for detection of a pair of tones conforming to the DTMF standard with outputs in hexadecimal. Switched capacitor filter technology is used together with digital circuitry for the timing control and output circuits. The MC145436 provides excellent power line noise and dial tone rejection and is suitable for applications in central office equipment, PABX, and keyphone systems, remote control equipment and consumer telephony products.

The MC145436 offers the following performance features:

- Single +5 V Power Supply
- Detects All 16 Standard Digits
- Uses Inexpensive 3.58-MHz Crystal
- Provides Guard Time Controls to Improve Speech Immunity
- Output in 4-Bit Hexadecimal Code
- Built-in 60 Hz and Dial Tone Rejection
- Pin Compatible with SSI-204



P SUFFIX
PLASTIC
CASE 646



DW SUFFIX
SOG
CASE 751G

PIN ASSIGNMENTS

PLASTIC

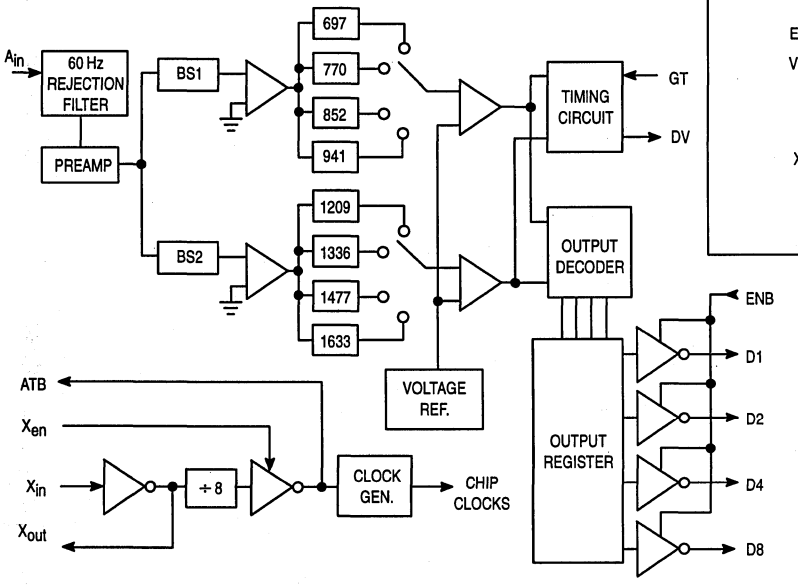
D2	1	14	D4
D1	2	13	D8
ENB	3	12	DV
V_{DD}	4	11	ATB
GT	5	10	X_{in}
X_{en}	6	9	X_{out}
A_{in}	7	8	GND

SOG

D2	1	16	D4
D1	2	15	D8
ENB	3	14	DV
V_{DD}	4	13	NC
NC	5	12	ATB
GT	6	11	X_{in}
X_{en}	7	10	X_{out}
A_{in}	8	9	GND

NC = NO CONNECTION

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages Referenced to GND Unless Otherwise Noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +6.0	V
Input Voltage, Any Pin Except A_{in}	V_{in}	−0.5 to V_{DD} + 0.5	V
Input Voltage, A_{in}	V_{in}	V_{DD} − 10 to V_{DD} + 0.5	V
DC Current Drain per Pin	I	±10	mAdc
Power Dissipation	P_D	30	mW
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to and appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS
(All Polarities Referenced to V_{SS} = 0 V, V_{DD} = 5.0 V ±10%, T_A = − 40 to + 85°C, Unless Otherwise Noted)

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.5	5	5.5	V
Supply Current (f_{CLK} = 3.58 MHz)	I_{DD}	—	7	15	mA
Input Current GT ENB, X_{in}, X_{en}	I_{in}	— —	— —	200 ±1	µA
Input Voltage Low ENB, GT, X_{en}	V_{IL}	—	—	1.5	V
Input Voltage High ENB, GT, X_{en}	V_{IH}	3.5	—	—	V
I_{out} Data and DV Pins: V_{out} = 4.5 V (Source)	I_{OH}	800	—	—	µA
I_{out} Data and DV Pins: V_{out} = 0.4 V (Sink)	I_{OL}	1.0	—	—	mA
Input Impedance A_{in}	R_{in}	90	100	—	kΩ
Fanout ATB	F_{out}	—	—	10	
Input Capacitance X_{en}, ENB	C_{in}	—	6	—	pF

ANALOG CHARACTERISTICS (V_{DD} = 5.0 V ±10%, T_A = − 40 to + 85°C, Unless Otherwise Noted)

Parameter	Min	Typ	Max	Unit
Signal Level for Detection (A_{in})	−35	—	−2	dBm
Twist = High Tone/Low Tone	−10	—	10	dB
Frequency Detect Bandwidth	±(1.5 + 2 Hz)	±2.5	±3.5	% f_O
60-Hz Tolerance	—	—	0.8	Vrms
Dial Tone Tolerance (Note 1) (Dial Tone 330 + 440)	—	—	0	dB
Noise Tolerance (Notes 1 and 2)	—	—	−12	dB
Power Supply Noise (Wide Band)	—	—	10	mVp-p
Talk Off (Mitel Tape #CM7290)	—	2	—	Hits

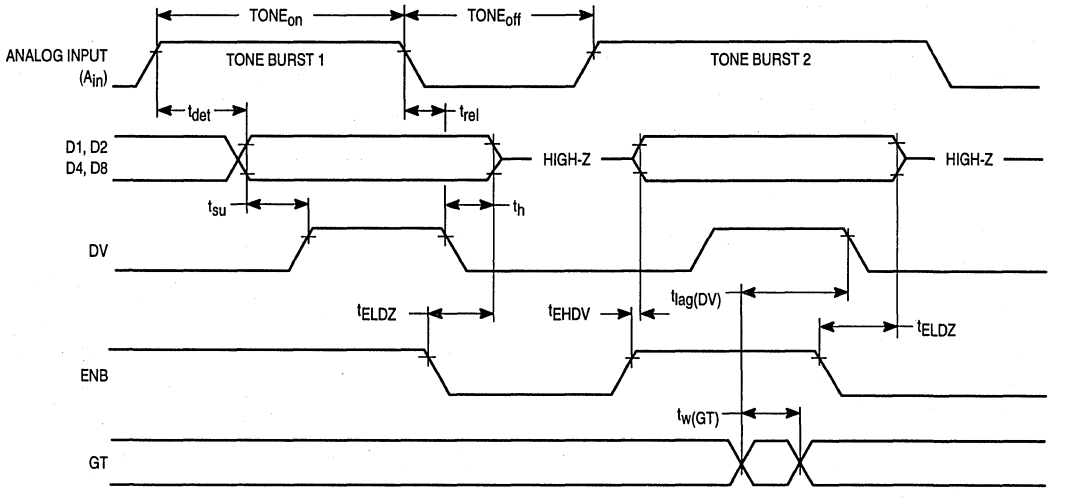
NOTES:
1. Referenced to lower amplitude tone.
2. Bandwidth limited (0 to 3.4 kHz) Gaussian Noise.

AC CHARACTERISTICS (V_{DD} = 5.0 V ± 10%, T_A = −40°C to +85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Tone On Time For Rejection	For Detection	$TONE_{on}$	40 —	— —	— 20	ms
Pause Time For Rejection	For Detection	$TONE_{off}$	40 —	— —	— 20	ms
Detect Time GT = 1	GT = 0	t_{det}	22 32	— —	40 50	ms
Release Time GT = 1	GT = 0	t_{rel}	28 18	— —	40 30	ms
Data Setup Time		t_{su}	7	—	—	µs
Data Hold Time		t_h	4.2	4.6	5	ms
Pulse Width	GT	$t_{w(GT)}$	18	—	—	µs
DV Reset Lag Time		$t_{lag(DV)}$	—	—	5	ms
ENB High to Output DV (Note 1)		t_{EHDV}	—	120	500	ns
ENB Low to Output High-Z (Note 1)		t_{ELDZ}	—	110	300	ns

NOTE:
1. Data out: C_L = 35 pF || R_L = 500 Ω.

TIMING DIAGRAM



PIN DESCRIPTIONS

V_{DD}
Positive Power Supply
The digital supply pin, which is connected to the positive side of the power supply.

V_{SS}
Ground
Ground return pin is typically connected to the system ground.

D1, D2, D4, D8
Data Output
These digital outputs provide the hexadecimal codes corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected and are cleared when a valid pause is timed. See Table 1 for hexadecimal codes.These output pins are high impedance when the enable pin is at logic 0.

EN
Enable
Outputs D1, D2, D4, D8 are enabled when ENB is at a logic 1, and high impedance (disabled) when ENB is at a logic 0.

GT
Guard Time
The Guard Time control input provides two sets of detected time and release time, both within the allowed ranges of tone on and tone off (see Figure 1). A longer tone detect time rejects signals too short to be considered valid. With GT = 1, talk off performance is improved, since it reduces the probability that tones simulated by speech will maintain signal conditions long enough to be accepted. In addition, a shorter release time reduces the probability that a pause simulated by an interrupt in speech will be detected as a valid pause. On the other hand, a shorter tone detect time with a long release time would be appropriate for an extremely noisy environment where fast acquisition time and immunity to dropouts would be required. In general, the tone signal time generated by a telephone is 100 ms, nominal, followed by a pause of about 100 ms. A high-to-low or low-to-high transition on the GT pin resets the internal logic and the MC145436 is immediately ready to accept a new tone input. If left open, this pin is internally pulled to ground.

Table 1. Hexadecimal Codes

Digit	Output Code			
	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

X_{en}
Oscillator Enable
A logic 1 on X_{en} enables the on-chip crystal oscillator. When using alternate time base from the ATB pin, X_{en} should be tied to V_{SS}.

A_{in}
Analog Input
This pin accepts the analog input and is internally biased so that the input signal may be ac coupled. The input may be dc coupled so long as it does not exceed the positive supply (see Figure 2).

X_{in}/X_{out}
Oscillator In and Oscillator Out
These pins connect to an internal crystal oscillator. In operation, a parallel resonant crystal is connected from X_{in} to X_{out}, as well as a 1-MΩ resistor in parallel with the crystal. When using the alternate clock source from ATB, X_{in} should be tied to V_{DD}.

ATB
Alternate Time Base
This pin serves as a frequency reference when more than one MC145436 is used, so that only one crystal is required for multiple MC145436s. When doing so, all ATB pins should be tied together as shown in Figure 3. When only one MC145436 is used, this pin should be left unconnected. The output frequency of ATB is 447.4 kHz.

DV
Data Valid
DV signals a detection by going high after a valid tone pair is sensed and decoded at output pins D1, D2, D4, D8. DV remains high until a loss of the current DTMF signal occurs or until a transition in GT occurs.

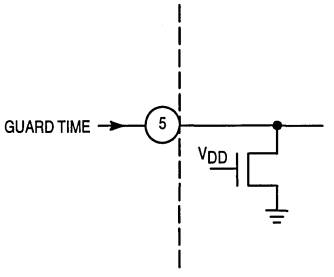


Figure 1. Guard Time

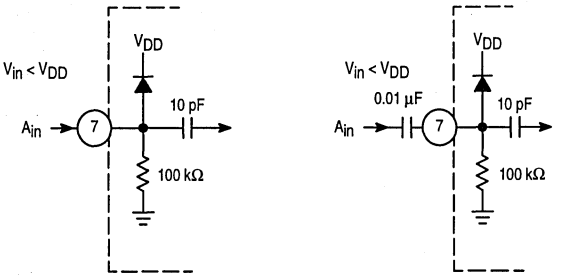


Figure 2. Analog Input (Operational Information based on PDIP package)

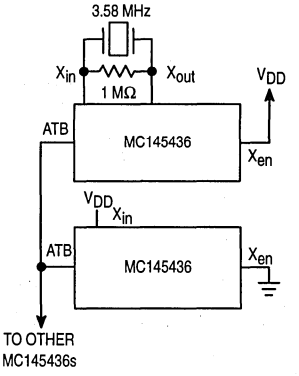


Figure 3. Multiple MC145436s

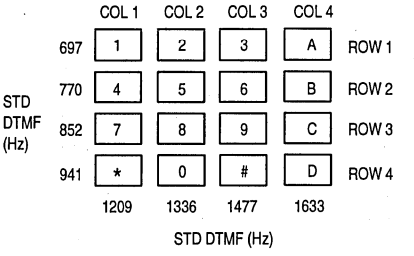


Figure 4. 4 × 4 Keyboard Matrix

MC145439
MC142103

Encoder/Decoder (Transcoder)
For Transmission Applications

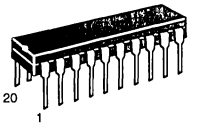
The MC145439 and MC142103 are high speed CMOS integrated circuits designed to perform the coding translation of clocked serial data into two streams of return to zero (RZ) digital pulses, which are externally mixed to form either AMI, HDB3, B6ZS, or B8ZS (MC142103—AMI or HDB3 only) ternary signals for driving transmission lines. They perform the reverse operation by translating two streams of clocked pulses [which have been derived from an incoming AMI, HDB3, B6ZS, or B8ZS (MC142103—AMI or HDB3 only) ternary encoded signal] into a single stream of clocked binary data. They also feature loopback and error monitoring functions. The coding and decoding functions perform independently at clock rates from 0 (dc) to 9 mbps. The HDB3 coding and decoding are performed in a manner consistent with the CCITT G.703 recommendations.

Both Devices:
- Low Power CMOS Operation
- Single 5-V Power Supply Operation
- Error Monitor Functions Provided
- Loopback Feature Provided
- Encode and Decode Clock Rates to 9 mbps
- Pin Selectable Modes of Operation
- TTL Compatible Inputs and Outputs

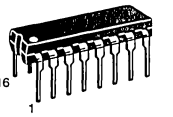
MC145439 Only:
- 20-Pin Package
- NRZ to AMI, HDB3, B6ZS, B8ZS; AMI, HDB3, B6ZS, B8ZS to NRZ
- Force Alarm and Output Enable Function
- Pin Compatible with HC-5560

MC142103 Only:
- 16-Pin Package
- NRZ to AMI, HDB3; AMI, HDB3 to NRZ
- Pin Selectable HDB3 or AMI Operation
- Pin Compatible with CD22103 and MJ1471

NOT RECOMMENDED FOR NEW DESIGN



MC145439
PLASTIC
CASE 738



MC142103
PLASTIC
CASE 648

PIN ASSIGNMENTS

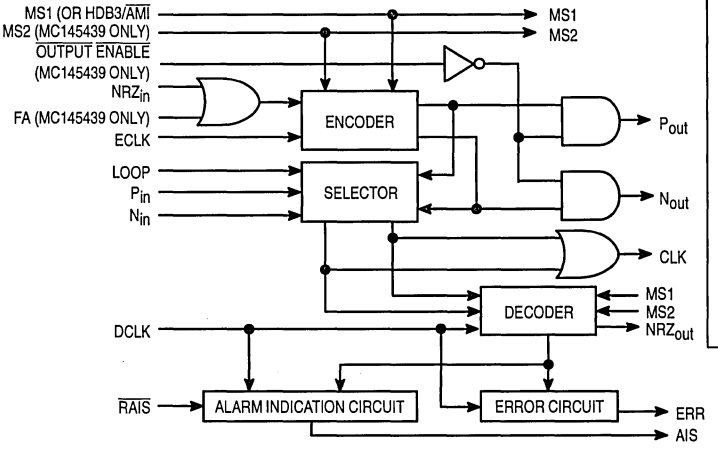
MC145439

FA	1	20	V_{DD}
MS1	2	19	$\overline{OE}$
NRZ_{in}	3	18	N.C.
ECLK	4	17	P_{out}
MS2	5	16	N_{out}
NRZ_{out}	6	15	N_{in}
DCLK	7	14	LOOP
$\overline{RAIS}$	8	13	P_{in}
AIS	9	12	CLK
V_{SS}	10	11	ERR

MC142103

NRZ_{in}	1	16	V_{DD}
ECLK	2	15	P_{out}
HDB3/AMI	3	14	N_{out}
NRZ_{out}	4	13	N_{in}
DCLK	5	12	LOOP
$\overline{RAIS}$	6	11	P_{in}
AIS	7	10	CLK
V_{SS}	8	9	ERR

BLOCK DIAGRAM



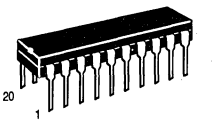
This document contains information on a new product. Specification and information herein are subject to change without notice.

MC145442
MC145443

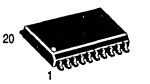
Single Chip 300-Baud Modem

The MC145442 and MC145443 silicon-gate CMOS single-chip low-speed modems contain a complete frequency shift keying (FSK) modulator, demodulator, and filter. These devices are with CCITT V.21 (MC145442) and Bell 103 (MC145443) specifications. Both devices provide full-duplex or half-duplex 300-baud data communication over a pair of telephone lines. They also include a carrier detect circuit for the demodulator section and a duplexer circuit for direct operation on a telephone line through a simple transformer.

- MC145442 Compatible with CCITT V.21
- MC145443 Compatible with Bell 103
- Low-Band and High-Band Band-Pass Filters On-Chip
- Simplex, Half-Duplex, and Full-Duplex Operation
- Originate and Answer Mode
- Analog Loopback Configuration for Self Test
- Hybrid Network Function On-Chip
- Carrier Detect Circuit On-Chip
- Adjustable Transmit Level and $\overline{CD}$ Delay Timing
- On-Chip Crystal Oscillator (3.579 MHz)
- Single +5 V Power Supply Operation
- Internal Mid-Supply Generator
- Power-Down Mode
- Pin Compatible with MM74HC943
- Capable of Driving −9 dBm into a 600 Ω Load

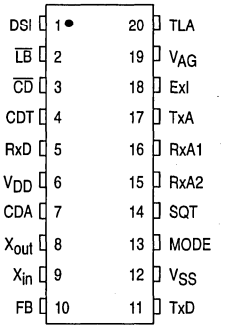


P SUFFIX
PLASTIC
CASE 738

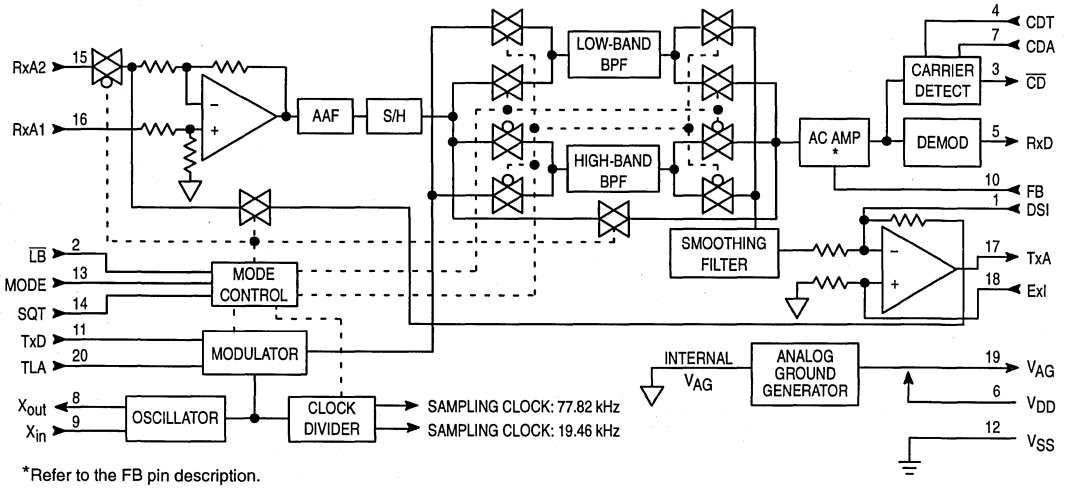


DW SUFFIX
SOG
CASE 751D

PIN ASSIGNMENT



BLOCK DIAGRAM



*Refer to the FB pin description.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.5 to +7.0	V
DC Input Voltage	V_{in}	−0.5 to V_{DD} +0.5	V
DC Output Voltage	V_{out}	−0.5 to V_{DD} +0.5	V
Clamp Diode Current, per Pin	I_{IK}, I_{OK}	±20	mA
DC Output Current, per Pin	I_{out}	±28	mA
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
DC Input or Output Voltage	V_{in}, V_{out}	0	V_{DD}	V
Input Rise or Fall Time	t_r, t_f	—	500	ns
Crystal Frequency*	$f_{crystal}$	3.2	5.0	MHz

*Changing the crystal frequency from 3.579 MHz will change the output frequencies. The change in output frequency will be proportional to the change in crystal frequency.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ± 10%, T_A = −40°C to +85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	$\overline{LB}$	V_{IH}	V_{DD} − 0.8	—	—	V
X_{in}, TxD, Mode, SQT			3.15	—	—	
Low-Level Input Voltage	$\overline{LB}$	V_{IL}	—	—	0.8	V
X_{in}, TxD, Mode, SQT			—	—	1.1	
High-Level Output Voltage		V_{OH}				V
I_{OH} = 20 µA	$\overline{CD}$, RxD		V_{DD} − 0.1	—	—	
I_{OH} = 2 mA	$\overline{CD}$, RxD		3.7	—	—	
I_{OH} = 20 µA	X_{out}		—	V_{DD} − 0.05	—	
Low-Level Output Voltage		V_{OL}				V
I_{OL} = 20 µA	$\overline{CD}$, RxD		—	—	0.1	
I_{OL} = 2 mA	$\overline{CD}$, RxD		—	—	0.4	
I_{OL} = 20 µA	X_{out}		—	0.05	—	
Input Current	$\overline{LB}$, TxD, Mode, SQT	I_{in}	—	—	±1.0	µA
RxA1, RxA2			—	10	±12	
X_{in}			—	—	±10	
Quiesent Supply Current (X_{in} or $f_{crystal}$ = 3.579 MHz)		I_{DD}	—	7	10	mA
Power-Down Supply Current			—	200	300	µA
Input Capacitance	X_{in}	C_{in}	—	10	—	pF
All Other Inputs			—	—	10	
V_{AG} Output Voltage (I_O = ± 10 µA)		V_{AG}	2.4	2.5	2.6	V
CDA Output Voltage (I_O = ± 10 µA)		V_{CDA}	1.1	1.2	1.3	V
Line Driver Feedback Resistor		R_f	10	20	30	kΩ

AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 V ± 10%, T_A = −40°C to +85°C, Crystal Frequency = 3.579 MHz ±0.1%; See Figure 1)

Characteristic		Min	Typ	Max	Unit
TRANSMITTER					
Power Output on TxA R_L = 1.2 kΩ, R_{TLA} = ∞ R_L = 1.2 kΩ, R_{TLA} = 5.5 kΩ		 −13 −10	 −12 −9	 −11 −8	dBm
Second Harmonic Power R_L = 1.2 kΩ		— 	−56 	— 	dBm
RECEIVE FILTER AND HYBRID					
Hybrid Input Impedance RxA1, RxA2		40	50	—	kΩ
FB Output Impedance		—	16	—	kΩ
Adjacent Channel Rejection		−48	—	—	dBm
DEMODULATOR					
Receive Carrier Amplitude		−48	—	−12	dBm
Dynamic Range		—	36	—	dB
Bit Jitter (S/N = 30 dB, Input = − 38 dBm, Bit Rate = 300 baud)		—	100	—	μs
Bit Bias		—	5	—	%
Carrier Detect Threshold (CDA = 1.2 V or CDA grounded through a 0.1-μF capacitor)	On to Off Off to On	— —	−44 −47	— —	dBm

PIN DESCRIPTIONS

V_{DD}
Positive Power Supply (Pin 6)

This pin is normally tied to 5.0 V.

V_{SS}
Negative Power Supply (Pin 12)

This pin is normally tied to 0 V.

V_{AG}
Analog Ground (Pin 19)

Analog ground is internally biased to (V_{DD} − V_{SS})/2. This pin must be decoupled by a capacitor from V_{AG} to V_{SS} and a capacitor from V_{AG} to V_{DD}. Analog ground is the common bias line used in the switched capacitor filters, limiter, and slicer in the demodulation circuitry.

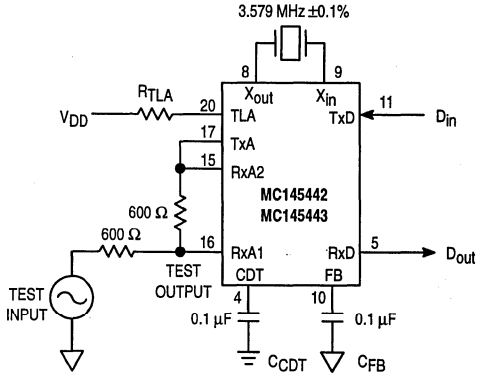


Figure 1. AC Characteristics Evaluation Circuit

TLA
Transmit Level Adjust (Pin 20)

This pin is used to adjust the transmit level. Transmit level adjustment range is typically from −12 dBm to −9 dBm. (See Applications Information.)

TxD
Transmit Data (Pin 11)

Binary information is input to the transmit data pin. Data entered for transmission is modulated using FSK techniques. A logic high input level represents a mark and a logic low represents a space (see Table 1).

Table 1. Bell 103 and CCITT V.21 Frequency Characteristics

Bell 103 (MC145443)				
	Originate Mode		Answer Mode	
Data	Transmit	Receive	Transmit	Receive
Space	1070 Hz	2025 Hz	2025 Hz	1070 Hz
Mark	1270 Hz	2225 Hz	2225 Hz	1270 Hz
CCITT V.21 (MC145442)				
	Originate Mode		Answer Mode	
Data	Transmit	Receive	Transmit	Receive
Space	1180 Hz	1850 Hz	1850 Hz	1180 Hz
Mark	980 Hz	1650 Hz	1850 Hz	980 Hz

NOTE: Actual frequencies maybe ±5 Hz assuming 3.579545-MHz crystal is used.

TxA
Transmit Carrier (Pin 17)

This is the output of the line driver amplifier. The transmit carrier is the digitally synthesized sine wave output of the modulator derived from a crystal oscillator reference. When a 3.579 MHz crystal is used the frequency outputs shown in Table 1 apply. (See ***Applications Information.***)

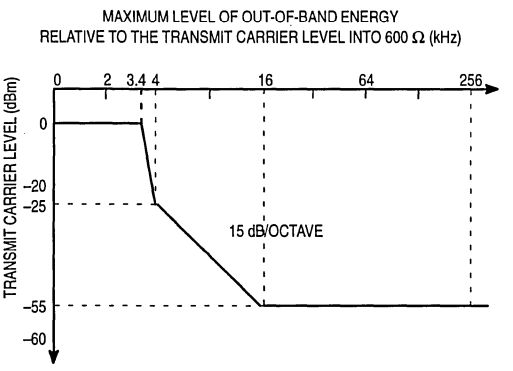


Figure 2. Out-of-Band Energy

ExI
External Input (Pin 18)

The external input is the non-inverting input to the line driver. It is provided to combine an auxiliary audio signal or speech signal to the phone line using the line driver. This pin should be connected to V_{AG} if not used. The average level must be the same as V_{AG} to maintain proper operation. (See ***Applications Information.***)

DSI
Driver Summing Input (Pin 1)

The driver summing input may be used to connect an external signal, such as a DTMF dialer, to the phone line. A series resistor, R_{DSI}, is needed to define the voltage gain A_V (see Applications Information and Figure 6). When applying a signal to do DSI pin, the modulator should be squelched by bringing SQT (Pin 14) to a logic high level. The voltage gain, A_V, is calculated by the formula $A_V = -R_f/R_{DSI}$ (where $R_f \approx 20$ kΩ). For example, a 20 kΩ resistor for R_{DSI} will provide unity gain ($A_V = -20$ kΩ/20 kΩ $= -1$). This pin **must** be left **open** if not used.

RxD
Receive Data (Pin 6)

The receive data output pin presents the digital binary data resulting from the demodulation of the receive carrier. If no carrier is present, $\overline{CD}$ high, the receive data output (RxD) is clamped high.

RxA2, RxA1
Receive Carrier (Pins 15, 16)

The receive carrier is the FSK input to the demodulator through the receive band-pass filter. RxA1 is the non-inverting input and RxA2 is the inverting input of the receive hybrid (duplexer) operational amplifier.

$\overline{LB}$
Analog Loopback (Pin 2)

When a high level is applied to this pin (SQT must be low), the analog loopback test is enabled. The analog loopback test connects the TxA pin to the RxA2 pin and the RxA1 to analog ground. In loopback, the demodulator frequencies are switched to the modulation frequencies for the selected mode. (See Tables 1 and 2 and Figures 4c and 4d.)

When $\overline{LB}$ is connected to analog ground (V_{AG}), the modulator generates an echo cancellation tone of 2100 Hz for MC145442 CCITT V.21 and 2225 Hz for MC145443 Bell 103 systems. For normal operation, this pin should be at a logic low level (V_{SS}).

The power-down mode is enabled when both $\overline{LB}$ and SQT are connected to a logic high level (see Table 2).

Table 2. Functional Table

MODE Pin 13	SQT Pin 14	$\overline{LB}$ Pin 2	Operating Mode
1	0	0	Originate Mode
0	0	0	Answer Mode
X	0	V_{AG} (V_{DD}/2)	Echo Tone
X	0	1	Analog Loopback
X	1	0	Squelch Mode
X	1	V_{AG} (V_{DD}/2)	Squelch Mode
X	1	1	Power Down

MODE
Mode (Pin 13)

This input selects the pair of transmit and frequencies used during modulation and demodulation. When a logic high level is placed on this input, originate (Bell) or channel 1 (CCITT) is selected. When a low level is placed on this input, answer (Bell) or channel 2 (CCITT) is selected. (See Tables 1 and 2 and Figure 4.)

CDT
Carrier Detect Timing (Pin 4)

A capacitor on this pin to V_{SS} sets the amount of time the carrier must be present before $\overline{CD}$ goes low (see ***Applications Information*** for the capacitor values).

$\overline{CD}$
Carrier Detect Output (Pin 3)

This output is used to indicate when a carrier has been sensed by the carrier detect circuit. This output goes to a logic low level when a valid signal above the maximum threshold level (defined by CDA, Pin 7) is maintained on the input to the hybrid circuit longer then the response (defined by CDT, Pin 4). This pin is held at the logic low level until the signal falls below the maximum threshold level for longer than the turn off time. (See ***Applications Information*** and Figure 5.)

CDA
Carrier Detect Adjust (Pin 7)

An external voltage may be applied to this pin to adjust the carrier detect threshold. The threshold hysteresis is internally fixed at 3 dB (see ***Applications Information***).

X_{out}, X_{in}
Crystal Oscillator (Pins 8, 9)

A crystal reference oscillator is formed when a 3.579 MHz crystal is connected between these two pins. X_{out} (Pin 8) is the output of the oscillator circuit, and X_{in} (Pin 9) is the input to the oscillator circuit. When using an external clock, apply the clock to the X_{in} (Pin 9) pin and leave X_{out} (Pin 8) open. An internal 10-MΩ resistor and internal capacitors, typically 10 pF on X_{in} and 16 pF on X_{out}, allow the crystal to be connected without any other external components. Printed circuit board layout should keep external stray capacitance to a minimum.

FB
Filter Bias (Pin 10)

This is the negative input to the ac amplifier. In normal operation, this pin is connected to analog ground through a 0.1 µF bypass capacitor in order to cancel the input offset voltage of the limiter. It has a nominal input impedance of 16 kΩ. (see Figure 3).

SQT
Transmit Squelch (Pin 14)

When this input pin is at a logic high level, the modulator is disabled. The line driver remains active if $\overline{LB}$ is at a logic low level (see Table 2) .

When both $\overline{LB}$ and SQT are connected to a logic high level, see Table 2, the entire chip is in a power down state and all circuitry except the crystal oscillator is disabled. Total power supply current decreases from 10 mA (Max) to 300 µA (Max).

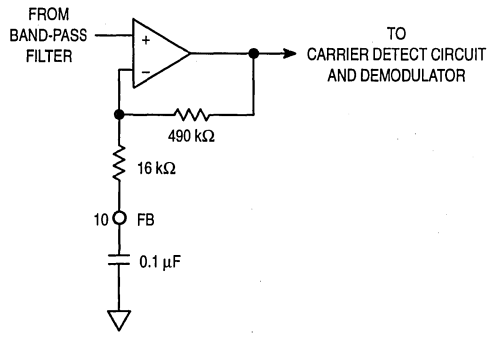


Figure 3. AC Amplifier Circuit

GENERAL DESCRIPTION

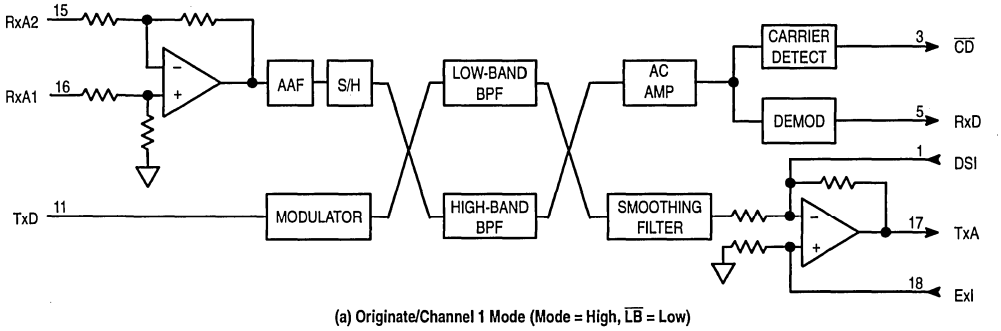
The MC145442 and MC145443 are full-duplex low-speed modems. They provide a 300 baud FSK signal for bidirectional data transmission over the telephone network. They can be operated in one of four basic configurations as determined by the state of MODE (Pin 13) and $\overline{LB}$ (Pin 2). The normal (nonloopback) and self test (loopback) modes in both answer and originate modes will be discussed.

For an originate or channel 1 mode, a logic high level is placed on MODE (Pin 13) and a logic low level is placed on $\overline{LB}$ (Pin 2). in this mode, transmit data is input on TxD, where it is converted to a FSK signal and routed through a low-band band-pass filter. The filtered output signal is then buffered by the Tx op-amp line driver, which is capable of driving –9 dBm onto a 600 Ω line. The receive signal is connected through a hybrid duplexer circuit on pins 15 and 16, RxA2 and RxA1. The signal then passes through the anti-aliasing filter, the sample-and-hold circuit, is switched into the high-band band-pass filter, and then switched into the ac amplifier circuit. The output of the ac amplifier circuit is routed to the demodulator circuit and demodulated. The resulting digital data is then output through RxD (Pin 5). The carrier detect circuit receives its signal from the output of the ac amplifier circuit and goes low when the incoming signal is detected (see Figure 4a).

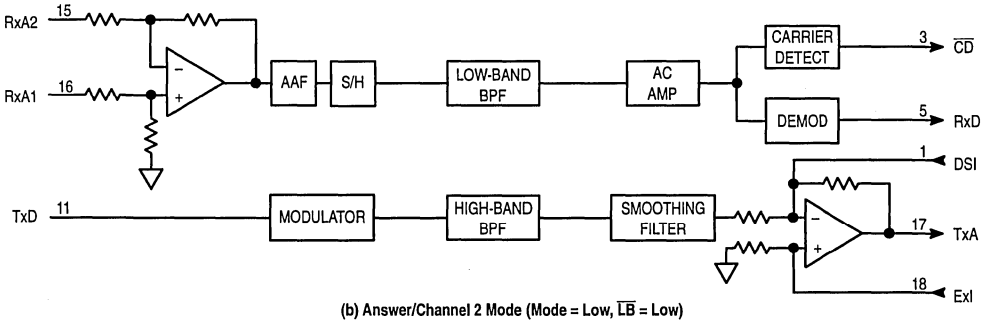
In the answer or channel 2 mode, a logic low level is placed on MODE (Pin 13) and on $\overline{LB}$ (Pin 2). In this mode, the data follows the same path except the FSK signal is routed to the high-band band-pass filter and the sample-and-hold signal is routed through the low-band band-pass filter. (See Figure 4b.)

In the analog loopback originate or channel 1 mode, a logic high level is placed on MODE (Pin 13) and on $\overline{LB}$ (Pin 2). This mode is used for a self check of the modulator, demodulator, and low-band pass-band filter circuit. The modulator side is configured exactly like the originate mode above except the line driver output (TxA, Pin 17) is switched to the negative input of the hybrid op-amp. The RxA2 input pin is open in this mode and the non-inverting input of the hybrid circuit is connected to V_{AG}. The sample-and-hold output bypasses the filter so that the demodulator receives the modulated Tx data (see Figure 4c). This test checks all internal device components except the high-band band-pass filter, which can be checked in the answer or channel 2 mode test.

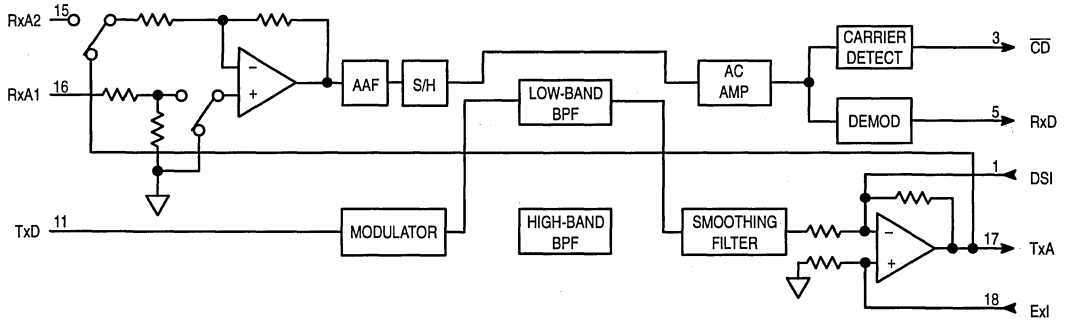
In the analog loopback or chanel 2 mode, a logic low level is placed on MODE (Pin 13) and a logic high level on $\overline{LB}$ (Pin 2). This mode is used for a self check of the modulator, demodulator, and high-band pass-band filter circuit. This configuration is exactly like the originate loopback mode above, except the signal is routed through the high-band pass-band filter (see Figure 4d).



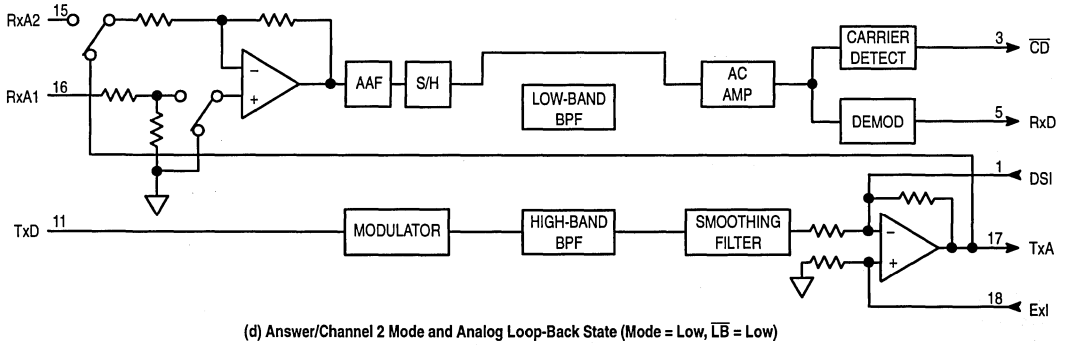
(a) Originate/Channel 1 Mode (Mode = High, $\overline{LB}$ = Low)



(b) Answer/Channel 2 Mode (Mode = Low, $\overline{LB}$ = Low)



(c) Originate/Channel 1 Mode and Analog Loop-Back State (Mode = High, $\overline{LB}$ = Low)



(d) Answer/Channel 2 Mode and Analog Loop-Back State (Mode = Low, $\overline{LB}$ = Low)

Figure 4. Basic Operating Modes

APPLICATIONS INFORMATION

CARRIER DETECT TIMING ADJUSTMENT

The value of a capacitor, C_{CDT} at CDT (Pin 4) determines how long a received modem signal must be present above the minimum threshold level before $\overline{CD}$ (Pin 3) goes low. The C_{CDT} capacitor also determines how long the $\overline{CD}$ pin stays low after the received modem signal goes below the minimum threshold. The $\overline{CD}$ pin is used to distinguish a strong modem signal from random noise. The following equations show the relationship between t_{CDL}, the time in seconds required for $\overline{CD}$ to go low; t_{CDH}, the time in seconds required for $\overline{CD}$ to go high; and C_{CDT}, the capacitor value in μF.

Valid signal to $\overline{CD}$ response time: $t_{CDL} \approx 6.4 \times C_{CDT}$

Invalid signal to $\overline{CD}$ off time: $t_{CDH} \approx 0.54 \times C_{CDT}$

Example: $t_{CDL} \approx 6.4 \times 0.1\ \mu F \approx 0.64$ seconds

$t_{CDH} \approx 0.54 \times 0.1\ \mu F \approx 0.054$ seconds

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is set by internal resistors to activate $\overline{CD}$ with a typical −44 dBm (into 600 Ω) signal and deactivate $\overline{CD}$ with a typical −47 dBm signal applied to the input of the hybrid circuit. The carrier detect threshold level can be adjusted by applying an external voltage on CDA (Pin 7). The following equations may be used to find the CDA voltage required for a given threshold voltage. (V_{on} and V_{off} are in Vrms.)

$$V_{CDA} = 244 \times V_{on}$$

$$V_{CDA} = 345 \times V_{off}$$

Example (internally set)

$V_{on} = 4.9$ mV ≈ −44 dBm: $V_{CDA} = 244 \times 4.9$ mV = 1.2 V

$V_{off} = 3.5$ mV ≈ −47 dBm: $V_{CDA} = 345 \times 3.5$ mV = 1.2 V

Example (externally set)

$V_{on} = 7.7$ mV ≈ −40 dBm: $V_{CDA} = 244 \times 7.7$ mV = 1.9 V

$V_{off} = 5.4$ mV ≈ −43 dBm: $V_{CDA} = 345 \times 5.4$ mV = 1.9 V

The CDA pin has an approximate Thevenin equivalent voltage of 1.2 V and an output impedance of 100 kΩ. When using the internal 1.2-V reference a 0.1-μF capacitor should be connected between this pin and V_{SS} (see Figure 5).

TRANSMIT LEVEL ADJUSTMENT

The power output at TxA (Pin 17) is determined by the value of resistor R_{TLA} that is connected between TLA (Pin 20) to V_{DD} (Pin 6). Table 3 shows the R_{TLA} values and the corresponding power output for a 600 Ω load. The voltage at TxA is twice the value of that at ring and tip because TxA feeds the signal through a 600 Ω resistor R_{TX} to a 600 Ω line transformer (see Figure 7). When choosing resistor R_{TLA}, keep in mind that −9 dBm is the maximum output level allowed from a modem onto the telephone line (in the U.S.). In addition, keep in mind that maximizing the power output from the modem optimizes the signal-to-noise ratio, improving accurate data transmission.

Table 3. Transmit Level Adjust

Output Transmit Level (Typical into 600 Ω)	R_{TLA}
−12 dBm	∞
−11 dBm	19.8 kΩ
−10 dBm	9.2 kΩ
−9 dBm	5.5 kΩ

THE LINE DRIVER

The line driver is a power amplifier used for driving the telephone line. Both the inverting and noninverting input to the line driver are available for transmitting externally generated tones.

Exl (Pin 18) is the noninverting input to the line driver and gives a fixed gain of 2 (R_i = 50 kΩ). The average signal level must be the same as V_{AG} to maintain proper operation. This pin should be connected to V_{AG} if not used.

The driver summing input (DSI, Pin 1) may be used to connect an external signal, such as a DTMF dialer, to the phone line. When applying a signal to the DSI pin, the modulator should be squelched by bringing SQT (Pin 14) to a logic high level. DSI ***must*** be left ***open*** if not used.

In addition, the DSI pin is the inverting side of the line driver and allows adjustable gain with a series resistor R_{DSI} (see Figure 6). The voltage gain, A_V, is determined by the equation:

$$A_V = -\frac{R_f}{R_{DSI}}$$

where $R_f \approx 20$ kΩ.

Example: A resistor value of 20 kΩ for R_{DSI} will provide unity gain.

$$A_V = -(20\ k\Omega / 20\ k\Omega) = -1$$

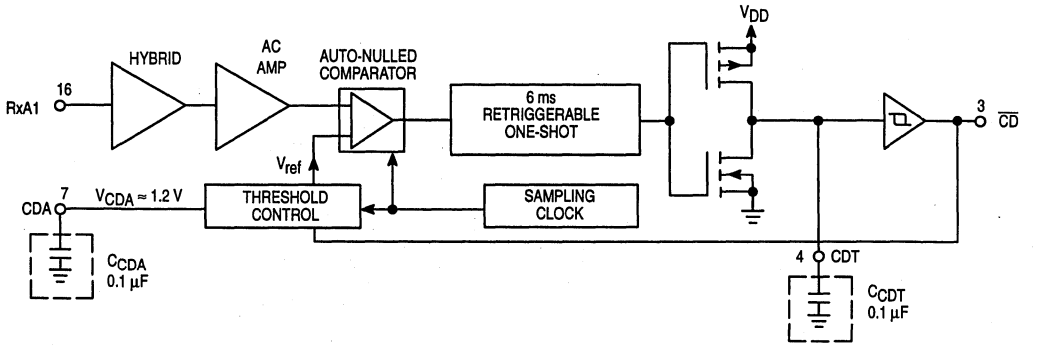


Figure 5. Carrier Detect Circuit

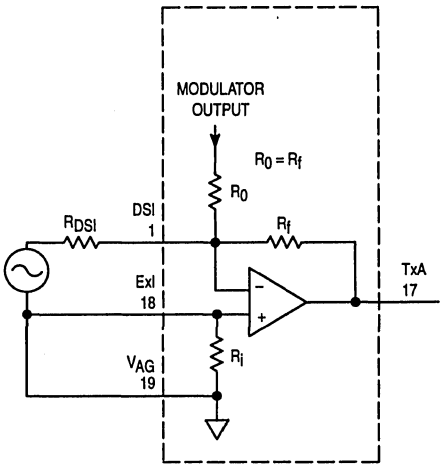


Figure 6. Line Driver Using the DSI Input

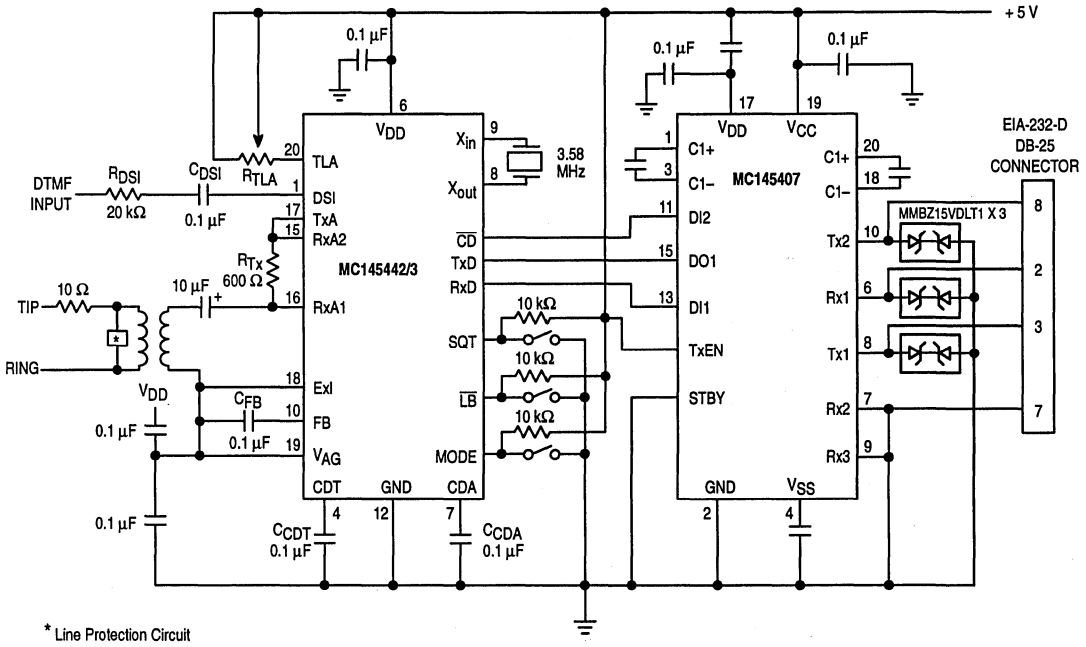
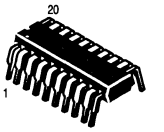


Figure 7. Typical MC145442/MC145443 Applications Circuit

MC145444

Advance Information

Single Chip 300-Baud Modem



H SUFFIX
PLASTIC
CASE 804

DW SUFFIX
PLASTIC
CASE 751D

MC145444 is a silicon gate CMOS frequency shift keying (FSK) modem intended for use with telemeter systems or remote control systems over the telephone network.

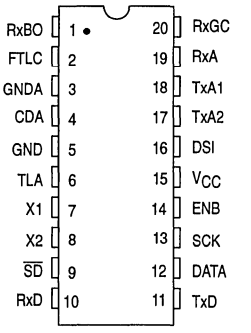
This device is compatible with CCITT V.21 and contains the entire circuit that provides a full-duplex or half-duplex 300 baud data communication over a pair of telephone lines. This device also includes the DTMF generator and call progress tone detector (CPTD).

The differential line driver has the capability of driving 0 dBm into a 600 Ω load with a single +5 V power supply.

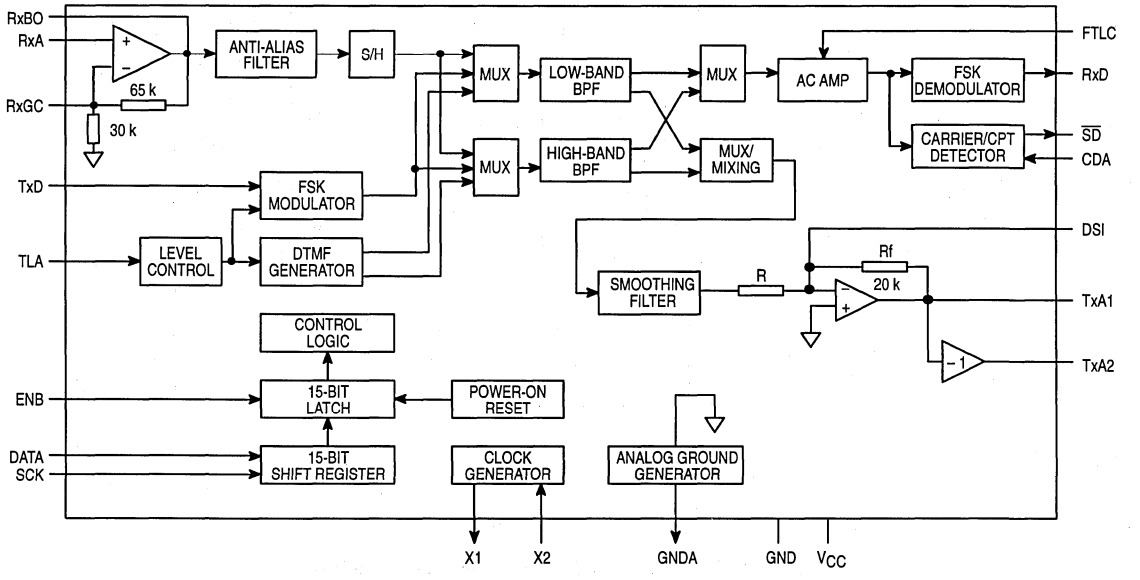
The transmit level is controlled by the programmable attenuator in 1 dB steps. Devices functions are controlled through a 3-wire serial interface.

- Capable of Driving 0 dBm into a 600 Ω Load
- DTMF Generator On-Chip
- Imprecise Call Progress Detector On-Chip
- A Transmit Attenuator Programmable in 1 dB Steps
- 3-wire Serial Interface
- Compatible with CCITT V.21
- 2100 Hz Answer Tone Generator On-Chip
- Analog Loop-Back Configuration for Self Test
- Simplex, Half-Duplex, and Full-Duplex Operation

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product. Specification and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	−0.5 to +7.0	V
DC Input Voltage	V_{in}	−0.5 to V_{CC} +0.5	V
DC Output Voltage	V_{out}	−0.5 to V_{CC} +0.5	V
Clamp Diode Current per Pin	I_{IK}, I_{OK}	±20	mA
DC Current per Pin	I_{out}	±25	mA
Power Dissipation	P_D	500	mW
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{CC}	4.5	5	5.5	V
DC Input Voltage	V_{in}	0	—	V_{CC}	V
DC Output Voltage	V_{out}	0	—	V_{CC}	V
Input Rise Time	t_r	0	—	500	ns
Input Fall Time	t_f	0	—	500	ns
Crystal Frequency	f_{osc}	—	3.579545	—	MHz
Operating Temperature Range	T_A	−20	25	70	°C

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc ±10%, T_A = −20 to +70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage	H Level	V_{IH}		3.15	—	—	V
	L Level	V_{IL}		—	—	1.1	
Output Voltage	H Level	V_{OH}	I_{OH} = 20 µA	V_{CC} − 0.1	V_{CC} − 0.01	—	V
	L Level	V_{OL}	I_{OL} = 20 µA I_{OL} = 2 mA	— —	0.01 —	0.1 0.4	
Input Current DATA, SCK, E, TxD		I_{in}	V_{in} = V_{CC} or GND	—	±1.0	±10.0	µA
Quiescent Supply Current		I_{CC}	FSK Mode	—	8	—	mA
Power-Down Supply Current		I_{CC}	Power-Down Mode 1	—	—	300	µA
		I_{CC}	Power-Down Mode 2	—	—	1	µA

TRANSMIT CARRIER CHARACTERISTICS (V_{CC} = +5.0 Vdc ±10%, T_A = −20 to +70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Carrier Frequency Channel 1	Mark "1"	f_{1M}	Crystal Frequency 3.579545 MHz	974	980	986	Hz
	Space "0"	f_{1S}		1174	1180	1186	
Carrier Frequency Channel 2	Mark "1"	f_{2M}		1644	1650	1656	
	Space "0"	f_{2S}		1844	1850	1856	
Answer Tone		f_{ans}		2094	2100	2106	
Transmit Carrier Level		V_O*	Attenuator = 0 dB RTLA = ∞	—	6	—	dBm
Second Harmonic Energy		V_{2h}*		—	−46	—	dBm
Out-of-Band Energy		V_{OE}*		Figure 1			dBm

* $V_{TXA1} - V_{TXA2}$, R_L = 1.2 kΩ

TRANSMIT ATTENUATOR CHARACTERISTICS (V_{CC} = +5.0 Vdc ±10%, T_A = −20 to +70°C)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Attenuator Range	A_{RNG}		0	—	15	dB
Attenuator Accuracy	A_{ACC}		−0.5	—	+0.5	dB

RECEIVER CHARACTERISTICS (Includes Hybrid, Demodulator and Carrier Detector)
(V_{CC} = + 5.0 Vdc ± 10%, T_A = −20 to +70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Input Impedance		R_{IRX}	RxA Pin (Pin 19)	50	—	—	kΩ
Receiver Carrier Amplitude		V_{IRX}		−48	—	−12	dBm
Carrier Detect	OFF to ON	V_{CDON}	CDA = 1.2 V f_{in} = 1.0 kHz	—	−44	—	dBm
Threshold	ON to OFF	V_{CDOF}		—	−47	—	
Hysterisis ($V_{CDON} - V_{CCDOF}$)		H_{VS}		2	—	—	dB
Carrier Detect Timing	OFF to ON	T_{CDON}	CD1 = 0, CD0 = 0	—	450	—	ms
			CD1 = 0, CD0 = 1	—	15	—	
			CD1 = 0, CD1 = 1	—	15	—	
			CD1 = 1, CD0 = 1	—	80	—	
	ON to OFF	T_{CDOFF}	CD1 = 0, CD0 = 0	—	30	—	
			CD1 = 0, CD0 = 1	—	30	—	
			CD1 = 0, CD0 = 1	—	15	—	
			CD1 = 1, CD0 = 1	—	10	—	

BAND-PASS FILTER CHARACTERISTICS (RxA to FTLC) (V_{CC} = +5.0 Vdc ±10%, T_A = −20 to +70°C)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
FTLC Output Impedance	R_{OFT}		10	—	50	kΩ
Adjacent Channel Rejection	REJ	V_{RXA} = −12 dBm	—	50	—	dB
Pass-Band Gain	G_{PAS}		—	10	—	dB
Group Delay		Low-Band Filter 930–1230 Hz	—	700	—	µs
		High-Band Filter 1600–1900 Hz	—	800	—	

DTMF CHARACTERISTICS (V_{CC} = +5.0 Vdc ±10%, T_A = − 20 to + 70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Tone Output Level	Low Group	V_{fl}*		—	3	—	dBm
	High Group	V_{fh}*		—	4	—	
High Group Pre Emphasis		P_E	Attenuator = 0 dB RTLA = ∞ Crystal Frequency 3.579545 MHz	0	—	3	dB
DTMF Distortion		DIST		—	5	—	%
DTMF Frequency Variation		Δf_V		−1	—	1	%
Out-of-Band Energy		V_{OE}*		Figure 1			dB
Setup Time		t_{osc}		—	4	—	ms

* $V_{TXA1} - V_{TXA2}$, R_L = 1.2 kΩ

CPTD CHARACTERISTICS (V_{CC} = +5.0 Vdc ±10%, T_A = −20 to +70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Bandpass Filter Center Frequency		f_c		—	400	—	Hz
Bandpass Filter – 3 dB Band Width		ΔBW		—	140	—	Hz
Tone Detect Level	OFF to ON	V_{TDON}	CDA = 1.2 V f_{in} = 400 Hz	—	−44	—	dBm
	ON to OFF	V_{TDOF}		—	−47	—	
Tone Detect Timing	OFF to ON	T_{TDON}		—	10	—	ms
	ON to OFF	T_{TDOF}		—	25	—	

DEMODULATOR CHARACTERISTICS (V_{CC} = +5.0 Vdc ±10%, T_A = −20 to +70°C)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Bit Bias	ID	Input Level = – 24 dBm	—	5	—	%
Bit Error Rate	BER	Input Level = – 24 dBm CCITT Line Simulation 511 Bit Pattern S/N = 5 dB	—	0.00001	—	—

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc ±10%, T_A = −20 to +70°C)

Characteristic		Symbol	Conditions	Min	Typ	Max	Unit
Setup Times	DATA to SCK	t_{su}		50	—	—	ns
	SCK to ENB			50	—	—	ns
Hold Time	SCK to DATA	t_h		50	—	—	ns
Recovery Time	ENB to SCK	t_{rec}		50	—	—	ns
Input Rise Time		t_r		—	—	2	µs
Input Fall Time		t_f		—	—	2	µs
Input Pulse Width	ENB, SCK	t_w		50	—	—	ns

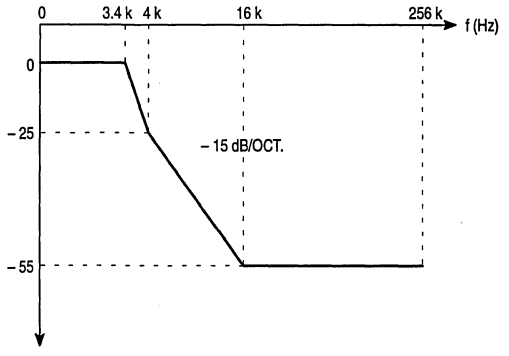


Figure 1. Out-of-Band Energy

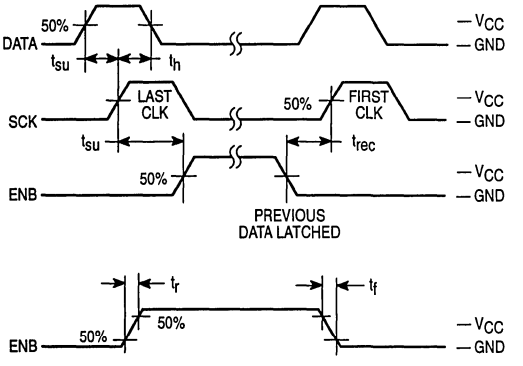


Figure 2. Switching Characteristics

PIN DESCRIPTION

V_{CC}
Positive Power Supply (Pin 15)
This pin is normally tied to the + 5.0 Vdc. A 0.1 µF decoupling capacitor should be used.

GND
Ground Pin (Pin 5)
This pin is normally tied to the 0 V.

GNDA
Analog Ground (Pin 3)
Analog ground is internally biased to $(V_{CC}-V_{SS})/2$. It should be tied to ground through a 0.1 µF and 100 µF capacitor.

X1
Crystal Oscillator Output (Pin 7)
Connecting a 3.579545 MHz ±0.1% crystal between X1 and X2 will cause the transmit frequencies to be within ±64 MHz of nominal. X1 is capable of driving several CMOS gates. An external clock may be applied to X2. X1 should then be left open.

X2
Crystal Oscillator Input (Pin 8)
Refer to X1.

SCK
Shift Resister Clock Input (Pin 13)
This pin is the clock input for the 15-bit shift register. Serial data is loaded into the shift register on the rising edge of this clock.

DATA
Serial Data Input (Pin 12)
This pin is the 15-bit serial data input. This data determines the mode, DTMF signal, transmit attenuation, carrier detect time, channel, and transmit squelch.

ENB
Enable Input (Pin 14)
Data is loaded into the 15-bit shift register when this pin is at a logic low. When this pin transitions from a logic high to low, the data is transferred to the internal latch on the falling edge of ENB. New data loaded into the shift register will not affect the device operation until this pin transitions from high to low. (See Figure 2.)

TxD
Transmit Data Input (Pin 11)
This pin is the transmit data input, The mark frequency is generated when this pin is at the logic high level. The space frequency is generated when the pin is at a logic low.

RxD
Receive Data Output (Pin 10)
This pin is the receive data output. A high logic level of this pin indicates that the mark carrier frequency has been received, and a low logic level indicates the space carrier frequency has been received.

$\overline{SD}$
Carrier/Call Progress Tone Detect (Pin 9)
This pin is the output from the carrier detector or call progress tone detector. This pin works as a carrier detector in the FSK mode and as the call progress tone detector in the CPTD mode. The output goes to a logic low level when the input signal reaches the minimum threshold of the detect level that is adjusted by the CDA voltage. When $\overline{SD}$ = H, the receive data output (RxD) is clamped high to avoid errors that may occur with loop noise. The $\overline{SD}$ pin is also clamped high in the other modes except during the power down mode.

TxA1
Non-Inverting Transmit Analog Carrier Output (Pin 18)
This pin is the line driver non-inverting output of the FSK and tone transmit analog signals. A +6 dBm (Max) differential output voltage can be obtained by connecting a 1.2 kΩ load resistor between Tx1 and Tx2. Attention must be set so as not to exceed this level when an external input is added to the DSI pin. A telephone line (600 Ω) is driven through an external 600 Ω resistor. In this case, the output level becomes about a half of the differential output.

TxA2
Inverting Transmit Analog Carrier Output (Pin 17)
This pin is the line driver inverting output. The signal is equal in magnitude, but 180° out of phase with the TxA1 (refer to TxA1).

RxA
Receive Signal Input (Pin 19)
This pin is the receive signal input. The pin has an input impedance of 50 kΩ (Min).

RxGC
Receive Gain Adjust (Pin 20)
This pin is used to adjust the receive buffer gain. To adjust the gain, the signal from the RxBO through a divider is added as a feedback. This pin may be held open when the gain adjustment is not needed.

RxBO
Receiver Buffer Output (Pin 1)
This pin is the receive buffer output.

DSI
Driver Summing Input (Pin 16)
This pin is the inverting input of the line driver. An external signal is transmitted through an external series resistor R_{DSI}. The differential gain $Gdsi = (V_{TXA1} - V_{TXA2})/V_{DSI}$ is determined by the following equation.

$$G_{DSI} = -2Rf/R_{DSI},\ Rf \approx 20\ k\Omega$$

DSI should be left open when not used.

CDA
Carrier Detect Level/CPTD Level Control (Pin 4)
The carrier/call progress tone detect level is programmed with a CDA pin voltage.

When this pin is held open, the CDA voltage is set to 1.2 V with an internal divider. The detect level is set at −44 dBm (Typ) for off to on, and −47 dBm (Typ) for on to off.The minimum hysteresis is 2 dB. This pin has a very high input impedance so it should be connected to GND with a 0.1 µF capacitor to keep it well regulated. An external voltage may be applied to this pin to adjust the carrier detect threshold. The following equations may be used to find the CDA voltage required for a given threshold voltage.

$$V_{CDA} = 245 \times V_{on}$$
$$V_{CDA} = 347 \times V_{off}$$

FTLC
Filter Test (Pin 2)

This pin is a high-impedance filter output. It may be used to check the receive filter. This pin also may be used as a demodulator input. In normal operation, this pin is connected to the GNDA through a 0.1 µF bypass capacitor. This pin handles very small signals so care must be used with the capacitor's wiring.

TLA
Transmit Carrier Level Adjust (Pin 6)

This pin is used to adjust the transmit carrier level that is determined by the value of the resistor (RTLA) connected between this pin and the GND. The maximum transmit level is obtained when this pin is connected to GND (RTLA = 0).

SERIAL INTERFACE

The following 6 functions are set up with the 15-bit serial data.

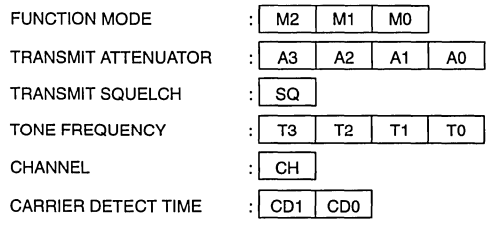


Figure 3 presents the 15-bit serial data timing, starting with the carrier detect time, CD1 followed by the channel, the tone frequency, the transmit squelch, the transmit attenuator and the function mode. This data is loaded into the internal shift register at the rising edge of the SCK signal and latched at the falling edge of the ENB signal.

FUNCTION MODE

Modes are selected from the following 3-bit data (M2–M0, see Table 1).

The following paragraphs describe each function. Table 2 presents each output status.

FSK Mode

The transmitter and the receiver work as a FSK modulator/demodulator. The $\overline{SD}$ pin output is the carrier's detect signal.

Table 1. Function Mode Truth Table

M2	M1	M0	Function Mode
0	0	0	FSK
0	0	1	Analog Loop Back
0	1	0	CPTD
0	1	1	Answer Tone
1	0	0	DTMF
1	0	1	Single Tone
1	1	0	Power-Down 1
1	1	1	Power-Down 2

Analog Loopback Mode

TxA1 connects to the receiver internally and FSK signals are demodulated. The frequency of the receiver is set up with the same frequency as the transmitter. The $\overline{SD}$ pin output is the carrier detect signal. An IC self test is supported with this function.

CPTD Mode

The receiver detects a 400 Hz call progress tone. The detect signal comes from the $\overline{SD}$ pin. The transmitter is disabled.

Answer Tone Mode

The transmitter works as 2100 Hz answer tone generator. The receiver is disabled.

DTMF Mode

The transmitter works as a DTMF tone generator. The receiver is disabled.

Single Tone Mode

The transmitter output is one of DTMF 8 frequencies. The receiver is disabled.

Table 2. Output Status

Function Mode	Output		
	RxD	$\overline{SD}$	TxA1, TxA2
FSK	Received Digital Data	Carrier Detect	FSK
Analog Loop Back			
CPTD	H	CPTD	$V_{CC}/2$
Answer Tone	H	H	Answer Tone
DTMF	H	H	DTMF Tone
Single Tone	H	H	Single Tone
Power Down 1, 2	Hi-Z	Hi-Z	Hi-Z

Power-Down Mode 1

Internal circuits except the oscillator are disabled, and all outputs except the X1 pin goes to the high impedance state. The supply current decreases to 300 μA (Max).

Power-Down Mode 2

All circuits including the oscillator stop working and all outputs go to the high impedance state. The supply current decreases to 1.0 μA (Max).

TRANSMIT ATTENUATOR

Four-bit serial data (A3–A0) sets up the analog transmit level in the FSK, answer tone, DTMF, analog loop back and single tone mode. The range of the transmit attenuator is 0–15 dB in 1 dB steps. The external signal (DSI) is not affected by this attenuator.

TONE FREQUENCY

The DTMF tones or the single tone mode is selected by the 4-bit serial data (T3–T0).

Table 3. Transmit Attenuator Truth Table

A3	A2	A1	A0	Attenuation (dB)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

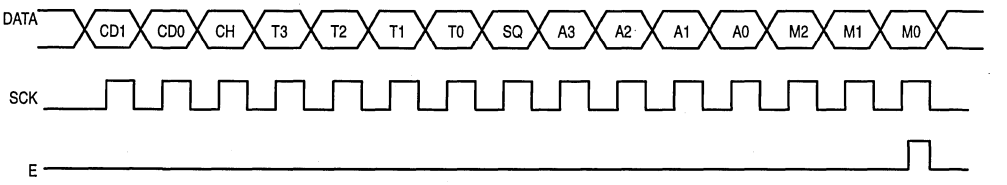


Figure 3. Serial Data Timing

Table 4. Tone Frequency Truth Table

				Tone Frequency (Hz)			
				DTMF Mode			
T3	T2	T1	T0	Low Group	High Group	Keyboard Equivalent	Single Tone Mode
0	0	0	0	941	1633	D	941
0	0	0	1	697	1209	1	697
0	0	1	0	697	1336	2	697
0	0	1	1	697	1477	3	697
0	1	0	0	770	1209	4	770
0	1	0	1	770	1336	5	770
0	1	1	0	770	1477	6	770
0	1	1	1	852	1209	7	852
1	0	0	0	852	1336	8	1336
1	0	0	1	852	1477	9	1477
1	0	1	0	941	1336	0	1336
1	0	1	1	941	1209	*	1209
1	1	0	0	941	1477	#	1477
1	1	0	1	697	1633	A	1633
1	1	1	0	770	1633	B	1633
1	1	1	1	852	1633	C	1633

TRANSMIT SQUELCH

The 1-bit serial data (SQ) controls the transmit analog signal. The FSK signal, DTMF tones, single tone, and answer tone are disabled. The external signal to the DSI will be transmitted at that time. The internal line driver works at all times except during the power-down mode.

SQ	Squelch
1	Enable
0	Disable

CHANNEL

The transmit and receive channel is set up with a 1-bit serial data (CH) when the function mode is either in FSK or analog loop back.

When the function mode is either on the FSK or analog loop back mode, the transmit and receive channel is set up with a 1-bit serial data (CH).

CH	Channel
1	1 (Originate)
0	2 (Answer)

CARRIER DETECT TIME

The carrier detect time (see Figure 4 and Table 5) is set by 2-bit serial data (CD1, CD0). t_{on} indicates the amount of time the carrier is greater than V_{on} threshold must be present before $\overline{SD}$ goes low.

t_{off}, on the other hand, indicates the amount of delay time $\overline{SD}$ goes high after the carrier level becomes lower than V_{off} threshold.

Table 5. Carrier Detect Time Truth Table

CD1	CD0	Carrier Detect Time (Typ)	
		t_{on} (ms)	t_{off} (ms)
0	0	450	30
0	1	15	30
1	0	15	15
1	1	80	10

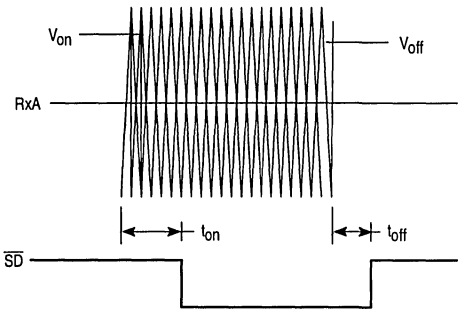


Figure 4. Carrier Detect Timing

POWER-ON RESET

When the power is switched on, this device has the following conditions.

Function Mode	FSK
Transmit Attenuator	0 dB
Transmit Squelch	Enable
Channel	1 (Originate)

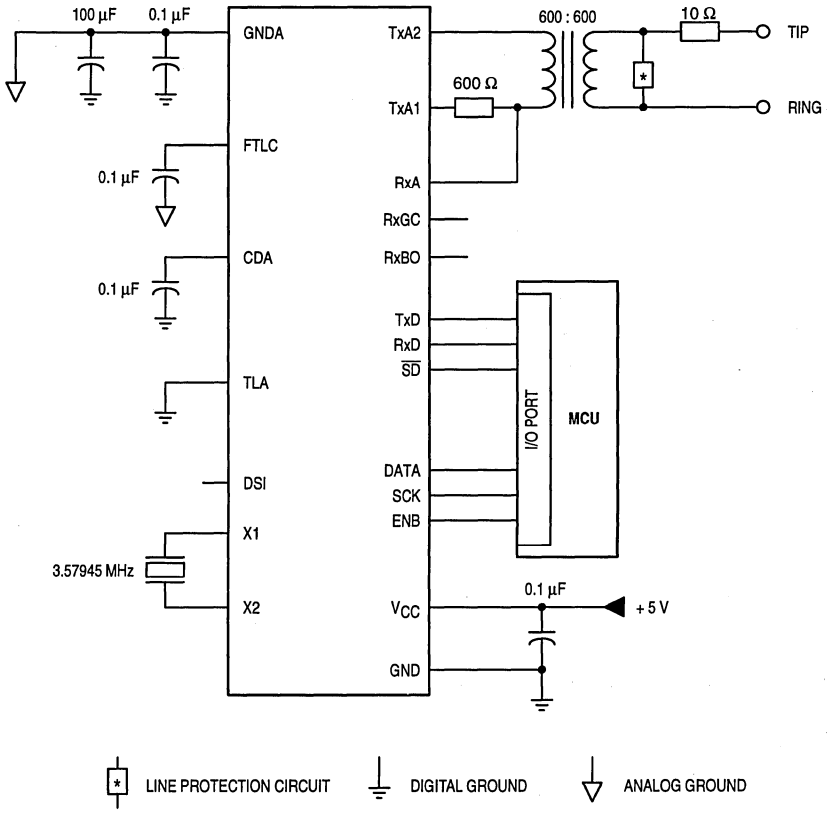


Figure 5. Application Circuit

MC145447

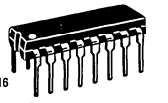
Calling Line Identification (CLID) Receiver with Ring Detector

The MC145447 is a silicon gate HCMOS IC designed to demodulate Bell 202 and V.23 1200-baud FSK asynchronous data. The primary application for this device is in products that will be used to receive and display the calling number, or message waiting indicator sent to subscribers from participating central office facilities of the public switched network. The device also contains a carrier detect circuit and ring detector which may be used to power up the device.

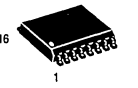
Applications for this device include adjunct boxes, answering machines, feature phones, fax machines, and computer interface products.

The MC145447 offers the following performance features.

- Ring Detector On Chip
- Ring Detect Output for MCU Interrupt
- Power Down Mode, Less Than 1 µA
- Single Supply: +3.5 to +6.0 V
- Pin Selectable Clock Frequencies: 3.68 MHz, 3.58 MHz, or 455 kHz
- Two Stage Power Up for Power Management Control
- Demodulates Bell 202 and V.23



P SUFFIX
PLASTIC DIP
CASE 648

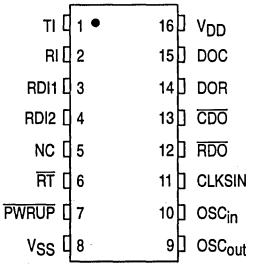


DW SUFFIX
SOG
CASE 751G

ORDERING INFORMATION

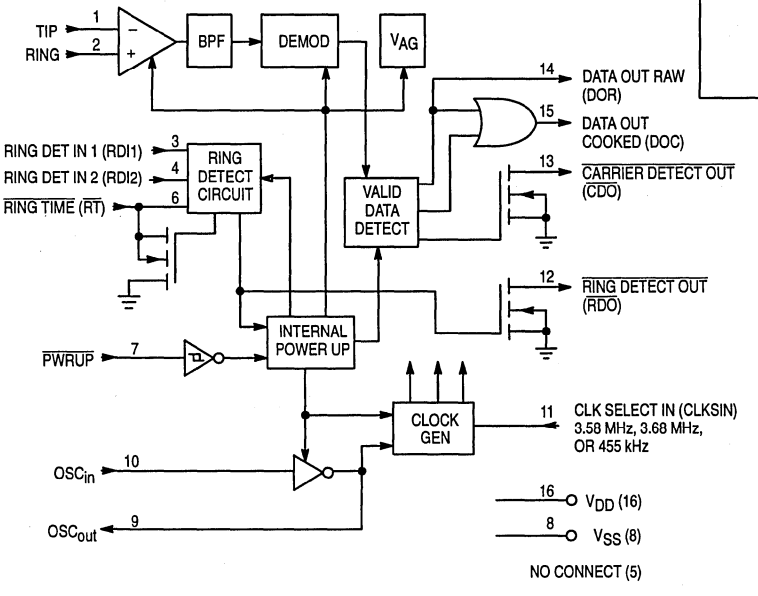
MC145447P	Plastic DIP
MC145447DW	SOG Package

PIN ASSIGNMENT



NC = NO CONNECTION

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Voltages referenced to GND, except where noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +6.0	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD}+0.5	V
DC Current Drain Per Pin	I	±10	mA
Power Dissipation	P_D	20	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−40 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS
(All polarities referenced to V_{SS} = 0 V, V_{DD} = +5 V ±10%, unless otherwise noted, T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	3.5	5	6	V
Supply Current (All Output Pins Unloaded) (See Figure 1) $\overline{RT}$ = 0, $\overline{PWRUP}$ = 1, XTAL = 3.58 MHz	I_{DD}	—	2.4	3	mA
Supply Current (All Output Pins Unloaded) (See Figure 1) $\overline{PWRUP}$ = 0, $\overline{RT}$ = Don't Care, XTAL = 3.58 MHz	I_{DD}	—	6.2	8	mA
Standby Current (All Output Pins Unloaded) (See Figure 1) $\overline{RT}$ = 1, $\overline{PWRUP}$ = 1	I_{STBY}	—	—	1	µA
Input Voltage 0 Level (CLKSIN, OSC_{in})	V_{IL}	—	—	V_{DD} x 0.3	V
Input Voltage 1 Level (CLKSIN, OSC_{in})	V_{IH}	V_{DD} x 0.7	—	—	V
Output Voltage High: V_{DD} = 5 V (DOR, DOC, OSC_{out}) I_{OH} = 40 µA $I_{OH} \le$ 1 µA	V_{OH}	 2.4 4.95	—	—	V
Output Voltage Low: V_{DD} = 5 V (DOR, DOC, OSC_{out}) I_{OL} = 1.6 mA $I_{OL} \le$ 1 µA	V_{OL}	—	—	 0.4 0.05	V
Input Leakage Current (OSC_{in}, CLKSIN, $\overline{PWRUP}$, $\overline{RT}$, RDI1, and RDI2)	I_{in}	—	—	±1	µA
Output Voltage Low: V_{DD} = 5 V ($\overline{RDO}$, $\overline{RT}$, $\overline{CDO}$) I_{OL} = 2.0 mA	V_{OL}	—	—	0.4	V
Input Threshold Voltage Positive Going: V_{DD} = 5 V (RDI1, $\overline{RT}$, $\overline{PWRUP}$) (See Figure 3)	V_{T+}	2.5	2.75	3.0	V
Input Threshold Voltage Negative Going: V_{DD} = 5 V (RDI1, $\overline{RT}$, $\overline{PWRUP}$) (See Figure 3)	V_{T-}	2.0	2.3	2.6	V
RDI2 Threshold	$R_{D2}V_T$	1.0	1.1	1.2	V
TIP/RING Input dc Resistance	R_{in}	—	500	—	kΩ

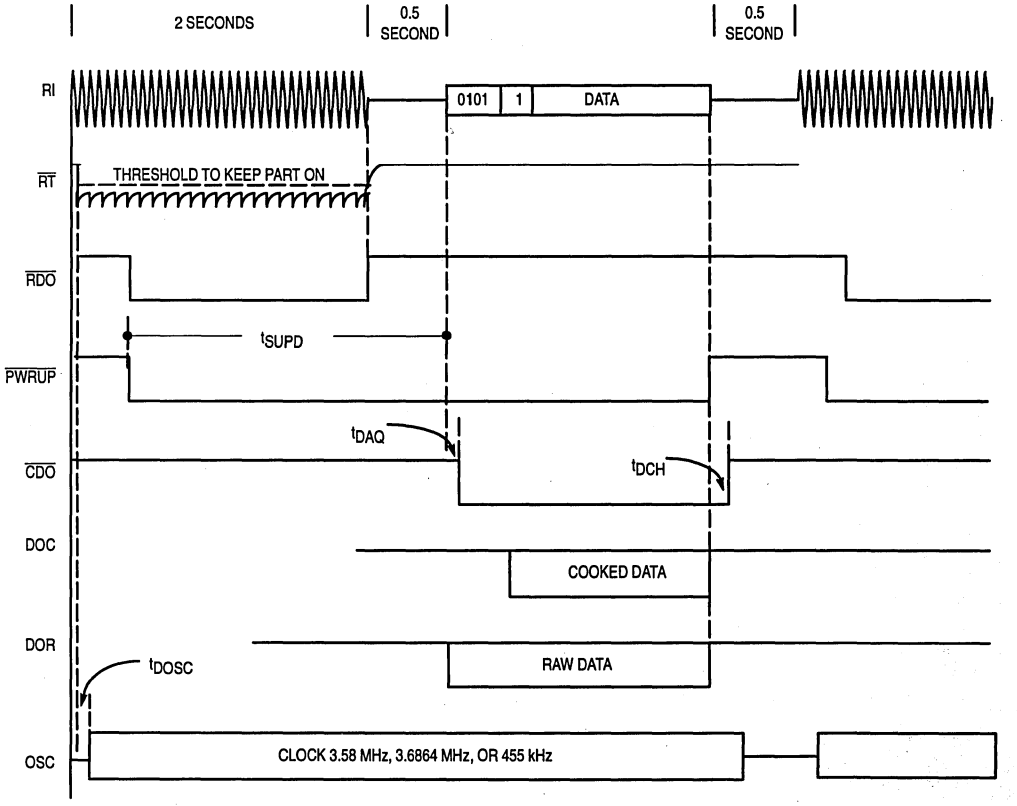
ANALOG CHARACTERISTICS (V_{DD} = +5 V, T_A = +25°C, unless otherwise noted, 0 dBm = 0.7746 Vrms @ 600 Ω)

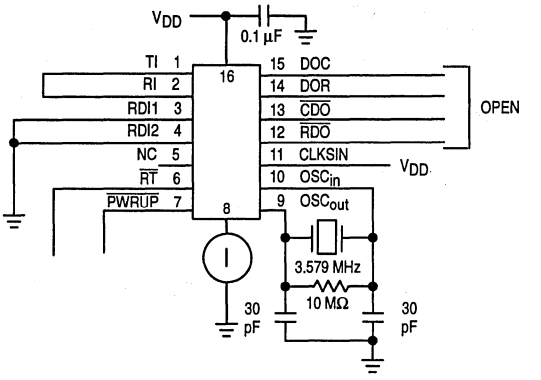
Characteristic		Min	Typ	Max	Unit
Input Sensitivity: TIP and RING (Pins 1 and 2, V_{DD} = +5 V)		−40	−45	—	dBm
Band-Pass Filter (BPF) Frequency Response (relative to 1700 Hz @ 0 dBm)	60 Hz	—	−64	—	dB
	500 Hz	—	−4	—	
	2700 Hz	—	−3	—	
	≥ 3300 Hz	—	−34	—	
Carrier Detect Sensitivity		—	−48	—	dBm

SWITCHING CHARACTERISTICS (V_{DD} = +5 V, C_L = 50 pF, T_A = +25°C)

Description	Symbol	Min	Typ	Max	Unit
OSC Startup	t_{DOSC}	—	2	—	ms
Power-Up Low to FSK (Setup Time)	t_{SUPD}	15	—	—	ms
Carrier Detect Acquisition Time	t_{DAQ}	—	14	—	ms
End of Data to Carrier Detect High	t_{DCH}	8	—	—	ms

TIMING DIAGRAM





RT	PWRUP	I_{DD}	OSC_{in}
1	1	1 µA MAX	DISABLE
0	1	2.4 mA TYP	ENABLE
X	0	6.2 mA TYP	ENABLE

Figure 1. I_{DD} Test Circuit

PIN DESCRIPTIONS

TI
Tip Input (Pin 1)
This input pin is normally connected to the tip side of the twisted pair. It is internally biased to 1/2 supply voltage when the device is in the power up mode. This pin must be dc isolated from the line.

RI
Ring Input (Pin 2)
This input is normally connected to the ring side of the twisted pair. It is internally biased to 1/2 supply voltage when the device is in the power up mode. This pin must be dc isolated from the line.

RDI1
Ring Detect Input 1 (Pin 3)
This input is normally coupled to one of the twisted pair wires through an attenuating network. It detects energy on the line and enables the oscillator and precision ring detection circuitry.

RDI2
Ring Detect Input 2 (Pin 4)
This input to the precision ring detection circuit is normally coupled to one of the twisted pair wires through an attenuating network. A valid ring signal as determined from this input sends the $\overline{RDO}$ (Pin 12) to a logic 0.

$\overline{RT}$
Ring Time (Pin 6)
An RC network may be connected to this pin. The RC time constant is chosen to hold this pin voltage below 2.2 V between the peaks of the ringing signal. $\overline{RT}$ is an internal power-up control and activates only the circuitry necessary to determine if the incoming ring is valid.

$\overline{PWRUP}$
Power Up (Pin 7)
A logic 0 on the $\overline{PWRUP}$ input causes the device to be in the active mode ready to demodulate incoming data. A logic 1 on this pin causes the device to be in the standby mode, if the $\overline{RT}$ input pin is at a logic 1. This pin may be controlled by $\overline{RDO}$ and $\overline{CDO}$ for auto power-up operation. For other applications, this pin may be controlled externally.

V_{SS}
Ground (Pin 8)
Ground return pin is typically connected to the system ground.

OSC_{out}
Oscillator Output (Pin 9)
This pin will have either a crystal or a ceramic resonator tied to it with the other end connected to OSC_{in}.

OSC_{in}
Oscillator Input (Pin 10)
This pin will have either a crystal or a ceramic resonator tied to it with the other end connected to OSC_{out}. OSC_{in} may also be driven directly from an appropriate external source.

CLKSIN
Clock Select Input (Pin 11)
A logic 1 on this input configures the device to accept either a 3.579-MHz or 3.6864-MHz crystal. A logic 0 on this pin configures the part to operate with a 455-kHz resonator.
For crystal and resonator specifications see Table 1.

$\overline{RDO}$
Ring Detect Out (Pin 12)
This open-drain output goes low when a valid ringing signal is detected. $\overline{RDO}$ remains low as long as the ringing signal remains valid. This signal can be used for auto power up, when connected to pin 7.

$\overline{CDO}$
Carrier Detect Output (Pin 13)
When low, this open drain output indicates that a valid carrier is present on the line. $\overline{CDO}$ remains low as long as the carrier remains valid. An 8-ms hysteresis is built in to allow for a momentary drop out of the carrier. $\overline{CDO}$ may be used in the auto power up configuration when connected to $\overline{PWRUP}$.

DOR
Data Out Raw (Pin 14)
This pin presents the output of the demodulator whenever $\overline{CDO}$ is low. This data stream includes the alternate 1 and 0 pattern, and the 150 ms of marking, which precedes the data. At all other times, DOR is held high.

DOC
Data Out Cooked (Pin 15)

This output presents the output of the demodulator whenever $\overline{CDO}$ is low, and when an internal validation sequence has been successfully passed. The output does not include the alternate 1 and 0 pattern. At all other times, DOC is held high.

V_{DD}
Positive Power Supply (Pin 16)

The digital supply pin, which is connected to the positive side of the power supply.

APPLICATIONS INFORMATION

The MC145447 has been designed to be one of the main functional blocks in products targeted for the CLASS (Custom Local Area Signaling Service). market. CLASS is a set of subscriber features now being presented to the consumer by the RBOCs (Regional Bell Operating Companies) and independent TELCOs. Among CLASS features, such as distinctive ringing and selective call forwarding, the subscriber will also have available a service known as Calling Number Delivery (CND) and message waiting. With these services, a subscriber will have the ability to display at a minimum, a message containing the phone number of the calling party, the date, and the time. A message containing only this information is known as a single format message, as shown in Figure 9. An extended message, known as multiple format message, can contain additional information as shown in Figure 10.

The interface should be arranged to allow simplex data transmission from the terminating central office, to the CPE (Customer Premises Equipment), only when the CPE is in an on-hook state. The data will be transmitted in the silent period between the first and second power ring after a voice path has been established.

The data signaling interface should conform to Bell 202, which is described as follows:

- Analog, phase coherent, frequency shift keying
- Logical 1 (Mark) = 1200 ±12 Hz
- Logical 0 (Space) = 2200 ±22 Hz
- Transmission rate = 1200 bps
- Application of data = serial, binary, asynchronous

The transmission level from the terminating C.O. will be −13.5 dBm ±1.0. The expected worst case attenuation through the loop is expected to be −20 dB. The receiver therefore, should have a sensitivity of approximately −34.5 dBm to handle the worst case installations.

Additional information on CLASS services can be obtained from:

BELLCORE CUSTOMER SVS.
1-800-521-2673
201-699-5800 FOREIGN CALLS
201-699-0936 FAX

The document number is: TA-NWT-000030

Title: "Voice Band Data Transmission Interface Generic Requirements"

Figure 7 is a conceptual design of how the MC145447 can be implemented into a product which will retrieve the incoming message and convert it to EIA-232 levels for transmission to the serial port of a PC. With this message and appropriate software, the PC can be used to look up the name and any additional information associated with the caller that had been previously stored.

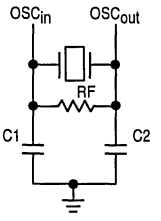
Figure 8 is a conceptual design of an adjunct unit in parallel with an existing phone. This arrangement gives the subscriber CND service without having to replace existing equipment.

Table 1. Oscillator Specifications

Clock Select Pin 11 = 1

Crystal Mode	Parallel
Frequency	3.579 MHz or 3.6864 MHz
R_f	10 MΩ
C1 and C2	30 pF

Source:
Fox Electronics
5570 Enterprise Pkwy.
Ft. Myers, FL 33905
Tel. 813-693-0099



Clock Select Pin 11 = 0

Resonator	#CSB455J
Frequency	455 kHz ±0.5%
R_f	1.0 MΩ
C1 and C2	100 pF

Source:
Murata Manufacturing Co. Ltd.
2200 Lake Park Dr.
Smyrna, GA 30080
Tel. 404-436-1300

Note:
Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing.

FULL-TIME POWER-UP APPLICATION WITH RING DETECTOR CIRCUIT DISABLED

Some MC145447 applications require that the Calling Line Identification Receiver be constantly powered. To ensure that the device is properly reset, a Logic 1 must be applied to $\overline{PWRUP}$ (Pin 7) for a minimum of 10 µs after V_{DD} has reached its full value. It is also necessary that the $\overline{RT}$ pin (Pin 6) be high while $\overline{PWRUP}$ is high. This may be accomplished with an external ring detect signal or MCU generated signal applied to $\overline{PWRUP}$. Alternatively, a power on reset RC network may be used as shown in Figure 6. Rpu and Cpu must be chosen such that the voltage at $\overline{PWRUP}$ meets the logic 1 input threshold requirements for 10 µs after V_{DD} has reached its full value. The power supply rise time on V_{DD} (Pin 16) must also be taken into account when determining Rpu and Cpu. See Figure 3 for a description of the change in input thresholds (V_{T+} and V_{T-}) with respect to V_{DD} for $\overline{PWRUP}$. Also, some applications may not require the ring detect function. In this case, RDI1 (Pin 3) and RDI2 (Pin 4) should be tied to V_{SS} and $\overline{RT}$ tied to V_{DD} as shown in Figure 6.

DESIGN INFORMATION

The circuit in Figure 2 illustrates in greater detail the relationship between device pins 3, 4, 6, and 7.

The external component values shown in Figure 2 are the same as those shown in Figures 7 and 8. When V_{DD} is applied to the circuit in these two figures, the RC network will charge cap C1 to V_{DD} holding $\overline{RT}$ (Pin 6) off. If the $\overline{PWRUP}$ (Pin 7) is also held at V_{DD}, the MC145447 will be in a power down mode, and will consume 1 µA of supply current (Max).

The resistor network (R2–R4) attenuates the incoming power ring applied to the top of R2. The values given have been chosen to provide a sufficient voltage at RDI1 (Pin 3) to turn on the Schmitt trigger input with approximately a 40 Vrms or greater power ring input from tip and ring. When V_{T+} of the Schmitt is exceeded, Q1 will be driven to saturation discharging cap C1 on $\overline{RT}$. This will initialize a partial power up, with only the portions of the part involved with the ring signal analysis enabled, including RDI2 (Pin 4). At this time the MC145447 power consumption is increased to approximately 2.4 mA (typ).

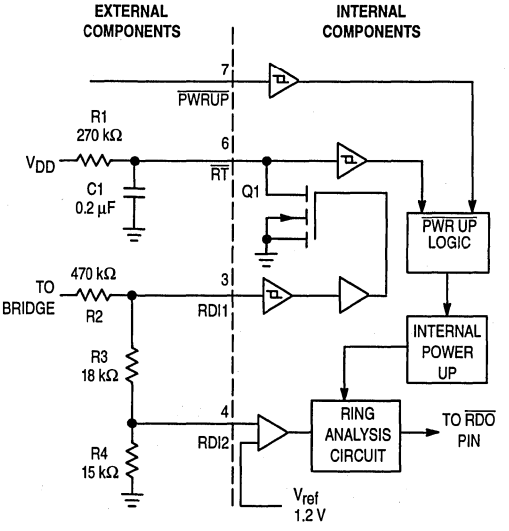


Figure 2.

The value of R1 and C1 must be chosen to hold the $\overline{RT}$ pin voltage below the V_{T+} of the $\overline{RT}$ Schmitt between the individual cycles of the power ring. The values shown will work for ring frequencies of 15.3 Hz (min).

With RDI2 now enabled, a portion of the power ring above 1.2 V is fed to the ring analysis circuit. This circuit is a digital integrator which looks at the duty cycle of the incoming signal. When the input to RDI2 is above 1.2 V, the integrator is counting up at an 800 Hz rate. When the input to RDI2 falls below 1.2 V, the integrator counts down at a 400 Hz rate.

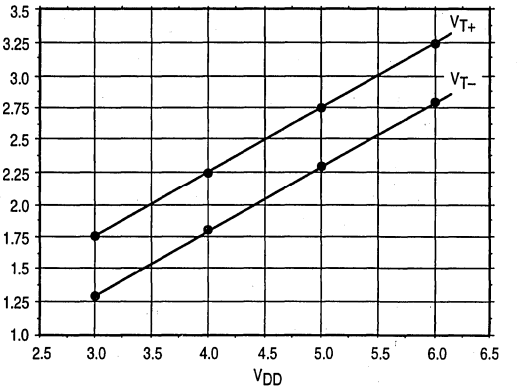


Figure 3. V_{DD} versus V_{T+} and V_{T-}

A ring is qualified when an internal count of binary 48 is reached. The ring is disqualified when the count drops to a binary 32. The number of ring cycles required to qualify the signal will depend on the amplitude of the voltage presented to RDI2. The shortest amount of time needed to do the qualification is approximately 60 ms. The shortest amount of time required for dequalification will be approximately 40 ms.

Once the ring signal is qualified, the $\overline{RDO}$ pin will be sent low. This can be fed back to $\overline{PWRUP}$ as shown in Figure 7, or with a pull-up resistor, can be used as an interrupt to an MCU as shown in Figure 8. In either case, once the $\overline{PWRUP}$ pin is below V_{T-}, the part will be fully powered up, and ready to receive FSK. During this mode, the device current will increase to approximately 6.2 mA (typ). The state of the $\overline{RT}$ pin is now a "don't care" as far as the part is concerned. Normally, however, this pin will be allowed to return to V_{DD}.

After the FSK message has been received, the $\overline{PWRUP}$ pin can be allowed to return to V_{DD} and the part will return to the standby mode, consuming less than 1 µA of supply current. The part is now ready to repeat the same sequence for the next incoming message.

TYPICAL DEMODULATOR PERFORMANCE

The following describes the performance of the MC145447 demodulator in the presence of noise over a simulated Bell 3002 telephone loop.

The Bell 3002 loop represents a worst case local telephone loop in North America. The characteristics of this loop, which affect performance, are high frequency attenuation and Envelope Delay Distortion (EDD) or group delay.

The minimum receiver sensitivity of the MC145447 under these conditions is typically –45 dBm.

The MC145447 achieves a Bit Error Rate (BER) of 1×10^{-5} at a Signal-to-Noise Ratio (SNR) of 15 dB in V.23 operation and at an SNR of 18 dB in Bell 202 operation (see Figures 4 and 5).

All measurements in dBm are referenced to 600 Ω: 0 dBm = 0.7746 Vrms.

All measurements were taken using the MC145460EVK evaluation board.

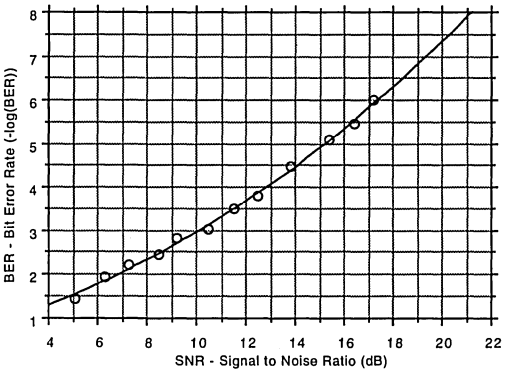


Figure 4. MC145447 V.23 Operation (Typical BER vs SNR)

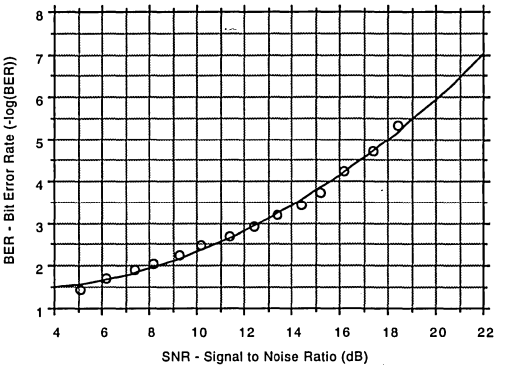


Figure 5. MC145447 Bell 202 Operation (Typical BER vs SNR)

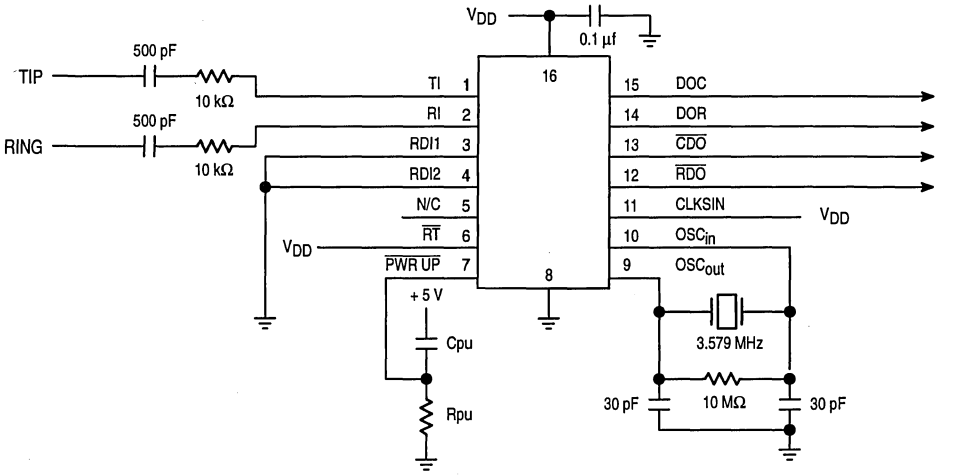
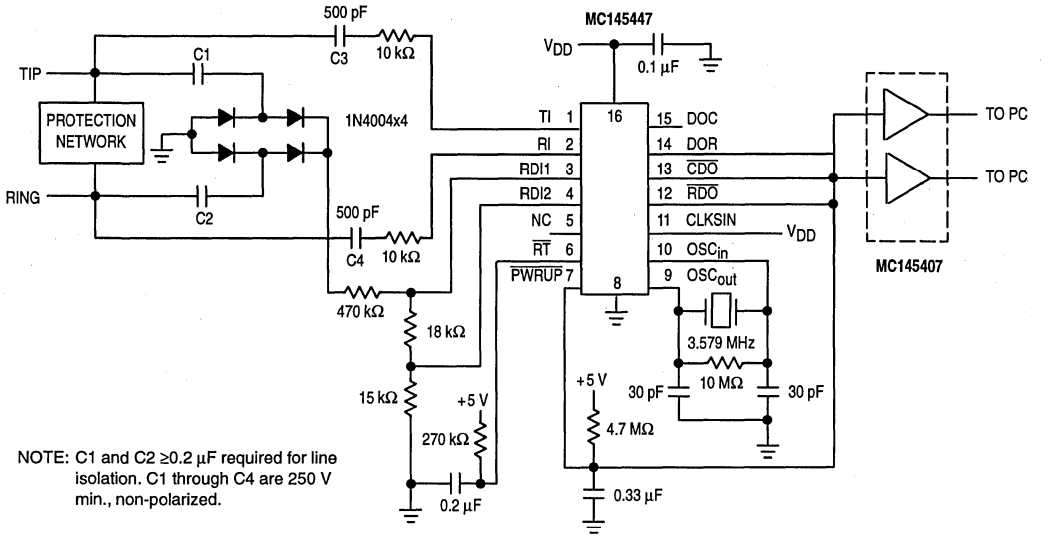


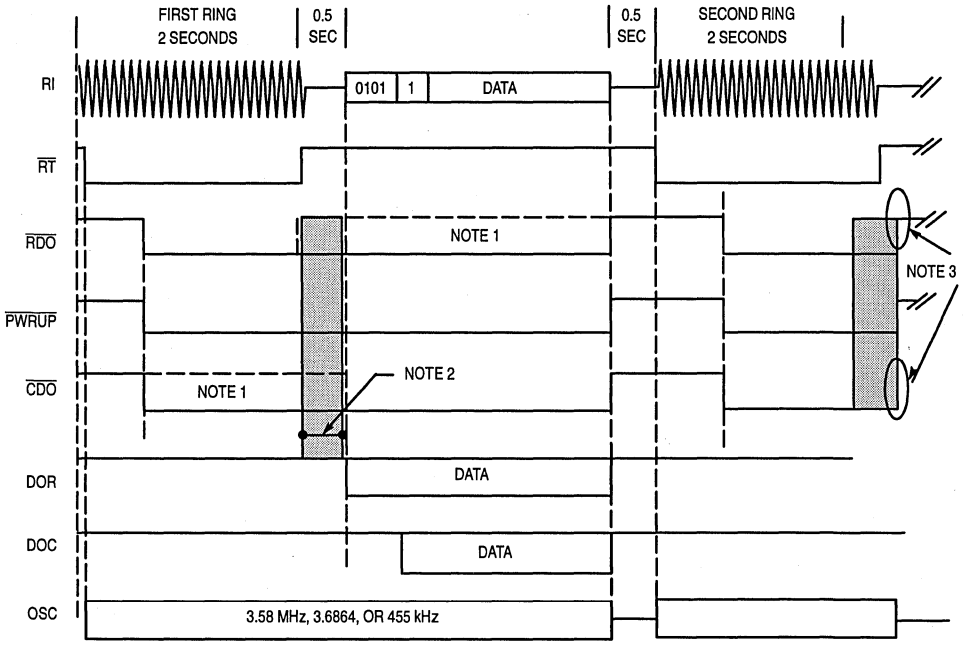
Figure 6.

APPLICATION CIRCUIT



NOTE: C1 and C2 ≥0.2 µF required for line isolation. C1 through C4 are 250 V min., non-polarized.

Figure 7. Partial Implementation of PC Interface to Tip and Ring



NOTES:
1. Wired 'OR' $\overline{RDO}$ with $\overline{CDO}$..
2. Overlap of $\overline{RDO}$ edge with $\overline{CDO}$ edge to ensure part stays in $\overline{PWRUP}$ determined by RC time constant on $\overline{RDO}$, $\overline{PWRUP}$, and $\overline{CDO}$. pin.
3. Part reverts to $\overline{PWR}$ $\overline{ON}$, on rising edge of $\overline{RDO}$ since there is no $\overline{CDO}$.

Timing Diagram for Figure 7

APPLICATION CIRCUIT

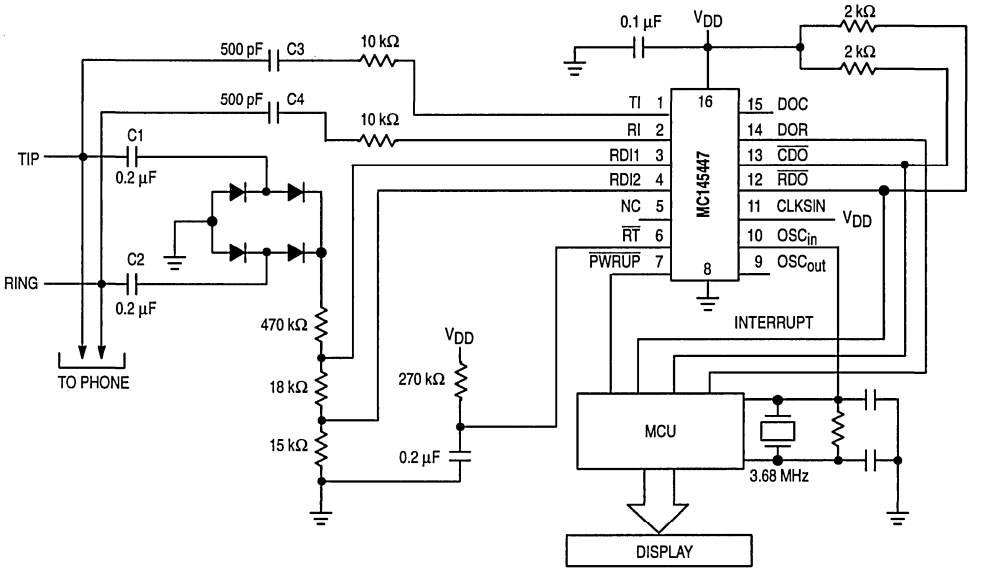
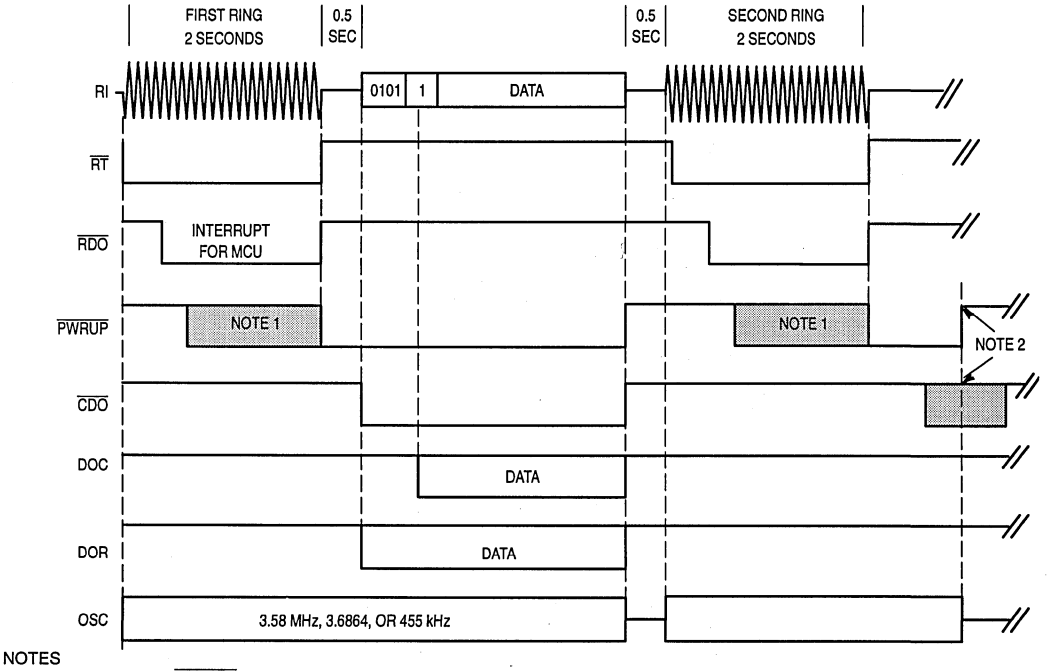


Figure 8. Adjunct Box Concept for Calling Number Display



NOTES
1. MCU must assert $\overline{\text{PWRUP}}$ to MC145447.
2. No data detected, MCU powers down the MC145447.

Timing Diagram for Figure 8

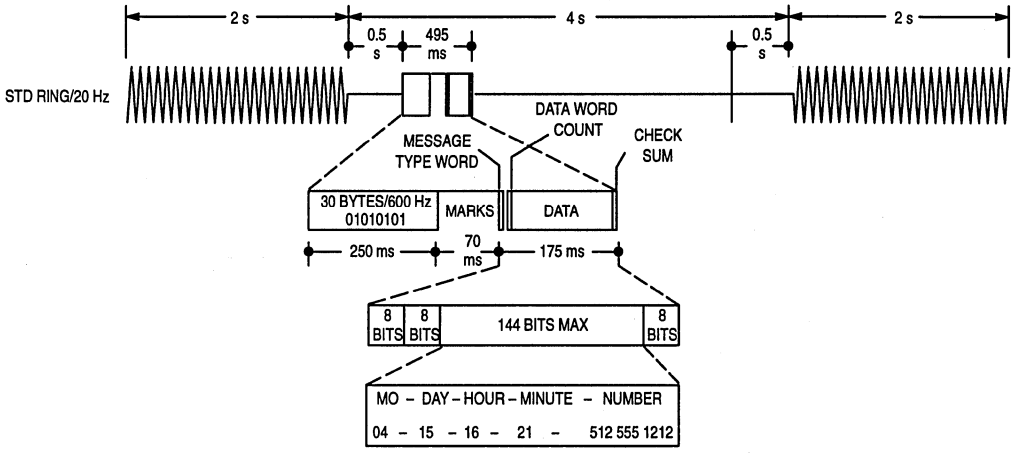


Figure 9. Single Message Format

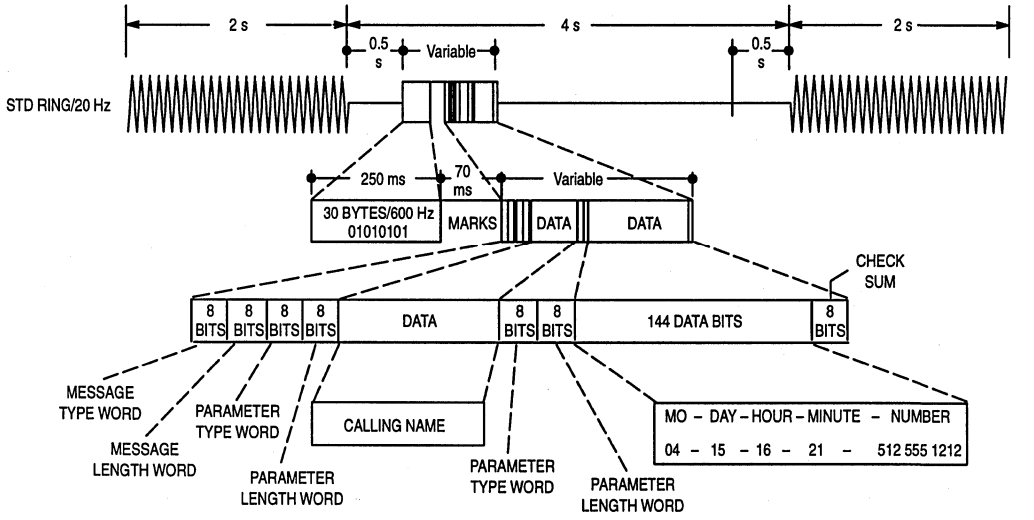


Figure 10. Multiple Message Format

MC145472
MC14LC5472

Technical Summary

U-Interface Transceiver

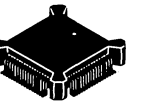
This technical summary provides a brief description of the MC145472 and MC14LC5472 U-Interface Transceivers. A complete data book for the MC145472 is available and can be ordered from your local Motorola sales office. The data book number is MC145472/D.

The MC145472 U-Interface Transceiver is a single chip device intended for the ISDN Basic Access Interface and conforms to the American National Standard known as ANSI T1.601-1992. The MC145472 can be configured for LT or NT applications and performs all necessary Layer 1 functions while utilizing 2B1Q line coding.

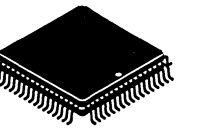
The customer data crossing the U Reference Point consists of two 64 kbps B channels and one 16 kbps D channel in each direction. This data is input to and output from the MC145472 via the industry standard Interchip Digital Link (IDL).

The MC145472 can operate in many different modes. The control of these various modes is provided via special purpose pins and the Serial Control Port (SCP). The SCP conforms to the Motorola Serial Peripheral Interface standard, an industry standard serial microprocessor interface.

The MC14LC5472 is a low power, lower cost version of the MC145472. This technical summary applies to both the MC145472 and MC14LC5472 unless otherwise indicated. The MC14LC5472 differs from the MC145472 in that its maximum power dissipation is 500 mW instead of 700 mW for the MC145472.



FU SUFFIX
PLASTIC
CASE 847

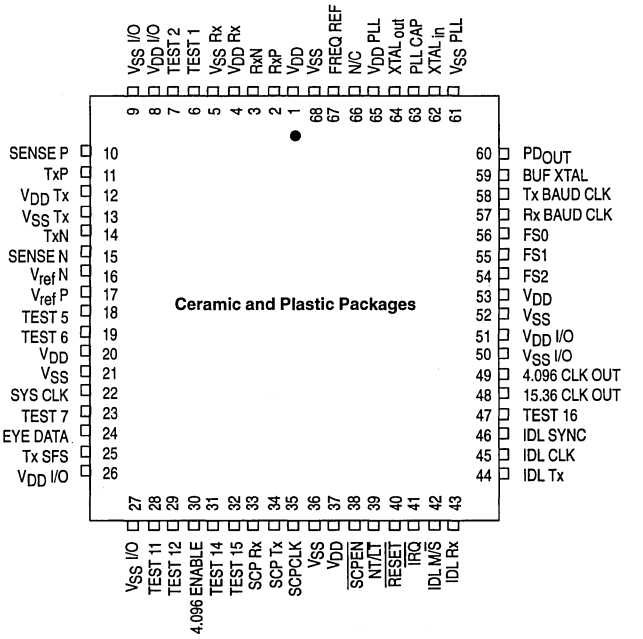


FE SUFFIX
CERAMIC
CASE 847B

ORDERING INFORMATION

MC145472FE	Ceramic
MC14LC5472	Ceramic
MC1454LC72FU	Plastic

PIN ASSIGNMENTS



Also, the MC14LC5472 is available in a 68-lead Plastic Quad Flat Package (PQFP). Both the MC145472 and MC14LC5472 are available in a 68-lead Ceramic Quad Flat Package. The 68-lead PQFP for the MC14LC5472 has a considerably smaller printed circuit board footprint than the 68-lead Ceramic Quad Flat Package. This permits more MC14LC5472s to be placed on a circuit board than would be the case if the MC145472 was used.

Information regarding the generic 2B1Q U-Interface requirement is readily available in standards documents such as ANSI T1.601-1992 and therefore has not been included in this document. The U-Interface equipment designer will find the ANSI document to be a useful reference.

Key features of the MC145472 U-Interface Transceiver include:

- Single Chip 2B1Q Echo Canceling Adaptively Equalized Transceiver
- Conforms to ANSI T1.601-1992, Integrated Services Digital Network (ISDN)-Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification) of the American National Standards Institute, Inc.
- Warm Start Capability
- NT Synchronizes to and Operates with 80 kHz ±32 ppm received signal from LT
- IDL Interface Supports Master, Slave, and Slave-Slave Timing Modes
- On-Chip FIFOs for Transmit and Receive Directions
- MC14LC5472 power consumption is 500 mW maximum when activated
- MC145472 power consumption is 700 mW maximum when activated
- 2B+D Customer Data Provided by the Industry Standard IDL Interface
- Control, Status, and Extended Maintenance Functions Provided through the SCP
- On-Chip Conformance with Activation and Deactivation as Specified in the American National Standard T1.601
- Automatic Handling of Basic Maintenance Functions
- Automatic Internal Compliance with the Embedded Operations Channel (eoc) Protocol as Specified in the American National Standard
- Extended Maintenance Functions Provided through the SCP
- Complete Set of Loop-backs for Both the IDL and U Reference Point Directions
- Pin Selectable for Line Termination (LT) or Network Termination (NT) Applications
- On-Chip 2.5 V Transmit Driver Meeting 1992 Requirement
- Eight Different Choices of Reference Frequency Input in LT Mode
- High Performance CMOS Process Technology
- 5 V Power Supply
- The MC14LC5494EVK is the evaluation platform for the MC14LC5472

ISDN BASIC ACCESS SYSTEM OVERVIEW

ISDN Reference Model

The ISDN Reference Model is shown in Figure 1. This is a general model which can be adapted to many different implementations of the ISDN. The diagram indicates the position of the U Reference Point between the Line Termination (LT) and the Network Termination 1 (NT1) blocks in the model.

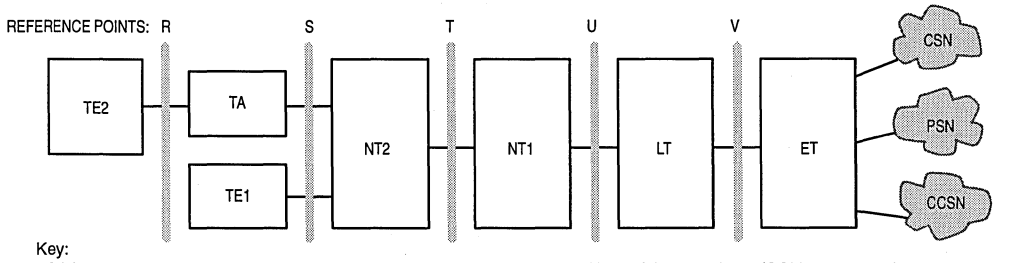
The U-Interface is the physical point of access to the ISDN at the U Reference Point defined in the Reference Model. This interface is a single twisted wire pair supporting full-duplex transmission of digital information at a rate of 160 kbps. The twisted wire pair can extend up to 18,000 feet and may include bridge taps. This interface is often referred to as a Digital Subscriber Line.

U-Interface Transceiver Applications

Some typical ISDN applications of the MC145472 U-Interface Transceiver are shown in Figure 2. This figure shows how Motorola ISDN devices can be configured with other Motorola MCUs and Codecs to implement ISDN equipment such as terminal adapters, NT1s, terminal equipment, line cards, and U-Interface terminals.

A typical non-ISDN pair gain application is shown in Figures 3 and 4. Pair gain is a technique to multiplex two or more analog phone lines over a digital line and recreate them at the customer location.

Figure 5 details how to connect two MC145472 U-Interface transceivers as a U-Repeater.



Key:

CCSN:	Common Channel Signalling Network	NT2:	Network Termination 2 (OSI Layers 2 and 3)
CSN:	Circuit Switched Network	PSN:	Packet Switched Network
ET:	Exchange Termination (C.O. Switch)	TA:	Terminal Adapter
LT:	Line Termination (Line Card)	TE1:	Terminal Equipment 1 (ISDN Terminal)
NT1:	Network Termination 1 (OSI Layer 1 Only)	TE2:	Terminal Equipment 2 (Non-ISDN Terminal)

Figure 1. ISDN Reference Model

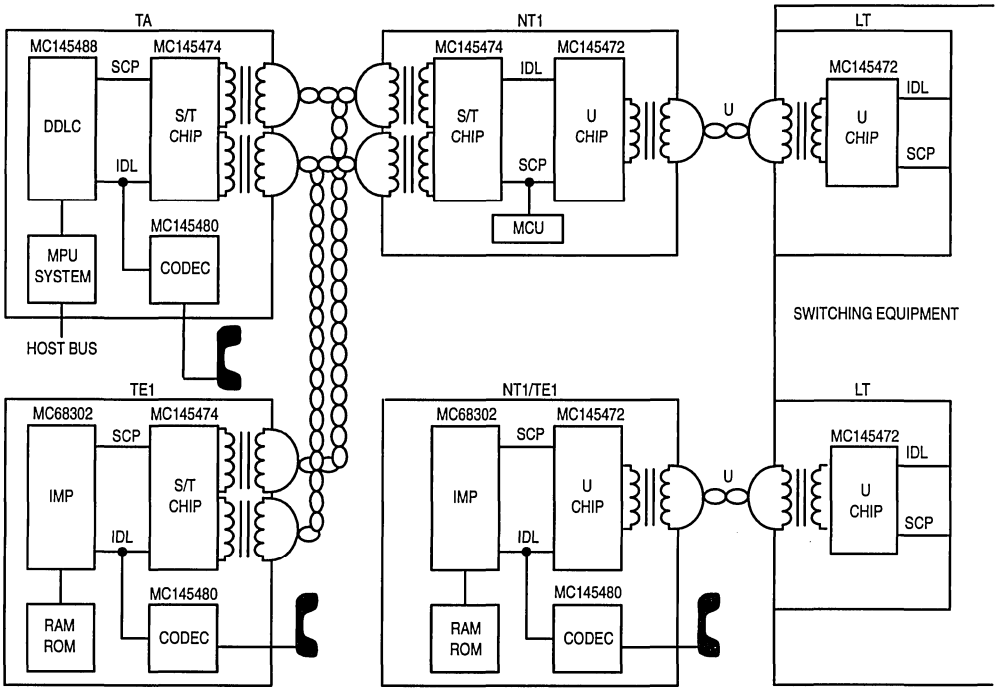


Figure 2. MC145472 Typical ISDN Applications

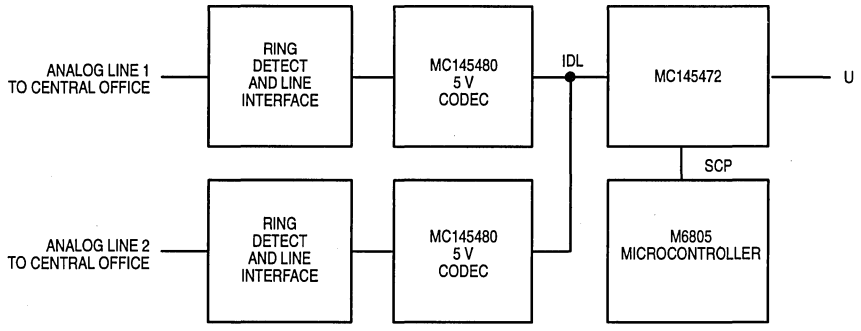


Figure 3. Pair Gain Application, Central Office Terminal

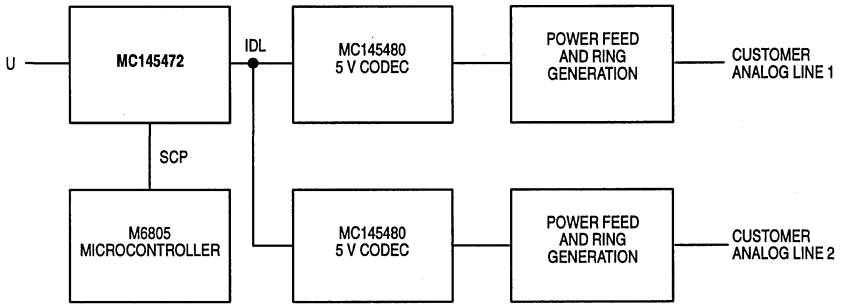
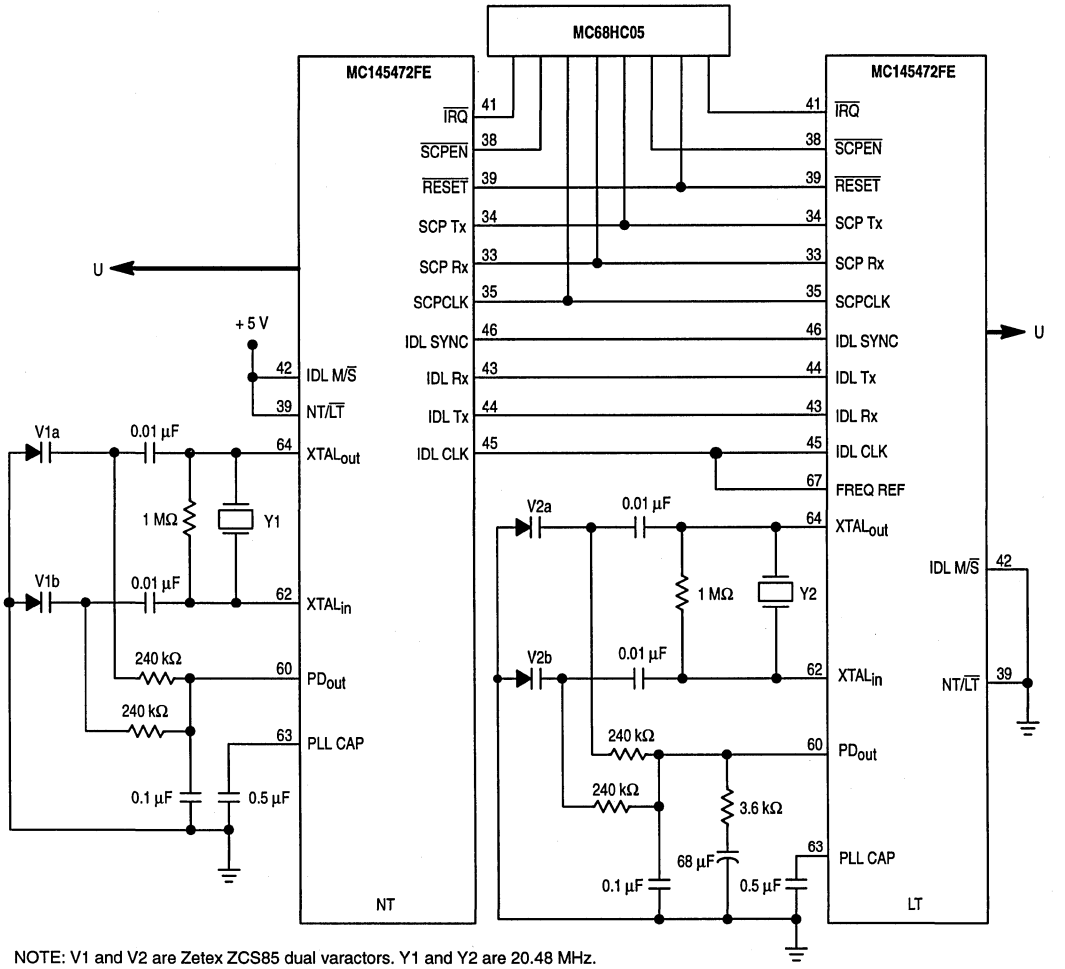


Figure 4. Pair Gain Application, Remote Terminal



NOTE: V1 and V2 are Zetex ZCS85 dual varactors. Y1 and Y2 are 20.48 MHz.

Figure 5. U Repeater Showing Clock and IDL Connections

DEVICE DESCRIPTION

FUNCTIONAL DESCRIPTION

A functional block diagram of the MC145472 U-Interface Transceiver is shown in Figure 6. The MC14572 utilizes mixed analog and digital signal processing circuit technology to implement an adaptively equalized echo canceling full-duplex transmitter/receiver or transceiver.

2B+D data is input to the device at the IDL Rx input. This data is passed through a FIFO prior to being formatted and scrambled in the Superframe Framer. The resulting 160 kbps binary data stream is converted to an 80 kbaud dibit stream which is subsequently converted to four analog amplitudes by the DAC (digital-to-analog converter). The resulting pulse amplitude modulated signal is band limited by the Tx Filter prior to entering the Tx Driver which differentially drives the line coupling circuit to the twisted wire pair.

From the twisted wire pair, information from the far end U-Interface Transceiver is coupled through the external line interface circuit to the differential receiver inputs RxP and RxN. (In this two wire environment, the transmitted signal is also coupled into the receiver inputs.) This combined analog signal is converted to a digital word in a sigma-delta, analog-to-digital converter. After filtering, an adaptively generated replica of the transmitted signal, calculated by the echo canceler, is subtracted from the combined signal leaving only the far end signal. In addition, phase dispersion present in the far end signal is corrected by the Decision Feedback Equalizer. The resulting four level signal is decoded by the slicer to produce a 160 kbps data stream. Timing information is also recovered from the far end signal. The Superframe Deframer descrambles and disassembles the received superframes and passes the received 2B+D data through a FIFO to the IDL Interface where it is available at the IDL Tx output.

Control and status of the device is handled via the SCP, a standard serial microcontroller interface. The SCP provides access to the 4 kbps Maintenance Channel in the U-Interface superframe. In addition, activation and deactivation are handled by an Automatic Activation Controller and the eoc portion of the M channel can be handled automatically with the Automatic eoc Processor.

A crystal oscillator and analog Phase Locked Loop (PLL) are provided to ease clocking requirements for the device.

U-INTERFACE DATA FORMAT

The data transmitted on the U-Interface is organized into a 12 ms long superframe. This superframe consists of eight basic frames each of 1.5 ms in duration. The first nine bauds of each frame are a synchronization word. The next 108 bauds consists of 12×2B+D data. The last three bauds consist of maintenance channel data including a cyclic redundancy check. The first frame of the superframe is identified by its sync word being inverted.

The U-Interface transceiver transmits a four level 2B1Q, (two binary, one quaternary), line code. Two bits are encoded into each baud. Each basic frame consists of 120 bauds or 240 bits of data. The baud symbols are called +3, +1, −1, −3. The B and D channel data is scrambled before being transmitted. Figure 7 gives an example of the 2B1Q line code. Tables 1 and 2 detail the U-Interface superframe formats.

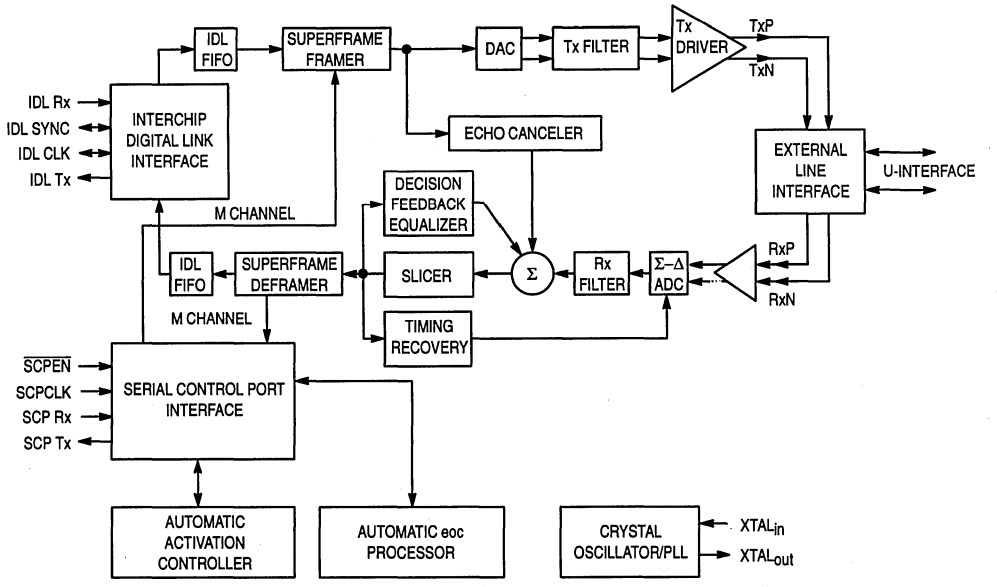


Figure 6. MC145472 Functional Block Diagram

Table 1. Superframe Data Format, LT → NT

	FRAMING	2B+D	OVERHEAD BITS (M1_M6)					
QUAT POSITIONS	1 – 9	10 – 117	118s	118m	119s	119m	120s	120m
BIT POSITIONS	1 – 18	19 – 234	235	236	237	238	239	240
BASIC FRAME #	SYNC WORD	2B+D	M1	M2	M3	M4	M5	M6
1	ISW	12 x 2B+D	eoc a1	eoc a2	eoc a3	act	1	1
2	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	dea	1	febe
3	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	1	crc1	crc2
4	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	1	crc3	crc4
5	SW	12 x 2B+D	eoc a1	eoc a2	eoc a3	1	crc5	crc6
6	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	1	crc7	crc8
7	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	uoa	crc9	crc10
8	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	aib	crc11	crc12

act = start up bit, set = 1 during start up
aib = alarm indication bit (set = 0 to indicate interruption).
crc = cyclic redundancy check: covers 2B + D + M4
dea = turn off bit (set = 0 to indicate turn off)
febe = far end block error
uoa = U-only-activation

1 = reserved bit for future standard (set = 1)
eoc = embedded operations channel
a = address bit
dm = data/message indicator (0 = data, 1 = message)
i = information bit

Table 2. Superframe Data Format, NT → LT

	FRAMING	2B+D	OVERHEAD BITS (M1_M6)					
QUAT POSITIONS	1 – 9	10 – 117	118s	118m	119s	119m	120s	120m
BIT POSITIONS	1 – 18	19 – 234	235	236	237	238	239	240
BASIC FRAME #	SYNC WORD	2B+D	M1	M2	M3	M4	M5	M6
1	ISW	12 x 2B+D	eoc a1	eoc a2	eoc a3	act	1	1
2	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	ps1	1	febe
3	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	ps2	crc1	crc2
4	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	ntm	crc3	crc4
5	SW	12 x 2B+D	eoc a1	eoc a2	eoc a3	cso	crc5	crc6
6	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	1	crc7	crc8
7	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	sai	crc9	crc10
8	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	1	crc11	crc12

act = start up bit, set = 1 during start up.
crc = cyclic redundancy check: covers 2B + D + M4
cso = cold start only (set = 1 for cold start only)
febe = far end block error
ntm = NT in test mode bit (set = 0 to indicate test mode)
sai = S-active indicator bit (optional, set = 1 for S/T activity)

1 = reserved bit for future standard (set = 1)
eoc = embedded operations channel
a = address bit
dm = data/message indicator (0 = data, 1 = message)
i = information bit
ps1, ps2 = power status bits (set = 0 to indicate power problems)

PIN FUNCTIONALITY

Tables 3 through 7 list the MC145472 pins in functional groups and provide brief pin descriptions. For more detailed information refer to the MC145472 data book.

MODE SELECTION

These pins are used to select the operating mode of the MC145472 U-Interface transceiver.

The RESET pin is a schmitt trigger input and holds the MC145472 in a hardware reset condition when at logic 0.

The NT/$\overline{LT}$ input pin selects the operating mode of the MC145472. When at logic 1 the U-Interface transceiver is in NT mode. When at logic 0 the U-Interface transceiver is in LT mode.

Figures 8 and 9 show typical LT and NT mode connections, respectively.

INTERCHIP DIGITAL LINK (IDL) INTERFACE

The IDL Interface consists of five pins: IDL M/$\overline{S}$, IDL SYNC, IDL CLK, IDL Tx, and IDL Rx. With the IDL M/$\overline{S}$ pin the IDL Interface can be configured as an IDL Master (IDL SYNC and IDL CLK are outputs) or an IDL Slave (IDL SYNC and IDL CLK are inputs). The IDL Interface receives 2B+D data on the IDL Rx pin and buffers it through a FIFO to the Superframe Framer (See Figure 6). Simultaneously, this block accepts 2B+D data from the Superframe Deframer, buffers it through a FIFO, and transmits it out the IDL Tx pin. Figure 10 shows the IDL data formats.

Table 3. Quick Reference to Power Supply and Mode Selection Pins

Power Supply Pins		
Pin Name	**Pin No.**	**Pin Description**
V_{DD}	1, 20, 37, 53	Positive power supply, nominally + 5 V.
V_{SS}	21, 36, 52, 68	Negative power supply, nominally ground.
V_{DD} Rx	4	Positive power supply for analog receive circuits, nominally + 5 V.
V_{SS} Rx	5	Negative power supply for analog receive circuits, nominally ground.
V_{DD} Tx	12	Positive power supply for analog transmit circuits, nominally + 5 V.
V_{SS} Tx	13	Negative power supply for analog transmit circuits, nominally ground.
V_{DD} I/O	8, 26, 51	Positive power supply for input and output circuits, nominally + 5 V.
V_{SS} I/O	9, 27, 50	Negative power supply for input and output circuits, nominally ground.
V_{DD} PLL	65	Positive power supply for phase locked loop circuits, nominally + 5 V.
V_{SS} PLL	61	Negative power supply for phase locked loop circuits, nominally ground.
Mode Selection Pins		
Pin Name	**Pin No.**	**Pin Description**
$\overline{RESET}$	40	Hardware reset when at a logic low, normal operation when at a logic high. This pin has a Schmitt trigger input.
NT/$\overline{LT}$	39	Hardware selection of LT (logic low) and NT (logic high) operating mode.

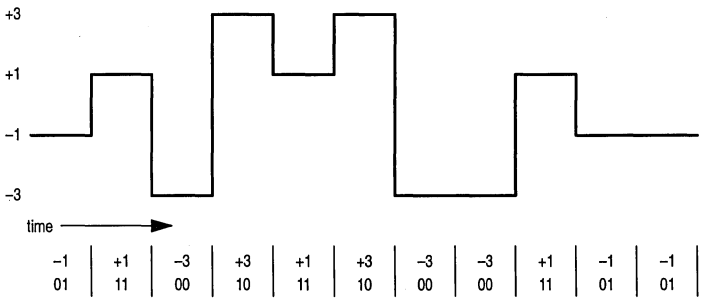


Figure 7. 2B1Q line code

Table 4. Quick Reference to IDL and SCP Pins

Interchip Digital Link (IDL) Interface Pins		
Pin Name	**Pin No.**	**Pin Description**
IDL M/$\overline{S}$	42	Selects between IDL Master (IDL CLK and IDL SYNC are outputs) and IDL Slave (IDL CLK and IDL SYNC are inputs) modes. Logic high selects IDL Master mode and logic low selects IDL Slave mode.
IDL SYNC	46	8 kHz IDL frame synchronization input (IDL Slave mode) or output (IDL Master mode).
IDL CLK	45	Bit clock input (IDL Slave mode) or output (IDL Master mode) for serial transfer of 2B+D data at IDL Tx and IDL Rx.
IDL Tx	44	This is the IDL output for the 2B+D data.
IDL Rx	43	This is the IDL input for the 2B+D data.
Serial Control Port (SCP) Interface Pins		
Pin Name	**Pin No.**	**Pin Description**
$\overline{SCPEN}$	38	SCP Enable Input held low selects the device for a read or write operation to the SCP.
SCPCLK	35	SCP Clock is an input which clocks the SCP data.
SCP Tx	34	SCP data output.
SCP Rx	33	SCP data input.
$\overline{IRQ}$	41	Open drain output held low during an interrupt condition.

Table 5. Quick Reference to 2B1Q Interface Pins

2B1Q Interface Pins		
Pin Name	**Pin No.**	**Pin Description**
TxP	11	Positive output of the differential transmit driver.
TxN	14	Negative output of the differential transmit driver.
SENSE P	10	This pin senses the amplitude of the positive transmit driver output.
SENSE N	15	This pin senses the amplitude of the negative transmit driver output.
RxP	2	Positive input to the differential receive circuit.
RxN	3	Negative input to the differential receive circuit.
V_{ref} P	17	Positive input for off chip voltage reference. Connect a 0.1 µF ceramic capacitor between this pin and V_{ref} N.
V_{ref} N	16	Negative input for off chip voltage reference. Connect a 0.1 µF ceramic capacitor between this pin and V_{ref} P.
Tx BAUD CLK	58	This pin provides an 80 kHz clock output corresponding to the transmitted 2B1Q bauds.
Rx BAUD CLK	57	This pin provides an 80 kHz clock output corresponding to the received 2B1Q bauds.
EYE DATA	24	Once per received baud period, this pin outputs at a rate of 10.24 Mbps a serial digital word which represents the recovered 2B1Q signal or eye pattern.
SYS CLK	22	A 10.24 MHz clock output derived from the 20.48 MHz crystal oscillator which may be used to sample EYE DATA.
Tx SFS	25	Generates an output pulse once every transmitted superframe.

Table 6. Quick Reference to Phase Locked Loop and Test Pins

Phase Locked Loop and Clock Pins		
Pin Name	**Pin No.**	**Pin Description**
FREQ REF	67	In LT mode this input accepts one of eight possible stable input frequencies which is frequency multiplied to 20.48 MHz, the device's master clock frequency. Connect this pin high or low in NT mode. This pin has a Schmitt trigger input.
FS0 FS1 FS2	56 55 54	The state of these three inputs indicates the frequency being applied to the FREQ REF pin. Connect these pins low or high in NT mode.
$XTAL_{in}$	62	This is the input of the 20.48 MHz crystal oscillator amplifier.
$XTAL_{out}$	64	This is the output of the 20.48 MHz crystal oscillator amplifier.
BUF XTAL	59	Buffered 20.48 MHz square wave output.
PD_{out}	60	Output of the PLL phase detector.
PLL CAP	63	Connect a 0.1 µF ceramic capacitor from this pin to ground.
15.36 CLK OUT	48	Buffered 15.36 MHz output.
4.096 CLK OUT	49	Buffered 4.096 MHz output.
4.096 ENABLE	30	When tied high this input enables the buffered 4.096 MHz clock output.

Table 7. Quick Reference to Test Pins

Test Pins		
Pin Name	**Pin No.**	**Pin Description**
TEST 5, 7, 11, 12, 14, 15, 16	18, 23, 28, 29, 31, 32, 47	Test pins for Motorola use. These pins should be connected to ground for normal operation.
TEST 1, 2, 6	6, 7, 19	Test pins for Motorola use. These pins should be left open circuit for normal operation.

The IDL interface can operate in IDL slave mode or IDL master mode. This is independent of the transceiver being in LT or NT mode. Normally, IDL slave mode is used when the MC145472 is configured as an LT and IDL master mode is used when the MC145472 is configured as an NT. The MC145472 can be used in slave-slave applications. Refer to the complete MC145472 data book for further details.

SERIAL CONTROL PORT (SCP) INTERFACE

The MC145472 is equipped with an industry standard SCP Interface. The SCP is used by an external controller, such as an MC6805 family microcontroller, MC145488 Dual Data Link Controller, or MC68302 Integrated Multiprotocol Processor, to communicate with the U-Interface Transceiver.

The SCP is a full-duplex, four-wire interface with control and status information passed to and from the U-Interface Transceiver. The SCP Interface consists of a transmit output, a receive input, a data clock, and an enable signal. These device pins are known as SCP Tx, SCP Rx, SCP CLK, and $\overline{SCPEN}$, respectively. The SCP Clock determines the rate of exchange of data in both the transmit and receive directions, and the SCP Enable signal governs when this exchange is to take place. The four-wire SCP Interface is supplemented with an interrupt request line, $\overline{IRQ}$, for external microcontroller notification of an event requiring service.

The operation and configuration of the MC145472 is controlled by setting the state of its control registers and monitoring its status registers. The control, status, and M channel data registers reside in six 4-bit wide Nibble Registers, one 12-bit wide "Nibble Register", and sixteen 8-bit wide Byte Registers. Figures 11 and 12 are examples of how data is transferred over the SCP.

2B1Q INTERFACE

Figure 13 shows the recommended 2B1Q interface network for connection to the U-Interface and component specifications are shown in Table 8.

NOTE

Motorola continues to qualify several third party sources for the 2B1Q Interface transformer. Contact your local Motorola representative or the Motorola factory applications staff for the latest information regarding component sourcing.

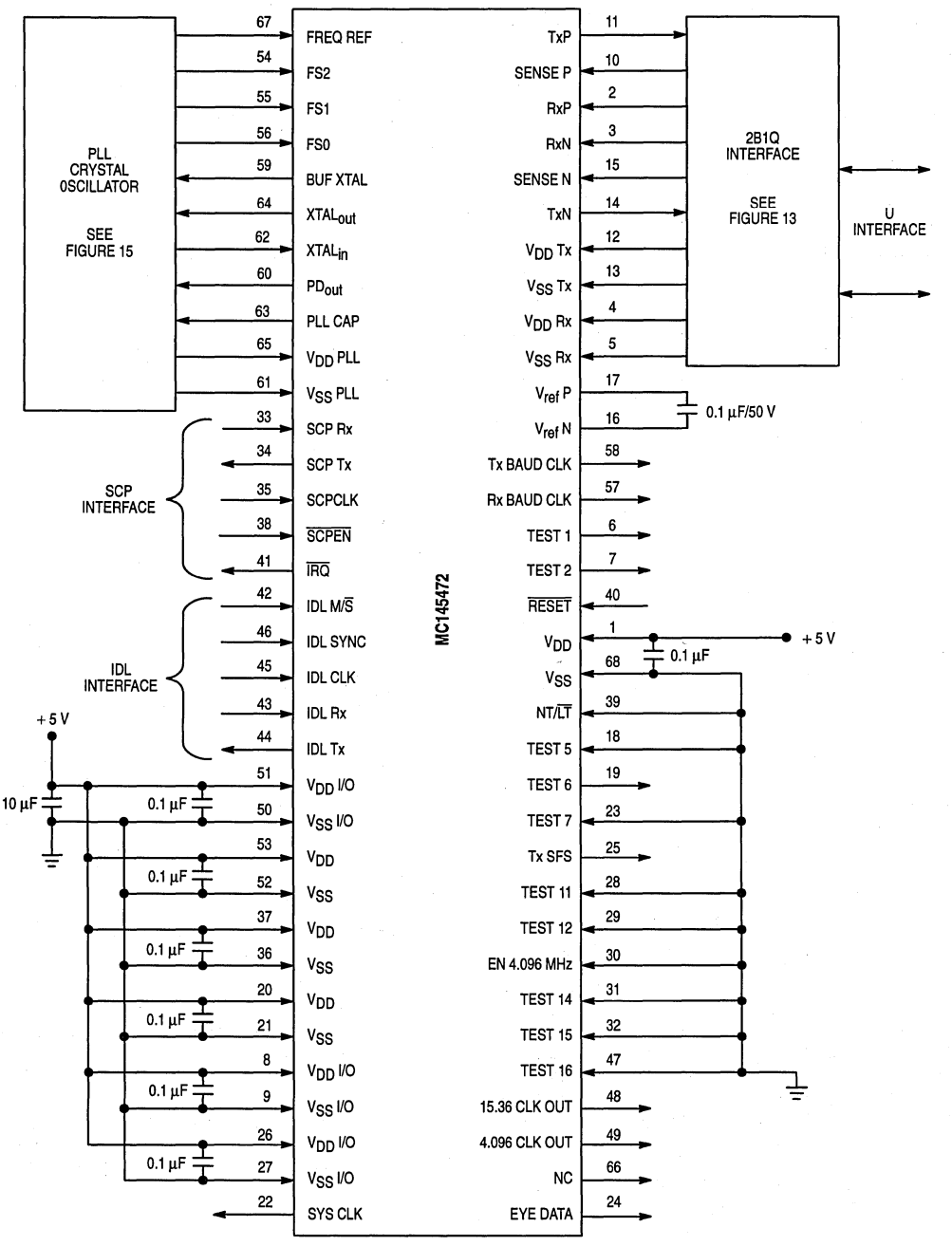


Figure 8. Typical LT Mode Connections

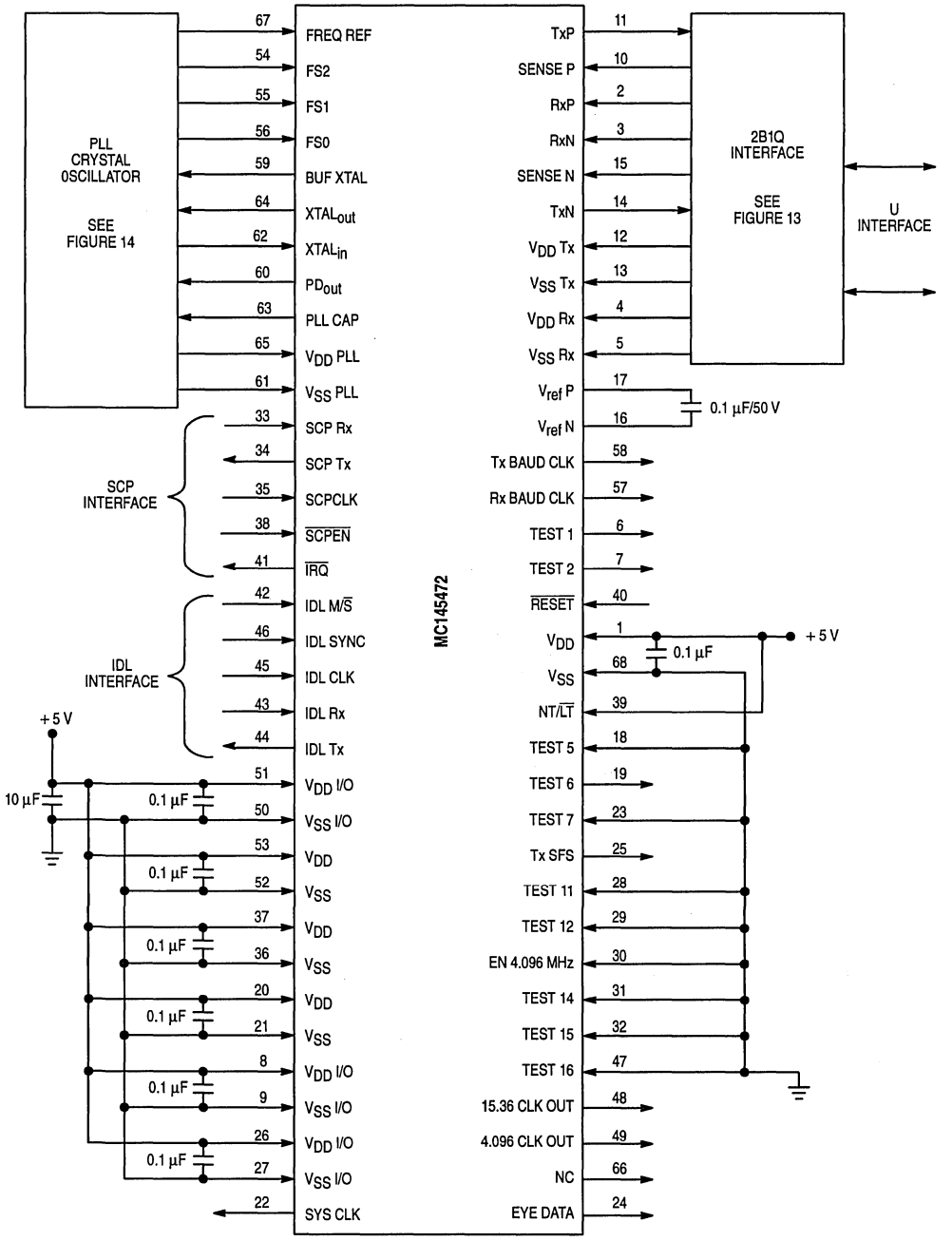
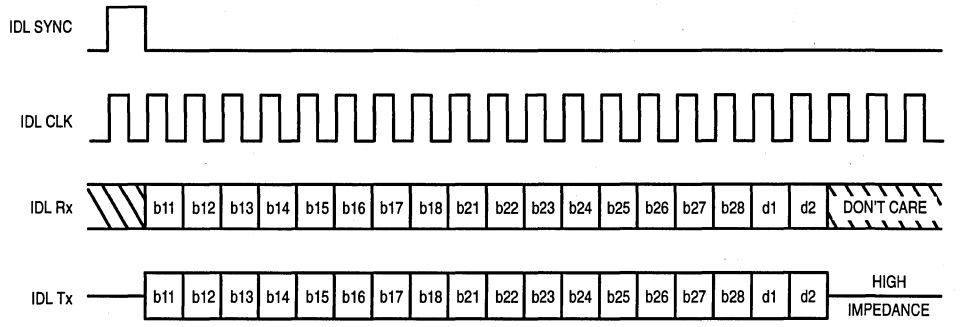
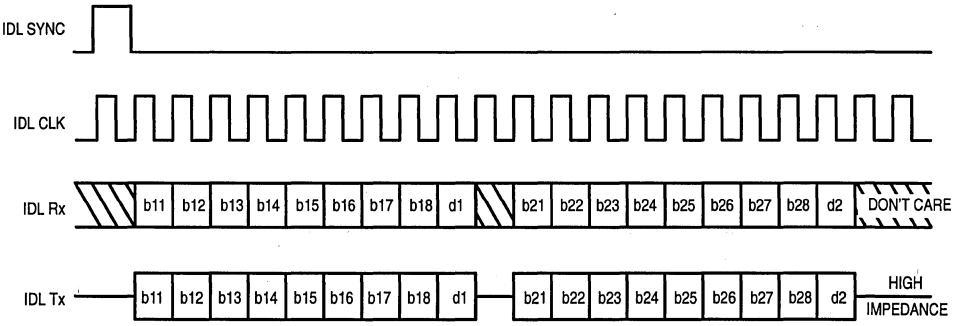


Figure 9. Typical NT Mode Connections



a. IDL Interface Timing in 8-Bit Mode



b. IDL Interface Timing in 10-Bit Mode

Figure 10. IDL Interface Data Formats

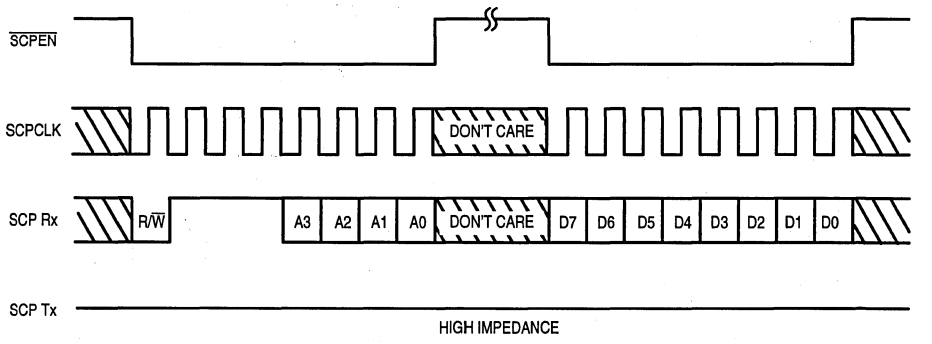


Figure 11. SCP Byte Register Write Operation Using Double 8-Bit Transfer

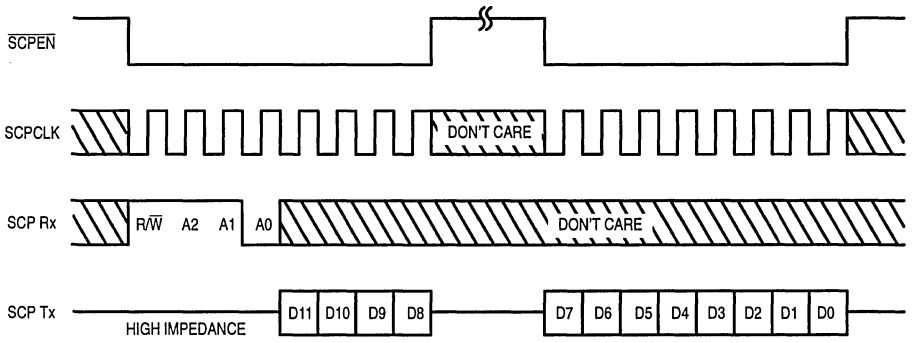


Figure 12. SCP Register R6 Read Operation

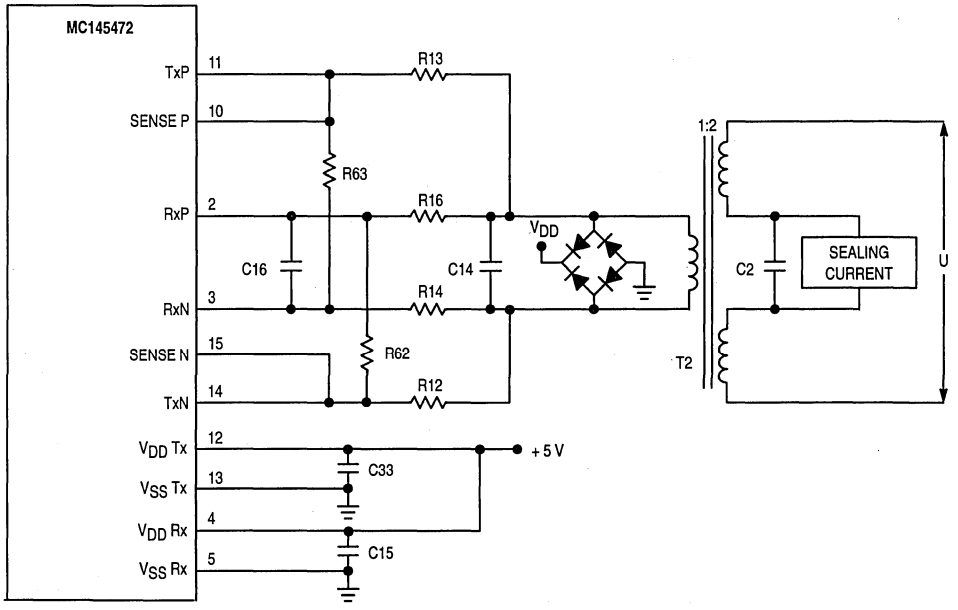


Figure 13. Typical 2B1Q Interface Schematic

Table 8. Line Interface Component Values

Component	Description
C2	1.0 µF, 100 V, 10%, low distortion capacitor
C14	0.033 µF, 50 V, 10%, low distortion capacitor.
C15	0.1 µF ceramic, 50 V
C16	270 pF, or nearest commercial value, 10%, silver mica or other low distortion, high quality capacitor.
C33	0.1 µF ceramic, 50 V
R12	14.3 Ω, 1%, metal film or other high quality low distortion resistor.
R13	14.3 Ω, 1%, metal film or other high quality low distortion resistor.
R14	1.00 kΩ, 1% metal film or other high quality low distortion resistor
R16	1.00 kΩ, 1% metal film or other high quality low distortion resistor
R62	1.69 kΩ, 1% metal film or other high quality low distortion resistor
R63	1.69 kΩ, 1% metal film or other high quality low distortion resistor
T2	Pulse transformer, 1:2 turns ratio.
Diode Bridge	4 x 1N4001

NOTE: R12, R13, C14, and C16 are specific to Dale transformer part number PT-200-02. Motorola does not warrant this transformer, and in no way suggests that this is the only appropriate transformer.

Crystal Oscillator Or Phase-Locked Loop (PLL)

These pins provide access to the phase detector and crystal oscillator portions of the U-Interface Transceiver PLL. A 15.36 MHz and a 4.096 MHz clock output are available for other devices.

In the LT mode, the PLL synchronizes a 20.48 MHz crystal oscillator to one of eight possible reference frequencies supplied by the switching equipment. This phase locked clock assures that the transmitted 2B1Q signal is synchronized to the frequency reference supplied at the FREQ REF pin. In addition, the very low frequency response (≈1 Hz) of the PLL loop filter limits jitter present in the frequency reference. Refer to Figures 14 and 15 for details of the loop filter network and voltage controlled crystal oscillator and Table 11 for suggested component values.

In the NT mode there is both an analog and a digital PLL. The analog PLL synchronizes the 20.48 MHz crystal oscillator to the recovered 2B1Q signal. The digital PLL synchronizes the IDL clock to the recovered 2B1Q signal and also updates the analog PLL on a regular basis. This ensures that the recovered timing is synchronized to the signal received from the LT. In NT mode the U-Interface Transceiver can lock to 80 kbaud ±32 ppm receive signals when the recommended VCXO circuit is used.

The FREQ REF pin is a Schmitt trigger digital input which provides the reference frequency for the phase locked loop in LT mode. The eight possible frequencies include: 2.048, 2.560, 4.096, 7.680, 8.192, 10.24, 15.36, and 20.48 MHz.

The three frequency select inputs (FS0–FS2) are used to select one of the eight possible reference frequencies which may be used to drive the Frequency Reference Input when the device is in the LT mode.

$XTAL_{in}$ and $XTAL_{out}$ are the oscillator pins. A 20.48 MHz pullable crystal and other components may be connected to $XTAL_{in}$ and $XTAL_{out}$ to form a voltage controlled crystal oscillator in the LT or NT modes.

PD_{out} is the output of the on-chip phase detector of the PLL. PD_{out} is a current source output of approximately 15 µA and connects to the PLL filter network.

PLL CAP must have a 0.1 µF capacitor connected between it and ground.

Clock Outputs

BUF XTAL is the buffered output from the 20.48 MHz oscillator and can be used to drive the $XTAL_{in}$ pin of other MC145472 devices in the same system. BUF XTAL must not be used as a microprocessor clock since it is turned off after a reset.

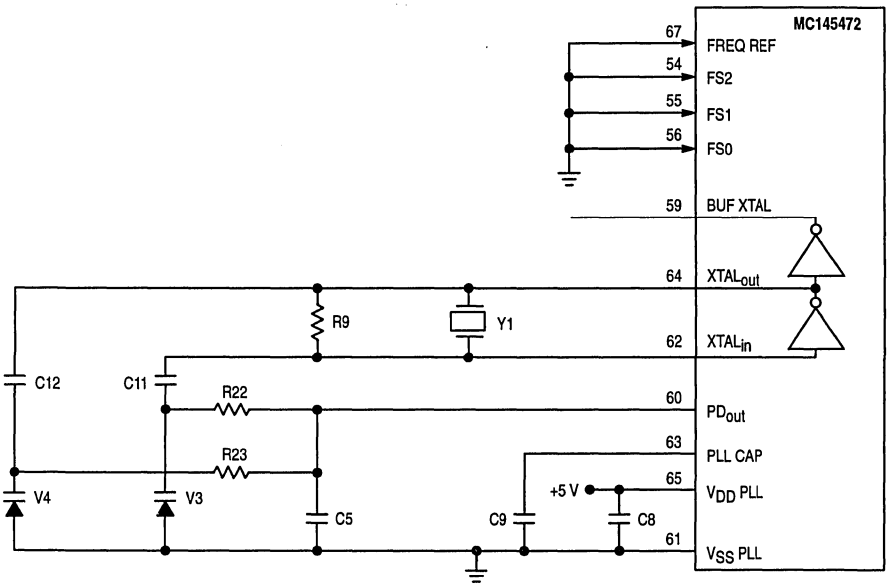
15.36 CLKOUT provides a buffered 15.36-MHz clock output that can be used for the MC145474/75 S/T transceiver clock. This clock is a 20.48 MHz clock with every fourth clock tick removed. Figure 16 shows the 15.36 MHz clock waveform. There may be applications where this clock is inadequate.

4.096 CLKOUT provides a buffered 4.096 MHz clock out-put that can be used for a microcontroller clock. The 4.096 Enable input, (Pin 30), must be high to enable this clock.

Test Pins

The following input pins are utilized by Motorola to test the functionality of the MC145472 during the manufacturing process. These pins should be connected to ground for normal operation.

TEST 5, TEST 7, TEST 11, TEST 12, TEST 14, TEST 15, TEST 16



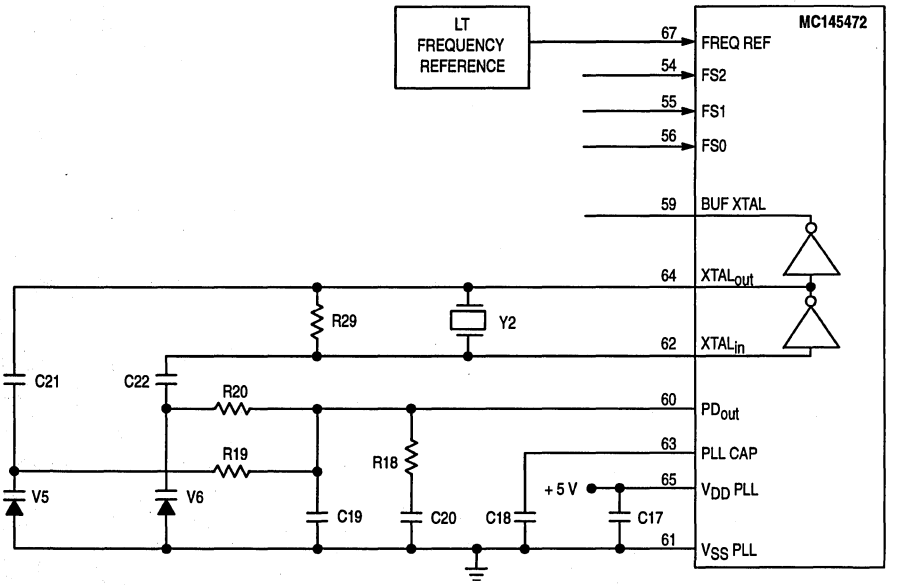
NOTE: See Table 9 for component values.

Figure 14. Typical NT Mode Voltage Controlled Crystal Oscillator Schematic

Table 9. NT Mode Crystal Oscillator Component Values

Component	Description
C5	0.1 µF ceramic, 50 V
C8	0.1 µF ceramic, 50 V
C9	0.1 µF ceramic, 50 V
C11, C12	0.01 µF to 0.1 µF ceramic, 50 V
R22, R23	270 kΩ, 5%
R9	0.5 MΩ to 1.5 MΩ, 5%
V3, V4	See complete MC145472 data book for sourcing and specification information. See Note below.
Y1	20.48 MHz ± 40 ppm, 18 pF, pullable between 240 to 300 ppm over a capacitance range of 12 to 22 pF. See complete MC145472 data book for sourcing.

NOTE: V3, V4 may be combined into a single package.



NOTE: See Table 10 for component values.

Figure 15. Typical LT Mode PLL Crystal Oscillator Schematic

Table 10. LT Mode PLL Crystal Oscillator Component Values

Component	Description
C17	0.1 µF ceramic, 50 V
C18	0.1 µF ceramic, 50 V
C19	0.1 µF ceramic, 50 V
C20	See Table 3-3 for reference frequency dependent value.
C21	0.01 µF to 0.1 µF ceramic, 50 V
C22	0.01 µF to 0.1 µF ceramic, 50 V
R18	See Table 3-3 for reference frequency dependent value.
R19	270 kΩ, 5%
R20	270 kΩ, 5%
R29	0.5 MΩ to 1.5 MΩ, 5%
R_B	1 kΩ
R_C	47 kΩ
V5	See complete MC145472 data book for sourcing and specification information.
V6	See complete MC145472 data book for sourcing and specification information.
Y2	20.48 MHz ± 40 ppm, 18 pF, pullable between 240 to 300 ppm over a capacitance range of 12 to 22 pF. See complete MC145472 data book for sourcing.

The following output pins are utilized by Motorola to test the functionality of the MC145472 during the manufacturing process. These pins should be left open circuit for normal operation.

TEST 1, TEST 2, TEST 6

SCP HIDOM

The MC145472 U-Interface Transceiver has the capability of forcing all outputs (both analog and digital) to the high impedance state. This feature, known as "the serial control port high impedance digital output mode" is provided to allow "in circuit" testing of other circuits or devices resident on the same PCB without requiring the removal of the MC145472.

TEST AND DEBUG

The MC145472 permits an external microcontroller to take control of the transmit framer by writing to control bits in Byte Register 8. This is very useful for debugging prototypes since the MC145472 can be forced to transmit a variety of signals regardless of the presence or lack of presence of a signal on the receive pins. Table 12 summarizes these signals and the control bits.

Table 11. LT PLL Frequency Select Options and Component Values

Reference Frequency (MHz)	FS2	FS1	FS0	R18 (Ω, 5%)	C20 (μF)
15.36	0	0	0	1800	150
10.24	0	0	1	910	330
8.192	0	1	0	2200	150
7.68	0	1	1	3300	100
4.096	1	0	0	2200	150
2.56	1	0	1	3300	100
2.048	1	1	0	3600	68
20.48	1	1	1	360	680

Table 12. Frame Control Modes

Frame Steering	Frame Control 2:0			Superframe Framer Mode of Operation	
b7	b6	b5	b4	NT	LT
1	0	0	0	SN0	SL0
1	0	0	1	Six frames of 10 kHz tone followed by SN1	SL1
1	0	1	0	SN2	SL2
1	0	1	1	SN3	SL3
1	1	0	0	10 kHz tone	
1	1	0	1	40 kHz tone	
1	1	1	0	Generates a single quat every basic frame which alternates over all four of the 2B1Q symbols.	
1	1	1	1	Superframe Framer free runs the scrambler with no synchronization words.	
0	Don't care			The Superframe Framer output is determined by the state of the Automatic Activation Controller.	

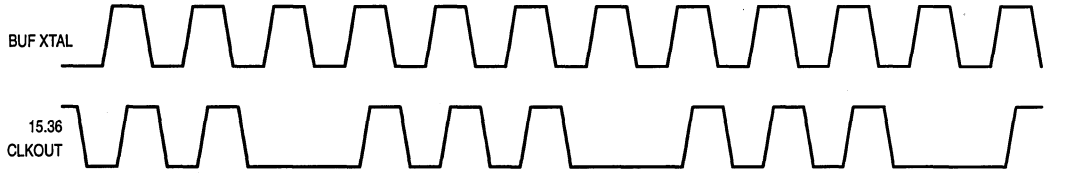


Figure 16. Waveform for 15.36 MHz Clock Output

SERIAL CONTROL PORT REGISTERS

INTRODUCTION

This section summarizes all of the MC145472 U-Interface Transceiver control and status registers available via the SCP Interface. Tables 13 through 15 summarize the registers.

The MC145472 SCP Interface is pin-for-pin identical to that of the MC145474/75 S/T-Interface Transceiver. Using the same interface as the MC145474/75 provides a common interface for applications utilizing both the MC145472 and the MC145474/75 such as an NT1 and for applications which can use either interface device such as line cards or terminal equipment.

In addition to being pin-for-pin compatible, the architecture of the nibble register map and the operation of the SCP Interface is similar to that of the MC145474/75. This is intended to simplify the code development effort and minimize device driver code size for a microcontroller.

See the MC145472 data book for a complete description of the bits in the register map.

The Register Map consists of six 4-bit Nibble Registers, one 12-bit Register. and sixteen 8-bit Byte Registers, designated as NR0-NR5, R6 (See Tables 13 and 14), and BR0-BR15 (See Table 15), respectively. Register R6 appears in the nibble register memory map but is a 12-bit register and is used to access the embedded operations channel

NIBBLE REGISTER DESCRIPTIONS

This section briefly describes the U chip nibble registers and their uses. The embedded operations channel register R6 appears in the nibble register map even though it is a 12-bit register.

NR0

This register contains read/write control bits. All bits are cleared on Hardware Reset ($\overline{\text{RESET}}$, Pin 40), but are unaffected by Software Reset (NR0(b3)). This register is write only when the U-Interface Transceiver is in Absolute Power Down mode (NR0(b1)).

NR1

This register contains device activation status. All bits are cleared on Software Reset or Hardware Reset. If any bit in this register changes from 0 to a 1, or if Linkup, Superframe Sync, or Transparent/Activation in Progress change from a one to a zero, an IRQ 3 (NR3(b3)) is generated.

NR2

Register NR2 contains activation and deactivation control bits. All bits are cleared on Software Reset or hardware reset.

NR3

This is the interrupt status register. The register is read only. All bits are cleared on Software Reset or Hardware Reset. Each interrupt status bit in the register operates the same. If it is a 1, and its corresponding interrupt enable is a 1 in Register NR4, the $\overline{\text{IRQ}}$ pin on the chip will become active. IRQ 3 has the highest priority while IRQ 0 has the lowest.

NR4

This is the interrupt mask register. All bits are cleared on Software Reset or Hardware Reset. Each bit operates the same. For example, if bit Enable IRQ 1 is set to 1 by the external microcontroller and the IRQ 1 interrupt bit is set to 1 in NR3, the $\overline{\text{IRQ}}$ pin (Pin 41) becomes active.

NR5

This register contains control bits for the IDL Interface. More IDL controls are in Registers BR6 and BR7. All bits are cleared on Software Reset or Hardware Reset.

Table 13. Nibble Registers Map

	b3	b2	b1	b0
NR0	SOFTWARE RESET	POWER DOWN ENABLE	ABSOLUTE POWER DOWN	RETURN TO NORMAL
NR1	LINKUP	ERROR INDICATION	SUPERFRAME SYNC	TRANSPARENT/ACTIVATION IN PROGRESS
NR2	ACTIVATION REQUEST	DEACTIVATION REQUEST	SUPERFRAME UPDATE DISABLE	CUSTOMER ENABLE
NR3	IRQ 3	IRQ 2	IRQ 1	IRQ 0
NR4	ENABLE IRQ 3	ENABLE IRQ 2	ENABLE IRQ 1	ENABLE IRQ 0
NR5	RESERVED	BLOCK B1	BLOCK B2	SWAP B1/B2

Table 14. Register R6 Map

	b22	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
R6	eoc a1	eoc a2	eoc a3	eoc dm	eoc i1	eoc i2	eoc i3	eoc i4	eoc i5	eoc i6	eoc i7	eoc i8

Table 15. Byte Register Map, BR0–BR15A

	b7	b6	b5	b4	b3	b2	b1	b0
BR0	M40	M41	M42	M43	M44	M45	M46	M47
BR1	M40	M41	M42	M43	M44	M45	M46	M47
BR2	M50	M60	M51	febe INPUT	RESERVED	RESERVED	RESERVED	RESERVED
BR3	M50	M60	M51	RECEIVED febe	COMPUTED nebe	VERIFIED act	VERIFIED dea	SUPERFRAME DETECT
BR4	febe COUNTER 7	febe COUNTER 6	febe COUNTER 5	febe COUNTER 4	febe COUNTER 3	febe COUNTER 2	febe COUNTER 1	febe COUNTER 0
BR5	nebe COUNTER 7	nebe COUNTER 6	nebe COUNTER 5	nebe COUNTER 4	nebe COUNTER 3	nebe COUNTER 2	nebe COUNTER 1	nebe COUNTER 0
BR6	U-LOOP B1	U-LOOP B2	U-LOOP 2B+D	U-LOOP TRANSPARENT	IDL-LOOP B1	IDL-LOOP B2	IDL-LOOP 2B+D	IDL-LOOP TRANSPARENT
BR7	BR15A SELECT	RESERVED	RESERVED	IDL INVERT	IDL FREE RUN	IDL SPEED	IDL M/S INVERT	IDL 8/10
BR8	FRAME STEERING	FRAME CONTROL 2	FRAME CONTROL 1	FRAME CONTROL 0	crc CORRUPT	MATCH SCRAMBLER	RECEIVE WINDOW DISABLE	NT/LT INVERT
	FRAME STATE 3	FRAME STATE 2	FRAME STATE 1	FRAME STATE 0	RESERVED	RESERVED	RESERVED	NT/LT MODE
BR9	eoc CONTROL 1	eoc CONTROL 0	M4 CONTROL 1	M4 CONTROL 0	M5/M6 CONTROL 1	M5/M6 CONTROL 0	febe/nebe CONTROL	RESERVED
BR10	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
BR11	ACTIVATION CONTROL 6	ACTIVATION CONTROL 5	ACTIVATION CONTROL 4	ACTIVATION CONTROL 3	ACTIVATION CONTROL 2	ACTIVATION CONTROL 1	ACTIVATION CONTROL 0	ACTIVATION TIMER DISABLE
	ACTIVATION STATE 6	ACTIVATION STATE 5	ACTIVATION STATE 4	ACTIVATION STATE 3	ACTIVATION STATE 2	ACTIVATION STATE 1	ACTIVATION STATE 0	ACTIVATION TIMER EXPIRE
BR12	ACTIVATION CONTROL STEER	INTERPOLATE ENABLE	LOAD ACTIVATION STATE	STEP ACTIVATION STATE	HOLD ACTIVATION STATE	JUMP SELECT	RESERVED	FORCE LINKUP
	EPI 18	EPI 17	EPI 16	EPI 15	EPI 14	EPI 13	EPI 12	EPI 11
BR13	ENABLE MEC UPDATES	ACCUM EC OUTPUT	ENABLE EC UPDATES	FAST EC BETA	ACCUM DFE OUTPUT	ENABLE DFE UPDATES	FAST DFE/ARC BETA	CLEAR ALL COEFF'S
	EPI 10	EPI 9	EPI 8	EPI 7	EPI 6	EPI 5	EPI 4	EPI 3
BR14	RESERVED	ro/wo TO r/w	RESERVED	FRAMER TO DEFRAMER LOOP	± 1 TONES	RESERVED	RESERVED	ENABLE CLKs
BR15	RESERVED	RESERVED	RESERVED	MASK 4	MASK 3	MASK 2	MASK 1	MASK 0
BR15A	FREQ ADAPT	JUMP DISABLE	RESERVED	RESERVED	ENABLE Tx SFS	ENABLE 15.36 MHz	ENABLE 20.48 MHz	ENABLE EYE DATA AND BAUD CLK
				RESERVED	RESERVED	RESERVED	RESERVED	RESERVED

R6

This register is 12-bits long to match the length of the eoc message. Operation of Register R6 depends on the setting of the eoc control bits in BR9(b7:b6) and BR14(b6). This register is double buffered.

In the default mode (BR14(b6) is 0), R6 performs as a read only/write only register. Data that is read from R6 by the external microcontroller is the eoc message that the Superframe Deframer stores according to the eoc Control register, BR9(b7:b6). Data that is written to R6 is stored in a latch contained in the Superframe Framer and is subsequently transmitted beginning on the next transmit eoc frame boundary. The Superframe Framer latches are set to ones on hardware or software resets.

BYTE REGISTER DESCRIPTIONS

This section briefly describes the U-chip byte registers and their uses.

BR0

This register contains the M4 channel bits that are framed and sent by the Superframe Framer. The bits that are written to this register are sent out on the next transmit superframe boundary. This register is double buffered. All bits are set to 1s following a Hardware Reset ($\overline{\text{RESET}}$, Pin 40) or Software Reset (NR0(b3)).

BR1

By reading this register, the external microcontroller obtains a buffered copy of the M4 bits that are parsed from the received superframe by the Superframe Deframer. The values in the register are valid when Superframe Sync, NR1(b1), is a one. BR1 is updated based on the mode set in Register BR9(b5:b4). This register is double buffered. The receive M4 channel byte can be read at any time during the superframe prior to the next update.

BR2

This register contains the reserved M5 and M6 bits that are sent by the Superframe Framer. The bits that are written to the register are sent out on the next transmit superframe boundary, provided Superframe Updated Disable (NR2(b1)) is set to 0. All bits are set to 1s following a Hardware Reset or Software Reset. The febe input bit is used to indicate how the returning febe bit is calculated. Bits b7, b6, and b5 are double buffered. The state of the Reserved bits BR2(b3:b0) is inconsequential.

BR3

This register contains the ANSI T1.601-1992 reserved M5 and M6 bits that are received by the Superframe Deframer, occurring in basic frames 1 and 2 of the superframe, and four other Superframe Deframer status bits. The M5 and M6 values in the register are valid when the Superframe Sync bit (NR1(b1)) is a 1. M50, M51, and M60 are updated based on the mode set in Register BR9(b3:b2). Bits b7, b6, b5 are double buffered. They can be read at any time during the superframe prior to the next update.

BR4

This register contains the current febe count. The counter is not cleared by a software or hardware reset. The register can be preset to any value by writing to it. If the febe bit is active in a superframe, the counter will increment at the end of the received superframe. The count does not wrap around from FF to 00 The counter will not increment unless Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are both 1s.

BR5

This register contains the current nebe count. A nebe occurs whenever the received crc message does not match the computed crc or when Linkup (NR1(b3)) is a 1 and Superframe Sync (NR1(b1)) is a 0. Superframe timing to increment the nebe counter during times when Superframe Sync is a 0 is maintained by the Superframe Framer. The counter is not cleared by a software or hardware reset. The register can be preset to any value by writing to it. If the Superframe Deframer detects a crc error in the received superframe, the counter will increment at the end of that superframe. The count does not wrap around from FF to 00.

BR6

This register contains the loop-back controls. Loopbacks can be directed towards the U-Interface or towards the IDL interface. For normal (no loop-back) operation all bits should be 0. BR6 is cleared by a Software Reset, Hardware Reset, or when the Return to Normal bit (NR0(b0)) is set. When a bit is set to a 1 the appropriate loop-back is enabled.

BR7

This register is used to configure the IDL interface. By setting bits in this register the IDL interface can be configured as master or slave, 8- or 10-bit data format, or the IDL clock rate can be selected when in master mode. BR7 is cleared on Hardware Reset or Software Reset. All bits in this register are read/write.

BR8

This register contains controls that are used for maintenance operations such as external loop-backs, Superframe Framer Control and State information, and NT/$\overline{\text{LT}}$ mode control. All write capable bits are cleared on a Software Reset or Hardware Reset. Bits b7–b4, and b0, are read only/write only. To read the write only bits, it is necessary to set BR14(b6) to a one.

BR9

This register contains mode control over the Deframer's updating of the received maintenance bits. The register is cleared on Software Reset or Hardware Reset.

BR10

This register is RESERVED.

BR11

This register contains activation state and control data. All the bits are cleared on Hardware Reset and Software Reset. The register is a read only/write only register. Setting BR14(b6) to a 1 permits the external microcontroller to read back the write portion of the register.

BR12

This register is read only/write only. The write only portion controls the U-Interface Transceiver's Central Processing Unit (CPU) and activation controller. The read portion contains the eight most significant bits of the Error Power Indicator (EPI) register in the CPU. By setting BR14(b6) to a 1, the external microcontroller can read back the setting of the control bits. These bits are cleared on a Hardware Reset or Software Reset.

BR13

This register contains several bits that control the internal operation of the U-Interface Transceiver. These bits are cleared on a Hardware Reset or Software Reset.

BR14

This register is used for setting various diagnostic modes. This register is cleared on a Hardware Reset or Software

Reset. When all of these bits are 0, the register map is in the default mode.

BR15

This register contains the revision number of the particular U-Interface Transceiver device in bits 0–4. BR15 is accessed by an SCP transfer when BR7(b7) is a 0 and the byte address in the SCP transfer is 15.

BR15A

This register is used to enable clock and test data outputs. All writeable bits in this register are cleared to 0 after a reset. BR15A is accessed by an SCP transfer when BR7(b7) is a 1 and the byte address in the SCP transfer is 15.

Table 16. NT Mode Activation Signals

Information Station	Description
TN	A 10 kHz tone consisting of alternating four + 3 quats followed by four – 3 quats for a time period of 6 frames.
SN0	No signal transmitted
SN1	Synchronization word present, no superframe synchronization word (ISW), and 2B + D + M = 1.
SN2	Synchronization word present, no superframe synchronization word (ISW), and 2B + D + M = 1.
SN3	Synchronization word present, superframe synchronization word (ISW) present. M channel bits active. Transmitted 2B + D data operational when M4 act bit = 1. When M4 act = 0, transmitted 2B + D data = 1.

ACTIVATION AND DEACTIVATION

INTRODUCTION

Activation or start-up is the process that U-Interface Transceivers use to initiate a robust full-duplex communications channel. This process, which may be initiated from either the LT or the NT mode U-Interface Transceiver, is a well-defined sequence of procedures during which the training of the equalizers and echo cancelers at each end of the transmission line takes place. Two types of activation, cold start or warm start, may occur. The MC145472 is capable of automatically supporting both types.

Deactivation is the process used to gracefully end communication between the U-Interface Transceivers at each end of the transmission line. Only the LT mode U-Interface Transceiver may initiate a deactivation procedure.

The internal register set of the MC145472 is detailed in Tables 13 through 15.

ACTIVATION SIGNALS FOR NT MODE

When configured as an NT, the U-Interface Transceiver can transmit any of the signals shown in Table 16. The actual procedure undertaken by the device using these five signals is described later in this section.

ACTIVATION SIGNALS FOR LT MODE

When configured as an LT, the U-Interface Transceiver can transmit any of the signals shown in Table 17. The actual procedure undertaken by the device using these five signals is described later in this section.

Table 17. LT Mode Activation Signals

Information Station	Description
TL	A 10 kHz tone consisting of alternating four + 3 quats followed by four – 3 quats for a time period of 2 frames.
SL0	No signal transmitted
SL1	Synchronization word present, no superframe synchronization word (ISW), and 2B + D + M = 1.
SL2	Synchronization word present, superframe synchronization word (ISW) present, 2B + D = 0, and M = 1.
SL3	Synchronization word present, superframe synchronization word (ISW) present. M channel bits active. Transmitted 2B + D data operational when M4 act bit = 1. When M4 act = 0, transmitted 2B + D data = 0.

ACTIVATION INITIATION

The U-Interface Transceiver can be activated in either of two ways. The external microcontroller can explicitly set the Activation Request bit, NR2(b3), to a 1 or the transceiver can detect an incoming 10 kHz wake-up tone from the far end.

An LT configured U-Interface Transceiver looks for an NT sending the TN wake-up tone. An NT configured U-Interface Transceiver looks for an LT sending the TL wake-up tone. In either case, Activation Request being set or a wake-up tone being detected, the U-Interface Transceiver proceeds with activation automatically and signals the result of the activation to the external microcontroller by setting status bits in NR1.

ACTIVATION INDICATION

The activation status is indicated in Nibble Register 1. This register indicates whether the MC145472 is not activated, is in the process of activating or fully activated. This register also is used to provide error status.

LT DEACTIVATION PROCEDURES

ANSI T1.601-1992 specifies that only the LT can deactivate the U-Interface. This is done in the MC145472 by setting Deactivation Request (NR2(b2)) to 1.

NT DEACTIVATION PROCEDURES

ANSI T1.601-1992 specifies that the NT cannot initiate deactivation. The MC145472 deactivates to a warm start condition when Deactivation Request (NR2(b2)) is set to 1 prior to the LT deactivating the U-Interface. This should be done in response to the M4 dea bit changing from a 1 to a 0 at the NT when the loop is active.

M CHANNEL BITS

The eoc, M4, M5, and M6 channel bits are available at the SCP Interface once activation has been attained. All of the maintenance channel bits appear in the register map of the MC145472. These bits can be programmed by an external microcontroller to operate as defined in the ANSI T1.601 specification. The MC145472 has several operating modes

for the M channel bits including a mode that automatically implements the embedded operations channel function in NT mode. Due to the M channel bits being register accessible they can also be redefined for proprietary applications.

SCP INTERFACE INDICATION OF TRANSMIT STATES

The four SCP bits, FS3–FS0 BR8(b7:b4), indicate the current state of the Superframe Framer. See Table 12 for frame control modes.

MAINTENANCE CHANNEL

INTRODUCTION

The MC145472 provides a very flexible interface to the 4 kbps Maintenance Channel (M channel) defined in ANSI T1.601-1992. The M channel consists of 48 bits sent by both the LT and NT configured U-Interface Transceivers during the course of a superframe. These 48 bits are divided into six channels designated M1–M6, each consisting of eight bits per superframe. The Embedded Operations Channel (eoc) consists of M1, M2, and M3. The overhead bits, such as crc, febe, act, and dea, are contained in channels M4, M5, and M6.

An external microcontroller can read from or write to the M channel via the SCP Interface. Interrupts to an external microcontroller can be enabled when an eoc, M4, M5, or M6 channel register is updated. M channel registers can be configured to update when a new value is detected between successive superframes, when a bit changes, or when two or three successive superframes of a new value are detected. The M4 channel act bit (BR1(b7)) can also be configured to automatically enable or disable customer data when in NT or LT mode of operation. The M4 channel dea bit (BR1(b6)) can also be configured to automatically issue a deactivation request in NT mode of operation. The M channel registers are updated only when Superframe Sync (NR1(b1)) is set to 1.

Figures 17 and 18 detail Maintenance Channel interrupt times with respect to the U-Interface for both NT and LT modes.

EMBEDDED OPERATIONS CHANNEL (eoc)

The eoc consumes 2 kbps of the 4 kbps Maintenance Channel (M4 channel). The eoc channel is used by the central office (LT) to initiate maintenance operations at the NT. The MC145472 can be configured to automatically perform the standard ANSI T1.601 eoc operations when in NT mode. The MC145472 can also be configured to permit an external microcontroller to service eoc commands. This permits extensions of the eoc command set to be implemented as the ANSI T1.601 standard is changed or proprietary solutions can be implemented for non-ISDN applications. Byte Register BR9 is used to configure the operating mode of the eoc. An interrupt is generated when the eoc register R6 is updated and Enable IRQ 2 (NR4(b2)) is set to 1.

M4 CHANNEL

The M4 channel is used for signaling maintenance and system status between the NT and the LT. Typical information will be power status sent from the NT to the LT or the LT letting the NT know that the LT will deactivate the loop. The MC145472 provides four different modes that the M4 channel can operate in. A system designer can select whichever mode best fits the application. The received M4 data from the Superframe Deframer is available in BR0. The transmitted M4 channel data is written to Byte Register BR1. Byte Register BR9 is used to configure the operating mode of the M4 channel. An interrupt is generated when BR0 is updated and Enable IRQ 1, NR4(b1), is set to 1.

M5 AND M6 CHANNELS

The M5 and M6 channels are similar to the M4 channel. At this time the ANSI T1.601 specification defines all bits in these two channels as reserved bits. The MC145472 provides full access to these channels so they can be used in non-ISDN applications. The received M5 and M6 data from the Superframe Deframer is available in BR2. The transmitted M5/M6 channel data is written to Byte Register BR3. Register BR9 is used to configure the operating mode of the M5/M6 channels. These channels are configured as a pair. An interrupt is generated when BR2 is updated and Enable IRQ 0 (NR4(b0)) is set to one.

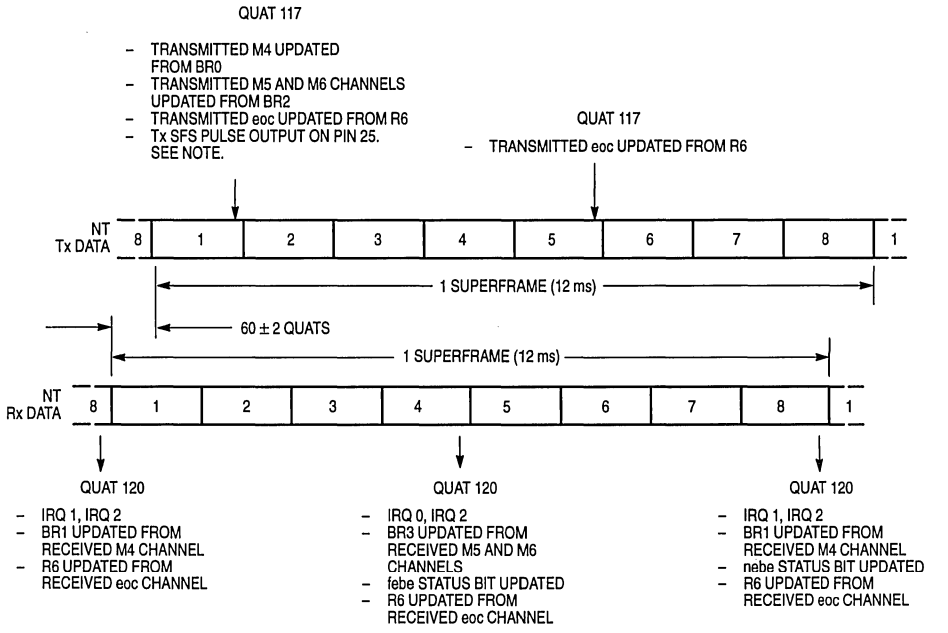
febe AND nebe BITS

The MC145472 has extensive febe (Far End Block Error) and nebe (Near End Block Error) maintenance capabilities. The state of the received computed nebe and of the received febe is available through the SCP Interface. Also, independent febe and nebe counters are available for performance monitoring purposes.

LOOP-BACK MODES

INTRODUCTION

The MC145472 U-Interface Transceiver supports four different loop-back types, each having various modes. The four types are: 1) U-Interface Loop-Back, 2) IDL Interface Loop-back , 3) Superframe Framer-to-Deframer Loop-Back, and 4) External Analog Loop-Back. Each of these loop-back modes is selected by setting bits in the appropriate SCP register(s). Any combination of loop-backs may be invoked, including simultaneous loop-backs toward the U-interface and toward the IDL Interface. These loop-backs are available with transparency or non-transparency. "Transparent" means that a loop-back passes the data on through to the other side as well as looping it back and "non-transparent" means that the data is blocked from being passed downstream and is replaced with the idle code (all 1s).



NOTE:
Due to internal superframe delays the actual sync word marker on the TxP and TxN pins occurs 8 quats prior to the Tx SFS pulse. This causes the Tx SFS pulse to appear during Quat 113 at pin 25. Internal to the MC145472 the Tx SFS pulse is generated during Quat 117.

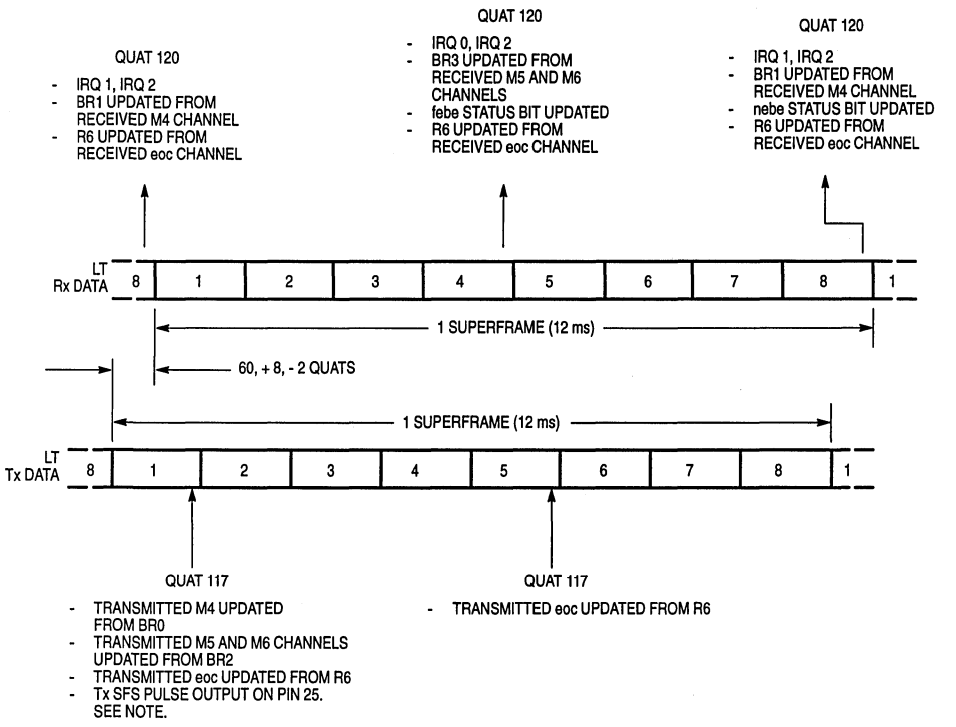
Figure 17. NT Mode Maintenance Channel Updates

U-INTERFACE LOOP-BACK

U-Interface Loop-back is shown in Figure 19. As the shaded portion of the block diagram shows, this loop-back mode exercises virtually the entire U-Interface Transceiver. 2B1Q symbols are received from the far end transmitter, recovered, passed through the IDL Interface block, and transmitted back to the far end receiver.

IDL INTERFACE LOOP-BACK

IDL Interface Loop-back is shown in Figure 20. As the shaded portion of the block diagram shows, this loop-back mode takes B and D channel data in at the IDL Rx pin and sends the same data back out the IDL Tx pin.



NOTE:
Due to internal superframe delays the actual sync word marker on the TxP and TxN pins occurs 8 quats prior to the Tx SFS pulse. This causes the Tx SFS pulse to appear during Quat 113 ± 1 at pin 25. Internal to the MC145472 the Tx SFS pulse is generated during Quat 117.

Figure 18. LT Mode Maintenance Channel Updates

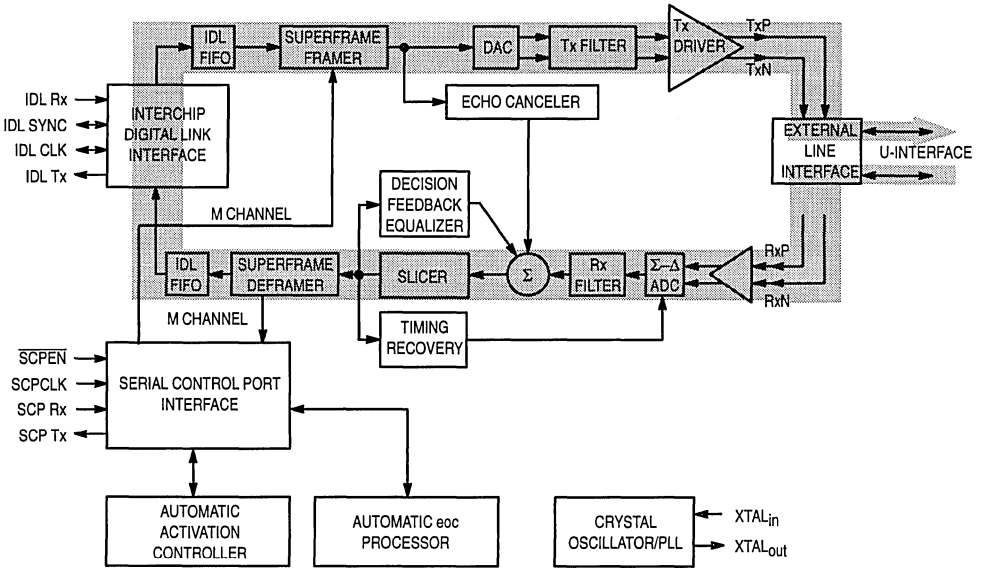


Figure 19. U-Interface Loop-Back Block Diagram

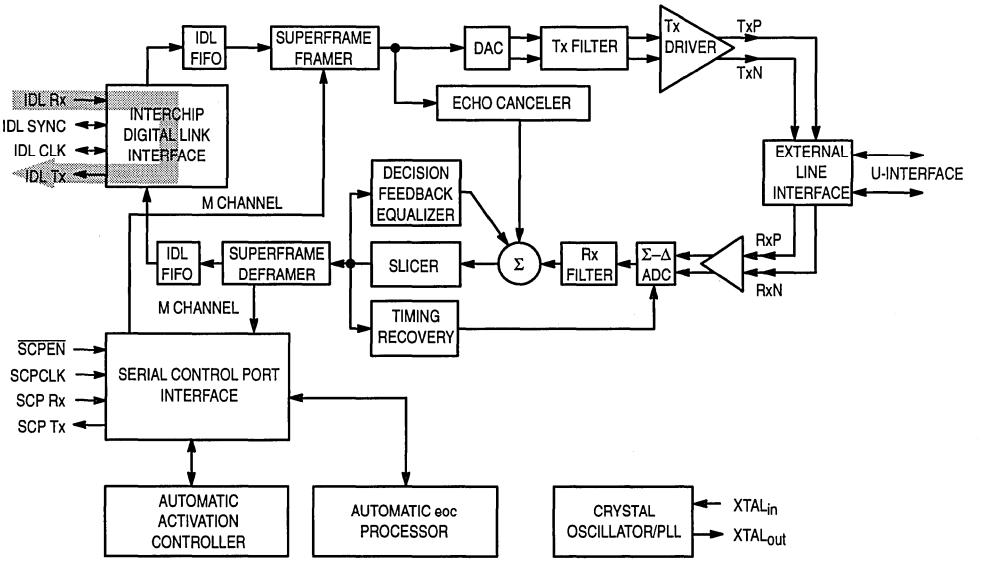


Figure 20. IDL Interface Loop-Back Block Diagram

Superframe Framer-to-Deframer Loop-Back

Superframe Framer-to-Deframer Loop-back is shown in Figure 21. As the shaded portion of the block diagram shows, this loop-back mode takes B and D channel data in at the IDL Rx pin and M channel data via the SCP, performs all of the superframe framing and subsequent deframing functions, and sends the same data back out the IDL Tx pin and SCP. This loop-back mode is intended primarily for diagnostic purposes.

External Analog Loop-Back

External Analog Loop-back is shown in Figure 22. As the shaded portion of the block diagram shows, this loop-back mode takes B and D channel data in at the IDL Rx pin and transmits the data out the Tx Driver pins. The 2B1Q signal passes through the external line interface circuitry and back into the receiver input pins. The signal is then recovered and sent out the IDL Tx pin. Note that the external line interface has been physically disconnected from the U-Interface twisted wire pair.

Since the entire 2B1Q superframe is being looped back, loop-back data includes the 2B+D channels and all of the M channels. For instance, data written by an external microcontroller to the eoc, M4, and M5/M6 registers, (R6, BR0, and BR2), is looped back and can be read from the eoc, M4, and M5/M6 registers, (R6, BR1, and BR3).

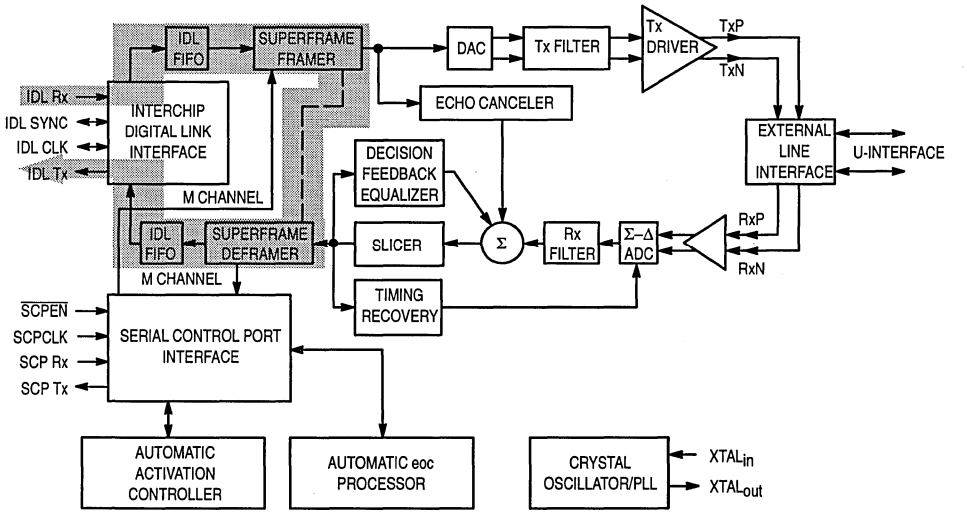


Figure 21. Superframe Framer-to-Deframer Loop-Back Block Diagram

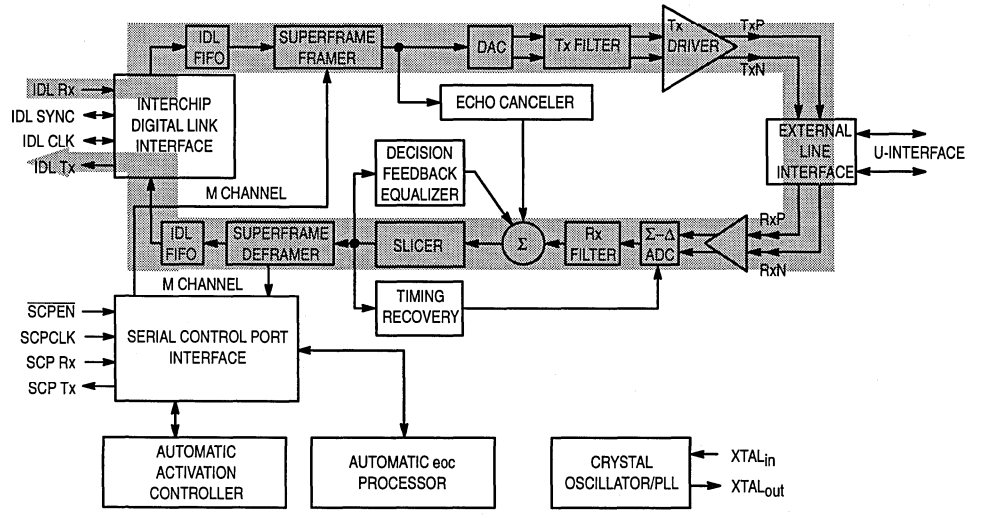


Figure 22. External Analog Loop-Back Block Diagram

MC145474
MC145475

Technical Summary

ISDN S/T Interface Transceiver

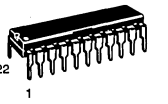
This technical summary provides a brief description of the MC145474 and MC145475 S/T Interface Transceivers. A complete data book for the MC145474/75 is available and can be ordered from your local Motorola Semiconductor Sales Office (order number MC145474/D).

The MC145474/75 ISDN S/T transceiver provides an economical VLSI Layer 1 interface for the transportation of two 64 kpbs B channels and one 16 kpbs D channel between the network termination or NT and terminal equip- ment applications or TEs. Both the MC145474 and the MC145475 conform to CCITT I.430 and ANSI TI.605 specifications.

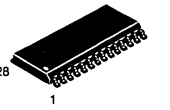
The MC145474/75 provides the modulation/line drive and demodulation/line receive functions required of the interface. In addition, the MC145474/75 provides the activation/deactivation, error monitoring, framing, bit, and octet timing. The MC145474/75 provides the control signals for the interface to the Layer 2 devices. Complete multiframe capability is provided.

The MC145474/75 features to Interchip Digital Link (IDL) for the exchange of 2B+D channel information between ISDN components and systems. The MC145474/75 provides an industry standard serial control port (SCP) to program the operation of the tranceiver.

- Conforms to CCITT I.430 and ANSI T1.605 Specifications
- Detects Far-End Code Violations (FECVs) in the NT Mode
- Incorporates the IDL
- Pin Selectable NT or TE Modes of Operation
- Industry Standard Microprocessor SCP
- Supports 1:1 Transformers for Transmit and Receive
- Exceeds the Recommended Range of Operation in all Configurations
- Complete Multiframing Capability Supported (SC1–SC5 and Q Channel)
- Optional B Channel Idle, Invert, or Exchange
- Supports Full Range of S/T and IDL Loopbacks
- Supports Transmit Power Down and Absolute Minimum Power Mode
- Supports Crystal or External Clock Input Modes
- MC145475 Bonded Out for NT1 Star Mode of Operation
- CMOS Design for Low Power Operation
- The MC14LC5494EVK may be used to evaluate the MC145474



P SUFFIX
PLASTIC
CASE 736B



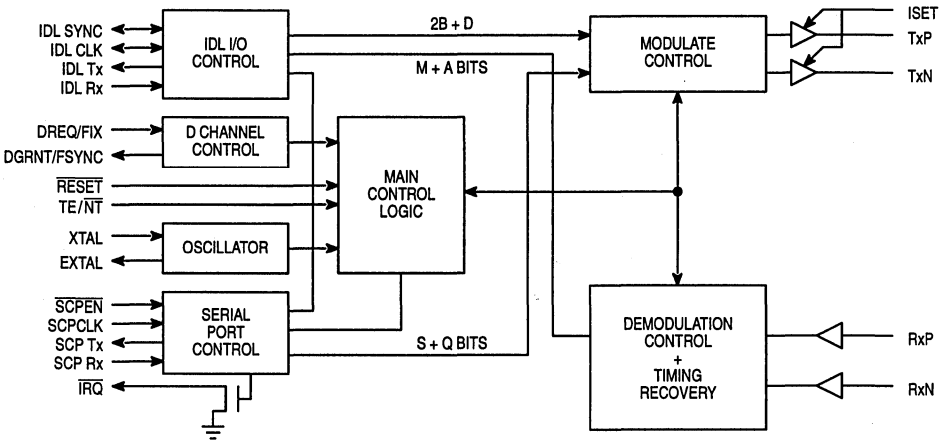
DW SUFFIX
SOG
CASE 751F

ORDERING INFORMATION

MC145474P	Plastic
MC145475DW	SOG

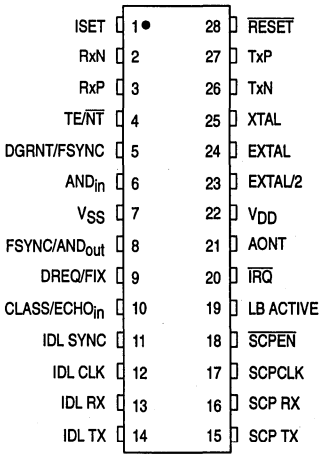
This document contains information on a new product. Specification and information herein are subject to change without notice.

BLOCK DIAGRAM

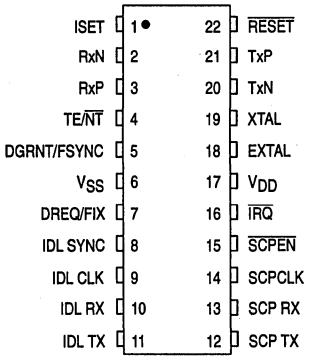


PIN ASSIGNMENT

MC145475
SOG PACKAGE



MC145474
PLASTIC PACKAGE



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage (any pin to V_{SS})	V_{in}	−0.3 to V_{DD} + 0.3	V
DC Current, any pin (excluding V_{DD}, V_{SS}, TxP, and TxN)	I	±10	mA
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−85 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \ge V_{DD}$. Reliability of operation is enhanced if unused digital inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DIGITAL DC ELECTRICAL CHARACTERISTICS (CMOS MODE, BR13(6) = 0)

(T_A = −40 to +85°C, V_{DD} = 5.0 V ±10%, Voltages referenced to V_{SS})

Characteristics	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	3.5	—	V
Input Low Voltage	V_{IL}	−0.3	1.5	V
Input Leakage Current @ 5.5 V	I_{in}	—	5	µA
High-Impedance Input Current @ 4.5/0.5 V	$I_{lkg(Z)}$	—	10	µA
Input Capacitance	C_{in}	—	10	pF
Output High Voltage (I_{OH} = −400 µA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = 5.0 mA)	V_{OL}	—	0.5	V
XTAL Input High Level	$V_{IH(X)}$	3.5	—	V
XTAL Input Low Level	$V_{IL(X)}$	—	0.5	V
EXTAL Output Current (V_{OH} = 4.6 V)	$I_{OH(X)}$	—	−400	µA
EXTAL Output Current (V_{OL} = 0.4 V)	$I_{OL(X)}$	—	400	µA
$\overline{IRQ}$ Output Low Current (V_{OL} = 0.4 V)		—	1.7	mA
$\overline{IRQ}$ Output Off-State Impedance		100	—	kΩ

DIGITAL DC ELECTRICAL CHARACTERISTICS (TTL MODE, BR13(6) = 1)

(T_A = −40 to +85°C, V_{DD} = 5.0 V ±10%, Voltages referenced to V_{SS})

Characteristics	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	—	V
Input Low Voltage	V_{IL}	−0.3	0.8	V

Note: The MC145474/75 can be programmed to accept TTL levels on all digital input pins (this does not include XTAL and EXTAL). The MC145474/75 is configured for TTL mode by writing a 1 to BR13(6). Programming the MC145474/75 for TTL mode has no effect on either the digital output pins, the crystal circuit, TxP/TxN, or RxP/RxN. Thus, the only dc electrical characteristics that differ, when operating in the CMOS mode, are the input voltages accepted on the digital inputs.

ANALOG CHARACTERISTICS (T_A = −40 to +85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Characteristics		Min	Typ	Max	Unit
TxP/TxN Drive Current	R_L = 50 Ω	13.5	15	16.5	mA
(TxP − TxN) Voltage Limit		—	—	1.17	Vpeak
Input Ampliftude (RxP − RxN)		35	—	—	mVpeak

POWER DISSIPTION (T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Characteristics	Min	Typ	Max	Unit	Notes
DC Supply Voltage (V_{DD})	4.5	5.0	5.5	V	
Worst Case Power Consumption	—	—	175	mW	1
Transmit Power Down (NR1(2) = 1)	—	—	75	mW	2
Absolute Minimum Power (NR1(1) = 1)	—	—	40	mW	2

NOTES:
1. The worst case power consumption occurs when the MC145474/75 is transmitting a 96 kHz test tone (BR11(0) = 1) into a 50 Ω load resistor. The 15.36 MHz clock is being provided by the crystal as depicted in Figure 1.
2. The power consumption figures for transmit power-down and absolute minimum power are both determined with the crystal circuit as depicted in Figure 1 still connected and operational.

IDL TIMING CHARACTERISTICS (NT MODE, IDL SLAVE) (T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Ref #	Characteristics	Min	Max	Unit
1	Time Between Successive IDL SYNCs	Note 1		
2	IDL SYNC Active after IDL CLK Falling Edge (Hold Time)	30	—	ns
3	IDL SYNC Active before IDL CLK Falling Edge (Setup Time)	30	—	ns
4	IDL CLK Period	Note 2		
5	IDL CLK Width High	70	—	ns
6	IDL CLK Width Low	70	—	ns
7	IDL Rx Valid before IDL CLK Falling Edge (Setup Time)	30	—	ns
8	IDL Rx Valid fater IDL CLK Falling Edge (Hold Time)	30	—	ns
9	IDL Tx Time to High Impedance	—	30	ns
10	IDL Tx High Impedance to Active State	—	70	ns
11	IDL CLK to IDL Tx Active	—	70	ns

NOTES:
1. IDL SYNC is an 8 kHz signal. The phase relationship between IDL SYNC and IDL CLK is as described earlier.
2. IDL CLK input frequency can be run at 1.536 MHz, 1.544 MHz, 2.046 MHYz, 2.56 MHz, or 4.098 MHz.

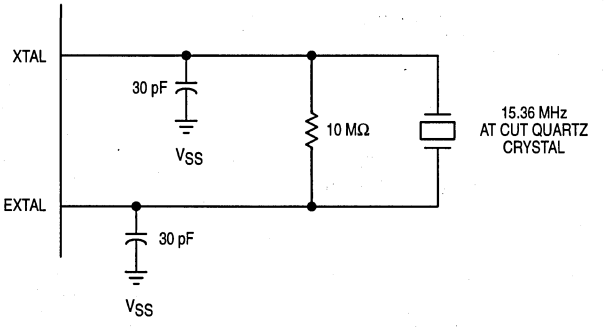


Figure 1. Crystal Circuit

IDL TIMING CHARACTERISTICS (NT MODE IDL MASTER OR TE MODE WITH THE IDL CLK RATE SET TO 2.56 MHz)
(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Ref #	Characteristics	Min	Max	Unit
1	Time Between Successive IDL SYNCs		Note 1	
2	IDL SYNC Active after IDL CLK Falling Edge (Hold Time)	160	230	ns
3	IDL SYNC Active before IDL CLK Falling Edge (Setup Time)	160	230	ns
4	IDL CLK Period		Note 2	
5	IDL CLK Width High		Note 2	
6	IDL CLK Width Low		Note 2	
7	IDL Rx Valid before IDL CLK Falling Edge (Setup Time)	30	—	ns
8	IDL Rx Valid fater IDL CLK Falling Edge (Hold Time)	30	—	ns
9	IDL Tx Time to High Impedance	0	30	ns
10	IDL Tx High Impedance to Active State	—	45	ns
11	IDL CLK to IDL Tx Active	—	45	ns

NOTES:
1. IDL SYNC is an 8 kHz signal. The phase relationship between IDL SYNC and IDL CLK is as described earlier.
2. In NT Mode IDL Master or TE Mode, the IDL CLK is generated internally in the MC145474/75. When configured for 2.56 MHz operation, IDL CLK is the crystal frequency divded by 6 and has a 50% duty cycle.

IDL TIMING CHARACTERISTICS (NT MODE IDL MASTER OR TE MODE WITH THE IDL CLK RATE SET TO 2.048 MHz)
(T_A = – 40 to + 85°C, V_{DD} = 5.0 V ± 10%, Voltages referenced to V_{SS})

Ref #	Characteristics	Min	Max	Unit
1	Time Between Successive IDL SYNCs		Note 1	
2	IDL SYNC Active after IDL CLK Falling Edge (Hold Time)	210	280	ns
3	IDL SYNC Active before IDL CLK Falling Edge (Setup Time)	210	280	ns
4	IDL CLK Period		Note 2	
5	IDL CLK Width High		Note 2	
6	IDL CLK Width Low		Note 2	
7	IDL Rx Valid before IDL CLK Falling Edge (Setup Time)	30	—	ns
8	IDL Rx Valid fater IDL CLK Falling Edge (Hold Time)	30	—	ns
9	IDL Tx Time to High Impedance	0	30	ns
10	IDL Tx High Impedance to Active State	—	45	ns
11	IDL CLK to IDL Tx Active	—	45	ns

NOTES:
1. IDL SYNC is an 8 kHz signal. The phase relationship between IDL SYNC and IDL CLK is as described earlier.
2. In NT Mode IDL Master or TE Mode, the IDL CLK is generated internally in the MC145474/75. When configured for 2.048 MHz operation, IDL CLK is the crystal frequency divded by 7.5 and has a 53.3% duty cycle.

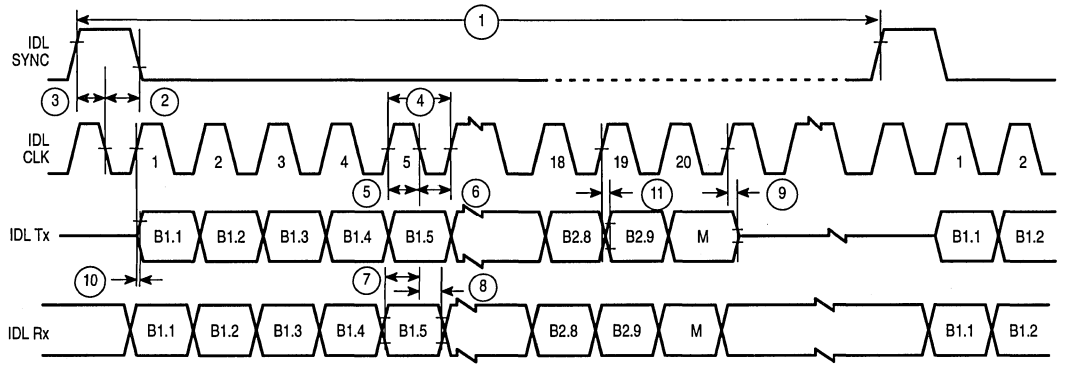
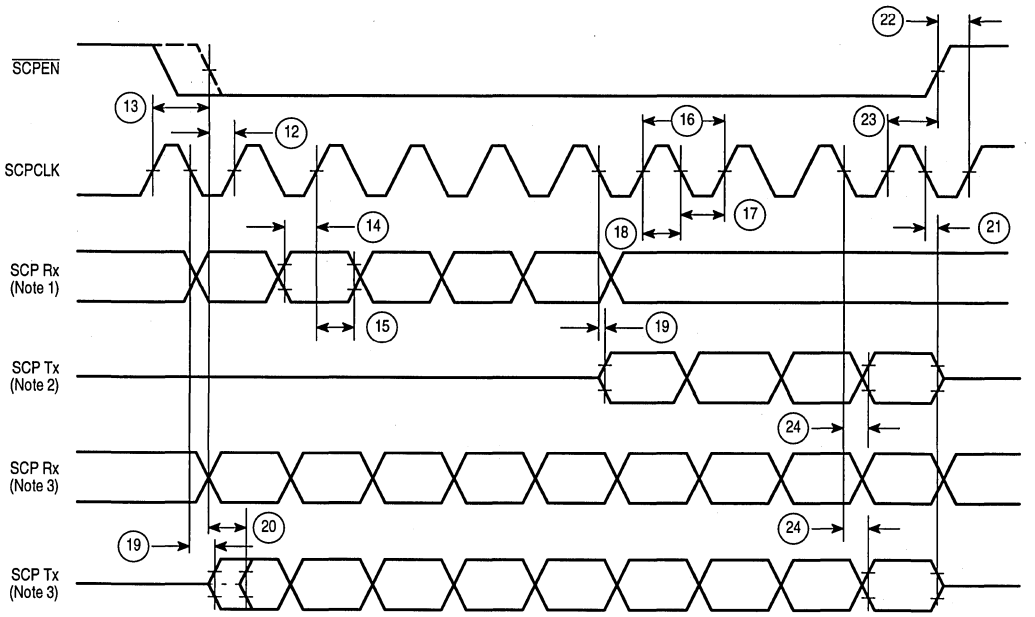


Figure 2. IDL Timing Characteristics

SCP TIMING CHARACTERISTICS

Ref #	Characteristics	Min	Max	Unit
12	$\overline{\text{SCPEN}}$ Active before Rising Edge of SCPCLK	50	—	ns
13	SCPCLK Rising Edge before $\overline{\text{SCPEN}}$ Active	50	—	ns
14	SCP Rx Valid before SCPCLK Rising Edge (Setup Time)	35	—	ns
15	SCP Rx Valid after SCPCLK Rising Edge (Hold Time)	20	—	ns
16	SCPCLK Period (See Note 1)	244	—	ns
17	SCPCLK Width (Low)	30	—	ns
18	SCPCLK Width (High)	30	—	ns
19	SCP Tx Active Delay	0	50	ns
20	$\overline{\text{SCPEN}}$ Active to SCP Tx Active	0	50	ns
21	SCPCLK Falling Edge to SCP Tx High Impedance	—	30	ns
22	$\overline{\text{SCPEN}}$ Inactive before SCPCLK Rising Edge	50	—	ns
23	SCPCLK Rising Edge before $\overline{\text{SCPEN}}$ Active	50	—	ns
24	SCPCLK Falling Edge to SCP Tx Valid Data	0	50	ns

NOTES:
1. Maximum SCPCLK frequency is 4.096 MHz.



NOTES:
1. During a nibble read, four bits are presented on SCP Rx.
2. During a nibble read, SCP Tx will be active for the duration of the 4-bit transmission as shown.
3. A byte transaction consists of two 8-bit exchanges. During the first exchange, whether a read or a write, 8 bits (the byte register address) are presented on SCP Rx. In the second exchange, 8 bits are presented on SCP Tx during a byte read. During a byte write, the second exchange consists of 8 bits presented to SCP Rx.

Figure 3. SCP Timing Characteristics

NT1 STAR MODE TIMING CHARACTERISTICS

Ref #	Characteristics	Min	Max	Unit
25	Propagation Delay from AND_{in} to AND_{out}, while receiving INFO 0	—	30	ns

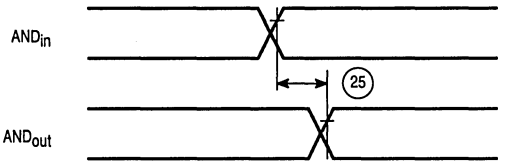


Figure 4. NT1 Star Mode

D CHANNEL TIMING CHARACTERISTICS (TE Mode)

Ref #	Characteristics	Min	Max	Unit
26	DREQ Valid before Falling Edge of IDL SYNC	30	—	ns
27	DREQ Valid after Falling Edge of IDL SYNC	30	—	ns
28	DGRNT Valid before Falling Edge of IDL SYNC	390	—	ns

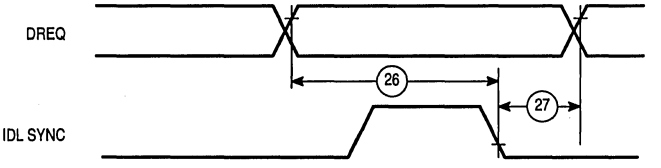


Figure 5. D-Channel Timing

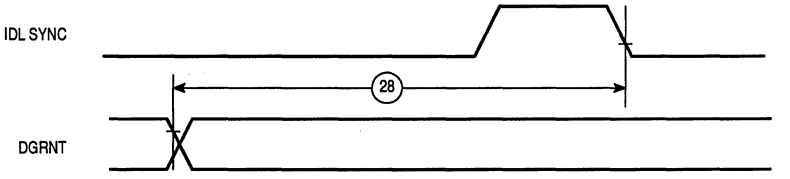


Figure 6. D-Channel Timing

PIN DESCRIPTIONS

ISET
Current Set
A current programming resistor is connected between this pin and ground.

RxP, RxN
Receive Positive, Receive Negative
The S/T interface pseudo-ternary signal is input through these pins.

TE/$\overline{NT}$
Terminal Equipment/Network Termination
This pin is an input and selects the TE or NT mode of operation.

DGRANT/FSYNC
D Channel Grant/Frame Synchronization
This pin is a dual function output and operates as DGRANT when TE mode is selected, and FSYNC when NT mode is selected.

DGRANT: The DGRANT output is asserted when the MC145474/75 has determined that it can access the D channel.

FSYNC: FSYNC is asserted when the MC145474/75 has achieved frame synchronization.

AND_{in}
NT1 Star Mode D Channel AND Gate Input
This pin is an input to the MC145475 and is used in NT1 star mode.

V_{SS}
Negative Power Supply
This pin is the most negative power supply pin and digital logic ground. It is normally 0 V.

FSYNC/AND_{out}
Frame Synchronization/
NT1 Star D Mode Channel AND Gate Output
This pin is a dual function output and operates as FSYNC when TE mode is selected and AND_{out} when NT mode is selected. This pin is available only on the MC145475.

FSYNC: FSYNC is asserted when the MC145475 has achieved frame synchronization.

AND_{out}: This pin is an output from the MC145475 and is used in NT1 star mode.

DREQ/FIX
D Channel Request/
Fixed/Adaptive Timing Select
This pin is a dual function input and operates as DREQ when TE mode is selected and FIX when NT mode is selected.

DREQ: The DREQ input should be asserted when access to the D channel is desired

FIX: This input is used to select fixed or adaptive timing mode in an NT configured MC145474/75.

CLASS/$ECHO_{in}$
D Channel Class Selection/
NT1 Star Mode Echo Channel Input
This pin is a dual function input and operates as CLASS when TE mode is selected and $ECHO_{in}$ when NT mode is selected. This pin is available only on the MC145475.

CLASS: This pin selects the desired class or priority to be used when transmitting data on the D channel.

$ECHO_{in}$: This pin is an input to the MC145475 and is used in NT1 star mode.

IDL SYNC
IDL Frame Synchronization Signal
The 8 kHz IDL frame synchronization signal is transmitted or received through this pin. When the MC145474/75 is operating as an IDL slave, this pin is an input to the device. Conversely, when the device is operating as an IDL master, this pin is an output.

IDL CLK
IDL Clock Signal
The IDL clock signal is transmitted through this pin. When the MC145474/75 is operating as an IDL slave, this pin is an input to the device. Conversely, when the device is operating as an IDL master, this pin is an output.

IDL Rx
IDL Receive Input
This pin is an input to the MC145474/75. 2B+D data is received through this pin and then modulated onto the S/T interface.

IDL Tx
IDL Transmit Output
This pin is an output from the MC145474/75. Demodulated 2B+D data from the S/T interface is transmitted through this pin.

SCP Rx
SCP Receive Input
The serial control port receive line is used to input control, status, and data information into the MC145474/75 S/T transceiver.

SCP Tx
SCP Transmit Output
The serial control port (SCP) transmit line is used to output control, status, and data information from the MC145474/75 S/T transceiver.

SCPCLK
SCP Clock Signal
The serial control port clock is used to clock control, status, and data information into and out of the MC145474/75 S/T transceiver.

$\overline{SCPEN}$
SCP Enable Signal
This signal when held low selects the SCP for the transfer of control, status, and data information into and out of the MC145474/75 S/T transceiver.

LB ACTIVE
Loopback Active
This pin is always an output from the device. If any of the loopbacks are invoked, or any combination of the loopbacks are invoked then this pin will be held high.

$\overline{IRQ}$
Interrupt Request Line
The interrupt request active low pin is an active low open drain output used to signal MPU or MCU devices that an interrupt condition exists in the MC145474/75 S/T transceiver.

AONT
Active Only NT
This pin is always an input to the device. The active only NT feature is applicable only to the NT mode of operation and is available as an output pin on the MC145475 and as an SCP control bit (BR7(6)) in both versions of the device.

V_{DD}
Positive Power Supply

This pin is the positive power supply input to the MC145474/75 and is 5.0 V ± 10% with respect to V_{SS}.

XTAL/2
7.68 MHz Clock Output

This pin is always an output from the device. The MC145474/75 S/T transceiver's 15.36 MHz clock is internally divided by two and the output of this divider (7.68 MHz) presents itself on the XTAL/2 pin.

XTAL and EXTAL
Crystal Input and Crystal Output

The MC145474/75 S/T transceiver requires a 15.36 MHz clock source for operation. This can be provided by a 15.36 MHz resonant crystal circuit using XTAL and EXTAL as the terminals of the circuit, or an external 15.36 MHz clock source can be input to the device via the XTAL pin. An inverter is internally connected between XTAL and EXTAL with XTAL as the input to the inverter and EXTAL as the output.

TxP, TxN
Transmit Positive, Transmit Negative

These pins act as differential current limited voltage source drive pairs for creating the logical line signals.

$\overline{\text{RESET}}$
MC145474/75 Reset

When low, a hardware reset is applied to the MC145474/75.

WIRING CONFIGURATIONS

INTRODUCTION

The MC145474/75 ISDN S/T transceiver conforms to CCITT I.430 and ANSI T1.605 specifications. It is a Layer 1 S/T transceiver designed for use at the S and T reference points. It is designed for both point-to-point and multipoint operation. The S/T transceiver is designed for use in either the network terminating (NT) mode or in terminal equipment (TE) applications. Two 64 kpbs B channels and one 16 kpbs D channel are transmitted in a full duplex fashion across the interface.

Suggested wiring configurations follow. These configurations are deemed to be the most common but by no means the only wiring configurations. Note that when operating in the TE mode, only one TE has the 100 Ω termination resistors in the transmit and receive paths. Figures 7 through 10 illustrate where to connect the termination resistors for the described loop configurations.

POINT-TO-POINT OPERATION

In the point-to-point mode of operation one NT communicates with one TE. As such, 100 Ω termination resistors must be connected across the transmit and receive paths of both the NT and TE transceivers. Figure 7 illustrates this wiring configuration.

When using the MC145474/75 in this configuration, the NT must be in adaptive timing. This is accomplished by holding the DREQ/FIX pin low (i.e., connecting it to VSS). CCITT I.430 and ANSI T1.605 specify that the S/T transceiver must be able to operate up to a distance of 1 km in the point-to-point mode. This is the distance D1, shown in Figure 7.

SHORT PASSIVE BUS OPERATION

The short passive bus is intended for use when up to eight TEs are required to communicate with one NT. TEs can be distributed at any point along the passive bus, the only requirement being that the termination resistors be located at the end of the passive bus. Figure 8 illustrates this wiring configuration. CCITT I.430 and ANSI T1.605 specify a maximum operational distance from the NT of 200 meters. This corresponds to the distance D2, as shown in Figure 8.

EXTENDED PASSIVE BUS OPERATION

A wiring configuration whereby the TEs are restricted to a grouping at the far end of the cable, distant from the NT, is shown as the "Extended Passive Bus." This configuration is as illustrated in Figure 9. The termination resistors are to be positioned as illustrated in the diagram.

The essence of this configuration is that a restriction is placed on the distance between the TEs. The distance D3, as illustrated in Figure 9, corresponds to the maximum distance between the grouping of TEs. CCITT I.430 and ANSI T1.605 specify a distance of 25 to 50 meters for the separation between the TEs, and a distance of 500 meters for the total length. These distances correspond to the distances D3 and D4, as shown in Figure 9.

Note that the "NT configured" MC145474/75 should be placed in the adaptive timing mode for this configuration. This is achieved by holding the DREQUEST/FIX pin low.

BRANCHED PASSIVE BUS OPERATION

A wiring configuration which has somewhat similar characteristics to those of the "Extended Passive Bus" is known as the "Branched Passive Bus" and is illustrated in Figure 10. In this configuration the branching occurs at the end of the bus. The branching occurs after a distance D1 from the NT. The distance D5 corresponds to the maximum separation between the TEs.

NT1 STAR MODE OF OPERATION

A wiring configuration which may be used to support multiple T interfaces is known as the "NT1 Star Mode of Operation." This mode of operation is supported by the MC145475. This mode is described later. Note that the NT1 Star mode contains multiple NTs. Each of these NTs can be connected to either a passive bus (short, extended, or branched) or to a single TE.

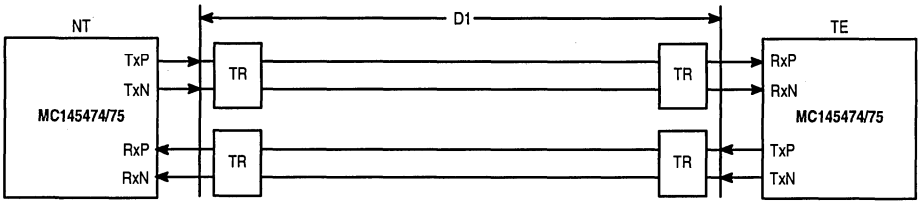


Figure 7. Point to Point

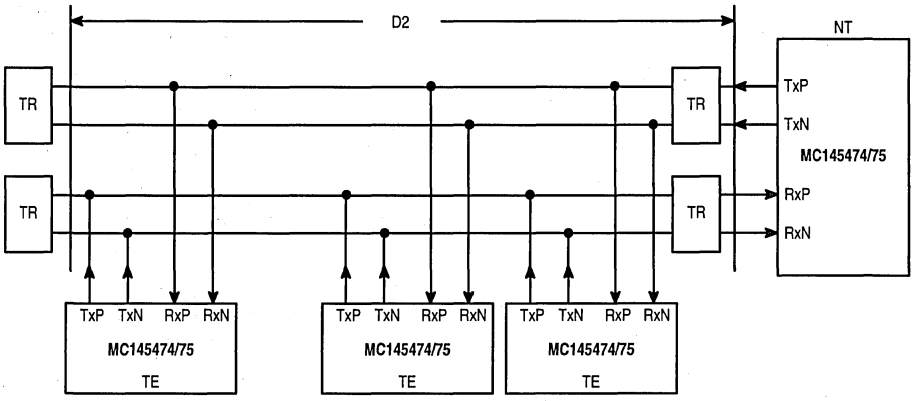


Figure 8. Short Passive Bus

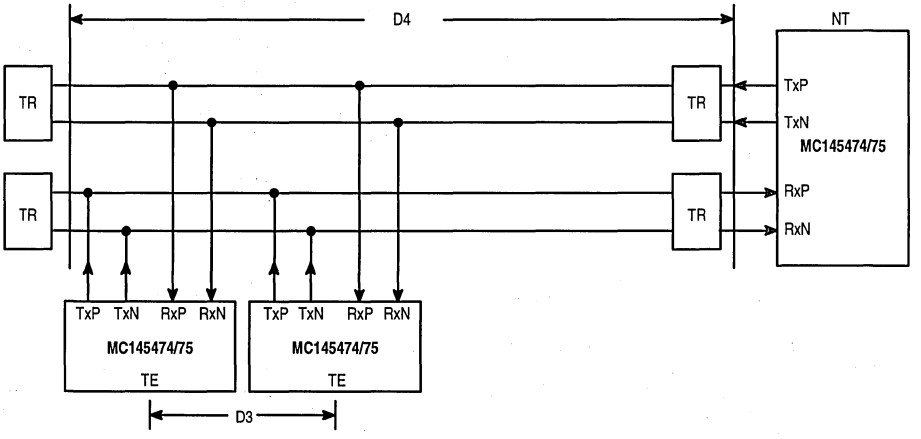


Figure 9. Extended Passive Bus

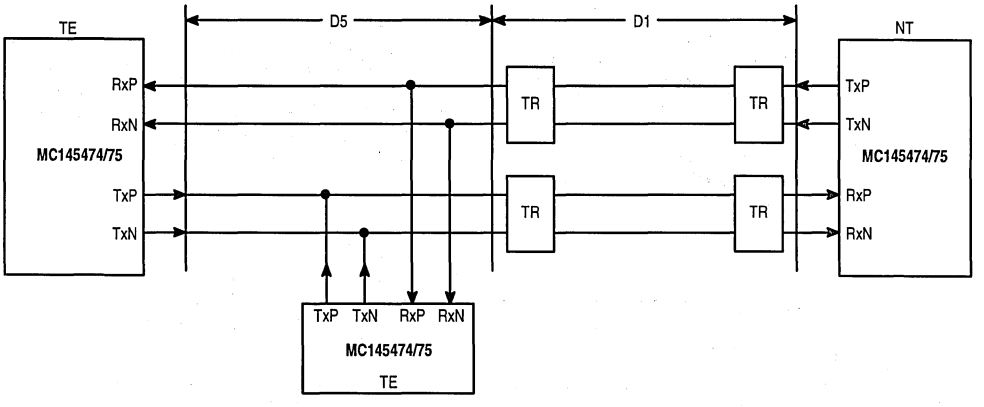


Figure 10. Branched Passive Bus

ACTIVATION/DEACTIVATION OF S/T TRANSCEIVER

INTRODUCTION

CCITT I.430 and ANSI T1.605 define five information states for the S/T transceiver. When the NT is in the fully operational state it transmits INFO 4. When the TE is in the fully operational state it transmits INFO 3. INFO 1 is transmitted by the TE when it wants to wake up the NT. INFO 2 is transmitted by the NT when it wants to wake up the TE, or in response to the TEs transmitted INFO 1. These states cause unique patterns of symbols to be transmitted over the S/T interface. Only when the S/T loop is in the fully activated state are the 2B+D channels of data transmitted over the interface.

TRANSMISSION STATES FOR NT MODE S/T TRANSCEIVER

When configured as an NT, an S/T transceiver can be in any of the following transmission states shown in Table 1.

Table 1. NT Mode Transmission States

Information State	Description
INFO 0	The NT transmits 1s in every bit position. This corresponds to no signal being transmitted.
INFO 2	The NT sets its B1, B2, D, and E channels to 0. The A bit is set to 0.
INFO 4	INFO 4 corresponds to frames containing operational data on the B1, B2, D, and E channels. The A bit is set to 1.

TRANSMISSION STATES FOR TE MODE S/T TRANSCEIVER

When configured as a TE, an S/T transceiver can be in any of the following transmission states shown in Table 2.

ACTIVATION OF S/T LOOP BY NT

The NT activates the loop by transmitting INFO 2 to the TE or TEs. This is accomplished in the MC145474/75 by setting NR2(3) to a 1. Note that this bit is internally reset to 0 after the internal activation state machine has recognized its active transition.

Table 2. TE Mode Transmission States

Information State	Description
INFO 0	The TE transmits 1s in every bit position. This corresponds to no signal being transmitted.
INFO 1	The TE transmits a continuous signal with the following pattern: positive zero, negative zero, six ones. This signal is asynchronous to the NT.
INFO 3	INFO 3 corresponds to frames containing operational data on the B1, B2, and D channels. If INFO 4 or INFO 2 is being received, INFO 3 will be synchronized to it.

The TE or TEs on receiving INFO 2 will synchronize to it and transmit back INFO 3 to the NT. The NT on receiving INFO 3 from the TE will respond with INFO 4, thus activating the loop.

ACTIVATION OF S/T LOOP BY TE

The TE can activate an inactive loop by transmitting INFO 1 to the NT. This is accomplished in the MC145474/75 by setting NR2(3) to a 1. Note that this bit is internally reset to 0 after the internal activation state machine has recognized its active transition.

The NT upon detecting INFO 1 from the TE will respond with INFO 2. The TE upon receiving a signal from the NT will cease transmission of INFO 1, reverting to an INFO 0 state. After synchronizing to the received signal and having fully verified that it is INFO 2, the TE will respond with INFO 3, thus activating the loop.

FULL ACTIVATION

When the S/T interface is fully activated, INFO 3 is transmitted by the TE and INFO 4 by the NT. Figure 11 shows the binary organization and phase relationship of these signals from the TE's perspective.

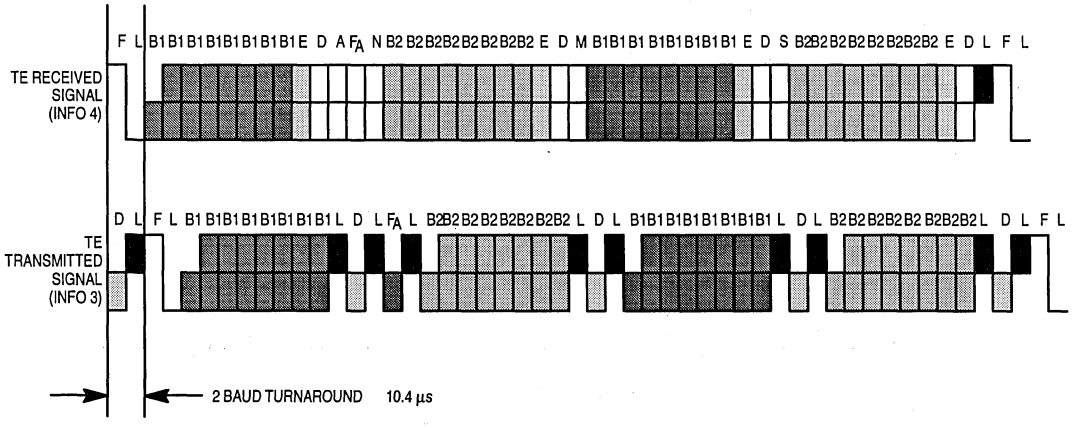


Figure 11. Two Baud Turnaround in TE

THE INTERCHIP DIGITAL LINK

The interchip digital link (IDL) is a four-wire interface used for full-duplex communication between ICs on the board-level. The interface consists of a transmit path, a receive path, an associated clock and a sync signal. These signals are known as IDL Tx, IDL Rx, IDL CLK, and IDL SYNC, respectively. The clock determines the rate of exchange of data in both the transmit and receive directions, and the sync signal controls when this exchange is to take place. Five channels of data are exchanged in a 20-bit package every 8 kHz. These channels consist of two 64 kbps B channels and one 16 kbps D channel used for full-duplex communication between the NT and TE. Figure 12 shows phase alignment and order of transmission.

In addition to these 2B+D channels there are two 8 kbps channels. These two additional channels, known as the IDL A and IDL M channels, are for local communication only (i.e., they are not transmitted from NT to TE or vice versa). Use of these channels is optional. The IDL A and IDL M channels have no effect on the operation of the S/T transceiver. There are two modes of operation for an IDL device: IDL master and IDL slave. If an IDL device is configured as an IDL master, then IDL SYNC and IDL CLK are outputs from the device. Conversely, if an IDL device is configured as an IDL slave, then IDL SYNC and IDL CLK are inputs to the device. Ordinarily the MC145474/75 is configured as an IDL slave when acting as an NT, and as an IDL master when acting as a TE. The exception to this rule is the option to configure the NT as an IDL master. Note that an NT configured MC145474/75 comes out of reset in the IDL slave mode.

THE SERIAL CONTROL PORT

INTRODUCTION

The MC145474/75 is equipped with a serial control port (SCP). This SCP is used by external devices (such as an MC145488 DDLC) to communicate with the S/T transceiver. The SCP is an industry standard serial control port and is compatible with Motorola's SPI used on several single chip MCUs.

The SCP is a four-wire bus with control and status bits as well as data being passed to and from the S/T transceiver in a full-duplex fashion. The SCP interface consists of a transmit path, a receive path, an associated clock, and an enable signal. These signals are known as SCP Tx, SCP Rx, SCPCLK, and $\overline{\text{SCPEN}}$. The clock determines the rate of exchange of data in both the transmit and receive directions, and the enable signal governs when this exchange is to take place.

The operation/configuration of the S/T transceiver is programmed by setting the state of the control bits within the S/T transceiver. The control, status, and data information reside in eight 4-bit wide nibble registers and sixteen 8-bit wide byte registers. The nibble registers are accessed via an 8-bit SCP bus transaction. The 16 byte-wide registers are accessed by first writing to a pointer register within the eight 4-bit wide nibble registers. This pointer register (NR(7)) will then contain the address of the byte wide register to be read from or written to, on the following SCP transaction. Thus, an SCP byte access is in essence a 16-bit operation. Note that this 16-bit operation can take place by means of two 8-bit accesses or a single 16-bit access.

SCP TRANSACTIONS

There are four types of SCP transactions. These are:

1. SCP nibble read
2. SCP nibble write
3. SCP byte read
4. SCP byte write

SCP Nibble Read

A nibble read is an 8-bit SCP transaction. Figure 13 illustrates this process. To initiate an SCP nibble read the $\overline{\text{SCPEN}}$ pin must be brought low. Following this, a Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit followed by three primary address bits (A0–A3), are shifted (MSB first) into an intermediate buffer register on the first four rising edges of SCPCLK, following the high-to-low transition of $\overline{\text{SCPEN}}$. If a read operation is to be performed then R/$\overline{\text{W}}$ should be a 1. The three address bits clocked in after the R/$\overline{\text{W}}$ bit select which nibble register is to be read. The contents of this nibble register are shifted out on SCP Tx on the subsequent four falling edges of SCPCLK (i.e., the four falling edges of SCPCLK after the rising edge of SCPCLK which clocked in the last address bit, LSB). $\overline{\text{SCPEN}}$ should be brought back high after the transaction, before another falling edge of SCPCLK is encountered. Note that SCP Rx is ignored during the time that SCP Tx is being driven. Also note that SCP Tx comes out of high impedance only when it is transmitting data.

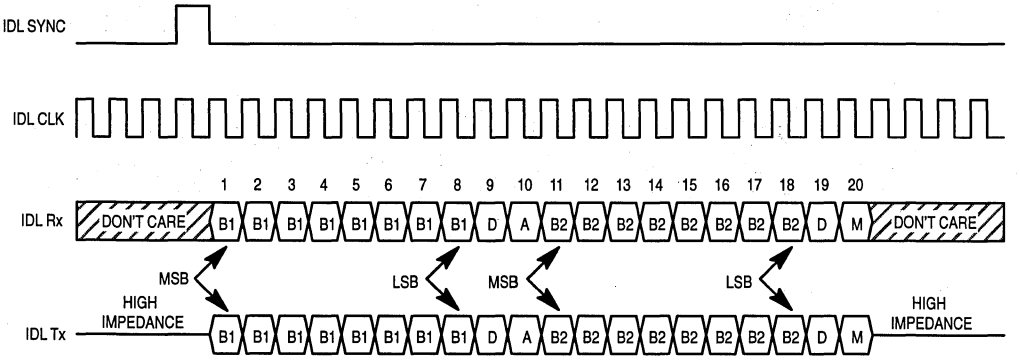
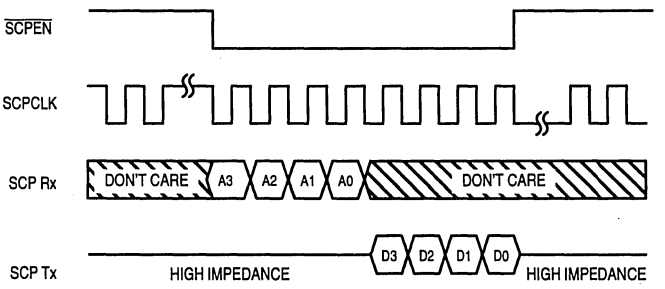
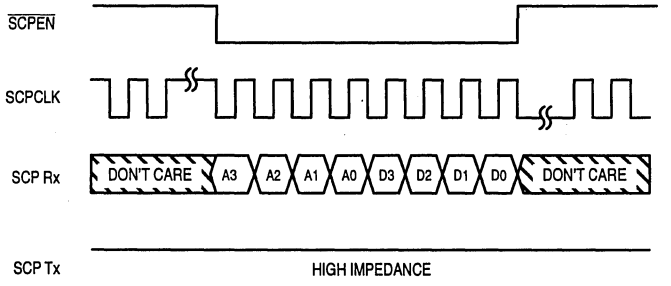


Figure 12. Interchip Digital Link



NOTES:
1. R/$\overline{W}$ = 1 for a read operation.
2. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCPCLK, MSB first.

Figure 13. Serial Control Port Nibble Read Operation



NOTES:
1. R/$\overline{W}$ = 0 for a write operation.
2. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCPCLK, MSB first.

Figure 14. Serial Control Port Nibble Write Operation

SCP Nibble Write

A nibble write is an 8-bit SCP transaction. Figure 14 illustrates this process. To initiate an SCP nibble write the $\overline{SCPEN}$ pin must be brought low. Following this an R/$\overline{W}$ bit followed by three primary address bits are shifted (MSB first) into an intermediate buffer register on the first four rising edges of SCPCLK following the high to low transition of $\overline{SCPEN}$. If a write operation is to be performed then R/$\overline{W}$ should be a 0. The three address bits clocked in after the R/$\overline{W}$ bit select the nibble register to be written to. The data shifted in on the next four rising edges of SCPCLK is then written to the selected register. Throughout this whole operation the SCP Tx pin remains in high-impedance state. Note that if a selected register or bit in a selected register is "read only" then a write operation has no effect.

SCP Byte Read

A byte read is a 16-bit SCP transaction. Figure 15 illustrates this process. To initiate an SCP byte read the $\overline{SCPEN}$ must be brought low. Following this an R/$\overline{W}$ bit is shifted in from SCP Rx on the next rising edge of SCPCLK. This bit determines the operation to be performed, read or write. If R/$\overline{W}$ is a 1 then a read operation is selected. Conversely, if R/$\overline{W}$ is a 0 then a write operation is selected. The next three bits shifted in from SCP Rx on the three subsequent rising edges of SCPCLK are primary address bits as mentioned previously. If all three bits are 1, then nibble register 7 is selected (NR7). This is a pointer register, selection of which informs the device that a byte operation is to be performed. When NR7 is selected, the following four bits shifted in from SCP Rx on the following four rising edges of SCPCLK, are automatically written to NR7. These four bits are the address bits for the byte operation. In a read operation the next eight falling edges of SCPCLK will shift out the data from the selected byte register on SCP Tx.

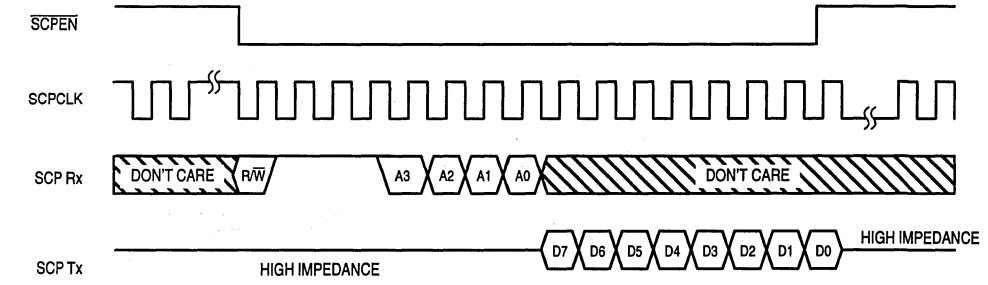
As mentioned previously, an SCP byte access is a 16-bit transaction. This can take place in one 16-bit exchange

(Figure 15) or two 8-bit exchanges (Figure 16). If the transaction is performed in two 8-bit exchanges the $\overline{SCPEN}$ should be returned high after the first eight bits have been shifted into the part. When $\overline{SCPEN}$ comes low again the MSB of the selected byte will present itself on SCP Tx. The following eight falling edges of SCPCLK will shift out the remaining eight bits of the byte register. Note that the order in which data is written into the part and read out of the part is independent of whether the byte access is done in one 16-bit exchange or in two 8-bit exchanges.

SCP Byte Write

A byte write is also a 16-bit SCP transaction. Figure 17 illustrates this process. To initiate an SCP byte write the $\overline{SCPEN}$ must be brought low. As before, the next bit determines whether the operation is to be read or write. If the first bit is a 0 then a write operation is selected. Again the next three bits read in from SCP Rx on the subsequent three rising edges of SCPCLK must all be 1 in order to select the pointer nibble register (NR7). The following four bits shifted in are automatically written into NR7. As in an SCP byte read these bits are the address bits for the selected byte register operation. The next eight rising edges of SCPCLK shift in the data from the SCP Rx. This data is then stored in the selected byte register. Throughout this operation SCP Tx will be in a high-impedance state. Note that if the selected byte is **read only**, then this operation will have no effect.

As mentioned previously an SCP byte access is a 16-bit transaction. This can take place in one 16-bit exchange (Figure 17) or two 8-bit exchanges (Figure 18). If the transaction is performed in two 8-bit exchanges, then $\overline{SCPEN}$ should be returned high after the first eight bits have been shifted into the part. When $\overline{SCPEN}$ comes low again, the next eight rising edges of SCPCLK shift data in from SCP Rx. This data is then stored in the selected byte. Figure 18 illustrates this process.



NOTES:
1. R/$\overline{W}$ = 1 for a read operation.
2. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCPCLK, MSB first.

Figure 15. Serial Control Port Byte Read Operation

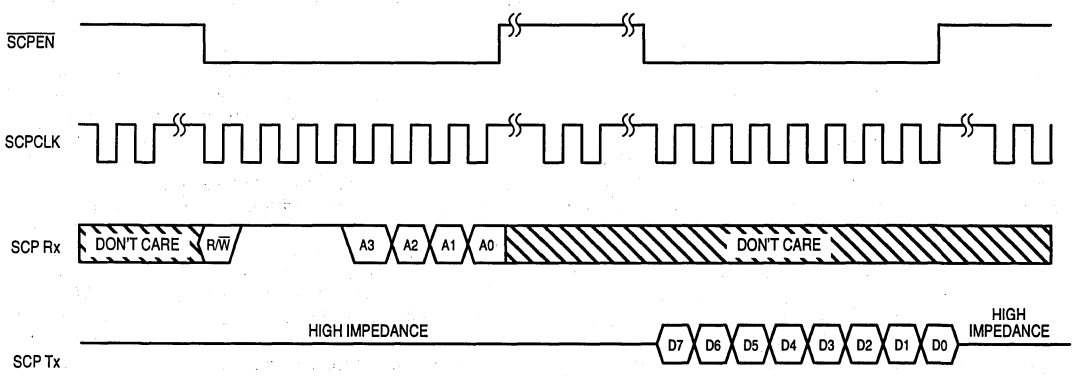
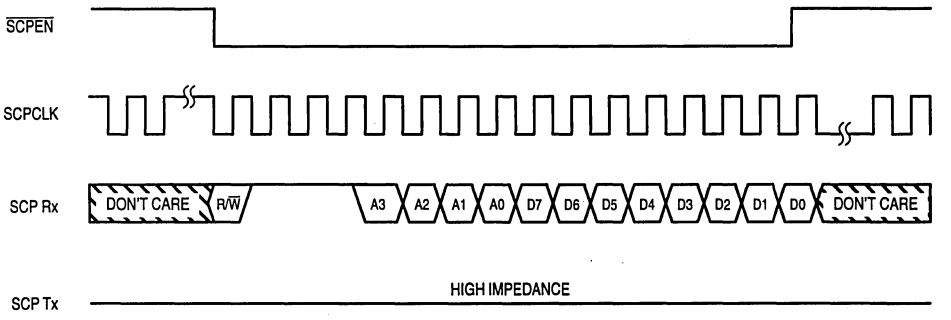


Figure 16. Serial Control Port Byte Read Operation (Double 8-Bit Transaction)



NOTES:
1. R/W = 0 for a write operation.
2. Data is shifted out on SCP Tx on the falling edges of SCPCLK, MSB first.
3. Data is shifted into the chip from SCP Rx on the rising edges of SCPCLK, MSB first.

Figure 17. Serial Control Port Byte Write Operation

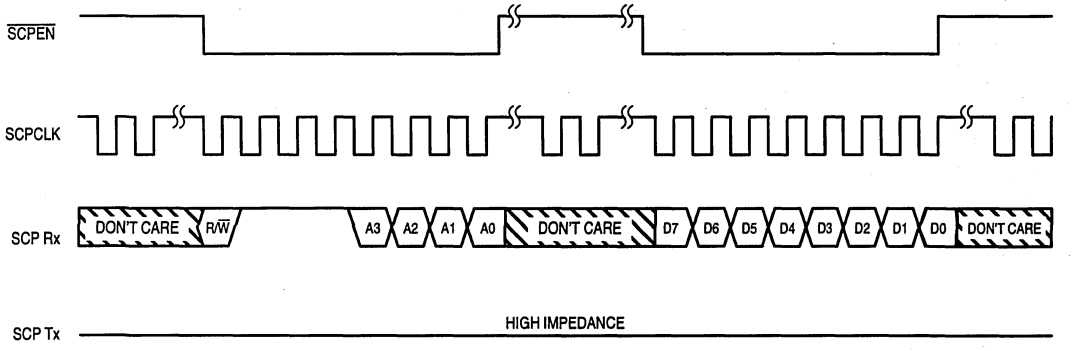


Figure 18. Serial Control Port Byte Write Operation (Double 8-Bit Transaction)

NIBBLE MAP DEFINITION

There are eight nibble registers (NR0 through NR7) in the MC145474/75. Control and status information reside in these nibble registers. These nibble registers are accessed via the SCP (see Tables 3 and 4).

BYTE MAP DESCRIPTION

There are sixteen byte registers (BR0 through BR15) in the MC145474/75. Control, status, and maintenance information reside in these byte registers. These byte registers are accessed via the SCP (see Tables 5 and 6).

Table 3. SCP Nibble Map for NT Operation

	(3)	(2)	(1)	(0)
NR0	Software Reset	Transmit Power Down	Absolute Minimum Power	Return to Normal
NR1	Activation Indication (AI)	Error Indication (EI)		Frame Sync (FS)
NR2	Activation Request (AR)	Deactivate Request (DR)	Activation Timer #1 Expire	
NR3	IRQ #3 Change in Rx INFO	IRQ #2 Multiframe Reception	IRQ #6 FECV Detection	
NR4	IRQ #3 Enable	IRQ #2 Enable	IRQ #6 Enable	
NR5	Idle B1 Channel on S/T Loop	Idle B2 Channel on S/T Loop	Invert B1 Channel	Invert B2 Channel
NR6	2B+D IDL Non-Tranparent Loopback	Activate IDL M FIFO	Activate IDL A FIFO	Exchange B1 & B2 at IDL

Table 4. SCP Nibble Map for TE Operation

	(3)	(2)	(1)	(0)
NR0	Software Reset	Transmit Power Down	Absolute Minimum Power	Return to Normal
NR1	Activation Indication (AI)	Error Indication (EI)	Multiframing Detect	Frame Sync (FS)
NR2	Activation Request (AR)		Activation Timer #3 Expire	Class
NR3	IRQ #3 Change in Rx INFO	IRQ #2 Multiframe Reception	IRQ #1 D Channel Collision	
NR4	IRQ #3 Enable	IRQ #2 Enable	IRQ #1 Enable	
NR5	Enable B1 Channel on S/T Loop	Enable B2 Channel on S/T Loop	Invert B1 Channel	Invert B2 Channel
NR6	2B+D IDL Non-Tranparent Loopback	Activate IDL M FIFO	Activate IDL A FIFO	Exchange B1 & B2 at IDL

Table 5. SCP Byte Map for NT Operation

	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
BR0	M7	M6	M5	M4	M3	M2	M1	M0
BR1	A7	A6	A5	A4	A3	A2	A1	A0
BR2	SC1.1 to Loop	SC1.2 to Loop	SC1.3 to Loop	SC1.4 to Loop				
BR3	Q1 from Loop	Q2 from Loop	Q3 from Loop	Q4 from Loop	Q Bit Quality Indicate	INT Every M. Frame		
BR4	Fr. Viol. Count B7	Fr. Viol. Count B6	Fr. Viol. Count B5	Fr. Viol. Count B4	Fr. Viol. Count B3	Fr. Viol. Count B2	Fr. Viol. Count B1	Fr. Viol. Count B0
BR5	BPV Count B7	BPV Count B6	BPV Count B5	BPV Count B4	BPV Count B3	BPV Count B2	BPV Count B1	BPV Count B0
BR6	B1 S/T LB Transparent	B1 S/T LB Non-Trans.	B2 S/T LB Transparent	B2 S/T LB Non-Trans.	IDL B1 LB Transparent	IDL B1 LB Non-Trans.	IDL B2 LB Transparent	IDL B2 LB Non-Trans.
BR7	Act. Proc. Disabled	Reserved	Enable Multiframing	Invert E Channel	IDL Master Mode	IDL CLK Speed LSB		Act. Timer #2
BR8	IDL M FIFO ≤ 1/2 Full	IDL A FIFO ≤ 1/2 Full	Act. IDL M FIFO HOZ	Act. IDL A FIFO HOZ	Enable IRQ #4	Enable IRQ #5	IRQ #4 IDL A FIFO	IRQ #5 IDL M FIFO
BR9	SC2.1 to Loop	SC2.2 to Loop	SC2.3 to Loop	SC2.4 to Loop	SC3.1 to Loop	SC3.2 to Loop	SC3.3 to Loop	SC3.4 to Loop
BR10	SC4.1 to Loop	SC4.2 to Loop	SC4.3 to Loop	SC4.4 to Loop	SC5.1 to Loop	SC5.2 to Loop	SC5.3 to Loop	SC5.4 to Loop
BR11	Do Not React to INFO 1	Do Not React to INFO 3	Rx INFO State B1	Rx INFO State B0	Tx INFO State B1	Tx INFO State B0	EXT S/T Loopback	Tx 96 kHz Test Signal
BR12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR13	NT1 Star Mode	TTL Input Levels	IDL CLK Speed MSB	Mute B2 on IDL	Mute B1 on IDL	Force E to Zero		
BR14					Reserved	Reserved	Reserved	Reserved
BR15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 6. SCP Byte Map for TE Operation

	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)
BR0	M7	M6	M5	M4	M3	M2	M1	M0
BR1	A7	A6	A5	A4	A3	A2	A1	A0
BR2	Q1 to Loop	Q2 to Loop	Q3 to Loop	Q4 to Loop				
BR3	SC1.1 from Loop	SC1.2 from Loop	SC1.3 from Loop	SC1.4 from Loop		INT Every M Frame		
BR4	Fr. Viol. Count B7	Fr. Viol. Count B6	Fr. Viol. Count B5	Fr. Viol. Count B4	Fr. Viol. Count B3	Fr. Viol. Count B2	Fr. Viol. Count B1	Fr. Viol. Count B0
BR5	BPV Count B7	BPV Count B6	BPV Count B5	BPV Count B4	BPV Count B3	BPV Count B2	BPV Count B1	BPV Count B0
BR6	B1 S/T LB Transparent	B1 S/T LB Non-Trans.	B2 S/T LB Transparent	B2 S/T LB Non-Trans.	IDL B1 LB Transparent	IDL B1 LB Non-Trans.	IDL B2 LB Transparent	IDL B2 LB Non-Trans.
BR7	Act. Proc. Ignored	D Channel Proc. Ignored		Map E to IDL on D Channel	IDL Free Run	IDL CLK Speed LSB	LAPD Pol. Cont.	
BR8	IDL M FIFO ≤ 1/2 Full	IDL A FIFO ≤ 1/2 Full	Act. IDL M FIFO HOZ	Act. IDL A FIFO HOZ	Enable IRQ #4	Enable IRQ #5	IRQ #4 IDL A FIFO	IRQ #5 IDL M FIFO
BR9	SC2.1 from Loop	SC2.2 from Loop	SC2.3 from Loop	SC2.4 from Loop	SC3.1 from Loop	SC3.2 from Loop	SC3.3 from Loop	SC3.4 from Loop
BR10	SC4.1 from Loop	SC4.2 from Loop	SC4.3 from Loop	SC4.4 from Loop	SC5.1 from Loop	SC5.2 from Loop	SC5.3 from Loop	SC5.4 from Loop
BR11			Rx INFO State B1	Rx INFO State B0	Tx INFO State B1	Tx INFO State B0	EXT S/T Loopback	Tx 96 kHz Test Signal
BR12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR13		TTL Input Levels	IDL CLK Speed MSB	Mute B2 on IDL	Mute B1 on IDL		Force IDL Transmit	
BR14					Reserved	Reserved	Reserved	Reserved
BR15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

D CHANNEL OPERATION

INTRODUCTION

The S/T interface is designed for full duplex transmission of two 64 kbps B channels and one 16 kbps D channel, between one NT device and one or more TEs. The TEs gain access to the B channels by sending Layer 2 frames to the network over the D channel. CCITT I.430 and ANSI T1.605 specify a D channel access algorithm for TEs to gain access to the D channel. The MC145474/75 S/T transceiver is fully compliant with the D channel access algorithm as defined in CCITT I.430 and ANSI T1.605. The SCP bits and pins directly pertaining to D channel operation are shown in Tables 7 and 8.

D channel data is clocked into the MC145474/75 via IDL Rx on the falling edges of IDL CLK. Data is clocked out onto IDL Tx on the rising edges of IDL CLK. This is in accordance with the IDL specification as outlined earlier.

GAINING ACCESS TO THE D CHANNEL IN TE MODE

The pins DREQ and DGRANT are used in the TE mode of operation to request and grant access to the D channel. An external device wishing to send a Layer 2 frame should bring DREQ high, and maintain it high for the duration of the Layer 2 frame. DGRANT is an output signal used to indicate to an external device that the D channel is clear. Note that the DGRANT signal actually goes high one received E echo bit prior to the programmed priority class selection. DGRANT goes high at a count of (n – 1) to accommodate the delay between the input of D channel data via the IDL interface and the line transmission of those bits towards the NT. If at the time of the IDL SYNC pulse falling edge, the DGRANT and the DREQ signals are both detected high, the TE mode

Table 7. D Channel SCP Bit Description

MC145474/75 NT Mode		MC145474/75 TE Mode	
SCP Bit	**Description**	**SCP Bit**	**Description**
BR7(4)	Invert the Echo Channel	NR2(0)	Class
BR13(2)	Force the Echo Channel to '0'	NR3(1)	Interrupt on D Channel Collision
BR13(7)	NT1 Star Mode	NR4(1)	Interrupt Enable for NR3(1)
		BR7(1)	LAPD Polarity Control
		BR7(4)	Map Echo Bits to D Timeslots on IDL Tx
		BR7(6)	D Channel Procedures Ignored

transceiver will begin FIFO buffering of the input D channel bits from the IDL interface. This FIFO is four bits deep. Note that DGRANT goes high on the boundaries of the demodulated E bits. In order for the contention algorithm to work on the D channel, HDLC data must be used. The MC145474/75 modulates the D channel data onto the S/T bus in the form that it is received from the IDL bus. Thus, the data must be presented to it in HDLC format. Note that one of the applications of the MC145488 DDLC is for use with the MC145474/75 in the terminal mode. The MC145488 will perform the HDLC conversion and perform the necessary D channel handshaking.

Table 8. D Channel Operation Pin Description

Pin #	MC145474	MC145475
5	DGRANT	DGRANT
7	DREQ	AND_{in}
8		AND_{out}
9		DREQ
10		CLASS/ECHOin

Note that the active polarity of the DREQ and DGRANT signals may be reversed by setting the LAPD polarity control bit (BR7(1)) in the SCP. When BR7(1) is a 0 the active polarity is as described above. Conversely, when BR7(1) is a 1 the MC145474/75 will drive DGRANT to a logic 0 when DGRANT is active and to a logic 1 when DGRANT is inactive. Also, when BR7(1) is 1, DREQ will be considered to be active low.

GAINING ACCESS TO THE D CHANNEL IN NT MODE

When configured as an NT the MC145474/75 has automatic access to the D channel. This is because the S/T interface is designed for communication between a single NT and one or more TEs. As such, the NT does not have to compete for access to the D channel. Thus, there are no DREQ or DGRANT functions associated with the NT mode of operation. Data present in the D bit positions of the IDL frame on IDL Rx are modulated onto the D bit timeslots on the S/T loop. Demodulated D channel data from the TE/TEs is transmitted onto IDL Tx in accordance with the IDL specification. The ECHO function of an NT configured S/T transceiver is performed internally in the MC145474/75. To assist in testing an S/T loop the MC145474/75 features the SCP test bits BR7(4) and BR13(2). Setting BR7(4) in the NT mode will invert the E echo channel (i.e., the logical inverse of the demodulated D channel data from the TE/TEs is transmitted in the E channel). Setting BR13(2) to a 1 will force the E channel to all 0s. Refer to Section 8 for a more detailed description of these test bits. Setting BR13(7) to a 1 puts the "NT configured" MC145474/75 S/T transceiver into the NT1 Star mode of operation. In this mode, the bits to be ECHOed back to the TE/TEs are obtained from the $ECHO_{in}$ pin.

MULTIFRAMING

A Layer 1 signalling channel between the NT and TE is provided in the MC145474/75 in accordance with CCITT I.430 and ANSI T1.605. In the NT to TE direction, this Layer 1 channel is the S channel. In the TE to NT direction it is the Q channel. The S channel is subdivided into five subchannels: SC1, SC2, SC3, SC4, and SC5. The MC145474/75 is capable of transmitting and receiving data in all S subchannels as well as the Q channel by simply reading or writing to the appropriate SCP registers. Interrupts are also available to indicate the reception of multiframe information. See the MC145474/75 Data Book for a complete description.

NT1 STAR MODE OPERATION

Appendix B of ANSI T1.605 describes an example of an NT that will support multiple T interfaces. This is to accommodate multipoint operation with more than eight TEs. The MC145475 can be configured for NT1 Star mode of operation. This mode is for use in wire ORing multiple NT configured S/T chips on the IDL side. Each NT has a common IDL SYNC, IDL CLK, IDL Tx, and IDL Rx, as shown in Figure 19. Each NT is then connected to its own individual S/T loop containing either a single TE or a group of TEs. As such, the contention for either of the B channels or for the D channel is now extended from a single passive bus to a grouping of passive busses.

ISDN employs the use of HDLC data on the D channel. Access to either of the B channels is requested and either granted or denied by the user sending Layer 2 frames on the D channel. In normal operation where there is only one NT, the TEs are granted access to the D channel in accordance with their priority and class. By counting the required number of E channel echo bits being 1, the TEs know when the D channel is clear. Thus in the NT1 Star mode of operation, where there are multiple passive busses competing for the same B1, B2, and D channels, the same E echo channel must be transmitted from each NT to its passive bus. This is accomplished in the MC145475 by means of the AND_{in}, AND_{out}, and $ECHO_{in}$ pins.

Figure 13 shows how to connect the multiple number of NTs in the NT1 Star mode. Successive connection of the AND_{out} (this is the output of an internal AND gate whose inputs are the demodulated D bits and the data on the AND_{in} pin) and AND_{in} pins, and the common connections of the $ECHO_{in}$ pins, succeeds in sending the same E echo channel to each group of TE/TEs. To configure a series of NTs for NT1 Star mode, BR13(7) must be set to 1 in each NT. Data transmitted on IDL Tx in NT1 Star mode, will have the following format: a logic 0 is V_{SS}, a logic 1 causes IDL Tx to go to a high-impedance state. This then permits the series wire ORing of the IDL bus. Note that one of the NTs must have its AND_{in} pin pulled high.

TRANSMISSION LINE INTERFACE CIRCUITRY

The MC145474/75 is an ISDN S/T transceiver fully compliant with CCITT I.430 and ANSI T1.605. As such it is designed to interface with a four wire transmission medium, one pair being the transmit path, the other pair the receive path. TxP and TxN, a fully differential output transmit pair from the MC145474/75, are designed to interface to the transmit pair of the transmission medium via auxiliary discrete components and a 1:1 turns ratio transformer. RxP and RxN are a high-impedance differential input pair used for coupling the receive line signal through a 1:1 turns ratio transformer (see Figures 20 and 21).

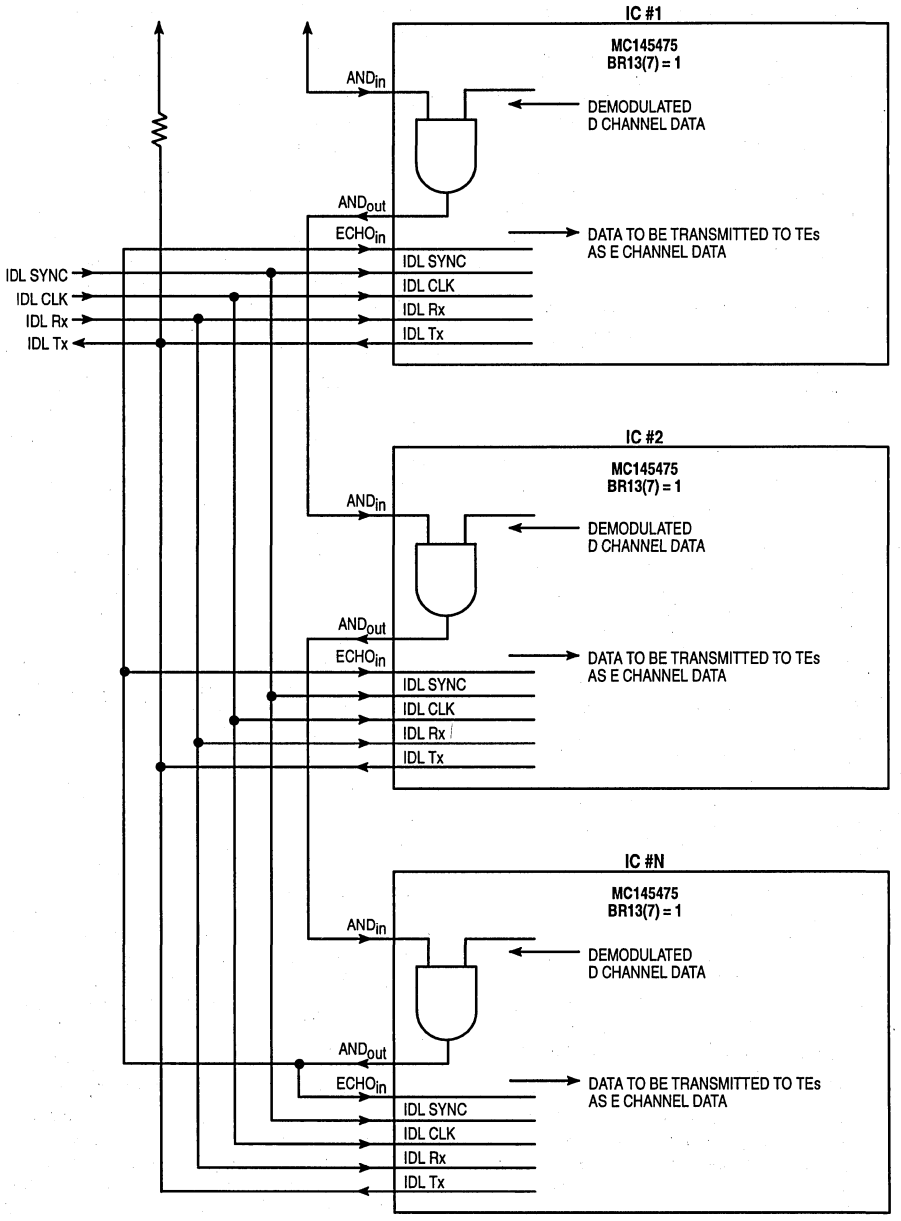


Figure 19. NT1 Star Mode of Operation

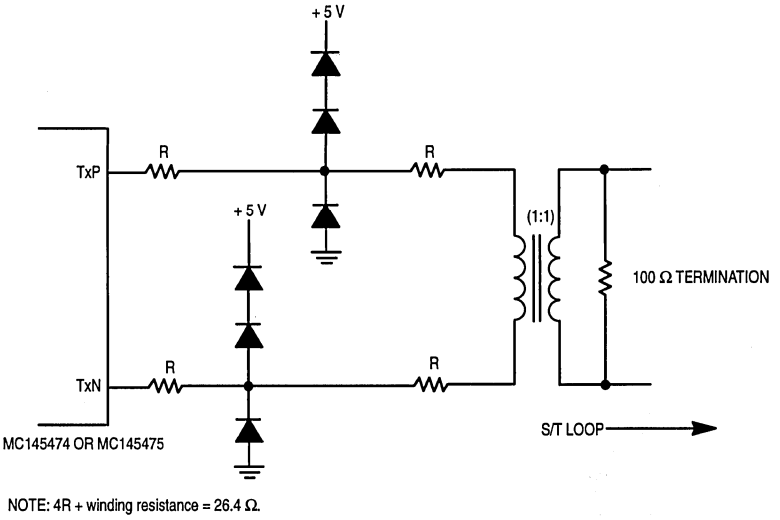


Figure 20. Transmit Line Interface Circuit

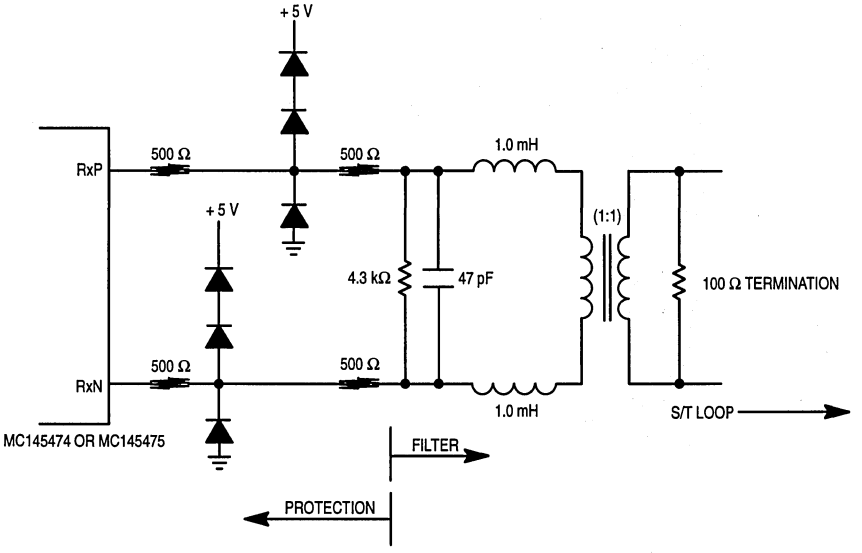
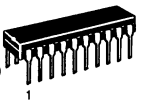


Figure 21. Receive Line Interface Circuit

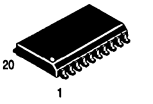
MC145480

Advance Information

5 V PCM Codec-Filter

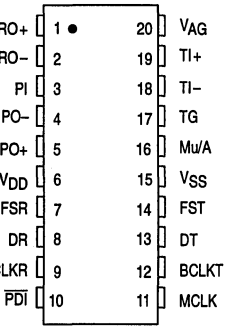


P SUFFIX
PLASTIC DIP
CASE 738



DW SUFFIX
SOG
CASE 751D

PIN ASSIGNMENT



The MC145480 is a general purpose per channel PCM Codec-Filter with pin selectable Mu-Law or A-Law companding, and is offered in 20-pin DIP and SOG packages. This device performs the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. This device is designed to operate in both synchronous and asynchronous applications and contains an on-chip precision reference voltage.

This device has an input operational amplifier whose output is the input to the encoder section. The encoder section immediately low-pass filters the analog signal with an active R-C filter to eliminate very high frequency noise from being modulated down to the passband by the switched capacitor filter. From the active R-C filter, the analog signal is converted to a differential signal. From this point, all analog signal processing is done differentially. This allows processing of an analog signal that is twice the amplitude allowed by a single-ended design, which reduces the significance of noise to both the inverted and non-inverted signal paths. Another advantage of this differential design is that noise injected via the power supplies is a common-mode signal that is cancelled when the inverted and non- inverted signals are recombined. This dramatically improves the power supply rejection ratio.

After the differential converter, a differential switched capacitor filter band-passes the analog signal from 200 Hz to 3400 Hz before the signal is digitized by the differential compressing A/D converter.

The decoder accepts PCM data and expands it using a differential D/A converter. The output of the D/A is low-pass filtered at 3400 Hz and sinX/X compensated by a differential switched capacitor filter. The signal is then filtered by an active R-C filter to eliminate the out of band energy of the switched capacitor filter.

The MC145480 PCM codec-filter accepts a variety of clock formats, including Short Frame Sync, Long Frame Sync, IDL, and GCI timing environments. This device also maintains compatibility with Motorola's family of Telecommunication products, including the MC14LC5472 U-Interface Transceiver, MC145474/75 S/T Interface Transceiver, MC145532 ADPCM Transcoder, MC145422/26 UDLT-1, MC145421/25 UDLT-2, and MC3419/MC33120 SLIC.

The MC145480 PCM codec-filter utilizes CMOS due to its reliable low-power performance and proven capability for complex analog/digital VLSI functions.

- Single 5 V Power Supply
- Typical Power Dissipation of 23 mW, Power Down of 0.01 mW
- Fully Differential Analog Circuit Design for Lowest Noise
- Transmit Band-Pass and Receive Low-Pass Filters on Chip
- Active R-C Pre-Filtering and Post-Filtering
- Mu-Law and A-Law Companding by Pin Selection
- On-Chip Precision Reference Voltage (1.575 V)
- Push-Pull 300 Ω Power Drivers with External Gain Adjust
- MC145536EVK is the evaluation kit that also includes the MC145532 ADPCM Transcoder

This document contains information on a new product. Specifications and information herein are subject to change without notice.

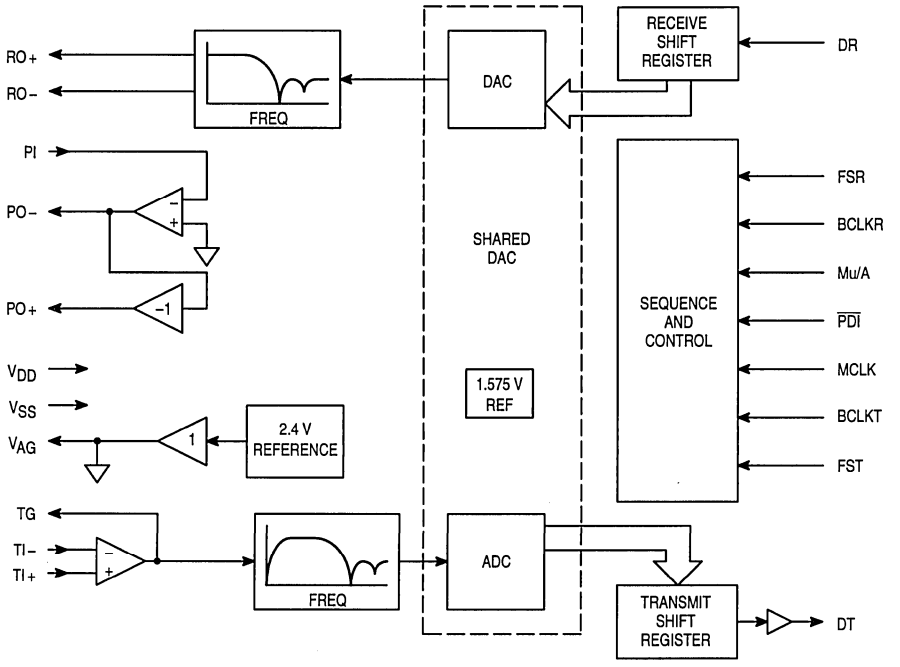


Figure 1. MC145480 PCM Codec-Filter Block Diagram

DEVICE DESCRIPTION

A PCM codec-filter is used for digitizing and reconstructing the human voice. These devices are used primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from "COder" for the analog-to-digital converter (ADC) used to digitize voice, and "DECoder" for the digital-to-analog converter (DAC) used for reconstructing voice. A codec is a single device that does both the ADC and DAC conversions.

To digitize intelligible voice requires a signal-to-distortion ratio of about 30 dB over a dynamic range of about 40 dB. This may be accomplished with a linear 13-bit ADC and DAC, but will far exceed the required signal-to-distortion ratio at larger amplitudes than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Two methods of data reduction are implemented by compressing the 13-bit linear scheme to companded pseudo-logarithmic 8-bit schemes. The two companding schemes are: Mu-255 Law, primarily in North America and Japan, and A-Law, primarily used in Europe. These companding schemes are accepted world wide. These companding schemes follow a segmented or "piecewise-linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all sixteen of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits which increment. When the chord bits increment, the step bits double their voltage weighting. This results in an effective resolution of six bits (sign + chord + four step bits) across a 42 dB dynamic range (seven chords above 0, by 6 dB per chord).

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low-pass filter to limit the high frequency energy above 3 kHz from distorting the inband signal. The telephone line is also subject to 50/60 Hz power line coupling, which must be attenuated from the signal by a highpass filter before the analog-to-digital converter.

The digital-to-analog conversion process reconstructs a staircase version of the desired inband signal, which has spectral images of the inband signal modulated about the sample frequency and its harmonics. These spectral images are called aliasing components, which need to be attenuated to obtain the desired signal. The low-pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The MC145480 PCM codec-filter has the codec, both presampling and reconstruction filters, a precision voltage refer- ence on chip, and requires no external components.

PIN DESCRIPTION

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 6)
This is the most positive power supply and is typically connected to +5 V. This pin should be decoupled to V_{SS} with a 0.1 µF ceramic capacitor.

V_{SS}
Negative Power Supply (Pin 15)
This is the most negative power supply and is typically connected to 0 V.

V_{AG}
Analog Ground Output (Pin 20)
This output pin provides a mid-supply analog ground regulated to 2.4 V. This pin should be decoupled to V_{SS} with a 0.01 µF to 0.1 µF ceramic capacitor. All analog signal processing within this device is referenced to this pin. If the audio signals to be processed are referenced to V_{SS}, then special precautions must be utilized to avoid noise between V_{SS} and the V_{AG} pin. Refer to the applications information in this document for more information. The V_{AG} pin becomes high impedance when this device is in the powered down mode.

CONTROL

Mu/A
Mu/A Law Select (Pin 16)
This pin controls the compression for the encoder and the expansion for the decoder. Mu-Law companding is selected when this pin is connected to V_{DD} and A-Law companding is selected when this pin is connected to V_{SS}.

$\overline{PDI}$
Power Down Input (Pin 10)
This pin puts the device into a low power dissipation mode when a logic 0 is applied. When this device is powered down, all of the clocks are gated off and all bias currents are turned off, which causes RO+, RO–, PO–, PO+, TG, V_{AG}, and DT to become high impedance. The device will operate normally when a logic 1 is applied to this pin. The device goes through a power-up sequence when this pin is taken to a logic 1 state, which prevents the DT PCM output from going low impedance for at least two FST cycles. The filters must settle out before the DT PCM output or the RO+ or RO– receive analog outputs will represent a valid analog signal.

ANALOG INTERFACE

TI+
Transmit Analog Input (Non-Inverting) (Pin 19)
This is the non-inverting input of the transmit input gain setting operational amplifier. This pin accommodates a differential to single ended circuit for the input gain setting op amp. This allows input signals that are referenced to the V_{SS} pin to be level shifted to the V_{AG} pin with minimum noise. This pin may be connected to the V_{AG} pin for an inverting amplifier configuration if the input signal is already referenced to the V_{AG} pin. The common mode range of the TI+ and TI– pins is from 1.2 V, to V_{DD} minus 2 V. This is an FET gate input. Connecting both TI+ and TI– pins to V_{DD} will place this amplifier's output (TG) into a high-impedance state, thus allowing the TG pin to serve as a high-impedance input to the transmit filter.

TI–
Transmit Analog Input (Inverting) (Pin 18)
This is the inverting input of the transmit gain setting operational amplifier. Gain setting resistors are usually connected from this pin to TG and from this pin to the analog signal source. The common mode range of the TI+ and TI– pins is from 1.2 V to V_{DD} –2 V. This is an FET gate input. Connecting both TI+ and TI– pins to V_{DD} will place this amplifier's output (TG) into a high-impedance state, thus allowing the TG pin to serve as a high-impedance input to the transmit filter.

TG
Transmit Gain (Pin 17)
This is the output of the transmit gain setting operational amplifier and the input to the transmit band-pass filter. This op amp is capable of driving a 2 kΩ load. Connecting both TI+ and TI– pins to V_{DD} will place this amplifier's output (TG) into a high-impedance state, thus allowing the TG pin to serve as a high-impedance input to the transmit filter. All signals at this pin are referenced to the V_{AG} pin. This pin is high impedance when the device is in the powered down mode.

RO+
Receive Analog Output (Non-Inverting) (Pin 1)
This is the non-inverting output of the receive smoothing filter from the digital-to-analog converter. This output is capable of driving a 2 kΩ load to 1.575 V peak referenced to the V_{AG} pin. This pin is high impedance when the device is in the powered down mode.

RO–
Receive Analog Output (Inverting) (Pin 2)
This is the inverting output of the receive smoothing filter from the digital-to-analog converter. This output is capable of driving a 2 kΩ load to 1.575 V peak referenced to the V_{AG} pin. This pin is high impedance when the device is in the powered down mode.

PI
Power Amplifier Input (Pin 3)
This is the inverting input to the PO– amplifier. The non-inverting input to the PO– amplifier is internally tied to the V_{AG} pin. The PI and PO– pins are used with external resistors in an inverting op amp gain circuit to set the gain of the PO+ and PO– push-pull power amplifier outputs. Connecting PI to V_{DD} will power down the power driver amplifiers and the PO+ and PO– outputs will be high impedance.

PO–
Power Amplifier Output (Inverting) (Pin 4)
This is the inverting power amplifier output, which is used to provide a feedback signal to the PI pin to set the gain of the push-pull power amplifier outputs. This pin is capable of driving a 300 Ω load to PO+. The PO+ and PO– outputs are differential (push-pull) and capable of driving a 300 Ω load to 3.15 V peak, which is 6.3 V peak-to-peak. The bias voltage and signal reference of this output is the V_{AG} pin. The V_{AG} pin cannot source or sink as much current as this pin, and therefore low impedance loads must be between PO+ and PO–. Connecting PI to V_{DD} will power down the power driver amplifiers and the PO+ and PO– outputs will be high impedance. This pin is also high impedance when the device is powered down by the $\overline{PDI}$ pin.

PO+
Power Amplifier Output (Non-Inverting) (Pin 5)

This is the non-inverting power amplifier output, which is an inverted version of the signal at PO–. This pin is capable of driving a 300 Ω load to PO–. Connecting PI to V_{DD} will power down the power driver amplifiers and the PO+ and PO– outputs will be high impedance. This pin is also high impedance when the device is powered down by the $\overline{PDI}$ pin. See PI and PO– for more information.

DIGITAL INTERFACE

MCLK
Master Clock (Pin 11)

This is the master clock input pin. The clock signal applied to this pin is used to generate the internal 256 kHz clock and sequencing signals for the switched-capacitor filters, ADC, and DAC. The internal prescaler logic compares the clock on this pin to the clock at FST (8 kHz) and will automatically accept 256, 512, 1536, 1544, 2048, 2560, or 4096 kHz. For MCLK frequencies of 256 and 512 kHz, MCLK must be synchronous and approximately rising edge aligned to FST. For optimum performance at frequencies of 1.536 MHz and higher, MCLK should be synchronous and approximately rising edge aligned to the rising edge of FST. In many applications, MCLK may be tied to the BCLKT pin.

FST
Frame Sync, Transmit (Pin 14)

This pin accepts an 8 kHz clock that synchronizes the output of the serial PCM data at the DT pin. This input is compatible with various standards including IDL, Long Frame Sync, Short Frame Sync, and GCI formats. If both FST and FSR are held low for several 8 kHz frames, the device will power down.

BCLKT
Bit Clock, Transmit (Pin 12)

This pin controls the transfer rate of transmit PCM data. In the IDL and GCI modes it also controls the transfer rate of the receive PCM data. This pin can accept any bit clock frequency from 64 to 4096 kHz for Long Frame Sync and Short Frame Sync timing. This pin can accept clock frequencies from 256 kHz to 4.096 MHz in IDL mode, and from 512 kHz to 6.176 MHz for GCI timing mode.

DT
Data, Transmit (Pin 13)

This pin is controlled by FST and BCLKT and is high impedance except when outputting PCM data. When operating in the IDL or GCI mode, data is output in either the B1 or B2 channel as selected by FSR. This pin is high impedance when the device is in the powered down mode.

FSR
Frame Sync, Receive (Pin 7)

When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts an 8 kHz clock, which synchronizes the input of the serial PCM data at the DR pin. FSR can be asynchronous to FST in the Long Frame Sync or Short Frame Sync modes. When an ISDN mode (IDL or GCI) has been selected with BCLKR, this pin selects either B1 (logic 0) or B2 (logic 1) as the active data channel.

BCLKR
Bit Clock, Receive (Pin 9)

When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts any bit clock frequency from 64 to 4096 kHz. When this pin is held at a logic 1, FST, BCLKT, DT, and DR become IDL Interface compatible. When this pin is held at a logic 0, FST, BCLKT, DT, and DR become GCI Interface compatible.

DR
Data, Receive (Pin 8)

This pin is the PCM data input, and when in a Long Frame Sync or Short Frame Sync mode is controlled by FSR and BCLKR. When in the IDL or GCI mode, this data transfer is controlled by FST and BCLKT. FSR and BCLKR select the B channel and ISDN mode, respectively.

FUNCTIONAL DESCRIPTION

ANALOG INTERFACE AND SIGNAL PATH

The transmit portion of this device includes a low-noise, three-terminal op amp capable of driving a 2 kΩ load. This op amp has inputs of TI+ (Pin 19) and TI– (Pin 18) and its output is TG (Pin 17). This op amp is intended to be configured in an inverting gain circuit. The analog signal may be applied directly to the TG pin if this transmit op amp is independently powered down by connecting the TI+ and TI– inputs to the V_{DD} power supply. The TG pin becomes high impedance when the transmit op amp is powered down. The TG pin is internally connected to a 3-pole anti-aliasing pre-filter. This pre-filter incorporates a 2-pole Butterworth active low-pass filter, followed by a single passive pole. This pre-filter is followed by a single-ended to differential converter that is clocked at 512 kHz. All subsequent analog processing utilizes fully differential circuitry. The next section is a fully-differential, 5-pole switched-capacitor low-pass filter with a 3.4 kHz frequency cutoff. After this filter is a 3-pole switched-capacitor high-pass filter having a cutoff frequency of about 200 Hz. This highpass stage has a transmission zero at dc that eliminates any dc coming from the analog input or from accumulated op amp offsets in the preceding filter stages. The last stage of the highpass filter is an autozeroed sample and hold amplifier.

One bandgap voltage reference generator and digital-to-analog converter (DAC) are shared by the transmit and receive sections. The autozeroed, switched-capacitor bandgap reference generates precise positive and negative reference voltages that are virtually independent of temperature and power supply voltage. A binary-weighted capacitor array (CDAC) forms the chords of the companding structure, while a resistor string (RDAC) implements the linear steps within each chord. The encode process uses the DAC, the voltage reference, and a frame-by-frame autozeroed comparator to implement a successive-approximation conversion algorithm. All of the analog circuitry involved in the data conversion (the voltage reference, RDAC, CDAC, and comparator) are implemented with a differential architecture.

The receive section includes the DAC described above, a sample and hold amplifier, a 5-pole, 3400 Hz switched capacitor low-pass filter with sinX/X correction, and a 2-pole active smoothing filter to reduce the spectral components of the switched capacitor filter. The output of the smoothing filter is buffered by an amplifier, which is output at the RO+ and RO– pins. These outputs are capable of driving a 4 kΩ load differentially or a 2 kΩ load to the V_{AG} pin. The MC145480 also has a pair of power amplifiers that are connected in a push-pull configuration. The PI pin is the inverting input to the PO– power amplifier. The non-inverting input is internally tied to the V_{AG} pin. This allows this amplifier to be used in an inverting gain circuit with two external resistors. The PO+ amplifier has a gain of minus one, and is internally connected

to the PO– output. This complete power amplifier circuit is a differential (push-pull) amplifier with adjustable gain that is capable of driving a 300 Ω load to +12 dBm. The power amplifier may be powered down independently of the rest of the chip by connecting the PI pin to V_{DD}.

POWER DOWN

There are two methods of putting this device into a low power consumption mode, which makes the device nonfunctional and consumes virtually no power. $\overline{PDI}$ is the power down input pin which, when taken low, powers down the device. Another way to power the device down is to hold both the FST and FSR pins low. When the chip is powered down, the V_{AG}, TG, RO+, RO–, PO+, PO–, and DT outputs are high impedance. To return the chip to the power up state, $\overline{PDI}$ must be high and either the FST or the FSR frame sync pulse must be present. The DT output will remain in a high-impedance state for at least two FST pulses after power up.

MASTER CLOCK

Since this codec-filter design has a single DAC architecture, the MCLK pin is used as the master clock for all analog signal processing including analog-to-digital conversion, digital-to-analog conversion, and for transmit and receive filtering functions of this device. The clock frequency applied to the MCLK pin may be 256 kHz, 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, 2.56 MHz, or 4.096 MHz. This device has a prescaler that automatically determines the proper divide ratio to use for the MCLK input, which achieves the required 256 kHz internal sequencing clock. The clocking requirements of the MCLK input are independent of the PCM data transfer mode (i.e., Long-Frame Sync, Short-Frame Sync, IDL mode or GCI mode).

DIGITAL I/O

The MC145480 is pin selectable for Mu-Law or A-Law. Table 1 shows the 8-bit data word format for positive and negative zero and full scale for both companding schemes (see Tables 3 and 4 at the end of this document for a complete PCM word conversion table). Table 2 shows the series of eight PCM words for both Mu-Law and A-Law that correspond to a digital milliwatt. The digital mW is the 1 kHz callbration signal reconstructed by the DAC that defines the absolute gain or 0 dBm0 Transmission Level Point (TLP) of the DAC. The 0 dBm0 level for Mu-Law is 3.17 dB below the maximum level for an unclipped tone signal. The 0 dBm0 level for A-Law is 3.14 dB below the maximum level for an unclipped tone signal. The timing for the PCM data transfer is independent of the companding scheme selected. Refer to Figure 2 for a summary and comparison of the four PCM data interface modes of this device.

Long Frame Sync

Long Frame Sync is the industry name for one type of clocking format that controls the transfer of the PCM data words. (Refer to Figure 2a) The "Frame Sync" or "Enable" is used for two specific synchronizing functions. The first is to synchronize the PCM data word transfer, and the second is to control the internal analog-to-digital and digital-to-analog conversions. The term "Sync" refers to the function of synchronizing the PCM data word onto or off of the multiplexed serial PCM data bus, which is also known as a PCM highway. The term "Long" comes from the duration of the frame sync measured in PCM data clock cycles. Long Frame Sync timing occurs when the frame sync is used directly as the PCM data output driver enable. This results in the PCM output going low impedance with the rising edge of the transmit frame sync, and remaining low impedance for the duration of the transmit frame sync.

The implementation of Long Frame Sync has maintained compatibility and been optimized for external clocking simplicity. This optimization includes the PCM data output going low impedance with the logical AND of the transmit frame sync (FST) with the transmit data bit clock (BCLKT). The optimization also includes the PCM data output (DT) remaining low impedance until the middle of the LSB (seven and a half PCM data clock cycles) or until the FST pin is taken low, whichever occurs last. This requires the frame sync to be approximately rising edge aligned with the initiation of the PCM data word transfer, but the frame sync does not have a precise timing requirement for the end of the PCM data word transfer. The device recognizes Long Frame Sync clocking when the frame sync is held high for two consecutive falling edges of the transmit data clock. The transmit logic decides on each frame sync whether it should interpret the next frame sync pulse as a Long or a Short Frame Sync. This decision is used for receive circuitry also. The device is designed to prevent PCM bus contention by not allowing the PCM data output to go low impedance for at least two frame sync cycles after power is applied or when coming out of the powered down mode.

Table 1. PCM Codes for Zero and Full Scale

	Mu-Law			A-Law		
Level	Sign Bit	Chord Bits	Step Bits	Sign Bit	Chord Bits	Step Bits
+ Full Scale	1	000	0000	1	010	1010
+ Zero	1	111	1111	1	101	0101
– Zero	0	111	1111	0	101	0101
– Full Scale	0	000	0000	0	010	1010

Table 2. PCM Codes for Digital mW

Phase	Mu-Law			A-Law		
	Sign Bit	Chord Bits	Step Bits	Sign Bit	Chord Bits	Step Bits
$\pi/8$	0	001	1110	0	011	0100
$3\pi/8$	0	000	1011	0	010	0001
$5\pi/8$	0	000	1011	0	010	0001
$7\pi/8$	0	001	1110	0	011	0100
$9\pi/8$	1	001	1110	1	011	0100
$11\pi/8$	1	000	1011	1	010	0001
$13\pi/8$	1	000	1011	1	010	0001
$15\pi/8$	1	001	1110	1	011	0100

The receive side of the device is designed to accept the same frame sync and data clock as the transmit side and to be able to latch its own transmit PCM data word. Thus the PCM digital switch needs to be able to generate only one type of frame sync for use by both transmit and receive sections of the device.

The logical AND of the receive frame sync with the receive data clock tells the device to start latching the 8-bit serial word into the receive data input on the falling edges of the receive data clock. The internal receive logic counts the receive data clock cycles and transfers the PCM data word to the digital-to-analog converter sequencer on the ninth data clock rising edge.

This device is compatible with four digital interface modes. To ensure that this device does not reprogram itself for a different timing mode, the BCLKR pin must change logic state no less than every 125 µs. The minimum PCM data bit clock frequency of 64 kHz satisfies this requirement.

Short Frame Sync

Short Frame Sync is the industry name for the type of clocking format that controls the transfer of the PCM data words (refer to Figure 2b). The "Frame Sync" or "Enable" is used for two specific synchronizing functions. The first is to synchronize the PCM data word transfer, and the second is to control the internal analog-to-digital and digital-to-analog conversions. The term "Sync" refers to the function of synchronizing the PCM data word onto or off of the multiplexed serial PCM data bus, which is also known as a PCM highway. The term "Short" comes from the duration of the frame sync measured in PCM data clock cycles. Short Frame Sync timing occurs when the frame sync is used as a "pre-synchronization" pulse that is used to tell the internal logic to clock out the PCM data word under complete control of the data clock. The Short Frame Sync is held high for one falling data clock edge. The device outputs the PCM data word beginning with the following rising edge of the data clock. This results in the PCM output going low impedance with the rising edge of the transmit data clock, and remaining low impedance until the middle of the LSB (seven and a half PCM data clock cycles).

The device recognizes Short Frame Sync clocking when the frame sync is held high for one and only one falling edge of the transmit data clock. The transmit logic decides on each frame sync whether it should interpret the next frame sync pulse as a Long or a Short Frame Sync. This decision is used for receive circuitry also. The device is designed to prevent PCM bus contention by not allowing the PCM data output to go low impedance for at least two frame sync cycles after power is applied or when coming out of the powered down mode.

The receive side of the device is designed to accept the same frame sync and data clock as the transmit side and to be able to latch its own transmit PCM data word. Thus the PCM digital switch needs to be able to generate only one type of frame sync for use by both transmit and receive sections of the device.

The falling edge of the receive data clock latching a high logic level at the receive frame sync input tells the device to start latching the 8-bit serial word into the receive data input on the following eight falling edges of the receive data clock. The internal receive logic counts the receive data clock cycles and transfers the PCM data word to the digital-to-analog converter sequencer on the rising data clock edge after the LSB has been latched into the device.

This device is compatible with four digital interface modes. To ensure that this device does not reprogram itself for a different timing mode, the BCLKR pin must change logic state no less than every 125 µs. The minimum PCM data bit clock frequency of 64 kHz satisfies this requirement.

Interchip Digital Link (IDL)

The Interchip Digital Link (IDL) Interface is one of two standard synchronous 2B+D ISDN timing interface modes with which this device is compatible. In the IDL mode, the device can communicate in either of the two 64 kbps B channels (refer to Figure 2c for sample timing). The IDL mode is selected when the BCLKR pin is held high for two or more FST (IDL SYNC) rising edges. The digital pins that control the transmit and receive PCM word transfers are reprogrammed to accommodate this mode. The pins affected are FST, FSR, BCLKT, DT and DR. The IDL Interface consists of four pins: IDL SYNC (FST), IDL CLK (BCLKT), IDL TX (DT), and IDL RX (DR). The IDL interface mode provides access to both the transmit and receive PCM data words with common control clocks of IDL Sync and IDL Clock. In this mode, the FSR pin controls whether the B1 channel or the B2 channel is used for both transmit and receive PCM data word transfers. When the FSR pin is low, the transmit and receive PCM words are transfered in the B1 channel, and for FSR high the B2 channel is selected. The start of the B2 channel is ten IDL CLK cycles after the start of the B1 channel.

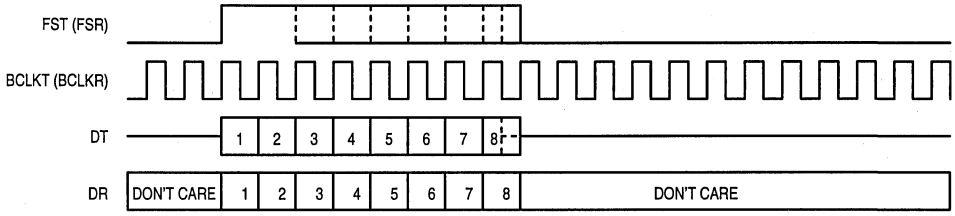


Figure 2a. Long Frame Sync (Transmit and Receive have individual clocking)

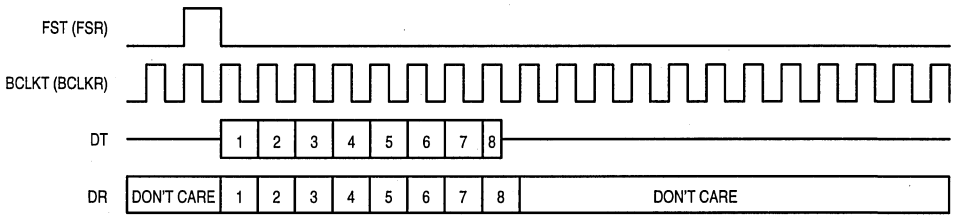


Figure 2b. Short Frame Sync (Transmit and Receive have individual clocking)

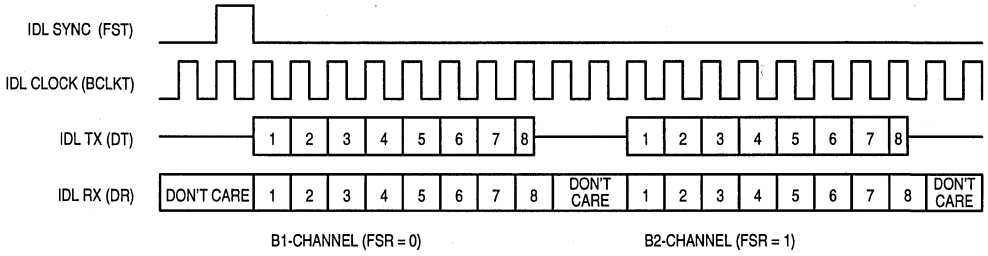


Figure 2c. IDL Interface — BCLKR = 1 (Transmit and Receive have common clocking)

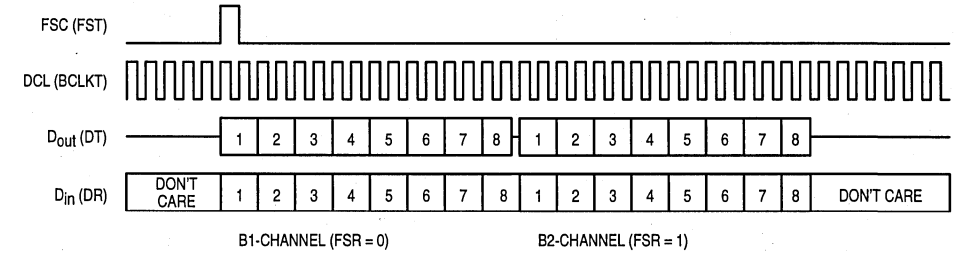


Figure 2d. GCI Interface — BCLKR = 0 (Transmit and Receive have common clocking)

Figure 2. Digital Timing Modes for the PCM Data Interface

The IDL SYNC (FST, Pin 14) is the input for the IDL frame synchronization signal. The signal at this pin is nominally high for one cycle of the IDL Clock signal and is rising edge aligned with the IDL Clock signal. (Refer to Figure 4 and the IDL Timing specifications for more details.) This event identifies the beginning of the IDL frame. The frequency of the IDL Sync signal is 8 kHz. The rising edge of the IDL SYNC (FST) should be aligned approximately with the rising edge of MCLK. MCLK must be one of the clock frequencies specified in the Digital Switching Characteristics table, and is typically tied to IDL CLK (BCLKT).

The IDL CLK (BCLKT, Pin 12) is the input for the PCM data clock. All IDL PCM transfers and data control sequencing are controlled by this clock following the IDL SYNC. This pin accepts an IDL data clock frequency of 256 kHz to 4.096 MHz.

The IDL TX (DT, Pin 13) is the output for the transmit PCM data word. Data bits are output for the B1 channel on sequential rising edges of the IDL CLK signal beginning after the IDL SYNC pulse. If the B2 channel is selected, then the PCM word transfer starts on the eleventh IDL CLK rising edge after the IDL SYNC pulse. The IDL TX pin will remain low impedance for the duration of the PCM word until the LSB after the falling edge of IDL CLK. The IDL TX pin will remain in a high impedance state when not outputting PCM data or when a valid IDL Sync signal is missing.

The IDL RX (DR, Pin 8) is the input for the receive PCM data word. Data bits are input for the B1 channel on sequential falling edges of the IDL CLK signal beginning after the IDL SYNC pulse. If the B2 channel is selected, then the PCM word is latched in starting on the eleventh IDL CLK falling edge after the IDL SYNC pulse.

General Circuit Interface (GCI)

The General Circuit Interface (GCI) is the second of two standard synchronous 2B+D ISDN timing interface modes with which this device is compatible. In the GCI mode, the device can communicate in either of the two 64 kbps B-channels. (Refer to Figure 2d for sample timing.) The GCI mode is selected when the BCLKR pin is held low for two or more FST (FSC) rising edges. The digital pins that control the transmit and receive PCM word transfers are reprogrammed to accommodate this mode. The pins affected are FST, FSR, BCLKT, DT and DR. The GCI Interface consists of four pins: FSC (FST), DCL (BCLKT), D_{out} (DT), and D_{in} (DR). The GCI interface mode provides access to both the transmit and receive PCM data words with common control clocks of FSC (frame synchronization clock) and DCL (data clock). In this mode, the FSR pin controls whether the B1 channel or the B2 channel is used for both transmit and receive PCM data word transfers. When the FSR pin is low, the transmit and receive PCM words are transfered in the B1 channel, and for FSR high the B2 channel is selected. The start of the B2 channel is 16 DCL cycles after the start of the B1 channel.

The FSC (FST, Pin 14) is the input for the GCI frame synchronization signal. The signal at this pin is nominally rising edge aligned with the DCL clock signal. (Refer to Figure 6 and the GCI Timing specifications for more details.) This event identifies the beginning of the GCI frame. The frequency of the FSC synchronization signal is 8 kHz. The rising edge of the FSC (FST) should be aligned approximately with the rising edge of MCLK. MCLK must be one of the clock frequencies specified in the Digital Switching Characteristics table, and is typically tied to DCL (BCLKT).

The DCL (BCLKT, Pin 12) is the input for the clock that controls the PCM data transfers. The clock applied at the DCL input is twice the actual PCM data rate. The GCI frame begins with the logical AND of the FSC with the DCL. This event initiates the PCM data word transfers for both transmit and receive. This pin accepts a GCI data clock frequency of 512 kHz to 6.176 MHz for PCM data rates of 256 kHz to 3.088 MHz.

The GCI D_{out} (DT, Pin 13) is the output for the transmit PCM data word. Data bits are output for the B1 channel on alternate rising edges of the DCL clock signal, beginning with the FSC pulse. If the B2 channel is selected, then the PCM word transfer starts on the seventeenth DCL rising edge after the FSC rising edge. The D_{out} pin will remain low impedance for 15-1/2 DCL clock cycles. The D_{out} pin becomes high impedance after the second falling edge of the DCL clock during the LSB of the PCM word. The D_{out} pin will remain in a high-impedance state when not outputting PCM data or when a valid FSC signal is missing.

The D_{in} (DR, Pin 8) is the input for the receive PCM data word. Data bits are latched in for the B1 channel on alternate rising edges of the DCL clock signal, beginning with the second DCL clock after the rising edge of the FSC pulse. If the B2 channel is selected then the PCM word is latched in starting on the eighteenth DCL rising edge after the FSC rising edge.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

The MC145480 is manufactured using high-speed CMOS VLSI technology to implement the complex analog signal processing functions of a PCM codec-filter. The fully differential analog circuit design techniques used for this device result in superior performance for the switched capacitor filters, the analog-to-digital converter (ADC) and the digital-to-analog converter (DAC). Special attention was given to the design of this device to reduce the sensitivities of noise, including power supply rejection and susceptibility to radio frequency noise. This special attention to design includes a fifth order low-pass filter, followed by a third order high-pass filter whose output is converted to a digital signal with greater than 75 dB of dynamic range, all operating on a single 5 V power supply. This results in a Mu-Law LSB size for small audio signals of about 386 μV. The typical idle channel noise level of this device is less than one LSB. In addition to the dynamic range of the codec/filter function of this device, the input gain-setting op amp has the capability of greater than 35 dB of gain intended for an electret microphone interface.

This device was designed for ease of implementation, but due to the large dynamic range and the noisy nature of the environment for this device (digital switches, radio telephones, DSP front-end, etc.) special care must be taken to assure optimum analog transmission performance.

PC BOARD MOUNTING

It is recommended that the device be soldered to the PC board for optimum noise performance. If the device is to be used in a socket, it should be placed in a low parasitic pin inductance (generally, low-profile) socket.

Power Supply, Ground, and Noise Considerations

This device is intended to be used in switching applications which often require plugging the PC board into a rack with power applied. This is known as "hot-rack insertion." In these applications care should be taken to limit the voltage on any pin from going positive of the V_{DD} pins, or negative of the V_{SS} pins. One method is to extend the ground and power contacts of the PCB connector. The device has input protection on all pins and may source or sink a limited amount of current without damage. Current limiting may be accomplished by series resistors between the signal pins and the connector contacts.

The most important considerations for PCB layout deal with noise. This includes noise on the power supply, noise generated by the digital circuitry on the device, and cross coupling digital or radio frequency signals into the audio signals of this device. The best way to prevent noise is to:

1. Keep digital signals as far away from audio signals as possible.
2. Keep radio frequency signals as far away from the audio signals as possible.
3. Use short, low inductance traces for the audio circuitry to reduce inductive, capacitive, and radio frequency noise sensitivities.
4. Use short, low inductance traces for digital and RF circuitry to reduce inductive, capacitive, and radio frequency radiated noise.
5. Bypass capacitors should be connected from the V_{DD} and V_{AG} pins to V_{SS} with minimal trace length. Ceramic monolithic capacitors of about 0.1 µF are acceptable to decouple the device from its own noise. The V_{DD} capacitor helps supply the instantaneous currents of the digital circuitry in addition to decoupling the noise which may be generated by other sections of the device or other circuitry on the power supply. The V_{AG} decoupling capacitor helps to reduce the impedance of the V_{AG} pin to V_{SS} at frequencies above the bandwidth of the V_{AG} generator, which reduces the susceptibility to RF noise.
6. Use a short, wide, low inductance trace to connect the V_{SS} ground pin to the power supply ground. The V_{SS} pin is the digital ground and the most negative power supply pin for the analog circuitry. All analog signal processing is referenced to the V_{AG} pin, but because digital and RF circuitry will probably be powered by this same ground, care must be taken to minimize high frequency noise in the V_{SS} trace. Depending on the application, a double sided PCB with a V_{SS} ground plane connecting all of the digital and analog V_{SS} pins together would be a good grounding method. A multilayer PC board with a ground plane connecting all of the digital and analog V_{SS} pins together would be the optimal ground configuration. These methods will result in the lowest resistance and the lowest inductance in the ground circuit. This is important to reduce voltage spikes in the ground circuit resulting from the high speed digital current spikes. The magnitude of digitally induced voltage spikes may be hundreds of times larger than the analog signal the device is required to digitize.
7. Use a short, wide, low inductance trace to connect the V_{DD} power supply pin to the 5 V power supply. Depending on the application, a double sided PCB with V_{DD} bypass capacitors to the VSS ground plane, as described above, may complete the low impedance coupling for the power supply. For a multilayer PC board with a power plane, connecting all of the V_{DD} pins to the power plane would be the optimal power distribution method. The integrated circuit layout and packaging considerations for the 5 V V_{DD} power circuit are essen- tially the same as for the V_{SS} ground circuit.
8. The V_{AG} pin is the reference for all analog signal processing. In some applications the audio signal to be digitized may be referenced to the V_{SS} ground. To reduce the susceptibility to noise at the input of the ADC section, the three terminal op amp may be used in a differential to single ended circuit to provide level conversion from the V_{SS} ground to the V_{AG} ground with noise cancellation. The op amp may be used for more than 35 dB of gain in microphone interface circuits, which will require a compact layout with minimum trace lengths as well as isolation from noise sources. It is recommended that the layout be as symmetrical as possible to avoid any imbalances which would reduce the noise cancelling benefits of this differential op amp circuit. Refer to the application schematics for examples of this circuitry.

   If possible, reference audio signals to the V_{AG} pin instead of to the V_{SS} pin. Handset receivers and telephone line interface circuits using transformers may be audio signal referenced completely to the V_{AG} pin. Refer to the application schematics for examples of this circuitry. The V_{AG} pin cannot be used for ESD or line protection.
9. For applications using multiple MC145480 PCM codec-filters, the V_{AG} pins cannot be tied together. The V_{AG} pins are capable of sourcing and sinking current and will each be driving the node, which will result in large contention currents, crosstalk susceptibilities, and increased noise.
10. The MC145480 is fabricated with advanced high speed CMOS technology that is capable of responding to noise pulses on the clock pins of 1 ns or less. It should be noted that noise pulses of such short duration may not be seen with oscilloscopes that have less bandwidth than 600 MHz. The most often encountered sources of clock noise spikes are inductive or capacitive coupling of high-speed logic signals, and ground bounce. The best solution for addressing clock spikes from coupling is to separate the traces and use short low inductance PC board traces. To address ground bounce problems, all integrated circuits should have high frequency bypass capacitors directly across their power supply pins, with low inductance traces for ground and power supply. A less than optimum solution may be to limit the bandwidth of the trace by adding series resistance and/or capacitance at the input pin.

MAXIMUM RATINGS (Voltages Referenced to V_{SS} Pin)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	− 0.5 to 6	V
Voltage on any Analog Input or Output Pin		V_{SS} − 0.3 to V_{DD} + 0.3	V
Voltage on any Digital Input or Output Pin		V_{SS} − 0.3 to V_{DD} + 0.3	V
Operating Temperature Range	T_A	− 40 to + 85	°C
Storage Temperature Range	T_{stg}	− 85 to +150	°C

POWER SUPPLY (T_A = − 40 to + 85°C)

Characteristics		Min	Typ	Max	Unit
DC Supply Voltage		4.75	5.0	5.25	V
Active Power Dissipation	(No Load, PI ≥ V_{DD} − 0.5 V) (No Load, PI ≤ V_{DD} − 1.5 V)	— —	23 25	33 35	mW
Power Down Dissipation (V_{IH} for logic levels must be ≥ 3.0 V)	$\overline{PDI}$ = V_{SS} FST and FSR = V_{SS}, $\overline{PDI}$ = V_{DD}	— —	0.01 0.1	0.5 1.0	mW

DIGITAL LEVELS (V_{DD} = + 5 V ± 5%, V_{SS} = 0 V, T_A = − 40 to + 85°C)

Characteristics	Symbol	Min	Max	Unit
Input Low Voltage	V_{IL}	—	0.6	V
Input High Voltage	V_{IH}	2.2	—	V
Output Low Voltage (DT pin, I_{OL} = 2.5 mA)	V_{OL}	—	0.4	V
Output High Voltage (DT pin, I_{OH} = − 2.5 mA)	V_{OH}	V_{DD} − 0.5	—	V
Input Low Current (V_{SS} ≤ V_{in} ≤ V_{DD})	I_{IL}	− 10	+ 10	µA
Input High Current (V_{SS} ≤ V_{in} ≤ V_{DD})	I_{IH}	− 10	+ 10	µA
Output Current in High Impedance State (V_{SS} ≤ DT ≤ V_{DD})	I_{OZ}	− 10	+ 10	µA
Input Capacitance of Digital Pins (except DT)	C_{in}	—	10	pF
Input Capacitances of DT pin when High-Z	C_{out}	—	15	pF

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = + 5 V ± 5%, V_{SS} = 0 V, T_A = – 40 to + 85°C)

Characteristics		Min	Typ	Max	Unit
Input Current	TI+, TI–	—	± 0.1	± 1.0	µA
AC Input Impedance to V_{AG} (1 kHz)	TI+, TI–	—	1.0	—	MΩ
Input Capacitance	TI+, TI–	—	—	10	pF
Input Offset Voltage of TG Op Amp	TI+, TI–	—	—	± 5	mV
Input Common Mode Voltage Range	TI+, TI–	1.2		V_{DD} – 2.0	V
Input Common Mode Rejection Ratio	TI+, TI–	—	60	—	dB
Gain Bandwidth Product (10 kHz) of TG Op Amp ($R_L \geq$ 10 kΩ)		—	3000	—	kHz
DC Open Loop Gain of TG Op Amp ($R_L \geq$ 10 kΩ)		—	95	—	dB
Equivalent Input Noise (C-Mess) Between TI+ and TI– at TG		—	– 30	—	dBrnC
Output Load Capacitance for TG Op Amp		0	—	100	pF
Output Voltage Range for TG (R_L = 10 kΩ to V_{AG}) (R_L = 2 kΩ to V_{AG})		 0.5 1.0	 — —	 V_{DD} – 0.5 V_{DD} – 1.0	V
Output Current (0.5 V ≤ $V_{out} \leq V_{DD}$ – 0.5 V)	TG, RO+, RO–	± 1.0	—	—	mA
Output Load Resistance to V_{AG}	TG, RO+, and RO–	2	—	—	kΩ
Output Impedance (0 to 3.4 kHz)	RO+ or RO–	—	1	—	Ω
Output Load Capacitance	RO+ or RO–	0	—	500	pF
DC Output Offset Voltage of RO+ or RO– Referenced to V_{AG}		—	—	± 25	mV
V_{AG} Output Voltage Referenced to V_{SS} (No Load)		2.2	2.4	2.6	V
V_{AG} Output Current with ± 25 mV Change in Output Voltage		± 2.0	± 10	—	mA
Power Supply Rejection Ratio (0 to 100 kHz @100 mVrms applied to V_{DD}, C-Message Weighting, all analog signals referenced to V_{AG} pin.)	Transmit Receive	50 50	80 75	— —	dBC
Power Drivers PI, PO+, PO–					
Input Current (V_{AG} – 0.5 V ≤ PI ≤ V_{AG} + 0.5 V)	PI	—	±0.05	±1.0	µA
Input Resistance (V_{AG} – 0.5 V ≤ PI ≤ V_{AG} + 0.5 V)	PI	10	—	—	MΩ
Input Offset Voltage	PI	—	—	±20	mV
Output Offset Voltage of PO+ Relative to PO– (Inverted Unity Gain for PO–)		—	—	±50	mV
Output Current (V_{SS} + 0.7 V ≤ PO+ or PO– ≤ V_{DD} – 0.7 V)		±10	—	—	mA
PO+ or PO– Output Resistance (Inverted Unity Gain for PO–)		—	1	—	Ω
Gain Bandwidth Product (10 kHz, Open Loop for PO–)		—	1000	—	kHz
Load Capacitance (PO+ or PO– to V_{AG}, or PO+ to PO–)		0	—	1000	pF
Gain of PO+ Relative to PO– (R_L = 300 Ω, + 3 dBm0, 1 kHz)		–0.2	0	+0.2	dB
Total Signal to Distortion at PO+ and PO– with a 300 Ω Differential Load		45	60	—	dBC
Power Supply Rejection Ratio (0 to 25 kHz @ 100 mVrms applied to V_{DD}. PO– Connected to PI. Differential or measured referenced to V_{AG} pin.)	0 to 4 kHz 4 to 25 kHz	40 —	55 40	— —	dB

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = + 5 V ± 5%, V_{SS} = 0 V, All Analog Signals Referenced to V_{AG}, 0 dBm0 = 0.775 Vrms = +0 dBm @ 600 Ω, FST = FSR = 8 kHz, BCLKT = MCLK = 2.048 MHz Synchronous Operation, T_A = – 40 to + 85°C, Unless Otherwise Noted)

Characteristics	End-to-End		A/D		D/A		Units
	Min	Max	Min	Max	Min	Max	
Absolute Gain (0 dBm0 @ 1.02 kHz, T_A=25°C, V_{DD} = 5.0 V)	—	—	– 0.25	+ 0.25	– 0.25	+ 0.25	dB
Absolute Gain Variation with Temperature 0 to +70°C	—	—	—	± 0.03	—	± 0.03	dB
–40 to +85°C	—	—	—	± 0.05	—	± 0.05	
Absolute Gain Variation with Power Supply (T_A = 25°C)	—	—	—	± 0.03	—	± 0.04	dB
Gain vs Level Tone (Mu-Law, Relative to –10 dBm0, 1.02 kHz)							dB
+ 3 to – 40 dBm0 @ 0 to +85°C	—	—	– 0.25	+ 0.25	– 0.20	+ 0.20	
+ 3 to – 40 dBm0 @ – 40 to 0°C	—	—	– 0.25	+ 0.25	– 0.25	+ 0.25	
– 40 to – 50 dBm0 @ 0 to +85°C	—	—	– 0.8	+ 0.8	– 0.5	+ 0.5	
– 40 to – 50 dBm0 @ – 40 to 0°C	—	—	– 0.8	+ 0.8	– 0.9	+ 0.9	
– 50 to – 55 dBm0 @ 0 to +85°C	—	—	– 1.3	+ 1.3	– 1.0	+ 1.0	
– 50 to – 55 dBm0 @ – 40 to 0°C	—	—	– 1.3	+ 1.3	– 1.8	+ 1.8	
Gain vs Level Pseudo Noise, CCITT G.712							dB
(A–Law, Relative to –10 dBm0) – 10 to – 40 dBm0	—	—	– 0.25	+ 0.25	– 0.25	+ 0.25	
– 40 to – 50 dBm0	—	—	– 0.60	+ 0.30	– 0.30	+ 0.30	
– 50 to – 55 dBm0	—	—	– 1.00	+ 0.45	– 0.45	+ 0.45	
Total Distortion, 1.02 kHz Tone (Mu-Law, C-Message Weighting)							dBC
+ 3 dBm0	—	—	34	—	34	—	
0 to – 30 dBm0	—	—	36	—	36	—	
– 40 dBm0 @ 0 to +85°C	—	—	30	—	30	—	
– 40 dBm0 @ – 40 to 0°C	—	—	28.5	—	28.5	—	
– 45 dBm0	—	—	25	—	25	—	
Total Distortion, Pseudo Noise, CCITT G.714 (A-Law)							dB
– 3 dBm0	—	—	30.0	—	30.0	—	
– 6 to – 27 dBm0	—	—	35.0	—	36.0	—	
– 34 dBm0	—	—	34.0	—	34.5	—	
– 40 dBm0 @ 0 to +85°C	—	—	28.5	—	29.5	—	
– 40 dBm0 @ – 40 to 0°C	—	—	28.0	—	28.5	—	
– 55 dBm0	—	—	13.5	—	14.5	—	
Idle Channel Noise (For End-to-End and A/D, See Note 1)							
(Mu-Law, C-Message Weighted)	—	—	—	18	—	11	dBrnc0
(A-Law, Psophometric Weighted)	—	—	—	– 68	—	– 78	dBm0p
Frequency Response (Relative to 1.02 kHz @ 0 dBm0)							dB
15 Hz	—	—	—	– 40	– 0.5	0	
50 Hz	—	—	—	– 30	– 0.5	0	
60 Hz	—	—	—	– 26	– 0.5	0	
200 Hz	—	—	– 1.0	– 0.4	– 0.5	0	
300 to 3000 Hz	—	—	– 0.20	+ 0.15	– 0.15	+ 0.15	
3300 Hz	—	—	– 0.35	+ 0.15	– 0.35	+ 0.15	
3400 Hz	—	—	– 0.8	0	– 0.8	0	
4000 Hz	—	—	—	– 14	—	– 14	
4600 Hz to 100 kHz	—	—	—	– 32	—	30	
Inband Spurious (1.02 kHz @ 0 dBm0, Transmit and Receive)							dB
300 to 3000 Hz	—	– 48	—	– 48	—	– 48	
Out-of-Band Spurious at RO+ (300 to 3400 Hz @ 0 dBm0 in)							dB
4600 to 7600 Hz	—	– 30	—	—	—	– 30	
7600 to 8400 Hz	—	– 40	—	—	—	– 40	
8400 to 100,000 Hz	—	– 30	—	—	—	– 30	
Idle Channel Noise Selective (8 kHz, Input = V_{AG}, 30 Hz Bandwidth)	—	– 70	—	—	—	– 70	dBm0
Absolute Delay (1600 Hz)	—	—	—	315	—	205	µs
Group Delay Referenced to 1600 Hz							µs
500 to 600 Hz	—	—	—	210	– 40	—	
600 to 800 Hz	—	—	—	130	– 40	—	
800 to 1000 Hz	—	—	—	70	– 40	—	
1000 to 1600 Hz	—	—	—	35	– 30	—	
1600 to 2600 Hz	—	—	—	70	—	85	
2600 to 2800 Hz	—	—	—	95	—	110	
2800 to 3000 Hz	—	—	—	145	—	175	
Crosstalk of 1020 Hz @ 0 dBm0 from A/D or D/A (Note 2)	—	—	—	– 75	—	– 70	dB
Intermodulation Distortion of two Frequencies of Amplitudes							dB
(– 4 to – 21 dBm0 from the Range 300 to 3400 Hz)	—	– 41	—	– 41	—	– 41	

NOTES: 1. Extrapolated from a 1020 Hz @ – 50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while stimulated with 2667 Hz @ – 50 dBm0.

DIGITAL SWITCHING CHARACTERISTICS, LONG FRAME SYNC AND SHORT FRAME SYNC

(V_{DD} = + 5 V ± 5%, V_{SS} = 0 V, All Digital Signals Referenced to V_{SS}, T_A = – 40 to + 85°C, C_L = 150 pF, Unless Otherwise Noted)

Ref #	Characteristics	Min	Typ	Max	Unit
1	Master Clock Frequency for MCLK	— — — — — — —	256 512 1536 1544 2048 2560 4096	— — — — — — —	kHz
1	MCLK Duty Cycle for 256 kHz Operation	45	—	55	%
2	Minimum Pulse Width High for MCLK (Frequencies of 512 kHz or Greater)	50	—	—	ns
3	Minimum Pulse Width Low for MCLK (Frequencies of 512 kHz or Greater)	50	—	—	ns
4	Rise Time for All Digital Signals	—	—	50	ns
5	Fall Time for All Digital Signals	—	—	50	ns
6	Setup Time from MCLK Low to FST High	50	—	—	ns
7	Setup Time from FST High to MCLK Low	50	—	—	ns
8	Bit Clock Data Rate for BCLKT or BCLKR	64	—	4096	kHz
9	Minimum Pulse Width High for BCLKT or BCLKR	50	—	—	ns
10	Minimum Pulse Width Low for BCLKT or BCLKR	50	—	—	ns
11	Hold Time from BCLKT (BCLKR) Low to FST (FSR) High	20	—	—	ns
12	Setup Time for FST (FSR) High to BCLKT (BCLKR) Low	80	—	—	ns
13	Setup Time from DR Valid to BCLKR Low	0	—	—	ns
14	Hold Time from BCLKR Low to DR Invalid	50	—	—	ns
	LONG FRAME SPECIFIC TIMING				
15	Hold Time from 2nd Period of BCLKT (BCLKR) Low to FST (FSR) Low	50	—	—	ns
16	Delay Time from FST or BCLKT, Whichever Is Later, to DT for Valid MSB Data	—	—	60	ns
17	Delay Time from BCLKT High to DT for Valid Chord and Step Bit Data	—	—	60	ns
18	Delay Time from the Later of the 8th BCLKT Falling Edge, or the Falling Edge of FST to DT Output High Impedance	10	—	60	ns
19	Minimum Pulse Width Low for FST or FSR	50	—	—	ns
	SHORT FRAME SPECIFIC TIMING				
20	Hold Time from BCLKT (BCLKR) Low to FST (FSR) Low	50	—	—	ns
21	Setup Time from FST (FSR) Low to MSB Period of BCLKT (BCLKR) Low	50	—	—	ns
22	Delay Time from BCLKT High to DT Data Valid	10	—	60	ns
23	Delay Time from the 8th BCLKT Low to DT Output High Impedance	10	—	60	ns

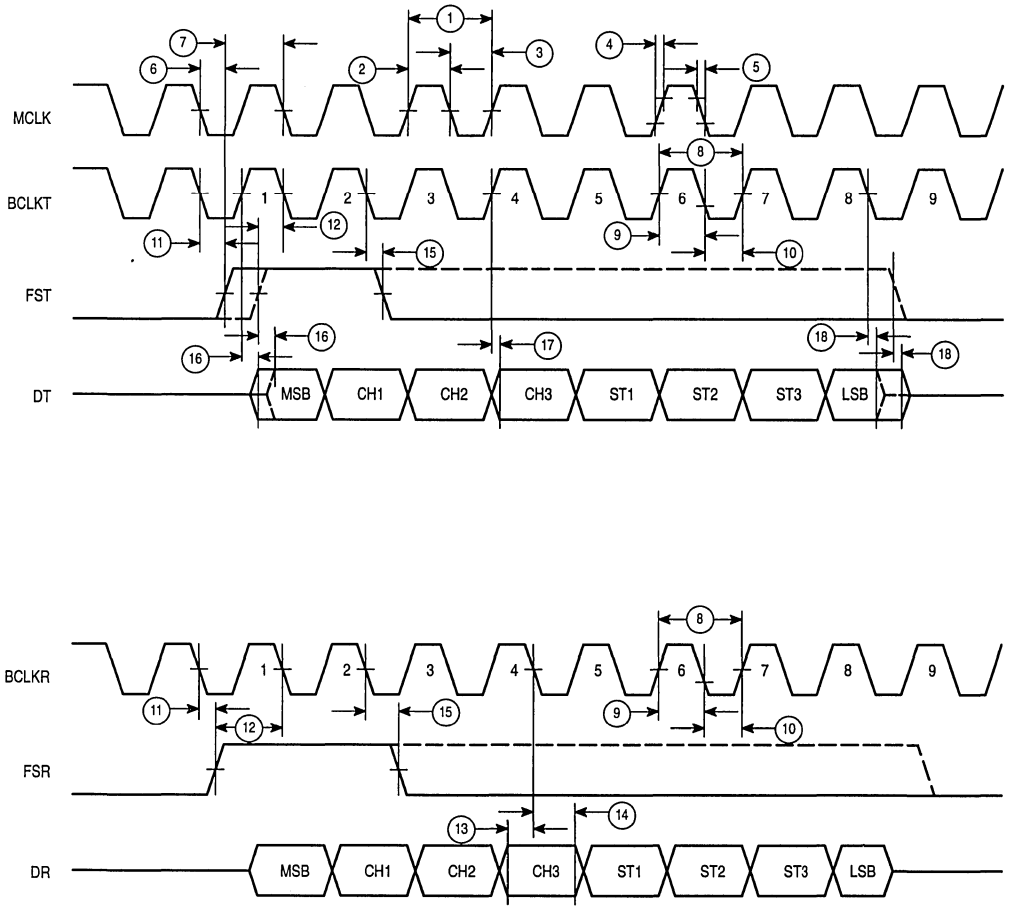


Figure 3. Long Frame Sync Timing

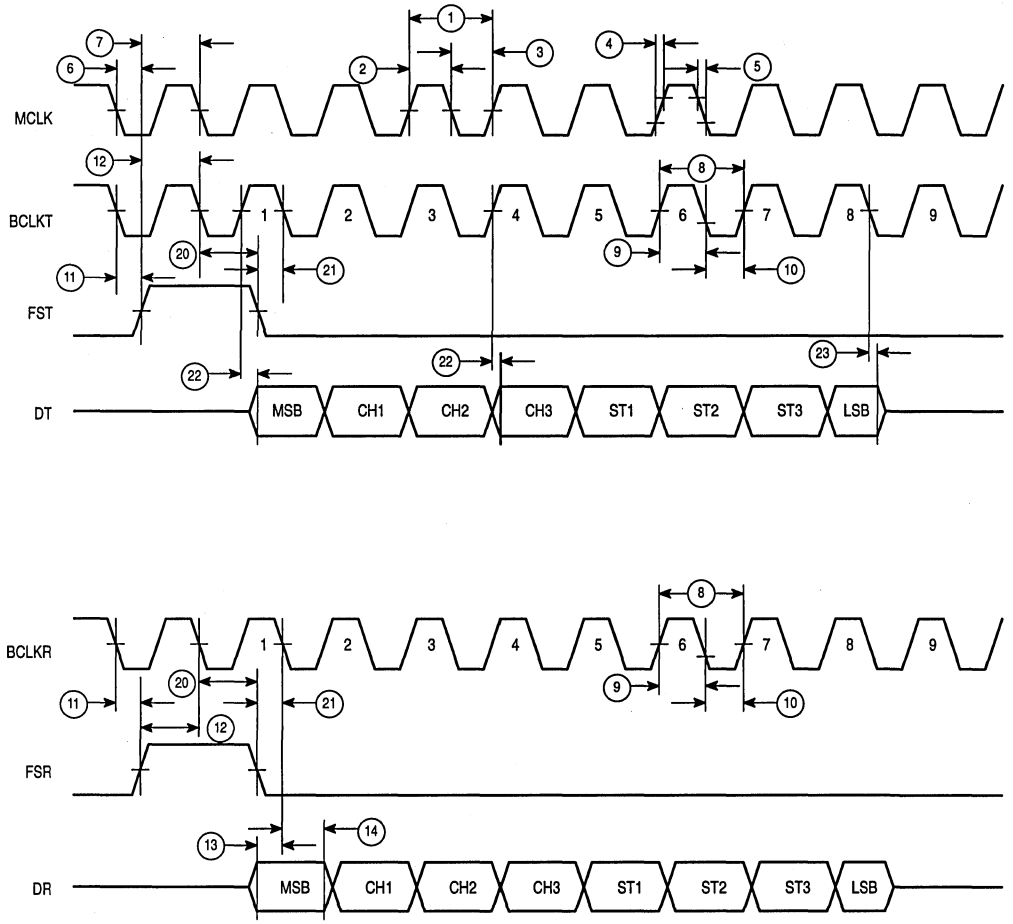


Figure 4. Short Frame Sync Timing

DIGITAL SWITCHING CHARACTERISTICS FOR IDL MODE

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 150 pF, See Figure 5, Note 1.)

Ref #	Characteristics	Min	Max	Unit
31	Time Between Successive IDL Syncs	Note 2		
32	Hold Time of IDL SYNC After Falling Edge of IDL CLK	20	—	ns
33	Setup Time of IDL SYNC Before Falling Edge IDL CLK	60	—	ns
34	IDL Clock Frequency	256	4096	kHz
35	IDL Clock Pulse Width High	50	—	ns
36	IDL Clock Pulse Width Low	50	—	ns
37	Data Valid on IDL RX Before Falling Edge of IDL CLK	20	—	ns
38	Data Valid on IDL RX After Falling Edge of IDL CLK	75	—	ns
39	Falling Edge of IDL CLK to High Z on IDL TX	10	50	ns
40	Rising Edge of IDL CLK to Low Z and Data Valid on IDL TX	10	60	ns
41	Rising Edge of IDL CLK to Data Valid on IDL TX	—	50	ns

NOTES: 1. Measurements are made from the point at which the logic signal achieves the guaranteed minimum or maximum logic level.
2. In IDL mode, both transmit and receive 8-bit PCM words are accessed during B1 channel or both transmit and receive 8-bit PCM words are accessed during the B2 channel as shown in Figure 5. IDL accesses must occur at a rate of 8 kHz (125 μs interval).

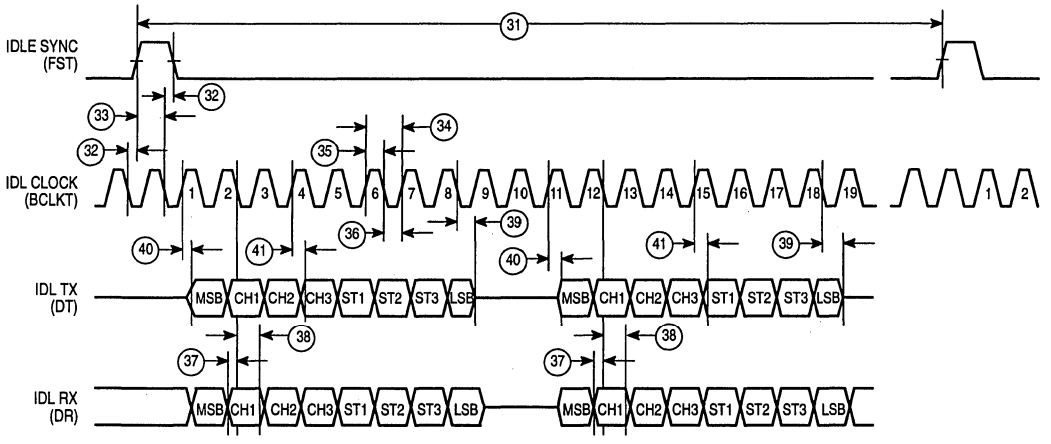


Figure 5. IDL Interface Timing

DIGITAL SWITCHING CHARACTERISTICS FOR GCI MODE

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 150 pF, See Figure 6, Note 1.)

Ref #	Characteristics	Min	Max	Unit
42	Time Between Successive FSC Pulses	Note 2		
43	DCL Clock Frequency	512	6176	kHz
44	DCL Clock Pulse Width High	50	—	ns
45	DCL Clock Pulse Width Low	50	—	ns
46	Hold Time of FSC After Falling Edge of DCL	20	—	ns
47	Setup Time of FSC to DCL Falling Edge	60	—	ns
48	Rising Edge of DCL (After Rising Edge of FSC) to Low Impedance and Valid Data of D_{out}	—	60	ns
49	Rising Edge of FSC (While DCL is High) to Low Impedance and Valid Data of D_{out}	—	60	ns
50	Rising Edge of DCL to Valid Data on D_{out}	—	60	ns
51	Second DCL Falling Edge During LSB to High Impedance of D_{out}	10	50	ns
52	Setup Time of D_{in} Before Rising Edge of DCL	20	—	ns
53	Hold Time of D_{in} After DCL Rising Edge	—	60	ns

NOTES: 1. Measurements are made from the point at which the logic signal achieves the guaranteed minimum or maximum logic level.
2. In GCI mode, both transmit and receive 8-bit PCM words are accessed during B1 channel or both transmit and receive 8-bit PCM words are accessed during the B2 channel as shown in Figure 6. GCI accesses must occur at a rate of 8 kHz (125 µs interval).

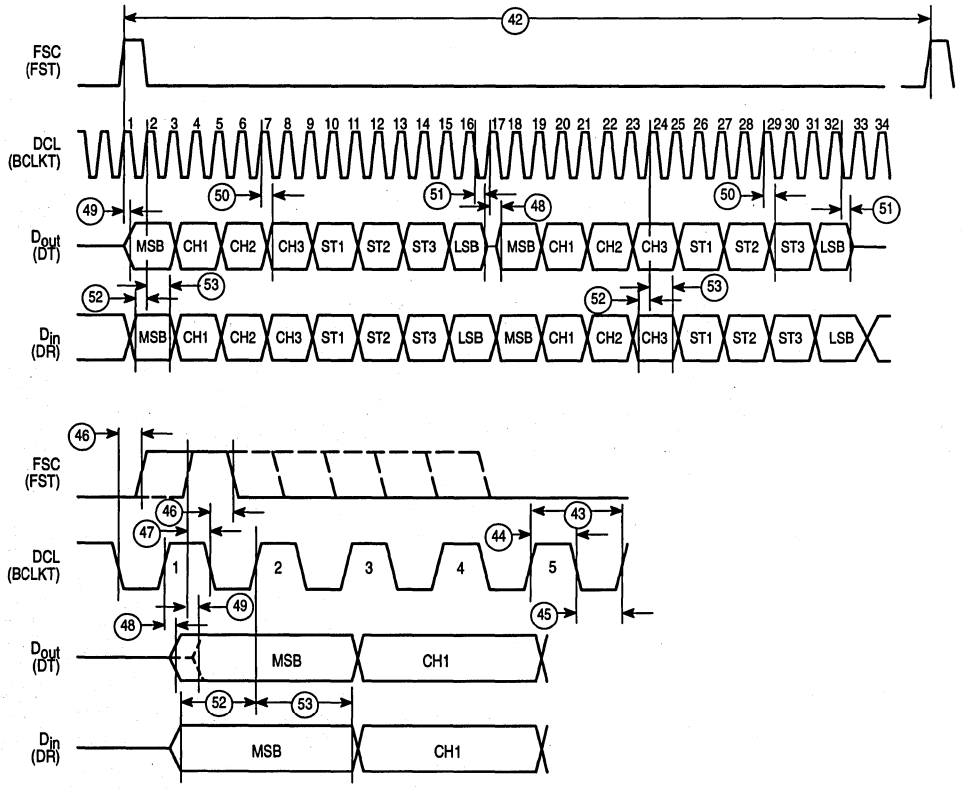


Figure 6. GCI Interface Timing

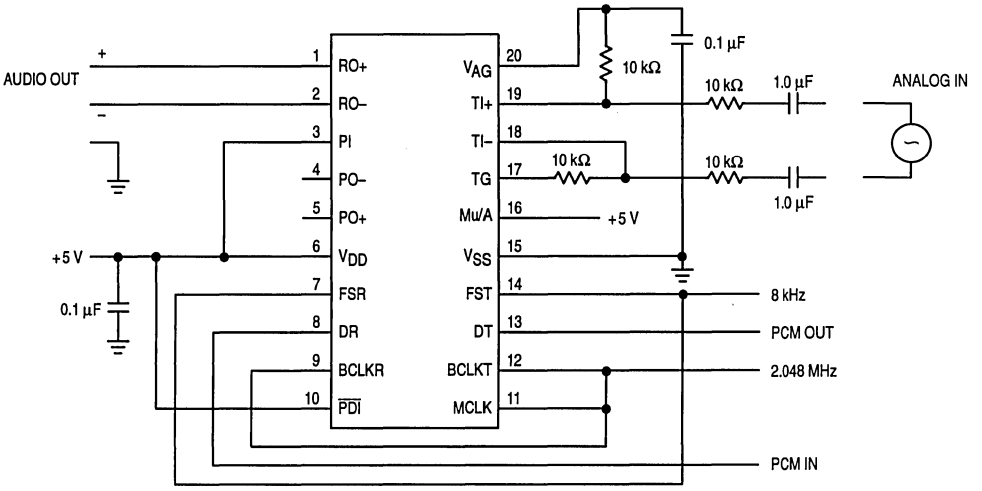


Figure 7. MC145480 Test Circuit with Differential Input and Output

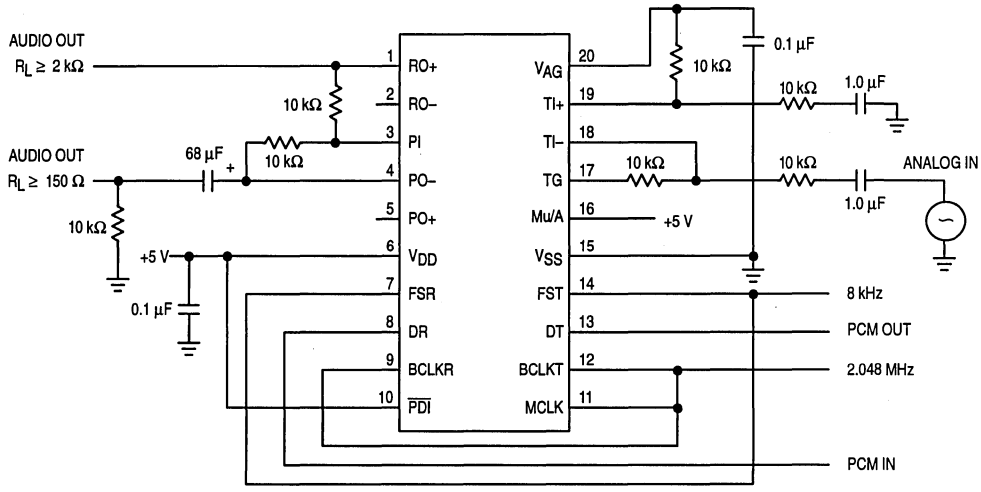


Figure 8. MC145480 Test Circuit with Input and Output Referenced to V_{SS}

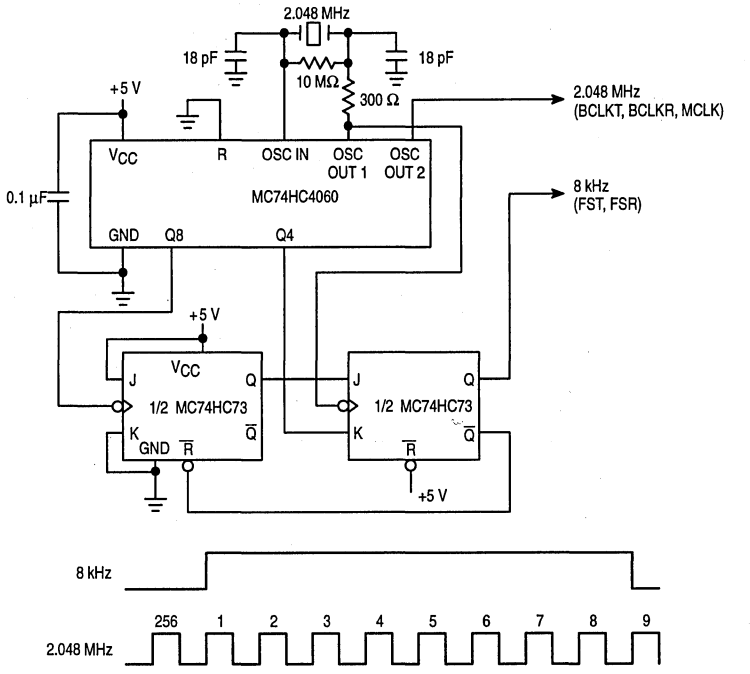


Figure 9. Long Frame Sync Clock Circuit for 2.048 MHz

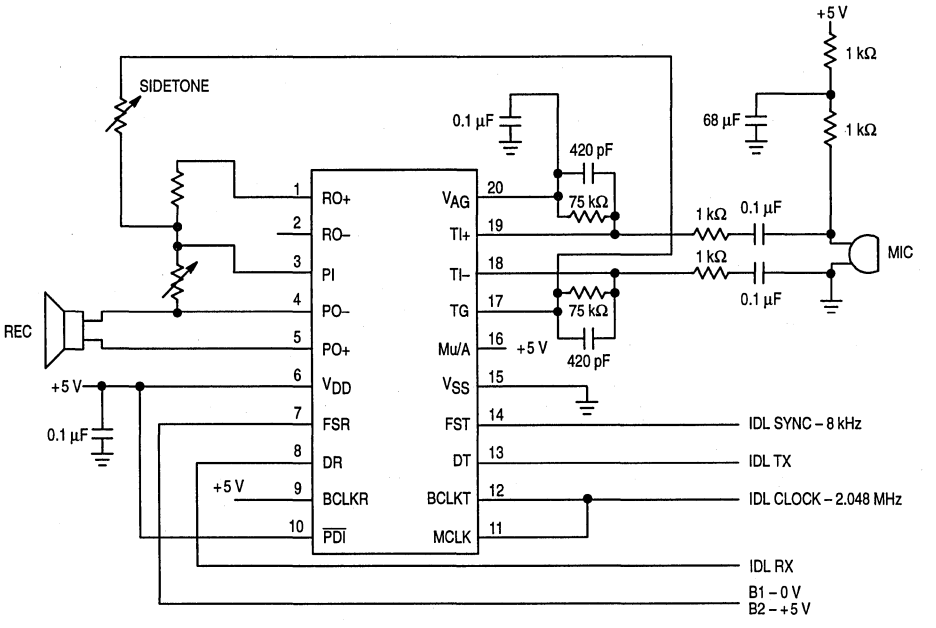


Figure 10. MC145480 Analog Interface to Handset with IDL Clocking

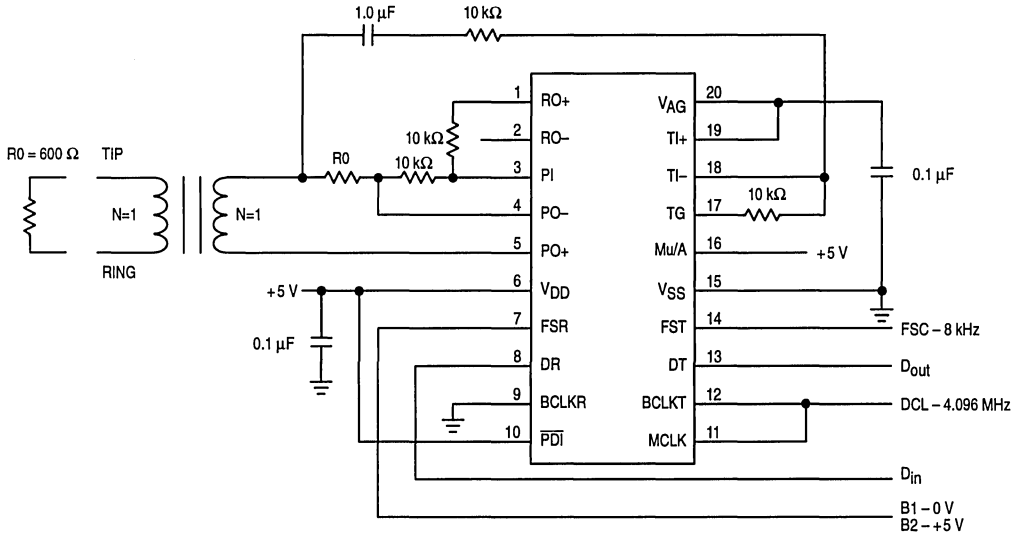


Figure 11. MC145480 Transformer Interface to 600 Ω Telephone Line with GCI Clocking

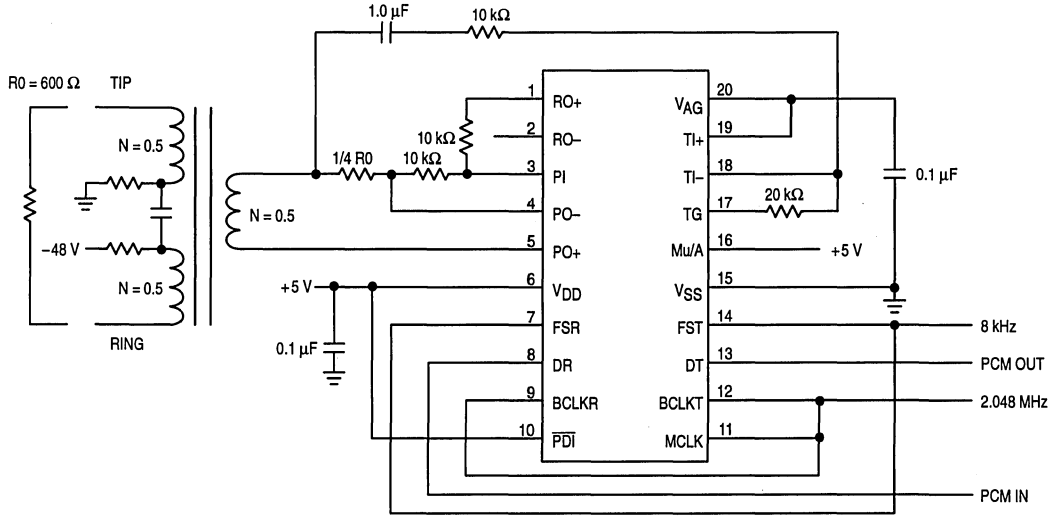


Figure 12. MC145480 Step-Up Transformer Interface to 600 Ω Telephone Line

Table 3. Mu-Law Encode-Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code								Normalized Decode Levels
				1	2	3	4	5	6	7	8	
				Sign	Chord	Chord	Chord	Step	Step	Step	Step	
			8159									
8	16	256	7903	1	0	0	0	0	0	0	0	8031
			:					:				:
			4319	1	0	0	0	1	1	1	1	4191
7	16	128	4063					:				:
			:									
			2143	1	0	0	1	1	1	1	1	2079
6	16	64	2015					:				:
			:									
			1055	1	0	1	0	1	1	1	1	1023
5	16	32	991					:				:
			:									
			511	1	0	1	1	1	1	1	1	495
4	16	16	479					:				:
			:									
			239	1	1	0	0	1	1	1	1	231
3	16	8	223					:				:
			:									
			103	1	1	0	1	1	1	1	1	99
2	16	4	95					:				:
			:									
			35	1	1	1	0	1	1	1	1	33
1	15	2	31					:				:
			:									
			3	1	1	1	1	1	1	1	0	2
	1	1	1	1	1	1	1	1	1	1	1	0
			0									

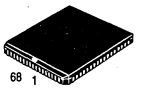
NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

Table 4. A-Law Encode-Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 (Sign)	2 (Chord)	3 (Chord)	4 (Chord)	5 (Step)	6 (Step)	7 (Step)	8 (Step)	Normalized Decode Levels
			4096									
7	16	128	3968	1	0	1	0	1	0	1	0	4032
			:					:				:
			2176	1	0	1	0	0	1	0	1	2112
			2048					:				:
6	16	64	1088	1	0	1	1	0	1	0	1	1056
			1024					:				:
5	16	32	544	1	0	0	0	0	1	0	1	528
			512					:				:
4	16	16	272	1	0	0	1	0	1	0	1	264
			256					:				:
3	16	8	136	1	1	1	0	0	1	0	1	132
			128					:				:
2	16	4	68	1	1	1	1	0	1	0	1	66
			64					:				:
1	32	2	2	1	1	0	1	0	1	0	1	1
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all even numbered bits.

MC145488



FN SUFFIX
PLCC
CASE 779

Technical Summary

Dual Data Link Controller

This Technical Summary gives a brief overview of the MC145488 Dual Data Link Controller. The MC145488 is a two-channel ISDN LAPD controller with an on-chip direct memory access (DMA) controller. It is intended for ISDN terminal and switch applications where one or two channels of data will use HDLC-type protocols. The DDLC can also be used in local area, wide area network, and bridge router applications. Each serial interface can be clocked at data rates up to 10 Mbps. The DDLC can operate with microprocessors using clock frequencies up to 20.5 MHz.

The DDLC is ideally suited for use with the MC145474 S/T transceiver. The interchip digital link (IDL) easily connects the chips together, providing a powerful layer one/layer two ISDN solution. A serial control port is provided to efficiently control the MC145474 or other ISDN family devices. The DDLC is compatible with 68000 and 80186 bus structures.

Note

This document is a summary of principal features and operation of the DDLC. Please refer to the MC145488 DDLC data book for the complete description and electrical specifications. It can be ordered from your local Motorola sales office or from the Motorola Literature Distribution Center as MC145488/D.

- Two Independent Full-Duplex Bit-Oriented Protocol Controllers Support
  - — HDLC, SDLC, CCITT X.25, CCITT Q.921 (LAPD), and V.120 at Basic
  - — and Primary Rates
- Four Channel On-Chip DMA Controller
  - — 64 Kbyte Address Range with Expansion Control
  - — Internal Programmable Wait-State Generator
  - — Two Buffer Descriptors for Each Receiver Channel
- Compatible with 68000 and 80186 Bus Structures
  - — Non-multiplexed 16- or 8-Bit Data Bus
  - — Frame sizes up to 4096 bytes
- Bit-Level HDLC Processing Including:
  - — Flag Generation/Detection
  - — Abort Generation/Detection
  - — Zero Insertion/Deletion
  - — CRC-CCITT Generation/Checking
  - — Residue Bit Handler
- TEI/SAPI Address Comparison
  - — Three Address Comparisons
  - — Wildcard Bits for Block Comparisons
- Transparent Mode for Codec Compatibility
- Programmable Interrupt Vector Generation
- Two Independent Timers Configurable as a Watchdog Timer
- Flexible Serial Interface with:
  - — IDL Interface for Connection to Other ISDN Family Devices
  - — Timeslot Interface for Connection to PBX-Type Backplanes
  - — Modem Interface for Other Applications
- Supports CCITT Specification 1.460
- Supports DMI Specification 3.1 Modes 0, 1, 2, and 3
- Serial Control Port for ISDN Family Device Control
- Low-Power CMOS with Automatic Power-Down
- Serial Data Rates Up to 10 Mbps
- DDLC Master Clock Up to 20.5 MHz

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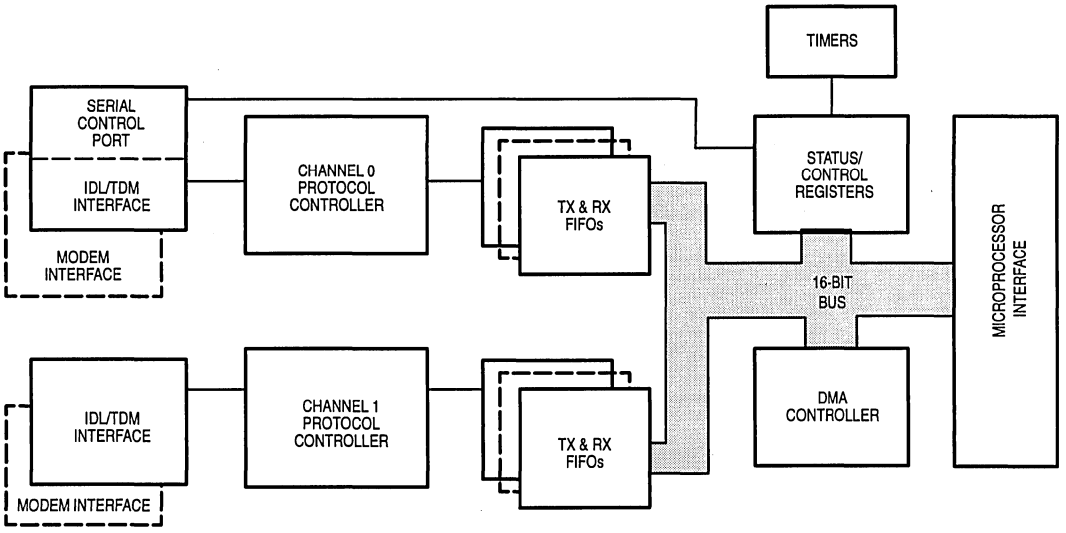
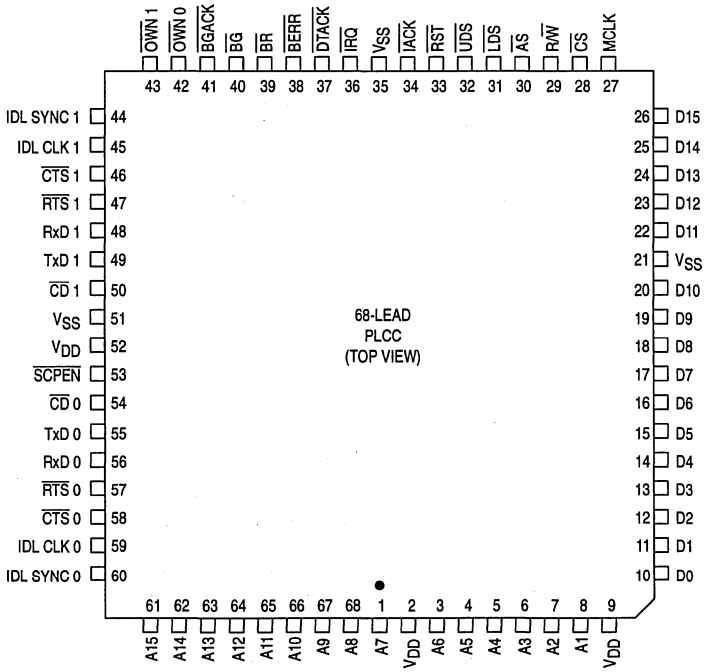
BLOCK DIAGRAM



PIN ASSIGNMENTS



GENERAL DESCRIPTION

DDLC OVERVIEW

The MC145488 Dual Data Link Controller (DDLC) is a high-performance two-channel protocol controller with an on-chip direct memory access controller (DMAC). Each channel has a full-duplex transceiver with independent protocol controllers to handle the bit-level tasks of HDLC-type bit-oriented protocols, including LAPB and LAPD. Each channel also has dedicated DMA controllers for transmit and receive. A transparent mode is provided which bypasses the protocol circuitry so that serial data may be directly transferred between the host processor's memory and the serial interface. The DDLC's microprocessor interface is configurable to 68000 or 80186 systems and may be used in 8-bit or 16-bit bus modes. The DDLC's master clock can be obtained from microprocessor clocks up to 20.5 MHz.

Each channel has a serial data interface which operates up to and above T1 or E1 primary rate speeds in three modes: IDL, Timeslot, and Modem. In the IDL (Interchip Digital Link) mode for ISDN applications, the IDL bus is supported. When in the IDL D channel mode, the DREQ and DGRNT access control lines to the ISDN D channel, through the MC145474 S/T transceiver, are enabled. The timeslot mode is used to connect the DDLC to PBX-type PCM highway backplanes. Both long-frame and short-frame timing are supported as well as synchronous transmit and receive. In the modem mode, each channel has its own separate transmit and receive clock inputs along with modem control lines (RTS, CTS, and CD). The two channels are independent and may be in different interface modes.

A serial control port (SCP) is provided to pass control information to other devices in a system. The SCP is compatible with Motorola's Serial Peripheral Interface (SPI) and National Semiconductor's MICROWIRE™ Plus. Two internal timers may be used for general purpose, low resolution timing of HDLC-type protocols. One of the timers may be configured as a watchdog timer to reset the entire system in the event of a hardware or software failure.

Power consumption is an important aspect of ISDN terminal designs, and the DDLC was designed to use the minimum power possible while maintaining maximum functionality. The DDLC keeps power consumption to a minimum with an automatic power-down feature that turns off sections of circuitry that are not being used. Only those circuits that are actually used (e.g., when the $\overline{CS}$ pin is activated for a register read/write or when the DMA controller performs a bus transaction) enter the normal power state for the duration of the access and for any time required for internal processing.

Two internal loopback functions and special chip and system test modes are available. The loopbacks are controlled by the host for on-line maintenance. The test modes are activated by bits in the master control register and provide access to the internal state machines.

HDLC PROTOCOL OVERVIEW

HDLC (High-Level Data Link Control) and its descendants, LAPB (Link Access Protocol-Balanced) and LAPD (Link Access Protocol for the D channel), are bit-oriented synchronous protocols which are widely used in data communications systems. LAPB and LAPD share the basic format of HDLC but differ in minor aspects (see Figure 1).

In the packet mode, the DDLC transmits and receives data in a format called a frame or packet. All frames start with an opening flag and end with a closing flag. Between the flags, a frame contains an address field, control field, information field, and a cyclic redundancy check field (CRC).

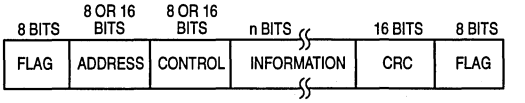


Figure 1. HDLC Frame Format

Flag

The flag is the unique binary pattern (01111110). It provides the frame boundary and a reference for the position of each field of the frame.

Address Field

The 8- or 16-bits following the opening flag comprise the address field. The address field is used to distinguish between the various devices in a network. The DDLC has address recognition circuitry included, which relieves the host from this task.

Control Field

The 8 or 16 bits following the address field are the control field. Commands and responses between the devices in a network are exchanged in this field.

Information Field

This field follows the control field and precedes the CRC field. The information field contains the data to be transferred and may be a null field.

Cycle Redundancy Check Field

The 16-bits preceding the closing flag are the Cycle Redundancy Check (CRC) field. This field detects bit errors in the address, control, and information fields. Checking is with the standard CCITT polynominal $x^{16} x^{12} x^5 + 1$ for both the transmitter and receiver. The transmitter calculates the CRC on all bits of the frame (except for the flags) and transmits the complement of the resulting remainder as the CRC field. The receiver performs the similar computation on all bits (except for the flags) and compares the result to F0B8.

Zero Insertion and Deletion

Zero insertion and deletion, which allows the content of the frame to be transparent, is automatically performed by the DDLC. A binary 0 is inserted by the transmitter after any succession of five 1s within a frame (between flags). This eliminates the possibility of data imitating a flag character. The receiver deletes all 0s that were inserted by the transmitter to regenerate the original data.

Abort

The function of prematurely terminating a data frame is called an abort. The transmitter aborts a frame by sending between seven and fourteen consecutive 1s. When the receiver detects an abort character, it responds by clearing the FIFO and clearing the buffer in memory. It then begins searching for a new frame.

Idle and Interframe Time Fill

For LAPB and other applications, there are three states that the data link may be in: in-frame, inter-frame time fill, and idle. In-frame is the period from the beginning of an opening flag and the end of a closing flag. Inter-frame time fill is the period between frames when continuous flags are transmitted. Idle is an out-of-frame period when continuous 1s are on the link. In LAPD, on the D channel, there are only two states: inframe and idle. Continuous flags are not transmitted between frames.

BLOCK DIAGRAM DESCRIPTION

This section is a brief overview of the internal blocks of the DDLC. The blocks include two protocol controllers that handle the bit-level aspects of HDLC-like packet protocols and four FIFOs that buffer the data, a four-channel DMA controller, and a microprocessor interface block that connects the DDLC to the host system. Figure 3 is a simplified block diagram of the DDLC. While the DDLC has two data transceivers, only one is shown for simplicity.

TRANSMIT BIT HANDLER

Two identical bit-level protocol transmitters are provided which perform HDLC-type framing. This section describes the operation of only one transmitter, but it applies to both.

Packet Operation

The transmitter is designed to operate with as little intervention from the host processor as possible. To transmit a frame of data, the host merely informs the DDLC of the starting address of the data frame in memory and the length of the frame in bytes. The DDLC then transmits an opening flag and the data (LSB first) from memory. When the transmitter detects that the end of the data buffer has been reached, a CRC field and a closing flag are appended. The transmitter generates an abort character if the FIFO underruns. During inter-frame periods, the DDLC can be configured to transmit either continuous flags (7E hex) or continuous marks (FF hex).

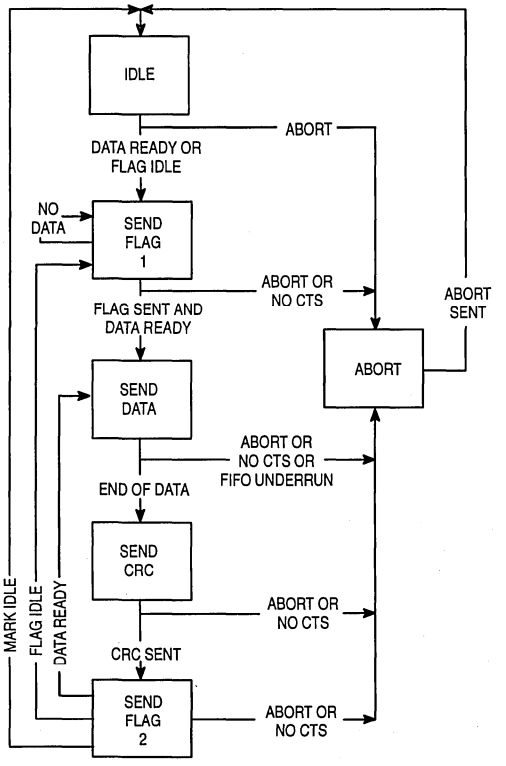


Figure 2. Transmitter State Diagram HDLC Operation

State Diagram

Figure 2 is the state diagram for the transmitter in packet operation.

Abort

The DDLC can be configured to transmit a standard HDLC abort character. It can also transmit an abort character which is compatible with DMI 3.1 modes 2 or 3 for restricted B-channel applications. An abort character will be transmitted when the TX Fifo underruns, when the Force Abort bit is set in the Transmit Control Register, or when the CTS pin is deasserted.

Flow Control Mechanisms

The DDLC provides two flow control mechanisms: one for basic rate ISDN applications and the other for standard modem applications. The following paragraphs describe the operation of the two schemes.

ISDN D Channel Contention

When the DDLC is operating on the D channel with the companion MC145474 S/T transceiver, the DREQ and DGRNT lines must be used to comply with the basic rate D channel contention algorithm. When the DDLC has a data frame to transmit, it asserts DREQ (high). When DGRNT is detected high from the MC145474 transmission from the DDLC begins in the IDL D-bit time slots when DREQ and DGRNT are both active. If DGRNT is deasserted (goes low) in the middle of a frame, the DDLC automatically aborts the frame in progress and prepares to retransmit the entire frame when the D channel becomes available again. This is done without interrupting the host.

Modem Flow Control

The transmitter indicates to a modem that it has data ready to transmit with signals similar to D channel operation. In this mode, Request-To-Send ($\overline{RTS}$) is directly controlled by the Transmit Enable (TE) bit. When TE is high, the $\overline{RTS}$ pin is asserted (low). During inter-frame periods, either flags or marks (as selected) are transmitted but the $\overline{RTS}$ pin remains asserted until the user negates the TE bit. Transmission of a frame, if one is ready, actually begins when the modem asserts Clear-to-Send ($\overline{CTS}$ low). If $\overline{CTS}$ is negated for more than one Tx CLK period while a frame is in transmission, the frame is aborted and the DMA pointers are reset so that the frame can be retransmitted without interrupting the host.

Interrupts

There is one interrupt generated by the transmitter state machine. Transmit Frame Complete indicates that an entire frame and its closing flag have been successfully transmitted. Ordinarily, this interrupt is used for basic rate ISDN D channel operation. Two other interrupts associated with the transmitter are generated by the DMA controller and are discussed in the section describing the DMA controller.

Transmit FIFO

The transmitter has a FIFO which buffers it from the DMA controller. It is four characters deep and nine bits wide. The ninth bit is a Tag bit which is set when the the last byte of a frame is read from memory by the DMA controller. After the tagged byte, the DDLC sends a closing CRC and flag sequence.

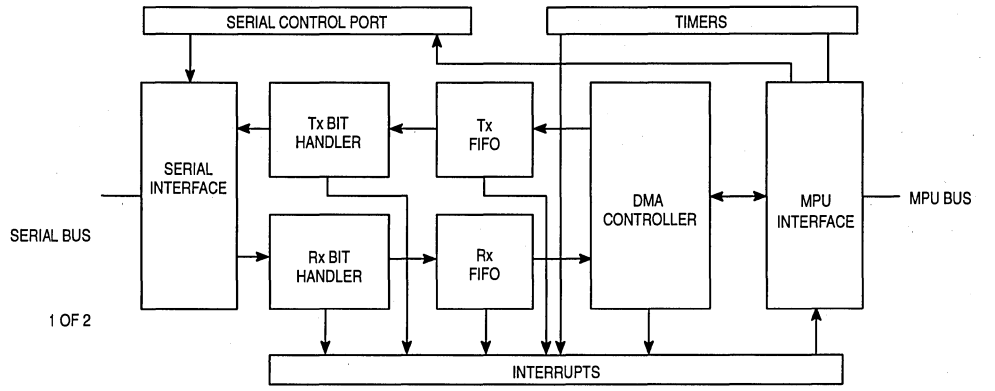


Figure 3. DDLC Block Diagram (One Transceiver Shown)

Transparent Operation

The transmitter has the capability of operating with unframed data such as PCM-encoded voice or proprietary protocols. Raw data may be transmitted from memory with byte alignment maintained through the FIFO and transmitter. Byte alignment signals must be provided. In the modem mode, the alignment signal is externally generated. In IDL and timeslot operation, it is internally generated but user programmable. The DDLC transmits data continuously as long as there is data to transmit.

Interframe Time Fill

The bit sequence that is transmitted between frames is determined by the value of the ITF bit in the Transmit Control register. The interframe time fill can be either the X.25 flag character (7E hex) or the LAPD marks (1) idle.

RECEIVE BIT HANDLER

The receiver provides the complementary functions to the transmitter. This section describes the operation of one receiver, but it applies to both receivers.

Packet Operation

The receiver is reset and idle until the Receive Enable bit is set, at which time it begins searching for a flag character. When a flag is found, the selected address field of the frame, if desired, is checked and if a match is found, the DDLC passes the frame of data to the allocated buffer in memory. If no address match is found, the DDLC clears the FIFO, resets the DMA pointers, and searches for a new frame. Zeros inserted by the transmitter are removed from the data before placing the bytes in memory. When the closing flag is detected, the CRC field is checked and if found to be correct, the DDLC queues an interrupt indicating that a good data frame has been received and is in memory. If the CRC is found to be in error, the DDLC automatically resets the buffer pointers to the start of the buffer and searches for a new frame.

Each receiver has two receive buffers, A and B. This permits one buffer to be actively receiving a frame while software is obtaining the data from and reinitializing the other buffer. If an incoming frame is longer than the length defined for the active receive buffer, the DDLC will switch to the second buffer if it is enabled.

If an abort character is found, the buffer pointers in the DMA controller are reset and the aborted frame is ignored. The FIFO is cleared and the receiver begins searching for a flag. No interrupt is generated.

State Diagram

Figure 4 shows the state diagram of the receiver.

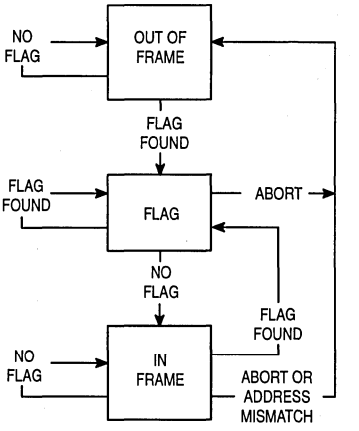


Figure 4. Receiver State Diagram HDLC Operation

Non-Octet Aligned Packets

The receiver has the capability of operating in non-octet aligned packet systems. The residue bit count indicating the number of orphan data bits at the end of the information field is placed in the RC bits of the Receive Status register. These bits are valid until overwritten by another frame. In non-octet aligned systems, the software should check the residue count soon after receiving a Receive Buffer Complete Interrupt to ensure that the residue count is not overwritten by the next frame. Orphan bits are LSB justified in memory. **Note:** The DDLC does not transmit non-octet aligned frames.

Address Recognition (Filtering)

The receiver can filter received frames by comparing their address fields to user programmable addresses. Two addresses may be programmed with another (broadcast, FF

hex) hardwired into the receiver. Address filtering may be performed on either the first OR second octet following the opening flag of a frame. Typically, in ISDN terminal applications, the TEI address (second) field will be of interest. In network applications, the SAPI (first) field will be checked. A separate Wildcard register allows selected bits of Compare Address 0 to be ignored during the comparison procedure. If received frames are rejected by address recognition, the receiver is reset and searches for a new frame. Address recognition may be disabled by clearing the Address Compare Enable bit to 0.

Receive FIFO

The receiver has a FIFO that is similar to the transmitter's. It is four characters deep and ten bits wide (eight bits for data and two bits for the Tag). Serial bytes are produced by the receiver and converted to parallel. As each byte is formed, it is pushed into the FIFO. A comparator in the controller keeps track of the occupancy of the FIFO and requests that the DMA controller place a word of data (16-bits) in memory when there are two or more bytes in the FIFO. In 8-bit operation, the FIFO requests service when one or more bytes of data read are ready to be placed in memory. If the FIFO overruns because the DMA controller did not service a request, an interrupt is queued. When a receiver is operating at 64 kbps in the 16-bit mode, DMA requests from that FIFO occur at approximately 250 µs intervals.

Transparent Operation

The DDLC receiver provides a transparent operation mode for passing raw octet-aligned serial data to memory via DMA. This feature is useful for storing PCM voice or proprietary protocols in memory. When using the DDLC to pass PCM voice to memory, maximum buffer size of 4096 bytes should be used. The Receive Buffer Overrun Interrupt is used in conjunction with Receive Buffers A and B that are available for each channel when transparent mode is used. Because the transparent mode requires that data be in eight-bit quantities, synchronization procedures for defining octet boundaries are required. In the modem mode, the sync signal is externally generated and input on the $\overline{CD}$ pin. In IDL mode timeslot operation, the sync signal is internally generated but user programmable. Once byte alignment is obtained in the receiver, it is maintained through the DMA controller into memory.

Interrupts

There are two interrupts generated by the receiver. The receiver queues an interrupt when a frame has been successfully received. The receive idle interrupt indicates that 15 or more consecutive 1s were received. This interrupt is considered normal operation. The current status of receive idle and carrier detect is available in the Receive Status register, but the user must remember that they can change immediately after being read. The carrier detect pin also generates an interrupt when it changes state.

DMA CONTROLLER

In order to relieve the host software from critically timed data transfers to or from the protocol controllers, the DDLC provides four DMA channels, one for each transmitter and receiver.

DMA Operation

When the DMA controller detects a service request from one of the FIFOs, it prepares the address and data from the transfer then requests ownership of the system bus from the host. When ownership is granted, the DMA controller assumes control of the bus and transfers data either to or from memory. Transfers are 16 bits or 8 bits, depending on the selected bus width. When the number of bytes in a received frame is odd, the last byte is placed in the most significant byte of the last word. The least significant byte contains unknown data. The receive byte count contains the correct number of bytes received (including the CRC). When odd length frames are transmitted, the last word read from memory has the last byte transmitted in the most significant byte, and the least significant byte of that word is discarded.

The DMA controller uses a round robin strategy to service internal DMA requests. A channel that was just serviced is not polled again until all other channels have been polled and serviced, if needed. The DDLC services one DMA request per bus arbitration cycle. The DDLC does not perform burst DMAs, so other devices can have access to the microprocessor bus. This type of operation improves system performance and guarantees that the DDLC is well behaved.

It is impossible to precisely predict what the DDLC bus occupancy will be, but worst case with both channels operating full-duplex at 64 kbps (aggregate rate of 256 Kbps) in a 16-bit 68000 system with a 12 MHz MCLK, approximately 0.66% of the host bus bandwidth is consumed by the DDLC. Bus occupancy increases linearly with data rate. At very high data rates, latency from the bus request to the bus grant and interrupt service latency become the limiting factors. It must also be kept in mind that the DDLC can generate interrupts quickly, especially with a large number of small data packets at a high clock rate.

Buffer Descriptors

As previously stated, the DDLC has four DMA channels. Pointer registers and counters are required so that the DMA controller knows where to place or fetch data in memory.

Transmit Buffer Descriptors

When the host has a frame of data to transmit, it informs the DMA controller where the data resides in memory. A 16-bit register, the Transmit Base Address register, points to the first word of the transmitted frame and provides a 64 kbyte address range. The host programs the address of the first word to be transmitted into this register. The length of the data frame must also be given to the DMA controller, so a 12-bit Transmit Frame Length register is used to indicate the length of the frame in bytes. Frames of up to 4096 bytes in length may be transmitted.

Back to back frames can be transmitted by updating the transmit buffers when the Transmit DMA Complete interrupt is generated.

Note

Once a transmit buffer descriptor has been prepared, it must not be disturbed until the transmit DMA complete or transmit frame complete interrupts are generated.

Receive Buffer Descriptors

The receive buffer descriptors have a 16-Bit Receive Buffer Base Address register, a 12-Bit Buffer Length register, and a 12-Bit Frame Length register. The 16-Bit Base Address register provides 64 kbyte address range and contains the address of the first word of the data buffer to accept a data frame. The 12-Bit Frame Length register indicates the length of the memory buffer in bytes. Buffers of up to 4096 bytes may be built. The DMA controller never places data outside of the boundaries set-up by these two registers. The Frame Length register indicates the number of bytes (including the CRC) received.

Each channel has a pair of buffer descriptors. These may be used alternately so that while one buffer is filling, another buffer is ready in-waiting. If back-to-back data frames are received, after the first buffer has been closed the second is immediately ready for the next frame. There must be at least one buffer ready to accept data when the Rx Enable bit is set. Figure 6 describes the activity of the receiver with four buffers in memory.

If a packet is being received and no buffers are ready, the receive FIFO will overrun, the Receiver Enable bit is reset, and an interrupt is queued indicating the overrun. If both descriptors are ready, then Buffer A is filled first. If a received frame is larger than a buffer, the Buffer (A or B) Overrun Interrupt is queued, but the receiver continues to receive and the DMA controller places the data in the alternate buffer (if it is available). If an alternate buffer is not ready, the Rx FIFO Overrun Interrupt is generated and the receiver is reset.

Once a data frame has been completely received, the number of bytes received is indicated in the Frame Length register. The number in this register is valid only when the Receive DMA Complete bit (Buffer A or Buffer B) in the Receive Status register is set to '1'.

Note: As with the transmitter, once a receive buffer descriptor has been prepared, it must not be disturbed until the closing flag has been found and DMA activity on the buffer has stopped.

Address Expansion

The DDLC provides signals for expansion of the 64 kbyte address space. The $\overline{OWN}$ pins are activated with timing identical to the address pins to enable external address expansion circuitry onto the address bus. Using the $\overline{OWN}$ pins with the R/$\overline{W}$ pin, the transmit and receive buffers may all be on separate 64 kbyte pages in memory.

Transmit Channel Operation

Figure 6 is a simplified state diagram of the DMA controller's operation when a transmit channel requests service.

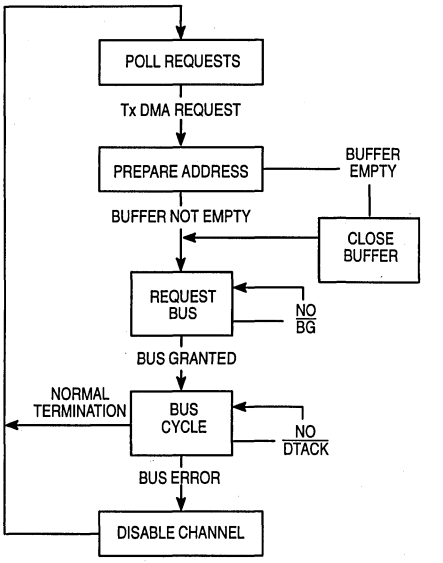


Figure 5. Transmit DMA State Diagram

Four interrupts are produced by the transmitter DMA channel. Transmit DMA Complete indicates that the last byte of data has been transferred from the buffer into the transmit FIFO. FIFO Underrun indicates the DMA requests were not serviced and the FIFO underran. Bus Error is generated when the $\overline{BERR}$ pin is activated during a DMA cycle. Address Error is generated when either $\overline{IACK}$ or $\overline{CS}$ are activated during a DMA cycle.

Receive Channel Operation

Figure 8 is a simplified state diagram for operation of the DMA controller when a receive channel requests service.

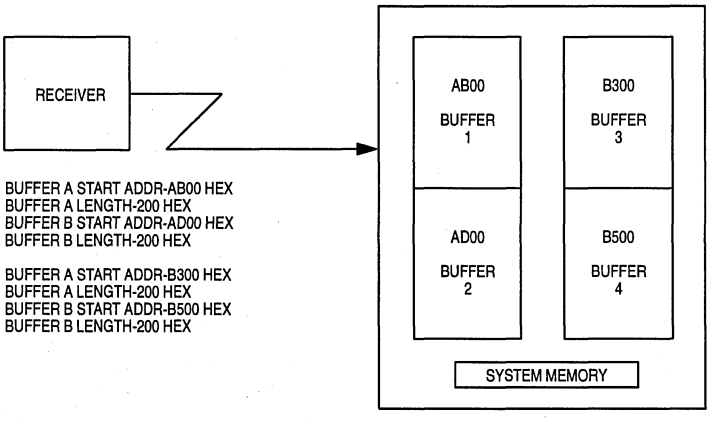


Figure 6. Alternate Receive Buffer Operation

MICROPROCESSOR INTERFACE

The microprocessor block interfaces the internal 16-bit bus to the host 8- or 16-bit bus. The block also performs all timing conversion and buffering. This block has three modes of operation described in this section: system slave, system master, and interrupt generator.

System Slave Mode

When the DDLC is in this mode, it appears as fast memory to the host processor. The host can read from or write to the registers in the DDLC. This mode is entered when the $\overline{CS}$ pin is activated. Internal address decoding circuitry is selected and the desired register is connected to the internal bus for access by the host.

System Master (DMA) Mode

During DMA operation, the DDLC becomes a system master and controls the system bus. When one of the internal FIFOs requests a DMA transfer, the DDLC negotiates with the system host for ownership of the bus. After successful negotiation, one DMA request is serviced, and then the bus is relinquished. The DDLC has the capability of reading or writing data from or to memory. If the memory system is slow, the DDLC inserts wait states (user selectable) until the memory is ready to complete the access. The DDLC has the capability of recovering from system faults such as address or bus errors.

Interrupt Operation

The DDLC has 27 vectored interrupt sources to inform the host of its status. One group of interrupts is normal operation interrupts. These inform the host that a particular task was completed and that new tasks are desired. Another group is bit handler faults, which inform the host that a DDLC channel detected a fault from which it cannot recover without assistance from the host. A third group is the timer and SCP interrupts. The last group of interrupts is the system faults. These include DMA bus and address errors. The interrupts are presented to the host as a vector number in an interrupt acknowledge cycle. The interrupts are encoded into the low four bits so the DDLC vector space consumes 16 out of 256 locations. Software can program the base vector number, so the DDLC vectors can be located anywhere within the vector table. For applications not using vectored interrupts, the equivalent vector number is accessible in the Master Status register.

SERIAL INTERFACE

The serial interface block has a variety of configurations that make it compatible with most common interfaces. Each serial interface is independent, so two different configurations may be active simultaneously. The serial interface has an IDL mode, a timeslot mode, and a general purpose modem mode. The serial interface supports long frame and short frame timing. It also supports subrate multiplexing. The serial mode is selected by programming the appropriate bits in the Serial Interface Control register.

A full set of serial interface control and handshake pins are provided. The name and functionality change to reflect the serial mode of operation. Separate receive and transmit clock inputs are provided for all modes except IDL and timeslot modes.

The serial interface also supports transfer of transparent data. Depending on which type of serial interface is used, an external synchronization signal must be provided to maintain byte alignment. In IDL mode, the byte synchronization is programmed by the microprocessor.

SERIAL CONTROL PORT

A Serial Control Port, similar to the Serial Peripheral Interface (SPI) on Motorola single-chip microprocessors, is provided to communicate with external devices via a serial link. The SCP functions are multiplexed onto other serial pins so when the SCP is enabled, certain modem control features are lost. Please refer to the MC145488/D Data Book for complete details.

TIMERS

Two timers are provided for general purpose low-resolution protocol uses. The clock to the timer is derived from the Master MPU Clock (MCLK). The baud rate generator in the SCP block is used to drive the timer divide chain. This clock is then divided by 1024 and applied to an eight-bit down-counter. The counter is readable and writable by the host and may be set to any value. The counter counts down toward zero from the current value. A non-maskable interrupt is generated when the counter underflows from FF to FE. The timers continue counting down after reaching FE. The status bit from the previous interrupt must be cleared before a new interrupt is generated. The timer function and interrupt are enabled by setting the Timer Enable bit in the Timer register to one. The timer interrupt status bits must be read while set before they can be cleared. The timers are intended for low accuracy uses such as protocol timers. Figure 7 describes the clock selection choices for the timers.

Watchdog Timer

Timer 0 may be configured as a watchdog timer for the entire host system. When the Watchdog Enable bit is set, an extra divide by 16 is added to the clock input of the counter. When the counter underflows from FF to FE, the Reset pin becomes an output for 16 MCLK cycles and a logic low is output. This provides a system reset to the host. The host can write any value (except FE hex) to the Timer register to setup any timeout. Time-outs of up to 5.6 seconds are available with a 12 MHz MCLK.

POWER CONSUMPTION

The DDLC is designed utilizing high-performance CMOS technology. As as result, average power consumption is very low. However, because there are wide address and data buses, peak currents may exceed 150 mA for short periods of time (less than 20 ns) while the drivers are charging or discharging the buses.

REGISTER SET

The DDLC has many user accessible registers. These registers control the blocks or indicate status. Other registers, used by the DMA section, are used as buffer descriptors and counters. For a more detailed description, please refer to the DDLC data book. The address for each register is the hexadecimal offset from the base address of the chip select. The registers may be accessed as 8-bit registers or 16-bit registers. Table 1 is a map of the registers and their principal function.

00	SYSTEM CONTROL	
02	MASTER STATUS	
04	INTERRUPT ENABLE	
06	DATA BUS SIZE SELECT	
10	SCP REGISTER	
12	CH 0 TIMER	
14	CH 1 TIMER	
20	CHANNEL 0 SERIAL INTERFACE CONTROL	CHANNEL 0 REGISTERS
22	CHANNEL 0 Tx CONTROL	
24	CHANNEL 0 Rx CONTROL	
26	CHANNEL 0 Tx STATUS	
28	CHANNEL 0 Rx STATUS	
2A	CHANNEL 0 ADDRESS COMPARE	
2C	CHANNEL 0 ADDRESS WILDCARD BITS	
2E	CHANNEL 0 CRC ERROR COUNT	
30	CHANNEL 0 Tx FRAME LENGTH	
32	CHANNEL 0 Tx BASE ADDRESS	
34	CHANNEL 0 Tx BYTE COUNT	
36	CHANNEL 0 Rx BUFFER LENGTH	
38	CHANNEL 0 Rx BUFFER A BASE ADDRESS	
3A	CHANNEL 0 Rx BUFFER A BYTE COUNT	
3C	CHANNEL 0 Rx BUFFER B BASE ADDRESS	
3E	CHANNEL 0 Rx BUFFER B BYTE COUNT	
40	CHANNEL 1 SERIAL INTERFACE CONTROL	CHANNEL 1 REGISTERS
42	CHANNEL 1 Tx CONTROL	
44	CHANNEL 1 Rx CONTROL	
46	CHANNEL 1 Tx STATUS	
48	CHANNEL 1 Rx STATUS	
4A	CHANNEL 1 ADDRESS COMPARE	
4C	CHANNEL 1 ADDRESS WILDCARD BITS	
4E	CHANNEL 1 CRC ERROR COUNT	
50	CHANNEL 1 Tx FRAME LENGTH	
52	CHANNEL 1 Tx BASE ADDRESS	
54	CHANNEL 1 Tx BYTE COUNT	
56	CHANNEL 1 Rx BUFFER LENGTH	
58	CHANNEL 1 Rx BUFFER A BASE ADDRESS	
5A	CHANNEL 1 Rx BUFFER A BYTE COUNT	
5C	CHANNEL 1 Rx BUFFER B BASE ADDRESS	
5E	CHANNEL 1 Rx BUFFER B BYTE COUNT	

Table 1. Register Memory Map

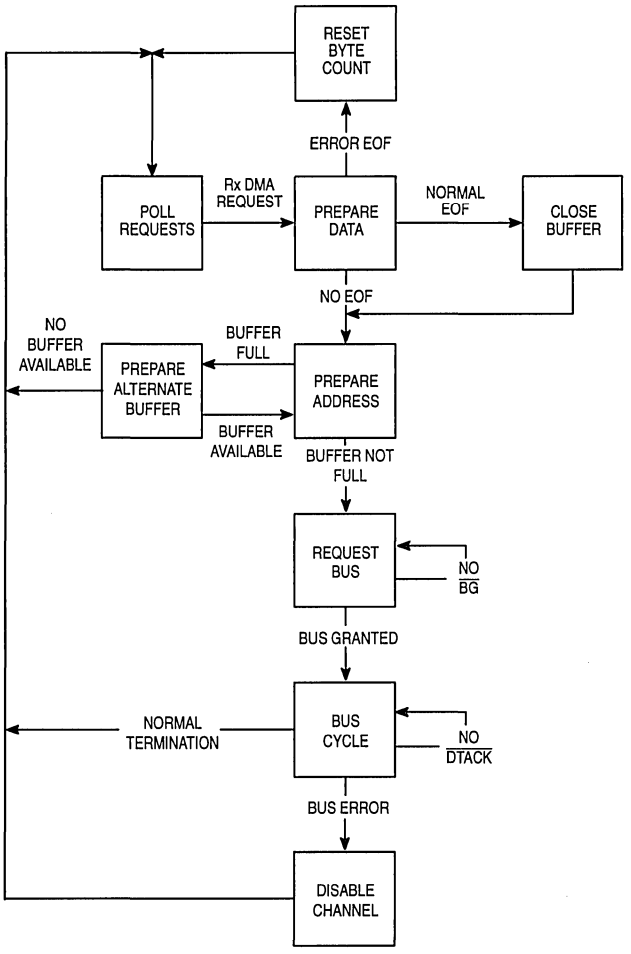


Figure 7. Receive DMA State Diagram

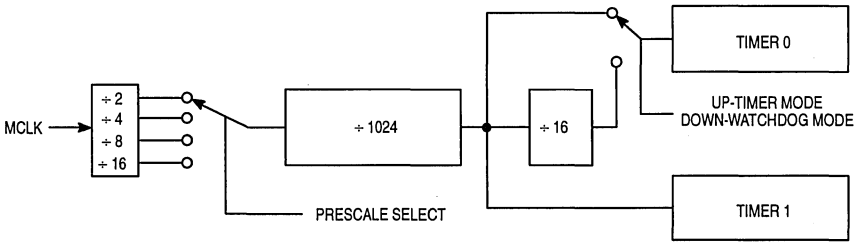


Figure 8. Timer Clock Selection

MC145500
MC145501
MC145502
MC145503
MC145505

Advance Information

PCM Codec-Filter Mono-Circuit

The MC145500, MC145501, MC145502, MC145503, and MC145505 are all per channel PCM codec-filter mono-circuits. These devices perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. The MC145500 and MC145503 are general purpose devices that are offered in a 16-pin package. They are designed to operate in both synchronous and asynchronous applications and contain an on chip precision reference voltage. The MC145501 is offered in an 18-pin package and adds the capability of selecting from three peak overload voltages (2.5, 3.15, and 3.78 V). The MC145505 is a synchronous device offered in a 16-pin DIP and wide body SOIC package intended for instrument use. The MC145502 is the full-featured device which presents all of the options of the chip. This device is packaged in a 22-pin DIP and a 28-pin chip carrier package and contains all the features of the MC145500 and MC145501 plus several more. Most of these features can be made available in a lower pin count package tailored to a specific user's application. Contact the factory for further details.

These devices are pin-for-pin replacements for Motorola's first generation of MC14400/01/02/03/05 PCM mono-circuits and upwardly compatible with the MC14404/06/07 codecs and other industry standard codecs. They also maintain compatibility with Motorola's family of MC33120 and MC3419 SLIC products.

The MC145500 family of PCM codec-filter mono-circuits utilizes CMOS due to its reliable low-power performance and proven capability for complex analog/digital VLSI functions.

MC145500

- 16-Pin Package
- Transmit Bandpass and Receive Low-Pass Filter on Chip
- Pin Selectable Mu/A Law Companding with Corresponding Data Format
- On Chip Precision Reference Voltage (3.15 V)
- Power Dissipation of 50 mW, Power Down of 0.1 mW at ± 5 V
- Automatic Prescaler Accepts 128 kHz, 1.536, 1.544, 2.048, and 2.56 MHz for Internal Sequencing

MC145501 — All of the Above Plus:

- 18-Pin Package
- Selectable Peak Overload Voltages (2.5, 3.15, 3.78 V)
- Access to the Inverting Input of the Txl Input Operational Amplifier

MC145502 — All of the Above Plus:

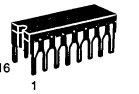
- 22-Pin and 28-Pin Packages
- Variable Data Clock Rates (64 kHz to 4.1 MHz)
- Complete Access to the Three Terminal Transmit Input Operational Amplifier
- An External Precision Reference May Be Used

MC145503 — All of the Above Features of the MC145500 Plus:

- 16-Pin Package
- Complete Access to the Three Terminal Transmit Input Operational Amplifier

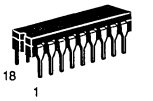
MC145505 — Same as MC145503 Except:

- 16-Pin Package
- Common 64 kHz to 4.1 MHz Transmit/Receive Data Clock

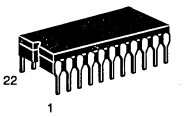


L SUFFIX
CERAMIC
CASE 620
MC145500/03/05

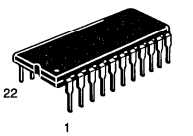
P SUFFIX
PLASTIC
CASE 648
MC145503/05



L SUFFIX
CERAMIC
CASE 726
MC145501

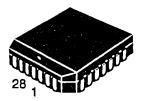


L SUFFIX
CERAMIC
CASE 736
MC145502



P SUFFIX
PLASTIC
CASE 708
MC145502

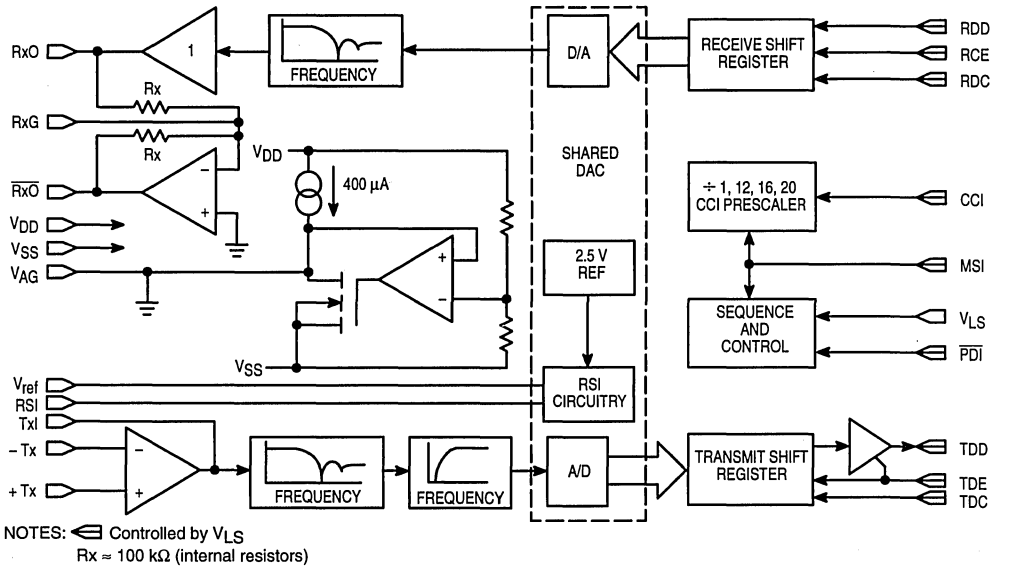
DW SUFFIX
SO
CASE 751G
MC145503/05



FN SUFFIX
PLCC
CASE 776
MC145502

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MC145500/01/02/03/05 PCM CODEC/FILTER MONO-CIRCUIT BLOCK DIAGRAM



PIN ASSIGNMENTS

(Drawings Do Not Reflect Relative Size)

MC145500L

V_{AG}	1	16	V_{DD}
RxO	2	15	RDD
$\overline{RxO}$	3	14	RCE
TxI	4	13	RDC
Mu/A	5	12	TDC
$\overline{PDI}$	6	11	TDD
V_{SS}	7	10	TDE
V_{LS}	8	9	MSI

MC145503L, P

V_{AG}	1	16	V_{DD}
RxO	2	15	RDD
+ Tx	3	14	RCE
TxI	4	13	RDC
– Tx	5	12	TDC
Mu/A	6	11	TDD
$\overline{PDI}$	7	10	TDE
V_{SS}	8	9	V_{LS}

MC145505L, P

V_{AG}	1	16	V_{DD}
RxO	2	15	RDD
+ Tx	3	14	RCE
TxI	4	13	DCLK
– Tx	5	12	CCI
Mu/A	6	11	TDD
$\overline{PDI}$	7	10	TDE
V_{SS}	8	9	V_{LS}

MC145501L

RSI	1	18	V_{DD}
V_{AG}	2	17	RDD
RxO	3	16	RCE
$\overline{RxO}$	4	15	RDC
TxI	5	14	TDC
– Tx	6	13	TDD
Mu/A	7	12	TDE
$\overline{PDI}$	8	11	MSI
V_{SS}	9	10	V_{LS}

MC145502L, P

V_{ref}	1	22	RSI
V_{AG}	2	21	V_{DD}
RxO	3	20	RDD
RxG	4	19	RCE
$\overline{RxO}$	5	18	RDC
+ Tx	6	17	TDC
TxI	7	16	CCI
– Tx	8	15	TDD
Mu/A	9	14	TDE
$\overline{PDI}$	10	13	MSI
V_{SS}	11	12	V_{LS}

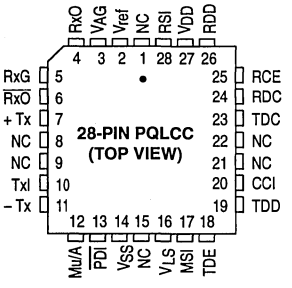
MC145503DW

V_{AG}	1	16	V_{DD}
RxO	2	15	RDD
+ Tx	3	14	RCE
TxI	4	13	RDC
– Tx	5	12	TDC
Mu/A	6	11	TDD
$\overline{PDI}$	7	10	TDE
V_{SS}	8	9	V_{LS}

MC145505DW

V_{AG}	1	16	V_{DD}
RxO	2	15	RDD
+ Tx	3	14	RCE
TxI	4	13	DCLK
– Tx	5	12	CCI
Mu/A	6	11	TDD
$\overline{PDI}$	7	10	TDE
V_{SS}	8	9	V_{LS}

MC145502FN



NC = NO CONNECTION

ABSOLUTE MAXIMUM RATINGS (Voltage Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	– 0.5 to 13	V
Voltage, Any Pin to V_{SS}	V	– 0.5 to V_{DD} + 0.5	V
DC Drain Per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., V_{SS}, V_{DD}, V_{LS}, or V_{AG}).

RECOMMENDED OPERATING CONDITIONS (T_A = – 40 to + 85°C)

Characteristic		Min	Typ	Max	Unit
DC Supply Voltage					V
Dual Supplies: V_{DD} = – V_{SS}, (V_{AG} = V_{LS} = 0 V)		4.75	5.0	6.3	
Single Supply: V_{DD} to V_{SS} (V_{AG} is an Output, V_{LS} = V_{DD} or V_{SS})					
MC145500, MC145501, MC145502, MC145503, MC145505 (Using Internal 3.15 V Reference)		8.5	—	12.6	
MC145501, MC145502 Using Internal 2.5 V Reference		7.0	—	12.6	
MC145501, MC145502 Using Internal 3.78 V Reference		9.5	—	12.6	
MC145502 Using External 1.5 V Reference, Referenced to V_{AG}		4.75	—	12.6	
Power Dissipation					mW
CMOS Logic Mode (V_{DD} to V_{SS} = 10 V, V_{LS} = V_{DD})		—	40	70	
TTL Logic Mode (V_{DD} = + 5 V, V_{SS} = – 5 V, V_{LS} = V_{AG} = 0 V)		—	50	90	
Power Down Dissipation		—	0.1	1.0	mW
Frame Rate Transmit and Receive		7.5	8.0	8.5	kHz
Data Rate		—	128	—	kHz
MC145500, MC145501, MC145503		—	1536	—	
Must Use One of These Frequencies, Relative to MSI Frequency of 8 kHz		—	1544	—	
		—	2048	—	
		—	2560	—	
Data Rate for MC145502, MC145505		64	—	4096	kHz
Full Scale Analog Input and Output Level					Vp
MC145500, MC145503, MC145505		—	3.15	—	
MC145501, MC145502 (V_{ref} = V_{SS})	RSI=V_{DD}	—	3.78	—	
	RSI=V_{SS}	—	3.15	—	
	RSI=V_{AG}	—	2.5	—	
MC145502 Using an External Reference Voltage Applied at V_{ref} Pin	RSI=V_{DD}	—	1.51 x V_{ref}	—	
	RSI=V_{SS}	—	1.26 x V_{ref}	—	
	RSI=V_{AG}	—	V_{ref}	—	

DIGITAL LEVELS (V_{SS} to V_{DD} = 4.75 V to 12.6 V, T_A = – 40 to + 85°C)

Characteristic		Symbol	Min	Max	Unit
Input Voltage Levels (TDE, TDC, RCE, RDC, RDD, DC, MSI, CCI, $\overline{PDI}$)					V
CMOS Mode (V_{LS} = V_{DD}, V_{SS} is Digital Ground)	"0"	V_{IL}	—	0.3 x V_{DD}	
	"1"	V_{IH}	0.7 x V_{DD}	—	
TTL Mode ($V_{LS} \le V_{DD}$ – 4.0 V, V_{LS} is Digital Ground)	"0"	V_{IL}	—	V_{LS} + 0.8 V	
	"1"	V_{IH}	V_{LS} + 2.0 V	—	
Output Current for TDD (Transmit Digital Data)					mA
CMOS Mode (V_{LS} = V_{DD}, V_{SS} = 0 V and is Digital Ground)					
(V_{DD} = 5 V, V_{out} = 0.4 V)		I_{OL}	1.0	—	
(V_{DD} = 10 V, V_{out} = 0.5 V)			3.0	—	
(V_{DD} = 5 V, V_{out} = 4.5 V)		I_{OH}	– 1.0	—	
(V_{DD} = 10 V, V_{out} = 9.5 V)			– 3.0	—	
TTL Mode ($V_{LS} \le V_{DD}$ – 4.75 V, V_{LS} = 0 V and is Digital Ground)	(V_{OL} = 0.4 V)	I_{OL}	1.6	—	
	(V_{OH} = 2.4 V)	I_{OH}	– 0.2	—	

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = + 5 V ± 5%, V_{SS} = −5 V ±5%, V_{LS} = V_{AG} = 0 V, V_{ref} = RSI = V_{SS} (Internal 3.15 V Reference), 0 dBm0 = 1.546 Vrms = + 6 dBm @ 600 Ω, T_A = − 40 to + 85°C, TDC = RDC = CC = 2.048 MHzI, TDE = RCE = MSI = 8 kHz, Unless Otherwise Noted)

Characteristic		End-to-End Min	End-to-End Max	A/D Min	A/D Max	D/A Min	D/A Max	Unit
Absolute Gain (0 dBm0 @ 1.02 kHz, T_A = 25°C, V_{DD} = 5 V, V_{SS} = −5 V)		—	—	− 0.30	+ 0.30	− 0.30	+ 0.30	dB
Absolute Gain Variation with Temperature 0 to + 70°C		—	—	—	± 0.03	—	± 0.03	dB
Absolute Gain Variation with Temperature − 40 to +85°C		—	—	—	± 0.1	—	± 0.1	dB
Absolute Gain Variation with Power Supply (V_{DD} = 5 V, V_{SS} = −5 V, 5%)		—	—	—	± 0.02	—	± 0.02	dB
Gain vs Level Tone (Relative to − 10 dBm0, 1.02 kHz)	+ 3 to − 40 dBm0	− 0.4	+ 0.4	− 0.2	+ 0.2	− 0.2	+ 0.2	dB
	− 40 to − 50 dBm0	− 0.8	+ 0.8	− 0.4	+ 0.4	− 0.4	+ 0.4	
	− 50 to − 55 dBm0	− 1.6	+ 1.6	− 0.8	+ 0.8	− 0.8	+ 0.8	
Gain vs Level Pseudo Noise (A-Law Relative to − 10 dBm0)								dB
CCITT G.714	− 10 to − 40 dBm0	—	—	− 0.25	+ 0.25	− 0.25	+ 0.25	
	− 40 to − 50 dBm0	—	—	− 0.30	+ 0.30	− 0.30	+ 0.30	
	− 50 to − 55 dBm0	—	—	− 0.45	+ 0.45	− 0.45	+ 0.45	
Total Distortion − 1.02 kHz Tone (C-Message)	0 to − 30 dBm0	35	—	36	—	36	—	dBC
	− 40 dBm0	29	—	29	—	30	—	
	− 45 dBm0	24	—	24	—	25	—	
Total Distortion With Pseudo Noise (A-Law)	− 3 dBm0	27.5	—	28	—	28.5	—	dB
CCITT G.714	− 6 to − 27 dBm0	35	—	35.5	—	36	—	
	− 34 dBm0	33.1	—	33.5	—	34.2	—	
	− 40 dBm0	28.2	—	28.5	—	30.0	—	
	− 55 dBm0	13.2	—	13.5	—	15.0	—	
Idle Channel Noise (For End-End and A/D, See Note 1)								
	Mu-Law, C-Message Weighted	—	15	—	15	—	9	dBrnC0
	A-Law, Psophometric Weighted	—	− 69	—	− 69	—	− 78	dBm0p
Frequency Response (Relative to 1.02 kHz @ 0 dBm0)	15 to 60 Hz	—	− 23	—	− 23	—	0.15	dB
	300 to 3000 Hz	− 0.3	+ 0.3	− 0.15	+ 0.15	− 0.15	+ 0.15	
	3400 Hz	− 1.6	0	− 0.8	0	− 0.8	0	
	4000 Hz	—	− 28	—	− 14	—	− 14	
	≥ 4600 Hz	—	− 60	—	− 32	—	− 30	
Inband Spurious (1.02 kHz @ 0 dBm0, Transmit and RxO)		—	—	—	− 43	—	− 43	dBm0
	300 to 3000 Hz							
Out-of-Band Spurious at RxO (300 − 3400 Hz @ 0 dBm0 In)								dB
	4600 to 7600 Hz	—	− 30	—	—	—	− 30	
	7600 to 8400 Hz	—	− 40	—	—	—	− 40	
	8400 to 100,000 Hz	—	− 30	—	—	—	− 30	
Idle Channel Noise Selective @ 8 kHz, Input = V_{AG}, 30 Hz Bandwidth		—	− 70	—	—	—	− 70	dBm0
Absolute Delay @ 1600 Hz (TDC = 2.048 MHz, TDE = 8 kHz)		—	—	—	310	—	180	µs
Group Delay Referenced to 1600 Hz (TDC = 2048 kHz,								µs
TDE = 8 kHz)	500 to 600 Hz	—	—	—	200	− 40	—	
	600 to 800 Hz	—	—	—	140	− 40	—	
	800 to 1000 Hz	—	—	—	70	− 30	—	
	1000 to 1600 Hz	—	—	—	40	− 20	—	
	1600 to 2600 Hz	—	—	—	75	—	90	
	2600 to 2800 Hz	—	—	—	110	—	120	
	2800 to 3000 Hz	—	—	—	170	—	160	
Crosstalk of 1020 Hz @ 0 dBm0 From A/D or D/A (Note 2)		—	—	—	− 75	—	− 80	dB
Intermodulation Distortion of Two Frequencies of Amplitudes − 4 to − 21 dBm0 from the Range 300 to 3400 Hz		—	—	—	− 41	—	− 41	dB

NOTES:

1. Extrapolated from a 1020 Hz @ − 50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while the A/D is stimulated with 2667 Hz @ − 50 dBm0.

ANALOG ELECTRICAL CHARACTERISTICS ($V_{DD} = -V_{SS} = 5$ V to 6 V ± 5%, $T_A = -40$ to +85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Current	+Tx, –Tx (TxI for MC145500)	I_{in}	—	± 0.01	± 0.2	µA
AC Input Impedance to V_{AG} (1 kHz)	+Tx, –Tx TxI for MC145500	Z_{in}	5 0.1	10 0.2	— —	MΩ
Input Capacitance	+Tx, –Tx		—	—	10	pF
Input Offset Voltage of TxI Op Amp			—	< ± 30	—	mV
Input Common Mode Voltage Range	+Tx, –Tx	V_{ICR}	V_{SS} + 1.0	—	V_{DD} – 2.0	V
Input Common Mode Rejection Ratio	+Tx, –Tx	CMRR	—	70	—	dB
TxI Unity Gain Bandwidth	$R_L \geq 10$ kΩ	BW_p	—	1000	—	kHz
TxI Open Loop Gain	$R_L \geq 10$ kΩ	A_{VOL}	—	75	—	dB
Equivalent Input Noise (C-Message) Between +Tx and –Tx, at TxI			—	– 20	—	dBrnC0
Output Load Capacitance for TxI Op Amp			0	—	100	pF
Output Voltage Range TxI Op Amp, RxO or $\overline{RxO}$ R_L = 10 kΩ to V_{AG} R_L = 600 Ω to V_{AG}		V_{out}	 V_{SS} + 0.8 V_{SS} + 1.5	 — —	 V_{DD} – 1.0 V_{DD} – 1.5	V
Output Current TxI, RxO, $\overline{RxO}$	$V_{SS} + 1.5\ V \leq V_{out} \leq V_{DD} - 1.5\ V$		± 5.5	—	—	mA
Output Impedance RxO, $\overline{RxO}$*	0 to 3.4 kHz	Z_{out}	—	3	—	Ω
Output Load Capacitance for RxO and $\overline{RxO}$*			0	—	200	pF
Output dc Offset Voltage Referenced to V_{AG} Pin	RxO $\overline{RxO}$*		— —	— —	± 100 ± 150	mV
Internal Gainsetting Resistors for RxG to RxO and $\overline{RxO}$			62	100	225	kΩ
External Reference Voltage Applied to V_{ref} (Referenced to V_{AG})			0.5	—	V_{DD} – 1.0	V
V_{ref} Input Current			—	—	20	µA
V_{AG} Output Bias Voltage			—	0.53 V_{DD} + 0.47 V_{SS}	—	V
V_{AG} Output Current	Source Sink	I_{VAG}	0.4 10.0	— —	0.8 —	mA
Output Leakage Current During Power Down for the TxI Op Amp, V_{AG}, RxO, and $\overline{RxO}$			—	—	± 30	µA
Positive Power Supply Rejection Ratio, 0–100 kHz @ 250 mV, C-Message Weighting	Transmit Receive		45 55	50 65	— —	dBC
Negative Power Supply Rejection Ratio, 0–100 kHz @ 250 mV, C-Message Weighting	Transmit Receive		50 50	55 60	— —	dBC

*Assumes that RxG is not connected for gain modifications to $\overline{RxO}$.

MODE CONTROL LOGIC (V_{SS} to V_{DD} = 4.75 V to 12.6 V, T_A = – 40 to + 85°C)

Characteristic	Min	Typ	Max	Unit
V_{LS} Voltage for TTL Mode (TTL Logic Levels Referenced to V_{LS})	V_{SS}	—	V_{DD} – 4.0	V
V_{LS} Voltage for CMOS Mode (CMOS Logic Levels of V_{SS} to V_{DD})	V_{DD} – 0.5	—	V_{DD}	V
Mu/A Select Voltage				V
Mu-Law Mode	V_{DD} – 0.5	—	V_{DD}	
Sign Magnitude Mode	V_{AG} – 0.5	—	V_{AG} + 0.5	
A-Law Mode	V_{SS}	—	V_{SS} + 0.5	
RSI Voltage for Reference Select Input (MC145501 and MC145502) 3.78 V Mode	V_{DD} – 0.5	—	V_{DD}	V
2.5 V Mode	V_{AG} – 0.5	—	V_{AG} + 0.5	
3.15 V Mode	V_{SS}	—	V_{SS} + 0.5	
V_{ref} Voltage for Internal or External Reference (MC145502 Only)				V
Internal Reference Mode	V_{SS}	—	V_{SS} + 0.5	
External Reference Mode	V_{AG} + 0.5	—	V_{DD} – 1.0	
Analog Test Mode Frequency, MS = CCI (MC145500, MC145501, MC145502 Only) See Pin Description; Test Modes	—	128	—	kHz

SWITCHING CHARACTERISTICS (V_{SS} to V_{DD} = 9.5 V to 12.6 V, T_A = – 40 to + 85°C, C_L = 150 pF, CMOS or TTL Mode)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Rise Time	TDD	t_{TLH}	—	30	80	ns
Output Fall Time		t_{THL}	—	30	80	
Input Rise Time	TDE, TDC, RCE, RDC, DC, MSI, CCI	t_{TLH}	—	—	4	µs
Input Fall Time		t_{THL}	—	—	4	
Pulse Width	TDE Low, TDC, RCE, RDC, DC, MSI, CCI	t_W	100	—	—	ns
DCLK Pulse Frequency (MC145502/05 ONLY)	TDC, RDC, DC	f_{CL}	64	—	4096	kHz
CCI Clock Pulse Frequency (MSI = 8 kHz)		f_{CL1}	—	128	—	kHz
CCI is internally tied to TDC on the MC145500/01/03, therefore, the		f_{CL2}	—	1536	—	
transmit data clock must be one of these frequencies. This pin will ac-		f_{CL3}	—	1544	—	
cept one of these discrete clock frequencies and will		f_{CL4}	—	2048	—	
compensate to produce internal sequencing.		f_{CL5}	—	2560	—	
Propagation Delay Time						ns
TDE Rising to TDD Low Impedance	TTL	t_{P1}	—	90	180	
	CMOS		—	90	150	
TDE Falling to TDD High Impedance	TTL	t_{P2}	—	—	55	
	CMOS		—	—	40	
TDC Rising Edge to TDD Data, During TDE High	TTL	t_{P3}	—	90	180	
	CMOS		—	90	150	
TDE Rising Edge to TDD Data, During TDC High	TTL	t_{P4}	—	90	180	
	CMOS		—	90	150	
TDC Falling Edge to TDE Rising Edge Setup Time		t_{su1}	20	—	—	ns
TDE Rising Edge to TDC Falling Edge Setup Time		t_{su2}	100	—	—	ns
TDE Falling Edge to TDC Rising Edge to Preserve the Next TDD Data		t_{su8}	20	—	—	ns
RDC Falling Edge to RCE Rising Edge Setup Time		t_{su3}	20	—	—	ns
RCE Rising Edge to RDC Falling Edge Setup Time		t_{su4}	100	—	—	ns
RDD Valid to RDC Falling Edge Setup Time		t_{su5}	60	—	—	ns
CCI Falling Edge to MSI Rising Edge Setup Time		t_{su6}	20	—	—	ns
MSI Rising Edge to CCI Falling Edge Setup Time		t_{su7}	100	—	—	ns
RDD Hold Time from RDC Falling Edge		t_h	100	—	—	ns
TDE, TDC, RCE, RDC, RDD, DC, MSI, CCI Input Capacitance			—	—	10	pF
TDE,TDC, RCE, RDC, RDD, DC, MSI, CCI Input Current			—	± 0.01	± 10	µA
TDD Capacitance During High Impedance (TDE Low)			—	12	15	pF
TDD Input Current During High Impedance (TDE Low)			—	± 0.1	± 10.0	µA

DEVICE DESCRIPTIONS

A codec-filter is a device which is used for digitizing and reconstructing the human voice. These devices were developed primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from "Coder" for the A/D used to digitize voice, and "Decoder" for the D/A used for reconstructing voice. A codec is a single device that does both the A/D and D/A conversions.

To digitize intelligible voice requires a signal to distortion of about 30 dB for a dynamic range of about 40 dB. This may be accomplished with a linear 13-bit A/D and D/A, but will far exceed the required signal to distortion at amplitudes greater than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Two methods of data reduction are implemented by compressing the 13-bit linear scheme to companded 8-bit schemes. These companding schemes follow a segmented or "piecewise-linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all 16 of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits which increment. With the chord bits incremented, the step bits double their voltage weighting. This results in an effective resolution of 6-bits (sign + chord + four step bits) across a 42 dB dynamic range (7 chords above zero, by 6 dB per chord). There are two companding schemes used; Mu-255 Law specifically in North America, and A-Law specifically in Europe. These companding schemes are accepted world wide. The tables show the linear quantization levels to PCM words for the two companding schemes.

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low-pass filter to limit the high frequency energy above 3 kHz from distorting the inband signal. The telephone line is also subject to 50/60 Hz power line coupling which must be attenuated from the signal by a high-pass filter before the A/D converter.

The D/A process reconstructs a staircase version of the desired inband signal which has spectral images of the inband signal modulated about the sample frequency and its harmonics. These spectral images are called aliasing components which need to be attenuated to obtain the desired signal. The low-pass filter used to attenuate filter aliasing components is typically called a reconstruction or smoothing filter.

The MC145500 series PCM codec-filters have the codec, both presampling and reconstruction filters, a precision voltage reference on chip, and require no external components. There are five distinct versions of the Motorola MC145500 Series.

MC145500

The MC145500 PCM codec-filter is intended for standard byte interleaved synchronous and asynchronous applications. The TDC pin on this device is the input to both the TDC and CCI functions in the pin description. Consequently, for MSI = 8 kHz, TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty cycle) 1.536, 1.544, 2.048, or 2.56 MHz. (For other data clock frequencies see MC145502 or MC145505.) The internal reference is set for 3.15 V peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 V peak-to-peak. This is the + 3 dBm0 level of the PCM codec-filter. All other functions are described in the pin description.

MC145501

The MC145501 PCM codec-filter offers the same features and is for the same application as the MC145500, but offers two additional pins and features. The reference select input allows the full scale level of the device to be set at 2.5 Vp, 3.15 Vp, or 3.78 Vp. The –Tx pin allows for external transmit gain adjust and simplifies the interface to the MC3419 SLIC. Otherwise, it is identical to MC145500.

MC145502

The MC145502 PCM codec-filter is the full feature 22-pin device. It is intended for use in applications requiring maximum flexibility. The MC145502 contains all the features of the MC145500 and MC145501. The MC145502 is intended for bit interleaved or byte interleaved applications with data clock frequencies which are nonstandard or time varying. One of the five standard frequencies (listed above) is applied to the CCI input, and the data clock inputs can be any frequency between 64 kHz and 4.096 MHz. The V_{ref} pin allows for use of an external shared reference or selection of the internal reference. The RxG pin accommodates gain adjustments for the inverted analog output. All three pins of the input gain-setting operational amplifier are present, providing maximum flexibility for the analog interface.

MC145503

The MC145503 PCM codec-filter is intended for standard byte interleaved synchronous or asynchronous applications. TDC can be one of five discrete frequencies. These are 128 kHz (40 to 60% duty cycle), 1.536, 1.544, 2.048, or 2.56 MHz. (For other data clock frequencies see MC145502 or MC145505.) The internal reference is set for 3.15 V peak full scale, and the full scale input level at TxI and output level at RxO is 6.3 V peak-to-peak. This is the + 3 dBm0 level of the PCM codec-filter. The +Tx and –Tx inputs provide maximum flexibility for analog interface. All other functions are described in the pin description.

MC145505

The MC145505 PCM codec-filter is intended for byte interleaved synchronous applications. The MC145505 has all the features of the MC145503 but internally connects TDC and RDC (see pin description) to the DC pin. One of the five standard frequencies (listed above) should be applied to CCI. The data clock input (DC) can be any frequency between 64 kHz and 4.096 MHz.

PIN DESCRIPTIONS

DIGITAL

V_{LS}

Logic Level Select Input and TTL Digital Ground

V_{LS} controls the logic levels and digital ground reference for all digital inputs and the digital output. These devices can operate with logic levels from full supply (V_{SS} to V_{DD}) or with TTL logic levels using V_{LS} as digital ground. For V_{LS} = V_{DD}, all I/O is full supply (V_{SS} to V_{DD} swing) with CMOS switch points. For V_{SS} < V_{LS} < (V_{DD} – 4 V), all inputs and outputs are TTL compatible with V_{LS} being the digital ground.

The pins controlled by V_{LS} are inputs MSI, CCI, TDE, TDC, RCE, RDC, RDD, $\overline{PDI}$, and output TDD.

MSI
Master Synchronization Input

MSI is used for determining the sample rate of the transmit side and as a time base for selecting the internal prescale divider for the convert clock input (CCI) pin. The MSI pin should be tied to an 8 kHz clock which may be a frame sync or system sync signal. MSI has no relation to transmit or receive data timing, except for determining the internal transmit strobe as described under the TDE pin description. MSI should be derived from the transmit timing in asynchronous applications. In many applications MSI can be tied to TDE. (MSI is tied internally to TDE in MC145503/05.)

CCI
Convert Clock Input

CCI is designed to accept five discrete clock frequencies. These are 128 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 2.56 MHz. The frequency at this input is compared with MSI and prescale divided to produce the internal sequencing clock at 128 kHz (or 16 times the sampling rate). The duty cycle of CCI is dictated by the minimum pulse width except for 128 kHz, which is used directly for internal sequencing and must have a 40 to 60% duty cycle. In asynchronous applications, CCI should be derived from transmit timing. (CCI is tied internally to TDC in MC145500/01/03.)

TDC
Transmit Data Clock Input

TDC can be any frequency from 64 kHz to 4.096 MHz, and is often tied to CCI if the data rate is equal to one of the five discrete frequencies. This clock is the shift clock for the transmit shift register and its rising edges produce successive data bits at TDD. TDE should be derived from this clock. (TDC and RDC are tied together internally in the MC145505 and are called DC.) CCI is internally tied to TDC on the MC145500/01/03. Therefore, TDC must satisfy CCI timing requirements also.

TDE
Transmit Data Enable Input

TDE serves three major functions. The first TDE rising edge following an MSI rising edge generates the internal transmit strobe which initiates an A/D conversion. The internal transmit strobe also transfers a new PCM data word into the transmit shift register (sign bit first) ready to be output at TDD. The TDE pin is the high impedance control for the transmit digital data (TDD) output. As long as this pin is high, the TDD output stays low impedance. This pin also enables the output shift register for clocking out the 8-bit serial PCM word. The logical AND of the TDE pin with the TDC pin clocks out a new data bit at TDD. TDE should be held high for eight consecutive TDC cycles to clock out a complete PCM word for byte interleaved applications. The transmit shift register feeds back on itself to allow multiple reads of the transmit data . If the PCM word is clocked out once per frame in a byte interleaved system, the MSI pin function is transparent and may be connected to TDE.

The TDE pin may be cycled during a PCM word for bit interleaved applications. TDE controls both the high impedance state of the TDD output and the internal shift clock. TDE must fall before TDC rises (t_{su8}) to ensure integrity of the next data bit. There must be at least two TDC falling edges between the last TDE rising edge of one frame and the first TDE rising edge of the next frame. MSI must be available separate from TDE for bit interleaved applications.

TDD
Transmit Digital Data Output

The output levels at this pin are controlled by the V_{LS} pin. For V_{LS} connected to V_{DD}, the output levels are from V_{SS} to V_{DD}. For a voltage of V_{LS} between V_{DD} – 4 V and V_{SS}, the output levels are TTL compatible with V_{LS} being the digital ground supply. The TDD pin is a three-state output controlled by the TDE pin. The timing of this pin is controlled by TDC and TDE. When in TTL mode, this output may be made high-speed CMOS compatible using a pull-up resistor. The data format (Mu-Law, A-Law, or sign magnitude) is controlled by the Mu/A pin.

RDC
Receive Data Clock Input

RDC can be any frequency from 64 kHz to 4.096 MHz. This pin is often tied to the TDC pin for applications that can use a common clock for both transmit and receive data transfers. The receive shift register is controlled by the receive clock enable (RCE) pin to clock data into the receive digital data (RDD) pin on falling RDC edges. These three signals can be asynchronous with all other digital pins. The RDC input is internally tied to the TDC input on the MC145505 and called DC.

RCE
Receive Clock Enable Input

The rising edge of RCE should identify the sign bit of a receive PCM word on RDD. The next falling edge of RDC, after a rising RCE, loads the first bit of the PCM word into the receive register. The next seven falling edges enter the remainder of the PCM word. On the ninth rising edge, the receive PCM word is transferred to the receive buffer register and the A/D sequence is interrupted to commence the decode process. In asynchronous applications with an 8 kHz transmit sample rate, the receive sample rate should be between 7.5 and 8.5 kHz. Two receive PCM words may be decoded and analog summed each transmit frame to allow on chip conferencing. The two PCM words should be clocked in as two single PCM words, a minimum of 31.25 µs apart, with a receive data clock of 512 kHz or faster.

RDD
Receive Digital Data Input

RDD is the receive digital data input. The timing for this pin is controlled by RDC and RCE. The data format is determined by the Mu/A pin.

Mu/A
Select

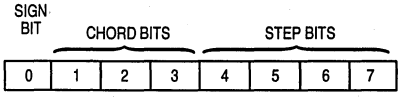
This pin selects the companding law and the data format at TDD and RDD.

Mu/A = V_{DD}; Mu255 Companding D3 Data Format with Zero Code Suppress

Mu/A = V_{AG}; Mu255 Companding with Sign Magnitude Data Format

Mu/A = V_{SS}; A-law Companding with CCITT Data Format Bit Inversions

CODE	SIGN/ MAGNITUDE	Mu-LAW	A-LAW (CCITT)
+ FULL SCALE	1111 1111	1000 0000	1010 1010
+ ZERO	1000 0000	1111 1111	1101 0101
– ZERO	0000 0000	0111 1111	0101 0101
– FULL SCALE	0111 1111	0000 0010	0010 1010



NOTE: Starting from sign magnitude, to change format:
To Mu-Law —
MSB is unchanged (sign)
Invert remaining seven bits
If code is 0000 0000, change to 0000 0010 (for zero code suppression)
To A-Law —
MSB is unchanged (sign)
Invert odd numbered bits
Ignore zero code suppression

$\overline{PDI}$
Power Down Input

The power down input disables the bias circuitry and gates off all clock inputs. This puts the V_{AG}, TxI, RxO, $\overline{RxO}$, and TDD outputs into a high-impedance state. The power dissipation is reduced to 0.1 mW when $\overline{PDI}$ is a low logic level. The circuit operates normally with $\overline{PDI}$ = V_{DD} or with a logic high as defined by connection at V_{LS}. TDD will not come out of high impedance for two MSI cycles after $\overline{PDI}$ goes high.

DCLK
Data Clock Input

In the MC145505, TDC and RDC are internally connected to DCLK.

ANALOG

V_{AG}
Analog Ground input/Output Pin

V_{AG} is the analog ground power supply input/output. All analog signals into and out of the device use this as their ground reference. Each version of the MC145500 PCM codec-filter family can provide its own analog ground supply internally. The dc voltage of this internal supply is 6% positive of the midway between V_{DD} and V_{SS}. This supply can sink more than 8 mA but has a current source limited to 400 µA. The output of this supply is internally connected to the analog ground input of the part. The node where this supply and the analog ground are connected is brought out to the V_{AG} pin. In symmetric dual supply systems (±5, ±6, etc.), V_{AG} may be externally tied to the system analog ground supply. When RxO or $\overline{RxO}$ drive low impedance loads tied to V_{AG}, a pull-up resistor to V_{DD} will be required to boost the source current capability if V_{AG} is not tied to the supply ground. All analog signals for the part are referenced to V_{AG}, including noise; therefore, decoupling capacitors (0.1 µF) should be used from V_{DD} to V_{AG} and V_{SS} to V_{AG}.

V_{ref}
Positive Voltage Reference Input (MC145502 Only)

The V_{ref} pin allows an external reference voltage to be used for the A/D and D/A conversions. If V_{ref} is tied to V_{SS}, the internal reference is selected. If V_{ref} > V_{AG}, then the external mode is selected and the voltage applied to V_{ref} is used for generating the internal converter reference voltage. In either internal or external reference mode, the actual voltage used for conversion is multiplied by the ratio selected by the RSI pin. The RSI pin circuitry is explained under its pin description below. Both the internal and external references are inverted within the PCM codec-filter for negative input voltages such that only one reference is required.

External Mode — In the external reference mode (V_{ref} > V_{AG}), a 2.5 V reference like the MC1403 may be connected from V_{ref} to V_{AG}. A single external reference may be shared by tying together a number of V_{ref} pins and V_{AG} pins from different codec-filters. In special applications, the external reference voltage may be between 0.5 and 5 V. However, the reference voltage gain selection circuitry associated with RSI must be considered to arrive at the desired codec-filter gain.

Internal Mode — In the internal reference mode (V_{ref} = V_{SS}), an internal 2.5 V reference supplies the reference voltage for the RSI circuitry. The V_{ref} pin is functionally connected to V_{SS} for the MC145500, MC145501, MC145503, and MC145505 pinouts.

RSI
Reference Select Input (MC145501/02 Only)

The RSI input allows the selection of three different overload or full scale A/D and D/A converter reference voltages independent of the internal or external reference mode. The RSI pin is a digital input that senses three different logic states: V_{SS}, V_{AG}, and V_{DD}. For RSI = V_{AG}, the reference voltage is used directly for the converters. The internal reference is 2.5 V. For RSI = V_{SS}, the reference voltage is multiplied by the ratio of 1.26, which results in an internal converter reference of 3.15 V. For RSI = V_{DD}, the reference voltage is multiplied by 1.51, which results in an internal converter reference of 3.78 V. The device requires a minimum of 1.0 V of headroom between the internal converter reference to V_{DD}. V_{SS} has this same absolute valued minimum, also measured from V_{AG} pin. The various modes of operation are summarized in Table 2. The RSI pin is functionally connected to V_{SS} for the MC145500, MC145503, and MC145505 pinouts.

RxO, $\overline{RxO}$
Receive Analog Outputs

These two complimentary outputs are generated from the output of the receive filter. They are equal in magnitude and out of phase. The maximum signal output of each is equal to the maximum peak-to-peak signal described with the reference. If a 3.15 V reference is used with RSI tied to V_{AG} and a + 3 dBm0 sine wave is decoded, the RxO output will be a 6.3 V peak-to-peak signal. $\overline{RxO}$ will also have an inverted signal output of 6.3 V peak-to-peak. External loads may be connected from RxO to $\overline{RxO}$ for a 6 dB push-pull signal gain or from either RxO or $\overline{RxO}$ to V_{AG}. With a 3.15 V reference each output will drive 600 Ω to + 9 dBm. With RSI tied to V_{DD}, each output will drive 900 Ω to + 9 dBm.

RxG
Receive Output Gain Adjust (MC145502 Only)

The purpose of the RxG pin is to allow external gain adjustment for the $\overline{RxO}$ pin. If RxG is left open, then the output signal at RxO will be inverted and output at $\overline{RxO}$. Thus the push-pull gain to a load from RxO to $\overline{RxO}$ is two times the output level at RxO. If external resistors are applied from RxO to RxG (RI) and from RxG to $\overline{RxO}$ (RG), the gain of $\overline{RxO}$ can be set differently from inverting unity. These resistors should be in the range of 10 kΩ. The RxO output level is unchanged by the resistors and the $\overline{RxO}$ gain is approximately equal to minus RG/RI. The actual gain is determined by taking into account the internal resistors which will be in parallel to these external resistors. The internal resistors have a large tolerance, but they match each other very closely. This

matching tends to minimize the effects of their tolerance on external gain configurations. The circuit for RxG and $\overline{RxO}$ is shown in the block diagram.

TxI
Transmit Analog Input

TxI is the input to the transmit filter. It is also the output of the transmit gain amplifiers of the MC145501/02/03/05. The input impedance is greater than 100 kΩ to V_{AG} in the MC145500. The TxI input has an internal gain of 1.0, such that a +3 dBm0 signal at TxI corresponds to the peak converter reference voltage as described in the V_{ref} and RSI pin descriptions. For 3.15 V reference, the +3 dBm0 input should be 6.3 V peak-to-peak.

+Tx / –Tx
Positive Tx Amplifier Input (MC145502/03/05 Only) / Negative Tx Amplifier Input (MC145501/02/03/05 Only)

The TxI pin is the input to the transmit band-pass filter. If +Tx or –Tx is available, then there is an internal amplifier preceding the filter whose pins are +Tx, –Tx, and TxI. These pins allow access to the amplifier terminals to tailor the input gain with external resistors. The resistors should be in the range of 10 kΩ. If +Tx is not available, it is internally tied to V_{AG}. If –Tx and +Tx are not available, the TxI is a unity gain high-impedance input.

POWER SUPPLIES

V_{DD}
Most Positive Power Supply

V_{DD} is typically 5 to 12 V.

V_{SS}
Most Negative Power Supply

V_{SS} is typically 10 to 12 V negative of V_{DD}.

For a ±5 V dual-supply system, the typical power supply configuration is V_{DD} = + 5 V, V_{SS} = – 5 V, V_{LS} = 0 V (digital ground accommodating TTL logic levels), and V_{AG} = 0 V being tied to system analog ground.

For single-supply applications, typical power supply configurations include:

V_{DD} = 10 V to 12 V
V_{SS} = 0 V

V_{AG} generates a mid supply voltage for referencing all analog signals.

V_{LS} controls the logic levels. This pin should be connected to V_{DD} for CMOS logic levels from V_{SS} to V_{DD}. This pin should be connected to digital ground for true TTL logic levels referenced to V_{LS}.

TESTING CONSIDERATIONS (MC145500/01/02 ONLY)

An analog test mode is activated by connecting MSI and CCI to 128 kHz. In this mode, the input of the A/D (the output of the Tx filter) is available at the $\overline{PDI}$ pin. This input is direct coupled to the A/D side of the codec. The A/D is a differential design. This results in the gain of this input being effectively attenuated by half. If monitored with a high-impedance buffer, the output of the Tx low-pass filter can also be measured at the $\overline{PDI}$ pin. This test mode allows independent evaluation of the transmit low-pass filter and A/D side of the codec. The transmit and receive channels of these devices are tested with the codec-filter fully functional.

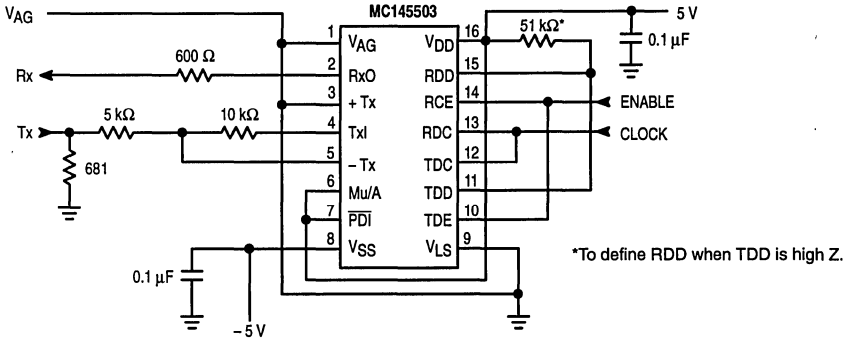


Figure 1. Test Circuit

Table 1. Options Available by Pin Selection

RSI* Pin Level	V_{ref}* Pin Level	Peak-to-Peak Overload Voltage (TxI, RxO)
V_{DD}	V_{SS}	7.56 Vpp
V_{DD}	V_{AG} + V_{EXT}	(3.02 x V_{EXT}) Vpp
V_{AG}	V_{SS}	5 Vpp
V_{AG}	V_{AG} + V_{EXT}	(2 x V_{EXT}) Vpp
V_{SS}	V_{SS}	6.3 Vpp
V_{SS}	V_{AG} + V_{EXT}	(2.52 x V_{EXT}) Vpp

*On MC145500/03/05, RSI and V_{ref} tied internally to V_{SS}. On MC145501, V_{ref} tied internally to V_{SS}.

Table 2. Summary of Operation Conditions User Programmed Through Pins V_{DD}, V_{AG}, and V_{SS}

Pin Programmed / Logic Level	Mu/A	RSI Peak Overload Voltage	V_{LS}
V_{DD}	Mu-Law Companding Curve and D3/D4 Digital Formats with Zero Code Suppress	3.78	CMOS Logic Levels
V_{AG}	Mu-Law Companding Curve and Sign Magnitude Data Format	2.50	TTL Levels V_{AG} Up
V_{SS}	A-Law Companding Curve and CCITT Digital Format	3.15	TTL Levels V_{SS} Up

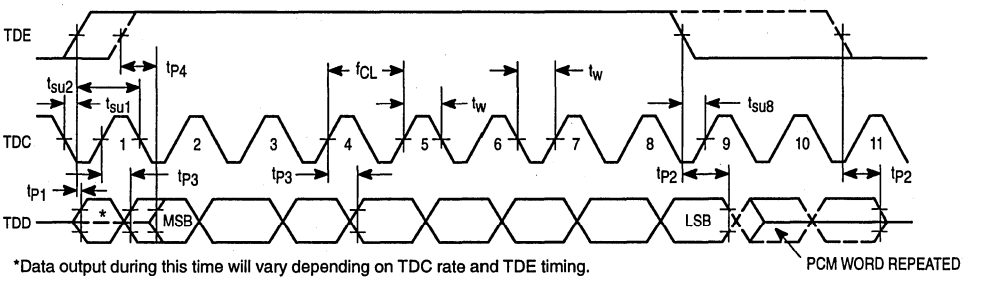


Figure 2. Transmit Timing Diagram

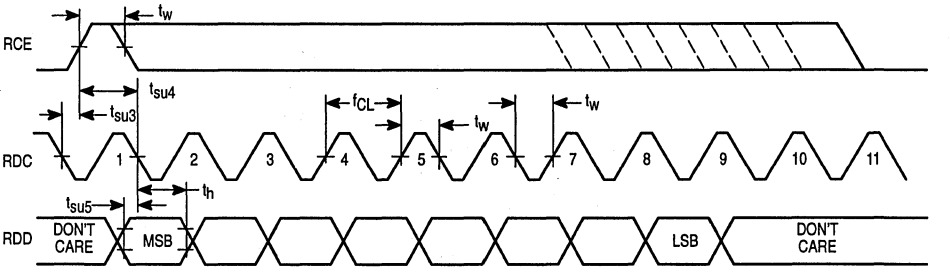


Figure 3. Receive Timing Diagram

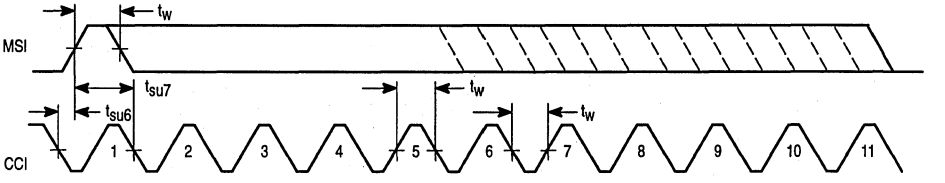


Figure 4. MSI/CCI Timing Diagram

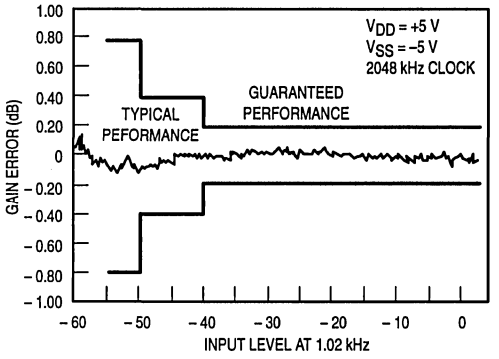


Figure 5. MC145502 Gain vs Level Mu-Law Transmit

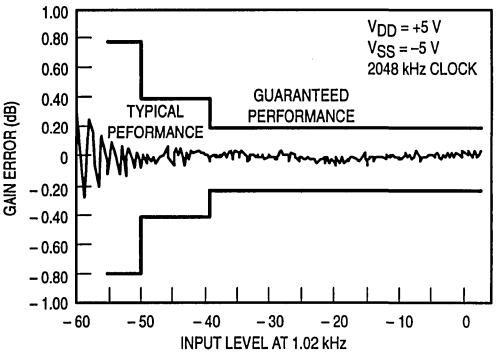


Figure 6. MC145502 Gain vs Level Mu-Law Receive

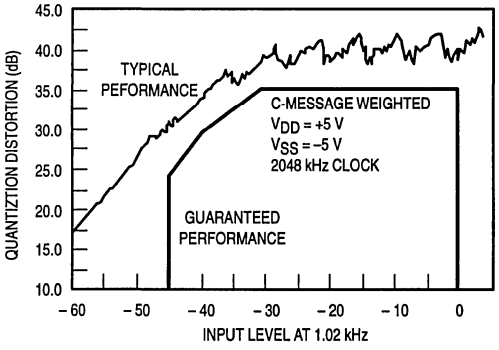


Figure 7. MC145502 Quantization Distortion Mu-Law Transmit

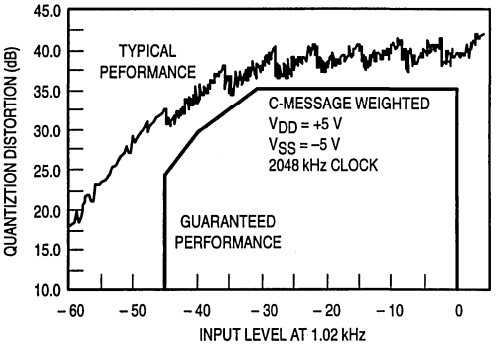


Figure 8. MC145502 Quantization Distortion Mu-Law Receive

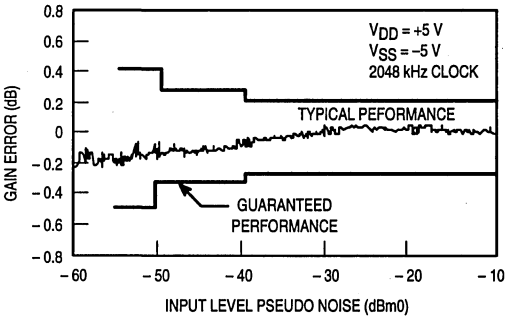


Figure 9. MC145502 Gain vs Level A-Law Transmit

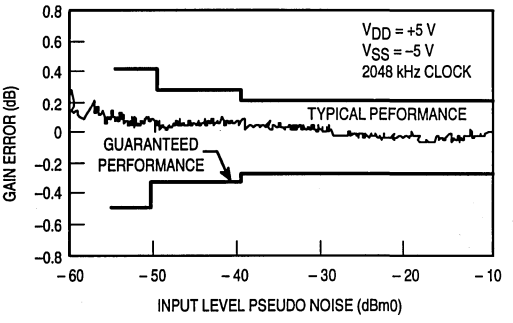


Figure 10. MC145502 Gain vs Level A-Law Receive

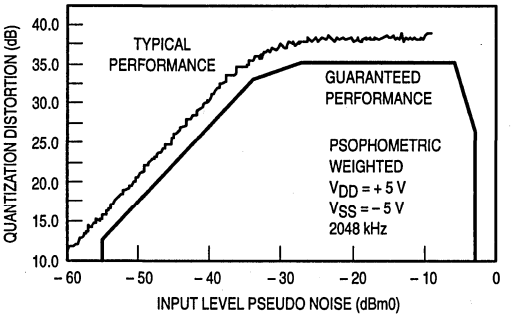


Figure 11. MC145502 Quantization Distortion A-Law Transmit

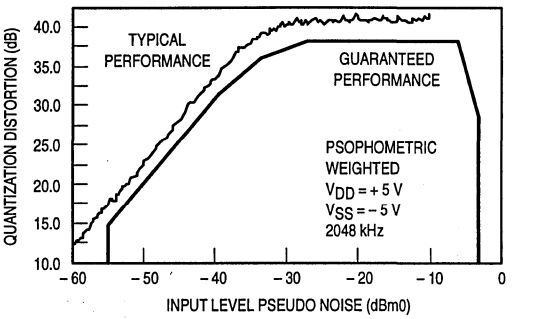


Figure 12. MC145502 Quantization Distortion A-Law Receive

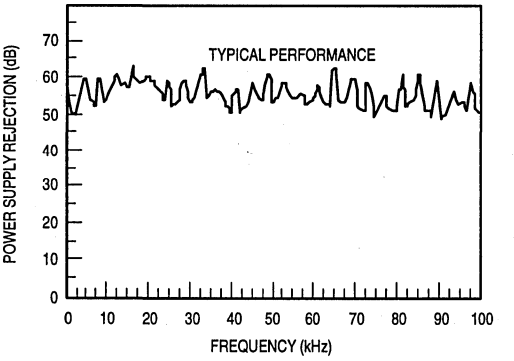


Figure 13. MC145502 Power Supply Rejection Ratio Positive Transmit VAC = 250 mVrms, C-Message Weighted

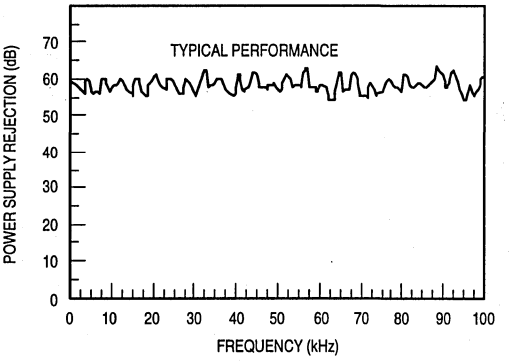


Figure 14. MC145502 Power Supply Rejection Ratio Negative Transmit VAC = 250 mVrms, C-Message Weighted

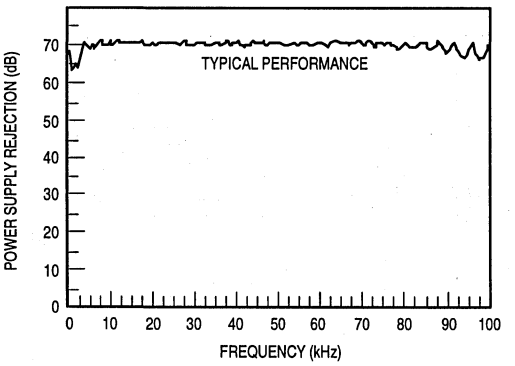


Figure 15. MC145502 Power Supply Rejection Ratio Positive Receive VAC = 250 mVrms, C-Message Weighted

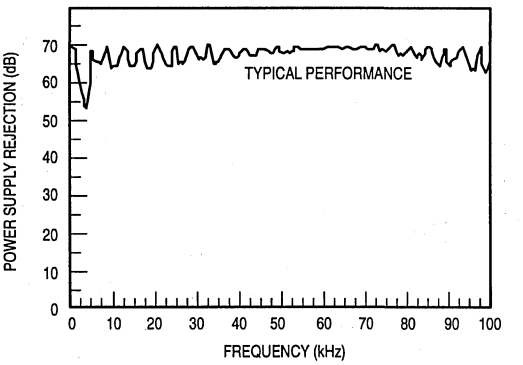


Figure 16. MC145502 Power Supply Rejection Ratio Negative Receive VAC = 250 mVrms, C-Message Weighted

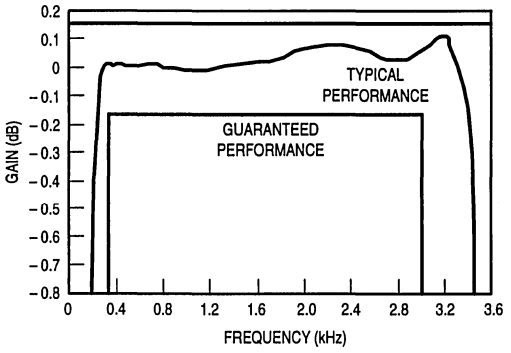


Figure 17. MC145502 Pass-Band Filter Response Transmit

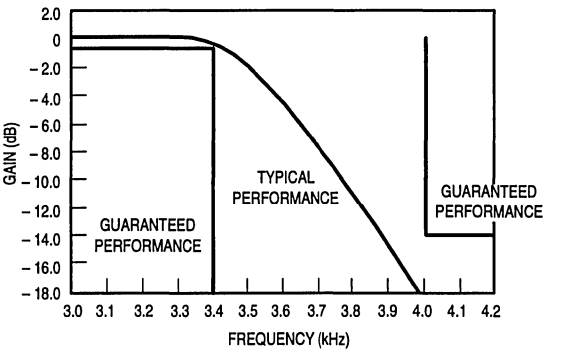


Figure 18. MC145502 Low-Pass Filter Response Transmit

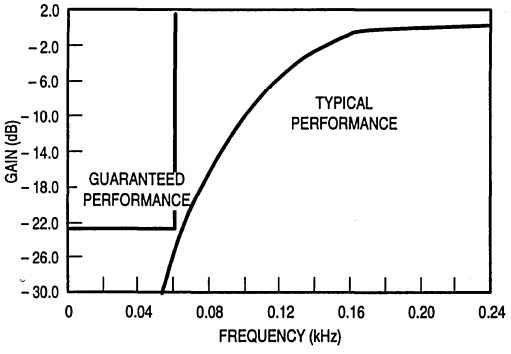


Figure 19. MC145502 High-Pass Filter Response Transmit

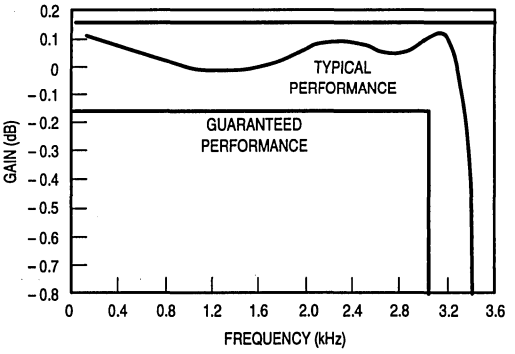


Figure 20. MC145502 Pass-Band Filter Response Receive

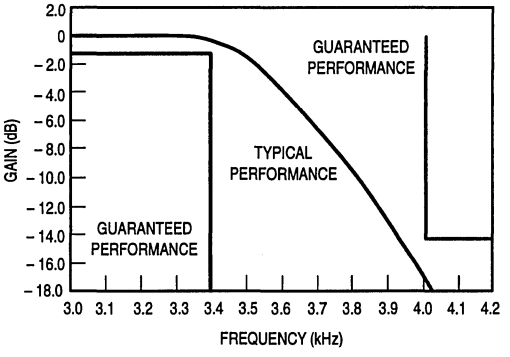


Figure 21. MC145502 Low-Pass Filter Response Receive

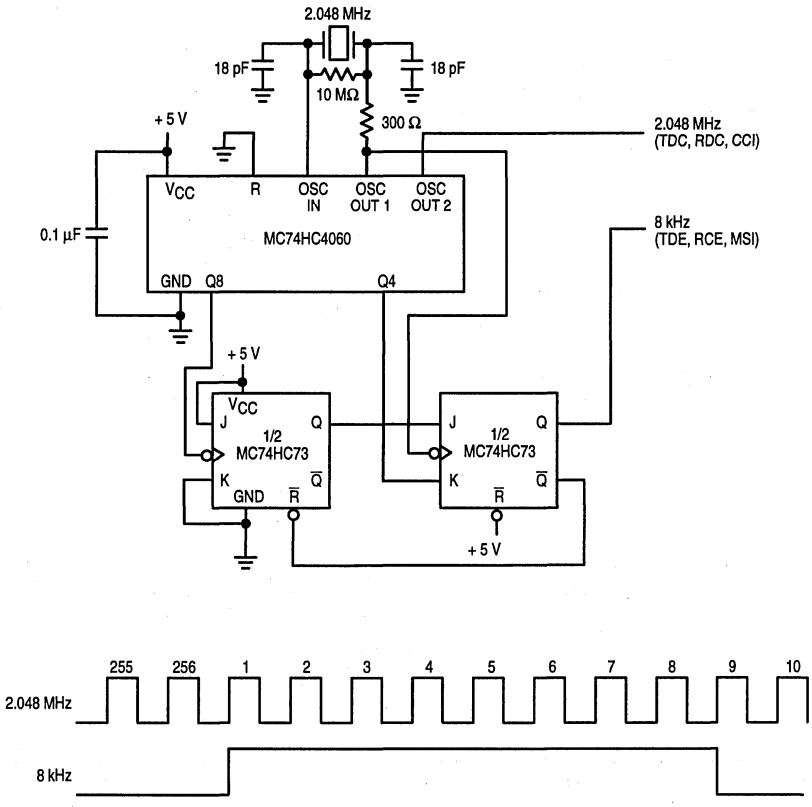
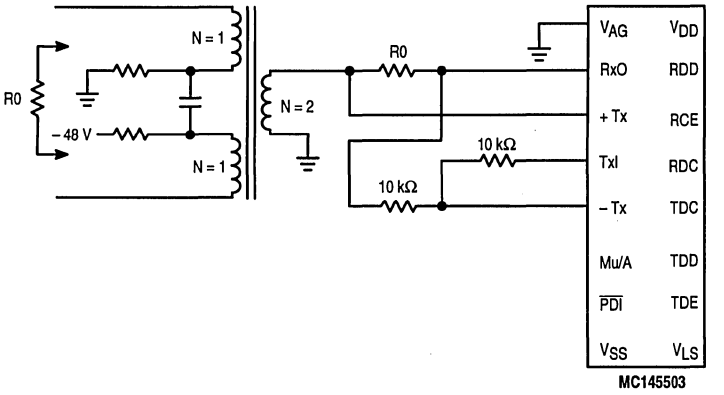
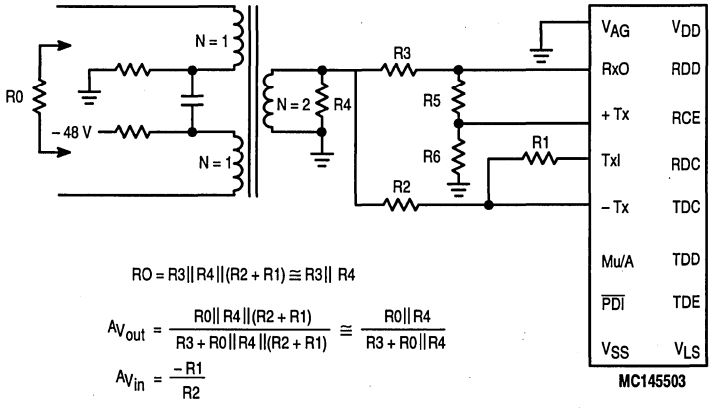


Figure 22. Simple Clock Circuit for Driving MC145500/01/02/03/05 Codec-Filters



23A. Simplified Transformer Hybrid Using MC145503



$$RO = R3 \| R4 \| (R2 + R1) \cong R3 \| R4$$

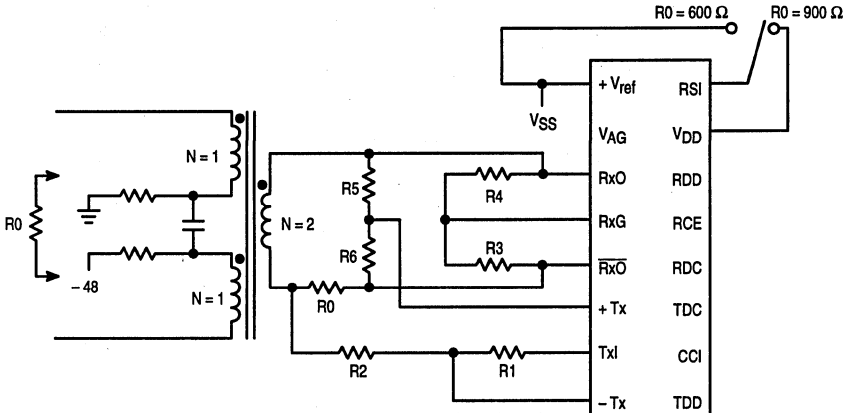
$$Av_{out} = \frac{R0 \| R4 \| (R2 + R1)}{R3 + R0 \| R4 \| (R2 + R1)} \cong \frac{R0 \| R4}{R3 + R0 \| R4}$$

$$Av_{in} = \frac{-R1}{R2}$$

NOTE: Hybrid Balance by R5 and R6 to equate the RxO signal gain at TxI through the inverting and non-inverting signal paths.

23b. Universal Transformer Hybrid Using MC145503

Figure 23. Hybrid Interfaces to the MC145503 PCM Codec-Filter Mono-Circuit

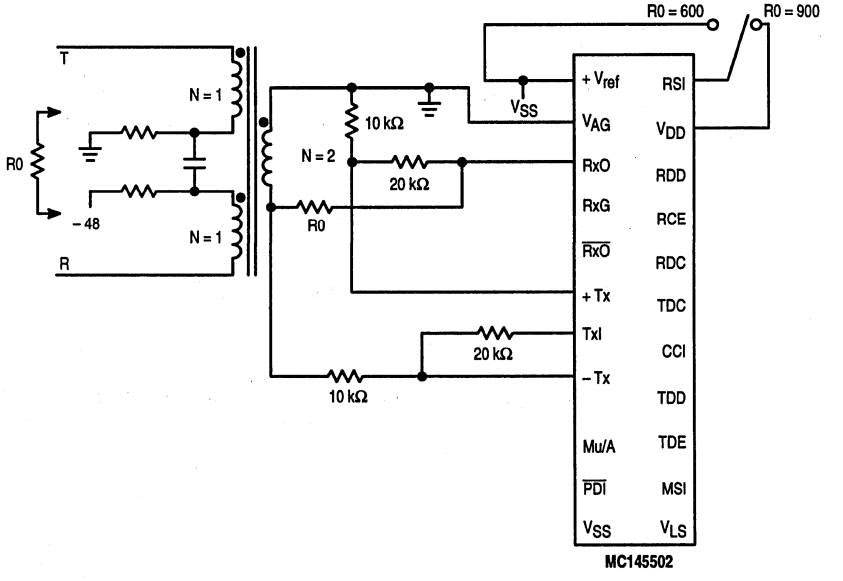


NOTE: Balance by R5 and R6 to equate the TxI gains through the inverting and non-inverting input signal paths, respectively, is given by:

$$\frac{R1}{2 \times R2}\left(1 - \frac{R3}{R4}\right) = \left(1 + \frac{R1}{R2}\right)\left[\frac{R6}{R5 + R6} - \frac{R3}{R4}\left(\frac{R5}{R5 + R6}\right)\right]$$

Tx Gain = R1/R2
Rx Gain = 1 + R3/R4
R5, R6 ≈ 10 kΩ
Adjust Rx Gain with R3
Adjust Tx Gain with R1

24a. Universal Transformer Hybrid Using MC145502



24b. Single–Ended Hybrid Using MC145502

Figure 24. Hybrid Interfaces to the MC145502 PCM Codec-Filter Mono-Circuit

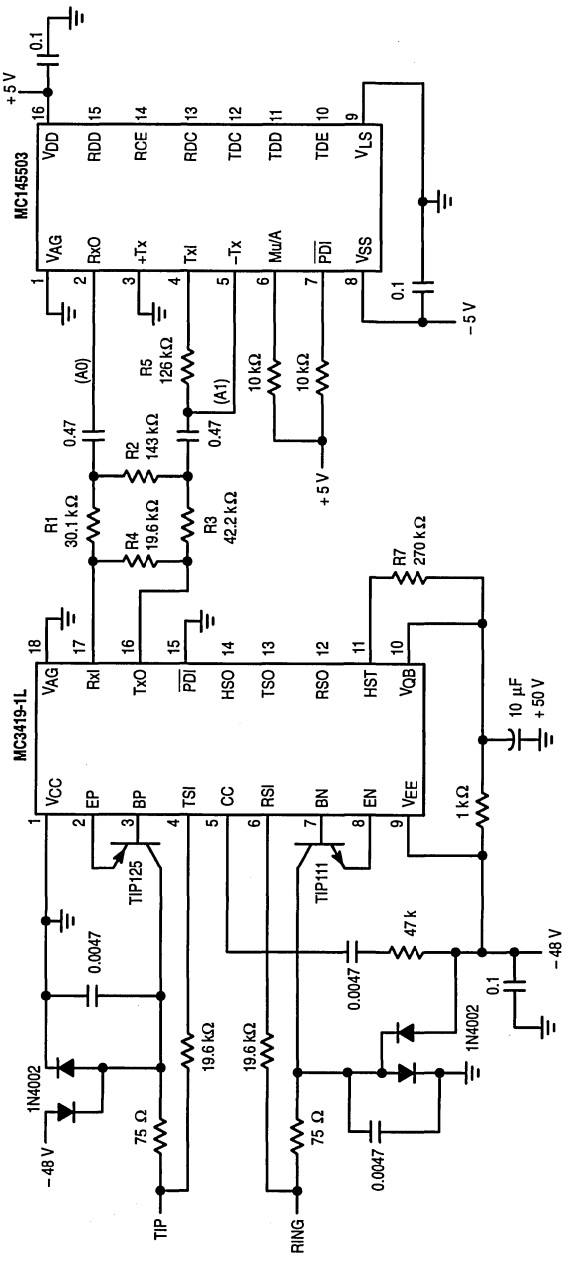


Figure 25. A Complete Single Party Channel Unit Using MC3419 SLIC and MC145503 PCM Mono-Circuit

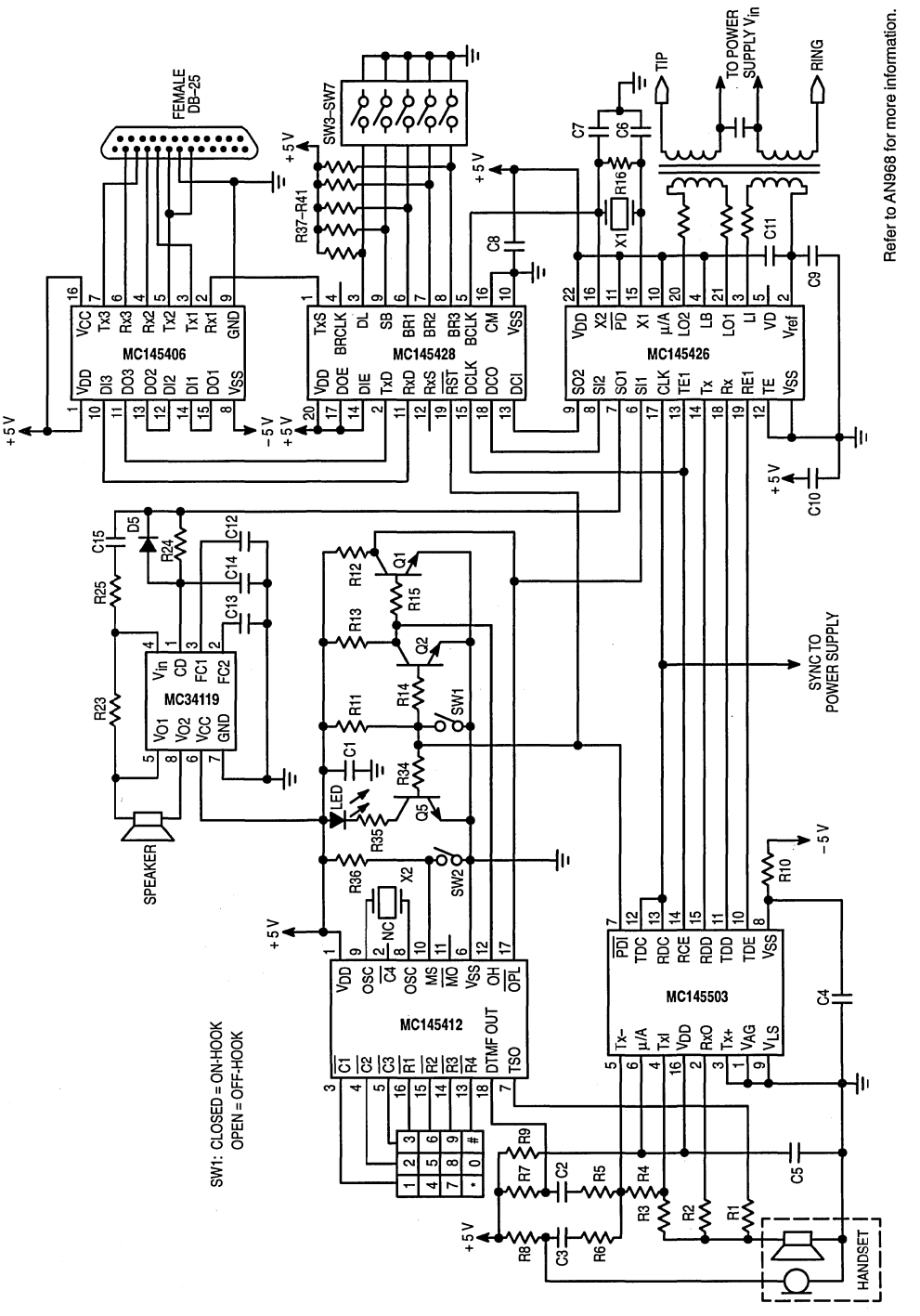


Figure 26. Digital Telephone Schematic

Table 3. Mu-Law Encode-Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			8159									
8	16	256	7903	1	0	0	0	0	0	0	0	8031
			⋮					⋮				⋮
			4319									
7	16	128	4063	1	0	0	0	1	1	1	1	4191
			⋮					⋮				⋮
			2143									
6	16	64	2015	1	0	0	1	1	1	1	1	2079
			⋮					⋮				⋮
			1055									
5	16	32	991	1	0	1	0	1	1	1	1	1023
			⋮					⋮				⋮
			511									
4	16	16	479	1	0	1	1	1	1	1	1	495
			⋮					⋮				⋮
			239									
3	16	8	223	1	1	0	0	1	1	1	1	231
			⋮					⋮				⋮
			103									
2	16	4	95	1	1	0	1	1	1	1	1	99
			⋮					⋮				⋮
			35									
1	15	2	31	1	1	1	0	1	1	1	1	33
			⋮					⋮				⋮
			3									
	1	1	1	1	1	1	1	1	1	1	0	2
			0	1	1	1	1	1	1	1	1	0

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inverison of all magnitude bits.

Table 4. A-Law Encode-Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			4096									
7	16	128	3968	1	0	1	0	1	0	1	0	4032
			⋮					⋮				⋮
			2176	1	0	1	0	0	1	0	1	2112
6	16	64	2048					⋮				⋮
			1088	1	0	1	1	0	1	0	1	1056
5	16	32	1024					⋮				⋮
			544	1	0	0	0	0	1	0	1	528
4	16	16	512					⋮				⋮
			272	1	0	0	1	0	1	0	1	264
3	16	8	256					⋮				⋮
			136	1	1	1	0	0	1	0	1	132
2	16	4	128					⋮				⋮
			68	1	1	1	1	0	1	0	1	66
1	32	2	64					⋮				⋮
			2	1	1	0	1	0	1	0	1	1
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes alternate bit inverison, as specified by CCITT.

MC145532

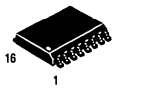
Advance Information

ADPCM Transcoder

Conforms to G.721-1988 and T1.301-1987

The MC145532 Adaptive Differential Pulse Code Modulation (ADPCM) Transcoder provides a low-cost, full-duplex, single-channel transcoder to (from) a 64 kbps PCM channel from (to) either a 16 kbps, 24 kbps, 32 kbps, or 64 kbps channel.

- Complies with CCITT Recommendation G.721-1988
- Complies with the American National Standard (T1.301-1987)
- Full-Duplex, Single-Channel Operation
- μ-Law or A-Law Coding is Pin Selectable
- Synchronous or Asynchronous Operation
- Easily Interfaces with Any Member of Motorola's PCM Codec-Filter Mono-Circuit Family or Other Industry Standard Codec
- Serial PCM and ADPCM Data Transfer Rate from 64 kbps to 5.12 Mbps
- Power Down Capability for Low Current Consumption
- The Reset State, an Option Specified in the Standards, is Automatically Initiated When the RESET Pin is Released
- Simple Time Slot Assignment Timing for Transcoder Applications
- Single 5 V Power Supply
- 16-Pin Package
- The MC145536EVK is the evaluation platform for the MC145532 and also includes the MC145480 5 V PCM Codec-Filter



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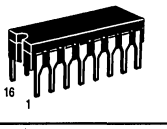
SOG
CASE 751G



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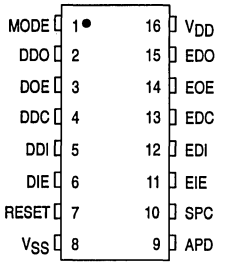
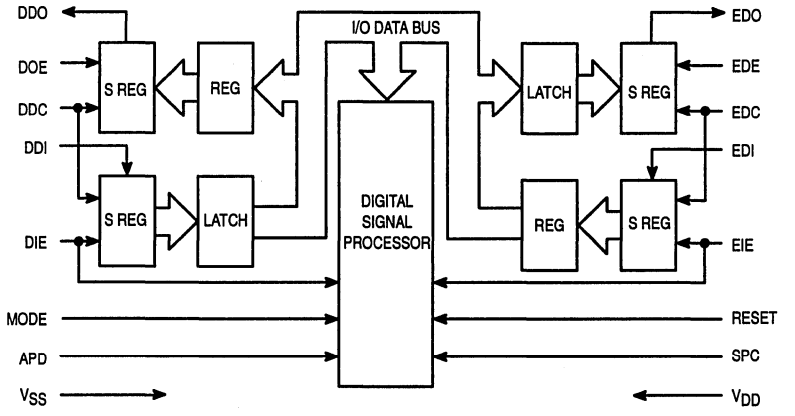
CERAMIC
CASE 620

PIN ASSIGNMENT



BLOCK DIAGRAM



This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

DEVICE DESCRIPTION

An Adaptive Differential PCM (ADPCM) transcoder is used to reduce the data rate required to transmit a PCM encoded voice signal while maintaining the voice fidelity and intelligibility of the PCM signal.

The transcoder is used on 64 kbps data streams which represent either voice or voice band data signals that have been digitized by a codec (e.g., MC145557). The transcoder uses a filter to attempt to predict the next PCM input value based on previous PCM input values. The error between the predicted and the true PCM input value is the information that is sent to the other end of the line. Hence the word differential, since the ADPCM data stream is the difference between the true PCM input value and the predicted value. The term "adaptive" applies to the filter that is performing the prediction. It is adaptive in that its transfer function changes based on the PCM input data. That is, it adapts to the statistics of the signals presented to it.

PIN DESCRIPTION

ENCODER INPUT

EDI
Encoder Data Input (Pin 12)

PCM data to be encoded are applied to this input pin which operates synchronously with EDC and EIE to enter the data in a serial format.

EDC
Encoder Data Clock (Pin 13)

Data applied to EDI are latched into the transcoder on a falling edge of EDC and data are output from EDO on a rising edge of this input pin. The frequency of EDC may be as low as 64 kHz or as high as 5.12 MHz.

EIE
Encoder Input Enable (Pin 11)

The beginning of a new PCM word is indicated to the transcoder by a rising edge applied to this input. The frequency of EIE may not exceed 8 kHz.

ENCODER OUTPUT

EDO
Encoder Data Output (Pin 15)

ADPCM data are available in a serial format from this output, which operates synchronously with EDC and EOE. EDO is a three-state output which remains in a high-impedance state, except when presenting data.

EOE
Encoder Output Enable (Pin 14)

Each ADPCM word is requested by a rising edge on this input, which causes the EDO pin to provide the data when clocked by EDC. One EOE must occur for each EIE.

DECODER INPUT

DDI
Decoder Data Input (Pin 5)

ADPCM data to be decoded are applied to this input pin, which operates in conjunction with DDC and DIE to enter the data in a serial format.

DDC
Decoder Data Clock (Pin 4)

Data applied to DDI are latched into the transcoder on the falling edge of DDC and data are output from DDO on the rising edge of DDC. The frequency of DDC may be as low as 64 kHz or as high as 5.12 MHz.

DIE
Decoder Input Enable (Pin 6)

The beginning of a new ADPCM word is indicated by a rising edge applied to this input. Data are serially clocked into DDI on the subsequent falling edges of DDC following the DIE rising edge. The frequency of DIE may not exceed 8 kHz.

DECODER OUTPUT

DDO
Decoder Data Output (Pin 2)

PCM data are available in a serial format from this output, which operates in conjunction with DDC and DOE. DDO is a three-state output that remains at a high-impedance state except when presenting data.

DOE
Decoder Output Enable (Pin 3)

Each ADPCM word is requested by a rising edge on this input which causes the DDO pin to provide the data when clocked by DDC. One DOE must occur for each DIE.

CONTEXT

MODE
Mode Select (Pin 1)

A logic 0 applied to this input makes the transcoder compatible with μ–255 companding and D3 data format. A logic 1 applied to this pin makes the transcoder compatible with A-law companding with even bit inversion data format.

SPC
Signal Processor Clock (Pin 10)

This input is typically clocked with a 20.48 MHz clock signal which is used as the digital signal processor master clock. This pin has a CMOS compatible input.

RESET
Reset (Pin 7)

A logic 0 applied to this input forces the transcoder into a low power dissipation mode. A rising edge on this pin causes power to be restored and the optional transcoder RESET state (specified in the standards) to be forced. Valid data is available at the output pins four input enables after a rising edge on this pin. This pin has a CMOS compatible input.

APD
Absolute Power Down (Pin 9)

A logic 1 applied to this input forces the transcoder into a power saving mode. This pin has a CMOS compatible input.

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 16)

The most positive power supply pin, normally 5 V.

V_{SS}
Negative Power Supply (Pin 8)

The most negative power supply pin, normally 0 V.

FUNCTIONAL DESCRIPTION

ENCODING/DECODING RATES

The MC145532 allows for the encoding and decoding of data at one of four rates on a sample by sample basis. Each data sample that is provided to the part is accompanied by an indication of the rate at which it is to be encoded or decoded. The width of the enable pulse determines the encoding/decoding rate chosen for each sample.

The 64 kbps rate allows for PCM data to be passed directly through the part. The 32 kbps rate is either the G.721 or the T1.301-1987 standard, depending on the state of the mode pin. The 24 kbps encoding rate is compliant with CCITT G.723 and G.726. The 16 kbps rate is a modified quantizer from the 32 kbps technique and is not a standard.

TIMING

Figures 1 through 8 show the timing of the input and output pins. The MC145532 determines the mode of the timing signals, either short or long frame, for each enable, independent of the mode of any previous enables. A transition from short frame to long frame mode or vice versa will cause at least one frame of data to be destroyed. Each of the four sets of I/O pins determines its mode independent of the other sets. Thus the encoder input could be operating with long frame timing and the output could be operating with short frame timing. Note that the short frame timing on the input enables can only be used with the 32 kbps transcoding rate. The number of data clock falling edges enclosed by the input enable line (EIE or DIE) determines both the short frame or long frame mode and the transcoding rate. The mode of the input or output is determined each frame. In all modes, the data is captured by the MC145532 on the falling edge of either EDC or DDC.

ENCODER INPUT — SHORT FRAME

Figure 1 shows the timing of the encoder data clock (EDC), the encoder input enable (EIE), and the encoder data input (EDI) pins in short frame operation.

The determination of short frame mode is made by the MC145532 based on one falling EDC edge while EIE is high. Note that only a 32 kbps encoding rate can be specified when using short frame mode on the encoder input.

ENCODER INPUT — LONG FRAME

Figure 2 shows the clock, enable, and data signals for the encoder input in long frame mode. In this mode, the data is captured by the MC145532 on the falling edge of EDC.

The determination of the encoding rate is made based on the number of falling EDC edges seen by the MC145532 while EIE is high. Four edges implies a 32 kbps encoding rate, three edges implies a 24 kbps encoding rate, two edges implies a 16 kbps rate, and from five to eight inclusive imply a 64 kbps rate. The encoding rate may be changed on a frame by frame basis. The encoded word is available at EDO (via EOE and EDC) from 250 μs to 375 μs after it is requested.

ENCODER OUTPUT — SHORT FRAME

Figure 3 shows the timing of the encoder output in short frame mode. The length of the LSB is always one half of an EDC cycle.

The EDO will provide the correct number of bits for the encoding rate that was selected for this frame of data on the encoder input pins. The data is loaded into the MC145532 during one frame, encoded on the next frame, and read during the third frame.

ENCODER OUTPUT — LONG FRAME

Figure 4 shows the timing of the encoder output in long frame mode. The enable must be wider than two falling edges of the EDC to be in long frame mode. If the enable falls before the correct number of bits have been presented to the output (EDO), the transcoder will complete the presentation of the bits to the output with the LSB being one half of an EDC period wide. If the enable falls after the one half EDC period of the LSB, then the LSB will be extended up to the full EDC clock period and the subsequent data will be a recirculation of the previous data, which repeats until the enable pin falls. This is shown on the second enable for the 16 kbps encoding rate example in Figure 4.

DECODER INPUT — SHORT FRAME

Figure 5 shows the timing of the decoder data clock, the decoder input enable, and the decoder data input pins in short frame operation. Note that in this mode only a 32 kbps decoding rate can be selected.

DECODER INPUT — LONG FRAME

Figure 6 shows the clock, enable, and data signals for the decoder input in long frame mode.

The determination of the decoding rate is made based on the number of falling DDC edges seen by the MC145532 while DIE is high. Four edges implies a 32 kbps decoding rate, three edges implies a 24 kbps decoding rate, two edges implies a 16 kbps rate, and from five to eight edges inclusive imply a 64 kbps rate. The decoding rate may be changed on a frame by frame basis.

DECODER OUTPUT — SHORT FRAME

Figure 7 shows the timing of the decoder output in short frame mode.

The DDO will provide the 8-bit PCM word for the decoding rate that was selected for this frame of data on the decoder input pins. The data is loaded into the MC145532 during one frame, decoded on the next frame, and read during the third frame.

DECODER OUTPUT — LONG FRAME

Figure 8 shows the timing of the decoder output in long frame mode. Note that at least eight bits are presented to the output, provided that at least two falling edges of DDC are seen while DOE is high. The enable can be used to extend the LSB to a full DDC period and/or cause the eight bits of data to be recirculated to the output pin until the enable falls.

STANDARDS INFORMATION

The following standards apply to the MC145532:

T1.301-1987—32 kbps APDCM

T1.303-1988—24 kbps ADPCM.

CCITT G.721, G.723, and G.726—32 kpbs and 24 kpbs

CCITT documents may be obtained by contacting Omnicom in the USA at (703) 281-1135.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 7.0	V
Voltage, Any Pin to V_{SS}	V	– 0.5 to V_{DD} + 0.5	V
DC Current, Any Pin	I_{in}	±10	mA
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS (T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V_{DD}	4.50	5.50	V
Power Dissipation	P_D	—	0.28	W

DIGITAL CHARACTERISTICS (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter		Symbol	Min	Max	Unit
High Level Input Voltage	Mode, DOE, DDC, DDI, DIE, EIE, EDI, EDC, EOE	V_{IH}	2.0	—	V
Low Level Input Voltage	Mode, DOE, DDC, DDI, DIE, EIE, EDI, EDC, EOE	V_{IL}	—	0.8	V
High Level Input Voltage	RESET, APD, SPC	V_{IH}	0.7 V_{DD}	—	V
Low Level Input Voltage	RESET, APD, SPC	V_{IL}	—	0.3 V_{DD}	V
Input Current		I_{in}	—	± 1.0	µA
Input Capacitance		C_{in}	—	10	pF
High Level Output Voltage (I_{OH} = –2.0 mA)	DDO, EDO	V_{OH}	4.6	—	V
Low Level Output Voltage (I_{OL} = 2.0 MA)	DDO, EDO	V_{OL}	—	0.4	V
Output Leakage Current (V_{DD} = 5.5 V)	DDO, EDO	I_{lkg}	—	± 5.0	µA

SWITCHING CHARACTERISTICS (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Min	Max	Unit
SPC Frequency	19.990	23	MHz
SPC Duty Cycle	45	55	%

ENCODER INPUT — SHORT FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Setup Time	$t_{su(EIE)L}$	15	—	ns
Enable Low Hold Time	$t_{h(EIE)H}$	30	—	ns
Enable Valid Time	$t_{V(EIE)}$	15	—	ns
Enable Hold Time	$t_{h(EIE)}$	15	—	ns
Data Valid Time	$t_{v(EDI)}$	15	—	ns
Data Hold Time	$t_{h(EDI)}$	15	—	ns

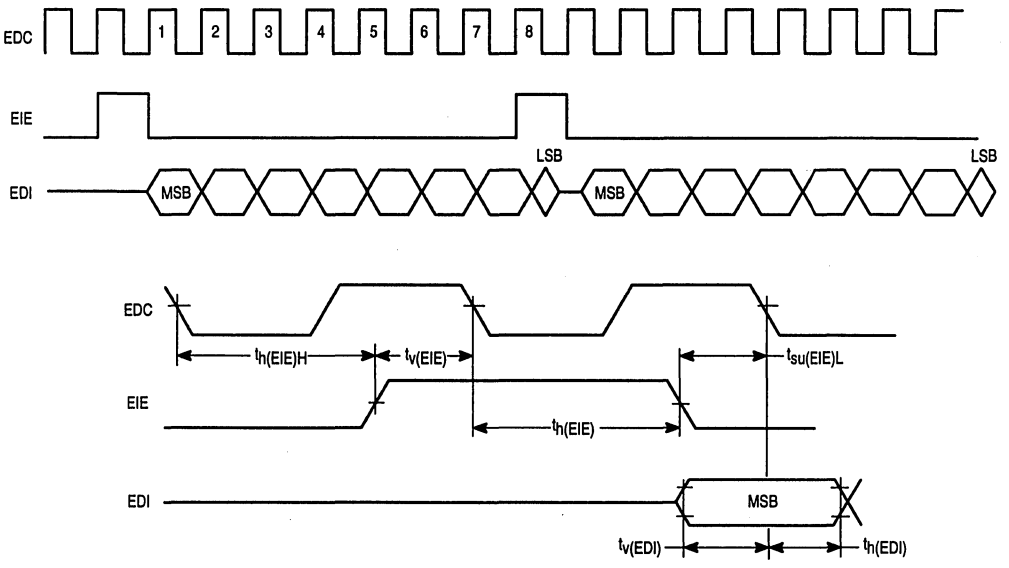


Figure 1. Encoder Input Timing—Short Frame

ENCODER INPUT — LONG FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(EIE)L}$	30	—	ns
Enable Valid Time	$t_{v(EIE)}$	15	—	ns
Data Valid Time	$t_{v(EDI)}$	15	—	ns
Data Hold Time	$t_{h(EDI)}$	15	—	ns

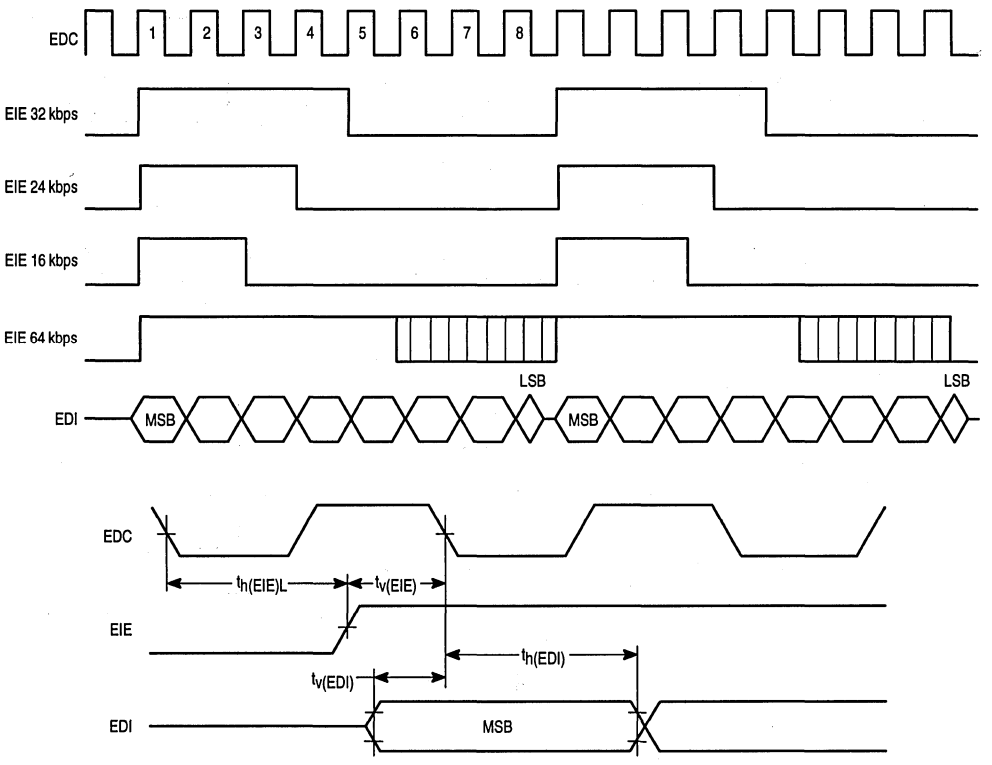


Figure 2. Encoder Input Timing—Long Frame

ENCODER OUTPUT — SHORT FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(EOE)L}$	30	—	ns
Enable Valid Time	$t_{v(EOE)}$	15	—	ns
Enable Hold Time	$t_{h(EOE)}$	15	—	ns
Data Valid Time	$t_{v(EDO)}$	—	40	ns
Data Three-State Time (with 150 pF Load)	$t_{z(EDO)}$	1	30	ns

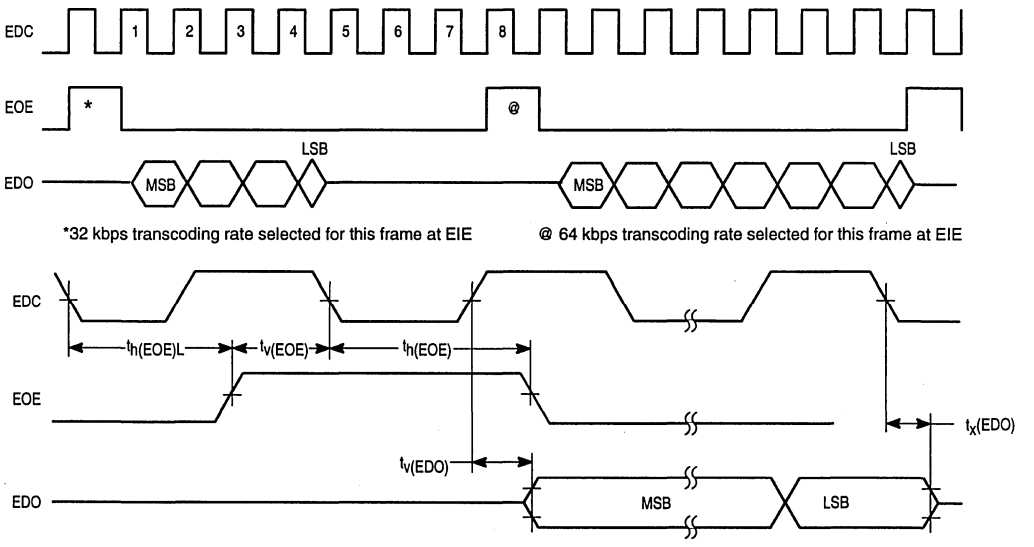


Figure 3. Encoder Output Timing—Short Frame

ENCODER OUTPUT — LONG FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(EOE)L}$	30	—	ns
Enable Valid Time	$t_{v(EOE)}$	15	—	ns
Enable to Data Time (Whichever Edge Occurs Last)	$t_{EOE-EDO}$	—	40	ns
Clock to Data Time (Whichever Edge Occurs Last)	$t_{EDC-EDO}$	—	45	ns

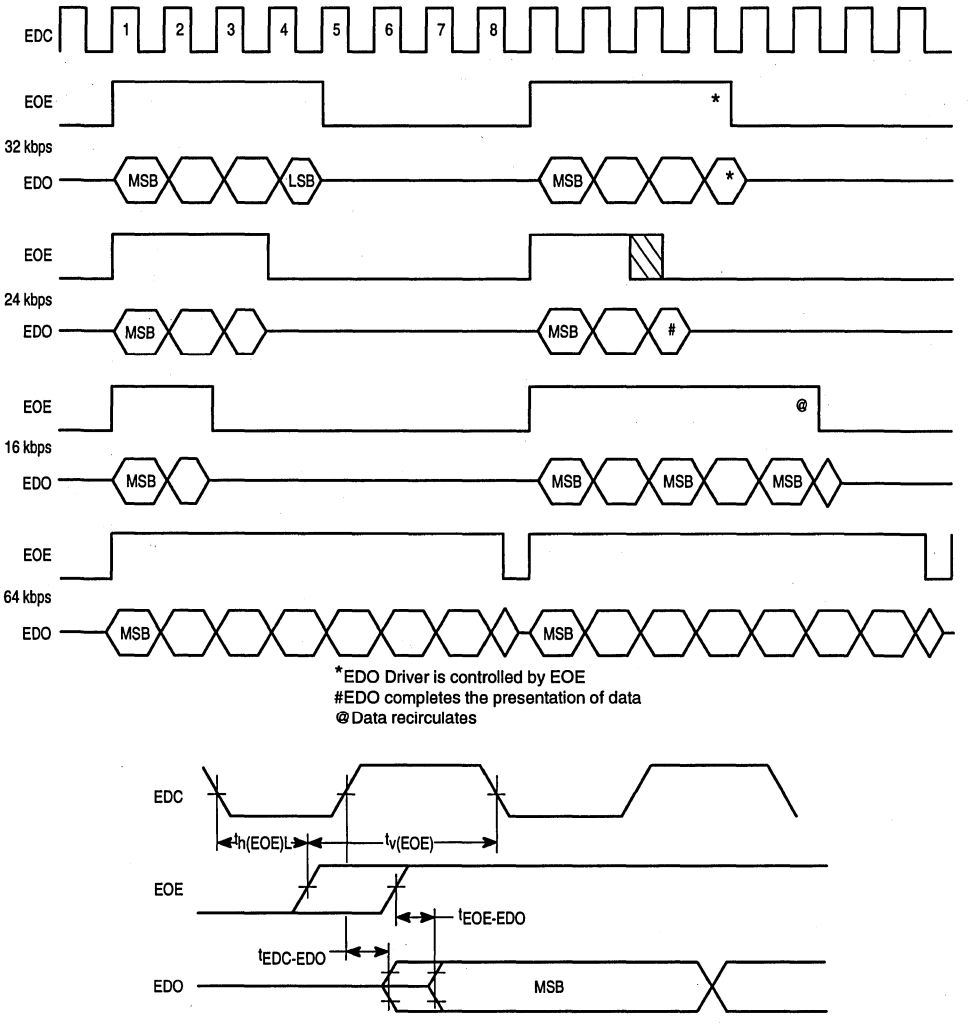


Figure 4. Encoder Output Timing—Long Frame

DECODER INPUT — SHORT FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Setup Time to Falling DDC	$t_{su(DIE)L}$	15	—	ns
Enable Low Hold Time from Falling DDC	$t_{h(DIE)H}$	30	—	ns
Enable Valid Time to Falling DDC	$t_{v(DIE)}$	15	—	ns
Enable Hold Time from Falling DDC	$t_{h(DIE)}$	15	—	ns
Data Valid Time Before Falling DDC	$t_{v(DDI)}$	15	—	ns
Data Hold Time from Falling DDC	$t_{h(DDI)}$	15	—	ns

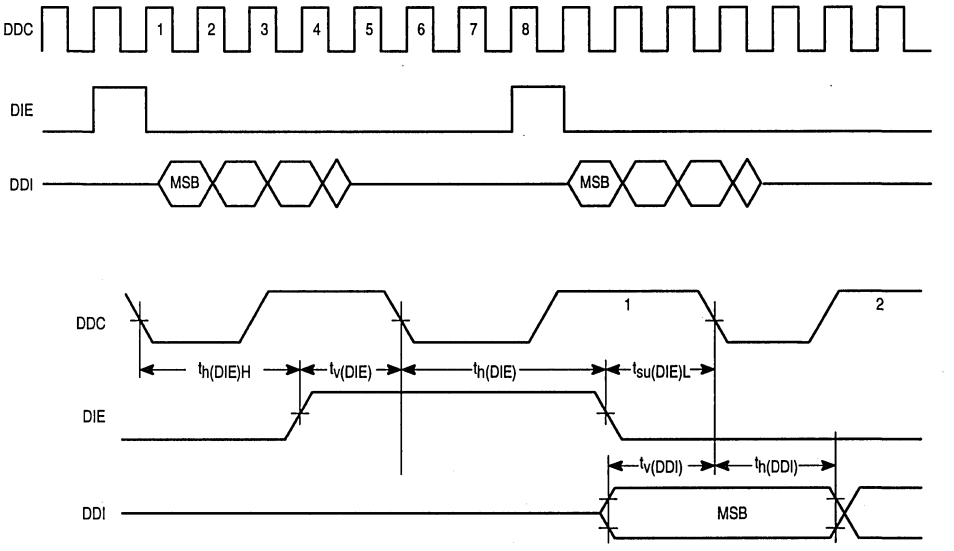


Figure 5. Decoder Input Timing—Short Frame

DECODER INPUT — LONG FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Hold Time from Falling DDC	$t_{h(DIE)}$	30	—	ns
Enable Valid Time to Falling DDC	$t_{v(DIE)}$	15	—	ns
Data Valid Time to Falling DDC	$t_{v(DDI)}$	15	—	ns
Data Hold Time from Falling DDC	$t_{h(DDI)}$	15	—	ns

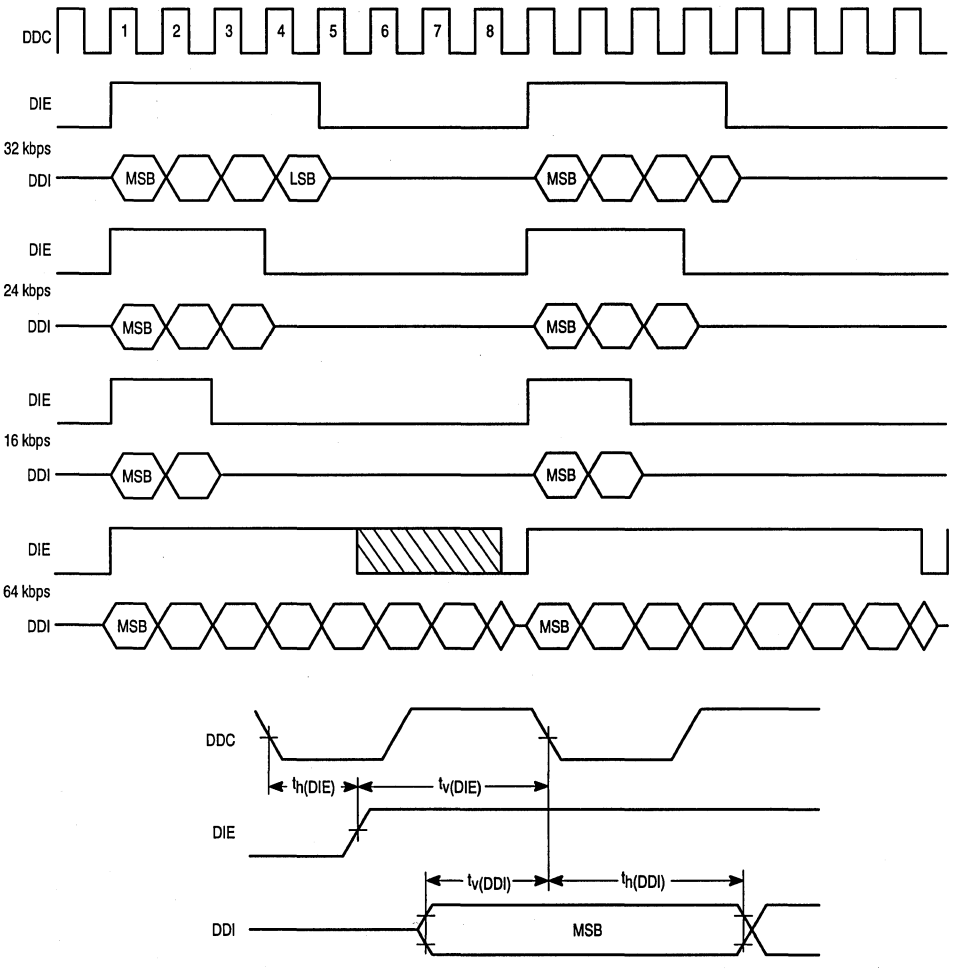


Figure 6. Decoder Input Timing—Long Frame

DECODER OUTPUT — SHORT FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(DOE)L}$	30	—	ns
Enable Valid Time	$t_{v(DOE)}$	15	—	ns
Enable Hold Time	$t_{h(DOE)}$	15	—	ns
Rising Edge of DDC to Valid DDO	$t_{v(DDO)}$	—	40	ns
Delay Time from 8th DDC Low to DDO Output Disabled	$t_{z(DDO)}$	—	30	ns

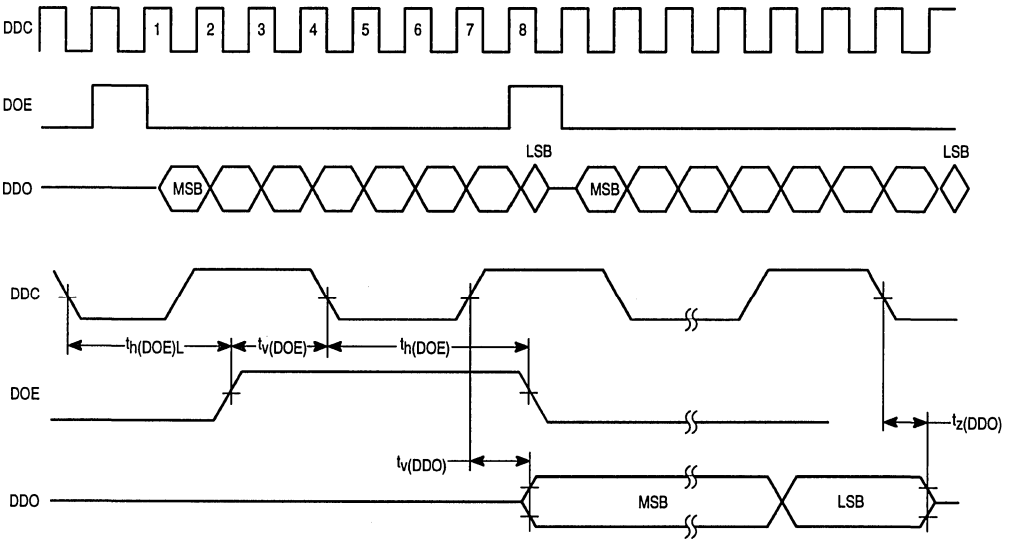


Figure 7. Decoder Output Timing—Short Frame

DECODER OUTPUT — LONG FRAME (V_{DD} = 5.0 V, T_A = – 40 to + 85°C)

Parameter	Symbol	Min	Max	Unit
Enable Low Hold Time	$t_{h(DOE)L}$	30	—	ns
Enable Valid Time	$t_{v(DOE)}$	15	—	ns
Rising Edge of DDE to Valid DDO (when DDC is High)	$t_{DOE-DDO}$	—	40	ns
Rising Edge of DDC to Valid DDO (when DOE is High)	$t_{DDC-DDO}$	—	45	ns
Delay Time from 8th DDC Low or DOE Low to DDO Output Disabled	$t_{z(DDO)}$	0	30	ns

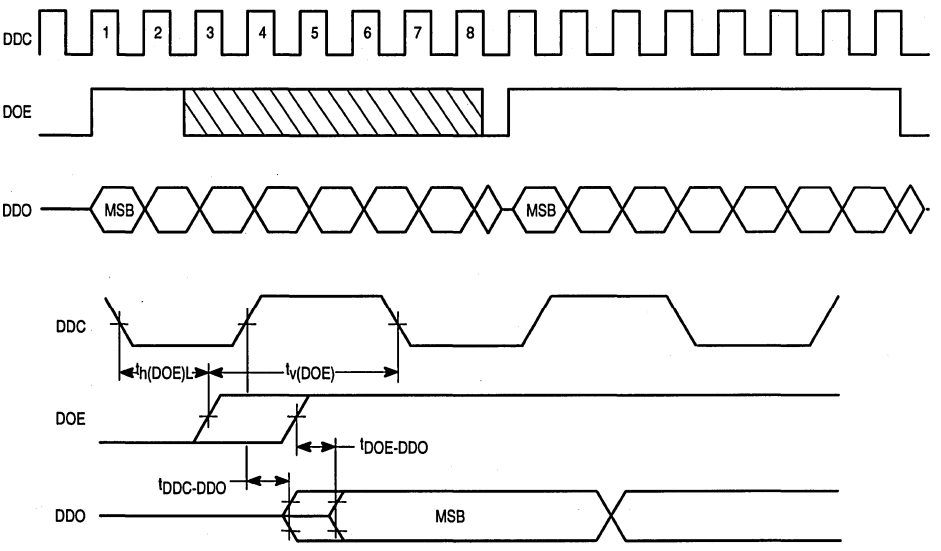


Figure 8. Decoder Output Timing—Long Frame

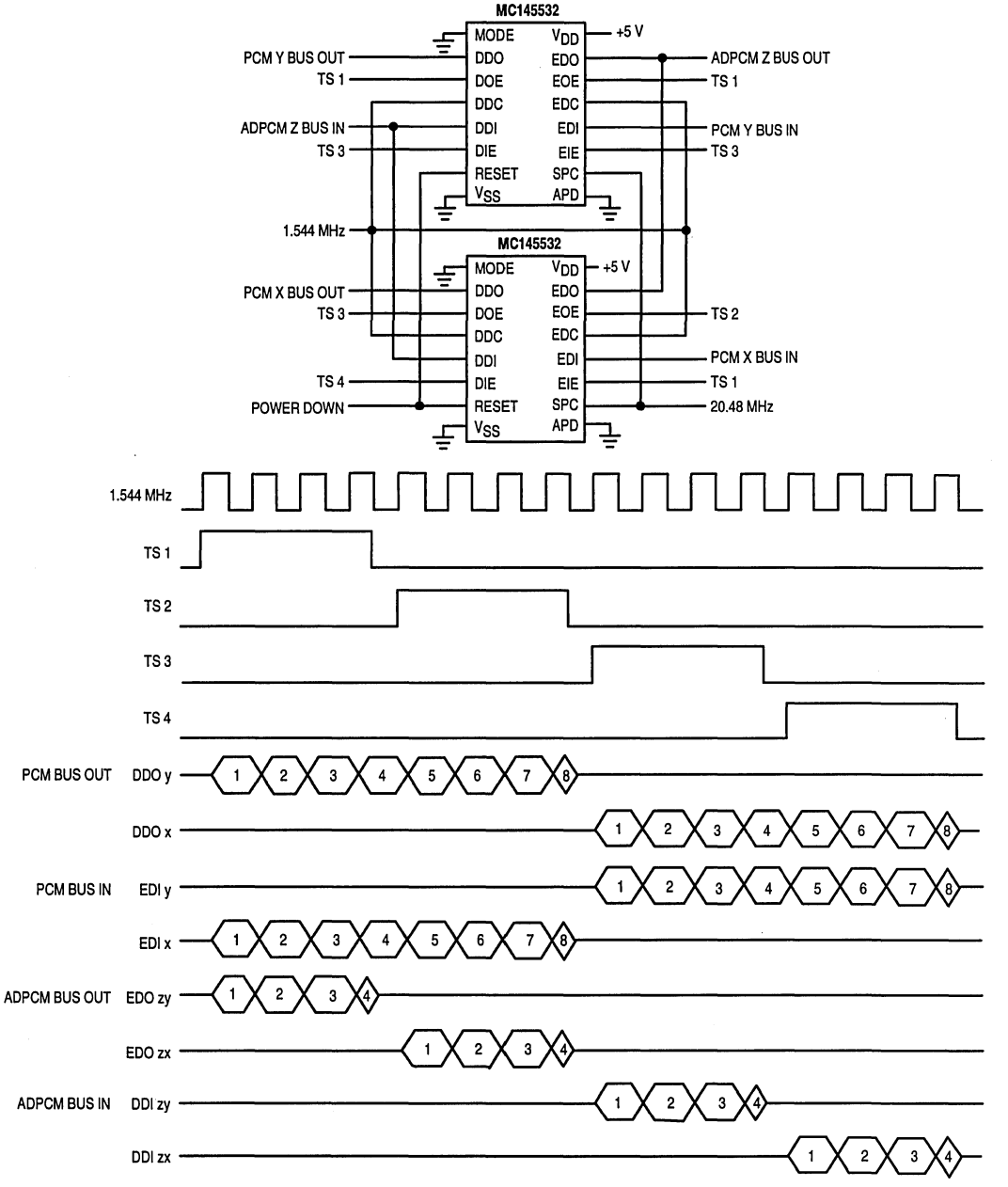


Figure 9. ADPCM Transcoder Application

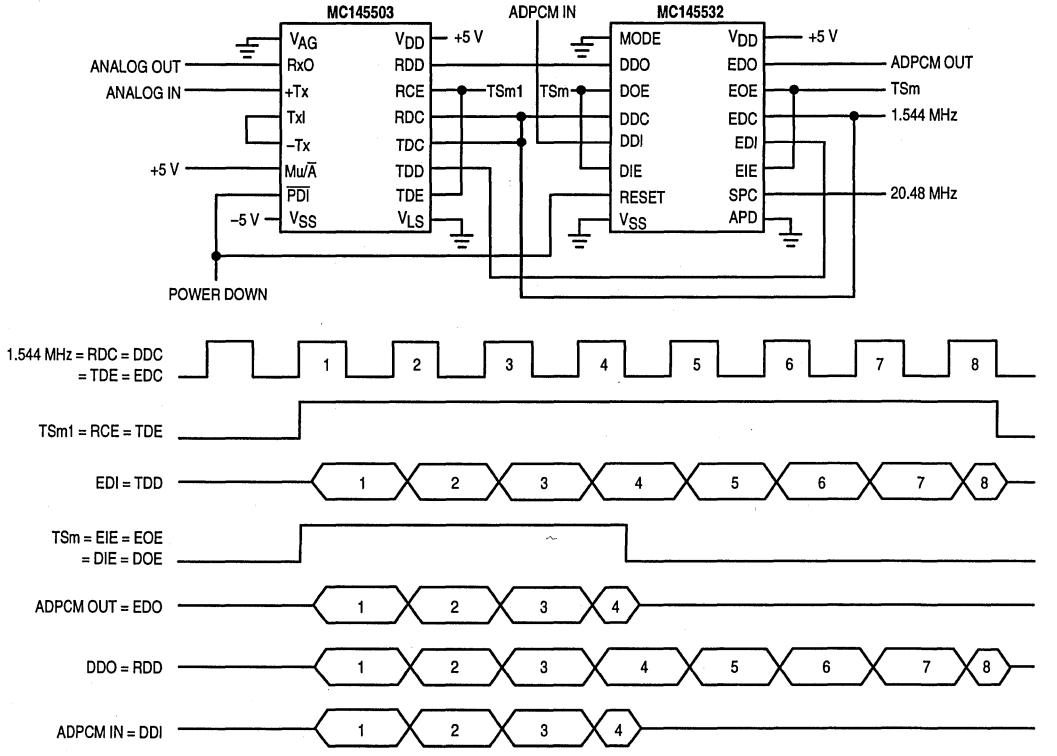
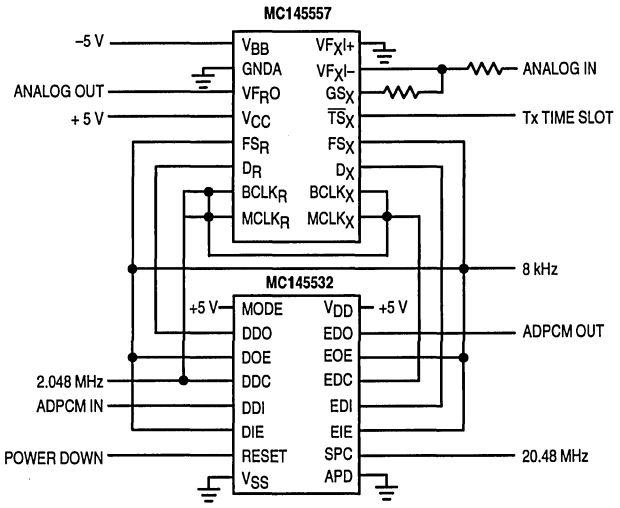


Figure 10. ADPCM Transcoder/Codec Application



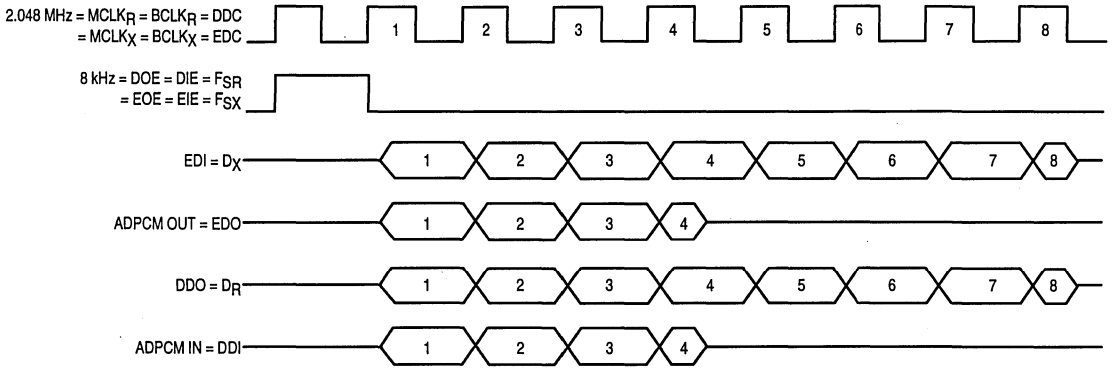


Figure 11. ADPCM Transcoder/Codec Application (A-Law)

MC145540

Technical Summary

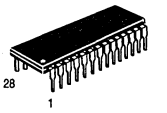
ADPCM Codec

This technical summary provides a brief description of the MC145540 ADPCM Codec. A complete data book for the MC145540 is available and can be ordered from your local Motorola sales office. The data book number is MC145540/D.

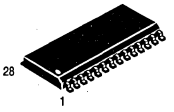
The MC145540 ADPCM Codec is a single chip implementation of a PCM codec-filter and an ADPCM encoder/decoder, and therefore provides an efficient solution for applications requiring the digitization and compression of voiceband signals. This device is designed to operate over a wide voltage range, 2.7 to 5.25 V and, as such, is ideal for battery powered as well as ac powered applications. The MC145540 ADPCM Codec also includes a serial control port and internal control and status registers that permit a microcomputer to exercise many built-in features.

The ADPCM Codec is designed to meet the 32 kbps ADPCM conformance requirements of CCITT Recommendation G.721 and ANSI T1.301. It also meets ANSI T1.303 and CCITT Recommendation G.723 for 24 kbps ADPCM operation, and the 16 kbps ADPCM standard, CCITT Recommendation G.726. This device also meets the PCM conformance specification of the CCITT G.714 Recommendation.

- Single 2.7 to 5.25 V Power Supply
- Typical 3 V Power Dissipation of 60 mW, Power Down of 15 µW
- Differential Analog Circuit Design for Lowest Noise
- Complete Mu-Law and A-Law Companding PCM Codec-Filter
- ADPCM Transcoder for 64, 32, 24, and 16 kbps data rates
- Universal Programmable Dual Tone Generator
- Programmable Transmit Gain, Receive Gain, and Sidetone Gain
- Low Noise, High Gain, Three Terminal Input Operational Amplifier for Microphone Interface
- Push-Pull, 300 Ω Power Drivers with External Gain Adjust for Receiver Interface
- Push-Pull, 300 Ω Auxiliary Output Drivers for Ringer Interface
- Voltage Regulated Charge Pump to Power the Analog Circuitry in Low Voltage Applications
- Receive Noise Burst Detect Algorithm
- Order Complete Document as MC145540/D
- Device Supported by MC145537EVK ADPCM Codec Evaluation Kit



P SUFFIX
PLASTIC DIP
CASE 710

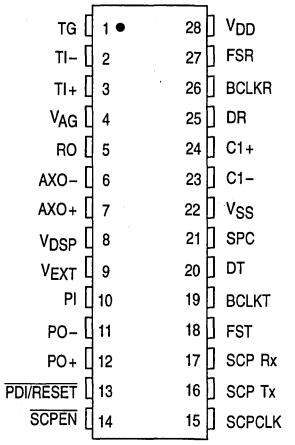


DW SUFFIX
SOG
CASE 751F

ORDERING INFORMATION

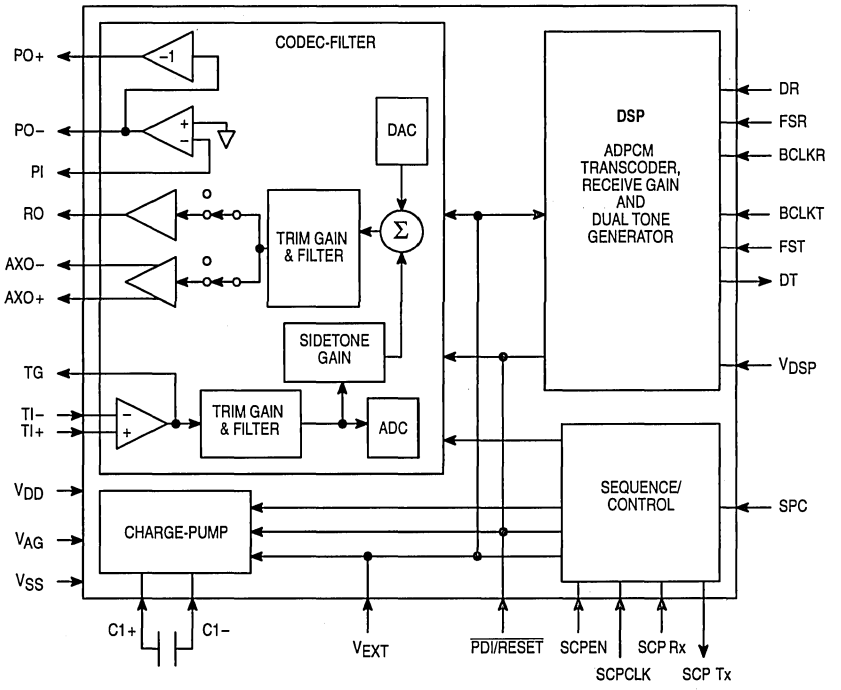
MC145540	SUFFIX	DENOTES
	P	Plastic DIP
	DW	SOG Package

PIN ASSIGNMENT



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

BLOCK DIAGRAM



PIN DESCRIPTIONS

POWER SUPPLY PINS

V_{SS}
Negative Power Supply (Pin 22)

This is the most negative power supply and is typically connected to 0 V.

V_{EXT}
External Power Supply Input (Pin 9)

This power supply input pin must be between 2.70 and 5.25 V. Internally, it is connected to the input of the V_{DSP} voltage regulator, the 5 V regulated charge pump, and all digital I/O including the Serial Control Port and the ADPCM Serial Data Port. This pin is also connected to the analog output drivers (PO+, PO–, AXO+, and AXO–). This pin should be decoupled to V_{SS} with a 0.1 µF ceramic capacitor. This pin is internally connected to the V_{DD} and V_{DSP} pins when the device is powered down.

V_{DSP}
Digital Signal Processor Power Supply Output (Pin 8)

This pin is connected to the output of the on-chip V_{DSP} voltage regulator which supplies the positive voltage to the DSP circuitry and to the other digital blocks of the ADPCM Codec. This pin should be decoupled to V_{SS} with a 0.1 µF ceramic capacitor. This pin cannot be used for powering external loads. This pin is internally connected to the V_{EXT} pin during power down to retain memory.

V_{DD}
Positive Power Supply Input/Output (Pin 28)

This is the positive output of the on-chip voltage regulated charge pump and the positive power supply input to the analog sections of the device. Depending on the supply voltage available, this pin can function in one of two different operating modes:

1. When V_{EXT} is supplied from a regulated 5 V (±5%) power supply, V_{DD} is an input and should be externally connected to V_{EXT}. Charge pump capacitor C1 should not be used and the charge pump should be disabled in BR0 (b2). In this case V_{EXT} and V_{DD} can share the same 0.1 µF ceramic decoupling capacitor to V_{SS}.
2. When V_{EXT} is supplied from 2.70 to 5.25 V, such as battery powered applications, the charge pump should be used. In this case, V_{DD} is the output of the on-chip voltage regulated charge pump and must **not** be connected to V_{EXT}. V_{DD} should be decoupled to V_{SS} with a 1.0 µF ceramic capacitor. This pin cannot be used for powering external loads in this operating mode. This pin is internally connected to the V_{EXT} pin when the charge pump is turned off or the device is powered down.

V_{AG}
Analog Ground Output (Pin 4)

This output pin provides a mid-supply analog ground regulated to 2.4 V. All analog signal processing within this device is referenced to this pin. This pin should be decoupled

to V_{SS} with a 0.01 to 0.1 µF ceramic capacitor. If the audio signals to be processed are referenced to V_{SS}, then special precautions must be utilized to avoid noise between V_{SS} and the V_{AG} pin. Refer to the applications information in this document for more information. The V_{AG} pin becomes high impedance when in analog power-down mode.

C1–, C1+
Charge Pump Capacitor Pins (Pin 23 And 24)

These are the capacitor connections to the internal voltage regulated charge pump that generates the V_{DD} supply voltage. A 0.1 µF capacitor should be placed between these pins. Note that if an external V_{DD} is supplied, this capacitor should not be in the circuit.

ANALOG INTERFACE PINS

TG
Transmit Gain (Pin 1)

This is the output of the transmit gain setting operational amplifier and the input to the transmit band-pass filter. This op amp is capable of driving a 2 kΩ load to the V_{AG} pin. When TI– and TI+ are connected to V_{DD}, the TG op amp is powered down and the TG pin becomes a high-impedance input to the transmit filter. All signals at this pin are referenced to the V_{AG} pin. This pin is high impedance when the device is in the analog power-down mode. This op amp is powered by the V_{DD} pin.

TI–
Transmit Analog Input (Inverting) (Pin 2)

This is the inverting input of the transmit gain setting operational amplifier. Gain setting resistors are usually connected from this pin to TG and from this pin to the analog signal source. The common mode range of the TI+ and TI– pins is from 1.0 V, to V_{DD} – 2 V. Connecting this pin and TI+ (Pin 3) to V_{DD} will place this amplifier's output (TG) in a high-impedance state, thus allowing the TG pin to serve as a high-impedance input to the transmit filter.

TI+
Transmit Analog Input (Non-inverting; Pin 3)

This is the non-inverting input of the transmit input gain setting operational amplifier. This pin accommodates a differential to single-ended circuit for the input gain setting op amp. This allows input signals that are referenced to the V_{SS} pin to be level shifted to the V_{AG} pin with minimum noise. This pin may be connected to the V_{AG} pin for an inverting amplifier configuration if the input signal is already referenced to the V_{AG} pin. The common mode range of the TI+ and TI– pins is from 1.0 V to V_{DD} – 2 V. Connecting this pin and TI– (Pin 2) to V_{DD} will place this amplifier's output (TG) in a high-impedance state, thus allowing the TG pin to serve as a high-impedance input to the transmit filter.

RO
Receive Analog Output (Pin 5)

This is the non-inverting output of the receive smoothing filter from the digital-to-analog converter. This output is capable of driving a 2 kΩ load to 1.575 V peak referenced to the V_{AG} pin. This pin may be dc referenced to either the V_{AG} pin or a voltage of half of V_{EXT} by BR2 (b7). This pin is high impedance when the device is in the analog power-down mode. This pin is high impedance except when it is enabled for analog signal output.

AXO–
Auxiliary Audio Power Output (Inverting) (Pin 6)

This is the inverting output of the auxiliary power output drivers. The Auxiliary Power Driver is capable of differentially driving a 300 Ω load. This power amplifier is powered from V_{EXT} and its output can swing to within 0.5 V of V_{SS} and V_{EXT}. This pin may be dc referenced to either the V_{AG} pin or a voltage of half of V_{EXT} by BR2 (b7). This pin is high impedance in power down. This pin is high impedance except when it is enabled for analog signal output.

AXO+
Auxiliary Audio Power Output (Non-inverting; Pin 7)

This is the non-inverting output of the auxiliary power output drivers. The Auxiliary Power Driver is capable of differentially driving a 300 Ω load. This power amplifier is powered from V_{EXT} and its output can swing to within 0.5 V of V_{SS} and V_{EXT}. This pin may be dc referenced to either the V_{AG} pin or a voltage of half of V_{EXT} by BR2 (b7). This pin is high impedance in power down. This pin is high impedance except when it is enabled for analog signal output.

PI
Power Amplifier Input (Pin 10)

This is the inverting input to the PO– amplifier. The non-inverting input to the PO– amplifier may be dc referenced to either the V_{AG} pin or a voltage of half of V_{EXT} by BR2 (b7). The PI and PO– pins are used with external resistors in an inverting op amp gain circuit to set the gain of the PO+ and PO– push-pull power amplifier outputs. Connecting PI to V_{DD} will power down these amplifiers and the PO+ and PO– outputs will be high impedance.

PO–
Power Amplifier Output (Inverting) (Pin 11)

This is the inverting power amplifier output that is used to provide a feedback signal to the PI pin to set the gain of the push-pull power amplifier outputs. This power amplifier is powered from V_{EXT} and its output can swing to within 0.5 V of V_{SS} and V_{EXT}. This should be noted when setting the gain of this amplifier. This pin is capable of driving a 300 Ω load to PO+ independent of supply voltage. The PO+ and PO– outputs are differential (push-pull) and capable of driving a 300 Ω load to 3.15 V peak, which is 6.3-V peak-to-peak when a nominal 5 V power supply is used for V_{EXT}. The bias voltage and signal reference for this pin may be dc referenced to either the V_{AG} pin or a voltage of half of V_{EXT} by BR2 (b7). Low impedance loads must be between PO+ and PO–. This pin is high impedance when the device is in the analog power-down mode. This pin is high impedance except when it is enabled for analog signal output.

PO+
Power Amplifier Output (Non-inverting) (Pin 12)

This is the non-inverting power amplifier output that is an inverted version of the signal at PO–. This power amplifier is powered from V_{EXT} and its output can swing to within 0.5 V of V_{SS} and V_{EXT}. This pin is capable of driving a 300 Ω load to PO–. This pin may be dc referenced to either the V_{AG} pin or a voltage of half of V_{EXT} by BR2 (b7). This pin is high impedance when the device is in the analog power-down mode. See **PI** and **PO–** for more information. This pin is high impedance except when it is enabled for analog signal output.

ADPCM/PCM SERIAL INTERFACE PINS

FST
Frame Sync, Transmit (Pin 18)
When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts an 8 kHz clock that synchronizes the output of the serial ADPCM data at the DT pin.

BCLKT
Bit Clock, Transmit (Pin 19)
When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts any bit clock frequency from 64 to 5120 kHz.

DT
Data, Transmit (Pin 20)
This pin is controlled by FST and BCLKT and is high impedance except when outputting data.

SPC
Signal Processor Clock (Pin 21)
This input requires a 20.48 or 20.736 MHz clock signal that is used as the DSP engine master clock. Internally the device divides down this clock to generate the 256 kHz clock required by the PCM Codec. (This clock may be optionally specified for higher frequencies; contact the factory for more information.)

DR
Data, Receive (Pin 25)
ADPCM data to be decoded are applied to this input, which operates synchronously with FSR and BCLKR to enter the data in a serial format.

BCLKR
Bit Clock, Receive (Pin 26)
When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts any bit clock frequency from 64 to 5120 kHz. This pin may be used for applying an external 256 kHz clock for sequencing the analog signal processing functions of this device. This is selected by the SCP port at BR0 (b7).

FSR
Frame Sync, Receive (Pin 27)
When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts an 8 kHz clock that synchronizes the input of the serial ADPCM data at the DR pin. FSR can operate asynchronous to FST in the Long Frame Sync or Short Frame Sync mode.

SERIAL CONTROL PORT INTERFACE PINS

$\overline{\text{PDI/RESET}}$
Power-Down Input/Reset (Pin 13)
A logic 0 applied to this input forces the device into a low-power dissipation mode. A rising edge on this pin causes power to be restored and the ADPCM Reset state (specified in the standards) to be forced.

$\overline{\text{SCPEN}}$
Serial Control Port Enable Input (Pin 14)
This pin, when held low, selects the Serial Control Port (SCP) for the transfer of control and status information into and out of the MC145540 ADPCM Codec. This pin should be held low for a total of 16 periods of the SCPCLK signal in order for information to be transferred into or out of the MC145540 ADPCM Codec. The timing relationship between $\overline{\text{SCPEN}}$ and SCPCLK is shown in Figures 6 through 9.

SCPCLK
Serial Control Port Clock Input (Pin 15)
This input to the device is used for controlling the rate of transfer of data into and out of the SCP Interface. Data are clocked into the MC145540 ADPCM Codec from SCP Rx on rising edges of SCPCLK. Data are shifted out of the device on SCP Tx on falling edges of SCPCLK. SCPCLK can be any frequency from 0 to 4.096 MHz. An SCP transaction takes place when $\overline{\text{SCPEN}}$ is brought low. Note that SCPCLK is ignored when $\overline{\text{SCPEN}}$ is high (i.e., it may be continuous or it can operate in a burst mode).

SCP Tx
Serial Control Port Transmit Output (Pin 16)
SCP Tx is used to output control and status information from the MC145540 ADPCM Codec. Data are shifted out of SCP Tx on the falling edges of SCPCLK, most significant bit first.

SCP Rx
Serial Control Port Receive Input (Pin 17)
SCP Rx is used to input control and status information to the MC145540 ADPCM Codec. Data are shifted into the device on rising edges of SCPCLK. SCP Rx is ignored when data are being shifted out of SCP Tx or when $\overline{\text{SCPEN}}$ is high.

ADPCM/PCM SERIAL INTERFACE TIMING DIAGRAMS

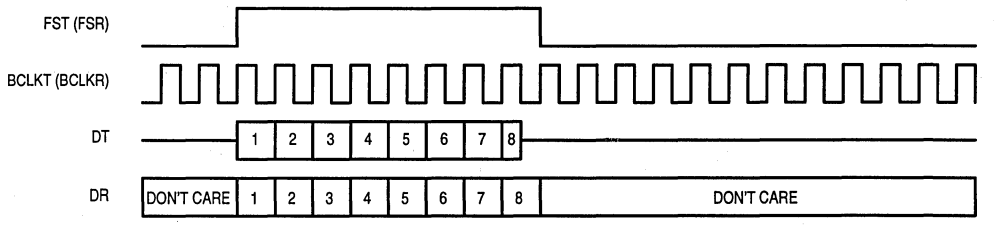


Figure 1. Long Frame Sync (64 kbps PCM Data Timing)

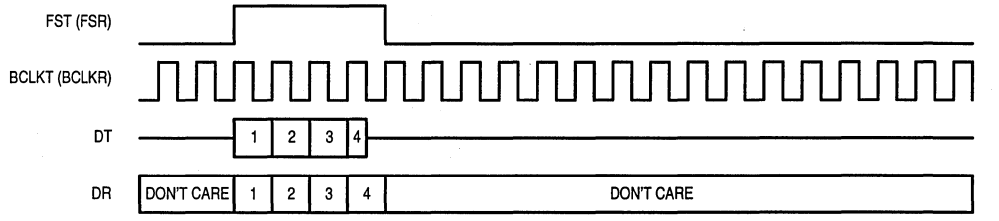


Figure 2. Long Frame Sync (32 kbps ADPCM Data Timing)

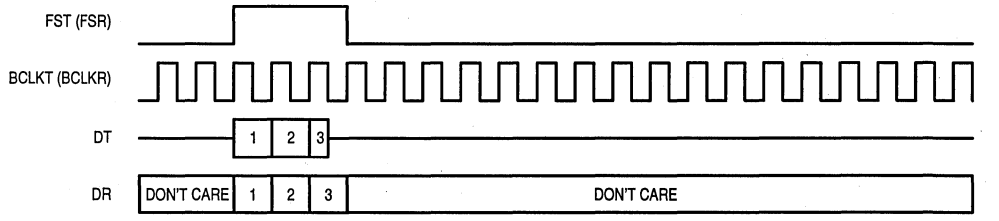


Figure 3. Long Frame Sync (24 kbps ADPCM Data Timing)

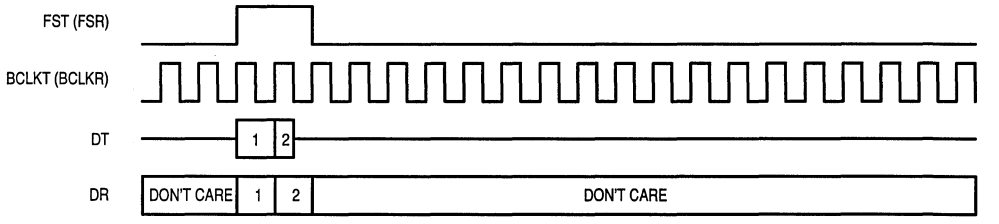


Figure 4. Long Frame Sync (16 kbps ADPCM Data Timing)

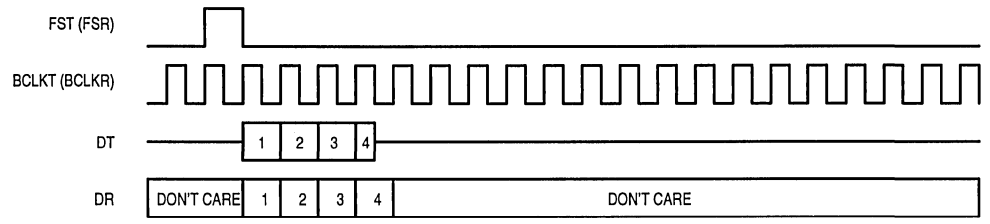


Figure 5. Short Frame Sync (32 kbps ADPCM Data Timing)

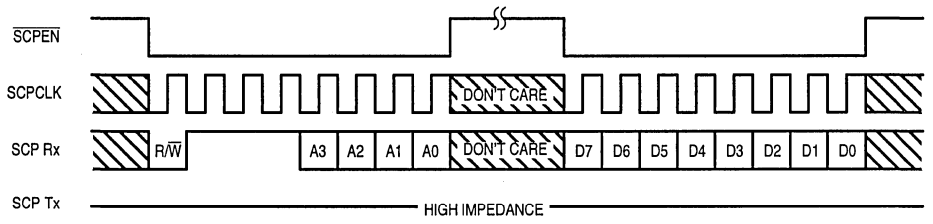


Figure 6. SCP Byte Register Write Operation Using Double 8-Bit Transfer

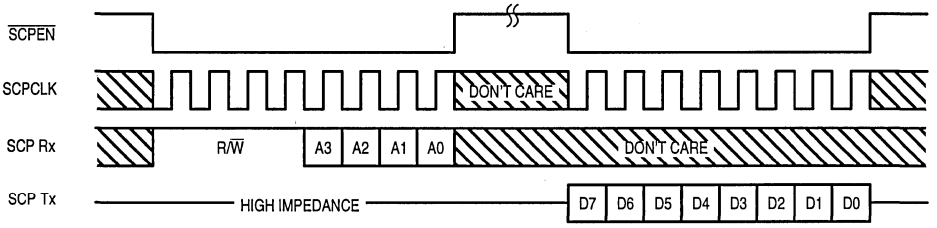


Figure 7. SCP Byte Register Read Operation Using Double 8-Bit Transfer

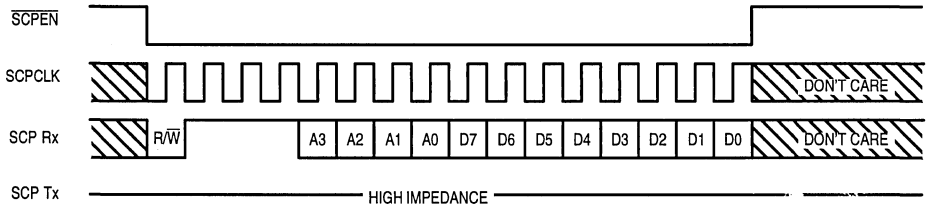


Figure 8. SCP Byte Register Write Operation Using Single 16-Bit Transfe

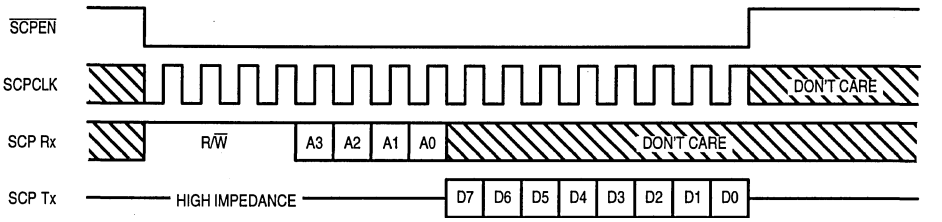


Figure 9. SCP Byte Register Read Operation Using Single 16-Bit Transfer

SERIAL CONTROL PORT (SCP) INTERFACE

The MC145540 is equipped with an industry standard Serial Control Port (SCP) Interface. The SCP is used by an external controller, such as an M68HC05 family microcontroller, to communicate with the MC145540 ADPCM Codec.

The SCP is a full-duplex, four-wire interface used to pass control and status information to and from the ADPCM Codec. The SCP Interface consists of a transmit output, a receive input, a data clock, and an enable signal. These device pins are known as SCP Tx, SCP Rx, SCPCLK, and $\overline{\text{SCPEN}}$, respectively. The SCPCLK determines the rate of exchange of data in both the transmit and receive directions, and the $\overline{\text{SCPEN}}$ signal governs when this exchange is to take place.

The operation and configuration of the ADPCM Codec is controlled by setting the state of the control and status registers within the MC145540 and then monitoring these control and status registers. The control and status registers reside in sixteen 8-bit wide Byte Registers, BR0–BR15. A complete register map can be found in the Serial Control Port Registers section.

BYTE REGISTER OPERATIONS

The sixteen Byte Registers are addressed by addressing a four-bit byte register address (A3:A0) as shown in Figures 6 and 7. A second 8-bit operation transfers the data word (D7:D0). Alternatively, these registers can be accessed with a single 16-bit operation as shown In Figures 8 and 9.

ADPCM CODEC DEVICE DESCRIPTION

The MC145540 is a single channel Mu-Law or A-Law companding PCM codec-filter with an ADPCM encoder/decoder operating on a single voltage power supply from 2.7 to 5.25 V.

The MC145540 ADPCM Codec is a complete solution for digitizing and reconstructing voice in compliance with CCITT G.714, G.721, G.723, G.726 and ANSI T1.301 and T1.303 for 64, 32, 24, and 16 kbps. This device satisfies the need for high quality, low power, low data rate voice transmission, and storage applications and is offered in 28-pin Plastic Dip and SOG packages.

Referring to Figure 10, the main functional blocks of the MC145540 are the switched capacitor technology PCM codec-filter, the DSP based ADPCM encoder/decoder, and the voltage regulated charge pump. As an introduction to the functionality of the ADPCM Codec, a basic description of these functional blocks follows.

PCM CODEC-FILTER BLOCK DESCRIPTION

A PCM codec-filter is a device used for digitizing and reconstructing the human voice. These devices were developed primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, fiber optics, satellites, etc.) without degradation. The name codec is an acronym from "COder" for the analog-to-digital converter (ADC) used to digitize voice, and "DECoder" for the digital-to-analog converter (DAC) used for reconstructing voice. A codec is a single device that does both the ADC and DAC conversions.

To digitize voice intelligibly requires a signal to distortion of about 30 dB for a dynamic range of about 40 dB. This may be accomplished with a linear 13-bit ADC and DAC, but will far exceed the required signal to distortion at amplitudes greater than 40 dB below the peak amplitude. This excess performance is at the expense of bits of data per sample. Two methods of data reduction are implemented by compressing the 13-bit linear scheme to companded 8-bit schemes. These companding schemes follow a segmented or "piecewise-linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all 16 of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits, which increment. When the chord bits increment, the step bits double their voltage weighting. This results in an effective resolution of six bits (sign + chord + four step bits) across a 42-dB dynamic range (seven chords above 0, by 6 dB per chord). There are two companding schemes used: Mu-255 Law specifically in North America and A-Law specifically in Europe. These companding schemes are accepted world wide.

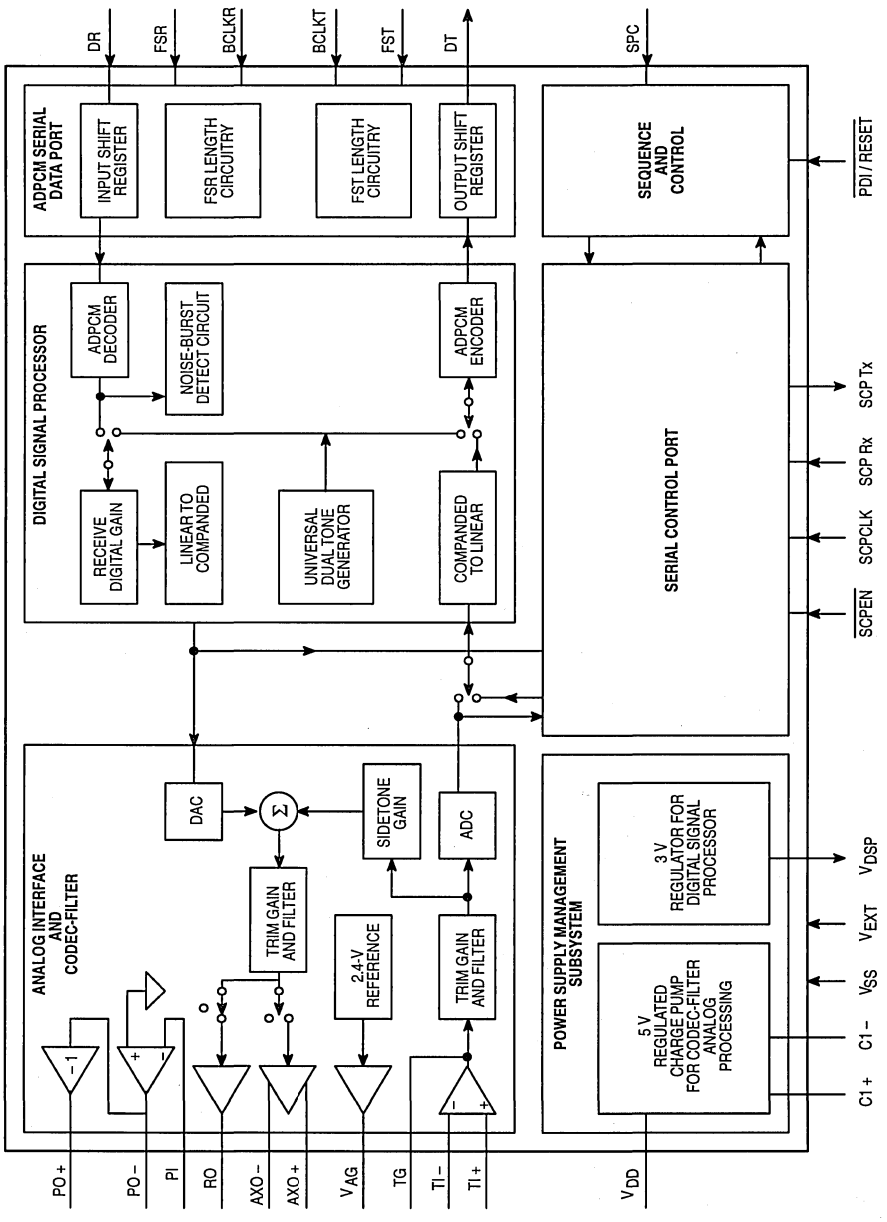


Figure 10. ADPCM Codec Block Diagram

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low-pass filter to limit the high frequency energy above 3 kHz from distorting the inband signal. The telephone line is also subject to 50/60 Hz power line coupling, which must be attenuated from the signal by a high-pass filter before the analog-to-digital converter.

The digital-to-analog conversion process reconstructs a staircase version of the desired inband signal which has spectral images of the inband signal modulated about the sample frequency and its harmonics. These spectral images are called aliasing components which need to be attenuated to obtain the desired signal. The low-pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The MC145540 ADPCM Codec incorporates this codec function as one of its main functional blocks.

ADPCM TRANSCODER BLOCK DESCRIPTION

An Adaptive Differential PCM (ADPCM) transcoder is used to reduce the data rate required to transmit a PCM encoded voice signal while maintaining the voice fidelity and intelligibility of the PCM signal.

The ADPCM transcoder is used on both Mu-Law and A-Law 64 kbps data streams which represent either voice or voice band data signals that have been digitized by a PCM codec-filter. The PCM to ADPCM encoder section of this transcoder has a type of linear predicting digital filter which is trying to predict the next PCM sample based on the previous history of the PCM samples. The ADPCM to PCM decoder section implements an identical linear predicting digital filter. The error or difference between the predicted and the true PCM input value is the information that is sent from the encoder to the decoder as an ADPCM word. The characteristics of this ADPCM word include the number of quantized steps (this determines the number of bits per ADPCM word) and the actual meaning of this word is a function of the predictor's output value, the error signal and the statistics of the history of PCM words. The term "adaptive" applies to the transfer function of the filter that generates the ADPCM word which adapts to the statistics of the signals presented to it. This means that an ADPCM word "3" does not have the same absolute error voltage weighting for the analog signal when the channel is quiet as it does when the channel is processing a speech signal. The ADPCM to PCM decoder section has a reciprocating filter function which interprets the ADPCM word for proper reconstruction of the PCM sample.

The adaptive characteristics of the ADPCM algorithm make it difficult to analyze and quantify the performance of the ADPCM code sequence. The 32 kbps algorithm was optimized for both voice and moderate speed modems ($\leq$4800 baud). This optimization includes that the algorithm supports the voice frequency band of 300–3400 Hz with minimal degradation for signal-to-distortion, gain-versus-level, idle channel noise, and other analog transmission performance. This algorithm has also been subjected to audibility testing with many languages for Mean Opinion Score (MOS) ratings and performed well when compared to 64 kbps PCM. The standards committees have specified multiple 16000 word test vectors for the encoder and for the decoder to verify compliance. To run these test vectors, the device must be initialized to the reference state by resetting the device.

In contrast to 64-kbps PCM, the ADPCM words appear as random bit activity on an oscilloscope display whether the audio channel is processing speech or a typical PCM idle channel with nominal bit activity. The ADPCM algorithm does not support dc signals with the exception of digital quiet, which will result in all ones in the ADPCM channel. All digital processing is performed on 13-bit linearizations of the 8-bit PCM companded words, whether the words are Mu-Law or A-Law. This allows an ADPCM channel to be intelligibly decoded into a Mu-Law PCM sequence or an A-Law PCM sequence irrespective of whether it was originally digitized as Mu-Law or A-Law. There will be additional quantizing degradation if the companding scheme is changed because the ADPCM algorithm is trying to reconstruct the original 13-bit linear codes, which included companding quantization.

CHARGE PUMP

The charge pump is the functional block that allows the analog signal processing circuitry of the MC145540 to operate with a power supply voltage as low as 2.7 V. This analog signal processing circuitry includes the PCM codec-filter function, the transmit trim gain, the receive trim gain, the sidetone gain control, and the transmit input operational amplifier. This circuitry does not dissipate much current but it does require a nominal voltage of 5 V for the V_{DD} power supply.

The charge pump block is a regulated voltage doubler which takes twice the current it supplies from the voltage applied to the V_{EXT} power supply pin which may range from 2.7 to 5.25 V and generates the required 5 V V_{DD} supply. The charge pump block receives as inputs the V_{EXT} supply voltage, the same 256 kHz clock that sequences the analog signal processing circuitry, and the Charge Pump Enable signal from the SCP block. It also makes use of the capacitor connected to the C1+ and C1– pins and the decoupling capacitor connected to the V_{DD} pin.

FUNCTIONAL DESCRIPTION

POWER SUPPLY CONFIGURATION

Analog Signal Processing Power Supply

All analog signal processing is powered by the V_{DD} pin at 5 V. This voltage may be applied directly to the V_{DD} pin or 5 V may be obtained by the on-chip 5 V regulated charge pump which is powered from the V_{EXT} pin. The V_{EXT} pin is the main positive power supply pin for this device.

For applications that are not 5 V regulated, the on-chip 5 V regulated charge pump may be turned on and C1 will be required. V_{DD} will require a 1.0 µF decoupling capacitor to filter the voltage spikes of the charge pump. This allows the V_{EXT} power supply to be from 2.7 to 5.25 V. This mode of operation is intended for hand held applications where three NiCad cells or three dry cells would be the power supply.

The on-chip 5 V regulated charge pump is a single stage charge pump that effectively series regulates the amount of voltage it generates and internally applies this regulated voltage to the V_{DD} pin. This 5 V voltage is developed by connecting the external 0.1 µF capacitor (C1) between the VEXT power supply pin and the power supply ground pin, V_{SS}. This puts a charge of as much as 2.7 V on C1. The charge pump circuitry then connects the negative lead of C1 to the V_{EXT}, pin which sums the voltage of C1 with the voltage at V_{EXT} for a minimum potential voltage of 5.4 V. The charge

voltage on C1 is regulated such that the summing of voltages is regulated to 5 V. This limits all of the voltages on the device to safe levels for this IC fabrication technology. This charge pumped voltage is then stored on the 1.0 µF capacitor connected at V_{DD} and V_{SS}, which filters and serves as a reservoir for power. The clock period for this charge pump is the same 256 kHz as the analog sequencing clock, minimizing noise problems.

For applications with a regulated 5 V (±5%) power supply, the V_{DD} pin and the V_{EXT} pin are connected to the 5 V power supply. These pins may share one decoupling capacitor in this configuration as a function of external noise on the power supply. The on-chip, 5 V regulated charge pump should be turned off via the SCP port at register 0. The external capacitor (C1) should not be populated for these applications.

Digital Signal Processing Power Supply

This device has an on-chip series regulator which limits the voltage of the Digital Signal Processing (DSP) circuitry to about 3 V. This reduces the maximum power dissipation of this circuitry. From the V_{EXT} power supply pin, the DSP circuitry appears as a constant current load instead of a resistive ($CV^2/2$) load for a constant clock frequency. This series regulator is designed to have a low drop-out voltage, which allows the DSP circuitry to work when the V_{EXT} voltage is as low as 2.7 V. The output of this regulator is brought out to the V_{DSP} pin for a 0.1 µF decoupling capacitor. This regulator is not designed to power any loads external to the device.

ANALOG INTERFACE AND SIGNAL PATH

Transmit Analog

The transmit analog portion of this device includes a low-noise, three terminal operational amplifier capable of driving a 2 kΩ load. This op amp has inputs of TI+ and TI– and its output is TG. This op amp is intended to be configured in an inverting gain circuit. The analog signal may be applied directly to the TG pin if this transmit op amp is independently powered down. Power down may be achieved by connecting both the TI+ and TI– inputs to the V_{DD} pin. The TG pin becomes high impedance when the transmit op amp is powered down. The TG pin is internally connected to a time continuous three-pole anti-aliasing pre-filter. This pre-filter incorporates a two-pole Butterworth active low-pass filter, followed by a single passive pole. This pre-filter is followed by a single-ended to differential converter that is clocked at 512 kHz. All subsequent analog processing utilizes fully differential circuitry. The output of the differential converter is followed by the transmit trim gain stage. This stage is intended to compensate for gain tolerances of external components such as microphones. The amount of gain control is 0–7 dB in 1 dB steps. This stage only accommodates positive gain because the maximum signal levels of the output of the input op amp are the same as the transmit filter and ADC, which should nominally be next to the clip levels of this device's circuitry. Any requirement for attenuation of the output of the input op amp would mean that it is being overdriven. The gain is programmed via the SCP port in BR1 (b2:b0). The next section is a fully-differential, 5-pole switched-capacitor low-pass filter with a 3.4 kHz frequency cutoff. After this filter is a 3-pole switched-capacitor high-pass filter having a cutoff frequency of about 200 Hz. This high-pass stage has a transmission zero at dc that eliminates any dc coming from the analog input or from accumulated op amp offsets in the preceding filter stages. (This high-pass filter may be removed from the signal path under control of the SCP port BR8 (b4).) The last stage of the high-pass filter is an autozeroed sample and hold amplifier.

One bandgap voltage reference generator and digital-to-analog converter (DAC) are shared by the transmit and receive sections. The autozeroed, switched-capacitor bandgap reference generates precise positive and negative reference voltages that are virtually independent of temperature and power supply voltage. A binary-weighted capacitor array (CDAC) forms the chords of the companding structure, while a resistor string (RDAC) implements the linear steps within each chord. The encode process uses the DAC, the voltage reference, and a frame-by-frame autozeroed comparator to implement a successive-approximation analog-to-digital conversion (ADC) algorithm. All of the analog circuitry involved in the data conversion (the voltage reference, RDAC, CDAC, and comparator) are implemented with a differential architecture.

The nonlinear companded Mu-Law transfer curve of the ADC may be changed to 8-bit linear by BR8 (b5).

The input to the ADC is normally connected to the output of the transmit filter section, but may be switched to measure the voltage at the V_{EXT} pin for battery voltage monitoring. This is selected by the I/O Mode in BR0 (b4:b3). In this mode, the ADC is programmed to output a linear 8-bit PCM word for the voltage at V_{EXT} which is intended to be read in BR9 (b7:b0). The data format for the ADC output is a "Don't Care" for the sign bit and seven magnitude bits. The scaling for the ADC is for 6.3 V at V_{EXT} equals full scale (BIN X111 1111). The ADPCM algorithm does not support dc signals.

Transmit Digital

The Digital Signal Processor (DSP) section of this device is a custom designed, interrupt driven, microcoded machine optimized for implementing the ADPCM algorithms. In the full duplex speech mode, the DSP services one encode interrupt and one decode interrupt per frame (125 µs). The encode algorithm (i.e., 16 kbps, 24 kbps, or 32 kbps ADPCM, or 64 kbps PCM) is determined by the length of the transmit output enable at the FST pin. The length of the FST enable measured in transmit data clock (BCLKT) cycles tells the device which encoding rate to use. This enable length information is used by the encoder each frame. The transmit ADPCM word corresponding to this request will be computed during the next frame and will be available a total of two frames after being requested. This transmit enable length information can be delayed by the device an additional four frames corresponding to a total of six frames. These six frames of delay allow the device to be clocked with the same clocks for both transmit (encode) and receive (decode), and to be frame aligned for applications that require every sixth frame signaling. It is important to note that the enable length information is delayed and not the actual ADPCM (PCM) sample word. The amount of delay for the FST enable length is controlled in BR7 (b5). If the FST enable goes low before the falling edge of BCLKT during the last bit of the ADPCM word, the digital data output circuitry counts BCLKT cycles to keep the data output (DT pin) low impedance for the duration of the ADPCM data word (2, 3, 4, or 8 BCLKT cycles) minus one half of a BCLKT cycle.

Receive

Receive Digital

The receive digital section of this device accepts serial ADPCM (PCM) words at the DR pin under the control of the BCLKR and FSR pins. The FSR enable duration, measured in BCLKR cycles, tells the device which decode algorithm (i.e.,

16 kbps, 24 kbps, or 32 kbps ADPCM, or 64 kbps PCM) the DSP machine should use for the word that is being received at the DR pin. This algorithm may be changed on a frame by frame basis.

The DSP machine receives an interrupt when an ADPCM word has been received and is waiting to be decoded into a PCM word. The DSP machine performs a decode and an encode every frame when the device is operating in its full duplex conversation mode. The DSP machine decodes the ADPCM word according to CCITT G.726 for 32 kbps, 24 kbps, and 16 kbps. This decoding includes the correction for the CCITT/ANSI Sync function, except when the receive digital gain is used. The receive digital gain is anticipated to be user adjustable gain control in handset applications where as much as 12 dB of gain or more than 12 dB of attenuation may be desirable. The receive digital gain is a linear multiply performed on the 13-bit linear data before it is converted to Mu-Law or A-Law, and is programmed via the SCP port in BR3 (b7:b0). The decoded PCM word may be read via the SCP port in BR10 (b7:b0).

Receive Analog Signal Processing

The receive analog signal processing section includes the DAC described above, a sample and hold amplifier, a trim gain stage, a 5-pole, 3400 Hz switched capacitor low-pass filter with sinX/X correction, and a 2-pole active smoothing filter to reduce the spectral components of the switched capacitor filter. (The receive low-pass smoothing filter may be removed from the signal path for the additional spectral components for applications using the on-chip tone generator function described below. This low-pass filter performs the sinX/X compensation. The receive filter is removed from the circuit via the SCP in BR2 (b4).) The input to the smoothing filter is the output to the receive trim gain stage. This stage is intended to compensate for gain tolerances of external components such as handset receivers. This stage is capable of 0 to 7 dB of attenuation in 1-dB steps. This stage only accommodates attenuation because the nominal signal levels of the DAC should be next to the clip levels of this device's circuitry and any positive gain would overdrive the outputs. The gain is programmed via the SCP port in BR2 (b2:b0).The output of the 2-pole active smoothing filter is buffered by an amplifier which is output at the RO pin. This output is capable of driving a 2 kΩ load to the V_{AG} pin.

Receive Analog Output Drivers and Power Supply

The high current analog output circuitry (PO+, PO–, PI, AXO+, AXO–) is powered by the V_{EXT} power supply pin. Due to the wide range of V_{EXT} operating voltages for this device, this circuitry and the RO pin have a programmable reference point of either V_{AG} (2.4 V) or $V_{EXT}/2$. In applications where this device is powered with 5 V, it is recommended that the dc reference for this circuitry be programmed to V_{AG}. This allows maximum output signals for driving high power telephone line transformer interfaces and loud speaker/ringers. For applications that are battery powered, V_{AG} pin will still be 2.4 V, but the receive analog output circuitry will be powered from as low as 2.7 V. To optimize the output power, this circuitry should be referenced to one half of the battery voltage, $V_{EXT}/2$. The RO pin is powered by the V_{DD} pin, but its dc reference point is programmed the same as the high current analog output circuitry.

This device has two pairs of power amplifiers that are connected in a push-pull configuration. These push-pull power driver pairs have similar drive capabilities, but have different circuit configurations and different intended uses. The PO+ and PO– power drivers are intended to accommodate large gain ranges with precise adjustment by two external resistors for applications such as driving a telephone line or a handset receiver. The PI pin is the inverting input to the PO– power amplifier. The non-inverting input is internally tied to the same reference as the RO output. This allows this amplifier to be used in an inverting gain circuit with two external resistors. The PO+ amplifier has a gain of –1, and is internally connected to the PO– output. This complete power amplifier circuit is a differential (push-pull) amplifier with adjustable gain which is capable of driving a 300 Ω load to +12 dBm when V_{EXT} is 5 V. The PO+ and PO– outputs are intended to drive loads differentially and not to V_{SS} or V_{AG}. The PO+ and PO– power amplifiers may be powered down independently of the rest of the chip by connecting the PI pin to V_{DD} or in BR2 (b5).

The other paired power driver outputs are the AXO+ and AXO–Auxiliary outputs. These push-pull output amplifiers are intended to drive a ringer or loud speaker with impedance as low as 300 Ω to +12 dBm when V_{EXT} is 5 V. The AXO+ and AXO– outputs are intended to drive loads differentially and not to V_{SS} or V_{AG}. The AXO+ and AXO–power amplifiers may be powered down independently of the rest of the chip via the SCP port in BR2 (b6).

SIDETONE

The Sidetone function of this device allows a controlled amount of the output from the transmit filter to be summed with the output of the DAC at the input to the receive low-pass filter. The sidetone component has gains of –8.5 dB, –10.5 dB, –12.0 dB, –13.5 dB, –15.0 dB, –18.0 dB, –21.5 dB, and ≤ –70 dB. The sidetone function is controlled by the SCP port in BR1 (b6:b4).

UNIVERSAL TONE GENERATOR

The Universal Dual Tone Generator function supports both the transmit and the receive sides of this device. When the tone generator is being used, the decoder function of the DSP circuit is disabled. The output of the tone generator is made available to the input of the receive digital gain function for use at the receive analog outputs. In handset applications, this could be used for generating DTMF, distinctive ringing or call progress feedback signals. In telephone line interface applications, this tone generator could be used for signaling on the line. The tone generator output is also available for the input to the encoder function of the DSP machine for outputting at the DT pin. This function is useful in handset applications for non-network signaling such as information services, answering machine control, etc. At the network interface side of a cordless telephone application, this function could be used for dialing feedback or call progress to the handset. The tone generator function is controlled by the SCP port in BR4, BR5, and BR7. The tone generator does not work when the device is operated in 64 kbps mode, except when analog loopback is enabled at BR0 (b5).

POWER DOWN AND RESET

There are two methods of putting all of this device into a low power consumption mode that makes the device nonfunctional and consumes virtually no power. $\overline{\text{PDI/RESET}}$ is the power down input and reset pin which, when taken low, powers down the device. Another way to power the device down is by the SCP port at BR0. BR0 allows the analog section

of this device to be powered down individually and/or the digital section of this device to be powered down individually. When the chip is powered down, the V_{AG}, TG, RO, PO+, PO−, AXO+, AXO−, DT and SCP Tx outputs are high impedance . To return the chip to the power up state, $\overline{PDI/RESET}$ must be high and the SPC clock and the FST or the FSR frame sync pulses must be present. The ADPCM algorithm is reset to the CCITT initial state following the reset transition from low to high logic states. The DT output will remain in a high impedance state for at least two FST pulses after power up. This device is functional after being reset for full-duplex voice coding with the charge pump active.

SIGNAL PROCESSING CLOCK (SPC)

This is the clock that sequences the DSP circuit. This clock may be asynchronous to all other functions of this device. Clock frequencies of 20.48 MHz or 20.736 MHz are recommended. This clock is also used to drive a digitally phase locked prescaler that is referenced to FST (8 kHz) and automatically determines the proper divide ratio to use for achieving the required 256 kHz internal sequencing clock for all analog signal processing, including analog-to-digital conversion, digital-to-analog conversion, transmit filtering, receive filtering and analog gain functions of this device and the charge pump.

The analog sequencing function of the SPC clock may be eliminated by reprogramming the device to use the BCLKR pin as the direct input for the required 256 kHz analog sequencing clock. The 256 kHz clock applied at BCLKR must be an integer 32 times the FST 8 kHz clock and be approximately rising edge aligned with the FST rising edge. This mode requires that the transmit and receive ADPCM transfers be controlled by the BCLKT pin. This is reprogrammed via the SCP port in BR0 (b7).

DIGITAL I/O

The MC145540 is programmable for Mu-Law or A-Law. The timing for the PCM data transfer is independent of the companding scheme selected. Table 1 shows the 8-bit data word format for positive and negative zero and full scale for both 64 kbps companding schemes (see Figures 1 through 5 for a summary and comparison of the five PCM data interface modes of this device).

Long Frame Sync

Long Frame Sync is the industry name for one type of clocking format which controls the transfer of the ADPCM or PCM data words (see Figures 1 through 4). The "Frame Sync" or "Enable" is used for two specific synchronizing functions. The first is to synchronize the PCM data word transfer, and the second is to control the internal analog-to-digital and digital-to-analog conversions. The term "Sync" refers to the function of synchronizing the PCM data word onto or off of the multiplexed serial PCM data bus, also known as a PCM highway. The term "Long" comes from the duration of the frame sync measured in PCM data clock cycles. Long Frame Sync timing occurs when the frame sync is used directly as the PCM data output driver enable. This results in the PCM output going low impedance with the rising edge of the transmit frame sync, and remaining low impedance for the duration of the transmit frame sync.

The implementation of Long Frame Sync for this device has maintained industry compatibility and been optimized for external clocking simplicity. The PCM data output goes low impedance with the rising edge of the FST pin but the MSB of the data is clocked out due to the logical AND of the transmit frame sync (FST pin) with the transmit data clock (BCLKT pin). This allows either the rising edge of the FST enable or the rising edge of the BCLKT data clock to be first. This implementation includes the PCM data output remaining low impedance until the middle of the LSB (seven and a half data clock cycles for 64 kbps PCM, three and a half data clock cycles for 32 kbps ADPCM, etc.). This allows the frame sync to be approximately rising edge aligned with the initiation of the PCM data word transfer but the frame sync does not have a precise timing requirement for the end of the PCM data word transfer. This prevents bus contention between similar devices on a common bus. The device recognizes Long Frame Sync clocking when the frame sync is held high for two consecutive falling edges of the transmit data clock.

In the full duplex speech mode, the DSP services one encode interrupt and one decode interrupt per frame (125 µs). The encode algorithm (i.e., 16 kbps, 24 kbps, or 32 kbps ADPCM or 64 kbps PCM) is determined by the length of the transmit output enable at the FST pin. The length of the FST enable measured in transmit data clock (BCLKT) cycles tells the device which encoding rate to use. This enable length information is used by the encoder each frame. The transmit ADPCM word corresponding to this request will be computed during the next frame and be available a total of two frames after being requested. This transmit enable length information can be delayed by the device an additional four frames corresponding to a total of six frames. This six frames of delay allows the device to be clocked with the same clocks for both transmit (encode) and receive (decode), and to be frame aligned for applications that require every sixth frame signaling. It is important to note that the enable length information is delayed and not the actual ADPCM (PCM) sample word. The amount of delay for the FST enable length is controlled by the SCP port at BR7 (b5). The digital data output circuitry counts BCLKT cycles to keep the data output (DT pin) low impedance for the duration of the ADPCM data word (2, 3, 4, or 8 BCLKT cycles) minus one half of a BCLKT cycle.

Table 1. PCM Full Scale and Zero Words

	Mu-Law			A-Law		
Level	**Sign Bit**	**Chord Bits**	**Step Bits**	**Sign Bit**	**Chord Bits**	**Step Bits**
+ Full Scale	1	0 0 0	0 0 0 0	1	0 1 0	1 0 1 0
+ Zero	1	1 1 1	1 1 1 1	1	1 0 1	0 1 0 1
− Zero	0	1 1 1	1 1 1 1	0	1 0 1	0 1 0 1
− Full Scale	0	0 0 0	0 0 0 0	0	0 1 0	1 0 1 0

The length of the FST enable tells the DSP what encoding algorithm to use. The transmit logic decides on each frame sync whether it should interpret the next frame sync pulse as a Long or a Short Frame Sync. The device is designed to prevent PCM bus contention by not allowing the PCM data output to go low impedance for at least two frame sync cycles after power is applied or when coming out of the power-down mode.

The receive side of the device is designed to accept the same frame sync and data clock as the transmit side and to be able to latch its own transmit PCM data word. Thus the PCM digital switch only needs to be able to generate one type of frame sync for use by both transmit or receive sections of the device.

The logical AND of the receive frame sync with the receive data clock tells the device to start latching the serial word into the receive data input on the falling edges of the receive data clock. The internal receive logic counts the receive data clock falling edges while the FSR enable is high and transfers the enable length and the PCM data word into internal registers for access by the DSP machine which also sets the DSP's decoder interrupt.

The receive digital section of this device accepts serial ADPCM (PCM) words at the DR pin under the control of the BCLKR and FSR pins. The FSR enable duration measured in BCLKR cycles, tells the device which decode algorithm (i.e., 16 kbps, 24 kbps, or 32 kbps ADPCM, or 64 kbps PCM) the DSP machine should use for the word that is being received at the DR pin. This algorithm may be changed on a frame by frame basis.

When the device is programmed to be in the PCM Codec mode by BR0 (4:3), the device will output and input the complete 8-bit PCM words using the long frame sync clocking format as though the FST and FSR pulses were held high for 8 data clock cycles.

The DSP machine receives an interrupt when an ADPCM word has been received and is waiting to be decoded into a PCM word. The DSP machine performs a decode and an encode every frame when the device is operating in its full duplex conversation mode. The DSP machine decodes the ADPCM word according to CCITT G.726 for 32 kbps, 24 kbps, and 16 kbps.

Short Frame Sync

Short Frame Sync is the industry name for this type of clocking format which controls the transfer of the ADPCM data words (see Figure 5). This device uses short frame sync timing for 32 kbps ADPCM only. The "Frame Sync" or "Enable" is used for two specific synchronizing functions. The first is to synchronize the ADPCM data word transfer, and the second is to control the internal analog to digital and digital to analog conversions. The term "Sync" refers to the function of synchronizing the ADPCM data word onto or off of the multiplexed serial ADPCM data bus, also known as a PCM highway. The term "Short" comes from the duration of the frame sync measured in PCM data clock cycles. Short Frame Sync timing occurs when the frame sync is used as a "pre-synchronization" pulse that is used to tell the internal logic to clock out the ADPCM data word under complete control of the data clock. The Short Frame Sync is held high for one falling data clock edge. The device outputs the ADPCM data word beginning with the following rising edge of the data clock. This results in the ADPCM output going low impedance with the rising edge of the transmit data clock, and remaining low impedance until the middle of the LSB (three and a half PCM data clock cycles).

The device recognizes Short Frame Sync clocking when the frame sync is held high for one and only one falling edge of the transmit data clock. The transmit logic decides on each frame sync whether it should interpret the next frame sync pulse as a Long or a Short Frame Sync. It is not recommended to switch between Long Frame Sync and Short Frame Sync clocking without going through a power down cycle due to bus contention problems. The device is designed to prevent PCM bus contention by not allowing the ADPCM data output to go low impedance for at least two frame sync cycles after power is applied or when coming out of a powered down mode.

The receive side of the device is designed to accept the same frame sync and data clock as the transmit side and to be able to latch its own transmit ADPCM data word. Thus the PCM digital switch only needs to be able to generate one type of frame sync for use by both transmit or receive sections of the device.

The falling edge of the receive data clock (BCLKR) latching a high logic level at the receive frame sync (FSR) input tells the device to start latching the 4-bit ADPCM serial word into the receive data input on the following four falling edges of the receive data clock. The internal receive logic counts the receive data clock cycles and transfers the ADPCM data word to a register for access by the DSP.

When the device is programmed to be in the PCM Codec mode by BR0 (4:3), the device will output the complete 8-bit PCM word using the short frame sync clocking format. The 8-bit PCM word will be clocked out (or in) the same way that the 4-bit ADPCM word would be, except that the fourth bit will be valid for the full BCLKT period and the eighth bit will be valid for only one half of the BCLKT period.

SERIAL CONTROL PORT REGISTER MAP

The SCP register map consists of 16 byte registers. Registers BR0–BR5 and BR7–BR10 provide external control of and status of the part. Register BR15 holds the value of the mask number for the particular MC145540. BR6 and BR11–BR14 are not defined and as such are presently reserved.

Table 2. Byte Register Map

Byte	b7	b6	b5	b4	b3	b2	b1	b0
BR0	Ext 256 kHz Clk	MU/A Law Select	Analog Loopback	I/O Mode (1)	I/O Mode (0)	Charge Pump Disable	Analog Power Down	Digital Power Down
BR1	Reserved	Sidetone Gain (2)	Sidetone Gain (1)	Sidetone Gain (0)	Transmit Mute	Transmit Gain (2)	Transmit Gain (1)	Transmit Gain (0)
BR2	RO Reference Select	AXO Enable	PO Disable	Receive Filter Disable	RO Mute	Analog Receive Gain (2)	Analog Receive Gain (1)	Analog Receive Gain (0)
BR3	Digital Rx Gain Enable	Digital Rx Gain (6)	Digital Rx Gain (5)	Digital Rx Gain (4)	Digital Rx Gain (3)	Digital Rx Gain (2)	Digital Rx Gain (1)	Digital Rx Gain (0)
BR4	N.B. Time / Tone Param. (7)	N.B. Time / Tone Param. (6)	N.B. Time / Tone Param. (5)	N.B. Time / Tone Param. (4)	N.B.Time / Tone Param. (3)	N.B. Time / Tone Param. (2)	N.B. Time / Tone Param. (1)	N.B. Time / Tone Param. (0)
BR5	N.B. Threshold (7) / Address Param. (1)	N.B. Threshold (6) / Address Param. (0)	N.B. Threshold (5) / Don't Care	N.B. Threshold (4) / Don't Care	N.B. Threshold (3) / Tone Param. (11)	N.B. Threshold (2) / Tone Param. (10)	N.B. Threshold (1) / Tone Param. (9)	N.B. Threshold (0) / Tone Param. (8)
BR6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR7	Tone Param. Status	N.B. Detect Enable	2/6 Delay	G.726/ Motorola 16 kbps	Tone Enable	Reserved	Tone 1 Enable	Tone 2 Enable
BR8	Software Encoder Reset	Software Decoder Reset	Linear Codec Mode	Highpass Disable	Reserved	Reserved	Reserved	Reserved
BR9	Encoder PCM (7)	Encoder PCM (6)	Encoder PCM (5)	Encoder PCM (4)	Encoder PCM (3)	Encoder PCM (2)	Encoder PCM (1)	Encoder PCM (0)
BR10	D/A PCM (7)	D/A PCM (6)	D/A PCM (5)	D/A PCM (4)	D/A PCM (3)	D/A PCM (2)	D/A PCM (1)	D/A PCM (0)
BR11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR13	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR14	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
BR15	Reserved	Reserved	Reserved	Reserved	Mask (3)	Mask (2)	Mask (1)	Mask (0)

Note: "Setting" a bit corresponds to writing a 1 to the register and "clearing" a bit corresponds to writing a 0 to the register.

APPLICATION CIRCUITS

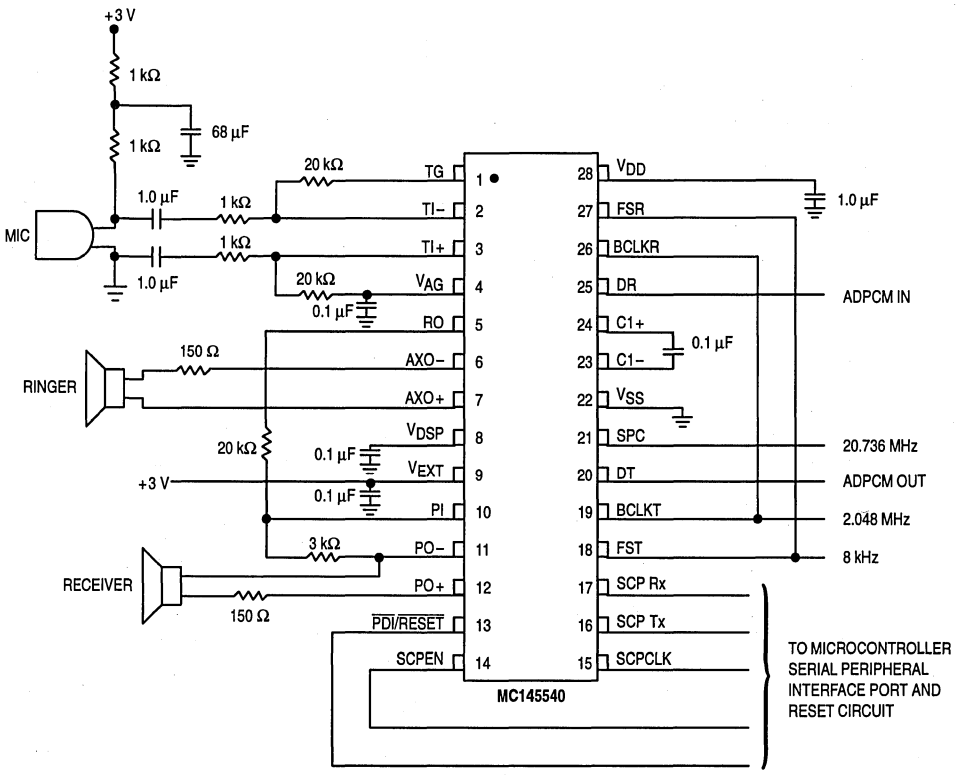


Figure 11. MC145540 Handset Application

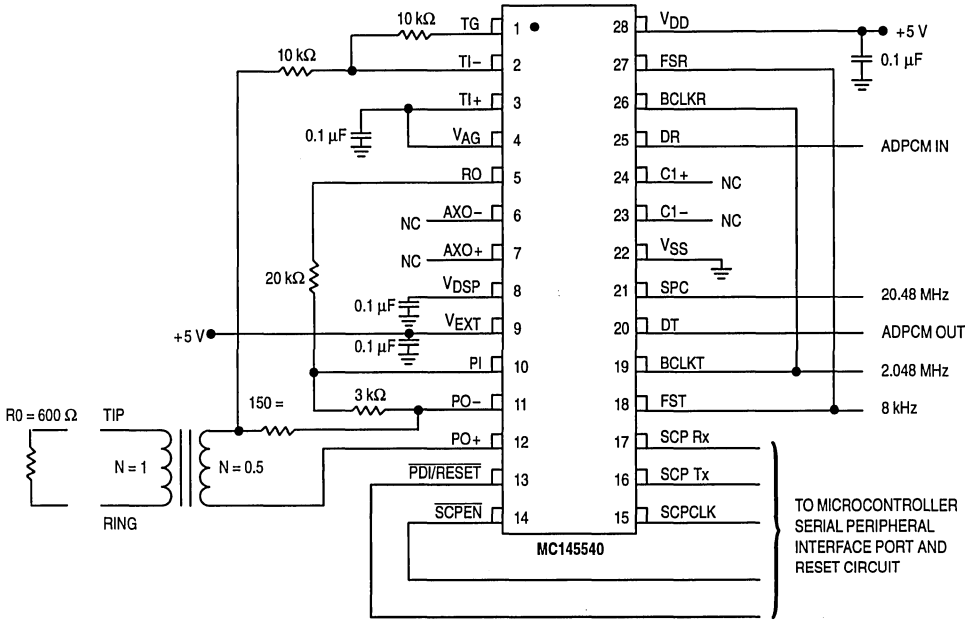


Figure 12. MC145540 Transformer Application

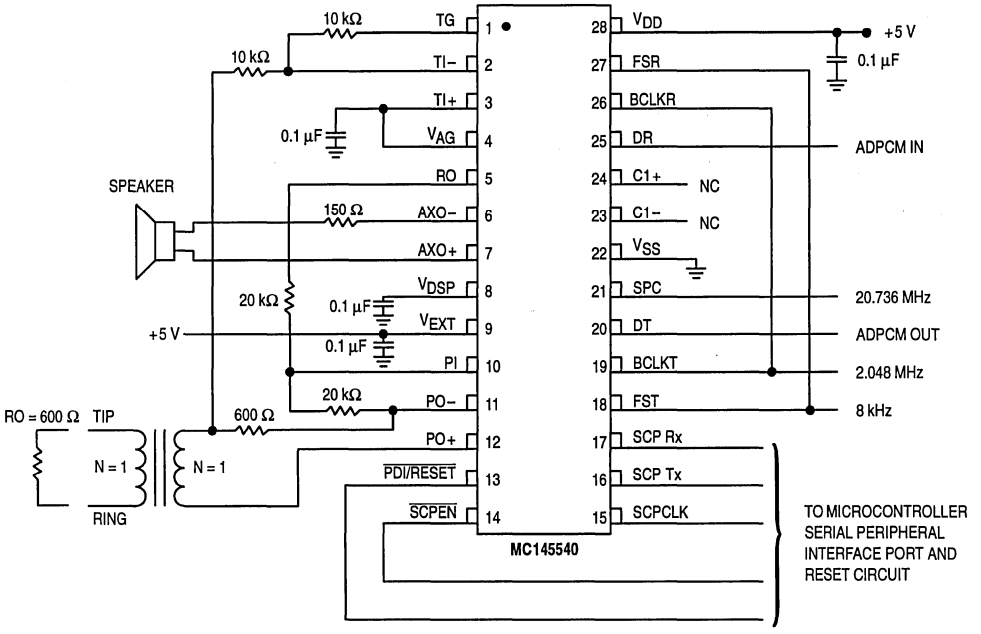


Figure 13. MC145540 Transformer + Speaker Application

MC145542

Product Preview

CT2 Speech and Framing IC

This specification describes a device to be used in a CT2 CAI handset or a single or multi-line base station. It provides three key functions of a CT2 system: voice conversion from analog-to-digital, ADPCM encoding of the voice data, and bit framing for the radio (RF) interface.

The CT2 Speech and Framing circuit (CT2SF) core is a combination of the MC145540 ADPCM/Codec and Time Division Duplex (TDD) bit framing logic.

More details of the architecture of the ADPCM/Codec can be found in the MC145540 data sheet.

- Intended for both fixed and portable applications
- Single 2.7 to 5.25 V Power Supply
- Typical 3 V Power Dissipation of 85 mW, Power Down of 1.2 mW
- Differential Analog Circuit Design for Lowest Noise
- Complete Mu-Law and A-Law Companding PCM Codec-Filter
- ADPCM Transcoder for 64, 32, 24, and 16 kbps Data Rates
- Universal Programmable Dual Tone Generator
- Programmable Transmit Gain, Receive Gain, and Sidetone Gain
- Low Noise, High Gain, Three Terminal Input Op Amp for Microphone Interface
- Push-Pull 300 Ω Power Drivers with External Gain Adjust for Receiver Interface
- Push-Pull 300 Ω Auxiliary Output Drivers for Ringer Interface
- Voltage Regulated Charge Pump to Power the Analog Circuitry in Low Voltage Applications
- Receive Side Noise Burst Detect Algorithm
- Implements Transmit/Receive Bit Framing and D Channel Handler as Defined in CAI spec MPT1375
- Includes D Channel Handler (Parity, CRC, SYNCD, Preamble, ...)
- 8 Bits Parallel Control Port PCP for MCU access of Internal Registers
- Timing Recovery Digital Phase-Locked Loop
- FSK Switched Capacitor Filter with Programmable Attenuation
- External Data Interface Enables Multiplexing of Speech and Data
- 64-Pin PQFP Package

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice. **REV. 1**

MC145554
MC145557
MC145564
MC145567

PCM Codec-Filter

The MC145554, MC145557, MC145564, and MC145567 are all per channel PCM codec-filters. These devices perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. They are designed to operate in both synchronous and asynchronous applications and contain an on-chip precision voltage reference. The MC145554 (Mu-Law) and MC145557 (A-Law) are general purpose devices that are offered in 16-pin packages. The MC145564 (Mu-Law) and MC145567 (A-Law), offered in 20-pin packages, add the capability of analog loop-back and push-pull power amplifiers with adjustable gain.

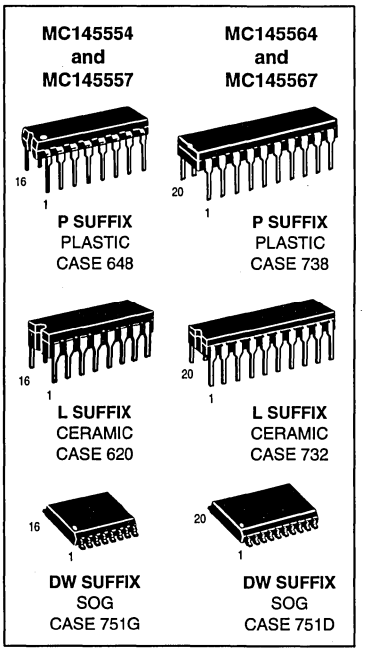
These devices have an input operational amplifier whose output is the input to the encoder section. The encoder section immediately low-pass filters the analog signal with an active R-C filter to eliminate very-high-frequency noise from being modulated down to the pass band by the switched capacitor filter. From the active R-C filter, the analog signal is converted to a differential signal. From this point, all analog signal processing is done differentially. This allows processing of an analog signal that is twice the amplitude allowed by a single-ended design, which reduces the significance of noise to both the inverted and non-inverted signal paths. Another advantage of this differential design is that noise injected via the power supplies is a common-mode signal that is cancelled when the inverted and non-inverted signals are recombined. This dramatically improves the power supply rejection ratio.

After the differential converter, a differential switched capacitor filter band passes the analog signal from 200 Hz to 3400 Hz before the signal is digitized by the differential compressing A/D converter.

The decoder accepts PCM data and expands it using a differential D/A converter. The output of the D/A is low-pass filtered at 3400 Hz and sinX/X compensated by a differential switched capacitor filter. The signal is then filtered by an active R-C filter to eliminate the out of band energy of the switched capacitor filter.

These PCM codec-filters accept both long-frame and short-frame industry standard clock formats. They also maintain compatibility with Motorola's family of TSACs and MC3419/MC34120 SLIC products.

The MC145554/57/64/67 family of PCM codec-filters utilizes CMOS due to its reliable low-power performance and proven capability for complex analog/digital VLSI functions.



MC145554/57 (16-Pin Package)

- Fully Differential Analog Circuit Design for Lowest Noise
- Performance Specified for Extended Temperature Range of – 40 to + 85°C
- Transmit Band-Pass and Receive Low-Pass Filters On-Chip
- Active R-C Pre-Filtering and Post-Filtering
- Mu-Law Companding MC145554
- A-Law Companding MC145557
- On-Chip Precision Voltage Reference (2.5 V)
- Typical Power Dissipation of 40 mW, Power Down of 1.0 mW at ± 5 V

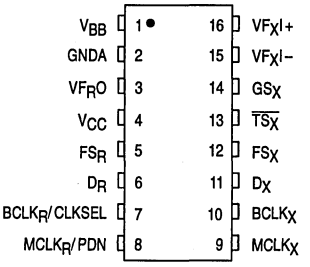
MC145564/67 (20-Pin Package)

All of the Features of the MC145554/57 Plus:

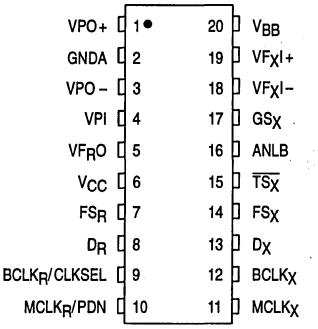
- Mu-Law Companding MC145564
- A-Law Companding MC145567
- Push-Pull Power Drivers with External Gain Adjust
- Analog Loop-Back

PIN ASSIGNMENTS

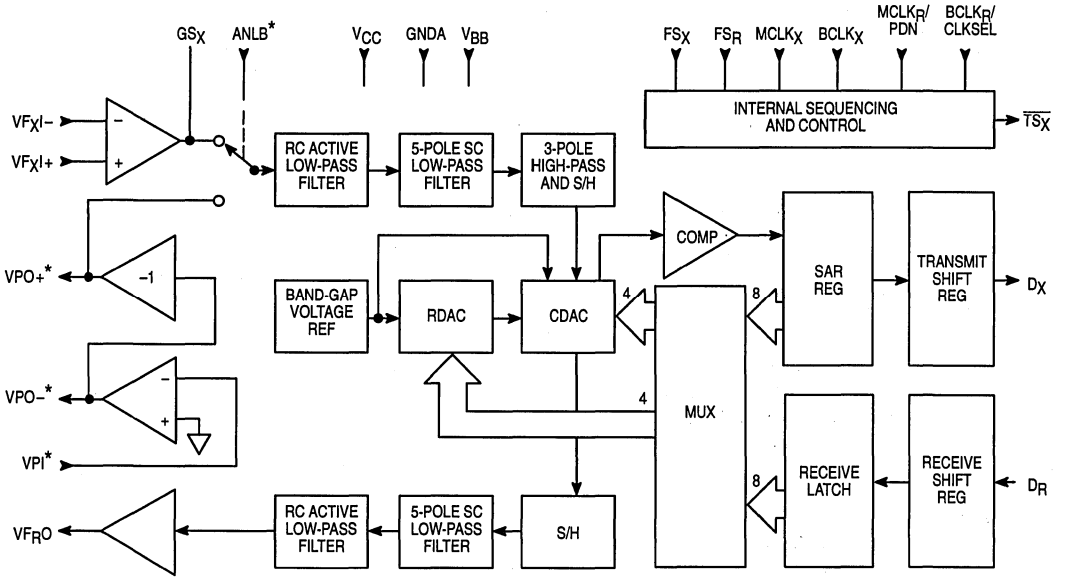
MC145554, MC145557



MC145564, MC145567



FUNCTIONAL BLOCK DIAGRAM



*MC145564 and MC145567 only.

DEVICE DESCRIPTION

A codec-filter is used for digitizing and reconstructing the human voice. These devices were developed primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from "COder" (for the A/D used to digitize voice) and "DECoder" (for the D/A used for reconstructing voice). A codec is a single device that does both the A/D and D/A conversions.

To digitize intelligible voice requires a signal-to-distortion ratio of about 30 dB over a dynamic range of about 40 dB. This can be accomplished with a linear 13-bit A/D and D/A, but will far exceed the required signal-to-distortion ratio at amplitudes greater than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Methods of data reduction are implemented by compressing the 13-bit linear scheme to companded 8-bit schemes. There are two companding schemes used: Mu-255 Law specifically in North America, and A-Law specifically in Europe. These companding schemes are accepted world wide. These companding schemes follow a segmented or "piecewise-linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all sixteen of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits which increment. When the chord bits increment, the step bits double their voltage weighting. This results in an effective resolution of six bits (sign + chord + four step bits) across a 42 dB dynamic range (seven chords above zero, by 6 dB per chord). Tables 3 and 4 show the linear quantization levels to PCM words for the two companding schemes.

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low-pass filter to limit the high frequency energy above 3 kHz from distorting the in-band signal. The telephone line is also subject to 50/60 Hz power line coupling, which must be attenuated from the signal by a high-pass filter before the A/D converter.

The D/A process reconstructs a staircase version of the desired in-band signal, which has spectral images of the in-band signal modulated about the sample frequency and its harmonics. These spectral images, called aliasing components, need to be attenuated to obtain the desired signal. The low-pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The MC145554/57/64/67 PCM codec-filters have the codec, both presampling and reconstruction filters, and a precision voltage reference on chip, and require no external components.

PIN DESCRIPTION

DIGITAL

FS_R
Receive Frame Sync

This is an 8 kHz enable that must be synchronous with $BCLK_R$. Following a rising FS_R edge, a serial PCM word at D_R Is clocked by $BCLK_R$ into the receive data register. FS_R also initiates a decode on the previous PCM word. In the absence of FS_X, the length of the FS_R pulse is used to determine whether the I/O conforms to the short frame sync or long frame sync convention.

D_R
Receive Digital Data Input

$BCLK_R$/CLKSEL
Receive Data Clock and Master Clock Frequency Selector

If this input is a clock, it must be between 128 kHz and 4.096 MHz, and synchronous with FS_R. In synchronous applications this pin may be held at a constant level; then $BCLK_X$ is used as the data clock for both the transmit and receive sides, and this pin selects the assumed frequency of the master clock (see Table 1 in ***Functional Description***).

$MCLK_R$/PDN
Receive Master Clock and Power Down Control

Because of the shared DAC architecture used on these devices, only one master clock is needed. Whenever FS_X is clocking, $MCLK_X$ is used to derive all internal clocks, and the $MCLK_R$/PDN pin merely serves as a power-down control. If $MCLK_R$/PDN pin is held low or is clocked (and at least one of the frame syncs is present), the part is powered up. If this pin is held high, the part is powered down. If FS_X is absent but FS_R is still clocking, the device goes into receive half-channel mode, and $MCLK_R$ (if clocking) generates the internal clocks.

$MCLK_X$
Transmit Master Clock

This clock is used to derive the internal sequencing clocks; it must be 1.536 MHz, 1.544 MHz, or 2.048 MHz.

$BCLK_X$
Transmit Data Clock

$BCLK_X$ may be any frequency between 128 kHz and 4.096 MHz, but it should be synchronous with $MCLK_X$.

D_X
Transmit Digital Data Output

This output is controlled by FS_X and $BCLK_X$ to output the PCM data word; otherwise this pin is in a high-impedance state.

FS_X
Transmit Frame Sync

This is an 8 kHz enable that must be synchronous with $BCLK_X$. A rising FS_X edge initiates the transmission of a serial PCM word, clocked by $BCLK_X$, out of D_X. If the FS_X pulse is high for more than eight $BCLK_X$ periods, the D_X and $\overline{TS_X}$ outputs will remain in a low-impedance state until FS_X is brought low. The length of the FS_X pulse is used to determine whether the transmit and receive digital I/O conforms to the short frame sync or to the long frame sync convention.

$\overline{TS_X}$
Transmit Time Slot Indicator

This is an open-drain output that goes low whenever the D_X output is in a low-impedance state (i.e., during the transmit time slot when the PCM word is being output) for enabling a PCM bus driver.

ANLB
Analog Loop-Back Control Input (MC145564/67 Only)

When held high, this pin causes the input of the transmit RC active filter to be disconnected from GS_X and connected

to VPO+ for analog loop-back testing. This pin is held low in normal operation.

ANALOG

GS_X
Gain-Setting Transmit
This output of the transmit gain-adjust operational amplifier is internally connected to the encoder section of the device. It must be used in conjunction with VF_XI- and VF_XI+ to set the transmit gain for a maximum signal amplitude of 2.5 V peak. This output can drive a 600 Ω load to 2.5 V peak.

VF_XI-
Voice-Frequency Transmit Input (Inverting)
This is the inverting input of the transmit gain-adjust operational amplifier.

VF_XI+
Voice-Frequency Transmit Input (Non-Inverting)
This is the non-inverting input of the transmit gain-adjust operational amplifier.

VF_RO
Voice-Frequency Receive Output
This receive analog output is capable of driving a 600 Ω load to 2.5 V peak.

VPI
Voltage Power Input (MC145564/67 Only)
This is the inverting input to the first receive power amplifier. Both of the receive power amplifiers can be powered down by connecting this input to V_{BB}.

VPO–
Voltage Power Output (Inverted) (MC145564/67 Only)
This inverted output of the receive push-pull power amplifiers can drive 300 Ω to 3.3 V peak.

VPO+
Voltage Power Output (Non-Inverted) (MC145554/67 Only)
This non-inverted output of the receive push-pull power amplifier pair can drive 300 Ω to 3.3 V peak.

POWER SUPPLY

GNDA
Analog Ground
This terminal is the reference level for all signals, both analog and digital. It is 0 V.

V_{CC}
Positive Power Supply
V_{CC} is typically 5 V.

V_{BB}
Negative Power Supply
V_{BB} is typically – 5 V.

FUNCTIONAL DESCRIPTION

ANALOG INTERFACE AND SIGNAL PATH

The transmit portion of these codec/filters includes a low-noise gain setting amplifier capable of driving a 600 Ω load. Its output is fed to a three-pole anti-aliasing pre-filter. This pre-filter incorporates a two-pole Butterworth active low-pass filter, and a single passive pole. This pre-filter is followed by a single ended-to-differential converter that is clocked at 256 kHz. All subsequent analog processing utilizes fully differential circuitry. The next section is a fully-differential, five-pole switched capacitor low-pass filter with a 3.4 kHz passband. After this filter is a 3-pole switched-capacitor high-pass filter having a cutoff frequency of about 200 Hz. This high-pass stage has a transmission zero at dc that eliminates any dc coming from the analog input or from accumulated operational amplifier offsets in the preceding filter stages. The last stage of the high-pass filter is an autozeroed sample and hold amplifier.

One bandgap voltage reference generator and digital-to-analog converter (DAC) are shared by the transmit and receive sections. The autozeroed, switched-capacitor bandgap reference generates precise positive and negative reference voltages that are independent of temperature and power supply voltage. A binary-weighted capacitor array (CDAC) forms the chords of the companding structure, while a resistor string (RDAC) implements the linear steps within each chord. The encode process uses the DAC, the voltage reference, and a frame-by-frame autozeroed comparator to implement a successive-approximation conversion algorithm. All of the analog circuitry involved in the data conversion—the voltage reference, RDAC, CDAC, and comparator—are implemented with a differential architecture.

The receive section includes the DAC described above, a sample and hold amplifier, a five-pole 3400 Hz switched capacitor low-pass filter with sinX/X correction, and a two-pole active smoothing filter to reduce the spectral components of the switched capacitor filter. The output of the smoothing filter is a power amplifier that is capable of driving a 600 Ω load. The MC145564 and MC145567 add a pair of power amplifiers that are connected in a push-pull configuration; two external resistors set the gain of both of the complementary outputs. The output of the second amplifier may be internally connected to the input of the transmit anti-aliasing filter by bringing the ANLB pin high. The power amplifiers can drive unbalanced 300 Ω loads or a balanced 600 Ω load; they may be powered down independent of the rest of the chip by tying the VPI pin to V_{BB}.

MASTER CLOCKS

Since the codec-filter design has a single DAC architecture, only one master clock is used. In normal operation (both frame syncs clocking), the $MCLK_X$ is used as the master clock, regardless of whether the $MCLK_R$/PDN pin is clocking or low. The same is true if the part is in transmit half-channel mode (FS_X clocking, FS_R held low). But if the codec-filter is in the receive half-channel mode, with FS_R clocking and FS_X held low, $MCLK_R$ is used for the internal master clock if it is clocking; if MCLKR is low, then $MCLK_X$ is still used for the internal master clock. Since only one of the master clocks is used at any given time, they need not be synchronous.

The master clock frequency must be 1.536 MHz, 1.544 MHz, or 2.048 MHz. The frequency that the codec-filter expects depends upon whether the part is a Mu-law or an A-law part, and on the state of the $BCLK_R$/CLKSEL pin. The allowable options are shown In Table 1. When a level (rather than a clock) is provided for $BCLK_R$/CLKSEL, $BCLK_X$ is used as the bit clock for both transmit and receive.

Table 1. Master Clock Frequency Determination

$BCLK_R$/CLKSEL	Master Clock Frequency Expected	
	MC145554/64	MC145557/67
Clocked, 1, or Open	1.536 MHz 1.544 MHz	2.048 MHz
0	2.048 MHz	1.536 MHz 1.544 MHz

FRAME SYNCS AND DIGITAL I/O

These codec-filters can accommodate both of the industry standard timing formats. The long frame sync mode is used by Motorola's MC145500 family of codec-filters and the UDLT family of digital loop transceivers. The short frame sync mode is compatible with the IDL (Interchip Digital Link) serial format used in Motorola's ISDN family and by other companies in their telecommunication devices. These codec-filters use the length of the transmit frame sync (FS_X) to determine the timing format for both transmit and receive unless the part is operating in the receive half-channel mode.

In the long frame sync mode, the frame sync pulses must be at least three bit clock periods long. The D_X and $\overline{TS_X}$ outputs are enabled by the logical ANDing of FS_X and $BCLK_X$; when both are high, the sign bit appears at the D_X output. The next seven rising edges of $BCLK_X$ clock out the remaining seven bits of the PCM word. The D_X and $\overline{TS_X}$ outputs return to a high impedance state on the falling edge of the eighth bit clock or the falling edge of FS_X, whichever comes later. The receive PCM word is clocked into D_R on the eight falling $BCLK_R$ edges following an FS_R rising edge.

For short frame sync operation, the frame sync pulses must be one bit clock period long. On the first $BCLK_X$ rising edge after the falling edge of $BCLK_X$ has latched FS_X high, the D_X and $\overline{TS_X}$ outputs are enabled and the sign bit is presented on D_X. The next seven rising edges of $BCLK_X$ clock out the remaining seven bits of the PCM word; on the eighth $BCLK_X$ falling edge, the D_X and $\overline{TS_X}$ outputs return to a high impedance state. On the second falling $BCLK_R$ edge following an FS_R rising edge, the receive sign bit is clocked into D_R. The next seven $BCLK_R$ falling edges clock in the remaining seven bits of the receive PCM word.

Table 2 shows the coding format of the transmit and receive PCM words.

HALF-CHANNEL MODES

In addition to the normal full duplex operating mode, these codec-filters can operate in both transmit and receive half-channel modes. Transmit half-channel mode is entered by holding FS_R low. The VF_RO output goes to analog ground but remains in a low impedance state (to facilitate a hybrid interface); PCM data at D_R is ignored. Holding FS_X low while clocking FS_R puts these devices in the receive half-channel mode. In this state, the transmit input operational amplifier continues to operate, but the rest of the transmit circuitry is disabled; the D_X and $\overline{TS_X}$ outputs remain in a high impedance state. $MCLK_R$ is used as the internal master clock if it is clocking. If $MCLK_R$ is not clocking, then $MCLK_X$ is used for the internal master clock, but in that case it should be synchronous with FS_R. If $BCLK_R$ is not clocking, $BCLK_X$ will be used for the receive data, just as in the full channel operating mode. In receive half-channel mode only, the length of the FS_R pulse is used to determine whether short frame sync or long frame sync timing is used at D_R.

POWER DOWN

Holding both FS_X and FS_R low causes the part to go into the power down state. Power down occurs approximately 2 ms after the last frame sync pulse is received. An alternative way to put these devices in power down is to hold the $MCLK_R$/ PDN pin high. When the chip is powered down, the D_X, $\overline{TS_X}$, and GS_X outputs are high impedance, the VF_RO, VPO–, and VPO+ operational amplifiers are biased with a trickle current so that their respective outputs remain stable at analog ground. To return the chip to the power up state, $MCLK_R$/PDN must be low or clocking and at least one of the frame sync pulses must be present. The D_X and $\overline{TS_X}$ outputs will remain in a high-impedance state until the second FS_X pulse after power up.

Table 2. PCM Data Format

	Mu-Law (MC145554/64)			A-Law (MC145557/67)		
Level	Sign Bit	Chord Bits	Step Bits	Sign Bit	Chord Bits	Step Bits
+ Full Scale	1	000	0000	1	010	1010
+ Zero	1	111	1111	1	101	0101
– Zero	0	111	1111	0	101	0101
– Full Scale	0	000	0000	0	010	1010

MAXIMUM RATINGS (Voltage Referenced to GNDA)

Rating		Symbol	Value	Unit
DC Supply Voltage	V_{CC} to V_{BB} V_{CC} to GNDA V_{BB} to GNDA		−0.5 to +13 −0.3 to +7.0 −7.0 to +0.3	V
Voltage on Any Analog Input or Output Pin			V_{BB} − 0.3 to V_{CC} + 0.3	V
Voltage on Any Digital Input or Output Pin			GNDA − 0.3 to V_{CC} + 0.3	V
Operating Temperature Range		T_A	−40 to +85	°C
Storage Temperature Range		T_{stg}	−85 to +150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., V_{BB}, GNDA, or V_{CC}).

POWER SUPPLY (T_A = − 40 to + 85°C)

Characteristic		Min	Typ	Max	Unit
DC Supply Voltage	V_{CC} V_{BB}	4.75 −4.75	5.0 −5.0	5.25 −5.25	V
Active Power Dissipation (No Load)	MC145554/57 MC145564/67 MC145564/67, VPI = V_{BB}	— — —	40 45 40	60 70 60	mW
Power Down Dissipation (No Load)	MC145554/57 MC145564/67 MC145564/67, VPI = V_{BB}	— — —	1.0 2.0 1.0	3.0 5.0 3.0	mW

DIGITAL LEVELS (V_{CC} = 5 V ± 5%, V_{BB} = − 5 V ± 5%, GNDA = 0 V, T_A = − 40 to + 85°C)

Characteristic		Symbol	Min	Max	Unit
Input Low Voltage		V_{IL}	—	0.6	V
Input High Voltage		V_{IH}	2.2	—	V
Output Low Voltage	D_X or $\overline{TS_X}$, I_{OL} = 3.2 mA	V_{OL}	—	0.4	V
Output High Voltage	D_X, I_{OH} = − 3.2 mA I_{OH} = − 1.6 mA	V_{OH}	2.4 V_{CC} − 0.5	— —	V
Input Low Current	GNDA ≤ V_{in} ≤ V_{CC}	I_{IL}	−10	+10	μA
Input High Current	GNDA ≤ V_{in} ≤ V_{CC}	I_{IH}	−10	+10	μA
Output Current in High Impedance State	GNDA ≤ D_X ≤ V_{CC}	I_{OZ}	−10	+10	μA

ANALOG ELECTRICAL CHARACTERISTICS

(V_{CC} = + 5 V ± 5%, V_{BB} = −5 V ± 5%, VF_XI- Connected to GS_X, T_A = −40 to +85°C)

Characteristic		Min	Typ	Max	Unit
Input Current (− 2.5 ≤ V_{in} ≤ + 2.5 V)	VF_XI+, VF_XI-	—	±0.05	±0.2	µA
AC Input Impedance to GNDA (1 kHz)	VF_XI+, VF_XI-	10	20	—	MΩ
Input Capacitance	VF_XI+, VF_XI-	—	—	10	pF
Input Offset Voltage of GS_X Op Amp	VF_XI+, VF_XI-	—	—	±25	mV
Input Common Mode Voltage Range	VF_XI+, VF_XI-	−2.5	—	2.5	V
Input Common Mode Rejection Ratio	VF_XI+, VF_XI-	—	65	—	dB
Unity Gain Bandwidth of GS_X Op Amp (R_{load} ≥ 10 kΩ)		—	1000	—	kHz
DC Open Loop Gain of GS_X Op Amp (R_{load} ≥ 10 kΩ)		75	—	—	dB
Equivalent Input Noise (C-Mess) Between VF_XI+ and VF_XI- at GS_X		—	−20	—	dBrnC0
Output Load Capacitance for GS_X Op Amp		0	—	100	pF
Output Voltage Range for GS_X	R_{load} = 10 kΩ to GNDA R_{load} = 600 Ω to GNDA	−3.5 −2.8	— —	+3.5 +2.8	V
Output Current (− 2.8 V ≤ V_{out} ≤ + 2.8 V)	GS_X, VF_RO	±5.0	—	—	mA
Output Impedance VF_RO (0 to 3.4 kHz)		—	1	—	Ω
Output Load Capacitance for VF_RO		0	—	500	pF
VF_RO Output DC Offset Voltage Referenced to GNDA		—	—	±100	mV
Transmit Power Supply Rejection	Positive, 0 to 100 kHz, C-Message Negative, 0 to 100 kHz, C-Message	45 45	— —	— —	dBC
Receive Power Supply Rejection	Positive, 0 to 100 kHz, C-Message Positive, 4 kHz to 25 kHz Positive, 25 kHz to 50 kHz Negative, 0 to 100 kHz, C-Message Negative, 4 kHz to 25 kHz Negative, 25 kHz to 50 kHz	50 50 43 50 45 38	— — — — — —	— — — — — —	dBC dB dB dBC dB dB
MC145564/67 Power Drivers					
Input Current (− 1 V ≤ VPI ≤ + 1 V)	VPI	—	±0.05	±0.5	µA
Input Resistance (− 1 V ≤ VPI ≤ + 1 V)	VPI	5	10	—	MΩ
Input Offset Voltage (VPI Connected to VPO−)	VPI	—	—	±50	mV
Output Resistance, Inverted Unity Gain	VPO+ or VPO−	—	1	—	Ω
Unity Gain Bandwidth, Open Loop	VPO−	—	400	—	kHz
Load Capacitance (∞ Ω ≥ R_{load} ≥ 300 Ω)	VPO+ or VPO− to GNDA	0	—	1000	pF
Gain from VPO− to VPO+ (R_{load} = 300 Ω, VPO+ to GNDA Level at VPO− = 1.77 Vrms, +3 dBm0)		—	−1	—	V/V
Maximum 0 dBm0 Level for Better than ± 0.1 dB Linearity Over the Range −10 dBm0 to +3 dBm0 (For R_{load} between VPO+ and VPO−)	R_{load} = 600 Ω R_{load} = 1200 Ω R_{load} = 10 kΩ	3.3 3.5 4.0	— — —	— — —	Vrms
Power Supply Rejection of V_{CC} or V_{BB} (VPO− Connected to VPI) VPO+ or VPO− to GNDA	0 to 4 kHz 4 to 50 kHz	55 35	— —	— —	dB
Differential Power Supply Rejection of V_{CC} or V_{BB} (VPO− Connected to VPI)	VPO+ to VPO−, 0 to 50 kHz	50	—	—	dB

ANALOG TRANSMISSION PERFORMANCE

(V_{CC} = +5 V ± 5%, V_{BB} = −5 V ± 5%, GNDA = 0 V, 0 dBm0 = 1.2276 Vrms = +4 dBm @ 600 Ω, FS_X = FS_R = 8 kHz, $BCLK_X$ = $MCLK_X$ = 2.048 MHz Synchronous Operation, VF_XI- Connected to GS_X, T_A = − 40 to + 85°C Unless Otherwise Noted)

Characteristic		End-to-End Min	End-to-End Max	A/D Min	A/D Max	D/A Min	D/A Max	Unit
Absolute Gain (0 dBm0 @ 1.02 kHz, T_A = 25°C, V_{CC} = 5 V, V_{BB} = − 5 V)		—	—	−0.25	+0.25	−0.25	+0.25	dB
Absolute Gain Variation with Temperature	0 to 70°C	—	—	—	±0.03	—	±0.03	dB
	− 40 to + 85°C	—	—	—	±0.06	—	±0.06	
Absolute Gain Variation with Power Supply (V_{CC} = 5 V, ± 5%, V_{BB} = − 5 V, ± 5%)		—	—	—	±0.02	—	±0.02	dB
Gain vs Level Tone (Relative to − 10 dBm0, 1.02 kHz)	+ 3 to − 40 dBm0	−0.4	+0.4	−0.2	+0.2	−0.2	+0.2	dB
	− 40 to − 50 dBm0	−0.8	+0.8	−0.4	+0.4	−0.4	+0.4	
	− 50 to − 55 dBm0	−1.6	+1.6	−0.8	+0.8	−0.8	+0.8	
Gain vs Level Pseudo Noise CCITT G.712	− 10 to − 40 dBm0	—	—	−0.25	+0.25	−0.25	+0.25	dB
(MC145557/67 A-Law Relative to − 10 dBm0)	− 40 to − 50 dBm0	—	—	−0.30	+0.30	−0.30	+0.30	
	− 50 to − 55 dBm0	—	—	−0.45	+0.45	−0.45	+0.45	
Total Distortion, 1.02 kHz Tone (C-Message)	+ 3 dBm0	33	—	33	—	33	—	dBC
	0 to − 30 dBm0	35	—	36	—	36	—	
	− 40 dBm0	29	—	30	—	30	—	
	− 45 dBm0	24	—	25	—	25	—	
	− 55 dBm0	15	—	15	—	15	—	
Total Distortion With Pseudo Noise CCITT G.714	− 3 dBm0	27.5	—	28	—	28.5	—	dB
(MC145557/67 A-Law)	− 6 to − 27 dBm0	35	—	35.5	—	36	—	
	− 34 dBm0	33.1	—	33.5	—	34.2	—	
	− 40 dBm0	28.2	—	28.5	—	30	—	
	− 55 dBm0	13.2	—	13.5	—	15	—	
Idle Channel Noise (For End-End and A/D, Note 1)								
(MC145554/64 Mu-Law, C-Message Weighted)		—	15	—	15	—	7	dBrnC0
(MC145557/67 A-Law, Psophometric Weighted)		—	−70	—	−70	—	−83	dBm0p
Frequency Response (Relative to 1.02 kHz @ 0 dBm0)	15 Hz	—	−40	—	−40	−0.15	0	dB
	50 Hz	—	−30	—	−30	−0.15	0	
	60 Hz	—	−26	—	−26	−0.15	0	
	200 Hz	—	—	−1.0	−0.4	−0.15	0	
	300 to 3000 Hz	−0.3	+0.3	−0.15	+0.15	−0.15	+0.15	
	3300 Hz	−0.70	+0.3	−0.35	+0.15	−0.35	+0.15	
	3400 Hz	−1.6	0	−0.8	0	−0.8	0	
	4000 Hz	—	−28	—	−14	—	−14	
	4600 Hz	—	−60	—	−32	—	−30	
In-Band Spurious (1.02 kHz @ 0 dBm0, Transmit and Receive)	300 to 3000 Hz	—	−48	—	−48	—	−48	dBm0
Out-of-Band Spurious at VF_RO (300–3400 Hz @ 0 dBm0 In)								dB
	4600 to 7600 Hz	—	−30	—	—	—	−30	
	7600 to 8400 Hz	—	−40	—	—	—	−40	
	8400 to 100,000 Hz	—	−30	—	—	—	−30	
Idle Channel Noise Selective (8 kHz, Input = GNDA, 30 Hz Bandwidth)		—	−70	—	—	—	−70	dBm0
Absolute Delay (1600 Hz)		—	—	—	315	—	215	µs
Group Delay Referenced to 1600 Hz	500 to 600 Hz	—	—	—	220	−40	—	µs
	600 to 800 Hz	—	—	—	145	−40	—	
	800 to 1000 Hz	—	—	—	75	−40	—	
	1000 to 1600 Hz	—	—	—	40	−30	—	
	1600 to 2600 Hz	—	—	—	75	—	90	
	2600 to 2800 Hz	—	—	—	105	—	125	
	2800 to 3000 Hz	—	—	—	155	—	175	
Crosstalk of 1020 Hz @ 0 dBm0 from A/D or D/A (Note 2)		—	—	—	−75	—	−75	dB
Intermodulation Distortion of Two Frequencies of Amplitudes −4 to −21 dBm0 from the Range 300 to 3400 Hz		—	−41	—	−41	—	−41	dB

NOTES:
1. Extrapolated from a 1020 Hz @ −50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while the A/D is stimulated with 2667 Hz @ −50 dBm0.

DIGITAL SWITCHING CHARACTERISTICS

V_{CC} = 5 V ± 5%, V_{BB} = – 5 V ± 5%, GNDA = 0 V, All Signals Referenced to GNDA; T_A = – 40 to + 85°C, C_{load} = 150 pF Unless Otherwise Noted

Characteristic		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	$MCLK_X$ or $MCLK_R$	f_M	— — —	1.536 1.544 2.048	— — —	MHz
Minimum Pulse Width High or Low	$MCLK_X$ or $MCLK_R$	$t_{w(M)}$	100	—	—	ns
Minimum Pulse Width High or Low	$BCLK_X$ or $BCLK_R$	$t_{w(B)}$	50	—	—	ns
Minimum Pulse Width Low	FS_X or FS_R	$t_{w(FL)}$	50	—	—	ns
Rise Time for all Digital Signals		t_r	—	—	50	ns
Fall Time for all Digital Signals		t_f	—	—	50	ns
Bit Clock Data Rate	$BCLK_X$ or $BCLK_R$	f_B	128	—	4096	kHz
Setup Time from $BCLK_X$ Low to $MCLK_R$ High		$t_{su(BRM)}$	50	—	—	ns
Setup Time from $MCLK_X$ High to $BCLK_X$ Low		$t_{su(MFB)}$	20	—	—	ns
Hold Time from $BCLK_X$ ($BCLK_R$) Low to FS_X (FS_R) High		$t_{h(BF)}$	20	—	—	ns
Setup Time for FS_X (FS_R) High to $BCLK_X$ ($BCLK_R$) Low for Long Frame		$t_{su(FB)}$	80	—	—	ns
Delay Time from $BCLK_X$ High to D_X Data Valid		$t_{d(BD)}$	20	60	140	ns
Delay Time from $BCLK_X$ High to $\overline{TS_X}$ Low		$t_{d(BTS)}$	20	50	140	ns
Delay Time from the 8th $BCLK_X$ Low of FS_X Low to D_X Output Disabled		$t_{d(ZC)}$	50	70	140	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever is Later		$t_{d(ZF)}$	20	60	140	ns
Setup Time from D_R Valid to $BCLK_X$ Low		$t_{su(DB)}$	0	—	—	ns
Hold Time from $BCLK_R$ Low to D_R Invalid		$t_{h(BD)}$	50	—	—	ns
Setup Time from FS_X (FS_R) High to $BCLK_X$ ($BCLK_R$) Low in Short Frame		$t_{su(F)}$	50	—	—	ns
Hold Time from $BCLK_X$ ($BCLK_R$) Low to FS_X (FS_R) Low in Short Frame		$t_{h(F)}$	50	—	—	ns
Hold Time from 2nd Period of $BCLK_X$ ($BCLK_R$) Low to FS_X (FS_R) Low in Long Frame		$t_{h(BFI)}$	50	—	—	ns

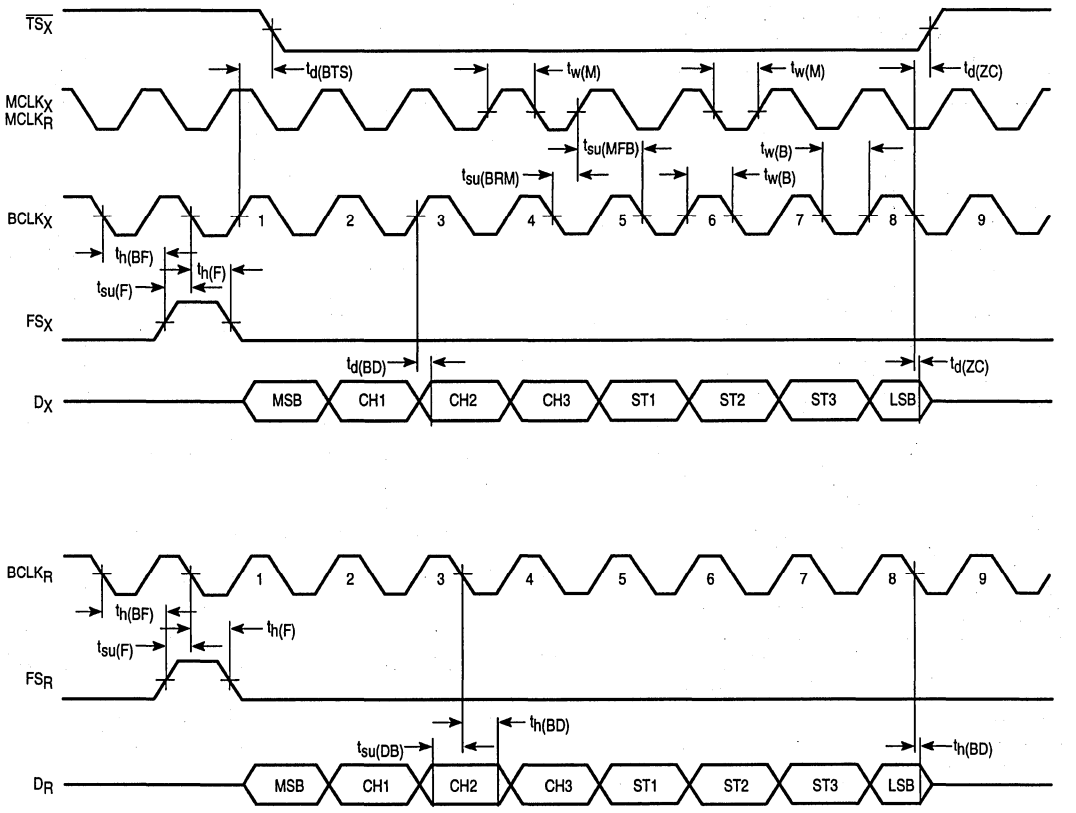


Figure 1. Short Frame Sync Timing

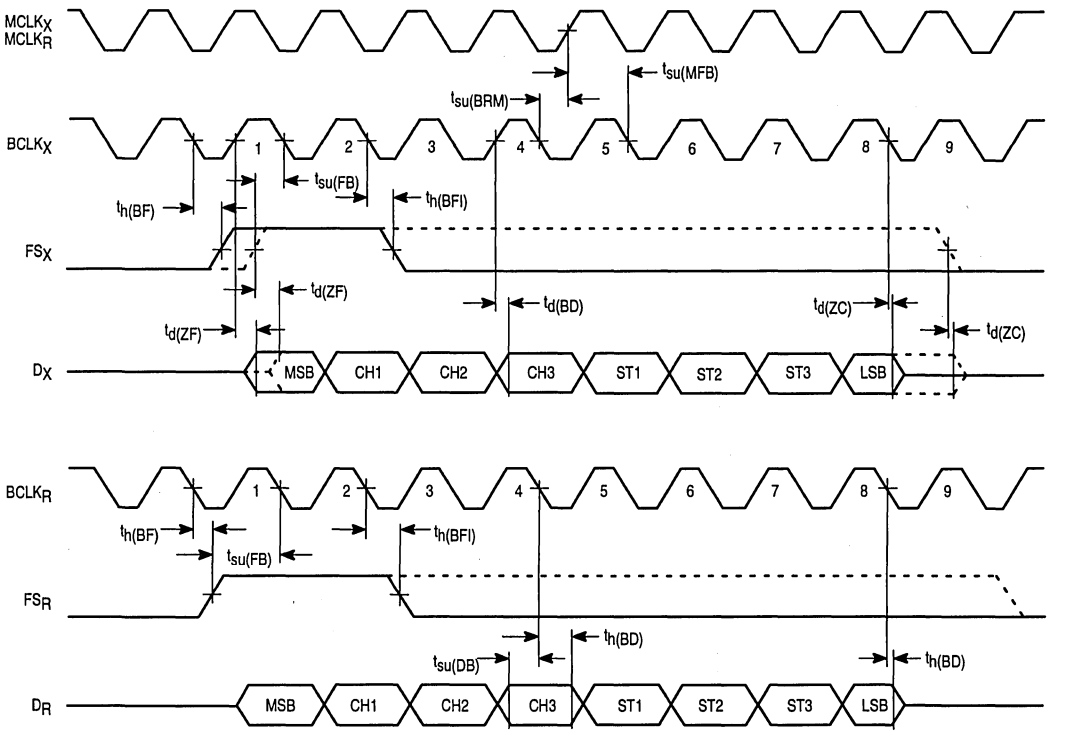


Figure 2. Long Frame Sync Timing

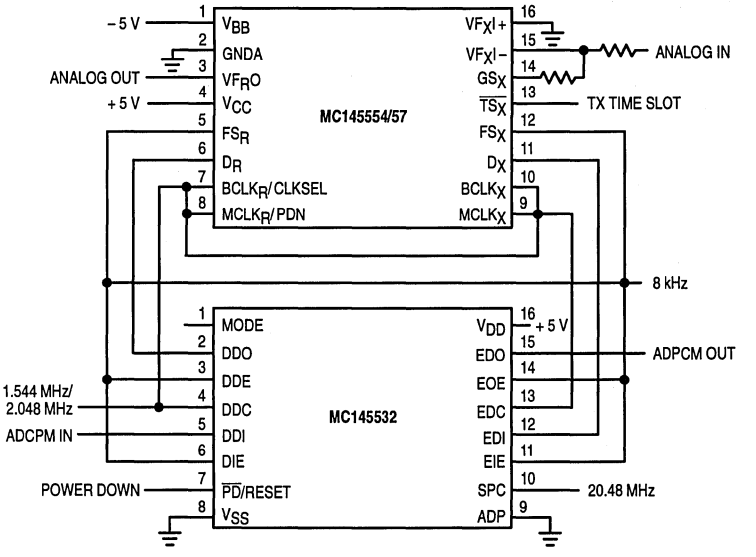
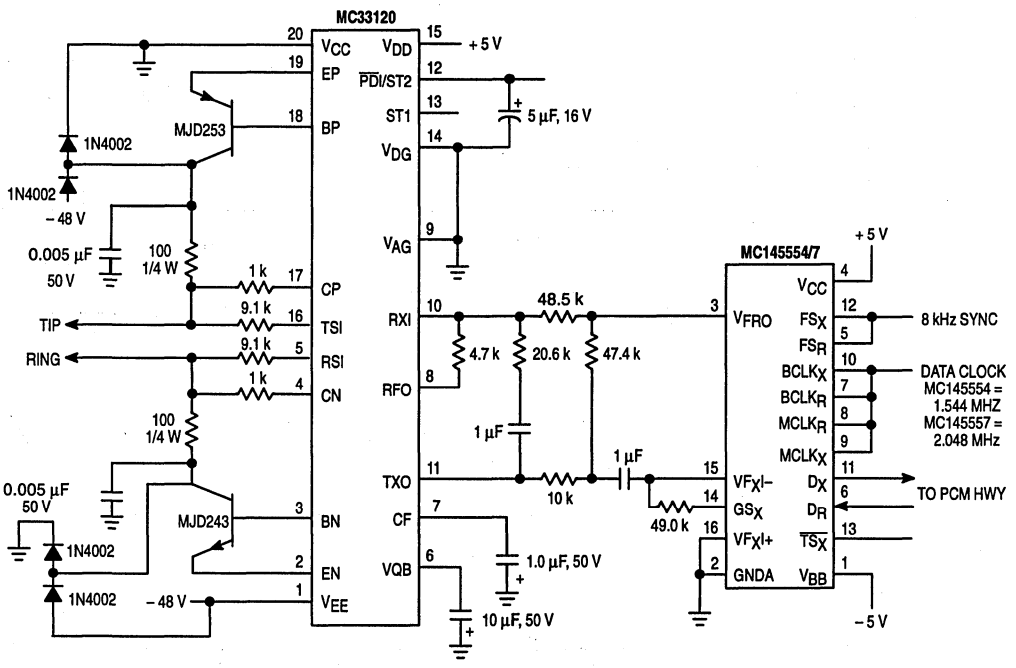


Figure 3. ADPCM Transcoder Application



NOTE: Six resistors and two capacitors can be 5% tolerance.

Figure 4. A Complete Single Party Channel Unit Using MC145554/57 PCM Codec/Filter and MC33120 SLIC

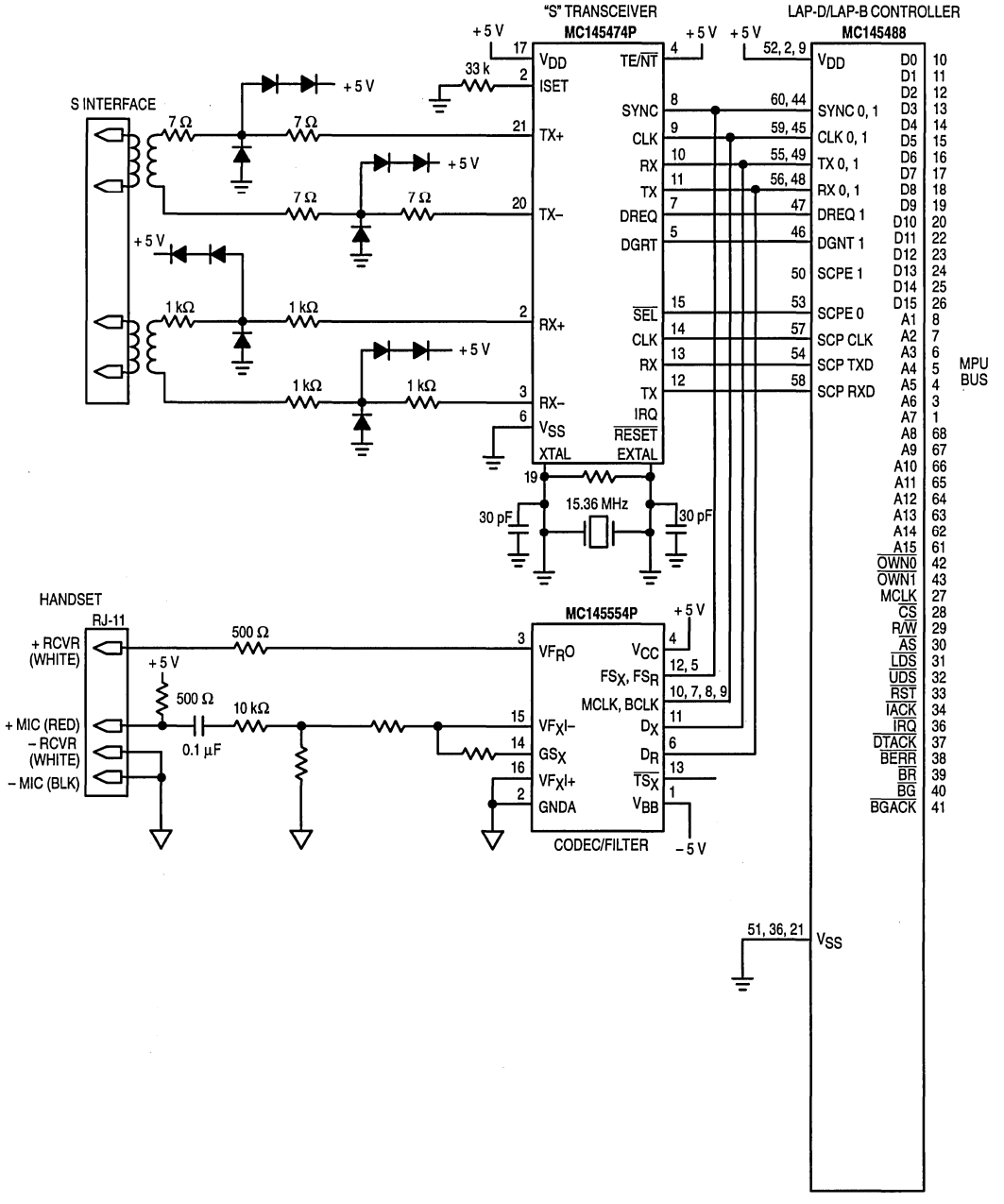


Figure 5. ISDN Voice/Data Terminal

Table 3. Mu-Law Encode-Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			8159									
8	16	256	7903	1	0	0	0	0	0	0	0	8031
			⋮					⋮				⋮
			4319	1	0	0	0	1	1	1	1	4191
7	16	128	4063					⋮				⋮
			2143	1	0	0	1	1	1	1	1	2079
6	16	64	2015					⋮				⋮
			1055	1	0	1	0	1	1	1	1	1023
5	16	32	991					⋮				⋮
			511	1	0	1	1	1	1	1	1	495
4	16	16	479					⋮				⋮
			239	1	1	0	0	1	1	1	1	231
3	16	8	223					⋮				⋮
			103	1	1	0	1	1	1	1	1	99
2	16	4	95					⋮				⋮
			35	1	1	1	0	1	1	1	1	33
1	15	2	31					⋮				⋮
			3	1	1	1	1	1	1	1	0	2
	1	1	1	1	1	1	1	1	1	1	1	0
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inverison of all magnitude bits.

Table 4. A-Law Encode-Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			4096									
7	16	128	3968	1	0	1	0	1	0	1	0	4032
			⋮					⋮				⋮
			2176	1	0	1	0	0	1	0	1	2112
			2048									
6	16	64	⋮					⋮				⋮
			1088	1	0	1	1	0	1	0	1	1056
			1024									
5	16	32	⋮					⋮				⋮
			544	1	0	0	0	0	1	0	1	528
			512									
4	16	16	⋮					⋮				⋮
			272	1	0	0	1	0	1	0	1	264
			256									
3	16	8	⋮					⋮				⋮
			136	1	1	1	0	0	1	0	1	132
			128									
2	16	4	⋮					⋮				⋮
			68	1	1	1	1	0	1	0	1	66
			64									
1	32	2	⋮					⋮				⋮
			2	1	1	0	1	0	1	0	1	1
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes alternate bit inversion, as specified by CCITT.

MC145572

Product Preview

ISDN U-Interface Transceiver II

The MC145572 is a second generation Integrated Services Digital Network U-Interface Basic Access Transceiver. The MC145572 is an enhancement of the MC145472/MC14LC5472 with low power consumption, fewer pins, fewer external components, and increased digital interface functionality. It provides 144 kbps full duplex data transmission on twisted pair loops up to 18,000 feet or 5.5 km in length.

- Single Chip 2B1Q, Echo Cancelling, Adaptively Equalized Transceiver
- Conforms to the ANSI T1.601, "... ISDN Basic Access Interface for Application for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification)" and to ETSI Standards
- Extended Maintenance Functions Provided Through Control Interface
- Automatic Embedded Operations Channel Mode
- All Maintenance Functions are Provided on Chip
- Pin Selectable LT/NT Mode of Operation
- Low Power CMOS
- Maximum 300 mW Power Consumption When Activated
- 44-Lead Surface Mount Package
- Selectable Between IDL and GCI Interfaces
- Six Programmable Timeslot Assigners
- 8-kHz Reference Clock Input
- Serial or Parallel Control Interfaces
- Optional D Channel Interface
- Optional Access to D Channel Through Control Interface
- Software Compatible with MC145472/MC14LC5472
- IDL Data Alignable to U-Interface Superframe for Transmit and Receive
- Fewer External Components in Line Interface Circuit
- Voltage Controlled Crystal Oscillator only Requires an External Crystal

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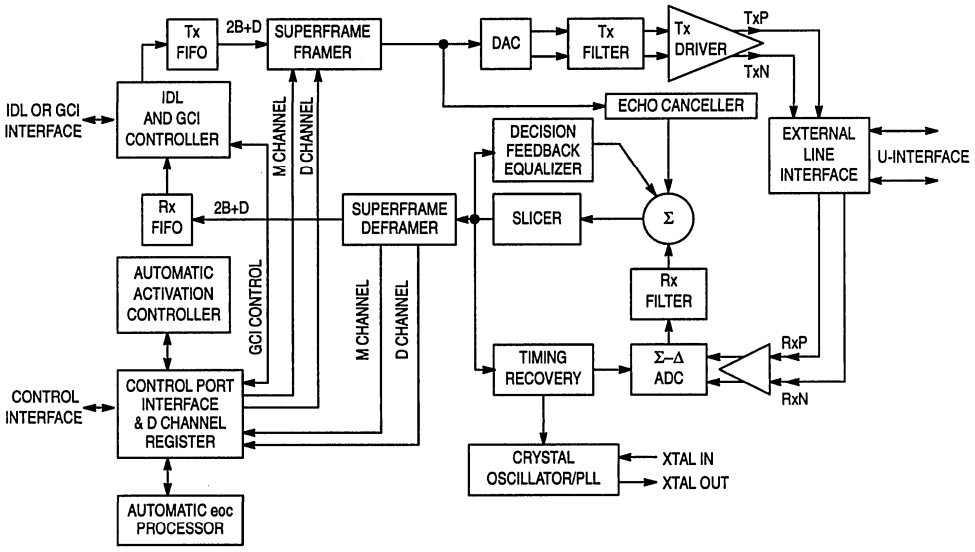
MC145572 BLOCK DIAGRAM



MC145574

Product Preview

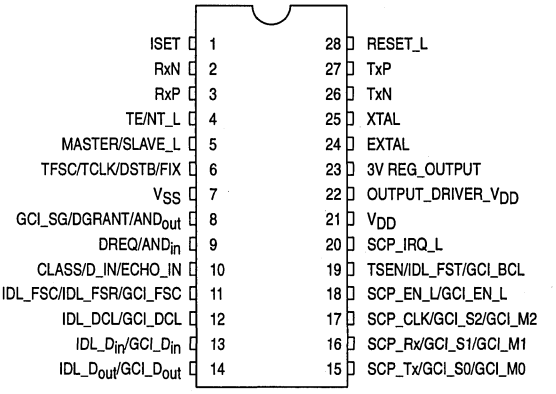
ISDN S/T Interface Transceiver II

The MC145574 is the Motorola second generation ISDN S/T Interface Transceiver. The MC145574 provides an economical VLSI Layer 1 interface for the transportation of two 64 kpbs B channels and one 16 kbps D channel between the network termination (NT) and terminal equipment (TE) applications. The MC145574 conforms to CCITT I.430 and ANSI T1.605 specifications.

The MC145574 provides the modulation line drive and demodulation/line receive functions required of the interface. In addition, the MC145574 provides the activation/deactivation, error monitoring, framing, bit, and octet timing. The MC145574 provides the control signals for the interface to the Layer 2 devices. Complete multiframe capability is provided.

- Backwards compatible with the MC145475
- Conforms to CCITT I.430 and ANSI T1.605 Specifications
- Detects Far-End Code Violations (FECVs) in the NT Mode
- Pin Selectable NT or TE Modes of Operation
- Industry Standard Microprocessor SCP Interface
- Incorporates IDL and IDL2 Interfaces
- Supports 1:2.5 Transformers for Transmit and Receive
- IDL2 Interface has Time Slot Assignment Capability
- GCI Compatible (General Circuit Interface)
- Supports Full Range of S/T and IDL Loopbacks
- Enhanced S&Q Multiframing Capability
- Reduced Power Consumption
- NT1 Star Mode of Operation
- Incorporates all the Features of the MC145474
- Supports TE Slave/Slave Mode for PBX Applications
- Supports NT Terminal Mode for NT1/TA Applications

PIN ASSIGNMENT



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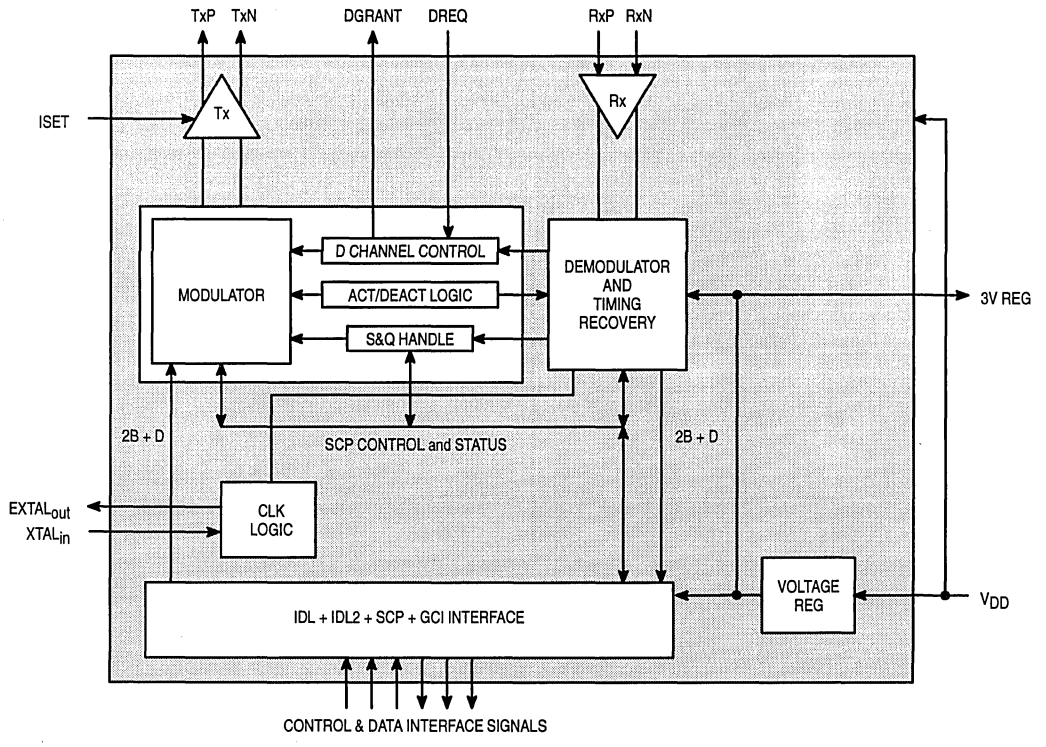
MC145574 BLOCK DIAGRAM

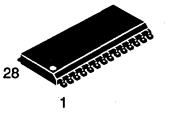


MC145583

Product Preview

3.3-Volt-Only Driver/Receiver With an Integrated Standby Mode

EIA-232E and CCITT V.28



DW SUFFIX
SOG
CASE 751F

The MC145583 is a CMOS transceiver composed of three drivers and five receivers that fulfills the electrical specifications of EIA-232E, EIA-562, and CCITT V.28 while operating from a single +3.3 or +5.0 V power supply. This transceiver is a high-performance, low-power consumption device that is equipped with a Standby function.

A voltage tripler and inverter converts the +3.3 V to ±8.8 V, or a voltage doubler and inverter converts the +5.0 V to ±8.8 V. This is accomplished through an on-board 40 kHz oscillator and five inexpensive external electrolytic capacitors.

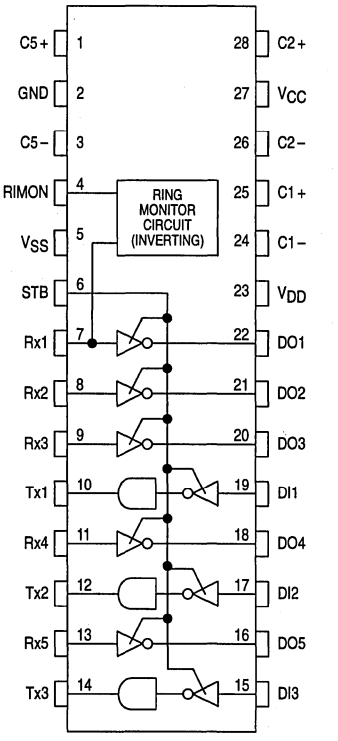
Drivers:
- ±6.0 Output Swing at 3.3 or 5.0 V power supply
- 300 Ω, Power-Off Impedance
- Output Current Limiting
- Three-State Outputs During Standby Mode

Receivers:
- ±25 V Input Range
- 3 to 7 kΩ Input Impedance
- 0.8 V Hysteresis for Enhanced Noise Immunity
- Three-State Outputs During Standby Mode

Charge Pumps:
- +3.3 V to ±8.8 V Triple Charge Pump Architecture or +5.0 V to ±8.8 V Doubler Charge Pump Architecture
- Requires Five Inexpensive Electrolytic Capacitors
- On-Chip 40 kHz Oscillators

Ring Monitor Circuit:
- Invert the Input Level on Rx1 to Logic Output Level on RIMON at Standby Mode

PIN ASSIGNMENTS



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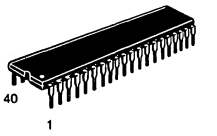
MC145601

Product Preview

Time Slot Interchange Circuit



P SUFFIX
PLASTIC
CASE 711

The MC145601 time slot interchange circuit (TSIC) is a CMOS IC designed for switching pulse code modulation 9PCM) voice or data, under microprocessor control, in a digital exchange or central office. It connects any of 256 incoming PCM channels to any of 256 outgoing PCM channels.

- 5 V Supply
- 8 × 32 Channel Input
- 8 × 32 Channel Output
- 256 Port Non-blocking Digital Switching Matrix
- Building Block for Digital PABX
- Expandable to Larger Capacity Block
- 32 Serial Channels Per Frame
- Typical Bit Rate: 2.048 Mbps
- Typical Synchronization Rate: 8 kHz
- Interface to MC88XXX Family Microprocessors
- 8 Instructions Available
- 40-Pin Dual-In-Line Package

PIN ASSIGNMENT

OC4	1	40	$\overline{\text{RESET}}$
OC3	2	39	CLK
OC2	3	38	SYNC
OC1	4	37	Tx7
OC0	5	36	Tx6
Rx7	6	35	Tx5
Rx6	7	34	Tx4
Rx5	8	33	V_{DD}
Rx4	9	32	Tx3
V_{SS}	10	31	Tx2
Rx3	11	30	Tx1
Rx2	12	29	Tx0
Rx1	13	28	D7
Rx0	14	27	D6
READY	15	26	D5
$\overline{\text{DTACK}}$	16	25	D4
RS1	17	24	D3
RS0	18	23	D2
R/$\overline{\text{W}}$	19	22	D1
$\overline{\text{CS}}$	20	21	D0

NOT RECOMMENDED FOR NEW DESIGN

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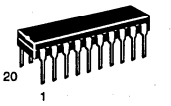
MC145611

Product Preview

PCM Conference Circuit



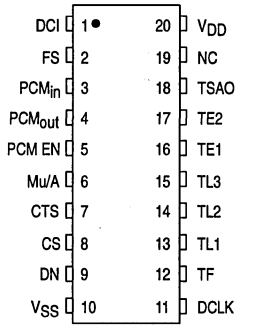
P SUFFIX
PLASTIC
CASE 738

The MC145611 PCM conference circuit is an HCMOS device designed for voice conference in a digital (PCM) telephone switch such as a TDM PABX. The device is capable of providing mixing of up to eight channels (parties) such that every party can hear when one or more parties speak at the same time.

The technique of level priority coding is used. It provides a low cost means of mixing of PCM voice codes for voice conference application.

- 20-Pin Dual-In-Line Package
- Single +5 V Power Supply
- Support Standard Mu-Law or A-Law PCM Codes
- Directly Off the PCM Highways
- 4.096 MHz Clock, 8 kHz Frame Sync, and Serial PCM Data Comply with Codec Timing Used in the PABX System
- One-Frame Delay to PCM Data
- Built-In Time Slot Assignment Circuit
- Serial Data with MCU Interface
- 8 Parties Conference in Single Group or Split into Two Groups
- Intrusion Party Channel Time Slot Assignment Provided
- Built-In Maskable Tone Signalling. Tone Level and Frequency External Adjustable

PIN ASSIGNMENT



NC = NO CONNECTION

NOT RECOMMENDED
FOR NEW DESIGN

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MC145705
MC145706
MC145707

Product Preview

5-Volt-Only Driver/Receiver With an Integrated Standby Mode

EIA-232-E and CCITT V.28

The MC145705/06/07 are a series of silicon-gate CMOS transceiver ICs that fulfill the electrical specifications of EIA-232-E and CCITT V.28 while operating from a single +5 V power supply. These transceiver series are high performance and low power consumption devices that are equipped with standby and output enable function.

A voltage doubler and inverter convert the +5 V to ±10 V. This is accomplished through an on-board 20 kHz oscillator and four inexpensive external electrolytic capacitors.

The MC145705 is composed of two drivers and three receivers, the MC145706 has three drivers and two receivers, and the MC145707 has three drivers and three receivers. These drivers and receivers are virtually identical to those of the MC145407.

Available Driver/Receiver Combinations

Device	Drivers	Receivers	No. of Pins
MC145705	2	3	20
MC145706	3	2	20
MC145707	3	3	24

Drivers:

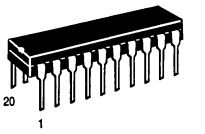
- ±7.5 Output Swing
- 300 Ω Power-Off Impedance
- Output Current Limiting
- TTL and CMOS Compatible Inputs
- Three-State Outputs During Standby Mode
- Hold Output OFF (MARK) State by TxEN Pin

Receivers:

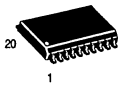
- ±25 V Input Range
- 3 to 7 kΩ Input Impedance
- 0.8 V Hysteresis for Enhanced Noise Immunity
- Three-State Outputs During Standby Mode

Charge Pumps:

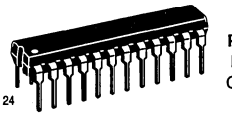
- +5 to ±10 V Dual Charge Pump Architecture
- Supply Outputs Capable of Driving Three Drivers on the MC145403/06 Simultaneously
- Requires Four Inexpensive Electrolytic Capacitors
- On-Chip 20 kHz Oscillators



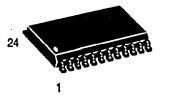
P SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOG
CASE 751D



P SUFFIX
PLASTIC
CASE 724



DW SUFFIX
SOG
CASE 751E

ORDERING INFORMATION

MC145705P MC145706P MC145707P	PLASTIC
MC145705DW MC145706DW MC145707DW	SOG

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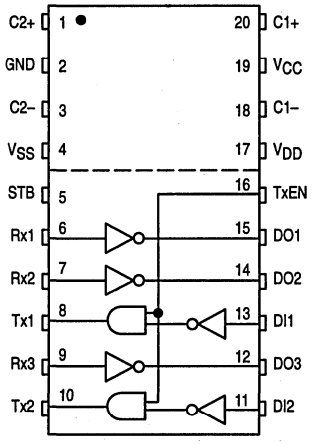
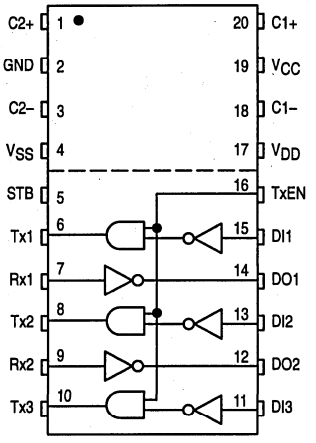
PIN ASSIGNMENTS

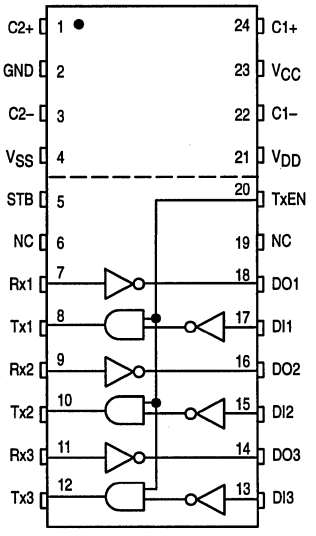
MC145705
2 Drivers/3 Receivers



MC145706
3 Drivers/2 Receivers



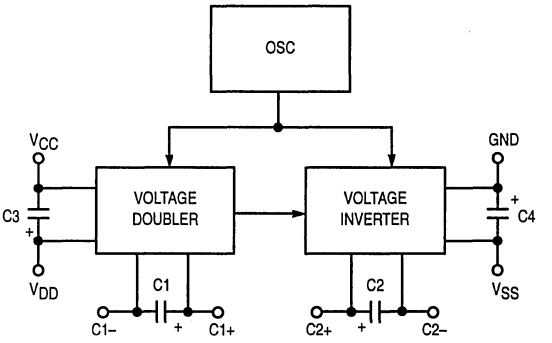
MC145707
3 Drivers/3 Receivers



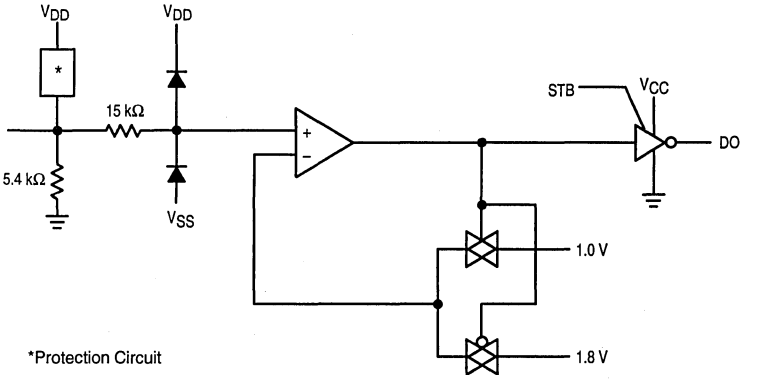
NC = NO CONNECTION

FUNCTION DIAGRAM

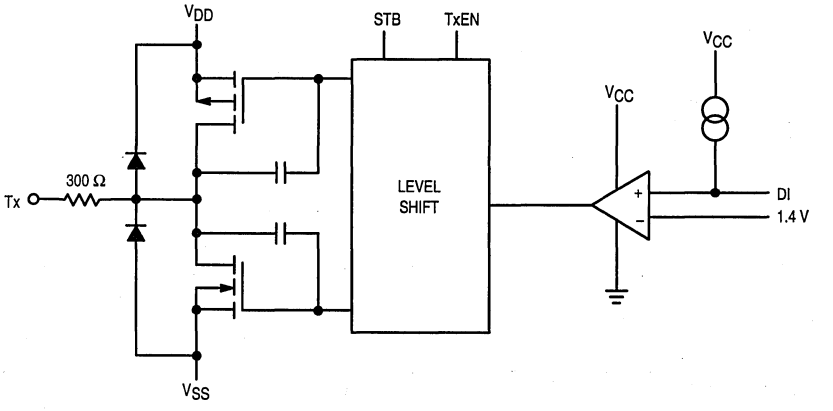
CHARGE PUMPS



RECEIVER



DRIVER



MAXIMUM RATINGS (Voltage Polarities Referenced to GND)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	–0.5 to +6.0	V
Input Voltage Rx1–3 Inputs DI1–3 Inputs	V_{IR}	V_{SS}–15 to V_{DD}+15 –0.5 to V_{CC}+0.5	V
DC Current Per Pin	I	±100	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–85 to +150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that the voltage at the DI and DO pins be constrained to the range $GND \le V_{DI} \le V_{DD}$ and $GND \le V_{DO} \le V_{CC}$. Also, the voltage at the Rx pin should be constrained to $(V_{SS} - 15\ V) \le V_{Rx1-Rx3} \le (V_{DD} + 15\ V)$, and Tx should be constrained to $V_{SS} \le V_{Tx1-Tx3} \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., GND or V_{CC} for DI, and GND for Rx).

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	4.5	5	5.5	V
Operating Temperature Range	T_A	–40	—	85	°C

DC ELECTRICAL CHARACTERISTICS (Voltage polarities referenced to GND = 0 V; C1–C4 = 10 µF; T_A = –40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
DC Power Supply	V_{CC}	4.5	5	5.5	V
Quiescent Supply Current (Output Unloaded, Input Low)	I_{CC}	—	1.7	3.5	mA
Quiescent Supply Current (Stand-By Mode) (Output Unloaded, Input Open)	$I_{CC(STB)}$	—	<10	20	µA
Control Signal Input Voltage (STB, TxEN) Logic Low Logic High	V_{IL} V_{IH}	— V_{CC}–0.5	— —	0.5 —	V
Control Signal Input Current Logic Low (TxEN) Logic High (STB)	I_{IL} I_{IH}	— —	— —	–10 10	µA
Charge Pumps Output Voltage (C1, C2, C3, C4 = 10 µF)	V_{DD}				V
Output Voltage (V_{DD}) I_{load} = 0 mA		8.5	10.0	11	
I_{load} = 5 mA		7.5	9.5	—	
I_{load} = 10 mA		6.0	9.0	—	
Output Voltage (V_{SS}) I_{load} = 0 mA	V_{SS}	–8.5	–10.0	–11	
I_{load} = 5 mA		–7.5	–9.2	—	
I_{load} = 10 mA		–6.0	–8.6	—	

RECEIVER ELECTRICAL SPECIFICATIONS
(Voltage polarities referenced to GND = 0 V; V_{CC} = +5 V ±10%; C1–C4 = 10 µF; T_A = –40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Turn-On Threshold ($V_{DO1-DO3} = V_{OL}$) Rx1–Rx3	V_{on}	1.35	1.8	2.35	V
Input Turn-Off Threshold ($V_{DO1-DO3} = V_{OH}$) Rx1–Rx3	V_{off}	0.75	1	1.25	V
Input Threshold Hysteresis ($V_{on} = V_{off}$) Rx1–Rx3	V_{hys}	0.6	0.8	—	V
Input Resistance	R_{in}	3	5.4	7	kΩ
High-Level Output Voltage (DO1–DO3) I_{out} = –20 µA	V_{OH}	V_{CC}–0.1	—	—	V
$V_{Rx1-Rx3}$ = –3 to –25 V I_{out} = –1 mA		V_{CC}–0.7	4.3	—	
Low-Level Output Voltage (DO1–DO3) I_{out} = +20 µA	V_{OL}	—	0.01	0.1	V
$V_{Rx1-Rx3}$ = +3 to +25 V I_{out} = +1.6 mA		—	0.5	0.7	

DRIVER ELECTRICAL SPECIFICATIONS

(Voltage polarities referenced to GND = 0 V; V_{CC} = +5 V ±10%; C1–C4 = 10 µF; T_A = –40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Digital Input Voltage DI1–DI3					V
Logic Low	V_{IL}	—	—	0.8	
Logic High	V_{IH}	2	—	—	
Input Current DI1–DI3					µA
V_{DI} = GND	I_{IL}	—	7	—	
V_{DI} = V_{CC}	I_{IH}	—	—	±1.0	
Output High Voltage Tx1–Tx3 ($V_{DI1–DI3}$ = Logic Low, R_L = 3 kΩ)	V_{OH}	6	7.5	—	V
Tx1–Tx6*		5	6.5	—	
Output Low Voltage Tx1–Tx3 ($V_{DI1–DI3}$ = Logic High, R_L = 3 kΩ)	V_{OL}	–6	–7.5	—	V
Tx1–Tx6*		–5	–6.5	—	
Off Source Impedance Tx1–Tx3	Z_{off}	300	—	—	Ω
Output Short Circuit Current (V_{CC} = 5.5 V)	I_{SC}				mA
Tx1–Tx3 Shorted to GND**		—	—	±60	
Tx1–Tx3 Shorted to ±15 V***		—	—	±100	

*Specifications for a MC14570X powering a MC145406 or MC145403 with three additional drivers/receivers.

**Specification is for one Tx output to be shorted at a time. Should all three driver outputs be shorted simultaneously, device power dissipation limits could be exceeded.

***This condition could exceed package limitations.

SWITCHING CHARACTERISTICS (V_{CC} = +5 V, ±10%; C1–C4 = 10 µF; T_A = –40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Drivers					
Propagation Delay Time Tx1–Tx3					µs
Low-to-High (R_L = 3 kΩ, C_L = 50 pF or 2500 pF)	t_{PLH}	—	0.5	1	
High-to-Low (R_L = 3 kΩ, C_L = 50 pF or 2500 pF)	t_{PHL}	—	0.5	1	
Output Slew Rate Tx1–Tx3	SR				V/µs
Minimum Load (R_L = 7 kΩ, C_L = 0 pF)		—	±6	±30	
Maximum Load (R_L = 3 kΩ, C_L = 2500 pF)		—	±5	—	
Output Disable Time	t_{DAZ}	—	4	10	µs
Output Enable Time	t_{DZA}	—	25	50	ms
Receivers					
Propagation Delay Time DO1–DO3					µs
Low-to-High	t_{PLH}	—	—	1	
High-to-Low	t_{PHL}	—	—	1	
Output Rise Time DO1–DO3	t_r	—	250	400	ns
Output Fall Time DO1–DO3	t_f	—	40	100	ns
Output Disable Time	t_{RAZ}	—	4	10	µs
Output Enable Time	t_{RZA}	—	25	50	ms

TRUTH TABLE

Drivers

DI	TxEN	STB	Tx
X	X	H	Z*
X	L	L	L
H	H	L	L
L	H	L	H

*$V_{SS} \le V_{Tx} \le V_{DD}$ X = Don't Care

Receivers

Rx	STB	DO
X	H	Z*
H	L	L
L	L	H

*GND ≤ V_{DO} ≤ V_{CC} X = Don't Care

PIN DESCRIPTIONS

V_{CC}
Digital Power Supply
This digital supply pin is connected to the logic power supply. This pin should have a 0.33 µF capacitor to ground.

GND
Ground
Ground return pin is typically connected to the signal ground pin of the EIA-232D connector (Pin 7) as well as to the logic power supply ground.

V_{DD}
Positive Power Supply
This is the positive output of the on-chip voltage doubler and the positive power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

V_{SS}
Negative Power Supply
This is the negative output of the on-chip voltage doubler/inverter and the negative power supply input of the driver/receiver sections of the device. This pin requires an external storage capacitor to filter the 50% duty cycle voltage generated by the charge pump.

TxEN
Output Enable
This is the driver output enable pin. When this pin is in logic low level, the condition of the driver outputs (Tx1–Tx3) are in keep OFF (mark) state.

STB
Stand-By
The device enters the stand-by mode while this pin is connected to the logic high level. During the stand-by mode, driver and receiver output pins become high-impedance state. In this condition, supply current I_{CC} is below 10 µA (Typ) and can be operated with low current consumption.

C2+, C2–, C1+, C1–
Voltage Doubler And Inverter
These are the connections to the internal voltage doubler and inverter, which generate the V_{DD} and V_{SS} voltages.

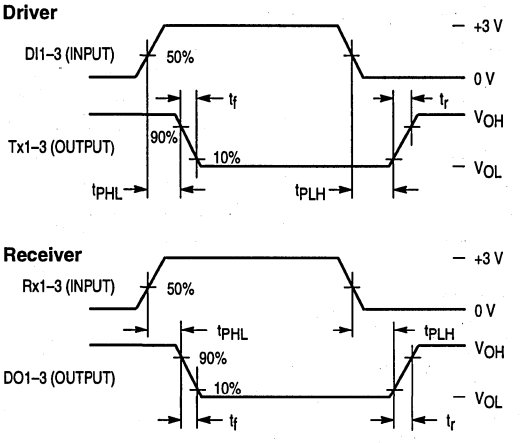
Rx1, Rx2 (Rx3)
Receive Data Input
These are the EIA-232-E receive signal inputs. A voltage between +3 and +25 V is decoded as a space, and causes the corresponding DO pin to swing to ground (0 V). A voltage between –3 and –25 V is decoded as a mark, and causes the DO pin to swing up to V_{CC}.

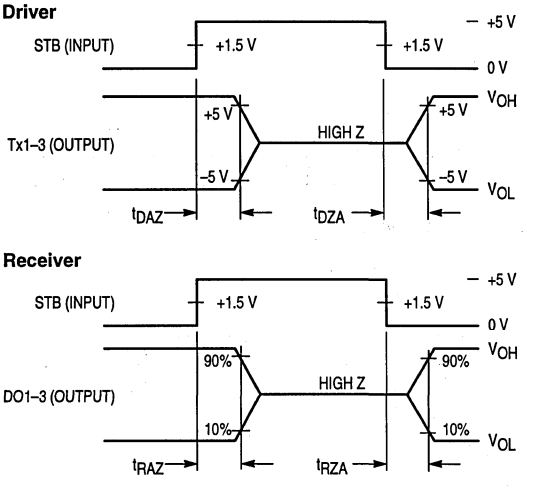
DO1, DO2 (DO3)
Data Output
These are the receiver digital output pins, which swing from V_{CC} to GND. Each output pin is capable of driving one LSTTL input load.
Output level of these pins is high-impedance while in standby mode.

DI1, DI2 (DI3)
Data Input
These are the high-impedance digital input pins to the drivers. Input voltage levels on these pins must be between V_{CC} and GND.
The level of these input pins are TTL/CMOS compatible.

Tx1, Tx2 (Tx3)
Transmit Data Output
These are the EIA-232-E transmit signal output pins, which swing toward V_{DD} and V_{SS}. A logic 1 at a DI input causes the corresponding Tx output to swing toward V_{SS}. The actual levels and slew rate achieved will depend on the output loading (RL/CL).
The minimum output impedance is 300 Ω when turned off.

SWITCHING CHARACTERISTICS





TCA3385

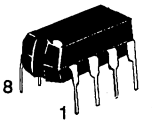
Advance Information

Telephone Ring Signal Converter

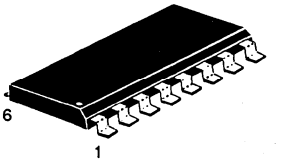
The TCA3385 is a high efficiency telephone ring signal converter designed for use with the TCA3386 (it can also be used stand-alone). These devices, together with a microprocessor, form the basis for a high-performance feature telephone set.

The circuit includes a switching regulator which converts the ring signal from the telephone line into a DC supply signal suitable for powering the other devices in the telephone, e.g. TCA3386 and the MPU, during the ringing phase.

- High efficiency step-down DC/DC converter with linear input impedance
- Power derived from rectified AC ring signal or DC voltage
- Drive output for external PNP transistor
- System supply voltage determined by external transistor, coils and diodes
- Two modes of operation: fixed internal or programmable ring detect threshold (7 to 35V)
- Programmable input impedance between 3K and 15Kohms
- Ring detect output for microprocessor
- Lightning and mains protection
- Applications: telephone set, answering machine, home appliance, etc...



DP SUFFIX
PLASTIC PACKAGE
CASE 626

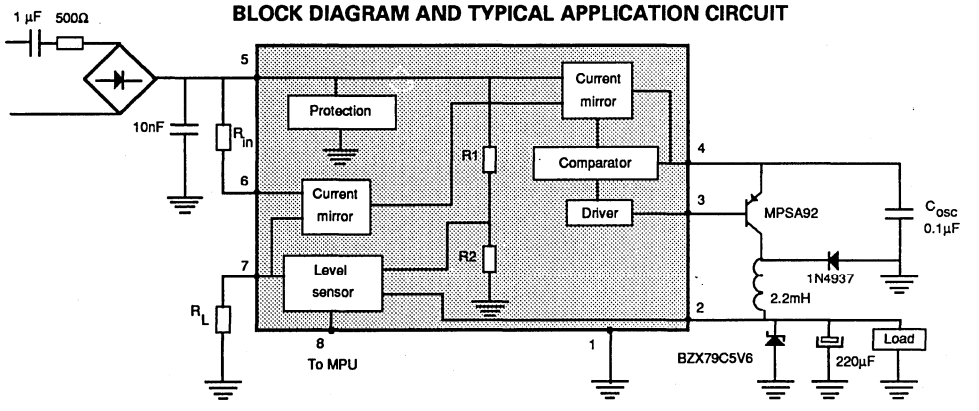


FP SUFFIX
PLASTIC PACKAGE
CASE 751G

ORDERING INFORMATION

TCA3385-DP Plastic DIP
TCA3385-FP SO package

BLOCK DIAGRAM AND TYPICAL APPLICATION CIRCUIT



TCA3385 PIN DESCRIPTIONS

Pin 1 GND, GROUND
This is the reference ground for the overall system.

Pin 2 V_{cc}, POWER SUPPLY
The output is a current which will establish a voltage defined by the load circuit and the voltage regulator (typically 5-6 volts for telephone application).

Pin 3 DRV, DRIVE OUTPUT
This output directly drives the base of the PNP transistor of the switchmode power supply system.

Pin 4 CO, CURRENT OUTPUT
This pin provides constant current output for charging the external capacitor C_{osc}.

Pin 5 LI, LINE INPUT
This pin can be driven either by a DC voltage or a non filtered rectified AC voltage. In a typical telephone application, it is connected to the positive side of a diode bridge before the twisted pair cable.

Pin 6 R_{in}
An external resistor R_{in} connected between this pin and LI sets the input impedance of the circuit.

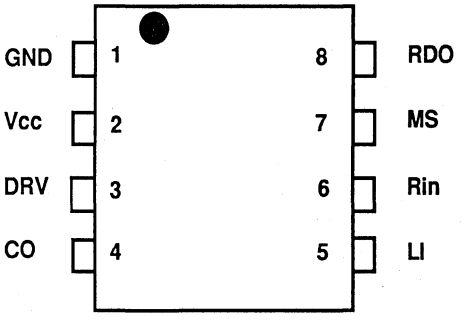
Pin 7 MS, MODE SELECT
An external resistor R_L connected between this pin and ground sets the value of the ring detect threshold.

If R_L = 0, Mode 1 is selected and a fixed 12 volt level is automatically chosen by the internal level sensor circuitry.

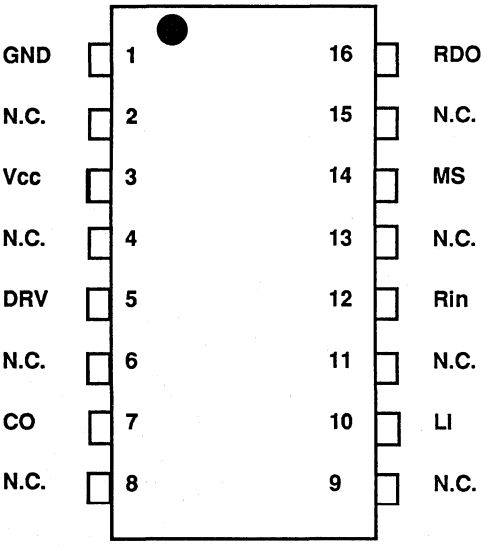
Otherwise Mode 2 is selected and R_L determines the value of the ring detect threshold. In Mode 2 R_L also affects the input impedance of the circuit.

Pin 8 RDO, RING DETECT OUTPUT
This is a digital output for a microprocessor which indicates that a ring signal has been detected. This pin will shift from low to high each time the input voltage passes the preset threshold voltage.

Depending on its load (resistive or capacitive), the signal at this pin can either remain high during the ring time, or be a square wave at twice the ringing signal frequency.



DIL 8 pins



SOIC wide 16 pins

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Line Voltage	120	V rms
Input Impedance	3K to 15K	Ohms
Maximum Peak Current (crowbar on)	500	mA
Storage Temperature Range	-65 to +150	°C
Operating Junction Temperature	150	°C

Devices should not be operated at or outside these values. Actual device operation should be restricted to within the "Recommended Operating Limits".

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Unit
Operating Ambient Temperature Range	T_a	0		70	°C
Line Voltage	V_{in}			90	V rms
Line Source Impedance	Z_s	500			Ohms

THERMAL DATA

Parameter	Value	Unit
Thermal Resistance Junction-Ambient Plastic Package Case 626 SO Package Case 751G	 90 110	°C/W

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Ring Detect Output Voltage High	V_{oh}	V_{cc} -0.93	V_{cc} -0.7	V_{cc} -0.57	V
Ring detect Output Voltage Low	V_{ol}		11	20	mV
Turn-on Threshold Input Voltage (Mode 1, R_L=0, I_{Load}=0)	V_{d1}	11.2	12	13.0	V
Threshold Temperature Drift (Mode 1, R_L=0)	DV_{d1}		-5		mV/°C
On/Off Threshold Hysteresis (Mode 1, R_L=0, I_{Load}=0)	Hys1	1.2	1.8	2.4	V
Turn-on Threshold Input Voltage (Mode 2, limit fixed by ext res R_L)	V_{d2}	8		35	V
Threshold Temperature Drift (Mode 2)	D_{Vd2}		-20		mV/°C
On/Off Threshold Hysteresis (Mode 2)	Hys2	0.5		7	V
Ring Detect Output Pull-up Current (V_{in} = 15V)	$I_{d\ up}$	0.5	1.5	2.5	mA
Ring Detect Output Pull-down Current Low State ($V_{RDO} < V_{cc}$ /2) High State ($V_{RDO} > V_{cc}$ /2)	$I_{d\ down}$	 60 10	 100 20	 140 26	µA
V_{cc} Level (Ring Detector Enabled) @ V_{cc} max = 5.5V	$V_{cc\ on}$	2.75	3.1	3.45	V
Vcc Level (Ring Detector Disabled) @ V_{cc} max = 5.5V	$V_{cc\ off}$	1.40	1.8	2.3	V
Ring Detect Output Rise Time (no capacitor)	t_r		1		µs
Ring Detect Output Fall Time (no capacitor)	t_f		4		µs
Ring Detect Output Ripple (Crd = 0.47µF, f = 50Hz, no load)	$V_{d\ rip}$		0.25	0.5	V pp

SWITCHMODE POWER SUPPLY

Parameter	Symbol	Min	Typ	Max	Unit
V_{cc} Output Voltage (I_{load} = 36mA)	V_{cc}	Fixed by Zener diode			
Output Power (V_{in} = 90V rms, f = 50Hz)	P_{out}			600	mW
Power Supply Efficiency	Eff	50	55		%
Switching Frequency (V_{in} = 40v, R_{in} = 500KΩ)	Fs	25	35	45	KHz
Output Voltage Ripple (I_{load} = 36mA, C_{load} = 220µF, V_{in} = 90V rms)	$V_{cc\ rip}$		0.5	0.7	V pp
C_{osc} Charge Current (V_{in} = 20V, R_{in} = 500KΩ, R_L = 0)	I_{charge}	3.1	3.5	4.1	mA
C_{osc} Discharge Current (V_{in} = 20V, R_{in} = 500KΩ, R_L = 0)	$I_{disch.}$	11	18	25	mA

LINE INPUT AND PROTECTION

Parameter	Symbol	Min	Typ	Max	Unit
Input Impedance	Z_{in}				Kohm
Off-state (V_{in} = 4.5V, R_{in} = 500KΩ, R_L = 0)		25	50		
On-state (V_{in} > 25V, Mode 1, R_L = 0)		3	$\frac{R_{in}}{100}$	15	
Fixed by external resistance R_{in}					
On-state (V_{in} > 25V, Mode 2)		3	$\frac{R_{in}+2R_L}{100}$	15	
Fixed by external resistance R_{in} and R_L					
Non-linearity @ 35 <V_{in} < 75 V	NL				%
Mode 1			3	8	
Mode 2			3	8	
Overvoltage Protection Threshold (Crowbar on)	V_{ov}	120	135	147	V
Crowbar-on Input Voltage (Crowbar On, I_{limit} = 40mA)	V_{on}	4.3	6.5	8.7	V
Crowbar-on Power Dissipation (Limited by Internal 100 ohms + external res.)	Pd			1.3	W
Crowbar Turn-on Delay (CRD = 0.1µF)	T_{on}		130		µs

INTRODUCTION

The TCA3385 is primarily intended for converting the ring signal delivered by a central office or PABX into a DC voltage which is suitable for powering the other components in an electronic telephone. It will supply the power to enable the use of the features of a sophisticated telephone, such as MPU control, generation and amplification of ringing melodies at a speaker, display short messages of information, etc... while the telephone is on-hook.

The circuit combines a high efficiency DC/DC converter and a level sensor device which acts as a programmable ring detector and indicator for a MPU, thus initiating the operation of the telephone.

Overvoltage protection is also achieved using a "crowbar" technique.

LINE INPUT AND PROTECTION

The DC/DC converter has linear input impedance, which means that the circuit input impedance is ohmic and constant whenever the input voltage varies above the turn-on threshold voltage inside the tolerated limits. Any value between 3K and 15Kohms can be set using one or two resistors, depending on the mode of operation (see paragraph "RING DETECTOR" below). In Mode 1 the circuit input impedance Z_{in} is a ratio of the resistor R_{in} between pin 5 and pin 6: $Z_{in} = R_{in}/100$. In Mode 2, Z_{in} is a function of R_{in} and the resistor R_L between pin 7 and ground: $Z_{in} = (R_{in} + 2R_L)/100$.

On the other hand, the turn-on input circuitry guarantees that the input impedance is high at low voltages to avoid perturbing the line.

The overvoltage protection device consists of two thyristors in series which are turned-on at a voltage between 120V and 150V. The input current is limited by a 100 ohms internal resistor, but an external resistor is mandatory to prevent excessive currents. A 500 ohms series resistor is recommended as minimum.

RING DETECTOR

The TCA3385 includes a ring detector (also called level sensor) whose function is to provide a digital output for a MPU. It only operates when the circuit is sufficiently powered, i.e. when the DC/DC converter output (V_{cc}) has reached a level greater than 3V. It also has hysteresis which powers the level sensor off at 2V.

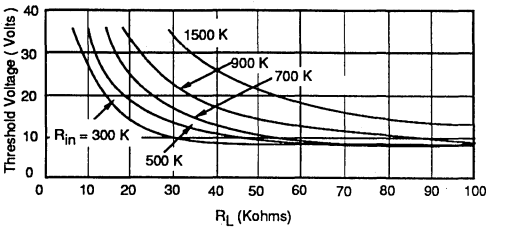


Figure 1. Ring Detection Threshold (Mode 2) vs R_{in} and R_L

The digital output shifts from low to high according to the line input voltage, a preset level for detection and its load at pin 8.

The level for ring detection may be set using one or two modes of operation as previously noted. In Mode 1, where pin 7 is connected to ground, an internally fixed level is set as the ring detect threshold, which is typically 12 Volts. In Mode 2 operation, where an external resistor R_L is connected between pin 7 and ground, the ring detect threshold is programmable. Its value is a function of R_L (see Figure 1).

It should be noted that due to the IC design structure, Mode 1 is not a particular case of Mode 2. In fact, in Mode 2, R_L must be chosen high enough so that the ring detector works efficiently (the minimum limit is fixed by the upper limit of 35V for the ring detect threshold; see Figure 1).

In a telephone application, where the input signal is a rectified AC ringing signal, we can choose between two output modes at pin 8, pulsed or continuous: without a capacitor at pin 8, the ouput voltage will change state each time the input crosses the ring detect turn-on and turn-off thresholds, thus providing information on the frequency of the ring signal; on the other hand, if the load at pin 8 is a capacitor, the output voltage will shift from low to high only the first time the input crosses the turn-on threshold, and remain high until the end of the ringing pulse. This is permitted by the internal input circuitry at pin 8, which has an emitter-follower transistor for pull-up and a non-linear current generator for pull-down (20µA for slow discharge, 100µA for fast discharge; see Figure 2).

SWITCHMODE POWER SUPPLY

The TCA3385 is basically a DC/DC converter which works with external components: a PNP transistor, a coil, a zener diode, a capacitor and a holding diode.

The circuit drives the external PNP for switching the current into the coil. This PNP should be a fast switching transistor, with a switching time of less than 2% of the total pulse time $T_0 = 1/f_0$ (where f_0 is the switching frequency). For example, in a 50KHz application (T_0 = 20µs), rise time and fall time should be less than 400ns; this is mandatory to keep the efficiency of the switchmode greater than 50%. Also, the PNP must withstand voltages as high as 150V. In the suggested application, a MPSA92 (or a BDC06) is used.

The holding diode should also have a low forward voltage drop and fast switching characteristics so that high power output is achieved. It must withstand voltages as high as 150V. The coil as well should have its losses (both magnetic and resistive) minimized.

The DC/DC converter consists of 3 main blocks:

- a current mirror which produces a constant current for charging the external capacitor. This current is dependent on V_{in}.
- a comparator to set the switching frequency of the power supply. The switching frequency is mainly dependent on the input voltage V_{in} and the input impedance Z_{in}.
- a drive stage for the PNP transistor.

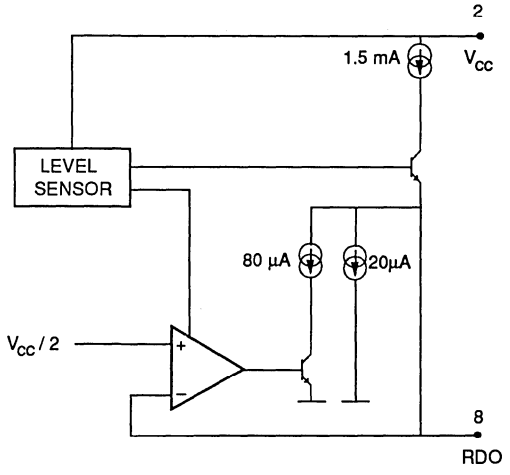


Figure 2. Ring Detect Output Stage

EXTERNAL PROTECTION RESISTOR

This device has been designed to accept overvoltage input signals, by switching ON two serial input thyristors, from levels exceeding 120V between pin 5 and pin 1. In this case the current is limited by an internal 100 ohms series resistor with an external resistor Rv (nominally 500 ohms).

a) Fast input signals

If the slew rate of the overvoltage pulse is much greater than 500V/ms (which is valid for a 1µF series capacitor with a current limit of 500mA), then the peak current is equal to the applied peak voltage divided by the external resistance R_v.

Under these conditions, the absolute maximum peak current is equal to 500mA, no matter how short the pulse .

For example : for 400V maximum limit, R_v = 400V/0.5A = 800 ohms.

b) Slow input signals

For slow signals (eg: ringing signals 25, 50, 100 Hz...) the maximum current must be limited to 250mA. So, for the French standard ringing voltage , R_v is equal to $120V_{max}/0.25A$ = 500 ohms.

If the overvoltage is higher, R_v must be calculated for the new maximum input voltage.

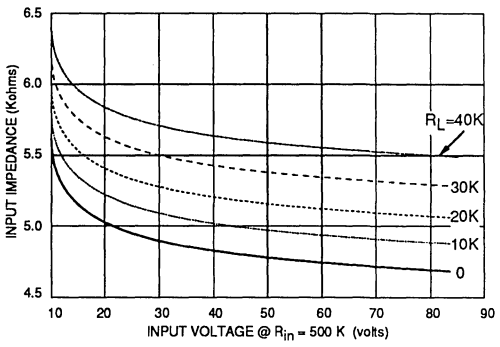


Figure 3. Input Impedance vs V_{in} @ R_{in} = 500K

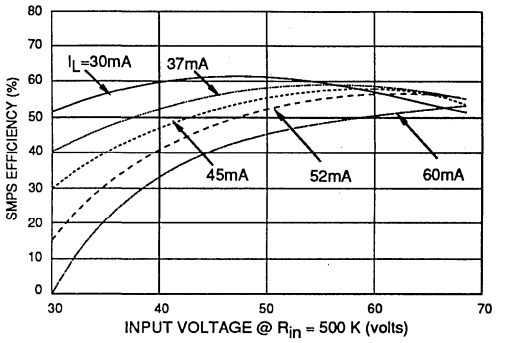


Figure 4. SMPS Efficiency vs V_{in} @ R_{in} = 500K

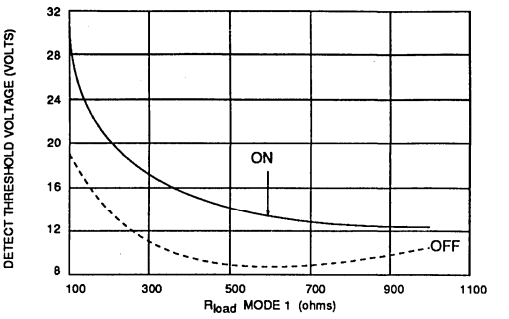


Figure 5. Detect Threshold vs R_{load} (Mode 1)

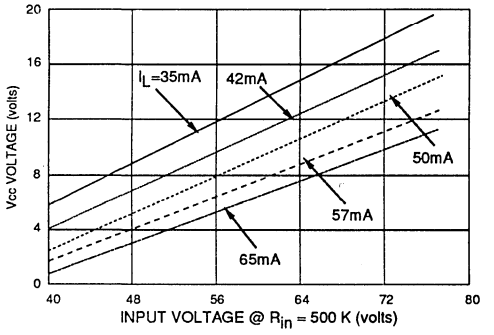


Figure 6. V_{cc} vs V_{in} @ R_{in} = 500K (without Zener)

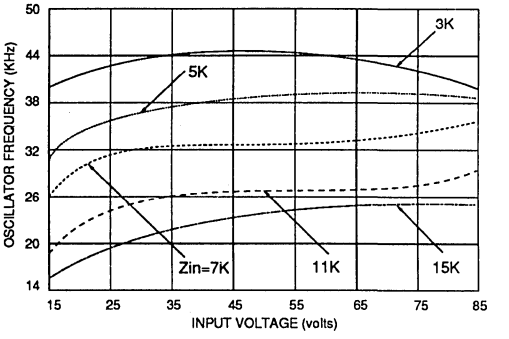


Figure 7. Oscillator frequency vs V_{in}

TCA 3388

Product Preview

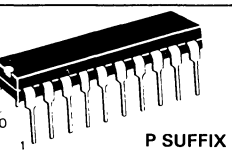
SPEECH CIRCUIT

The TCA3388 is a high density bipolar telephone speech network to replace the hybrid circuit in a telephone set.

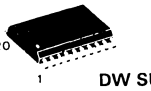
This circuit includes sidetone balance, microphone and push pull earphone amplifier with loop length compensation, programmable impedance (real or complex), programmable DC mask (French, UK Low voltage and PABX configuration for each), direct interface for a DTMF/pulse dialer (adjustble DTMF input, pulse input, hook status output and mute input), regulated power supply and protection against excess signal voltage.

Design precautions have been taken to increase RFI immunity. This circuit associated with a DTMF/pulse dialer (MC145516) and a tone ringer (MC34017) forms the basis of a low cost telephone set.

- Low voltage, low current operation: high peak-to-peak signal on the line
- DC mask programmable by external pins
- 2 to 4 wire conversion
- Programmable impedance (real or complex)
- Programmable sidetone balance with automatic line length tracking
- Automatic line length receiving and sending gain control
- Microphone amplifier with externally adjustable gain (piezo or electret transducers)
- Earphone push pull amplifier with externally adjustable gain (piezo or electrodynamic transducers)
- Mute facility for transmit and receive amplifier
- Regulated supply voltage (3.6V) with high output current capability
- Protection against excess signal voltage
- Interface for DTMF/pulse dialer
- Positive and negative logic input for pulse and mute
- Hook status output

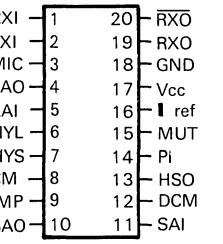


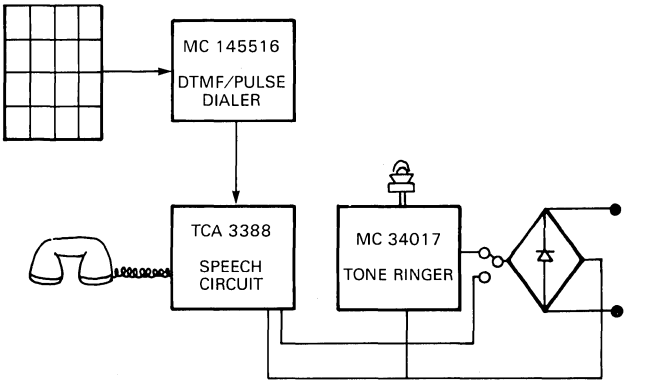
P SUFFIX
PLASTIC PACKAGE
CASE 738



DW SUFFIX
PLASTIC PACKAGE
CASE 751D

PIN ASSIGNMENT

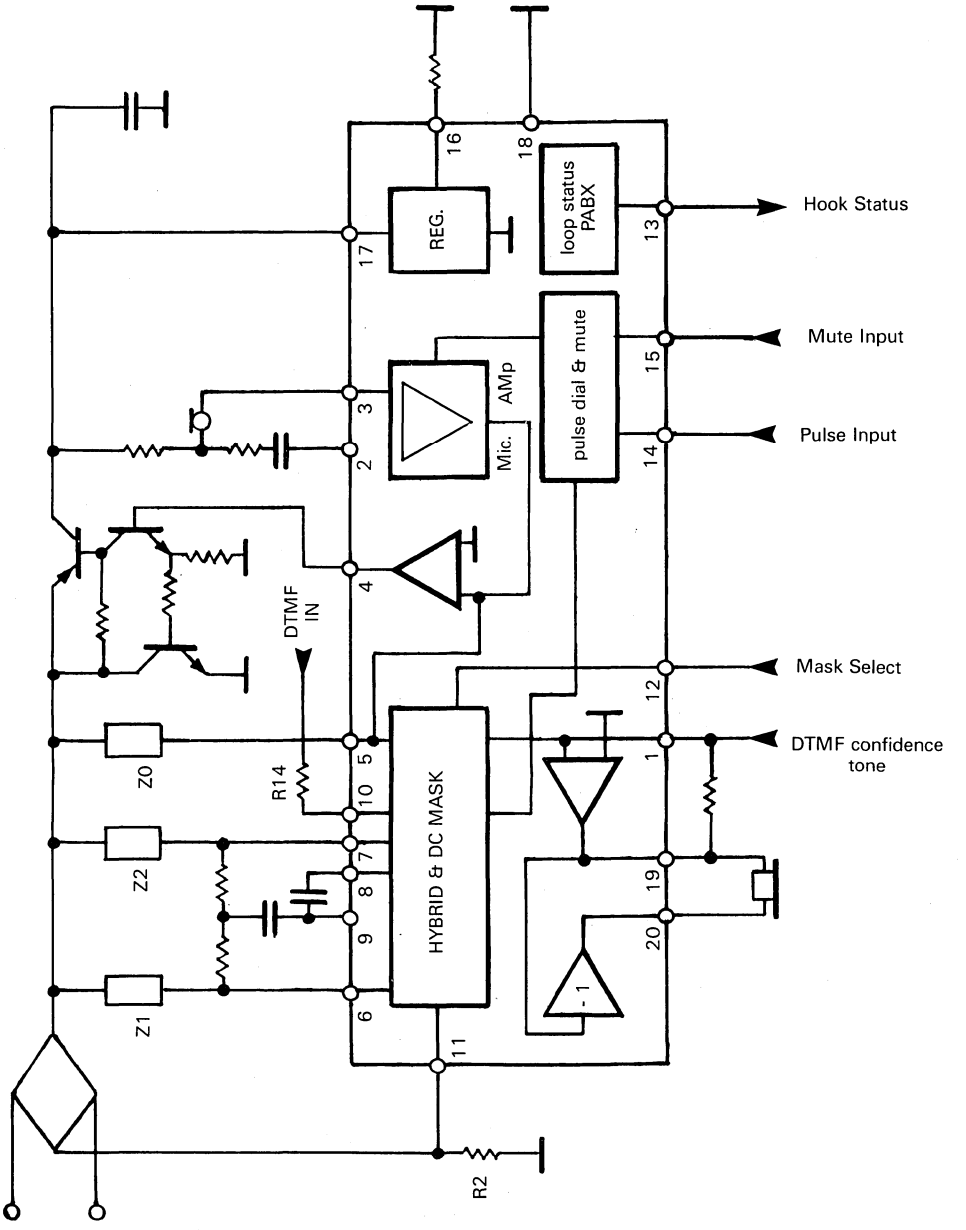


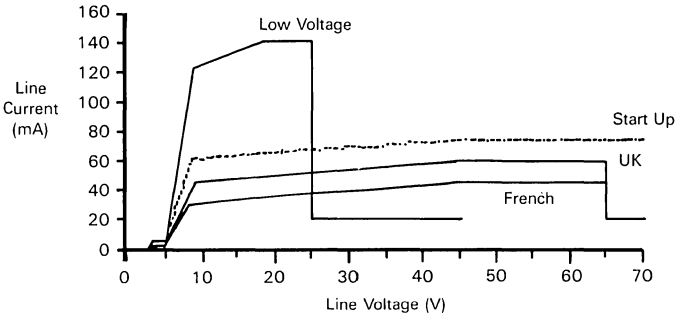


LOW END TELEPHONE SET

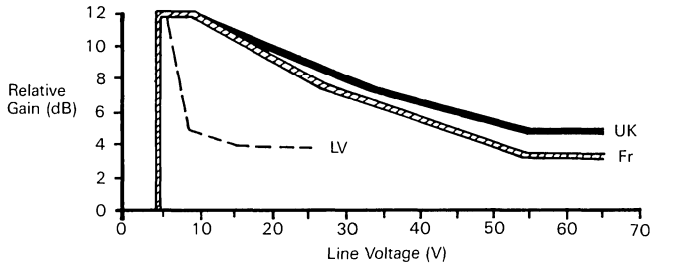
This document contains information on a new product.
Specifications and information herein are subject to change without notice.

TCA 3388 BLOCK DIAGRAM

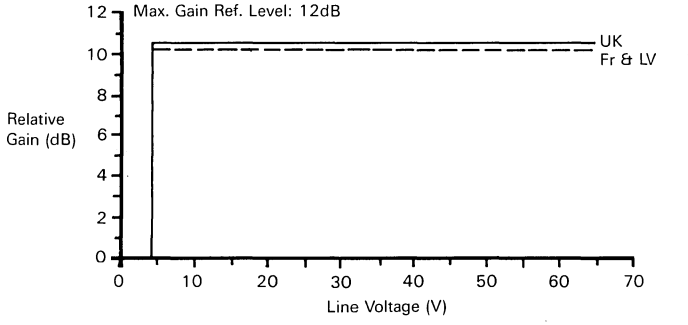




TCA 3388: DC MASKS



TCA 3388: GAIN REGULATION



TCA 3388: GAIN REGULATION, PABX MODE

PIN DESCRIPTION

1:RXI - Input for Earphone Amplifier and Confidence Tone

This pin receives the line signal via the hybrid balance and gain regulation circuits. A confidence tone (current) may also be applied to this point.

2:TXI - Microphone Current Amplifier Input

3:MIC - Microphone Negative Supply

Bias current from the electret microphone is returned to ground through this pin.

4:LAO - Line Interface Drive Amplifier Output

This pin controls the base of the high voltage line interface transistor.

5:LAI - Line Interface Drive Amplifier Input

This pin receives the AC line voltage from the input impedance network and the current for DTMF signalling. The circuit input impedance is determined by line voltage and current feedback to this pin (which is at virtual earth). The line current signal developed at pin 11 and transferred to pin 10 is received via R14 and the line voltage signal via the network ZO.

This pin may also receive a current for DTMF signalling.

6:HYL - Input for Long Line Hybrid Network

7:HYS - Input for Short Line Hybrid Network

The line signal is received between pins 6 and 10 and between pins 7 and 10. Pin 6 is connected to a network providing hybrid balance for long lines and pin 7 to a network providing hybrid balance for short lines. The received signals are weighted, according to the line length detected, summed and fed via the gain regulation and mute circuit to the earphone amplifier input (pin 1).

Both the hybrid balance impedance and the gain are therefore adapted to the line length. If this pin 7 is left open, the circuit will operate with a fixed hybrid balance impedance defined by the network on pin 6. In PABX mode, the receive mode and hybrid balance impedance are independant of the line length.

8:CM - Mask Decoupling Capacitor

For a return loss greater than 20 dB, and an imput impedance equal to 600 ohms at 300 Hz, C = 0.68μF.

9:IMP - Impedance Network Return Point

10:SAO - Line Current Sense Amplifier Output

11:SAI - Line Current Sense Amplifier Input

Voltage at this pin is proportional to the line current (I line x R2).

12:DCM - DC Mask Selection

Four dc masks are selected according to the DC voltage at this pin. An internal current generator sources (loop closed) or sinks (during line break) a constant current. The DC mask can be chosen by connecting appropriate external components (resistor, capacitor, or resistor plus capacitor) between this pin and ground.

13:HSO - Hook Status Output/PABX Mode

This pin is a digital output and reflects the status of the loop. HSO is high when the loop is closed, and low when loop is open. This pin also sets PABX mode if the load current is greater than 20μA. In PABX mode the transmission and reception gains are fixed. The hybrid balance impedance is fixed whether a single or double network is used.

14:PI - Pulse Dialing Input

This pin is a bidirectional input current for pulse dialing.

15:MUT - Mute Input

This pin is bidirectional input current for combined microphone and earphone mute.

16:I Ref - Reference Current

A programmable resistance connected to this pin sets a reference current for the circuit.

17:V_{CC} - Regulated Supply Voltage

18:GND - Ground

This pin is ground for the entire circuit.

19:RXO - Receive Amplifier Output

This pin is the output of the first receive amplifier. Receive gain is set by connecting a resistor between RXO and RX1.

20:$\overline{RXO}$ - Complementary Receive Amplifier Output

This pin is the output of the second receive amplifier.

Protection Mode

Protection is incorporated. Detection of excess continuous or signal voltage causes a transfer to a low dissipation mode after a delay.

Plastic Power Transistor Complementary Pair

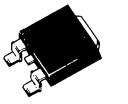
DPAK For Surface Mount and Telecom Applications

... designed for use in subscriber loop interface circuit (SLIC) applications, in conjunction with the MC33120 SLIC integrated circuit.

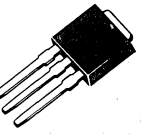
- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 100 Vdc (Min) @ I_C = 10 mAdc
- High DC Current Gain — h_{FE} = 40 (Min) @ I_C = 40 to 200 mAdc
  = 15 (Min) @ I_C = 1 Adc
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves ("-1" Suffix)
- Lead Formed Version in 16 mm Tape and Reel ("RL" Suffix)
- Low Collector-Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 0.3 Vdc (Max) @ I_C = 500 mAdc
  = 0.6 Vdc (Max) @ I_C = 1 Adc
- High Current-Gain — Bandwidth Product — f_T = 40 MHz (Min) @ I_C = 100 mAdc
- Low Leakage — I_{CBO} = 100 nAdc @ Rated V_{CB}

NPN
MJD243
PNP
MJD253

COMPLEMENTARY POWER TRANSISTORS
4 AMPERES
100 VOLTS
12.5 WATTS

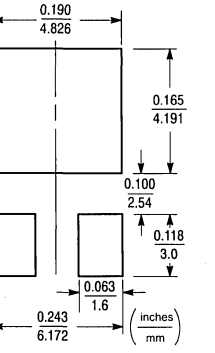


CASE 369A-13



CASE 369-07

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB}	100	Vdc
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Emitter-Base Voltage	V_{EB}	7	Vdc
Collector-Current — Continuous Peak	I_C	4 8	Adc
Base Current	I_B	1	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	12.5 0.1	Watts W/°C
Total Device Dissipation @ T_A = 25°C* Derate above 25°C	P_D	1.4 0.011	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Junction to Ambient*	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	°C/W

* When surface mounted on miminum pad sizes recommended.

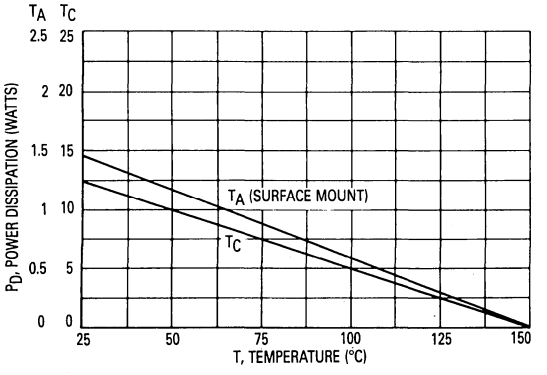


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)		$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)		I_{CBO}	—	100	nAdc
(V_{CB} = 100 Vdc, I_E = 0, T_J = 125°C)			—	100	μAdc
Emitter Cutoff Current (V_{BE} = 7 Vdc, I_C = 0)		I_{EBO}	—	100	nAdc
DC Current Gain (1)	(I_C = 40 mAdc, V_{CE} = 1 Vdc)	h_{FE}	40	—	—
	(I_C = 200 mAdc, V_{CE} = 1 Vdc)		40	180	
	(I_C = 1 Adc, V_{CE} = 1 Vdc)		15	—	
Collector-Emitter Saturation Voltage (1)	(I_C = 500 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	—	0.3	Vdc
	(I_C = 1 Adc, I_B = 100 mAdc)		—	0.6	
Base-Emitter Saturation Voltage (1)	(I_C = 2 Adc, I_B = 200 mAdc)	$V_{BE(sat)}$	—	1.8	Vdc
Base-Emitter On Voltage (1)	(I_C = 500 mAdc, V_{CE} = 1 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain — Bandwidth Product (2) (I_C = 100 mAdc, V_{CE} = 10 Vdc, f_{test} = 10 MHz)		f_T	40	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	50	pF

(1) Pulse Test: Pulse Width = 300 μs Duty Cycle ≈ 2%.
(2) $f_T = |h_{FE}| \cdot f_{test}$

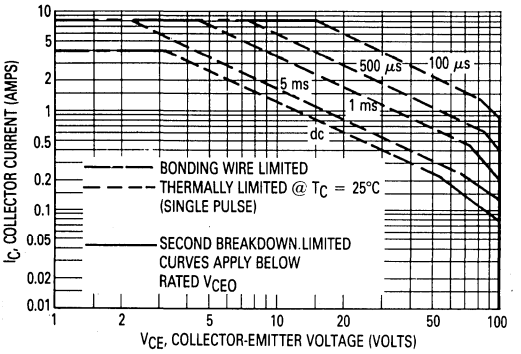


Figure 2. Active Region Maximum Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

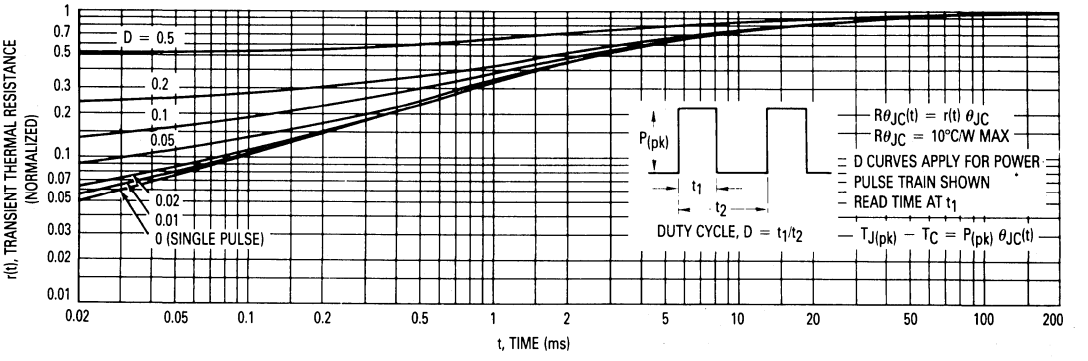


Figure 3. Thermal Response

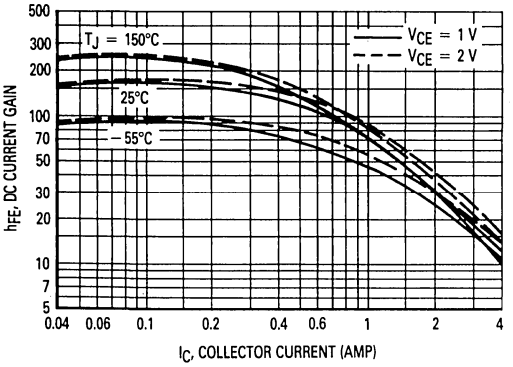


Figure 4. DC Current Gain

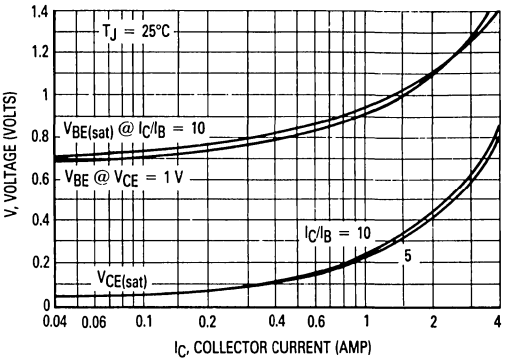


Figure 5. "On" Voltages

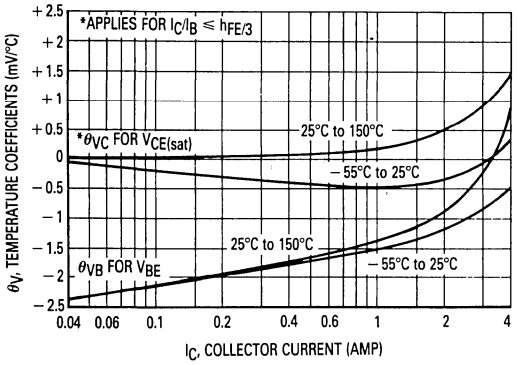


Figure 6. Temperature Coefficients

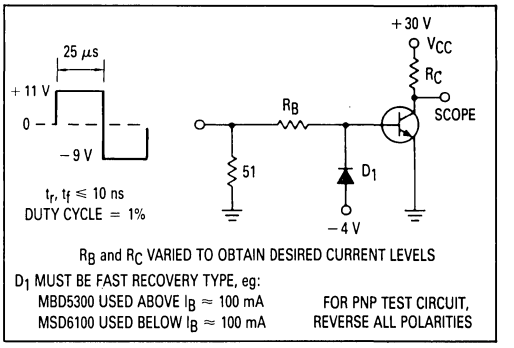


Figure 7. Switching Time Test Circuit

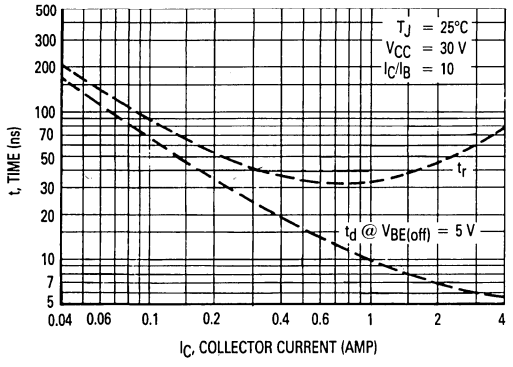


Figure 8. Turn-On Time

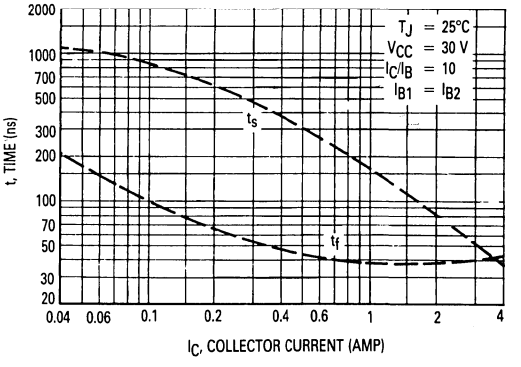


Figure 9. Turn-Off Time

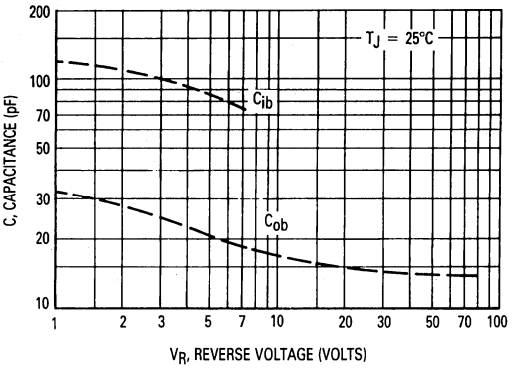


Figure 10. Capacitance

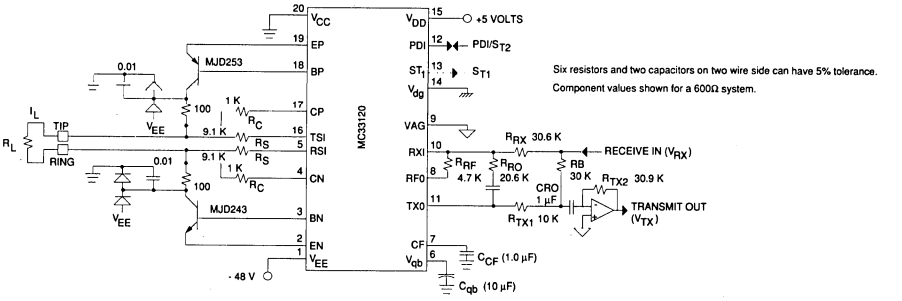


Figure 11. Application Circuit

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

NPN
MJE270
PNP
MJE271

2.0 AMPERE

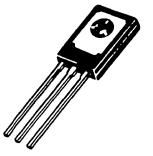
COMPLEMENTARY POWER DARLINGTON TRANSISTORS

100 VOLTS
15 WATTS

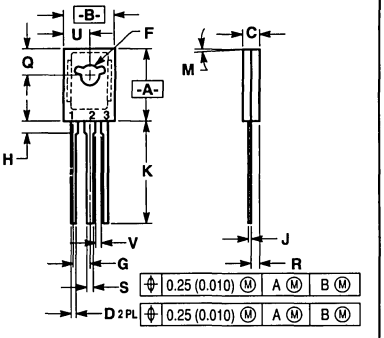
COMPLEMENTARY SILICON POWER TRANSISTORS

. . . designed specifically for use with the MC3419 Solid-State Subscriber Loop Interface Circuit (SLIC).

- High Safe Operating Area
  $I_{S/B}$ @ 40 V, 1.0 s = 0.375 A — TO-126
- Collector-Emitter Sustaining Voltage
  $V_{CEO(sus)}$ = 100 Vdc (Min)
- High DC Current Gain
  h_{FE} @ 120 mA, 10 V = 1500 (Min)



STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 077-01 THRU -06 OBSOLETE, NEW STANDARD 077-07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.80	11.04	0.425	0.435
B	7.50	7.74	0.295	0.305
C	2.42	2.66	0.095	0.105
D	0.51	0.66	0.020	0.026
F	2.93	3.30	0.115	0.130
G	2.39 BSC		0.094 BSC	
H	1.27	2.41	0.050	0.095
J	0.39	0.63	0.015	0.025
K	14.61	16.63	0.575	0.655
M	3° TYP		3° TYP	
Q	3.76	4.01	0.148	0.158
R	1.15	1.39	0.045	0.055
S	0.64	0.88	0.025	0.035
U	3.69	3.93	0.145	0.155
V	1.02	—	0.040	—

CASE 77-07
TO-225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current — Continuous — Peak	I_C	2.0 4.0	Adc
Base Current	I_B	0.1	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.5 0.012	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	8.33	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage (1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 100 Vdc, I_B = 0)	I_{CEO}	—	1.0	mAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	0.3	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	0.1	mAdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s, non-repetitive)	$I_{S/b}$	375	—	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 20 mAdc, V_{CE} = 3.0 Vdc) (I_C = 120 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 500 1500	 — —	—
Collector-Emitter Saturation Voltage (I_C = 20 mAdc, I_B = 0.2 mAdc) (I_C = 120 mAdc, I_B = 1.2 mAdc)	$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base-Emitter On Voltage (I_C = 120 mAdc, V_{CE} = 10 Vdc)	$V_{BE(on)}$	—	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (2) (I_C = 0.05 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)	f_T	6.0	—	MHz

NOTES:
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) $f_T = |h_{fe}| \bullet f_{test}$

FIGURE 1 — DC CURRENT GAIN

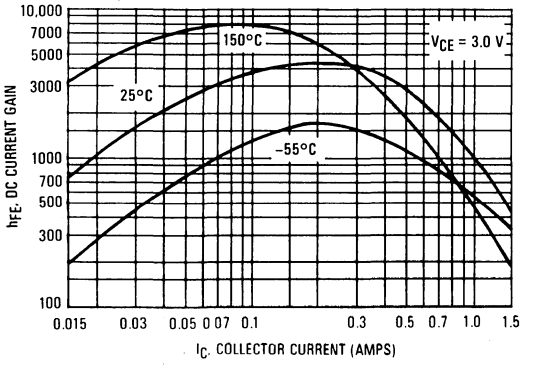
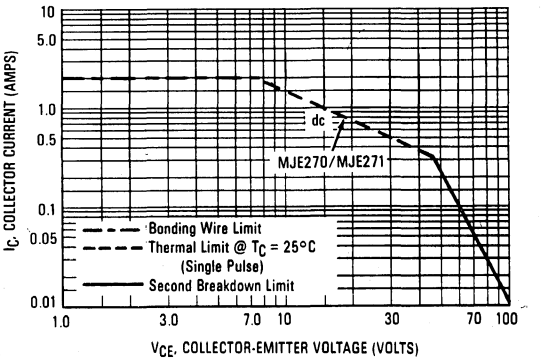
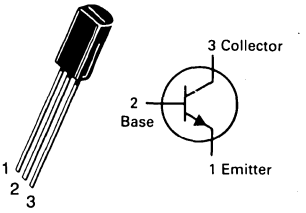


FIGURE 2 — SAFE OPERATING AREA



MPS6717

CASE 29-05, STYLE 1
TO-92 (TO-226AE)



ONE WATT
AMPLIFIER TRANSISTOR
NPN SILICON

Refer to MPSW05 for graphs.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	80	Vdc
Collector-Base Voltage	V_{CBO}	80	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous	I_C	500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.0 8.0	Watt mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	2.5 20	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	50	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage(1) (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	80	—	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	$V_{(BR)CBO}$	80	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	—	Vdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)	I_{CBO}	—	0.1	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	—	10	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 1.0 Vdc) (I_C = 250 mAdc, V_{CE} = 1.0 Vdc)	h_{FE}	 80 50	 — 250	—
Collector-Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 10 mAdc)	$V_{CE(sat)}$	—	0.5	Vdc
Base-Emitter On Voltage (I_C = 250 mAdc, V_{CE} = 1.0 Vdc)	$V_{BE(on)}$	—	1.2	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Collector-Base Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	—	30	pF
Small-Signal Current Gain (I_C = 200 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)	h_{fe}	2.5	25	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

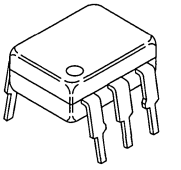
6-Pin DIP Optoisolators
Transistor Output

4N35
4N36
4N37

6-PIN DIP OPTOISOLATORS TRANSISTOR OUTPUT

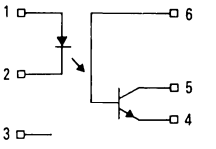
These devices consist of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon phototransistor detector.

- Convenient Plastic Dual-In-Line Package
- High Current Transfer Ratio — 100% Minimum at Spec Conditions
- Guaranteed Switching Speeds
- High Input-Output Isolation Guaranteed — 7500 Volts Peak
- UL Recognized. File Number E54915
- VDE approved per standard 0884/8.87 (Certificate number 62054), with additional approval to DIN IEC380/VDE0806, IEC435/VDE0805, IEC65/VDE0860, VDE0110b, covering all other standards with equal or less stringent requirements, including IEC204/VDE0113, VDE0160, VDE0832, VDE0833, etc. 884
- Meets or Exceeds All JEDEC Registered Specifications
- Special lead form available (add suffix "T" to part number) which satisfies VDE0883/6.80 requirement for 8 mm minimum creepage distance between input and output solder pads.
- Various lead form options available. Consult "Optoisolator Lead Form Options" data sheet for details.



CASE 730A
PLASTIC

SCHEMATIC



1. LED ANODE
2. LED CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT LED			
Reverse Voltage	V_R	6	Volts
Forward Current — Continuous	I_F	60	mA
LED Power Dissipation @ T_A = 25°C with Negligible Power in Output Detector	P_D	120	mW
Derate above 25°C		1.41	mW/°C
OUTPUT TRANSISTOR			
Collector-Emitter Voltage	V_{CEO}	30	Volts
Emitter-Base Voltage	V_{EBO}	7	Volts
Collector-Base Voltage	V_{CBO}	70	Volts
Collector Current — Continuous	I_C	150	mA
Detector Power Dissipation @ T_A = 25°C with Negligible Power in Input LED	P_D	150	mW
Derate above 25°C		1.76	mW/°C
TOTAL DEVICE			
Isolation Source Voltage (1) (Peak ac Voltage, 60 Hz, 1 sec Duration)	V_{ISO}	7500	Vac
Total Device Power Dissipation @ T_A = 25°C	P_D	250	mW
Derate above 25°C		2.94	mW/°C
Ambient Operating Temperature Range	T_A	−55 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Soldering Temperature (10 seconds, 1/16" from case)	—	260	°C

(1) Isolation surge voltage is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
INPUT LED						
Forward Voltage (I_F = 10 mA)	T_A = 25°C T_A = −55°C T_A = 100°C	V_F	0.8 0.9 0.7	1.15 1.3 1.05	1.5 1.7 1.4	V
Reverse Leakage Current (V_R = 6 V)		I_R	—	—	10	μA
Capacitance (V = 0 V, f = 1 MHz)		C_J	—	18	—	pF
OUTPUT TRANSISTOR						
Collector-Emitter Dark Current (V_{CE} = 10 V, T_A = 25°C) (V_{CE} = 30 V, T_A = 100°C)		I_{CEO}	— —	1 —	50 500	nA μA
Collector-Base Dark Current (V_{CB} = 10 V)	T_A = 25°C T_A = 100°C	I_{CBO}	— —	0.2 100	20 —	nA
Collector-Emitter Breakdown Voltage (I_C = 1 mA)		$V_{(BR)CEO}$	30	45	—	V
Collector-Base Breakdown Voltage (I_C = 100 μA)		$V_{(BR)CBO}$	70	100	—	V
Emitter-Base Breakdown Voltage (I_E = 100 μA)		$V_{(BR)EBO}$	7	7.8	—	V
DC Current Gain (I_C = 2 mA, V_{CE} = 5 V)		h_{FE}	—	400	—	—
Collector-Emitter Capacitance (f = 1 MHz, V_{CE} = 0)		C_{CE}	—	7	—	pF
Collector-Base Capacitance (f = 1 MHz, V_{CB} = 0)		C_{CB}	—	19	—	pF
Emitter-Base Capacitance (f = 1 MHz, V_{EB} = 0)		C_{EB}	—	9	—	pF
COUPLED						
Output Collector Current (I_F = 10 mA, V_{CE} = 10 V)	T_A = 25°C T_A = −55°C T_A = 100°C	I_C	10 4 4	30 — —	— — —	mA
Collector-Emitter Saturation Voltage (I_C = 0.5 mA, I_F = 10 mA)		$V_{CE(sat)}$	—	0.14	0.3	V
Turn-On Time	(I_C = 2 mA, V_{CC} = 10 V, R_L = 100 Ω, Figure 11)	t_{on}	—	7.5	10	μs
Turn-Off Time		t_{off}	—	5.7	10	
Rise Time		t_r	—	3.2	—	
Fall Time		t_f	—	4.7	—	
Isolation Voltage (f = 60 Hz, t = 1 sec)		V_{ISO}	7500	—	—	Vac(pk)
Isolation Current (V_{I-O} = 3550 Vpk) (V_{I-O} = 2500 Vpk) (V_{I-O} = 1500 Vpk)	4N35 4N36 4N37	I_{ISO}	— — —	— — 8	100 100 100	μA
Isolation Resistance (V = 500 V)		R_{ISO}	10^{11}	—	—	Ω
Isolation Capacitance (V = 0 V, f = 1 MHz)		C_{ISO}	—	0.2	2	pF

TYPICAL CHARACTERISTICS

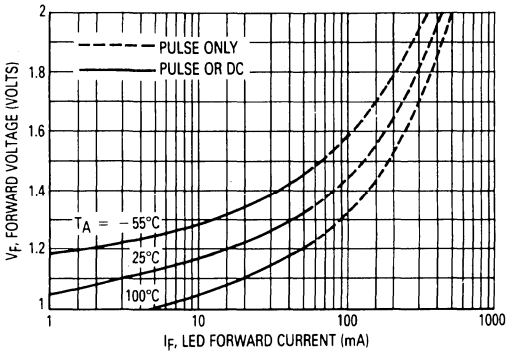


Figure 1. LED Forward Voltage versus Forward Current

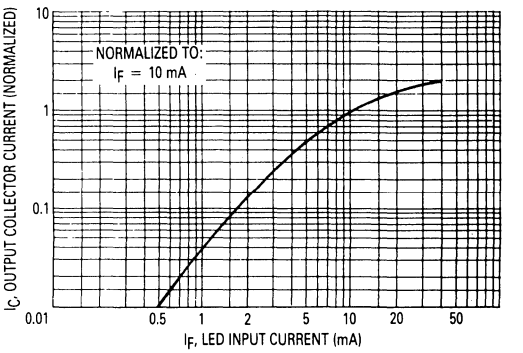


Figure 2. Output Current versus Input Current

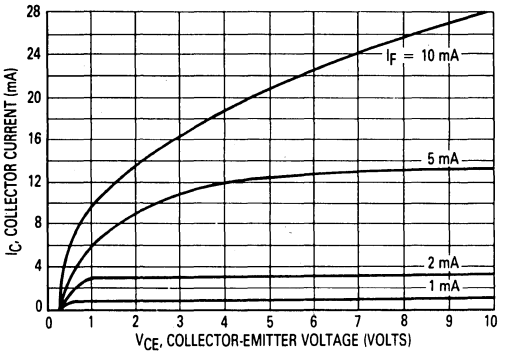


Figure 3. Collector Current versus Collector-Emitter Voltage

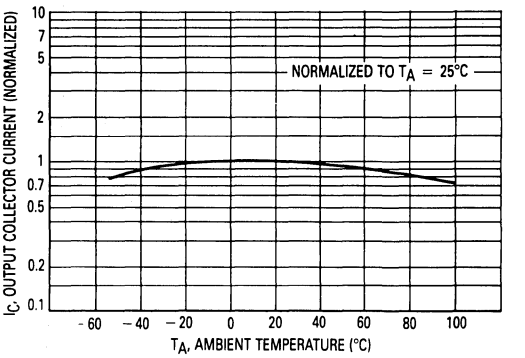


Figure 4. Output Current versus Ambient Temperature

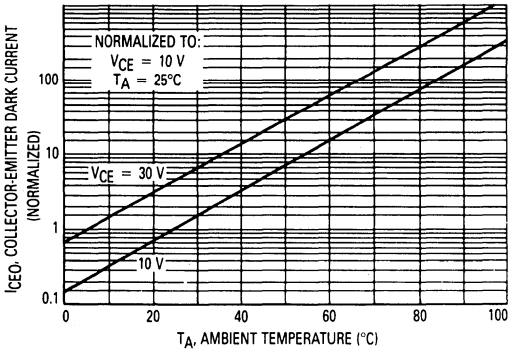


Figure 5. Dark Current versus Ambient Temperature

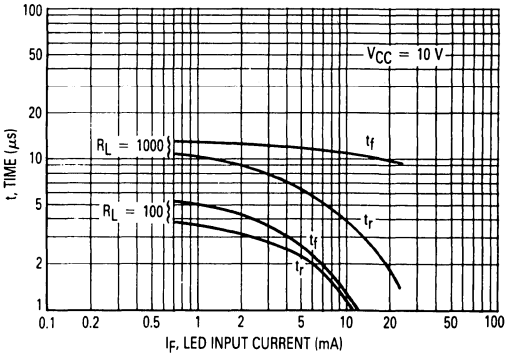


Figure 6. Rise and Fall Times

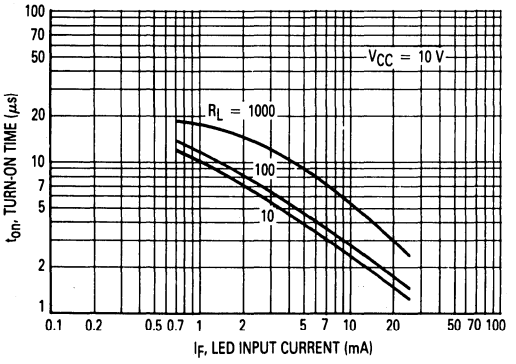


Figure 7. Turn-On Switching Times

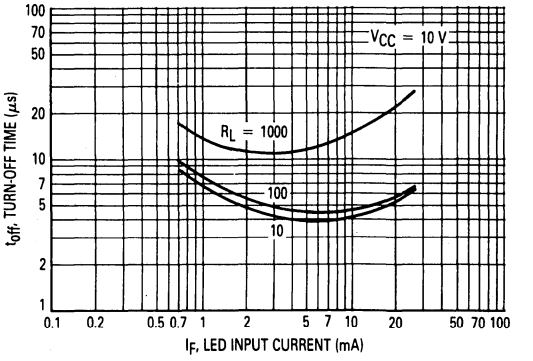


Figure 8. Turn-Off Switching Times

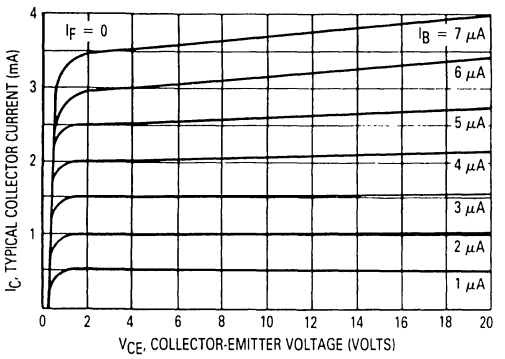


Figure 9. DC Current Gain (Detector Only)

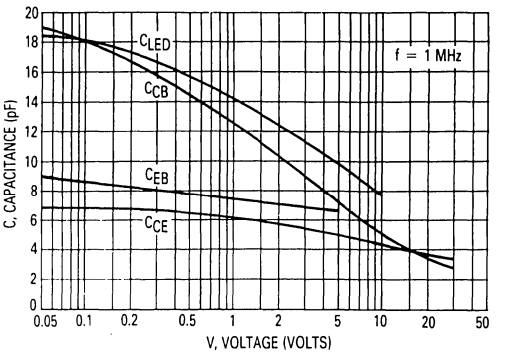


Figure 10. Capacitances versus Voltage

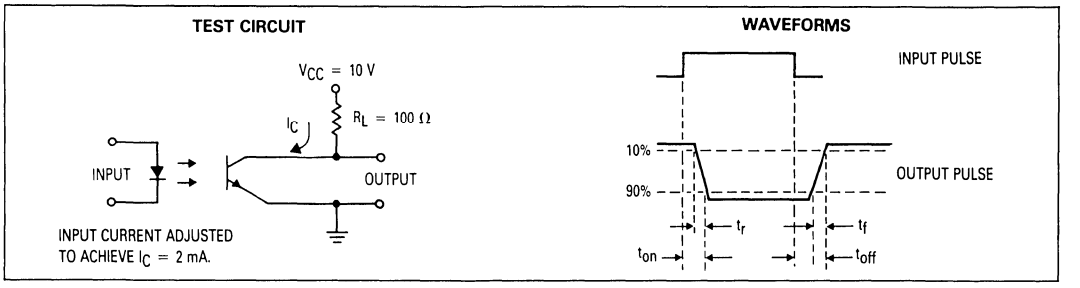
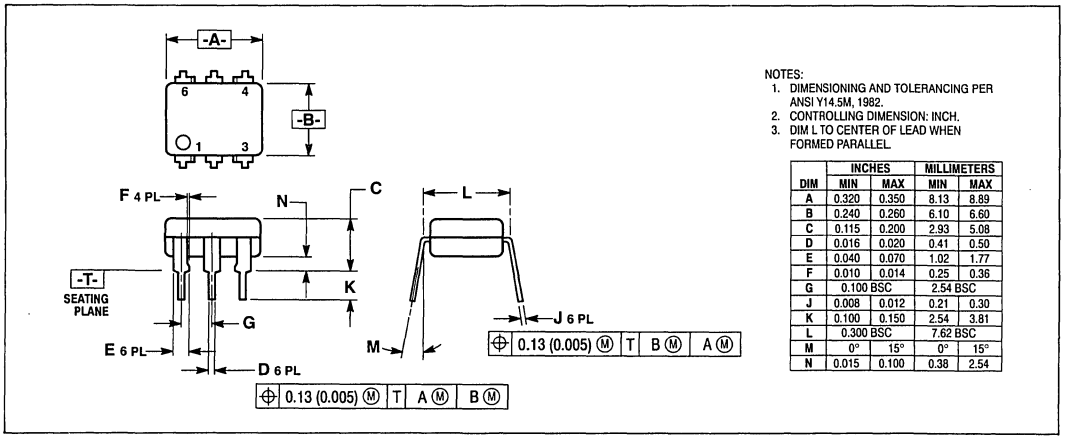


Figure 11. Switching Times

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.015	0.100	0.38	2.54

Evaluation Kits 3

3

MC145190EVK
MC145191EVK

Advance Information

1.1 GHz PLL Frequency Synthesizer Evaluation Kit

The MC145190EVK and MC145191EVK are two versions of the same board that allow evaluation and demonstration of the Motorola MC145190 and MC145191 Frequency Synthesizers. The MC145190/91EVK is factory populated and tested with the MC145191 PLL as the active device. A sample of the MC145190 PLL is included in the kit for those who wish to evaluate this device. In addition, the board may be modified to evaluate the MC145192.

MC145190/91EVK FEATURES

General:

- Turnkey Design Includes PLL Devices, Low-Pass Filter, and Voltage Controlled Oscillator
- Boards Are Controlled by Any IBM PC Compatible Computer Through the Printer Port
- Up to Three EVK Boards Can Operate Independently from One Printer Port
- Two or Three Board Cascades Are Constructed with Only Three Output Lines (Clock, Data, and Load) from the Printer Card
- Contains All Components for Use of Either an External or On-Board Crystal Reference
- Five-Element Loop Filter Included
- Includes Full Documentation, Including MC145190/91EVK User Guide and MC145190/91 and MC145192 Data Sheets

Software:

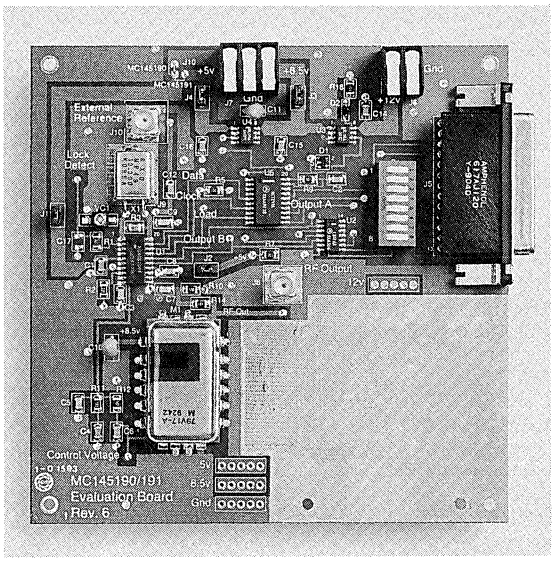
- Menu-Driven Control Program Written in Turbo Pascal with Source Code Provided on a 3.5″ PC Compatible Disk
- Frequency Range of Operation, Step Size, and Reference Frequency Can Be Changed in the Control Program
- Byte-Oriented Format Is Used to Allow for Easy PLL Programming

MC145190/MC145191:

- Single-Package Synthesizers with Serial Interfaces Capable of Direct Usage up to 1.1 GHz
- Interfaces are Both SPI and MICROWIRE™ Compatible
- No Address or Steering Bits are Required Because of Patented BitGrabber™ Registers
- Gain of Current Source/Sink Phase/Frequency Detectors Controllable via Serial Port
- 7 mA Dynamic Current Consumption

BitGrabber is a trademark of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.
This document contains information on a new product. Specifications and information herein are subject to change without notice.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



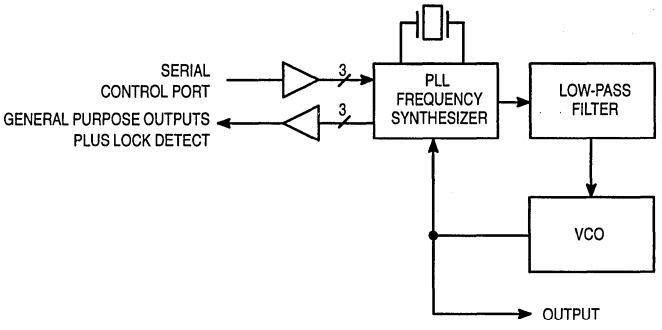


Figure 1. MC145190/91EVK Functional Block Diagram

MC145460EVK

Advance Information

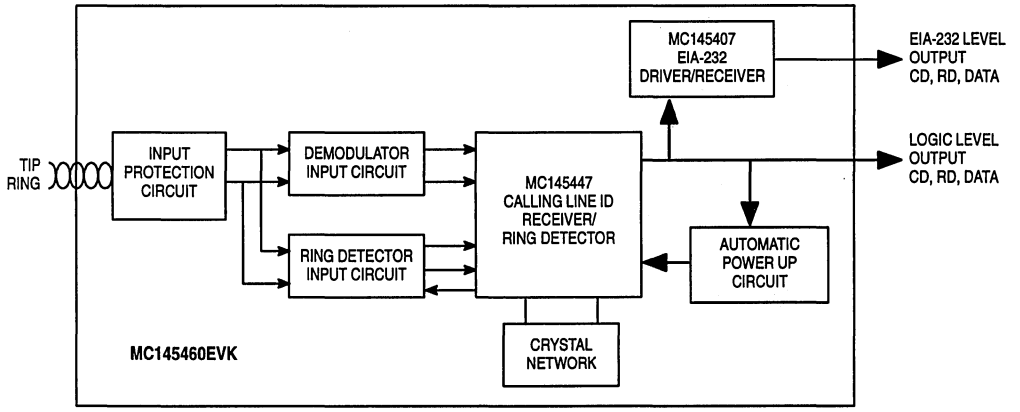
Calling Line I.D. Receiver Evaluation Kit

The MC145460EVK is a low cost evaluation platform for the MC145447 Calling Line I.D. Receiver with Ring Detector. The MC145460EVK will facilitate development and testing of products that support the Bellcore customer premises equipment (CPE) data interface, which enables services such as Calling Number Delivery (CND). The MC145447 can be easily incorporated into any telephone, FAX, PBX, key system, answering machine, CND adjunct box or other telephone equipment with the help of the MC145460EVK development kit.

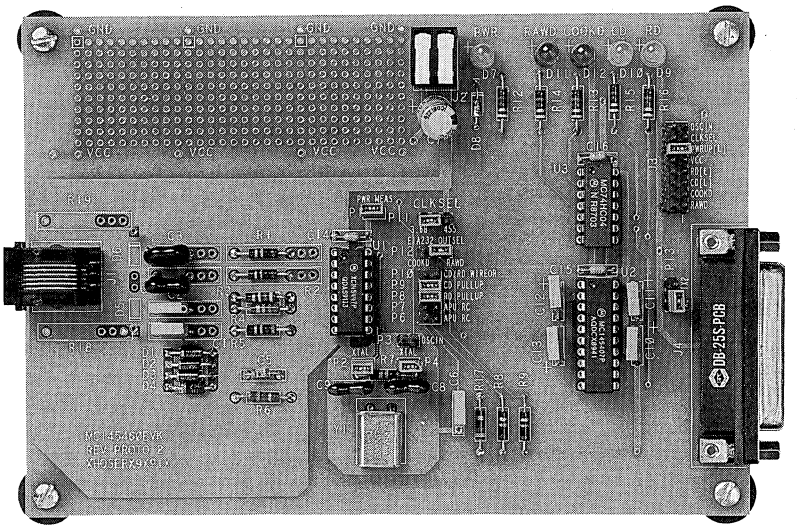
MC145460EVK FEATURES

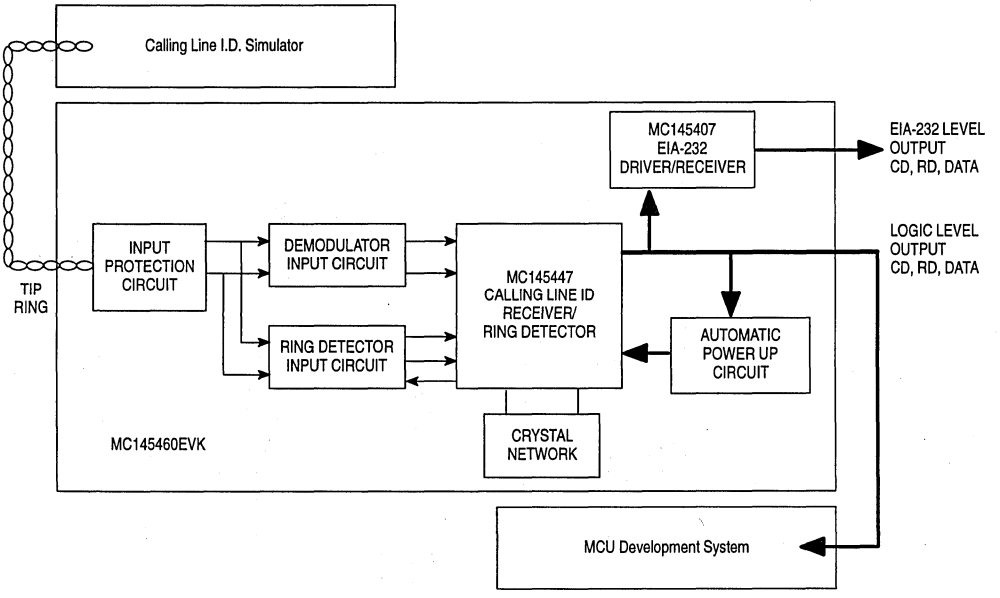
- Easy clip on access to key MC145447 signals
- Generous prototype area
- Configurable for MC145447 automatic or external power up control
- EIA-232 and logic level ports for connection to any PC or MCU development platform
- Carrier Detect, Ring Detect and Data status LEDs
- Component layout for input protection circuit
- Documentation: MC145460EVK User Guide, MC145447 Data Sheet
- Additional MC145447 sample

MC145460EVK Block Diagram



This document contains information on a new product. Specifications and information herein are subject to change without notice.





Calling Line I.D. Product Development System

MC14LC5494EVK

Advance Information

ISDN U-Interface Transceiver Evaluation Board

The MC14LC5494EVK is the evaluation platform for the MC14LC5472 ISDN Basic Rate Access Transceiver. The MC14LC5494EVK provides the user with the necessary hardware and software needed to evaluate the many separate configurations under which the MC1454742 is intended to operate.

General

- Functionally equivalent to preceeding MC145494EVK
- Provides Stand Alone NT1 and LT on Single Board
- Board Can Be Broken Apart Providing Separate NT1 and LT
- On Board microcontrollers with Resident Monitor Software
- Convenient Access to Key Signals
- NT1 and LT Software Development Platform
- Conforms to ANSI T1.601 (U-Interface) and CCITT I.430 (S/T-Interface)

Hardware

- Utilizes the MC145474 S/T-Interface Transceiver and the MC145472 U-Interface Transceiver
- +5 V Only Power Supply
- "Push Button" Activation of U-Interface from NT1 or LT
- Stand Alone Operation for Bit Error Rate Testing
- Gated Data Clocks Provided for Bit Error Rate Testing
- Interfaces Directly to M68302ADS IMP Evaluation Board
- Can Be Used as U- or S/T-Interface Terminal Development Tool
- On Board 5-ppm LT Frequency Reference
- EIA-232 Serial Port(s) for Terminal Interface

Software

- Stand Alone or Terminal Operation
- Resident Firmware Monitor for User Control of Board
- Device Driver for Serial Control Port Interface
- Help Menu
- Microcontroller Controlled or Automatic Activation/Deactivation
- Access to All Maintenance Channels
- MC68HC05 Assembly Language Source Code Available

This document contains information on a new product. Specifications and information herein are subject to change without notice.
BitGrabber is a trademark of Motorola Inc. MICROWIRE is a trademark of National Semiconductor Corp.

GENERAL OVERVIEW

The MC14LC5494EVK U-Interface Evaluation Kit provides Motorola ISDN customers a convenient and efficient vehicle for evaluation of the MC14LC5472 ISDN U-Interface Transceiver. The approach taken to demonstrate the MC14LC5472 ISDN U-Interface Transceiver is to provide the user with a fully functional NT1 (Network Termination TYPE 1) connected to an LT (Line Termination). An NT1 provides transparent 2B+D data transfer between the U- and S/T-Interfaces. In addition, it also provides for customer and network initiated maintenance procedures. It does not, however, provide any interface to higher level protocols—this functionality is left to entities such as the NT2 (Network Termination TYPE 2).

The MC14LC5494EVK ISDN U-Interface Evaluation Kit can be physically and functionally separated into two "halves." The left side of the card is the NT1 side, while the right side of the card is the LT side. Alternatively, it can be thought of as having both ends of the two-wire U-Interface, extending from the customer premise (NT1) to the switch line card (LT) on one board.

The kit provides the ability to interactively manipulate status registers in the MC14LC5472 ISDN U-Interface Transceiver as well as in the MC145474/75 S/T Interface Transceiver with the aid of an external terminal. A unique combination of hardware and software features allows for stand-alone or terminal activation of the U-Interface, providing an excellent platform for NT1 and LT software development.

The MC14LC5494EVK ISDN U-Interface Evaluation Kit can also be controlled using the MC68302 IMP Evaluation Board, thus completing a total Basic Rate ISDN evaluation solution with the Motorola MOS Digital/Analog ISDN product line.

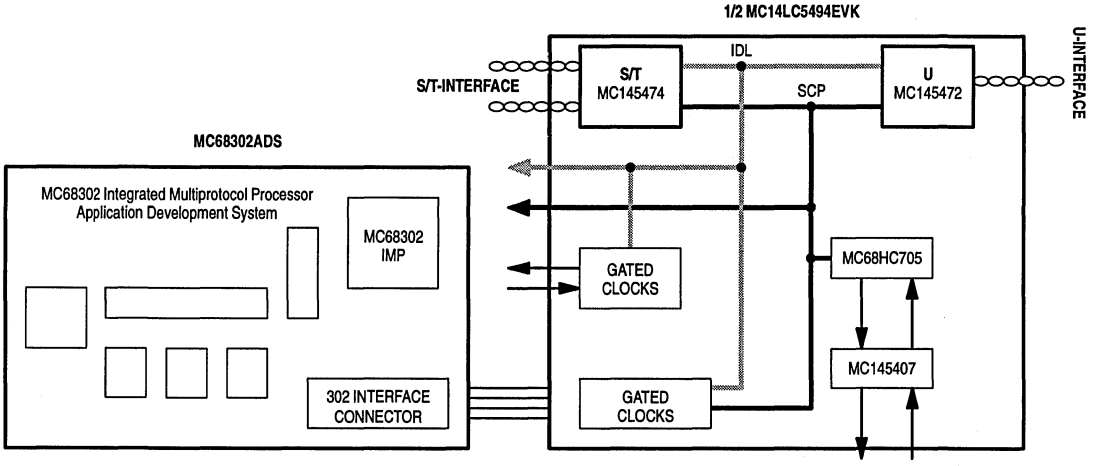


Figure 1. U-Interface Terminal or S/T-Interface Terminal Development Platform

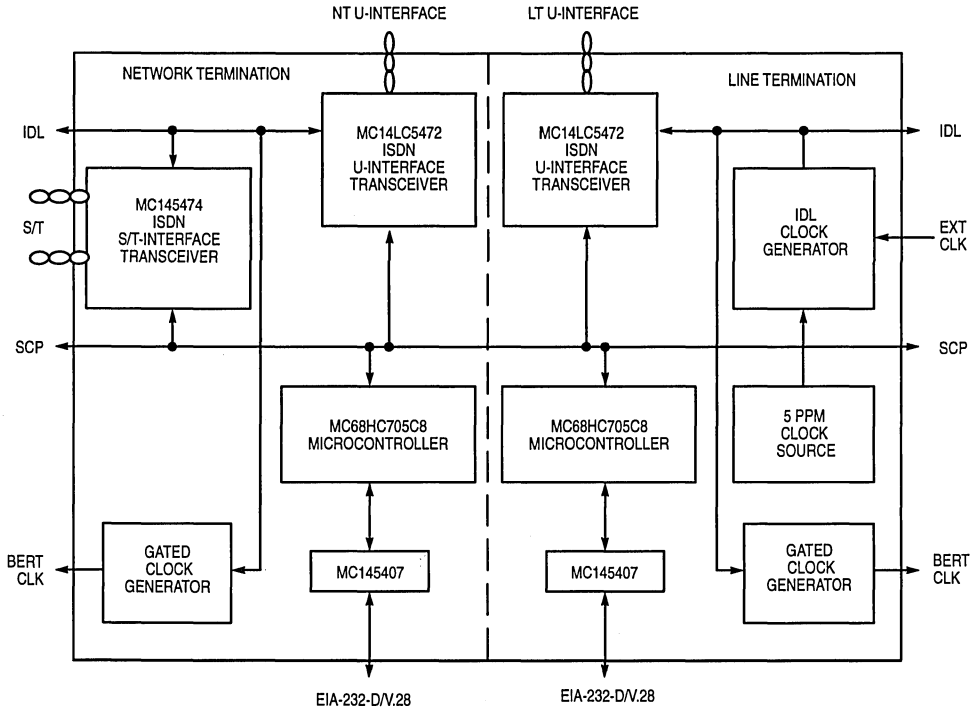


Figure 2. MC14LC5494EVK Block Diagram

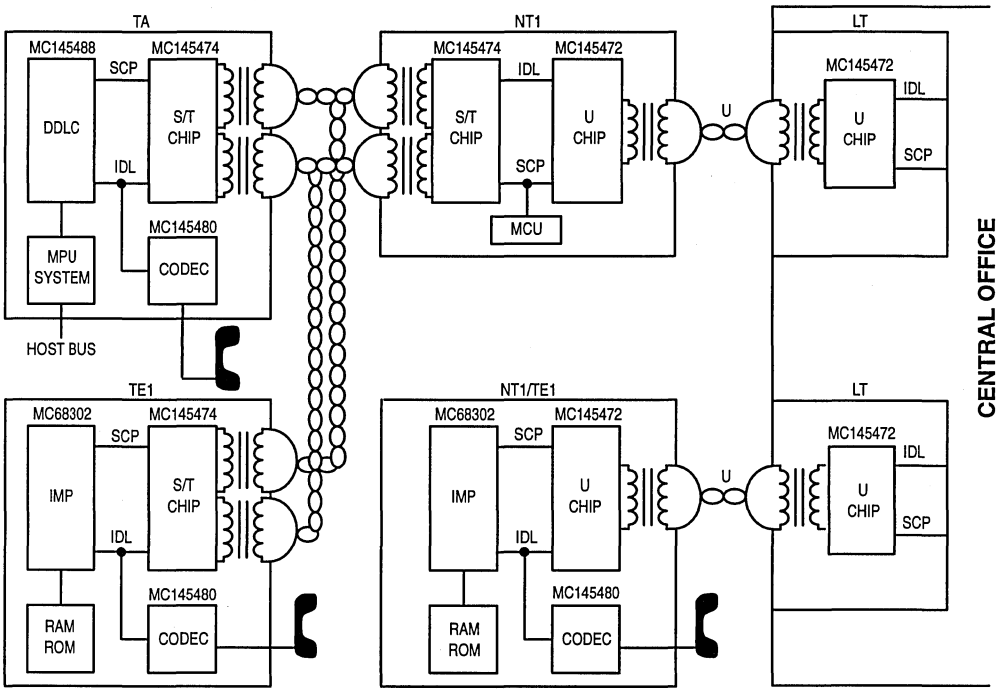


Figure 3. Motorola ISDN Solution

MC145536EVK

Advance Information

Codec-Filter/ADPCM Transcoder Evaluation Kit

The MC145536EVK is the primary tool for evaluation and demonstration of the MC145480 Single +5 V Supply PCM Codec-Filter and the MC145532 ADPCM Transcoder. The MC145536EVK provides the user with the hardware needed to evaluate the many separate operating modes under which the MC145480 and MC145532 are intended to operate.

General

- Provides Stand Alone Evaluation on Single Board
- +5 V Only Power Supply
- Easily Interfaced to Test Equipment, Customer System, Second MC145536EVK or MC145537EVK
- Convenient Access to Key Signals
- Generous Prototype Area for Application Development
- The kit provides analog-to-analog, analog-to-digital (64 kbps PCM; 32, 24, or 16 kbps ADPCM) or digital- (64 kbps PCM; 32, 24, or 16 kbps ADPCM) to-analog connections
- Handset Included
- Schematics, Data Sheets, and User's Manual Included

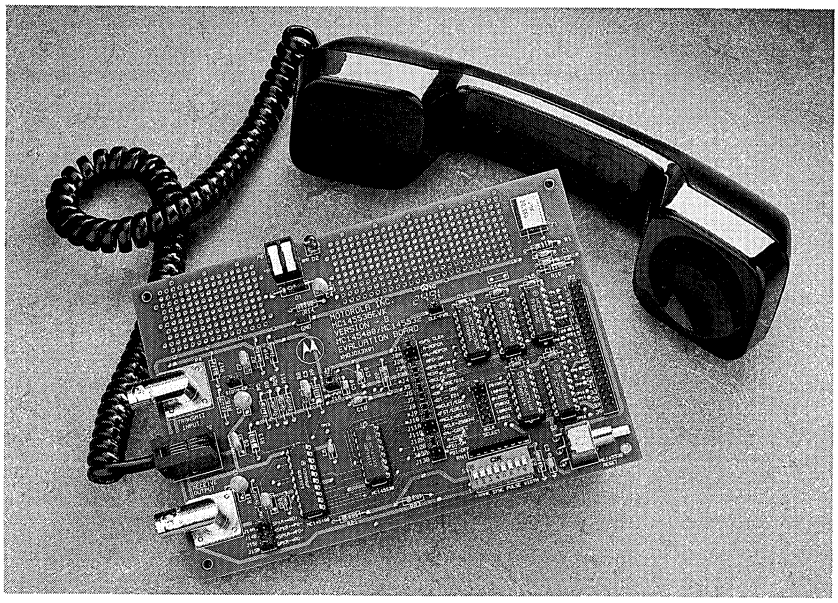
MC145480

- Single +5 V Power Supply
- Typical Power Dissipation of 25 mW, Power Down of <1 mW
- Conforms to CCITT and Bell Specifications
- Mu-Law or A-Law Companding
- Differential Analog Circuit Design for Lowest Noise
- 20-Pin Plastic Package
- Production in 1.5 Micron CMOS Process
- UDR Design Layout Rules for Core Cell Applications

MC145532

- Single-Chip Full-Duplex PCM-to-ADPCM Encoder and ADPCM-to-PCM Decoder
- Achieves High Audio Quality at Reduced Bit Rates
- PCM Data Rate of 64 kbps
- ADPCM Data Rates of 32, 24, or 16 kbps
- Conforms to CCITT and ANSI ADPCM Standards
- Custom DSP Engine Optimized for ADPCM Algorithm
- Volume Production in 1.5 Micron CMOS Process
- UDR Design Layout Rules for Core Cell Applications

This document contains information on a new product. Specifications and information herein are subject to change without notice.



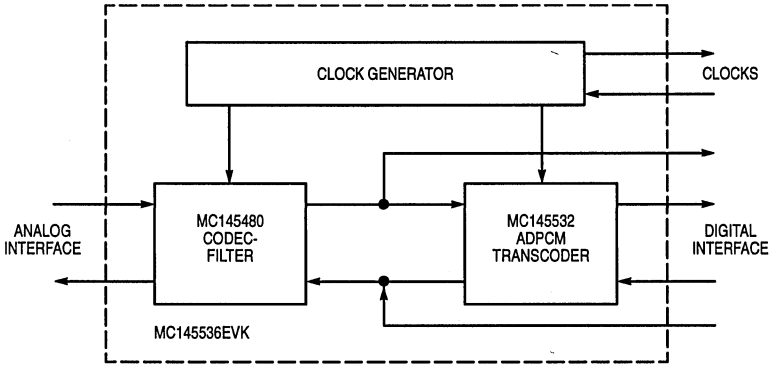


Figure 1. MC145536EVK System-Level Block Diagram

MC145537EVK

Advance Information

MC145540 ADPCM Codec Evaluation Kit

The MC145537EVK is the evaluation platform for the MC145540 ADPCM Codec. This board provides the clock generator circuitry and microcontroller interface to facilitate the evaluation of the MC145540.

MC145537EVK Hardware Features

- Supports MC145540 +5 V or +3 V Operation
- Handset Interface/Handset Included
- Easy Access to all Analog and Digital Data, Clock, and Enable Signals
- EIA-232-D/ V.28 Terminal Control
- Analog-to-Digital (64 kbps PCM; 32, 24, or 16 kbps ADPCM) Path
- Digital- (64 kbps PCM; 32, 24, or 16 kbps ADPCM) to-Analog Path
- Supports Hardware Loopbacks
  - Analog-to-Analog
  - Digital-to-Digital
- Ability to Connect Two MC145537EVKs Back-to-Back
- Ability to Connect MC145537EVK and MC145536EVK Back-to-Back for +5 V Operation Only

MC145537EVK Software Features

- MC68HC705C8 Resident Monitor
- Stand Alone or Terminal Operation
- Device Driver for Serial Control Port Interface
- Ability to Read/Write SCP Registers in MC145540
- Registers Can Be Individually Displayed and Modified
- Help Menu

This document contains information on a new product. Specifications and information herein are subject to change without notice.

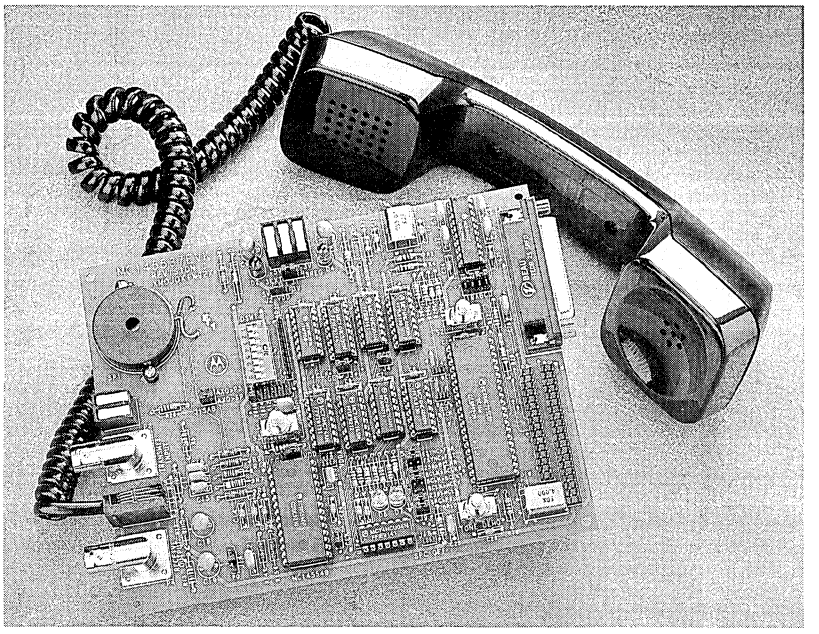
GENERAL OVERVIEW

The MC145540 ADPCM Codec is a single-chip implementation of a PCM Codec-Filter and an ADPCM Encoder/Decoder, and therefore provides an efficient solution for applications requiring the digitization and compression of voiceband signals. This device is designed to operate over a wide voltage range, 2.7 to 5.25 V, and as such is ideal for battery powered as well as ac powered applications. The MC145540 ADPCM Codec also includes a serial control port and internal control and status registers that permit a microcomputer to exercise many built-in features.

The MC145540 ADPCM Codec is designed to meet the 32 kbps ADPCM conformance requirements of CCITT Recommendation G.721 and ANSI T1.301. It also meets ANSI T1.303 and CCITT Recommendation G.723 for 24 kbps ADPCM operation, and the 16 kbps ADPCM standard, CCITT Recommendation G.726. This device also meets the 64 kbps PCM conformance specification of the CCITT G.714 Recommendation.

The MC145537EVK is the evaluation board for the MC145540 ADPCM Codec. This board provides the clock generation that controls both the transfer of PCM and ADPCM data into and out of the MC145540, as well as determining the data compression rate (16 kbps ADPCM, 24 kbps ADPCM, 32 kbps ADPCM, or 64 kbps PCM) for the ADPCM transcoder function. This data compression rate is determined by the duration of the transmit and receive frame synchronization pulses measured in data clock cycles, which are programmed by an 8-position dip switch. This evaluation board has voltage level shifters that allow the MC145540 to operate at a voltage lower than the +5 V supply required for the clock generator and microcontroller.

This MC145537EVK has an MC68HC705C8P microcontroller, which is running a monitor routine that interfaces the MC145540 to a 9600 bps EIA-232 port for access by a computer terminal. The microcontroller provides access to the programming registers of the MC145540 for read and write operations. This facilitates exercising both the hardware options for trim gain, sidetone, analog signal routing and charge-pump operation, and the software options of the dual tone generator, noise burst detect and receive gain control. The evaluation board is designed to configure the MC145540 after reset such that the charge-pump is operating and the device is encoding and decoding analog at the rate determined by the clock circuitry. This allows the MC145537EVK to be functional without a computer terminal.



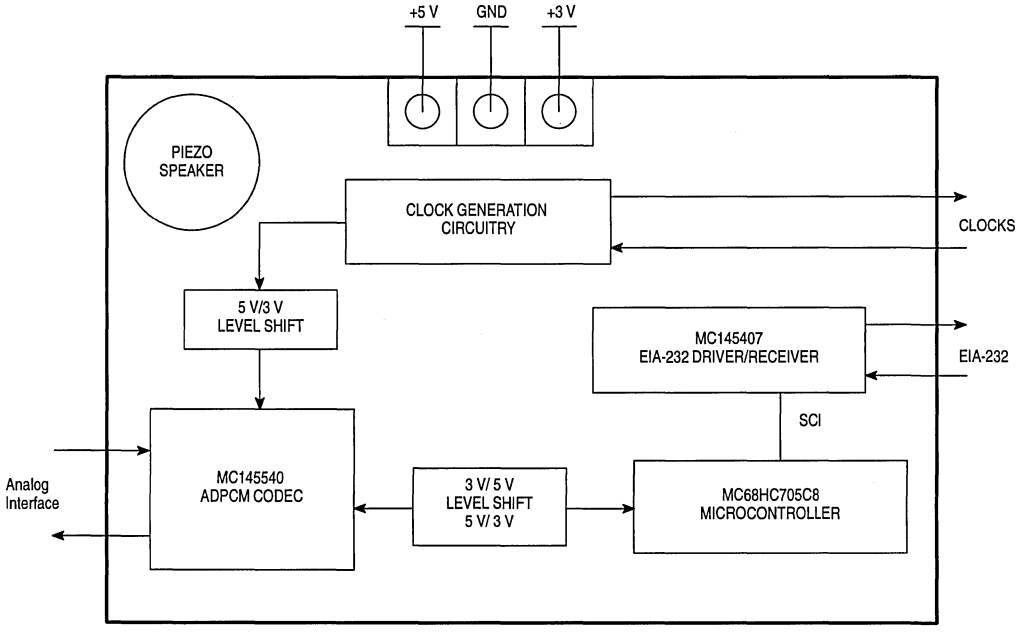


Figure 1. MC145537EVK Block Diagram

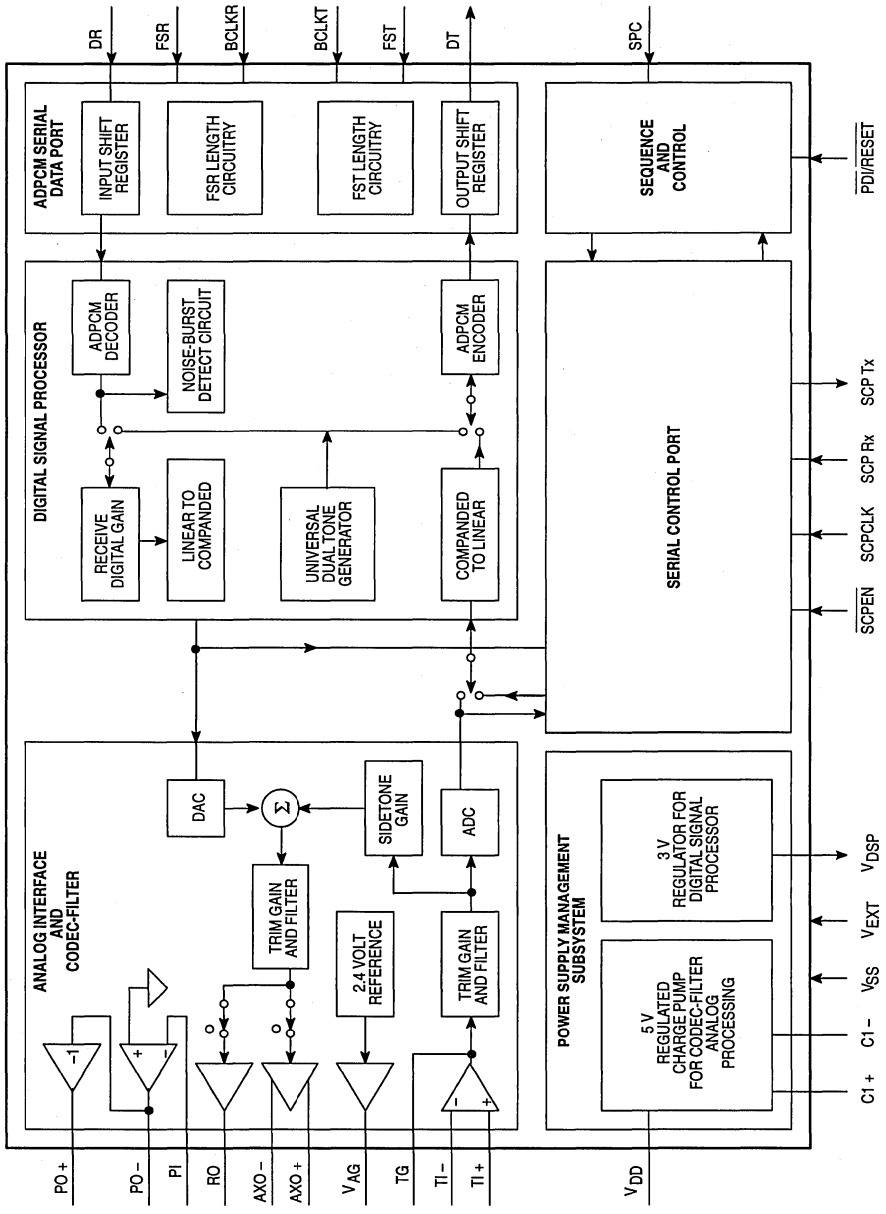


Figure 2. MC145540 ADPCM Codec Block Diagram

Telecom

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MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN-872
Application Note

MC14402 MONO-CIRCUIT APPLICATIONS INFORMATION

by
Richard L. Hall and Michael D. Floyd
Telecom Systems Engineering

This application note is intended to ease customer evaluation of the Motorola MC14402 PCM mono-circuit, particularly when using the Motorola Mono-circuit Evaluation Board. Schematics and artwork of this board are given as well as layout guidelines for designing the mono-circuit into a custom PC board. Analog testing considerations are mentioned to help sidestep some of the troublesome aspects of codec/filter evaluations.

EVALUATION BOARD DESCRIPTION

The Motorola Mono-circuit Evaluation Board is a small PC board that contains all necessary clock circuitry for operating the MC14402. Coaxial connectors allow access to the analog input/output ports and the only other connections required are to the three power terminals—V_{DD}, V_{SS} and V_{AG}. The schematic for this board is shown in Figure 1 while the artwork is given in Figure 2.

The clock circuitry uses a 2.048 Mhz crystal to produce the 2.048 Mhz data clock as well as the 8 kHz sync signal. The 8 kHz sync is an 8-data-clock-wide pulse that is connected to the RCE, TDE and MSI inputs of the mono-circuit. RCE and TDE are the receive and transmit enables respectively, while MSI is the 8 kHz reference input. The 8 kHz sync is generated by the MC14417 TSAC (Time Slot Assigner Circuit).

Options are available to help evaluate different channel parameters. These include:

* 600 or 900 ohm channel impedance
* RSI peak overload voltage of 3.15 or 3.78 volts
* TTL or CMOS logic levels
* Transmit and Receive gain adjustment ($\overline{RxO}$ gain only)
* A or MU-law coding
* Power-down capability

These options are selected by solderable wire straps (S1-S6) as described in the Strapping Information Chart. The straps can be replaced by DIP switches if desired and can be obtained from:

Grayhill Inc.
561 Hillgrove Avenue
La Grange, Illinois 60525

P/N	Name	Qty
78J05	S1	1
78J02	S2,S3	2
78J01	S4-S6	3

Figure 3 shows the physical location of the strap points as well as the component layout. The solid lines indicate the normal strap positions as shipped from the factory which select Mu-law, 900 ohm, CMOS, 3.78 volts peak operation. The straps E1-E10 allow reprogramming of the clock lines to provide different clock schemes. Refer to the schematic in Figure 1 for changing these straps.

TEST CONSIDERATIONS

Input/Output Levels

Obtaining valid test data is highly dependent upon establishing the proper input/output voltage levels. However, this can be a somewhat confusing task since the mono-circuit can use three different peak overload voltages—2.5, 3.1 and 3.8 volts. The evaluation board permits selection of either 3.1 or 3.8 volts. For 3.1 volts, the proper input/output level for a 0 dBm0 test signal is +6 dBm/600 ohms (1.5455 volts rms). For 3.8 volts, 0 dBm0 corresponds to +6 dBm/900 ohms (1.893 volts rms). Usually, measurement levels are referenced

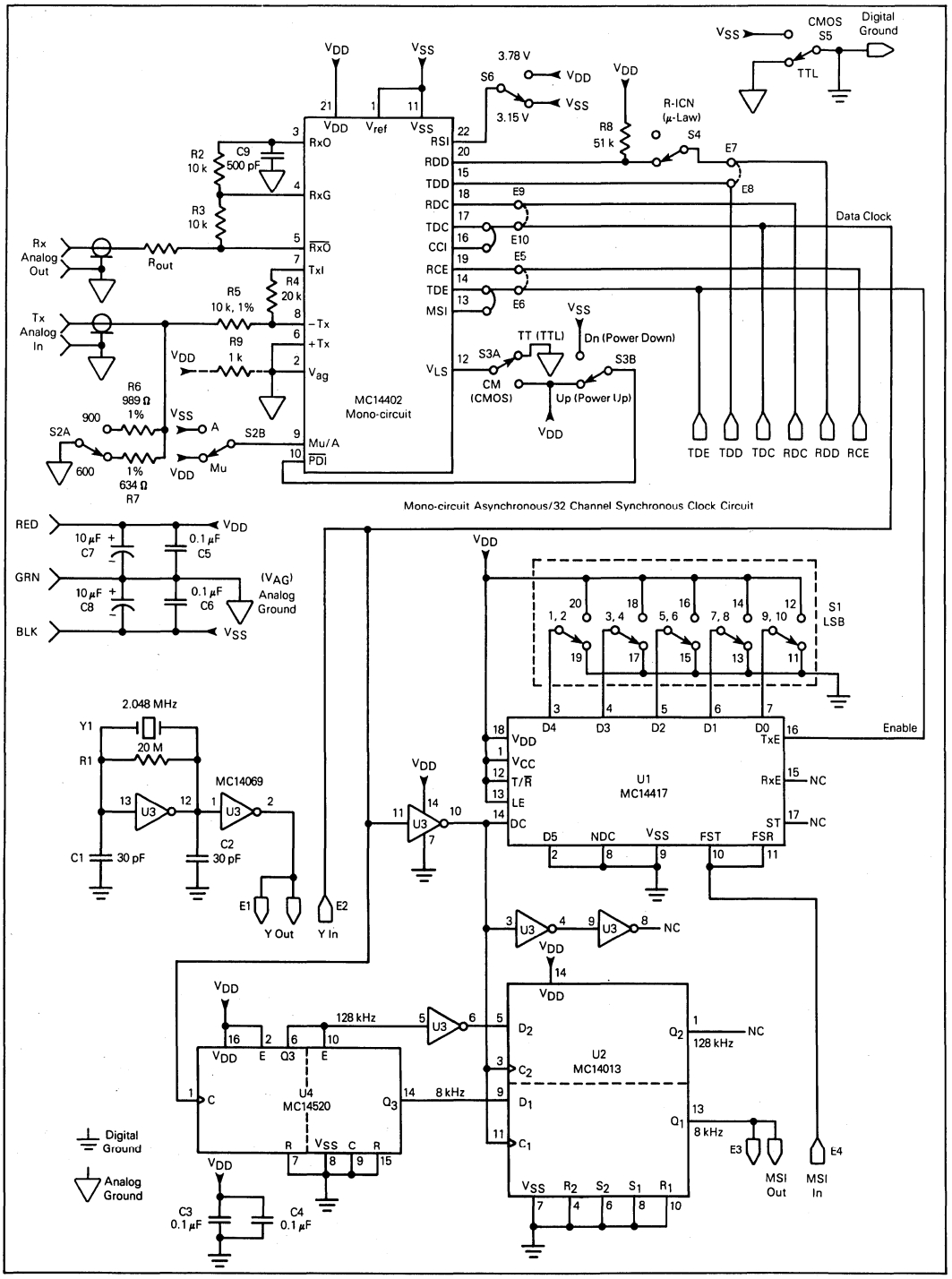


FIGURE 1 — MC14402 Switch Programmable Evaluation Board P/N 618-1030

to 0 dBm0 to avoid possible confusion over absolute levels. For example, an absolute idle noise measurement of 21 dBrnC becomes 15 dBrnC0 when referenced to 0 dBm0 (where 0 dBm0 = +6 dBm in our system).

Noise

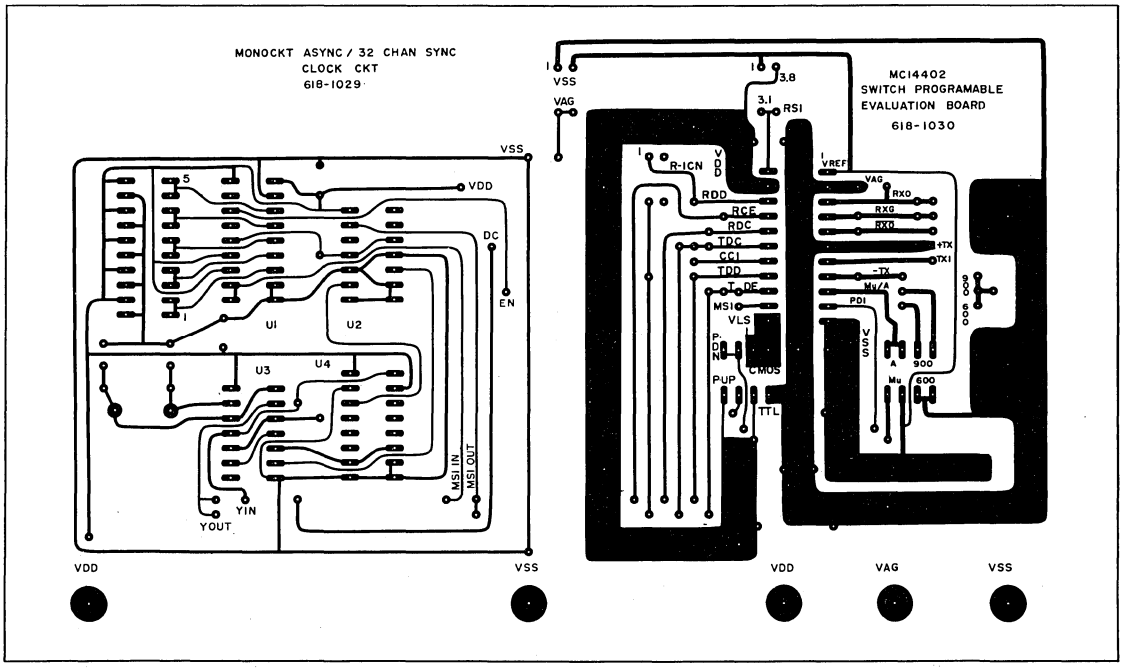
Special care has been taken in the layout of the evaluation board to minimize noise corruption. The analog and digital sections are isolated from each other and bypassing is present to reduce high frequency noise. The use of shielded cable for analog test lines is recommended to prevent extraneous environmental noise pickup as well as the use of a power supply reasonably free of high frequency noise. A 500 pF capacitor has been put on the RxO output to bypass any radiated asynchronous noise that might be picked up at this node.

Test Equipment

There are many different pieces of telecommunications test gear on the market and most will be more than adequate for testing codec/filter parameters. However, the use of wideband measurement devices for such tests as quantizing distortion and gain tracking should be avoided since these parameters involve very low voltage levels that require a selective voltmeter function for accurate results. Also, attention should be given to correct selection of input/output parameters on programmable test gear such as the Hewlett-Packard 3779 PMA and others.

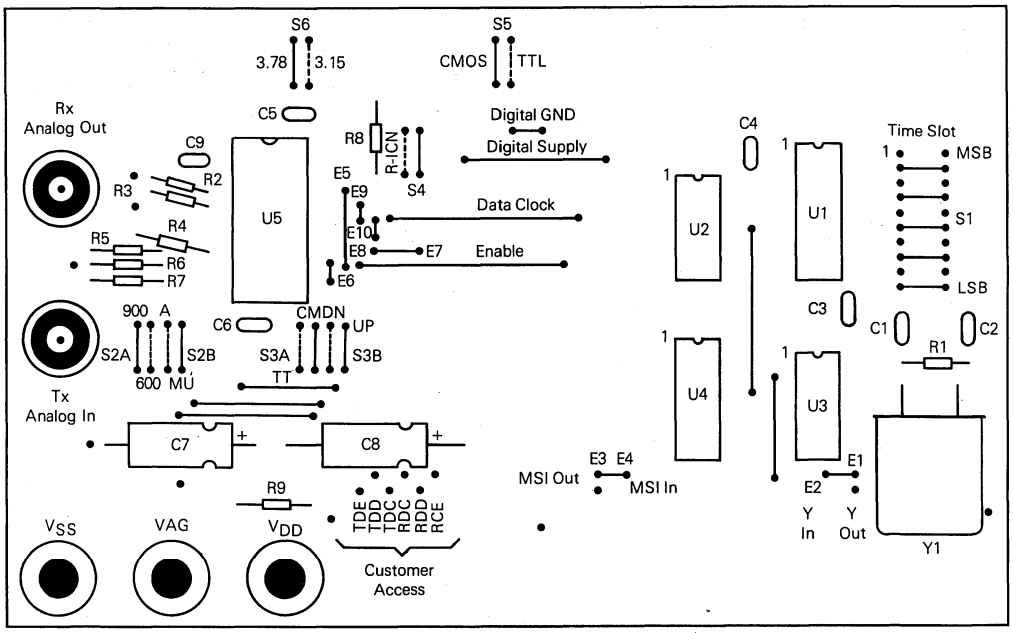
LAYOUT GUIDELINES FOR PC BOARDS

* Bypassing of both V_{DD} and V_{SS} to V_{AG} with 0.1 microfarad ceramic capacitors (or any other capacitors with good high frequency behavior) as close to the part as possible.
* Isolate analog lines from digital sections. The monocircuit pinout facilitates this by keeping digital and analog pins on opposite sides of the chip.
* Use gain-setting resistors in the range of 50 kΩ > R > 5 kΩ to avoid high impedance nodes in the analog section.
* If V_{LS} is tied to V_{AG} for TTL level selection, then this connection should be a short, direct, low inductance trace.
* In a dual supply environment, V_{DD} and V_{SS} should be connected before V_{AG} (ground).



NOTE: Drawings are not actual size.

FIGURE 2 — Evaluation Board Artwork



NOTE: Solid line indicates normal strapping as shipped from factory; dashed lines indicate optional straps as described below in the Strapping Information Chart.

Reference Voltage (S6)	Reference Impedance (S2A)	Input/Output Levels (dBm)	R2	R3	R4	R5	R_{out}*
3.15 V	600 Ω	+6/+6	–	–	10 k	10 k	Jumper
		+6/0	–	–	10 k	10 k	600 Ω
		0/0	–	–	20 k	10 k	600 Ω
	900 Ω	0/0	16.6 k	10 k	16.6 k	10 k	Jumper
3.78 V	900 Ω	+6/+6	–	–	10 k	10 k	Jumper
		+6/0	–	–	10 k	10 k	900 Ω
		0/0	–	–	20 k	10 k	900 Ω
	600 Ω	0/0	12.5 k	10 k	25 k	10 k	600 Ω

*R_{out} is located between Rx analog out and $\overline{RxO}$ output underneath the board.

NOTE: Drawings are not actual size.

FIGURE 3 — Component Layout

Strapping Information Chart

S1 These straps select via U1 (MC14417 TSAC) one of 32 possible time slots in the 8 kHz frame. When used in conjunction with another board, performance in different time slots can be evaluated. (that is TDE ≠ RCE).

S2A Selects 600 or 900 ohm input impedance.

S2B Selects A or Mu-law coding.

S3A Selects either TTL(TT) or CMOS(CM) logic levels. The TTL levels swing from V_{DD} and V_{AG}; CMOS levels swing from V_{DD} to V_{SS}.

S3B Powers device up or down. DN = Powered down and UP = Powered up.

S4 Normally loops RDD to TDD. When R-ICN is strapped, Mu-law receive idle channel noise can be measured (RDD = 1 111 1111).

S5 Controls digital ground of clock logic. When CMOS is strapped, digital ground = V_{SS}; when TTL is strapped, digital ground = V_{AG}. Note that this strap must agree with the selection on S3A.

S6 Selects either 3.78 or 3.15 volts peak overload voltage.

R2,R3 Adjusts RxO output level where gain = −R3/R2 (optional).

R4,R5 Adjusts Tx Analog In level where gain = −R4/R5.

R9 A 1 kilohm pullup resistor is needed when V_{AG} output is used by itself to provide ground return for RxO or $\overline{RxO}$. If V_{AG} is tied to system power ground, this resistor can be deleted.

R_{out} Determines output impedance.

APPENDIX

A DB By Any Other Name. . .

The following is a brief discussion of decibels and how they are used in the telephone industry in an attempt to lessen the notorious confusion this term can create.

Engineers are very familiar with the equation definition of a decibel which is:

$$\text{Decibels} = \text{dB} = 20 \log \frac{V2}{V1} \qquad (1)$$

or its corollary:

$$\text{dB} = 10 \log \frac{P2}{P1}. \qquad (2)$$

The use of the logarithmic function eases the use of the large range of voltage numbers encountered in the telephone industry. A decibel is only a relative term; it defines the difference between two absolute voltage levels.

Which now brings us to the absolute decibel—the dBm (decibel milliwatt). A dBm is equivalent to a milliwatt of power delivered into a reference impedance—usually 600 ohms. An equation commonly used to calculate dBm levels can be derived from equation (2):

$$\begin{aligned} \text{dBm} &= 10 \log (P2/P_{ref}) \\ &= 10 \log (P2/0.001\ \text{W}) \\ &= 10 \log 1000\ (P2) \\ &= 10 \log \frac{1000\ (\text{Vrms}^2)}{600\ \text{ohm}} \end{aligned}$$

where reference impedance = 600 ohms.

For example, to calculate the peak-to-peak voltage of a 0 dBm sinusoidal signal:

$$\begin{aligned} 0 &= 10 \log \frac{1000\ (\text{Vrms}^2)}{600} \\ 10^0 &= (5/3)\text{Vrms}^2 \\ \text{Vrms}^2 &= 0.6 \\ \text{Vrms} &= 0.7746 \\ \text{Vp-p} &= 2(2)^{1/2}\text{Vrms} \\ &= 2.191 \text{ volts peak-to-peak.} \end{aligned}$$

In order to understand the proper level at a certain point in a system, the term dBm0 is used for reference. A dBm0 defines the nominal signal level at a test point node. Absolute levels can then be referred to in dBm0 for comparison to the nominal level. For example, suppose that at a certain point in a system 0 dBm0 = +6 dBm/600 ohms. Then a −20 dBm signal would be equal to −20−(+6) = −26 dBm0. Therefore, a −20 dBm signal would be 26 dB down from the nominal level.

Noise measurements require a different decibel unit as they usually involve some bandwidth or filtering constraint. One such unit commonly used (especially in North America) is dBrn or decibels above reference noise. The reference noise level is defined as one picowatt into 600 ohms or −90 dBm. Telephone measurements typically refer to dBrnC which is the noise level measured through a C-message weighting filter (a filter that simulates the response of the human ear). European systems use a related term called dBmp which is the dBm level noise measured through a psophometric filter. Both dBrnC and dBmp can be referenced to 0 dBm0 by adding a zero—dBrnC0 and dBm0p. Two examples are shown below to illustrate the use of these units:

1) 0 dBm0 = +6 dBm/600 ohms
   Noise measurement = 20 dBrnC
   = 14 dBrnC0

2) 0 dBm0 = +9 dBm/600 ohms
   Noise measurement = −70 dBmp
   = −79 dBm0p.

Understanding these units should help avoid any possible correlation problems between measurements and published specifications.

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN893
Application Note

UNDERSTANDING TELEPHONE KEY SYSTEMS

Prepared By:
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INTRODUCTION

This application note is intended to give an understanding of key systems and how they differ. A theoretical architecture based loosely on many of the 16 station key systems now in existence will be presented. Possible variations and the impact on overall design will also be discussed.

WHAT IS A KEY SYSTEM?

A key system is a telephone system that can be used behind a PBX or central office. Generally, key systems are designed to support as many as 100 telephones, and provide service to these phones with up to 50 percent trunking (a trunk may be either a PBX or central office line connecting the key system to the rest of the world). The telephone set has several push buttons that are not generally found on a K500-type desk set. These push buttons allow direct access to several trunks, intercom lines and system features such as hold and do-not-disturb. The major difference between a key system and a PBX is that a key system allows the user full control over individual trunks, while a PBX assigns whatever trunk is available when requested (usually this is done by dialing a "9").

HOW DOES "SQUARENESS" AFFECT THE SIZE?

There are two basic architectural types of key systems, one known as a "square" system, and the other a "non-square" system. In a square system, every subset has control over every trunk so there can be no special reserved lines. Some designs go one step further by forcing a button appearance for each station. The most obvious size limiting factor in a square system is the number of buttons on the phone. In a non-square system, each phone is provided with a subset of the available trunks. While this makes the non-square system design appear more attractive, one must understand the complexity involved. In a square system, only one set of tip and ring wire pair must be routed to the phone, and since each phone looks identical, bookkeeping by the CPU is held to a minimum. In a non-square system there must either be a separate voice pair for each trunk and intercom link, as in 1A2 system, or there must be a way to program the telephone's "profile" into the CPU so it can control the station accesses. This presents real problems as there must be some input and display device associated with the CPU plus some form of non-volatile data storage. This storage can be anything as simple as several dip switches, or as complicated as an intelligent controller that hooks into the system with a CRT terminal and programs several EEPROMs.

WHAT IS A 1A2 SYSTEM?

The 1A2 key system is an older system that relied on electro-mechanical devices to accomplish the tasks now replaced by modern integrated circuit technology. These systems generally included several pairs of tip and ring signals which led to each station, where complicated mechanical switches selected the desired pair. The connections to the outside world were metallic, and therefore were of the non-protected variety. The biggest expense was cabling and installation labor, because the system required a 25-pair cable for each phone.

WHAT IS MEANT BY "PROTECTION"?

A protected key system is designed in such a way to prevent stressful voltages reaching the trunk under any circumstances. Generally, this is accomplished by transformer coupling the trunk to the system at the interface and adding overvoltage protection. This will prevent any accidents from causing problems with the trunk, such as 110 Vac getting to the trunk from an improperly installed telephone. When a key system is not protected, it must be installed by a registered agent of the manufacturing company. Both distributor and manufacturer are burdened by expensive agency agreements if a system is not protected.

KEY SYSTEM ARCHITECTURE

A 16-station square system with protection is outlined in Figure 1. The trunk interfaces provide the necessary protection to pass the FCC requirements, plus the circuitry to condition the voice and signaling information to make them

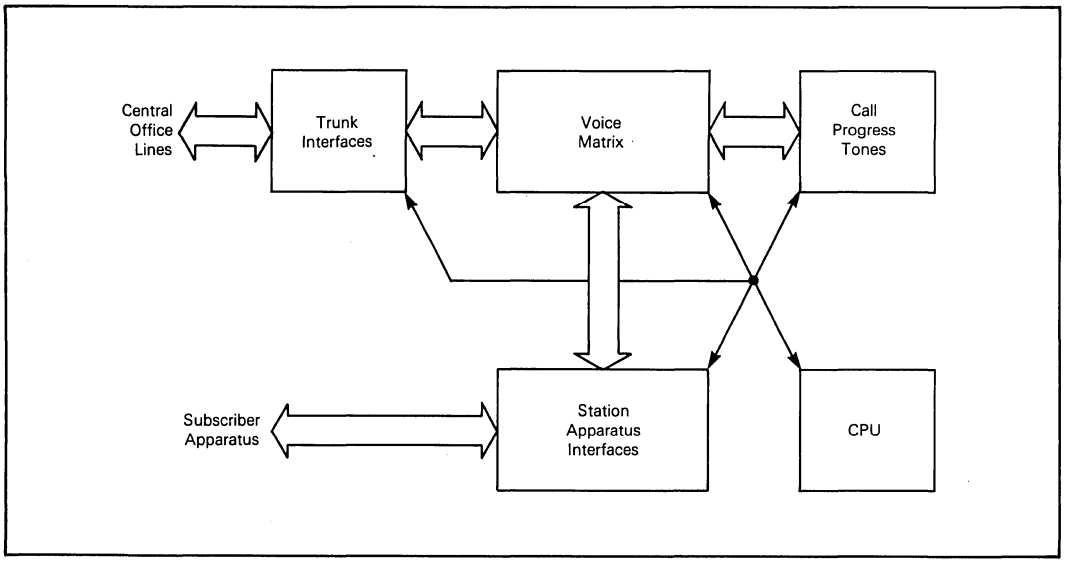


FIGURE 1 — Key System Unit

easier for the system to handle. The voice information is passed to a voice matrix, where the information can be routed to the proper destinations, and the signaling goes to the CPU to indicate what is happening at the interface. The station apparatus interfaces provide the voice and data interfaces to the phones. The progress tones are for internal supervisory signaling within the switch. The CPU is charged with the supervisory and monitoring tasks for all other parts of the system.

A much more detailed look at the voice matrix is provided in Figure 2. The voice matrix is an analog crosspoint variety which may be composed of relays or CMOS switches. Relays are a good voice switch medium for systems with eight or less stations, but the newer crosspoint ICs, such as the MC142100 and MC142101, are much more cost effective. There is some loss associated with the switches (about 100 ohms) that does not occur in the relays. In our example we will consider a 4 × 4 × 2 crosspoint and the dotted lines outlining the three chips needed for the matrix. The music-on-hold (MOH) music and the tones are separated to help alleviate crosstalk within the switch structure. The design includes the ability to handle 3 trunks and 1 internal conversion. This appears to be a standard that was implemented through the years. Most systems allow expansion to either 2 more trunks or a trunk and an intercom link by adding to the matrix. Bridging more than one trunk or station can be easily accomplished by setting multiple contact points.

The loss the switch introduces into the system is the major drawback to using the CMOS crosspoint switch. The FCC requires that the electrical-to-acoustical loss of the system from the trunk to the station must not exceed 2.5 dB. A look at Figure 3A shows that a typical trunk-to-station loop has loss in two areas. The two crosspoint switches represent a typical 200 ohm resistance when they are in an on state which creates about 2.5 dB of loss in a 600 ohm system. Each transformer also introduces some loss so the electrical-to-electrical loss exceeds 2.5 dB. Changing the internal resistance of the loop minimizes the switch resistance but the transformer efficiency is greatly decreased so no advantage is found here. The loop could be amplified, but this is costly and leads to unstable circuitry so the phone must be designed to operate on different levels from a standard phone. The FCC allows another 2.5 dB of loss for a station-to-station talk path as shown in Figure 3B so the extra switches in the loop are not a problem.

Figure 4A is a block diagram of the trunk circuit. When the trunk is idle, the tip and ring are bridged by the loop relay across the ring detect circuit. This circuit signals the CPU when a call is ringing in from the central office or PBX. When the trunk is accessed by the system the loop relay connects tip and ring to the transformer. The protect circuit helps prevent surge and static damage. The battery reversal detector is an optional circuit that alerts the CPU when the tip and ring polarity has been reversed. This usually happens momentarily when a central office toll circuit has been accessed, so this is for toll restriction. The loop detect circuit is needed to indicate when the connection has been terminated by the outside caller. This prevents the hold function from locking up a trunk. If pulse dialing is to be provided a relay circuit similar to the one in Figure 4B must be added to the loop. The CPU must read the pulses from the station and transfer them to the trunk. Another possible optional circuit is a ground loop detector. This is needed to detect grounds on a groundstart trunk. These trunks use a ground to start where loopstart trunks (the most common kind) use loop continuity to start.

The station interface in Figure 5 is a four-wire design. The first pair (tip and ring) are used to provide voice communications while the second pair (D+ and D−) provide data communications. The two resistors in the voice circuit provide a current limiting function to prevent catastrophic system failures should tip and ring get shorted together. The protect circuit functions in a manner similar to the trunk protect circuit and the loop detect is used to detect the making and

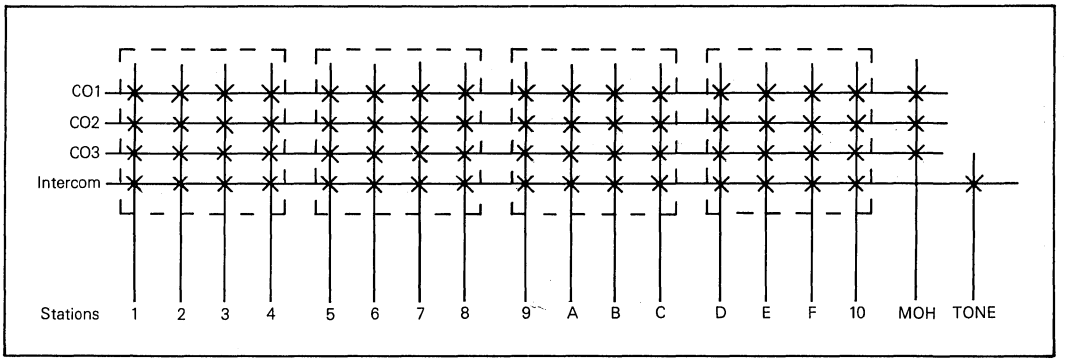


FIGURE 2 — Voice Matrix

breaking of the loop to pass pulse dialing signaling to the trunk. The resistors in the data interface do the same job in the voice circuit as does the protect circuit. The differential mode transmitter and receiver provide a serial data stream interface for the data communications. The data is generally in a half-duplex ping-pong arrangement, where the outgoing data tells the station which lamps should be on, whether the ringer is to ring, and whether the call announcer should be energized. The incoming data gives the status of the phone's hookswitch and the buttons on the keypad.

Another name for the station apparatus is the keyphone or the subset. Figure 6 is a block diagram of the subset. Tip and ring come into the subset through the hookswitch. When the handset is on-hook, the tip and ring are directed to the handsfree/call announcer circuit. This circuit is similar to a speakerphone circuit. When the handset is removed from its cradle, the tip and ring is routed to the speech network for normal telephone operation. Each voice network is powered by the battery voltage on tip and ring. The data circuit is powered by its own battery feed to help prevent crosstalk between voice and data. The data is brought into the control logic to activate the lamps, ringer, and in some cases, the handsfree/call announcer.

There are several variations on the voice and data links to the subset. Some systems impress the data, which generally has a rate well above the voice channel, onto the tip and ring for a single pair run. Extra filtering is needed to separate voice and data. Another variation connects tip and ring to the speech network causing the handsfree/call announcer to receive voice over the same wire pair as the data. This allows "off-hook call announcing" where the user can be paged via the call announcer while off-hook talking. Generally the output level of the call announcer is greatly attenuated when the handset is not in the cradle.

Another interesting variation to the architecture deals with how the dialing is controlled by the system. In this arrangement all DTMF tones or dial pulses originate at the subset and are passed through the system as though it is transparent. This is known as end-to-end signaling. An alternative is to place the pulse or tone dialer on the trunk interface and read the dial by the control logic so the dialing information is passed through the CPU to be interpreted at the trunk. The major drawback here is that there must be extra circuitry in the subset to produce aural feedback. In a normal phone the DTMF encoder mutes the speech network. Since the encoder is not here the mute is lost. The levels needed at the trunk may be uncomfortable, so they must not reach the user, therefore some feedback must be generated to indicate dialing has taken place.

Adaptation of this system into a non-square system requires several major system modifications. Since a non-square system allows only a portion of the trunks and available features to be represented as buttons on the subset, some scheme of accessing other non-appearing trunks and features must be employed. This is usually done by dial access. In a dial access system, every subset must have a dial intercom button. When this button is accessed the system must provide a dial tone and a dialing register. The dialing register must be capable of counting dial pulses and decoding DTMF data. Since DTMF decoders alone are in the $20-$30 price range the number of registers are generally restricted. This can cause bottlenecking problems when there is a need for more dial accesses than the number of registers available. There is generally a tone associated with this overload (the overload is called blocking) that indicates to the user that all circuits are busy. If all intercom links are busy when access is needed, then blocking also occurs. Now that the buttons must have some flexible assignments a data base of the subset "profiles" must be retained by the CPU. In addition to this data base duty, new software overheads are necessary for the CPU to allow dial and button accesses, as well as the addition of new, extended features such as dial intercom that are generally included in the non-square system.

There are several alternatives in operation during a power failure. One solution is called powerfail cutthrough. In this scheme certain trunks are metalically connected to certain phones. Our subset design does not support this arrangement since ringing would be impossible and the call announcer would be bridged across tip and ring when the subset is on-hook. The system can be designed so that ringing occurs in a normal manner, but a ringing generator is necessary. The ringing generator is a specialized ac power source. An alternative is battery back-up, and since most systems have a master power supply of 24-48 Vdc, this can be easily accomplished. The major advantage to this that no calls are lost on the power loss as in cut-through, and unless a sophisticated cut-through system is employed, calls are lost on the return to power which again is not a problem in a battery backed-up system. The system must be a low-power design or the battery back-up system may become prohibitively expensive.

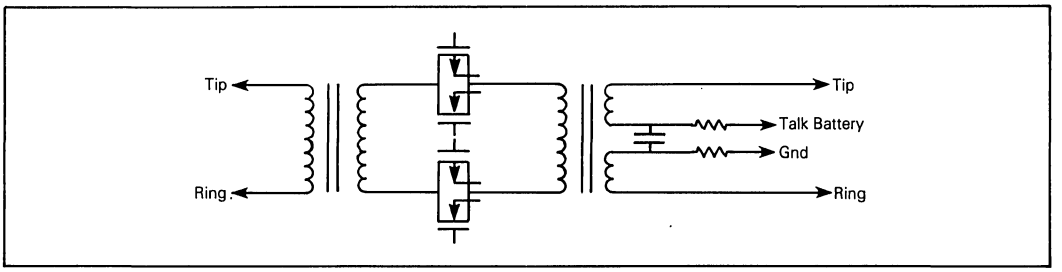


FIGURE 3A — Trunk-to-Station Loop

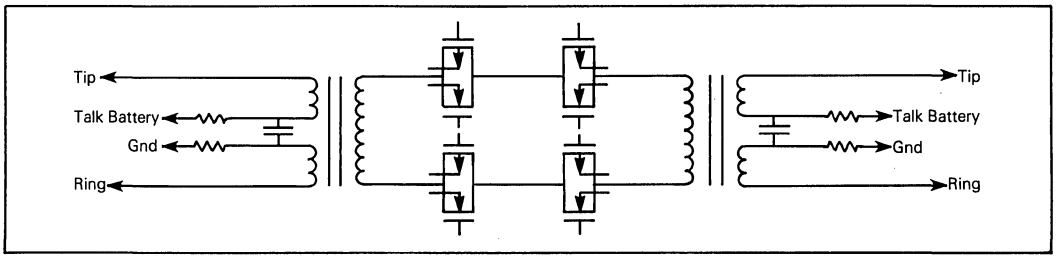


FIGURE 3B — Station-to-Station Loop

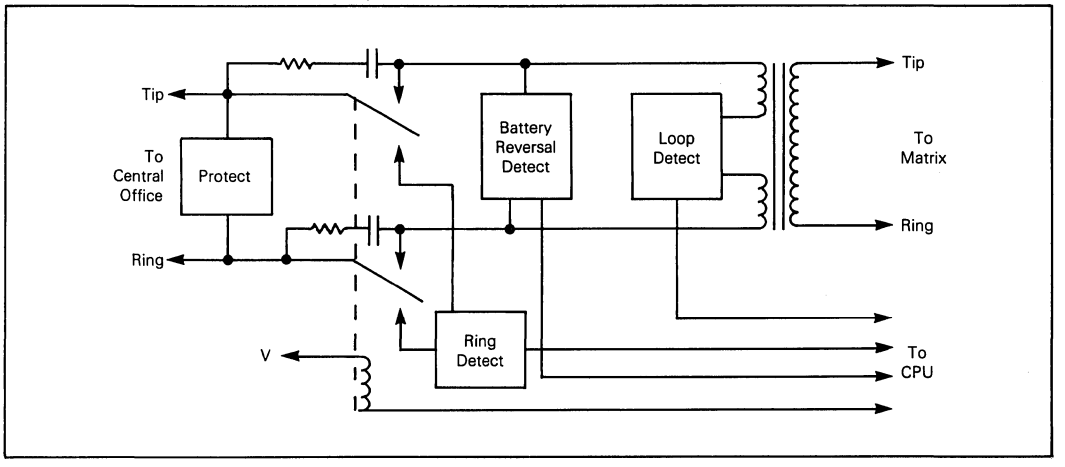


FIGURE 4A — Trunk Interface (Without Pulse Dialing)

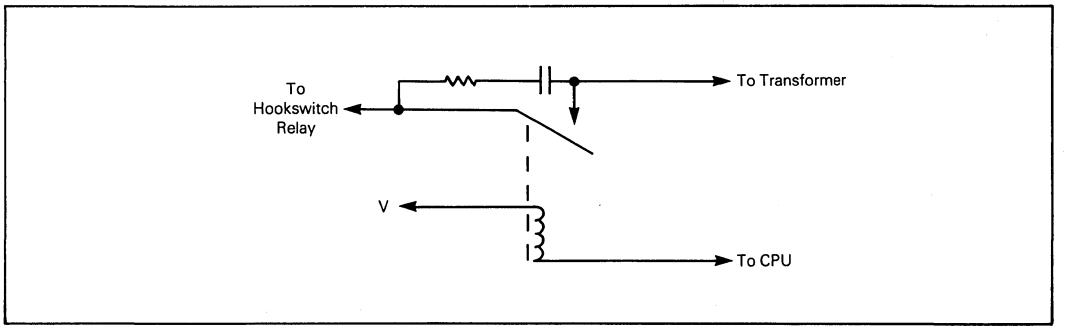


FIGURE 4B — Pulse Dialer

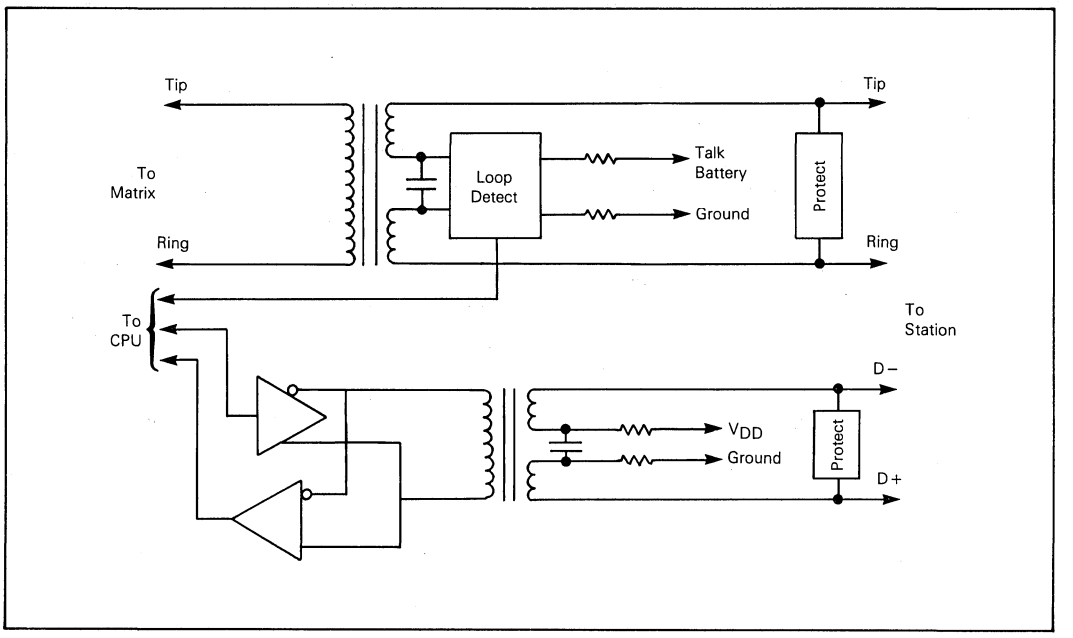


FIGURE 5 — Station Interface (Without Ring Generator)

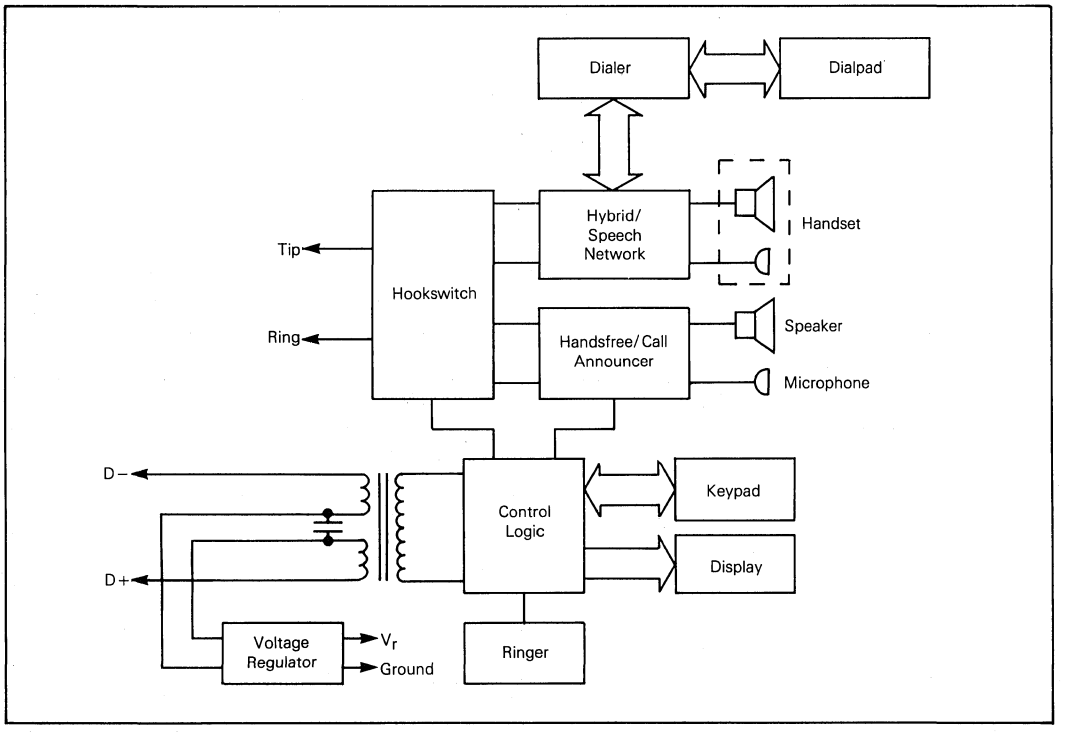


FIGURE 6 — Subset

GLOSSARY OF KEY SYSTEM FEATURES

All Call — This is where all of the call announcers are energized in the system for a general announcement. This is similar to a page except the call announcers are used instead of auxiliary amps and speakers.

Background Music — This is a feature that requires an external music source. The music is routed to all of the call announcers so that, if desired, the call announcer can provide music when the subset is idle.

Busy Lamp Field — This is an array of lamps or LEDs that indicate when each station in the system is busy or idle. This is usually abbreviated as BLF.

Call Announce — This function is performed instead of ringing. When an individual phone is call announced, the call announce circuitry is energized. A warning tone is then sent to both parties and then the parties are connected as in a conversation. The called party can talk over the call announcer as if it were a speakerphone.

Call Forward-Busy — An incoming call is routed to a secondary subset when first subset is busy.

Call Forward-Follow Me — An incoming call to one subset is routed directly to another subset.

Call Forward-No Answer — If a call is not answered in a specified period of time, the call is rerouted to a second subset.

Call Park — This feature is only used in non-square systems. When a call comes in it can be "parked," then any subset can pick the call up by accessing the parked call. This allows the subsets to pick up calls on non-appearing trunks.

Call Progress Monitor — This is a device that allows the monitoring of the calling function prior to completing the connection. All dial tones, dialing tones and ring back tones are heard over an auxiliary speaker as it would sound over a handset. This is a simplex device so no conversation can be held.

Camp On-Auto Call Back — When a called station is busy, the caller can camp on to that station so that when the subset becomes idle, it will ring. If the caller hangs up prior to the subset becoming idle, the caller's subset will ring and after he answers, the other subset will ring. The second case is known as auto call back and is an extension of the first case being camp on.

Conference — A conference is a call that has more than two parties involved in the call at one time.

Dial Intercom — A dial intercom is an intercom that when accessed allows the user to access other subsets, trunks and features with dial codes. This is only found in systems where there is not an access button for each subset.

Do Not Disturb — When this feature is activated at a subset, no incoming calls will ring the subset, however, the phone can still be used for outgoing calls. The subset will not acknowledge the call announcer either.

Direct Station Select — This allows one subset to establish an intercom call with a second subset by using a dedicated button as opposed to a dial code. This is a very popular feature in small square systems and is generally referred to as DSS.

Exclusion-Privacy — When active, this feature prevents other subsets from barging in on your call.

Executive Override-Barge In — Barge in is a feature that allows one to enter an already active conversation so that a conference is created. Executive override is the same feature applied to special phones to overcome an exclusive call (see Exclusion).

Handsfree — In an apparatus sense, this is known as speakerphone operation. In essence, a conversation is held over the subset's speaker and microphone while the handset is in the cradle. This frees the hands for other uses and several people can participate in the conversation at the handsfree end.

Music-On-Hold — This is a feature that requires an outside music source that may or may not be the same source used in background music. When someone is parked or put on hold they are provided with music instead of silence.

Page — This feature is similar to All Call except the general announcements are made over a user-supplied public address system instead of call announcers. This is especially useful in warehouse situations.

Recall — The recall feature is designed to prevent excessively long holds and call parks. When a call has exceeded the recall timeout while on hold or parked, it will ring the subset that either put it there or an attendant station.

Remote Answer — This feature exists only on non-square systems. When an incoming call rings a subset, it can be answered at another subset that does not have that particular line by invoking the remote answer feature.

Repertory Dial — This feature can be associated with either the subset or the system. This is where several commonly called phone numbers are internally stored and can be automatically dialed when accessed. This is also known as speed or abbreviated dialing.

Secretarial Intercom — This is a special case DSS where the called subset rings only while the access button is depressed. This allows private ring codes to be used between subsets to alert the users to special conditions.

Station Hunting — Station hunting is an advanced feature found usually on large, complex system. This feature allows groups of subsets to be "hunted". When a call is placed to this group, the first phone rings for a preset period of time, and if there is no answer, the second phone in the group rings. This will progress through all the subsets and the call can be answered at any subset at any time.

Tie Trunks — A tie trunk is used to link systems together. Generally the two systems are remotely located and can even be in different cities. The tie trunk does not rely on central office intervention.

Toll Restriction — This feature prevents unauthorized subsets from making toll calls.

Transfer — This feature is needed only in non-square systems and it allows a call to be moved to a subset that does not have a button appearance for that call.

TELEPHONE QUALITY CVSD CODECS USING NEW BIPOLAR LINEAR/I2L I.C.

Stephen H. Kelley
and
John J. Price

INTRODUCTION

Principles of continuously variable slope delta modulation for communications systems are discussed including an S plane model for a simple delta modulator with adjustable gain. A new bipolar I^2L circuit for implementing CVSD systems is presented. System performance and design techniques for a basic voice band codec and a telephone quality codec are included. Double integration and active companding ratio control techniques for improving codec performance is discussed. The emphasis is on a practical, mass producible telephone codec.

The continuously variable slope delta modulator (CVSD) is a simple alternative to more complex conversion schemes in systems requiring digital communication of analog signals. Voice and audio communications are analog, but digital transmission of any signal over great distance is more attractive. S/N ratios of the recovered signal do not vary with distance when using digital transmission; and multiplexing, switching, and repeating hardware is more economical and easier to design. However, instrumentation A to D converters do not easily meet the bandwidth constraints of communications requirements. The CVSD A to D is well suited to the requirements of digital communications and is an economical, efficient means of digitizing analog inputs for digital transmission.

THE DELTA MODULATOR

The innermost control loop of a CVSD converter is a simple delta modulator. That portion of the CVSD is shown in Figure 1. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the input analog signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and controls the direction of ramp in the integrator. The comparator is clocked so as to produce a synchronous and band limited digital bit stream.

If the clocked serial bit stream is transmitted to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the integrator at the transmitting location tracks the input signal, the remote receiver reconstructs the input signal. Low pass filtering at the receiver output will eliminate most of the quantizing noise if the clock rate of a the bit stream is an octave or more above the bandwidth of the input signal. Voice bandwidth is 4 kHz and clock rates of 8 kHz and up are possible. Thus, the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one zero alternation is transmitted. If the two integrators are made leaky, then during any loss of contact the receiver output decays to zero and receive restart begins

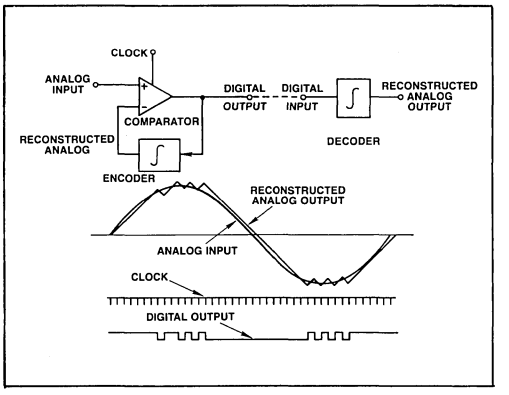


FIGURE 1 — SIMPLE DELTA MODULATION
An Analog Input Signal Can Be Digitalized and Transmitted by Synthesizing a Minimum Error Set of Voltage Ramps. The Comparator Clock Establishes the Channel Bandwidth.

without framing when the receiver reacquires. Similarly, a delta modulator is tolerant of sporatic bit errors.

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are its ability to accurately convert the input within a limited digital bit rate. The analog input must be frequency limited and amplitude limited. The frequency limitations are governed by the Nyquist rate while the amplitude capabilities are set by the gain of the integrator. For a given signal level, one specific gain will achieve an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

THE COMPANDING ALGORITHM

The continuously variable slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth, the additional circuitry increases the delta modulator's dynamic range. A block diagram of a complete CVSD codec is shown in Figure 2. A new bipolar/I^2L integrated circuit has been built to provide all of the active elements. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 3 or 4 bits long depending on the application. The CVSD algorithm simply monitors the contents of shift register and indicates if it contains all ones or zeros. This condition is called a coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output drives a low pass filter. The voltage output of this syllabic filter controls the integrator gain through a V to I converter and a slope polarity switch whose other input is the sign bit or the up/down control of the delta modulator.

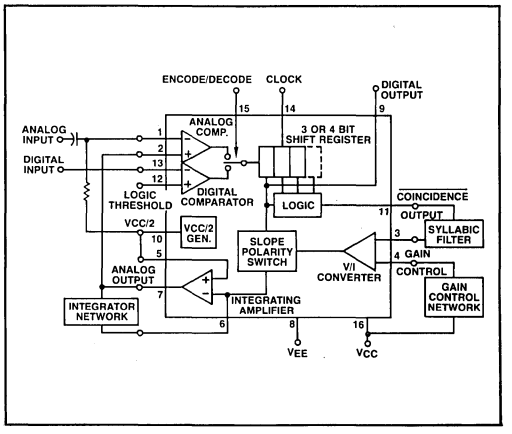


FIGURE 2 — CVSD BLOCK DIAGRAM
A Delta Modulator Is Enclosed in a Digitally Controlled Gain Loop and Composes a Continuously Variable Slope Delta Modulator. A Bipolar/I^2L Integrated Circuit Has Been Designed to Provide All the Active Circuitry Required.

The simplicity of the all ones, all zeros algorithm should not be taken lightly. Many other control algorithms using the shift register have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other schemes provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus, a measure of the average input level is needed. By monitoring both the coincidence of ones and zeros, the shift register performs a function similar to a full wave bridge rectifier.

The algorithm is repeated in the receiver and thus the level data is recoverable at the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate. The bit stream in the channel is as if it were from a standard delta modulator with a constant level input.

SYLLABIC AND INTEGRATION FILTER PROPERTIES

The circuit in Figure 3 is the most basic CVSD circuit possible. For many intelligible voice channel applications, it is adequate. In this circuit, both the syllabic filter and the integration filter are composed of single-pole networks.

The integration network is chosen to meet two simple constraints. First, it must be an integrator throughout the voice band and second, it must be leaky so that bit errors can be tolerated and loss of receiver contact does not require an external reset for reacquisition. C_I 5.1 μF and $R_I = 10$ k produce a 159 Hz break/frequency and a lossy network.

The selection of the syllabic filter components illustrates an interesting property of the codec. The operation of the simple delta modulator may be investigated by deriving its S plane transfer function. The comparator is modeled with a unit limiter and a summer. The unit limiter has a describing function in S if the system is analyzed for sinusoidal inputs of the form e sin wt, that is

$$\text{Digital Output} = \frac{4A}{\pi e} \text{ e sin wt where A is the peak voltage of the unit limiter.}$$

It is obviously a non-linear element since the transfer function is dependent on the magnitude of the input signal.

The integration filter has a straightforward transfer function description:

$$\frac{\text{Analog } V_{out}}{\text{Digital } V_{out}} = \frac{Rx}{C_I(S + 1/R_I C_I)}$$

where Rx is connected from the comparator output to the integrator input and sets the gain of the simple delta modulator.

The closed loop delta modulator model is then

$$\frac{\text{Analog Vout}}{\text{e sin wt}} = \frac{1}{1 + \dfrac{4ARx}{e\, C_I\, (S + 1/R_I C_I)}}$$

Note that the response of the codec is a function of the magnitude of the input level. Closed loop CVSD systems can be analyzed for steady state inputs by substituting the syllabic filter voltage which corresponds to an applied e for A. Thus, the gain of the delta modulator is varied to accommodate the applied input level.

For a CVSD circuit to perform as an adjusted delta modulator, the model equation indicates that A ∝ e must be nearly constant. The syllabic filter time constant must be large compared to the input frequency. For a maximum input frequency of 3300 Hz, the time constant must be much larger than the 0.3 ms. Thus 3 ms is the minimum allowed RC product for the syllabic filter in voice band applications. The syllabic nature of voice is responsible for the name "syllabic filter". A CVSD codec can only effectively transmit signals whose e varies at a frequency much lower than the fundamental frequency of the signal. Conveniently, voice, modem signals and DTMF signals have this syllabic property.

In Figure 3, a 6 ms time constant is used. In Figure 5, 3 ms charge and 9 ms discharge time constants are used to improve attack time without sacrificing constant A. Voice syllables tend to have this kind of shewed envelope.

CLOCK RATE AND SHIFT REGISTER LENGTH

The prime design constraint of a CVSD channel is the channel bit rate. Since delta modulator produces a serial unframed bit stream, the bit rate and sample frequency are the same. Obviously, as the clock rate increases so will the end to end performance. Clocks from 9600 kHz to 64 kHz can be used in various applications. 16 kHz, 32 kHz, and 37.7 kHz have the greatest acceptance in practical voice communication equipment.

After fixing the system bit rate, the shift register length selection must be made. The length of the shift register determines the amount of past history which will be taken into account in predicting slope. As the clock rate changes, so does the amount of signal time recorded by the shift register. Therefore, at rates below 16 kHz a three bit algorithm produces the best results. From 16 kilobits and up, either 3 or 4 bits may be used. Four bit algorithms provide flatter S/N performance because they account for a longer average past history of steady state signals. However, the transient response to level changes is slightly degraded because of the slower companding response.

The integrated circuit is produced with either 3 or 4 bit registers and is selected by laser link cutting rather than mask option. Depending on the results of the idle channel trim corrections, the die requiring the smallest step sizes is made into a 4 bit register.

LOOP GAIN CONSIDERATIONS

The feedback gain of the CVSD codec is set by the selection of Rx in Figure 3. After the clock rate, this gain is the most critical parameter of codec performance. Since the CVSD algorithm improves the dynamic range of the delta modulator for lower level inputs, the selection of loop gain should be based on the near maximum amplitude and frequency signal which must be transmitted. Experimental data shows that a CVSD codec produces optimum S/N ratio when the companding algorithm is active between 5% and 25% of the time. Taking this into account, the gain resistor Rx can be selected by determining the required integrator current which will produce the needed step size for a specified input signal. Then the resistor should source the required current when the syllabic filter output is about 25% of its maximum value.

The current required to move the integrator output a specific voltage from zero is simply

$$I_I = \frac{Vo}{R_I} + C_I \frac{dVo}{dt}$$

Now a 0 dBmo sine wave has a peak value of 1.0954 volts. In 1/8 of a cycle of the sine wave centered around the zero crossing the sine wave changes by approximately its peak value. The CVSD step should track that change. The required current for a 0 dBm 1 kHz sine wave is

$$I_I = \frac{1.1 \text{ volt}}{*2(10k)} + \frac{0.1\ \mu F\ 1.1}{0.125 \text{ ms}} = 0.935 \text{ mA}$$

*The maximum voltage across R_I when maximum slew is required is $\frac{1.1\ V}{2}$

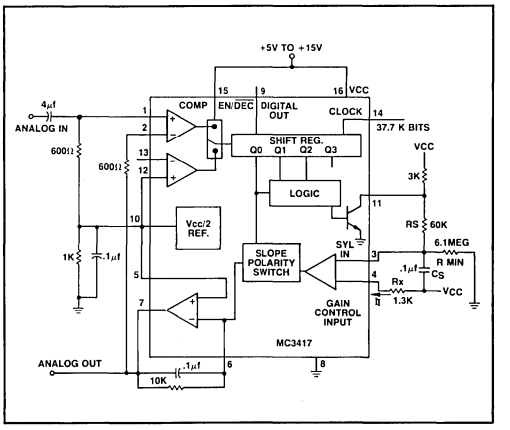


FIGURE 3 — BASIC CVSD ENCODER
Single Pole Integration and a Single Pole Syllabic Filter Are Sufficient for Many Voice Channel Applications. Selection of External Components Tailors the Integrated Circuit to the Application.

Now the voltage range of the syllabic filter is the power supply voltage, thus

$$Rx = 0.25(V_{CC})\ \frac{1}{0.935 \text{ mA}}$$

for a 5 volt supply Rx = 1.3 k

MINIMUM STEP SIZE

The final parameter to be determined for the simple encoder in Figure 3 is the minimum step size. With no input, the CVSD digital output becomes a one zero alternating pattern and the analog output becomes a small triangle wave. The peak to peak value of that triangle wave is the idle channel step size. Its meaning is analogous to the 1½ LSB quantization error of a conventional D to A converter. The codec

cannot resolve or transmit signal levels smaller than the minimum step size. In theory, one would wish to make this parameter go to zero. However, practical errors such as up and down ramp matching, comparator hysteresis, and filter op amp offsets combine to cause the idle channel analog output to drift away from the zero dc reference. The codec then produces two ones or two zeros in order to restore the level.

To set the idle channel step size, the value of R min must be selected. With no input signal, the slope control algorithm is inactive. A long series of ones or zeros never occurs. Thus, the voltage across the syllabic filter, the voltage divider of R_S and Rmin (see Figure 3) sets the minimum allowed voltage across the syllabic filter capacitor. That voltage divided by Rx must produce the desired ramps at the analog output. Again we write the integrator current equation

$$I_I = \frac{Vo}{R_I} + C_I \frac{dVo}{dt}. \text{ For small Vo } \frac{Vo}{R_I} \rightarrow 0.$$

$I_I = C_I \frac{\Delta Vo}{\Delta T}$ where ΔT is the clock period and ΔVo is the desired peak to peak value of the idle output.

Thus if Rx and R_S are known, R min may be calculated for any system. The design of Figure 3 is complete.

Figure 4 describes the performance of the codec in Figure 3 with two sets of curves. The codec was optimized around 0 dBm but the S/Nc ratio falls only 6 dB at −30 dBm. The low pass nature of the codec and the change of frequency response with input level is documented on the left of the figure.

S/N IMPROVEMENT USING TWO POLE INTEGRATION

One pole integration filters are not the only possibility. If a two pole integration network is used instead of the simple one pole, an S/N improvement can be realized. An encoder using such a network is shown in Figure 5. Adding a second pole in the transfer function of the integrator simply reduces the total noise bandwidth of the analog output without affecting the relevant voice energies. From another point of view, a 11110111 input to a single pole integrator produces a large ramp reversal at the 0 value since the 0 step will be in the opposite direction but equal in magnitude to the 1 ramp before and after it. Since the analog signal is band limited, it was obviously continuing to decrease at the 0 step and an error in tracking is encountered. If two pole integration is used, the 101 reversal is filtered and the 0 step is much smaller than the 1 step preceding it in the long string of ones. Thus the total error is less. A two pole filter can improve noise performance by 3 or more dB across the entire input level range.

The first pole is still placed below 300 Hz to provide the 1/S voice content curve and a second pole is placed somewhere above the 1 kHz frequency. For telephone circuits, the second pole can be placed at 1.8 kHz to exceed the 1633 DTMF frequency. The lower the second pole frequency, the greater the noise improvement. To ensure the encoder loop stability, a zero is added to keep the phase shift less than 180°. This zero should be placed slightly above the low pass output filter break frequency so as not to reduce the effectiveness of the second pole. A network of 244 Hz, 1.8 kHz and 5.3 kHz is used for telephone application in Figure 5 while 160 Hz, 1.2 kHz and 2.8 kHz might be used in voice only channels. The integration filter in Figure 5 has a transfer function of

$$\frac{V_{out}}{I_{in}} = \frac{R_0R_1\left(S+\frac{1}{R_1C_1}\right)}{R_2C_2(R_0+R_1)\left(S+\frac{1}{(R_0+R_1)C_1}\right)\left(S+\frac{1}{R_2C_2}\right)}$$

The selection of the two pole filter network affects the selection of the loop gain value and the minimum step size

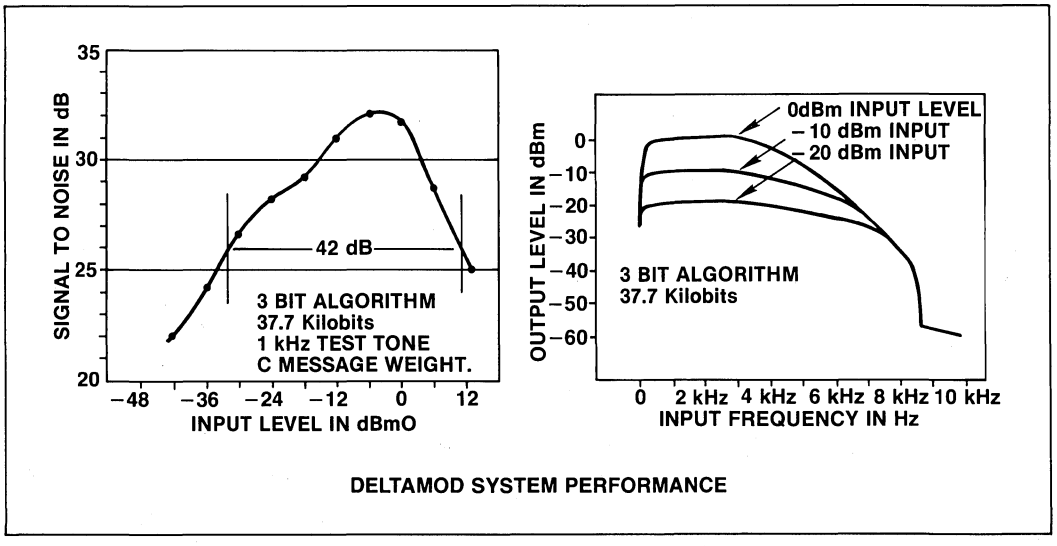


FIGURE 4 — SIGNAL TO NOISE PERFORMANCE AND FREQUENCY RESPONSE
Data Result From Testing the Circuit in Figure 3.

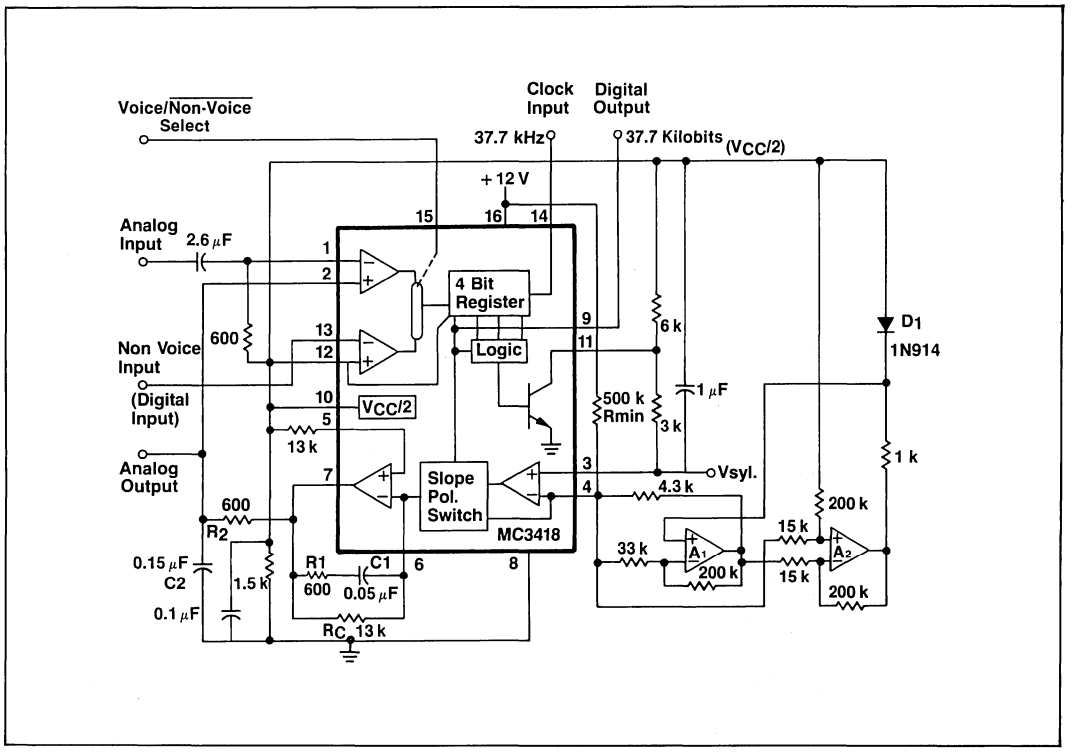


FIGURE 5 — TELEPHONE QUALITY DELTA MODULATOR CODER
Both Double Integration and Active Companding Control Are Used to Obtain Improved CVSD Performance. Laser Trimming of the Integrated Circuit Provides Reliable Idle Channel and Step Size Range Characteristics.

resistor. The required integrator current for a given change in voltage now becomes

$$I_{in} = \frac{V_{out}}{R_0} + \frac{R_2C_2}{R_0} + \frac{R_1C_1}{R_0} + C_1\frac{\Delta V_{out}}{\Delta T} +$$

$$R_2C_2C_1 + \frac{R_1C_1R_2C_2}{R_0}\frac{\Delta V_{out2}}{\Delta T2}$$

The calculation of desired gain resistor Rx then proceeds exactly as previously described using this current equation.

SUBSCRIBER CARRIER TELEPHONE QUALITY CODEC USING MC3418

Two specifications of the integrated circuit are specifically intended to meet the performance requirements of commercial telephone systems. First, slope polarity switch current matching is laser trimmed to guarantee proper idle channel performance with 5 mV minimum step size and a typical 1% current match from 10 μA $to \approx \mu\Delta$. Thus a 300 to 1 range of step size variation is possible. Second, the MC3418 provides the four bit algorithm currently used in subscriber loop telephone systems.

With these specifications and the circuit of Figure 5, a telephone quality codec can be mass produced.

The circuit in Figure 5 provides a 30 dB S/Nc ratio over 50 dB of dynamic range for a 1 kHz test tone at a 37.7 kilobit rate. At 37.7 kilobits, 40 voice channels may be multiplexed on a standard 1.544 megabit TI facility. This codec has also been tested for 10^{-7} error rates with asynchronous and synchronous data up to 2400 baud and for reliable performance with DTMF signaling. Thus, the design is applicable in telephone quality subscriber loop carrier systems, subscriber loop concentrators and small PABX installations.

THE ACTIVE COMPANDING NETWORK

The unique feature of the codec in Figure 5 is the step size control circuit which uses a companding ratio reference, the present step size, and the present syllabic filter output to establish the optimum companding ratios and step sizes for any given input level. The companding ratio of a CVSD codec is defined as the duty cycle of the coincidence output. It is the parameter measured by the syllabic filter and is the voltage across C_S divided by the voltage swing of the coincidence output. In Figure 5, the voltage swing of pin 11 is 6 volts. The operating companding ratio is analoged by the voltage between pin 10 and 4 by means of the virtual short across pin 3 and 4 of the V to I op amp within the integrated circuit. Thus, the instantaneous companding ratio of the codec is always available at the negative input of A1.

The diode D1 and the gain of A1 and A2 provide a companding ratio reference for any input level. If the output of A2 is more than 0.7 volts below $V_{CC}/2$, then the positive input of A1 is $(V_{CC}/2 - 0.7)$.

The on diode drop at the input of A1 represents a 12% companding ratio (12% = 0.7 V/6 V).

The present step size of the operating codec is directly related to the voltage across Rx which established the integrator current. In Figure 5, the voltage across Rx in a direction which reduces the difference between the companding reference and the operating ratio by changing the step size. The ratio of R4 and R3 determines how closely the voltage at pin 4 will be forced to 12%. The selection of R3 and R4 is initially experimental. However, the resulting companding control is dependent on Rx, R3, R4, and the full diode drop D1. These values are easy to reproduce from codec to codec.

For small input levels, the companding ratio reference becomes the output of A2 rather than the diode drop. The operating companding ratio on pin 4 is then compared to a companding ratio smaller than 12% which is determined by the voltage drop across Rx and the gain of A2 and A1. The gain of A2 is also experimentally determined but once determined, the circuitry is easily repeated.

With no input signal, the companding ratio at pin 4 goes to zero and the voltage across Rx goes to zero. The voltage at the output of A2 becomes zero since there is no drop across Rx. With no signal input, the actively controlled step size vanished.

The minimum step size is established by the 500 k resistor between V_{CC} and $V_{CC}/2$ and is, therefore, independently selectable.

The signal to noise results of the active companding network are shown in Figure 6. A smooth 2 dB drop is realized from +12 dBm to −24 under the control of A1. At −24 dbm, A2 begins to degenerate the companding reference and the resulting step size is reduced so as to extend the dynamic range of the codec by 20 dBm. The slope overload characteristic is also shown. The active companding network produces improved performance with frequency. The 0 dBm slope overload point is raised to 4.8 kHz because of the gain available in controlling the voltage across Rx. The curves demonstrate that the level linearity has been maintained or improved.

The codec in Figure 5 is designed specifically for 37.7 kilobit systems. However, the benefits of the active companding network are not limited to high bit rate systems. By modifying the crossover region (changing the gain of A2), the active technique may be used to improve the performance of lower bit rate systems.

The performance and repeatability of the codec in Figure 5 represents a significant step forward in the art and cost of CVSD codec designs.

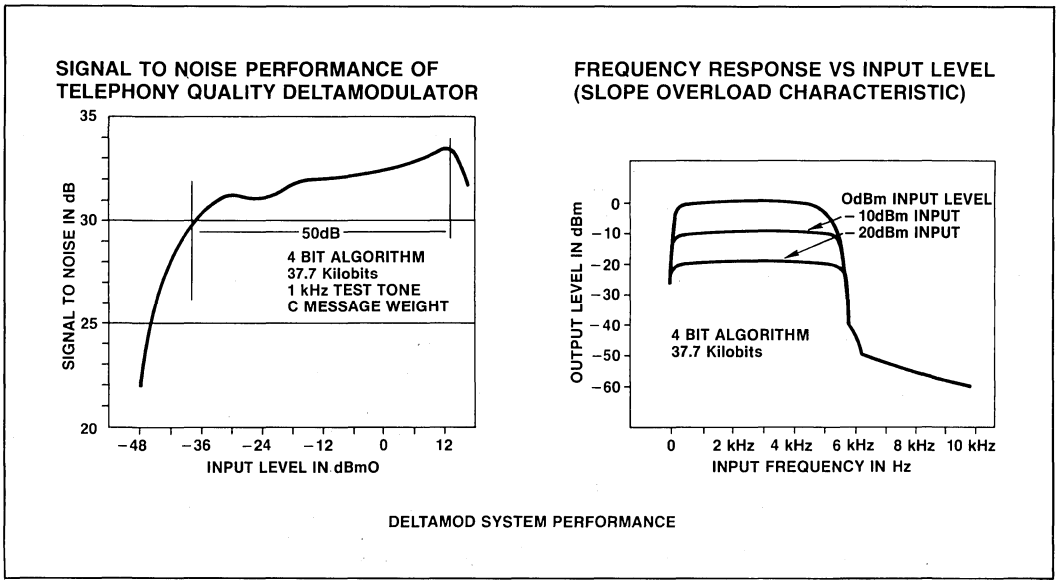


FIGURE 6 — SIGNAL TO NOISE PERFORMANCE AND FREQUENCY RESPONSE
Data Document the Improvement Realized with the Circuit in Figure 5.

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

UDLT Evaluation Board

INTRODUCTION

To help meet the demands for a cost effective solution to the ever growing voice/data world within the digital telephone and PBX realm, Motorola has created the Universal Digital Loop Transceiver (UDLT) voice/data circuit family. The purpose of this application note is to render an understanding of the UDLT voice/data family and show a typical application for these CMOS parts. This is an evaluation of the application and performance of the MC145422/26 UDLT demonstration board, which was designed and built for customer evaluation.

FUNCTION OF PARTS

UDLT's

The UDLT master (MC145422) and slave (MC145426) are transceivers that provide 80 kilobit-per-second full duplex synchronous voice and data communication to distances of two kilometers on 26 AWG twisted pair and further on heavier gauge pairs. The modulation technique used is a 256 kilobaud Modified Differential Phase Shift Keying (MDPSK) type burst. The MDPSK triangular waveform used in this modulation technique reduces radiation, EMI, and crosstalk due to its compact frequency spectrum.

The master which is used at the telephone switch linecard bursts ten bits to the slave, consisting of eight bits of voice/data and two signaling bits. The slave, which is used at the terminal or digital telephone, receives the burst from the master and upon demodulation of the burst synchronizes its clocks, and bursts ten bits back to the master. This "ping-pong" technique occurs within a 125 microsecond frame period and allows end to end full duplex, synchronous operation. This full duplex operation between the master, at the digital linecard and the slave/mono-circuit, at the digital telephone, enables each set to have high speed access to the PABX switching facility.

At the linecard a microprocessor has complete control of the master. The Signal Enable input (SE) is a three state controller pin which if held high enables the power down, loopback and the two signaling bits, thus allowing these signals to be bussed to the microprocessor. The master can be programmed via the Signal Insert Enable (SIE) pin to insert signaling bit two into the LSB of the PCM word at Tx. This allows simultaneous voice and data transmission through the PABX without the need of changing existing hardware and software. Both the master and the slave have power down and loopback features for system power conservation and testing. The power down pin on the slave is a bidirectional pin. It can be used as an input to initiate a call. When the PD pin is pulled high, the slave will continue to burst every other frame (once every 250 microseconds) until the master responds by bursting. Once the master responds, the slave synchronizes to ping-pong with the master at an eight kilohertz rate. The PD pin can be left floating as an output, in which case the slave will pull PD high until the slave stops receiving bursts from the master then it will take PD low and stop bursting until PD is brought high or the master bursts again. A three state control can be used on this pin if the designer wants to send data to the master during a power down. The slave also has a Tone Enable input pin (TE) which when held high generates a 500 hertz square wave tone at approximately −20 dBm0 which can be used in the digital telset to provide audio feedback.

MONO-CIRCUITS

Motorola's family of Pulse Code Modulation (PCM) mono-circuits incorporate a codec, filter and voltage reference into a single IC. The general block diagram for Motorola's mono-circuits is shown in Figure 1. These devices perform the digitizing and recovery, as well as the band-limiting and reconstruction filtering necessary for voice digitization in telephone systems. The mono-circuits are tailored for a variety of telephone switch architectures. The family consists of five different device types. The MC14400, MC14403, and MC14405 16 pin devices, the MC14401 18 pin device and the MC14402 22 pin device allow designers to optimize for minimal configurations or select a full set of features. The MC14403, for example, can be used where minimal space is desired for the digital phone design whereas the MC14402 is available for maximum flexibility. The mono-circuit incorporates the band-pass filter required for antialiasing and 60 hertz rejection, the A/D, the D/A, both for either U.S. Mu-Law or European A-Law companding formats, the lowpass filter required for reconstruction smoothing, on-board precision voltage reference and does not require any external components.

In this demonstration board, the full featured 22 pin MC14402 mono-circuit is used in the slave circuit showing its ability to adjust the receive gain while maintaining a low impedance output using the RxO, RxG, and $\overline{\text{RxO}}$ pins, The MC14403 is used on the master board showing a simple 16 pin solution for the telephone handset interface.

DATA SET INTERFACE (DSI)

The MC145428 Data Set Interface (DSI) provides the asynchronous to synchronous and synchronous to asynchronous data conversion. This low power five volt CMOS device is ideally suited to interface between the RS-232 compatible data port of any voice/data digital telset or terminal and the synchronous data channel of the UDLT. A block diagram of the Data Set Interface is shown in Figure 2.

There are two basic modes of operation for the synchronous channel interface. In the first mode the DSI inter-

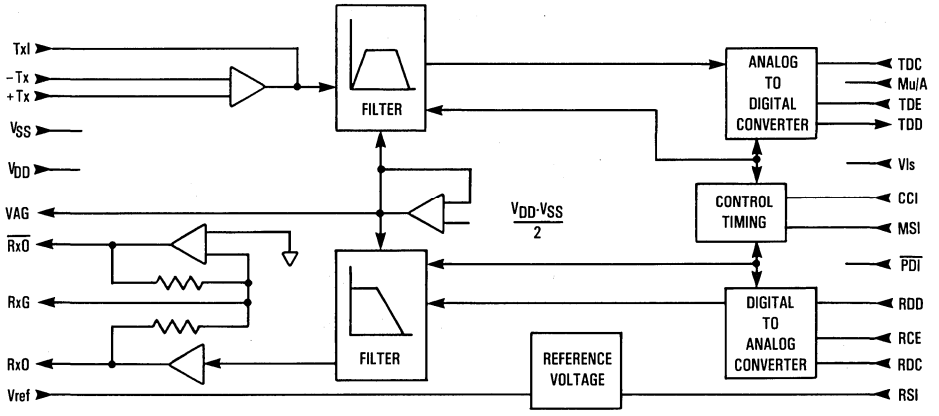


Figure 1. Block Diagram of the Mono-circuits

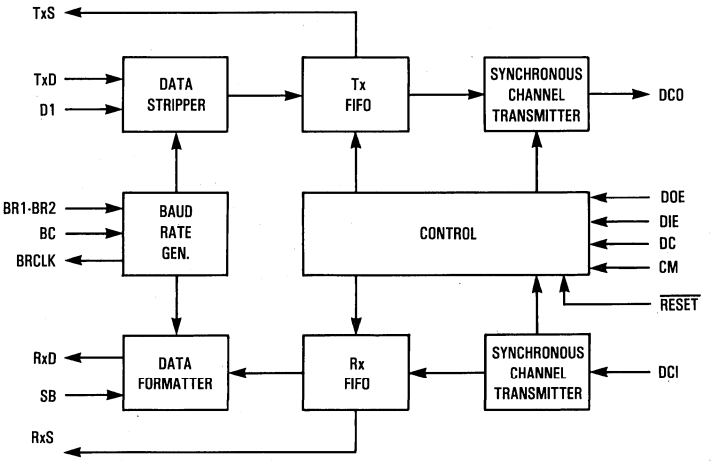


Figure 2. Block Diagram of the Data Set Interface

faces to the eight kilobits-per-second data channel of the UDLT. The Clock Mode input (CM) is tied low while the Data Output Enable (DOE) and Data Input Enable (DIE) are tied high. In this mode a new data bit is clocked out of Data Channel Output (DCO), a new data bit is clocked in at Data Channel Input (DCI), on each falling edge of the Data Clock (DC).

In the second mode of operation, the clock mode is held high. In this mode the DSI is intended to interface with the UDLT's 64 kilobits-per-second data channel. Data is clocked out under control of DOE and the rising edge of DC. Data may be clocked out at a maximum length of eight bits per enable high period. Data is clocked into DCI under control of DIE high and the falling edge of DC. The maximum word size is also eight bits per DIE high period.

Asynchronous data is input on the TxD pin from the output of the RS-232 receiver. This data must have at least one start and one stop bit and at least eight data bits, but will accept nine. The length of the data word is set by the DL pin. A high on DL selects a nine bit data word and a low selects an eight bit data word. The baud rate at which the DSI accepts data on the TxD pin, and outputs data on the RxD pin, is selected with the BR1, BR2, and BR3 pins which derive the internal sampling clock. The internal baud rate generator may be programmed to accept common asynchronous data rates from 300 to 38.4 kilobits-per-second. This internal sampling clock is 16 times the selected baud rate. If BR1-BR3 are all set to logic zero then an externally supplied 16 times clock can be used on the Baud Clock pin (BC) thus giving the user a variable data

rate from zero to 128 kilobits-per-second. For the internal baud rate generator to be accurate, a 4.096 megahertz clock must be used at the BC pin. If the internal baud rate generator dividers are used with a BC clock other than 4.096 megahertz, the data rate may be directly scaled.

Data input on the TxD pin is stripped of its start and stop bits and is loaded into the transmit FIFO register. If the transmit FIFO holds more than two data words or if RESET is held low, then the (TxS) Transmit Status output pin will go low.

Data coming in from the synchronous side is loaded into the receive FIFO, the data has its start and stop bits inserted and is output at RxD at the same baud rate as the transmit side. If the receive FIFO is overwritten, RESET is held low, or if loss of synchronization occurs by the loss of the synchronizing flag word, then the (RxS) Receive Status output pin will transition low.

RS-232 DRIVERS/RECEIVERS

The RS-232 Driver/Receiver chips interface the data terminal equipment with data communications equipment. Motorola manufactures both the MC1488 Quad Line Driver as well as the MC1489 Quad Line Receiver. Both 14 pin packages were used in this evaluation board. Motorola also manufactures the MC145406 Driver/Receiver chip which is a silicon-gate CMOS integrated circuit that combines three drivers and three receivers compatible with the electrical specifications of EIA standard RS-232-C, and CCITT V.28. This part has the capability of running with power supplies ranging from ±5 volts to ±12 volts while operating with a maximum quiescent current supply of 1.45 milliamperes. By combining both the drivers and receivers in a single CMOS chip, the MC145406 provides an efficient, low-power solution for RS-232-C/V.28 applications. A footprint for the MC145406 is included on the evaluation board design.

TRANSFORMER INTERFACE

The transformer interface between the UDLT and the twisted pair wire is of primary importance. The major transformer specifications can be determined from the specifications of the UDLT, driver/receiver, modulation technique, effective characteristic impedance of the wire, attenuation of the wire and dc current feed capacity. The UDLT has a differential output (LO1, LO2) that can drive 440 ohms differentially to five volts peak to peak. The receiver has an input threshold of ±25 millivolts. The UDLT modulation method has maximum power bandwidth from eight kilohertz to 512 kilohertz. To improve line settling between bursts, a bandwidth of 20 kilohertz to 512 kilohertz is used. The effective characteristic impedance of 26 AWG telephone twisted pair wire is approximately 110 ohms with an attenuation of 18 decibels-per-kilometer at a frequency of 256 kilohertz. The transformer configuration is shown in Figure 3.

The source impedance resistors for the LO1 and LO2 driver outputs were chosen to be 220 ohms on the transmit tap. This dictates a turns ratio of 2:1 to the line side of the transformer to result in an impedance match to the 110 ohms characteristic impedance of the twisted pair.

To set the 20 kilohertz low-frequency cut off of the transformer interface, the inductance of the transmit winding of the transformer should be 1.75 millihenries. To set the 512

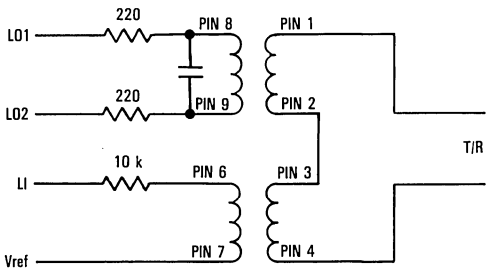


Figure 3. Transformer Configuration

kilohertz high-frequency cut off, a 0.001 microfarads capacitor is connected in parallel with the transmit tap. The turns ratio for the receive winding is determined by the maximum attenuation of the line and the threshold of the receiver detecter. With an initial amplitude of 2.5 volts peak (five volts peak to peak) at LO1 and LO2 halved by the source resistors to 1.25 volts peak at the transmit tap, which is halved again via the turns ratio to the line windings, yields 0.625 volts peak at the line side of the transformer. This 0.625 volts peak is reduced by 36 decibels or a factor of 63 to ten millivolts at the receiving transformer. The receiver of the UDLT has a positive and negative 25 millivolt threshold, which means the receive transformer tap needs a gain of approximately four to meet the needs of the receiver circuitry of the LI pin. This results in the transformer of the schematics, which may be obtained from:

Leonard Electric Products Company
85 Industrial Drive
Brownsville, Texas 78521
P/N P-1358-A

The signals from LO1 and LO2 on the transmit tap are 1.25 volts peak which through the turns ratio to the receive tap becomes 2.5 volts peak at LI. This can exceed the maximum and minimum voltage specification for LI requiring input protection such as the clamping diodes on LI, shown in Figure 4.

When using battery feed through the transformer, further protection is required due to loop current induced spikes at both transmit and receive taps of the transformer. There are several factors to take into consideration when determining the specifications for battery feed current by the center tap of the line side of the transformer. The maximum power is transferred when half of the source voltage is dropped across the effect source resistance. Based on a loop length of two kilometers with a dc resistance of 270 ohms per loop kilometer, a current of 44 milliampheres is the maximum power transfer current. The loop current chosen for the specification is 100 milliampheres. The circuit of Figure 4 is an example of this type of protection.

EVALUATION BOARD DESCRIPTION

The Motorola UDLT evaluation board is a single sided PC board that consists of all the necessary circuitry for end to end operation and demonstration of the 80 kilobits-per-second full duplex synchronous data link of the UDLT master and slave. The evaluation board itself consists of two smaller boards; a master board and a slave board. These two boards may be

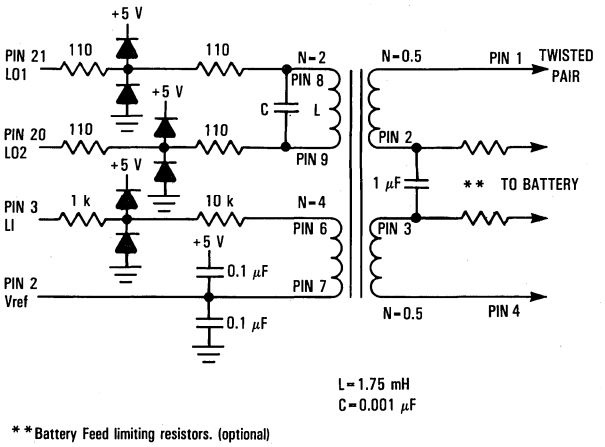


Figure 4. Application Circuit For the Transformer Interface

separated by cutting the panel in half along the two markers, shown in Figure 7. The master board schematic is shown in Figure 5 and the slave board schematic is shown in Figure 6, while the artwork is shown in Figure 7.

The master board contains the master UDLT (MC145422), DSI (MC145428), Mono-circuit (MC14403), the MC1488/1489 or MC145406 RS-232 drivers and receivers, and the necessary clock circuitry to drive these parts. The master board emulates both another digital telset plus the telephone switch interface to the slave board. The master typically is used in the digital switch at the PBX, networked with other digital and analog interface circuits.

The slave board contains the slave UDLT (MC145426), DSI (MC145428), Mono-circuit (MC14402), MC1488/1489, or MC145406 RS-232 Driver/Receiver chips. The slave side emulates a digital telephone where the analog information is digitized at the phone and the information from the phone is digital.

Both master and slave boards have their second eight kilobit signaling channel connected to a DSI for up to 9600 baud of user data simultaneously independent of voice. The baud rates are selected with switches BR1-BR3 (see strapping information). Each board has a DB-25 connector for easy connection to any terminal. Only TxD, RxD, and Ground are connected on the DB-25. Data to and from the DB-25 is fed through the MC1488, MC1489 and the MC145406 Driver/Receiver chips. The socket for the MC145406 RS-232 Driver/Receiver chip is included on each board for evaluation. This part can replace both the driver and receiver chips. Once replaced, the user at his option can cut the MC1488 and MC1489 pads out of the PC board along the dashed lines. This enables each board to fit in a K-2500 phone.

Each board has an RJ-11 socket for easy connection to any modular handset. The signal from each handset is fed through the respective mono-circuit into the 64 kilobit voice channel on the UDLTs. Both master and slave boards have space for a push button switch which can be hardwired onto the SI1, along with an LED on SO1 for signaling on channel one. This channel is optional to the user and can be used with a microprocessor in the phone or a pulse dialer. Signaling bits one and two provide eight kilobits-per-second each of protocol independent data. Switches permit access to particular features of the voice/data integrated circuits on both boards, as explained below.

STRAPPING INFORMATION

The component layout is shown in Figure 8. The layout shows the footprints for switches which can be used with wire straps. The solid lines indicate the normal strap positions which; select Mu law, 9600 baud data rate, with one start bit, eight data bits and one stop bit. The dip switches can be used if desired and can be obtained from:

Grayhill Inc.
561 Hillgrove Avenue
La Grange, Illinois 60525

P/N	Name	Qty
78J05	S1, S2	3
78J02	S3	1

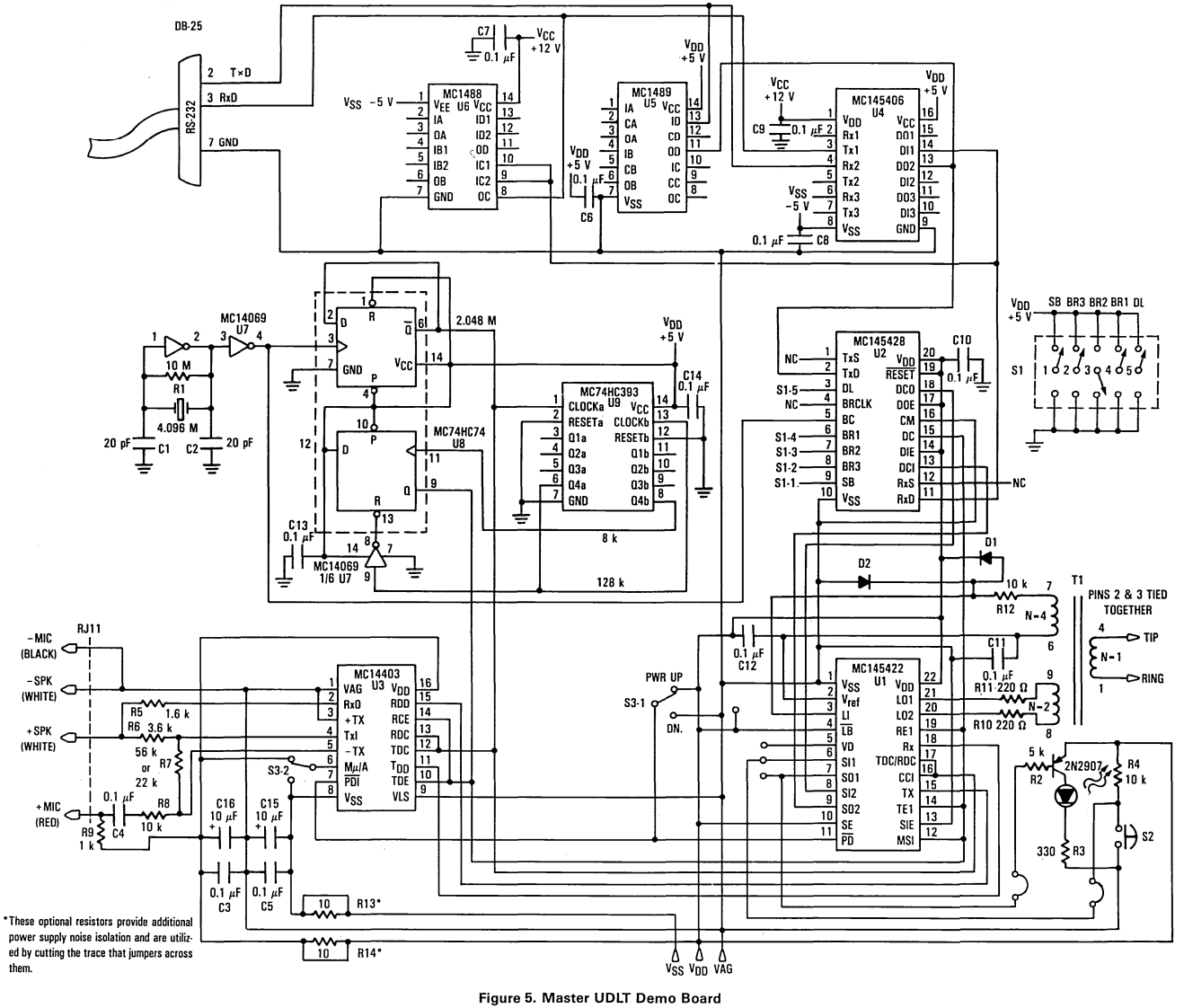
STRAPPING ON THE MASTER

S1 — These straps select via U2 (MC145428 DSI) the number of stop bits, the length of the data word and the baud rate selected for the asynchronous data.

SW1 — (SB) A high selects two stop bits; a low selects one stop bit.

SW2-SW4-(BR3-BR1) — These bit rate inputs select the asynchronous bit rate, either externally supplied at the BC pin (16 times clock) or one of the supplied bit rates shown in the table on page 2-309 of the Telecommunications data book.

SW5 — (DL) This Data Length input pin selects a nine bit data word when high or an eight bit word when low.



*These optional resistors provide additional power supply noise isolation and are utilized by cutting the trace that jumpers across them.

Figure 5. Master UDLT Demo Board

MASTER UDLT DEMO BOARD
PARTS LIST

PART	QUANTITY (PART NUMBER)
MC145422	1-U1
MC145428	1-U2
MC14403	1-U3
MC145406	1-U4
MC1489	1-U5
MC1488	1-U6
MC14069UB	1-U7
MC74HC74	1-U8
MC74HC393	1-U9
LEPCO P-1358A	1-T1
DB25	1
RJ11	1
GRAYHILL (SPDT 78J05)	1-S1
CUTLER-HAMMER B8500W/PZ81R	1-S2
GRAYHILL (SPDT 78J02)	1-S3
BANANA JACKS	6
20 pF	2-C1 & C2
0.1 μF	12-C3-C14
10 μF	2-C15, C16
10 M	1-R1
5 K	1-R2
330 Ω	1-R3
1.6 K	1-R5
3.6 K	1-R6
56 K	1-R7
10 K	1-R8
1 K	1-R9
220 Ω	2-R10, R11
10 K	2-R12, R4
10 Ω	2-R13, R14
CRYSTAL	1-4.096 M
JUMPERS	10
DIODES 1N914	2-D1, D2
LED (T1)	1
2N2907	1
SOLDER TAIL SOCKETS	
14 PIN	5
16 PIN	2
20 PIN	1
22 PIN	1

S2 — This switch is optional and is hardwired to signaling channel one for demonstration using LEDs. The footprint for this switch is included on the board.

This switch can be obtained from:

Cutler-Hammer
P/N B8500W/P281R

S3 — These straps select Mu or A laws and power down on the MC14403 Mono-circuit and MC145422 master UDLT.

SW1 — (PD) This strap when high, powers both the mono-circuit and master UDLT. When low, both parts are powered down.

SW2 — (Mu/A) Selects Mu or A law coding.

Loopback and Valid Data on the master can be accessed via pads.

STRAPPING ON THE SLAVE

S1 — Same as S1 on the master; selects asynchronous data format and bit rate.

S2 — These straps select Tone Enable, Power Down, Mu/A, and Loopback features of the slave (MC145426) as well as Mu/A and Power Down on the MC14402 Mono-circuit.

SW1 — ($\overline{TE}$) A high enables a 500 hertz tone.

SW2 — ($\overline{PD}$) Powers both the slave and mono-circuit up or down. High = powered up, and Low = powered down.

SW3 — (Mu/A) Selects Mu or A law coding for the mono-circuit.

SW4 — (Mu/A) Selects Mu or A law coding for the slave UDLT.

SW5 — (LB) When low, the 64 kilobits-per-second of information coming from the master will loop through the slave and return to the master. The signaling bits are unaffected.

S3 — Same as the S2 switch on the master.

POWER SUPPLY CONSIDERATIONS/LAYOUT GUIDELINES

The power supply requirements for these boards are V_{DD} at +5 volts, V_{SS} at −5 volts and V_{CC} which is the RS-232 driver positive voltage of +7 to +12 volts for the MC1488. V_{CC} may be as low as +5 volts with the MC145406 Driver/Receiver chip. The power supply current required by each of these voltages is less than 30 milliamperes. This results in a total slave board power consumption of less than 400 milliwatts. This amount of power may be supplied by the loop using a linear supply. To isolate the RS-232 port with respect to earth ground, a switching regulator powered by the loop or an external power supply will be required. If a switching regulator is used, it should be synchronized to the eight kilohertz and 128 kilohertz clocks of the slave UDLT to reduce the affects of aliasing noise into the analog circuitry of either the UDLT or audio voice channel. This function will be supported by the MC34129 Digital Telephone Switching Power Supply Controller chip. This device has the capability to power-up and regulate on its internal oscillator. After regulation is established it can synchronize to an external clock such as the slave's 128 kilohertz clock.

SLAVE UDLT DEMO BOARD PARTS LIST

PART	QUANTITY (PART NUMBER)	PART	QUANTITY (PART NUMBER)
MC145426	1-U1	500 Ω	1-R6
MC145428	1-U2	10 K	1-R7
MC14402	1-U3	56 K	1-R8
MC145406	1-U4	220 Ω	2-R9, R10
MC1489	1-U5	10 K	3-R11, R13, R2
MC1488	1-U6	1 K	1-R12
LEPCO P-1358A	1-T1	10 Ω	2-R14, R15
DB25	1	JUMPERS	12
RJ11	1	CRYSTAL	1-4.096 M
GRAYHILL (SPDT 78J05)	2-S1 & S2	LED (T1)	1
CUTLER-HAMMER B8500W/P281R	1-S3	DIODES 1N914	2-D1, D2
BANANA JACKS	6	2N2907	1
20 pF CAPS	2-C1 & C2		
0.1 μF CAPS	10-C3-C11, C14	**SOLDER TAIL SOCKETS**	
10 μF CAPS	2-C12, C13	14 PIN	2
10 M	1-R1	16 PIN	1
5 K	1-R3	20 PIN	1
330 Ω	1-R4	22 PIN	2
5 K	1-R5		

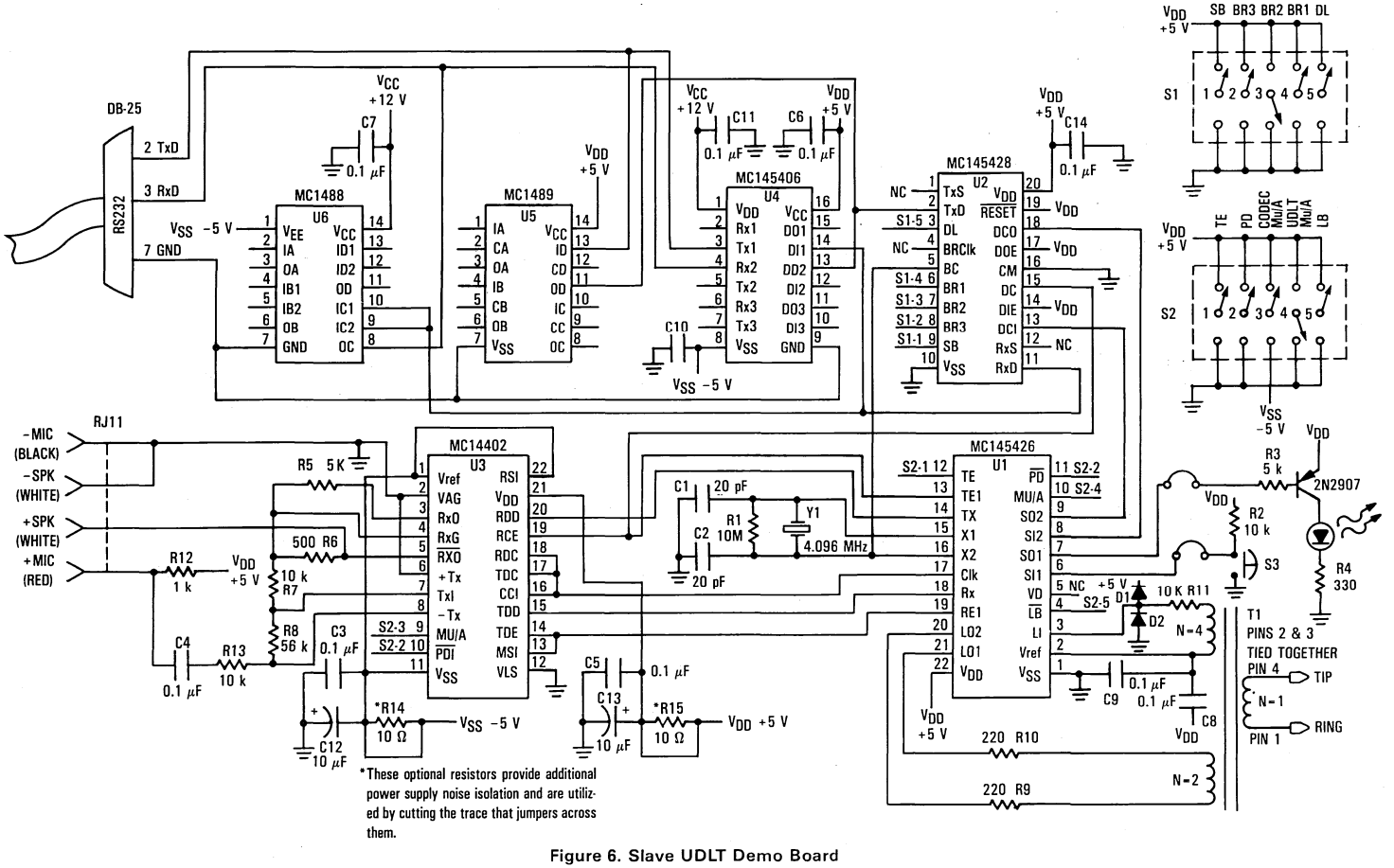
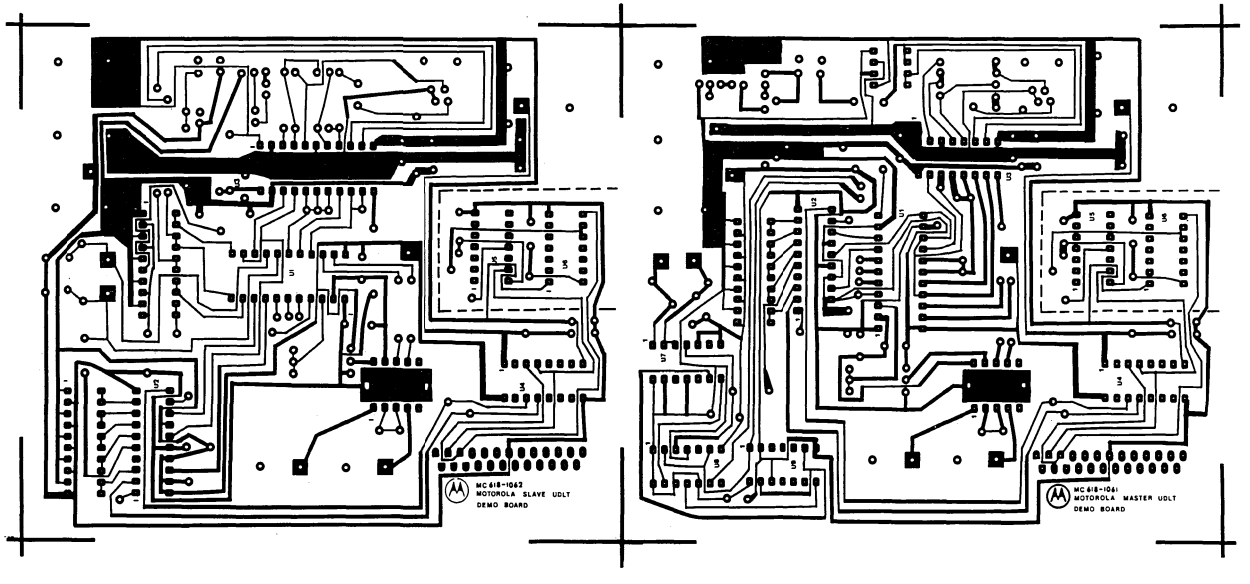
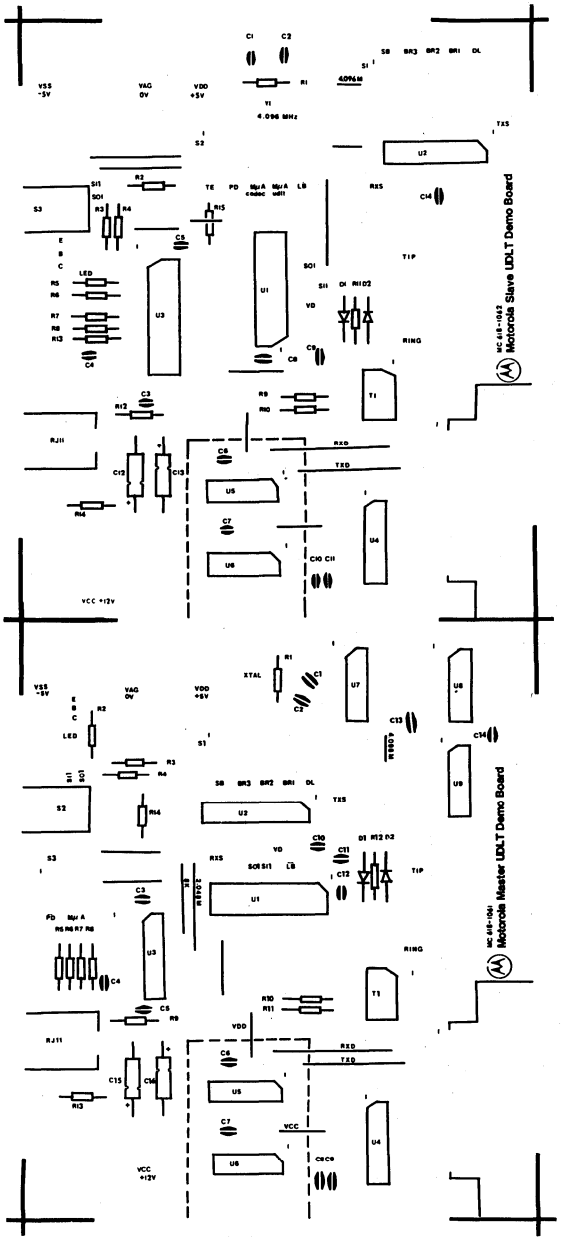


Figure 6. Slave UDLT Demo Board



NOTE: Drawings are not actual size.

Figure 7. Artwork of UDLT Voice/Data Evaluation Board



NOTE: Drawings are not actual size.

Figure 8. Component Layout

A Voice/Data Modem Using the MC145422/26, MC145428 and MC14403

GENERAL APPLICATIONS

This voice/data application allows an analog telephone system to support simultaneous voice and data across a single twisted-wire pair. Figure 1 shows how this system is implemented. To use the voice/data modem, the analog telephone line must be intercepted at the telephone system by one modem (the PBX-CPU Interface). The analog signals are then converted to digital signals, combined with data and transmitted down the remaining line as a digital loop. The second modem (the Telset-Terminal Interface) terminates the digital loop, reconstructs the analog signals and sends this information to the telephone that is plugged into the modem. The digital data is removed from the digital loop information and routed to the endpoint terminal. Any signalling information (hookswitch status and ringing) is handled by a second data channel, and it too is combined with the data and digitized voice for transmission on the digital loop.

ANALOG CODING AND DECODING

Analog signal digitization and reconstruction on both modems are done by the MC14403 Mono-circuit. The mono-circuit band limits incoming analog signals to prevent aliasing and then samples them with a sample and hold amplifier. This information is then digitized by an on-board analog-to-digital converter. This converter creates an eight bit 'companded' word for each sample by converting the signal to a pseudo-logarithmic form known as Mu-Law companding (A-Law companding is also available). In this manner approximately 78 dB of dynamic range can be represented by compromising the signal-to-distortion specifications. The mono-circuit is also capable of performing the reverse digital-to-analog conversion for this 'companding' technique. There is a reconstruction filter to convert the resultant stepped waveforms into a continuous waveform that very closely approximates the original analog input.

THE DIGITAL LOOP TRANSMISSION

The MC145422 master Universal Digital Loop Transceiver (UDLT) and MC145426 slave UDLT are used to transmit the digital information between the modems. In addition, the slave UDLT must be capable of determining and maintaining synchronization with the master UDLT so that word boundaries may be defined. The UDLT transmits a 10 bit, 256 kilobaud burst of information at an 8 kHz rate. By controlling the frequency of the burst from the master, the slave can sense and generate syncs. In this 10 bit word is the 8 bit voice sample along with one signalling bit and one data bit. Since each burst carries one digital "voice" word, the UDLT must create bursts at a rate of 8 kHz. This obviously means that both the data channel and the signalling channel operate at an 8 kbps speed.

ASYNCHRONOUS TO SYNCHRONOUS DATA CONVERSION

Since data is transferred at an 8 kbps rate in a synchronous mode, the MC145428 Data Set Interface (DSI) is used to convert an asynchronous data stream into the 8 kbps synchronous stream. The DSI can take data at speeds up to 9600 baud on the asynchronous channel and convert it to 8 kbps synchronous. The DSI is capable of supporting asynchronous speeds well in excess of 9600 baud, however, with an 8 kbps synchronous channel, dynamic handshaking on the asynchronous channel would be required. The DSI is also capable of converting the received synchronous data back into asynchronous data at the same time.

THE PBX-CPU INTERFACE

Figure 2 shows the block diagram of the PBX-CPU Interface. This circuit contains an analog interface that mimics the telephone electrical characteristics with respect to the PBX. This makes the voice/data modem transparent to the telephone system. The RS-232-C terminal interface is a 9600 baud asynchronous interface that appears to be a modem (data set equipment) to the data device (data terminal equipment). The digital loop is a specially devised transmission scheme that uses the UDLT to its fullest advantage. The digital loop is capable of excellent data performance (better than 8×10^{-8} bit-error-rate in 95% of the installations) on twisted pair up to 2 kilometers in length (26 gauge wire worst case).

The analog loop as shown in Figure 3 must be able to provide all the necessary interface considerations to simulate a telephone. The interface must be able to control the loop like a phone and it must be able to interface the voice signals, i.e., provide a 2-to-4 wire hybrid. In an idle condition (the handset is in the cradle or "on-hook"), the telephone appears as a high dc impedance. The relay provides this by "breaking" the loop and preventing dc current flow. When the phone goes off-hook, the dc impedance is drastically reduced. In a normal environment the phone must draw a minimum 20 mA of loop current, and since 48 volts is supplied to the loop at all times, this can be accomplished with resistor R6 or R7. This would energize a "ring-trip" relay coil which would disconnect any ring signals in the telephone system. At the same time an analog voice path would be established. The ac impedance of the telephone is typically held to 600 ohms to maintain transmission line balance and to minimize 60 Hz noise.

When the phone is on hook, it must be capable of detecting a ring signal. Ringing is typically a 100 volt RMS 20 Hz signal impressed on the 48 volt dc level. In this scheme ringing is detected with the MC34012 (U9) bipolar ringer chip. The 2-to-4 wire hybrid not only preserves the 600 ohm ac impedance, but it also converts a 4-wire system (separate transmit and receive) into a 2-wire current loop environment. In this design this is done with a duplexer circuit made up from the mono-circuit op-amps and resistors R12 through R16. Diodes 4 and 5 prevent excessive voltage transients from damaging the mono-circuit (U7). Engineering Bulletin EB111 provides a detailed analysis of the duplexer design.

TIMING SIGNAL GENERATION

The timing signals that drive the mono-circuit, UDLT (U4) and DSI (U5) are derived from U1, U2 and U3. U1A is a standard CMOS crystal oscillator topology designed for AT-cut parallel resonant crystals. U1B buffers the master clock signal (4.096 MHz) and then sends it to the DSI and U2A. U2A is a flip-flop that divides the signal by 2 to get the mono-circuit and UDLT master (CCI) and data clocks (2.048 MHz). U3 and U2B are a divider network that creates the 8 kHz master sync signal from the 2.048 MHz clock. This 8 kHz signal is also used as the enable signals for data communication between the UDLT and mono-circuit, and the DSI and UDLT.

Voice data is clocked out of both the UDLT and mono-circuit in 8 bit packets. These packets are defined by the 8 kHz sync positive-going level. This level is eight 2.048 MHz clocks long so the 2.048 MHz clock is the transport clock. The information is clocked out on leading edges. The information is clocked in on falling edges of the same 2.048 MHz clock and is likewise controlled by the positive portion of the 8 kHz signal.

Digital data and signalling information is directly controlled by the 8 kHz sync. The data is clocked into and out of the UDLT on the leading edge of the 8 kHz signal, and into and out of the DSI on the falling edge of the 8 kHz signal. This scheme is guaranteed on the UDLT but must be set up by tying the CM pin low on the DSI. Data out of the DSI can be three-stated through the DC0 pin, but in this application this is not necessary. The UDLT data-channel output can also be put into a high impedance mode by the SE pin, and again, this is not necessary in this application.

The asynchronous output and input of the DSI is an NRZ (Non-Return to Zero) 5-volt CMOS signal that requires level conversion to be RS-232-C compatible. The MC145406 CMOS RS-232-C Driver-Receiver chip (U6) performs this function quite nicely.

THE DIGITAL LOOP INTERFACE

The UDLT provides the needed signals for digital loop transmission. The interface circuit shown is a typical circuit designed to utilize the UDLT features to the fullest. For a detailed description of the digital loop, consult application note AN-943.

THE TELSET-TERMINAL INTERFACE

Figure 4 is the block diagram of the Telset-Terminal Interface. In a telephone system this unit must look like a line card to the telephone. The data communications port is once again intended to look like a modem. This portion of the design is the same as the digital loop interface. The only other variable part of the design is clock generation.

Clock generation is the sole responsibility of the slave UDLT. The UDLT has an on-board crystal oscillator that uses a 4.096 MHz crystal to generate a master clock. From this clock an 8 kHz sync similar to the one used in the PBX-CPU Interface is generated. This sync is now called TEI and is used like MSI except for communication from the mono-circuit. A sync that is basically the inverse of TEI, called REI, is used to enable the mono-circuit to output digital voice, and for the UDLT to receive this voice. The data clock that is generated (128 kHz) is used to clock the data with respect to TEI and REI. The DSI will use TEI to clock data to and from the UDLT, and it will get a master 4.096 MHz clock by tapping off the crystal oscillator output (X2).

The analog loop interface (see the schematic in Figure 5) uses the same duplexer circuit for regeneration of the 2-wire loop, but it must provide the complimentary signalling functions. It must first supply power to the telephone at all times and be able to tell when the phone is off-hook. Power is supplied by feeding the ± 5 volt supplies over the loop through current limiting resistors (R13 + R14). Current flow is detected through the opto-coupler (U5) when the phone is off-hook, and then hook status is passed to the loop relay on the PBX-CPU interface. Ringing is handled within the modem as opposed to generating the ring voltage and sending it to the phone. The output of the UDLT signalling channel toggles at the typical 34012 rate when the PBX is ringing out, so this output is used to drive a transistor which in turn drives a piezo speaker. An alternate solution would be to drive a small PM-type speaker that has a capacitor filter to eliminate harsh harmonics from the square waves.

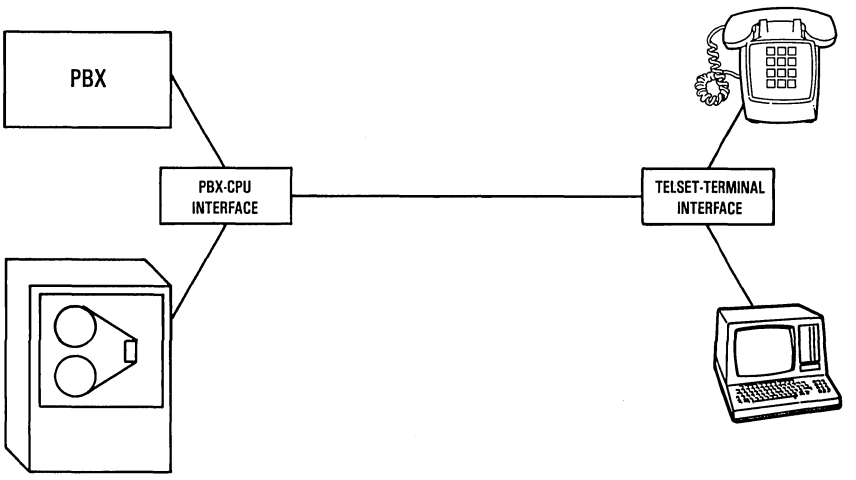


Figure 1. Typical Voice/Data Modem Implementation

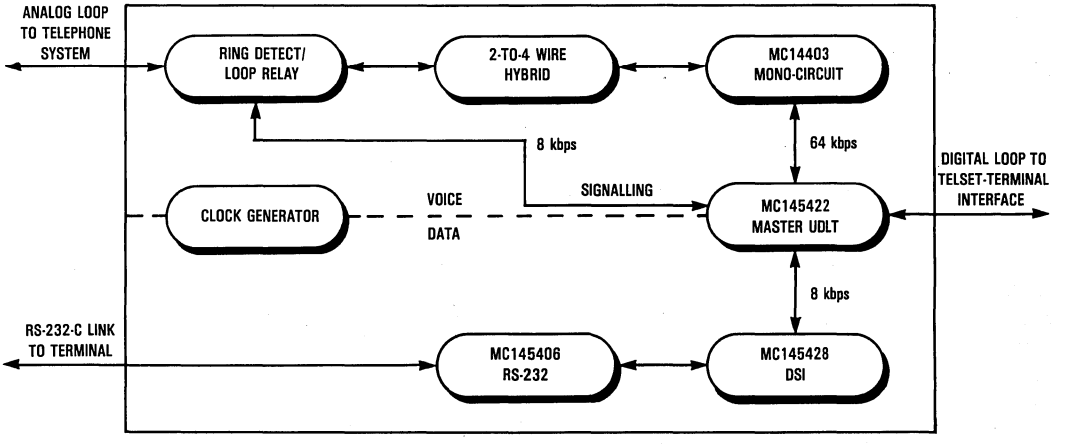


Figure 2. PBX-CPU Interface Block Diagram

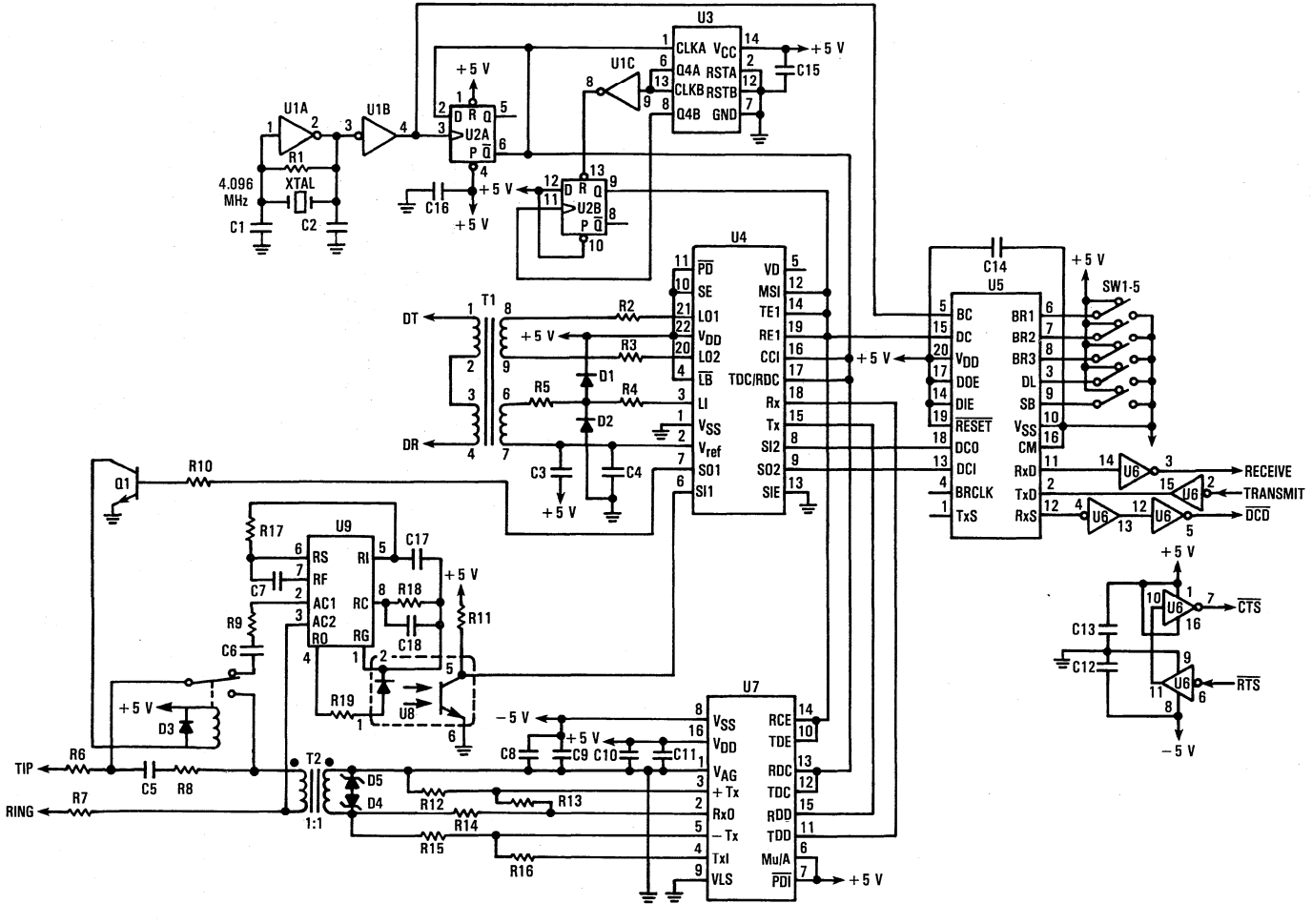


Figure 3. PBX-CPU Interface

PBX-CPU Interface Parts List

R1- 10 MΩ
R2- 220 Ω
R3- 220 Ω
R4- 1 kΩ
R5- 10 kΩ
R6- 67 1/2 W
R7- 67 1/2 W
R8- 560 Ω
R9- 4.7 kΩ
R10-4.7 kΩ
R11-270 kΩ
R12-10 kΩ
R13-20 kΩ
R14-600 Ω
R15-10 kΩ
R16-20 kΩ
R17-1.8 kΩ
R18-180 kΩ
R19-330 Ω

C1- 20 pF
C2- 20 pF
C3- 0.1 μF
C4- 0.1 μF
C5- 0.005 μF 1 kV
C6- 0.47 μF
C7- 2 μF
C8- 10 μF
C9- 0.1 μF
C10-10 μF
C11-0.1 μF
C12-0.1 μF
C13-0.1 μF
C14-0.1 μF
C15-0.1 μF
C16-0.1 μF
C17-4.7 μF
C18-1000 pF

D1- 1N914
D2- 1N914
D3- 1N4001
D4- 1N4683
D5- 1N4683
XTAL-4.096 MHz
U1- 74HCU04
U2- 74HC74
U3- 74HC393
U4- MC145422
U5- MC145428
U6- MC145406
U7- MC14403
U8- 4N26 Optocoupler
U9- MC34012
Q1- 2N2222

T1- Lepco P-1358-A
T2- 600 Ω:600 Ω
SW1-5:SPDT

Telset Terminal Interface Parts List

R1- 10 MΩ
R2- 1 kΩ
R3- 220 Ω
R4- 220 Ω
R5- 1 kΩ
R6- 10 kΩ
R7- 270 kΩ
R8- 10 kΩ
R9- 20 kΩ
R10-600 Ω
R11-10 kΩ
R12-20 kΩ
R13-92 1/2 W
R14-92 1/2 W

C1- 20 pF
C2- 20 pF
C3- 0.1 μF
C4- 0.1 μF
C5- 47 μF
C6- 0.1 μF
C7- 10 μF
C8- 10 μF
C9- 0.1 μF
C10-0.1 μF
C11-1 μF
C12-0.1 μF
C13-0.1 μF

D1- 1N914
D2- 1N914
D3- 1N4683
D4- 1N4683
Q1- 2N2222
Q2- 2N2907
XTAL-4.096 MHz
U1- MC145426
U2- MC145428
U3- MC14403
U4- MC145406
U5- 4N26 Optocoupler

T1- Lepco P-1358-A
T2- 600 Ω:600 Ω
SW1-5:SPDT

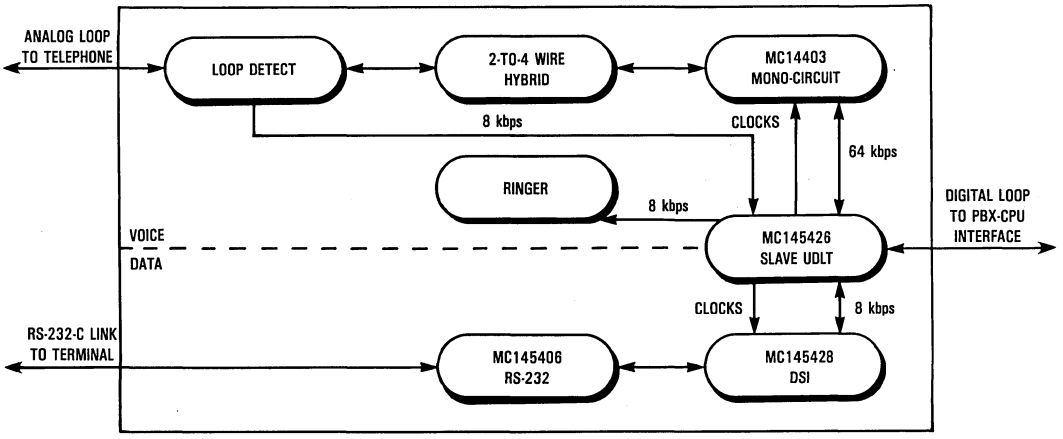


Figure 4. Telset-Terminal Interface Block Diagram

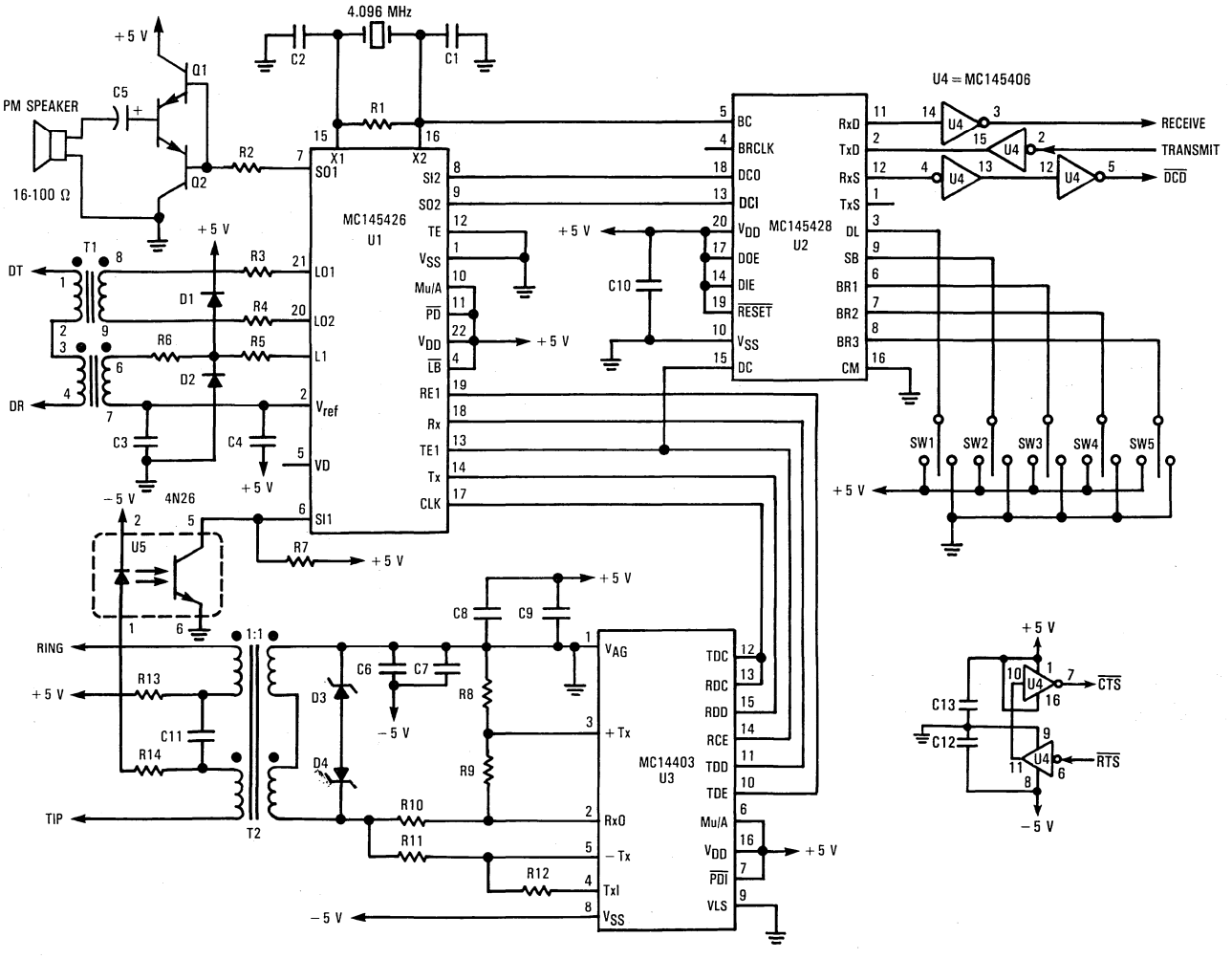


Figure 5. Telset-Terminal Interface

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

A Digital Voice/Data Telephone Set

by
Eric Fiene, Telecom Design Engineering, and
Glen Zoerner, Telecom Systems Design

OVERVIEW

This application note presents the design of a digital voice/data telephone set which provides standard analog telephone functions while simultaneously transmitting 9600 baud asynchronous data. This telephone set is built around Motorola's MC145422/26 UDLT (universal digital loop transceiver) family of voice/data ICs. The UDLTs provide 80 kbps full-duplex synchronous communication at distances of up to two kilometers on a single 26 AWG twisted pair telephone wire. The MC14403 codec/filter and MC145428 data set interface (DSI) convert voice and data signals respectively into digital formats compatible with the UDLTs' transmission scheme. The design includes the MC145413, a full-featured pulse/tone dialer, and the MC145406, a CMOS RS-232 driver/receiver for communicating with an external terminal or PC. An efficient switching power supply utilizing the MC34129 provides isolated power for the digital telephone set directly from the 48 V available on the transmission twisted pair.

BACKGROUND

Data has been transported over telephone lines for years, but the techniques for compressing the data into the voice bandwidth are getting more elaborate and expensive as data rates increase. Digital telephones simplify the task by directly sending high-speed digital data over the wires for distances of up to 2 km. The data is combined with voice information digitized by the codec/filter and signalling. This combined signal is transported over existing wiring to a digital linecard in a PBX or a voice/data multiplexer.

Digital PBXs used with analog telephones convert analog voice information into digital signals on the linecards for routing through the switch matrix. In a system where the analog telephones are replaced by digital phones, the digitization is still performed, but it is done in the phone itself and digital information is transported on the wires. Data from an attached PC or terminal can easily be combined with the digital voice and be transported to the PBX. At the linecard, the data can either be routed through the switch matrix or separated from the voice and connected directly to a data-only PBX or computer. Signalling between a digital telephone and the PBX is typically done by packet messages, with a microprocessor in the telephone to interpret the messages. This digital telephone uses traditional tone signalling on the voice channel. Hookswitch status is sent to the PBX on the inbound (to the PBX) link of the 8 kbps Signalling Channel One, and ringing information is sent to the phone on the outbound (from the PBX) link of Signalling Channel One.

This digital telephone could be used with a special digital linecard in a PBX or a voice/data multiplexer. To maintain generality, this application note will describe a system where a multiplexer is used rather than a linecard in a specific PBX system. The general principles, however, can be used in a linecard design. This telephone design has been used with both a digital linecard and a voice/data multiplexer.

The voice/data multiplexer in Figure 1 is described in detail in application note AN949. However, a brief description will be made here. From the PBX's point of view, the multiplexer appears to be an ordinary telephone. The telephone hookswitch is replaced by a relay which is controlled by a signal from the digital telephone. The ringing signal from the PBX is detected, sampled, and transported to the digital telephone where it is amplified and applied to a speaker. Analog voice signals are digitized and reconstructed and applied to the wires connected to the PBX through the duplexer in the codec/filter. Asynchronous data from the computer or data switch is synchronized to the UDLT timing by the DSI and added to the digital data stream. The combined signal is transported to the digital telephone which separates the signals and attaches to the data terminal. DC power is applied to the twisted pair wire at the multiplexer and transported over the wires so no extra power cords are required for the telephone.

The following sections describe the details of the digital telephone. Figure 2 shows a block diagram of the digital telephone set. Figures 3 and 4 are complete schematics of the telephone circuitry and the power supply respectively.

UDLT

The heart of the digital telephone set is the UDLT slave (MC145426). This chip is essentially a modem transceiver which operates over standard twisted pair telephone wiring. A 256 kbps data rate using modified differential phase shift keying (MDPSK) in a half-duplex time compression multiplex or "ping-pong" scheme provides full-duplex 80 kbps transmission. Transmission begins with the UDLT master (MC145422), which is located at the other end of the twisted pair in the voice/data multiplexer, bursting 10 bits of information to the slave. A similar burst is returned from the slave to the master a short time after the master's burst has been demodulated. This exchange occurs 8000 times per second

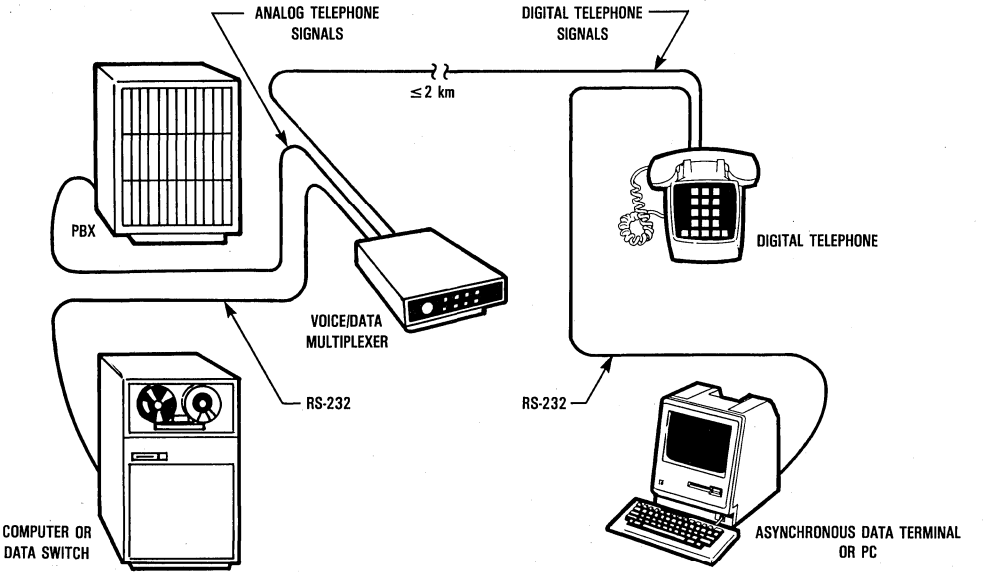


Figure 1. Voice/Data System

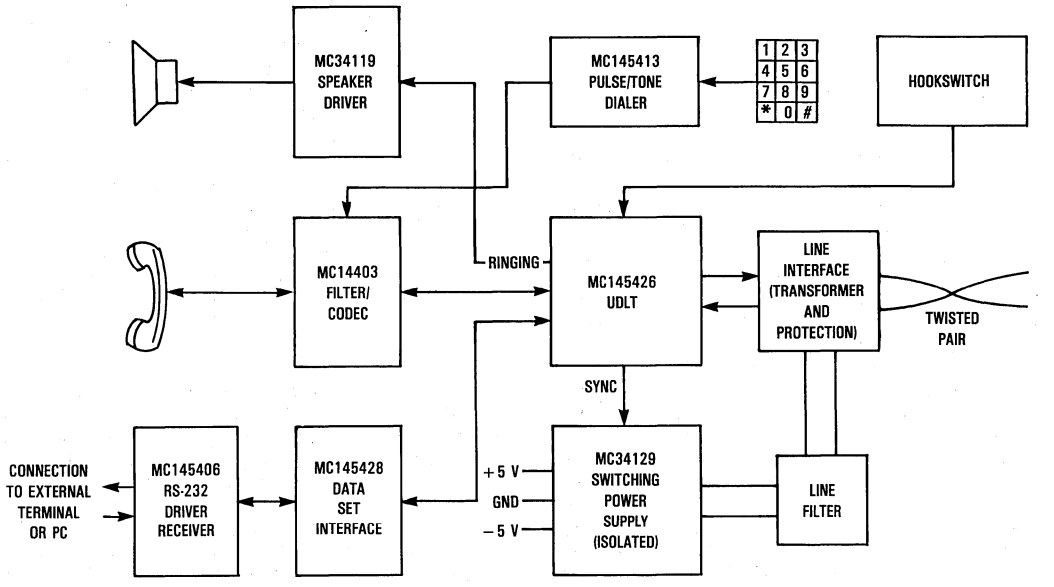


Figure 2. Digital Telephone Block Diagram

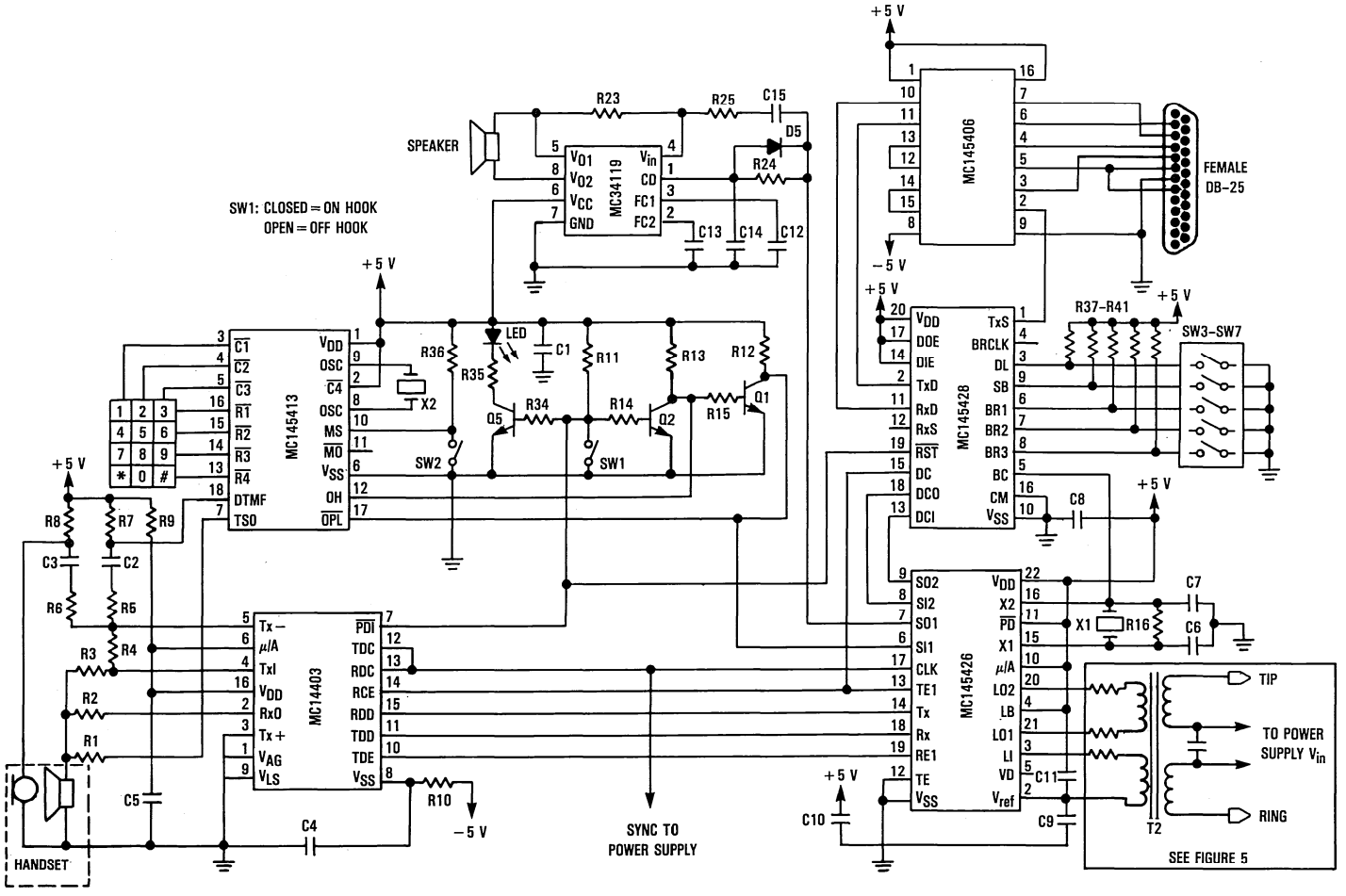


Figure 3. Digital Telephone Schematic

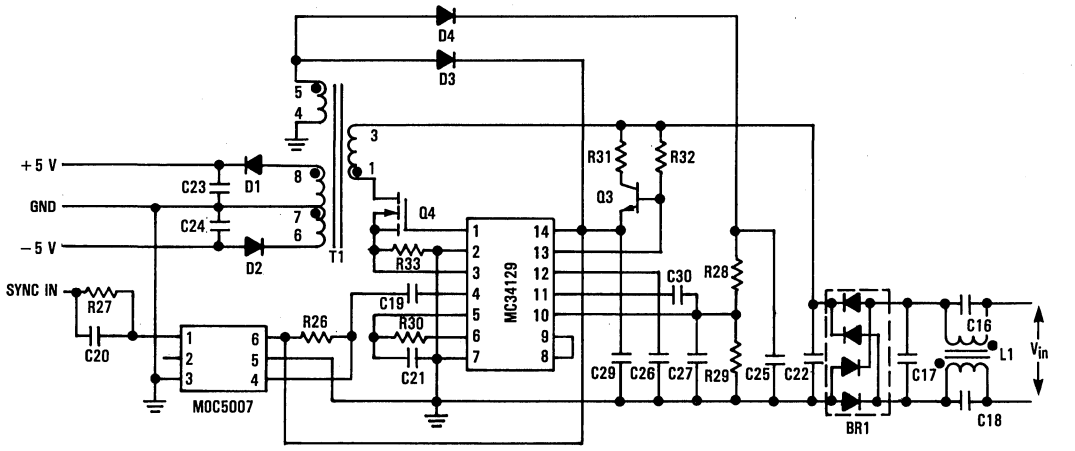


Figure 4. Switching Power Supply

PARTS LIST FOR FIGURES 3, 4, AND 5

Resistors

R1	22 kΩ
R2	3.3 kΩ
R3	7.5 kΩ
R4	47 kΩ
R5	22 kΩ
R6	10 kΩ
R7	620 Ω
R8	1 kΩ
R9–R10	10 Ω
R11–R13	10 kΩ
R14–R15	100 kΩ
R16	10 MΩ
R17	10 kΩ
R18	5 kΩ
R19–R22	110 Ω
R23	75 kΩ
R24–R25	100 kΩ
R26	10 kΩ
R27	3 kΩ
R28	9.1 kΩ
R29	1.3 kΩ
R30	22 kΩ
R31	2.2 kΩ
R32	220 kΩ
R33	10 Ω
R34	100 kΩ
R35	560 Ω
R36–R41	10 kΩ

Inductor

L1 80 μH each winding on a common core

Capacitors

C1–C3	0.1 μF
C4–C5	10 μF
C6–C7	20 pF
C8–C9	0.1 μF
C10	10 μF
C11–C15	0.1 μF
C16	0.005 μF
C17	0.1 μF
C18	0.005 μF
C19	100 pF
C20	0.01 μF
C21	330 pF
C22	100 μF (50 V)
C23–C24	100 μF (16 V)
C25	10 μF (16 V)
C26	0.1 μF
C27	510 pF
C28	0.1 μF
C29	10 μF (16 V)
C30	0.01 μF

Transformers

T1: Power Transformer
Coilcraft G6808-A

T2: Line Transformer
Coilcraft G6320-D or
Lepco P-1358-A

Diodes

D1	1N5819
D2–D11	1N4148
BR1	3N248 Bridge Rectifier

Integrated Circuits

MC14513	Dialer
MC14403	Mono-circuit
MC145428	Data Set Interface
MC145426	Slave UDLT
MC145406	RS-232 Transceiver
MC34119	Speaker Driver
MC34129	Power Supply Controller

Optocoupler

MOC5007 High-speed Optocoupler

Transistors

Q1–Q2	2N3904
Q3	2N5551 160 V NPN
Q4	MTP2N20 Power MOSFET
Q5	2N3904

Switches

SW1	SPST Hookswitch
SW2–SW7	DIP Switches

(every 125 μs), so the transceivers effectively exchange 80 kbps of full-duplex synchronous data. The data is arranged into three channels, a 64 kbps full-duplex voice channel and two 8 kbps full-duplex data channels.

The slave UDLT generates all timing signals used by the digital telephone. Timing is synchronized to the received bursts from the master UDLT. A 4.096 MHz on-chip crystal oscillator is the basis for all clocks. A 128 kHz clock (CLK), which drives the mono-circuit's D/A and A/D circuits and synchronizes the power supply, is produced. An 8 kHz clock (TE1 and RE1) is also produced. Any timing slip from master to slave UDLTs is corrected every 125 μs, keeping the master and slave devices in perfect synchronism. The baud rate generator in the data set interface is driven by the 4.096 MHz clock on the slave UDLT.

The burst received from the master's transmission is input on the slave's line input (LI) pin. The burst is demodulated, separated into the three channels, then output on the digital side of the slave every 125 μs. Eight voice bits are output serially from the transmit data output (Tx) on the rising edges of CLK while TE1 is high. One signalling bit is output on signalling output 1 (SO1) on the rising edge of TE1. The outbound signalling channel one provides the ringing signal for the speaker amplifier (MC34119). The other signalling bit is output on signalling output 2 (SO2) to the data set interface (MC145428), also on the rising edge of TE1. This channel, both inbound and outbound, carries the data between the attached terminal and the data switch or computer at the voice/data multiplexer or PBX.

After the slave receives a burst from the master, it transmits a 10-bit burst of its own back to the master. The slave outputs this burst on its line driver outputs (LO1, LO2) which are push-pull drivers configured as a balanced bridge. These outputs directly drive the line transformer through a resistor loading and protection network (see Figure 5). The 10 bits of data which are transmitted to the master are input every 125 μs. Eight bits of voice data are input serially on the receive data input (Rx) on the falling edges of CLK while receive data enable (RE1) is high. A signalling bit which carries the digital telephone's hookswitch status back to the voice/data multiplexer is input on signalling input 1 (SI1) on the rising edge of TE1. Data from the attached terminal or PC is input on signalling input 2 (SI2), also on the rising edge of TE1.

Transformer T2 interfaces the twisted pair wire to the UDLT's LO1, LO2, and LI pins. It performs the functions of impedance matching, bandwidth limiting, and gain adjustment for the receive signals. At the frequencies of interest (128 kHz and 256 kHz), ordinary telephone wire has a characteristic impedance of about 110 ohms. The loading resistors R19–R22 between LO1, LO2 and the Tx winding of the transformer are set to 110 ohms. The series combination of these resistors is significantly higher than the 20-ohm output impedance of the LO1 and LO2 drivers causing the resistance presented to the transformer to be set primarily by the resistors alone. Clamp diodes D6–D9 protect the LO1 and LO2 outputs from transient signals on the twisted pair. Line settling between data bursts is improved by selecting a bandwidth of 20 to 512 kHz for the transformer interface. The lower corner frequency is set by adjusting the inductance of the transformer's Tx winding to 1.75 mH. The upper corner frequency is determined by the design of the transformer winding technique.

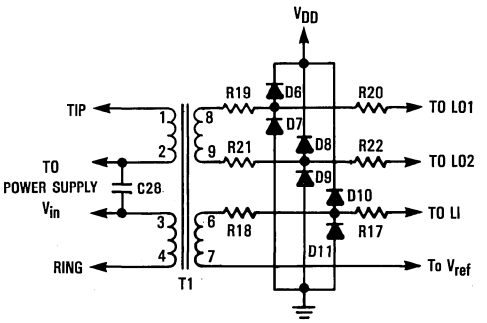


Figure 5. Line Interface and Protection

The impedance matching network on the transmit side of the transformer attenuates the transmitted signal by 12 dB. This loss is recovered in the receive side of the transformer. A step-up of 4:1 directly compensates for the 12 dB loss. As with the transmit side, a protection network is required. D10 and D11 clamp the received signal to a safe level but are sufficiently isolated by R17 so that they do not load the transformer when they are conducting. At 192 kHz (the spectral peak of MDPSK), 26 AWG wire attenuates signals about 17 dB/km. The receiver in the UDLTs has sufficient input dynamic range to operate on loops as long as 2 km. Transformers which are designed for the UDLT system may be obtained from:

Coilcraft, Inc.
1102 Silver Lake Rd.
Cary, Illinois 60013
Part Number: G6320-D

Leonard Electric Products Company
85 Industrial Drive
Brownsville, Texas 78521
Part Number: P-1358-A

The transformer from Coilcraft is similar to the Leonard Electric device, except it has a Faraday shield between the Rx and Tx windings and the line windings. The shield helps reduce the spurious radiation from the digital circuitry onto the twisted pair.

CODEC/FILTER

The MC14403 codec/filter is a PCM codec-filter which performs D/A, A/D, band-limiting, and reconstruction filtering for the voice signals in the digital telephone. Analog voice signals in the 300 Hz to 3400 Hz frequency band are sampled at an 8 kHz rate. The samples are converted into a pseudo-logarithmic code known as PCM and passed to the UDLT for transmission to the voice/data multiplexer or PBX. Received digital signals are reconstructed at an 8 kHz rate back into analog voice signals.

Three signals are available for use on the analog input amplifier. They are Tx+ (noninverting input), Tx− (inverting input), and TxI (filter input). Sidetone (feedback from the handset microphone to earpiece) and gain balance are controlled with external components around the Tx and Rx operational amplifiers in the codec/filter. Tx+ is tied to ground and a gain setting resistor is placed between Tx− and TxI.

The microphone output from the handset and the DTMF output from the dialer are both ac coupled to the Tx− input. The output of this amplifier is digitized and output to the UDLT on TDD on the eight rising edges of TDC when TDE is high. Digital data is input from the UDLT on RDD on the first eight falling edges of RDC after the rising edge of RCE. This data is reconstructed and output on the analog output pin (RxO). This signal is summed with TSO from the dialer and TxI and applied to the speaker in the handset.

A decoupling RC filter is used to attenuate any power supply noise seen at V_{CC} and V_{SS} of the codec/filter. This filter consists of 10-ohm resistors in series with the power feed to V_{CC} and V_{SS} with 10 μF capacitors from V_{CC} and V_{SS} to ground. Also, to reduce noise in the ground paths, a star-grounding scheme is used where all ground pins of the circuits are connected to the power supply's central isolated ground.

DATA SET INTERFACE

The MC145428 data set interface (DSI) is an interface between an asynchronous data terminal and the synchronous 8 kbps full-duplex data channel of the UDLT. The DSI performs basic UART functions of start-bit and stop-bit detection of the asynchronous data. It also detects and transports break signals over the synchronous link. Start and stop bits are stripped from the data which is then loaded into a FIFO. The data is then sent to the UDLT for transmission to the far end of the digital link. On the receive side, the reverse of these actions is performed. Special synchronization characters (transparent to the user) are exchanged between DSIs to maintain synchronization. The DSI has an internal clock generator which produces the most commonly used baud rates. The DSI is capable of operating at data rates up to 128 kbps, however this application uses 9600 baud.

On the synchronous side of the DSI, data is output to the UDLT on the data channel output (DCO) on the falling edge of data clock (DC) while the data output enable (DOE) is high. Data from the DSI is input and output by the UDLT on SI2 and SO2 respectively. DC is connected to TE1 of the UDLT. DIE and DOE are connected to V_{DD}, permanently enabling the synchronous inputs and outputs. RESET is connected to the hookswitch, clearing the FIFOs and resetting the device when the digital telephone is not in use.

RS-232 DRIVER/RECEIVER

The RS-232 interface is connected as follows. Asynchronous serial data from the attached data terminal (Tx DATA, RS-232 pin 2) is through a receiver on the MC145406 RS-232 driver/receiver and connected to the transmit data input (TxD) of the DSI. Asynchronous serial data from the DSI is output on the receive data output (RxD) and fed through a driver on the MC145406 to the data terminal (Rx DATA, RS-232 pin 3). Another output of the DSI, transmit data status (TxS), is used to generate a clear-to-send signal for local flow control (CLEAR-TO-SEND, RS-232 pin 5). TxS goes low when there are two words in the DSI's transmit FIFO and must be inverted to provide the CTS function. TxS is applied to a receiver of the MC145406 for inversion and then fed through a driver to convert the signal to RS-232 levels. The MC145406 threshold for the RS-232 receivers is 1.8 volt so it may be used as an inverter for ordinary digital signals. The receive data status (RxS) pin of the DSI may be used as a carrier detector. Since it goes high when synchronization with the far-end DSI is established, it must also be inverted before conversion to RS-232 levels. As with the TxS signal, an RS-232 receiver is used an an inverter. The inverted signal is then converted to RS-232 levels by a transmitter and applied to RECEIVED LINE SIGNAL DETECT, RS-232 pin 8. The baud rate, word length, and number of stop bits used on the asynchronous side of the DSI are controlled by five pins: BR1–BR3, DL, SB. These inputs are controlled by a DIP switch. Table 1 shows the switch settings to configure the asynchronous data port.

DIALER

The pulse tone repertory dialer (MC145413) converts keyboard inputs to either pulses or dual tone multiple frequency (DTMF) or Touch-Tone outputs for use in telephone dialing. This device also provides last number redial and a nine number repertory memory. The digital telephone in this application uses a 3 × 4 class A single contact keyboard, although a 4 × 4 keyboard could have been used for enhanced features. The MC145413 operates in pulse mode at either 10 or 20 pulses per second, or tone dialing modes. These modes are determined by the mode select (MS) pin.

When the pulse dialing mode is used in this telephone, dialing information is output at 20 pulses per second. Note: The PBX used with this telephone is capable of accepting dialing pulses at this rate. Other applications may require the pulses at 10 pulses per second, in which case the wiring of the DIP switch would have to be modified appropriately. The pulse output OPL, is an N-channel open-drain transistor which is wire-ORed with the hookswitch. This point is sampled 8000 times each second by the UDLT, and the status is passed to the loop monitoring circuitry in the voice/data multiplexer on signalling channel 1. In the tone dialing mode, dialing information is output as tones corresponding to the row and column pressed. This signal is output on the DTMF OUT pin of the dialer and is coupled to the analog input of the codec/filter. The analog DTMF signal is thus carried to the PBX in digital form on the 64 kbps voice channel.

Table 1. DIP Switch Settings

Pin Name	Low	High
DL	8 bits	9 bits
SB	One	Two
MS	Tone	Pulse

Baud	BR3	BR2	BR1
9600	0	1	1
4800	1	0	0
2400	1	0	1
1200	1	1	0
300	1	1	1

SWITCHING POWER SUPPLY

Figure 4 shows the schematic of the switching power supply for the digital telephone. This power supply has the capability of supplying about 900 mW of power at ±5 V when the length of the loop is 2 km. As the loop length is increased, the power available at the phone is reduced. To maintain stability of the power supply, the maximum power consumed by the phone (including the efficiency losses in the power supply) must be

less than 90% of the maximum power available (MPA) at the maximum loop length.

$$MPA = V_{source}^2/(4 \cdot R_{loop})$$

Example: R_{loop} for 2 km of 26 AWG wire = 576 Ω

$$MPA = 48^2/(4 \cdot 576\ \Omega) = 1\ Watt$$

The ±5 V outputs are isolated from the twisted pair so that a local ground reference may be established with the terminal attached to the RS-232 port.

The switching power supply operates by repetitively storing and releasing energy in a transformer. The energy is stored in the primary winding of transformer T1 for part of the switching cycle and discharged into the load through the secondary during the remaining part of the cycle. The controller for this power supply is the MC34129 high-performance current-mode power-supply controller. The MC34129 controls the current (energy) in the primary winding by varying the duty cycle of the power switch (Q4). As the duty cycle is changed, more or less energy is stored under control of the MC34129 to maintain regulation of the output voltage. The switching frequency of the power supply is synchronized to the 128 kHz clock signal used by the codec/filter by bringing CLK from the UDLT through an opto-isolator (MOC5007) into the sync input (pin 4) of the MC34129. Synchronization improves the idle-channel noise performance of the codec/filter and minimizes the filter requirements on the output of the power supply.

The input voltage for the power supply is taken from the 48 V available on the twisted pair. A 0.1 μf capacitor is placed between the two line windings of transformer T2. The dc voltage across the capacitor is then routed through a balanced three-pole elliptical lowpass LC filter (L1 and C16-C18) and a full-wave rectifier before being applied to the input of the power supply.

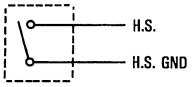
The power supply is regulated by two methods. Current in the primary winding is sensed as a voltage across resistor R30. Also, the +10 V nonisolated output is sensed by being fed back to the voltage divider formed by resistors R25 and R26. The controller maintains the voltage across R26 at 1.25 V by varying the switching duty cycle. This forces the output voltage to be 10 V. Regulation of the +5 V isolated outputs is maintained by the magnetic coupling from the 10 V winding to the +5 V windings. Because the primary current is sensed by the MC34129, pulse-by-pulse overcurrent limiting is automatically achieved. The power supply is thus fully protected against short circuits on the outputs. If an overload occurs, the MC34129 will shut the power supply down and attempt to restart. When the overload is removed, the power supply will again begin normal operation.

During normal operation, the MC34129 is powered by the +10 V output. However, since there is no voltage at this output when the circuit is first started-up, provisions must be made to power the circuit from another source until the outputs are stable. Transistor Q3 and the Start/Run output perform this task. During start-up, Q3 is biased on and power for the MC34129 is taken from the 48 V on the twisted pair through R28. After the power supply has completed the soft-start cycle and stabilized, transistor Q3 is turned off by the Start/Run pin (pin 13) and power is supplied by the +10 V output. This start-up sequence allows the power supply to reliably start in the presence of high source resistance seen at the end of a long twisted pair wire. Efficiency of this power supply is approximately 80%.

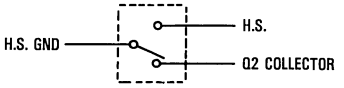
APPENDIX

On the printed circuit board there are three connections available for the hookswitch (SW1). These are +5 V, GND, and SI1. The following is a list of several implementations of the hookswitch.

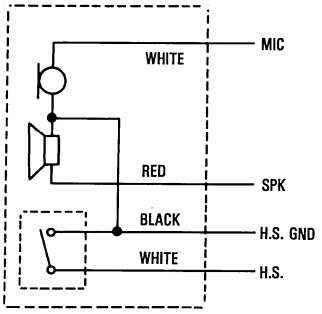
1. **Mechanical SPST switch (normally open)** — In this configuration the LED, R32, R31, and Q5 are not needed unless an LED signal is desired.



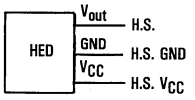
2. **Mechanical SPDT switch (normal position shown)** — In addition to the components listed in the above implementation, R14 and Q2 are not needed.



3. **Reed relay in handset (magnet in telephone case)** — The figure below shows how to modify the handset for this application.



4. **Hall Effect Device in telephone case (magnet in handset)** — For this and the previous application, a mechanical SPST switch can be used in parallel for on-hook operation.



IMPLEMENTING INTEGRATED OFFICE COMMUNICATIONS

By Tanya Tussing
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INTRODUCTION

ISDN has gotten a lot of attention during the course of the last year, and rightfully so. It's a revolutionary concept. The idea of being able to send high-speed data over a public network to anywhere in the world is phenomenal. But the hard questions concerning ISDN quickly become evident when a company contemplates designing a real ISDN system with an introduction date in the near future. Although the "U" interface being defined by the T1D1.3 committee in North America has a well defined function in the ISDN wide area network system, the local area network is a different situation.

ISDN discusses three local area network interfaces: the "S", "T", and "R" interface. (The ISDN reference model is shown in Figure 1.) The "S" and "T" interfaces have an identical specification, but the "R" interface is open, in other words—user defined. A key product strategy question asks which interface best services a particular function of the ISDN local area network. When formulating an answer, there are many parameters to consider. They all revolve around manufacturing costs vs. providing customers with the features they feel they need at the time the products are introduced. Some of these customer-driven parameters include price, performance, and compatibility to standards of terminals, peripherals—e.g., printers and the wide area network. These kinds of questions need to be addressed before a design specification can be completed.

ISDN REFERENCE MODEL

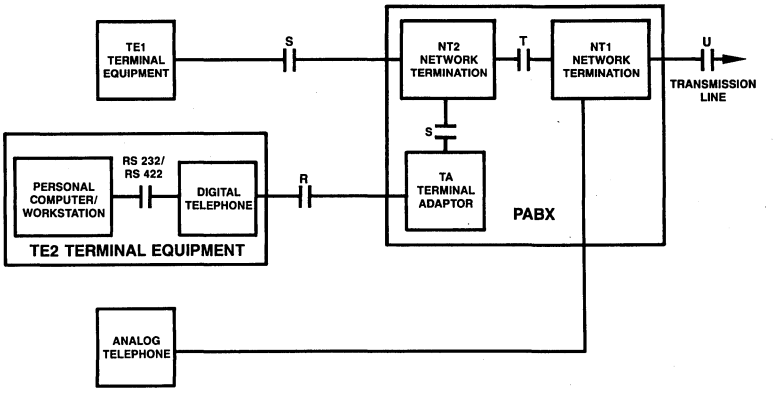


Figure 1

K5056

Question 1: Which terminal standards must be supported by an ISDN local area network in the near future?

Answer: RS-232 is now, and will be for some time to come, the most prominent terminal interface specification. So, whatever method is used to transmit data to the terminal—"S/T" or another—an RS-232 interface will be needed for many terminals for quite awhile.

Question 2: Is ISDN a mature standard?

Answer: No, ISDN is not a mature standard. So, any product designed today will probably have to be modified to fulfill the final ISDN specification.

Question 3: Will an ISDN terminal using an "S/T" interface for layer 1 communication and LAP-D for layer 2 communication be the best voice/data solution available for most applications?

Answer: The "S/T" interface and LAP-D are both specifications which try to accommodate many different functions. In some cases they may provide more features than are needed— for a price that consequently cannot be justified.

Because of these kinds of reasons, Motorola has a two-part product strategy. First, Motorola introduced a family of cost-effective voice/data integrated circuits which are compatible with the evolution of ISDN. The second part of the voice/data strategy is to develop an "S/T" transceiver, an LAP-D controller, and a "U" transceiver, as the specifications become more clearly defined.

MOTOROLA'S VOICE/DATA I.C. SOLUTIONS

There are many different ways to design a voice/data terminal. The following paragraphs describe three different approaches which vary in complexity/cost, data rate throughput, transmission distance, and system flexibility.

SYSTEM I: BASIC VOICE/DATA TERMINAL—B + D

A basic terminal, as shown in Figure 2, uses the slave UDLT, MC145426, to communicate the voice and data information to a switch. In the switch's line card is a master UDLT, MC145422. It converts the signals back into the original PCM, data, and signalling format. So, the PCM code can be transmitted through the switch as if a monocircuit (codec/filter) were sitting on the line card, and one of the signalling channels can convey the switchhook and ringing information. In this configuration, the dialing information is transmitted in the voice path and would be handled like a normal analog line card in a digital PABX. Because the UDLT interfaces to the switch like a monocircuit, the conversion from analog line cards to digital line cards is relatively painless.

The other signalling channel sends data to the line card. At the master UDLT, this data can either be put into a separate time slot on the line card—allowing the data to be switched separately from the voice, or it can be stuffed into the least significant bit of the PCM word—allowing it to be routed around with the voice information. Routing voice and data through one time slot per phone decreases the number of time slots needed for the system, and consequently, the switching system's complexity decreases.

The Universal Digital Loop Transceiver

The UDLT is an 80 kilobit per second (kbps) synchronous transceiver chip set capable of transmitting data up to two kilometers on 26 awg twisted pair wire. Between the UDLT master—MC145422 and the UDLT slave—MC145426, 10 bit data bursts at a 256 kHz rate are sent back and forth from the master and the slave. This is called a "ping pong" transmission scheme.

B + D VOICE/DATA TERMINAL

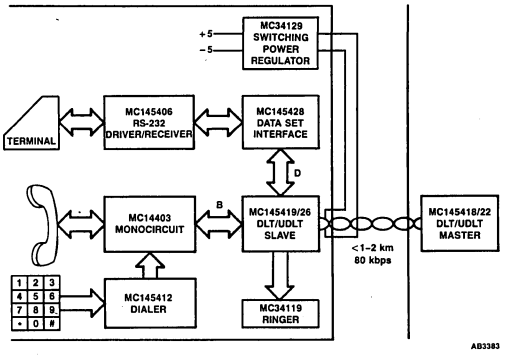


Figure 2

Figure 3 is a timing diagram showing the relationship between the master ane slave bursts, as well as the master sync input (MSI). First, a burst is differentially driven from the master's LO1 and LO2 pins to the slave's LI pin, referenced to V_{ref}. From this master burst, the slave synchronizes its clocks to the master's clocks and responds with a burst from its LO1 and LO2 pins to the master's LI pin.

The bursts are coded into a triangular Modified Differential Phase Shift Keyed (MDPSK) waveform. The MDPSK method was chosen because it minimizes radio frequency, electromagnetic, and crosstalk interference. Tests have shown that this MDPSK ping pong transmission technique can achieve better than a 10^{-7} bit error rate over two-kilometer distances.

The 10 bit data burst, from either the slave or the master, is derived from three different inputs of the chip. The Rx pin contributes 8 of the 10 bits, and the SI1 and the SI2 pins each contribute 1 of the 10 bits. Because both the master and slave bursts are typically sent at an 8 kHz rate, the data rates through these pins are 64 kbps, 8 kbps, and 8 kbps, respectively. The output of the 64 kbps channel is the Tx pin and the output of the 8 kbps channels are the SO1 and the SO2 pins. With the same data rate as the CCITT B channel, the 64 kbps channel can be used for standard PCM voice or it can be used to transmit high speed data. The 8 kbps channels are well suited for transmitting signalling—such as dialing, switchhook, and ringing information—or data. With a little external logic, the two 8 kbps channels can be combined into one 16 kbps channel—which is the same data rate as the CCITT LAP-D channel. This chip is available today in production quantities.

The Digital Loop Transceivers vs. the UDLT

The Digital Loop Transceiver (DLT) chip set, MC145418/MC145419, is very similar to the UDLT in function but is designed for applications requiring shorter loop lengths (< 1 k). There are three main differences between the UDLT and the DLT chips. The most important difference between the chip sets is that the UDLT automatically adjusts the threshold on the receive circuitry. This allows the UDLT to optimize its reception to a particular line's attenuation level. The DLT's threshold is externally set, so typically this receive optimization will not be achieved—unless some rather complex circuitry is implemented. Also, the DLT requires external drivers and usually transmits square waves instead of triangular waves. In conclusion, the UDLT has more features than the DLT, but the DLT's basic approach allows driver and threshold design flexibility. The DLT is available today in production quantities.

The Monocircuit Family

The single chip codec/filter (monocircuit) family consists of five different devices ranging in size from a 16 pin package to a 22 pin package. They are the 14400, the 14401, the 14402, the 14403, and the 14405. These chips perform standard PCM voice digitization and reconstruction. They will operate in both the U.S. standard, Mu-Law, and in the European standard, A-Law, companding formats. The chip includes on-board antialiasing/60 Hz rejection filtering, as well as low pass reconstruction smoothing filtering.

As opposed to just operating with split power supplies of ±5 volts, the chip will operate well using a variety of

80 KBIT/SECOND CHANNEL TIMING

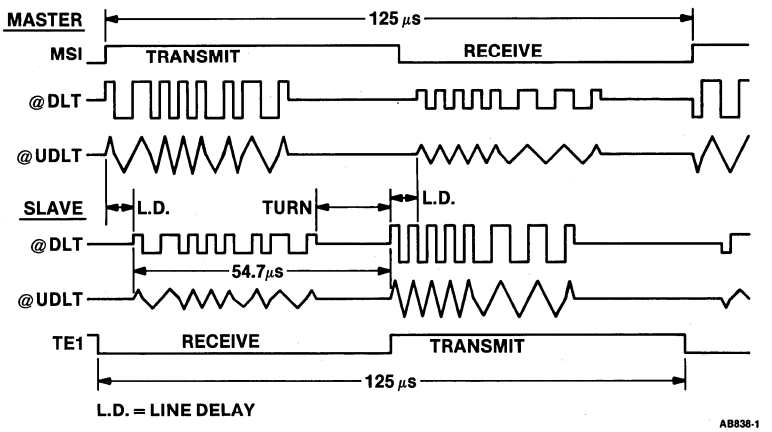


Figure 3

power supplies, 6 to 13 volt single supplies— or the equivalent in a split supply. In addition, by giving the V_{LS} pin the appropriate voltage level, the monocircuits' inputs and outputs will interface to other chips with either CMOS or TTL signal levels.

Although the monocircuits are available today in production quantities, an enhanced version of the existing monocircuit family is now being introduced. It features a typical idle channel noise of 9 dBrnco and a typical Power Supply Rejection Ratio (PSRR) of 55 dB over a 0-50 kHz range.

The Switching Power Supply Controller

A major consideration in designing a voice/data PBX is power. Providing power to digital phones, which may be on a two kilometer loop, is not a trivial task. The typical number of phones powered by a PBX alone means that the power supply in the PBX is a very significant design consideration. Also, because digital telephones require more power than analog phones, the maximum power available at the end of a two kilometer, 26 awg loop is not much more than the power required to operate a voice/data digital phone. Therefore, the efficiency of the power conversion method in the phone is critical—hence the importance of the efficiencies gained by using a switching power regulator.

Motorola's new switching power regulator, the MC34129, is especially designed to fulfill a digital telephone's power regulation requirements, although the regulator is popular for non-telecom applications as well. One of the most important features of this regulator is that it gives the designer the ability to synchronize his switching power supply to the sampling rate of the codec/filter in the phone. This is important because non-synchronized switching noise on the power supply of a codec can make meeting codec/filter idle channel noise specifications difficult. However, synchronized switching noise does not degrade a codec/filter's system performance.

A switching power regulator also offers another important feature for voice/data phones—line isolation. When driving the RS-232 input of a terminal with a local ground reference, isolation between the terminal's ground and the ground of the telephone line is necessary. This regulator can operate in an isolated or a non-isolated mode. The isolated mode simply requires an auxiliary winding on the transformer to supply power and a feedback signal. Otherwise, the chip is applied the same to isolated and non-isolated applications.

The Data Set Interface

The Data Set Interface (DSI), MC145428, is an asynchronous to synchronous converter. It takes data in a start/stop format of various speeds, and puts it into a new format. This new format has no stop or start bits and can be clocked out of the DSI using the input enable and data clocks of a synchronous data transmitter— such as the UDLT.

The chip has an on-board baud rate generator. By feeding a 4.096 MHz clock to the DSI, it will generate a 16x clock to sample the incoming asynchronous data. The data rates that can be programmed are 300, 1200, 2400, 4800, 9600, 19.2 k, and 38.4 k baud. Other asynchronous data rates may be fed to the DSI by supplying an (async data rate) × 16 clock.

In order to maintain synchronization when input data is unable to fill the output channel, the DSI will supplement its output channel with flag patterns. On the receiving side of the data transmission, another DSI will return the data to its original start/stop format.

The RS-232-C Driver/Receiver

The MC145406 has three drivers and three receivers on one CMOS integrated circuit. This device meets all of the EIA RS-232-C specifications. In general, it replaces the 1488/1489. The chip consumes less than 15 mW, which is critical when designing a line-powered digital telephone. A slew-rate limiting circuit is integrated into the chip, which removes the need for external slew-rate limiting capacitors.

SYSTEM II: VOICE/DATA WITH 2B + 2D DATA RATES

Figure 4 shows a more sophisticated terminal. This terminal supports full ISDN 2B + D data rates, as well as an additional D channel. In this case all of the signalling is handled by a microprocessor. One 64 kbps B channel can be used to transmit voice, while the other B channel can be used for transmitting high speed data. In addition, one 16 kbps D channel can be used for transmitting signalling information, while the other one can be used to transmit more specialized functions or additional data.

2B + 2D VOICE/DATA TERMINAL

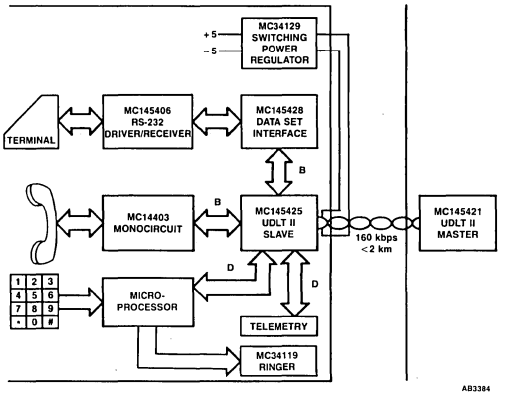


Figure 4

The interface between the data source and the ISDN UDLT, MC145421/MC145425, can be one of various types of data formatters. It could be a DSI handling up to 38.4 kbps, using the internal clock or a faster rate with an external clock. Data could also enter the ISDN UDLT II through an HDLC controller chip, or a clear channel configuration could be used.

This chip will transmit on two wires up to 2 kilometers, with the addition of a passive filter to compensate for the increased attenuation of the higher frequency spectrum.

The ISDN UDLT II—2B + 2D

The ISDN UDLT II, MC145421/MC145425, is very similar to the UDLT. However, instead of 80 kbps, the ISDN UDLT II sends 160 kbps. Also, a 512 kHz burst rate is used, instead of a 256 kHz rate. The data is formatted into four channels: two 64 kbps and two 16 kbps. Both of the 64 kbps channels are clocked out of the Tx pin under the direction of the TDC/RDC, TE1, and TE2 pins. Both of the 64 kbps channels are clocked into the Rx pin, and similarly their input is separately controlled by the RE1 and RE2 pins. The 16 kbps channels are input on the D1I and the D2I pins under control of the DCLK, and they are output on the D1O and D2O pins. Although the ISDN UDLT II does not transmit triangular bursts like the UDLT does, it will drive a twisted pair without external drivers. It also contains the on-board threshold-adjust circuitry. The ISDN UDLT II is being introduced today.

SYSTEM III: ISDN TERMINAL WITH LAP-D

The terminal in Figure 5 uses the "S/T" transceiver, MC145474, for data communication. This four wire transceiver can transmit 192 kbps up to 1 km on one pair of wires, and receives 192 kbps on an additional pair of wires. Besides having a four wire interface, the "S/T" transceiver's transmission method differs from the UDLT's in that alternate mark inversion (AMI) is used instead of MDPSK.

Of the 192 kbps, 144 kbps are used for the two B channels and one D channel. The additional 48 kbps provide framing, DC balance, D channel echoing, activation, and two other bits whose function will be defined in future definitions. Through the transceiver, a codec/filter

2B + D VOICE/DATA TERMINAL

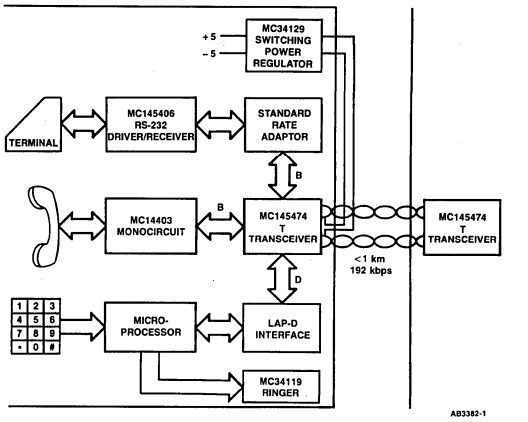


Figure 5

sends digitized voice; signalling information is sent through a LAP-D controller, packetized data can also be sent through the LAP-D controller, and high speed data can be sent through the other 64 kbps B channel. Although the chip offers point-to-point communication, the S/T transceiver is also capable of point-to-multipoint operation—if shorter loop lengths (150 m to 500 m) are acceptable.

CONCLUSION

Motorola's wide variety of integrated circuits offer flexibility to the design engineer. If low-cost voice/data communication is the top priority, the UDLT/DSI system provides a lot of functionality for a minimal cost. If higher data rates are needed, the ISDN UDLT is a solution to consider. And of course, Motorola plans to introduce an S/T transceiver chip and a LAP-D controller chip to provide the extensive features ISDN has to offer.

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN933
Application Note

A VARIETY OF USES FOR THE MC34012 AND MC34017 TONE RINGERS

Prepared by
Dennis Morgan

INTRODUCTION

The MC34012 and MC34017 electronic tone ringers were developed to replace the bulky electromechanical bell assembly of a telephone, while providing the same basic function. When used in conjunction with a piezo ceramic transducer, these circuits will output a warbling sound in response to the applied ringing voltage. With some imagination, however, the circuits can be used in a variety of ways, including non-telephone applications, — wherever an alerting sound or indication is required. Applications include appliance buzzers, burglar alarms, safety alerting functions, special sound effects, visual ringing indicators, and others. The circuits in this application note show how a variety of effects can be obtained.

HOW THE MC34012 WORKS

A block diagram is shown in Figure 1. An AC voltage is applied to the input terminals, and the current is rectified by the full wave bridge. The six series diodes provide the high impedance required by telephone systems at low input voltages, and are therefore not significant where the use does not involve a telephone. A small portion of the I_S current (I_a) flows through D_a and R_a setting the inverting input of the comparator at 1.5 volts below R_S (pin 6). The majority of the input current, however, flows through R3, and the waveform across it is filtered by C3 and the internal 50 k resistor before being applied to the non-inverting input of the comparator. When the input voltage is increased sufficiently so that the current through R3 causes the voltage at the non-inverting input to be more than 1.5 volts below R_S, the comparator's output changes to a low state, allowing the oscillator's signal to reach the piezo transducer. Additionally the value of I_a is reduced by 20% in order to provide hysteresis to the comparator.

The 22 volts zener diode provides regulation for the internal circuitry, and C4 filters noise and ripple from this voltage. The input current must be at least 0.5 mA for the regulation and bias circuits to function properly.

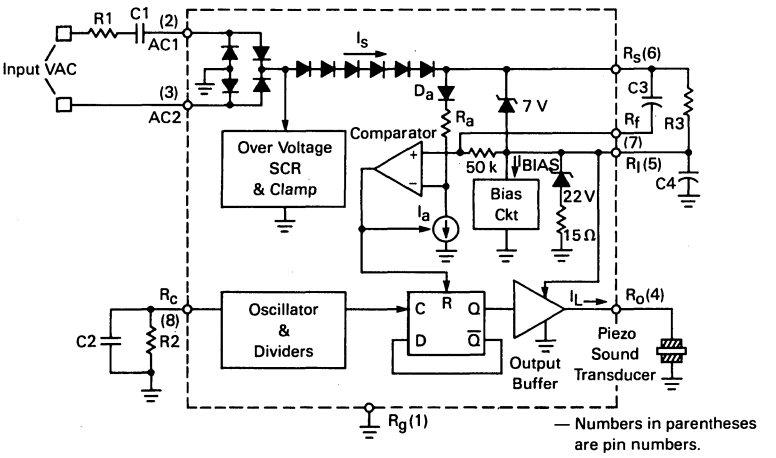


FIGURE 1 — MC34012 Block Diagram

The oscillator is a relaxation type, with the frequency determined by the values of R2 and C2. The base frequency (f = (0.671/R2C2) + 200 Hz) is divided down to produce two output frequencies (f/4 and f/5) which are outputted alternately at a warble rate determined by the base frequency, and the specific tone ringer model used. The MC34012-1 produces a warble rate of f/320, the MC34012-2 produces a warble rate of f/640, and the MC34012-3 produces a warble rate of f/160. The base frequency (f) should be selected to be between 1500 Hz and 10 kHz.

The output buffer is a totem-pole configuration with a 25 mA source-sink capability, and is intended to drive a piezo ceramic transducer. The output waveform is a 20 V p-p square wave.

HOW THE MC34017 WORKS

A block diagram is shown in Figure 2. The external components are labeled the same as in Figure 1. Operation is very similar to the MC34012 with the following differences:

a) The output to the piezo transducer is a push-pull configuration, rather than single ended, providing 40 Volts p-p.

b) The comparator's inputs are referenced to ground rather than to the supply voltage. V_r is 1.2 volts when the comparator's output is off (low), and 0.9 volts when the output is on.

c) The configuration consisting of the comparator, R3, and C3 sense the incoming current to determine the turn-on and turn-off trip points. When the voltage at R_S exceeds 1.2 volts, the comparator changes state to turn on the output.

SAMPLE CIRCUITS

The circuits of Figures 3 & 4 provide ON-DELAY, i.e., after applying voltage to the input terminals, sound is not produced until a delay period has elapsed. The output sound is continuous after that. The delay is primarily determined by C3 in the Figures, although R3 and R1 also affect the timing. The circuit may be controlled by turning on and off the voltage to the input terminals, or by leaving the input voltage applied continuously, and using a normally closed switch across C3 (open switch to start timing). Power consumption is typically less than 3/4 watt. Applications include time out circits for burglar alarms, dark room equipment, and others.

The circuits of Figures 5 and 6 provide OFF-DELAY, i.e., sound is produced immediately upon applying an input voltage, but then turns itself off after a delay. The delay time is determined by C_t. The circuits (as shown) have a long reset time (time for C_t to discharge after removing the input voltage) and so the user may want to consider providing a quick discharge path for C_t whenever the input voltage is removed (such as an extra set of contacts on the on-off switch). The particular application will determine the need for this. Applications include warning buzzers in washing machines, microwave ovens, alarm clocks, and other appliances.

The circuits of Figures 7 and 8 cause the sound output to be cycled on and off at a rate determined by C_t. The duty cycle can be varied by changing R_d. The LM393A dual comparator (configured as an oscillator) needs only 1 mA of power supply current, and so it is powered directly from the tone ringer's R_I pin. Several cycle times are listed in the Figures, and can be used to indicate different conditions, such as "WARNING" (slow cycle), and "EMERGENCY" (fast cycle). Applications include appliances, alarm clocks, emergency indicators on hot water heaters (overtemperature) and furnaces, smoke detectors, and any place where an attention getting sound is required.

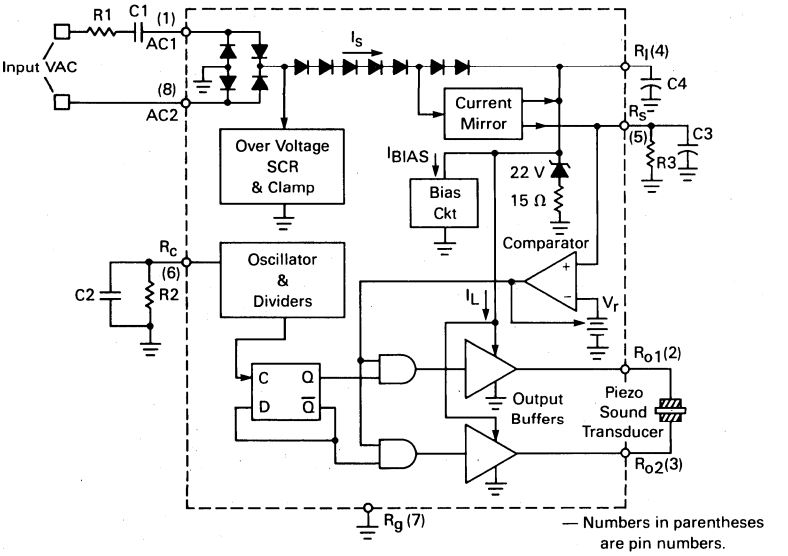
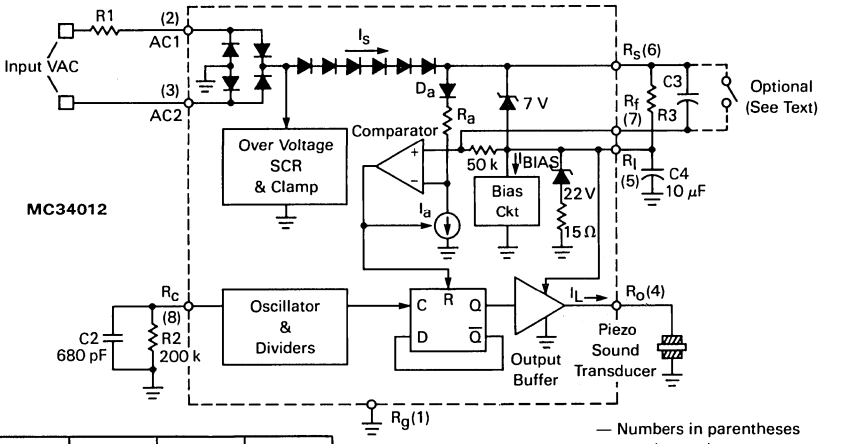


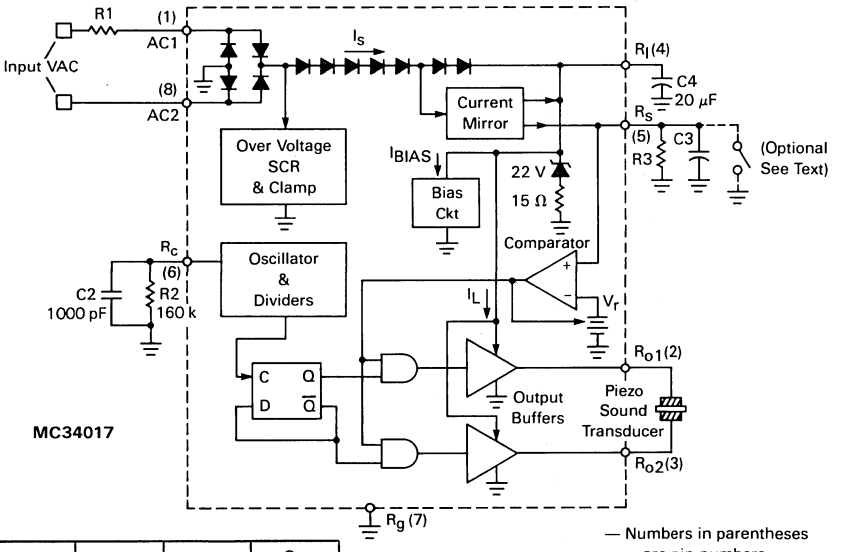
FIGURE 2 — MC34017 Block Diagram



— Numbers in parentheses are pin numbers.

Input VAC	R1	R3	C3	On Delay
24	100	1600	100 μF	30 Sec
120	16 k	750	1000 μF	30 Sec
120	16 k	750	100 μF	10 Sec

FIGURE 3 — On Delay Timer Using MC34012



— Numbers in parentheses are pin numbers.

Input VAC	R1	R3	C3	On Delay
24	1.0 k	15 k	500 μF	15 Sec
24	1.0 k	15 k	2200 μF	75 Sec
120	33 k	15 k	500 μF	8 Sec
120	33 k	15 k	2200 μF	40 Sec

FIGURE 4 — On Delay Timer Using MC34017

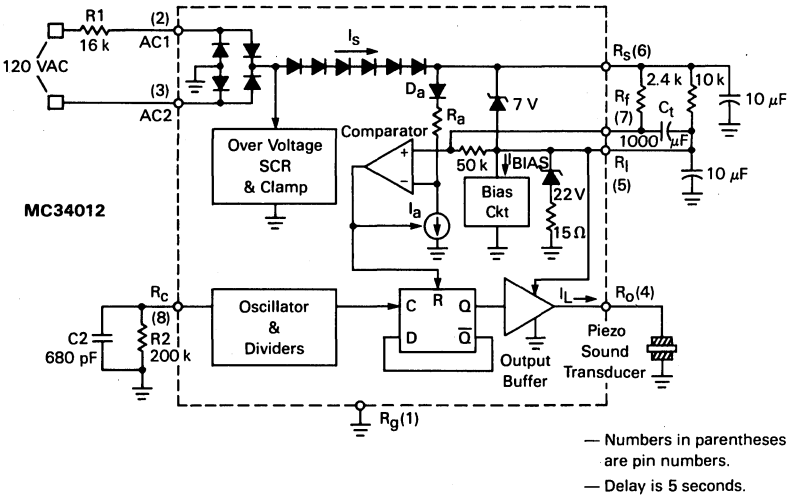
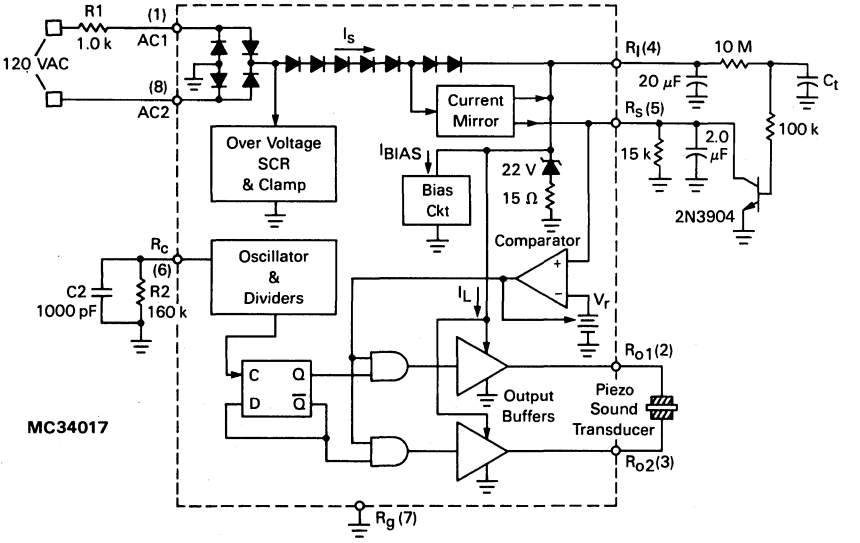
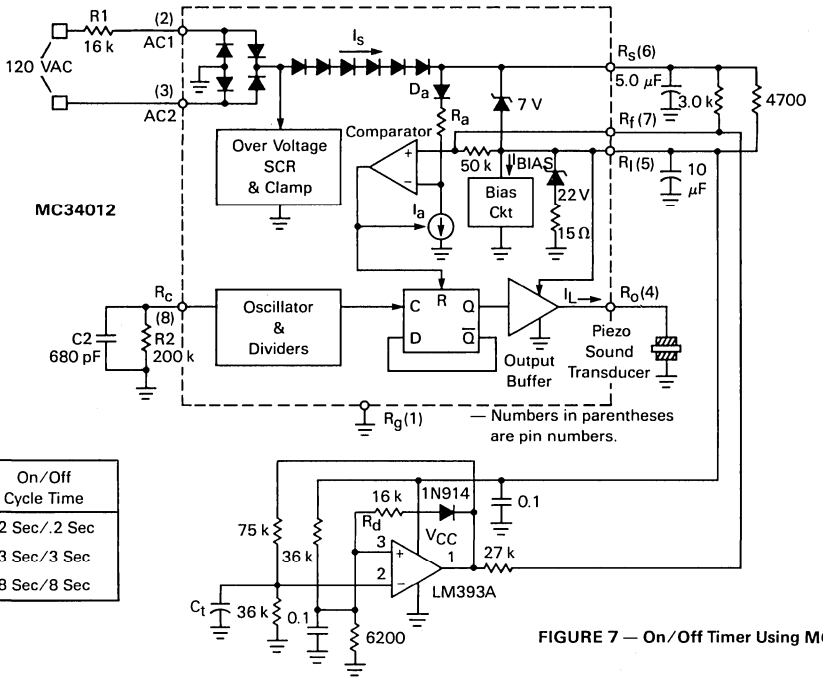


FIGURE 5 — Off Delay Timer Using MC34012



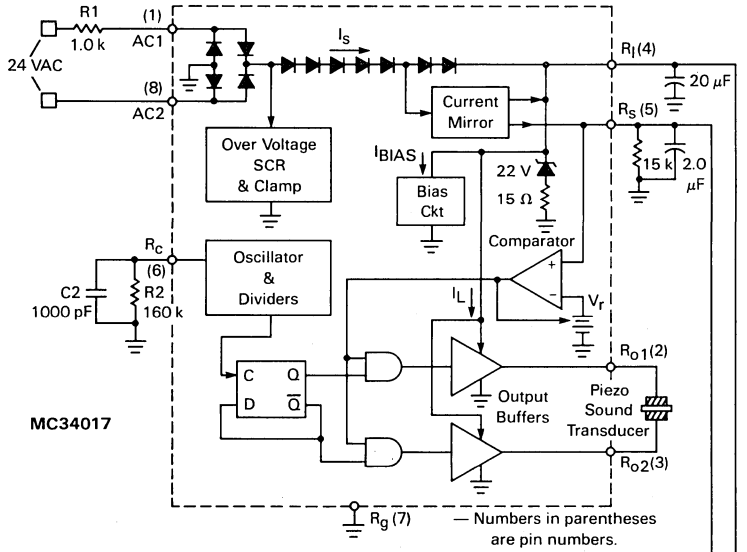
C_t	Off Delay
20 µF	17 Sec
10 µF	7 Sec
5.0 µF	4 Sec

FIGURE 6 — Off Delay Timer Using MC34017



C_t	On/Off Cycle Time
100 μF	.2 Sec/.2 Sec
500 μF	3 Sec/3 Sec
1000 μF	8 Sec/8 Sec

FIGURE 7 — On/Off Timer Using MC34012



C_t	On/Off Cycle Time
2.0 μF	.2 Sec/.2 Sec
20 μF	1.5 Sec/1.5 Sec
100 μF	2.5 Sec/5 Sec

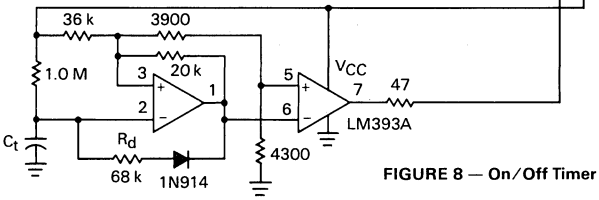


FIGURE 8 — On/Off Timer Using MC34017

The circuits of Figures 9 and 10 provide a special effects sound by varying the frequency of the base oscillator. The 2N3904 transistor is slowly turned on (as C_S charges up) thus varying the equivalent resistance at the R_C pin. This causes the frequency of the base oscillator to vary from low to high over a period of several seconds. C_S determines the rate at which the audio frequency is swept, and C_t determines how often the sweep cycle is repeated. The sound effects produced by this circuit are similar to those heard in many video games (home and arcade type), and in children's games and toys with sound effects. The two sweep circuits are different as they produce different effects. The circuit of Figure 9 uses feedback (via the 51 k resistor and the two portions of C_S) to generate a different linearity sweep curve than the simpler circuit of Figure 10. Either circuit can be used with the MC34012 or the MC34017 by making appropriate connections at R_I and R_C.

The circuits of Figure 11 & 12 are Ring Detector Circuits. Designed for use on the telephone line, they provide an output voltage level to indicate the presence of a ringing signal. (The 1.0 μF capacitor at terminal AC1 is necessary to meet FCC impedance requirements.) The output, at V_{out}, is high (+12 V) as long as an AC voltage is present on the Tip and Ring terminals. The optocoupler provides isolation from the circuit to be controlled, since telephone lines cannot be referenced to earth ground. The 1.0 k and 100 k resistors, and the 0.1 μF capacitor, filter the square wave output of the integrated circuit to provide a steady voltage at V_{out}. The output can be used to turn on a light, activate an answering machine, alert a computer that data is to be sent to it, and for many other uses. The circuit shown is not limited to telephones, however. By changing the value of R1 to 15 kohms for 120 VAC, or to 100 ohms for 24 VAC and deleting the 1.0 μF capacitor (as in the previous examples), the output will indicate the presence of an input voltage while providing isolation. Isolation can be used to prevent unwanted ground loops, or for safety reasons such as to meet UL requirements (the 4N25A and 4N35 optocouplers are UL listed).

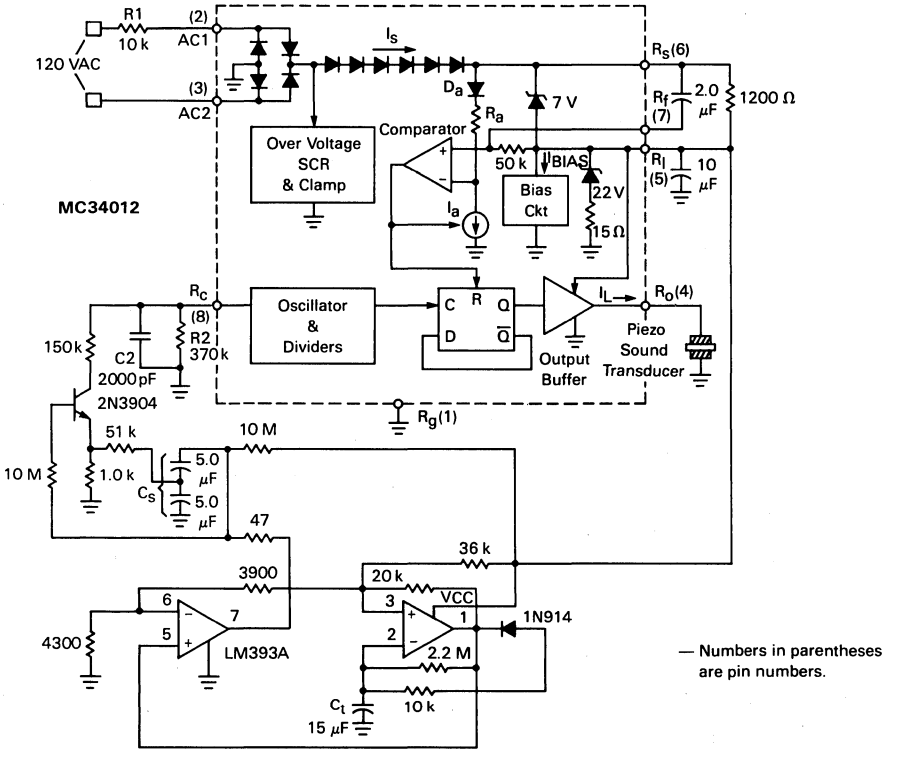


FIGURE 9 — Audio Frequency Sweeper Using MC34012

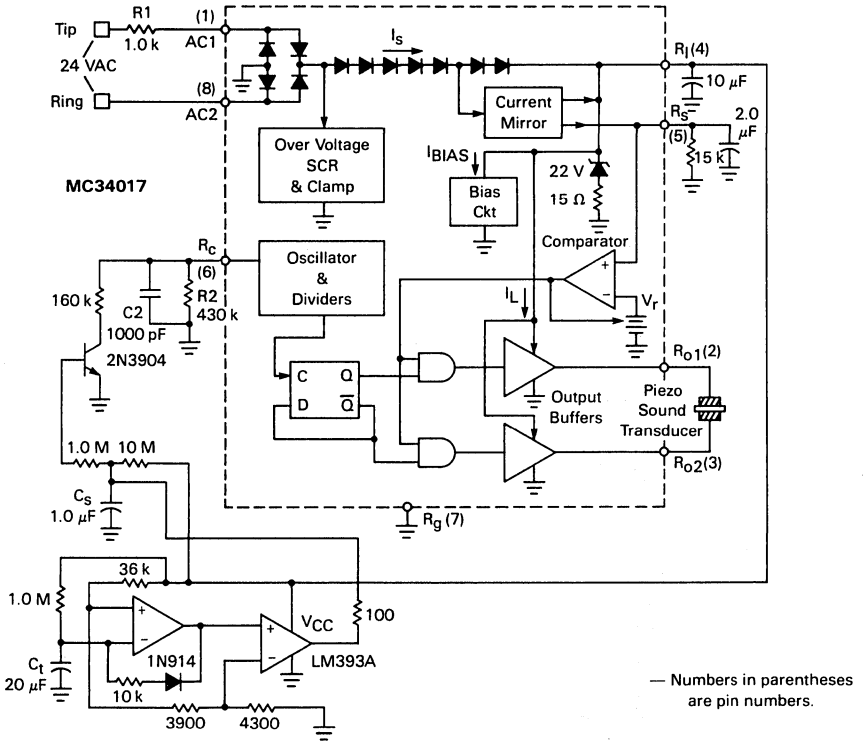
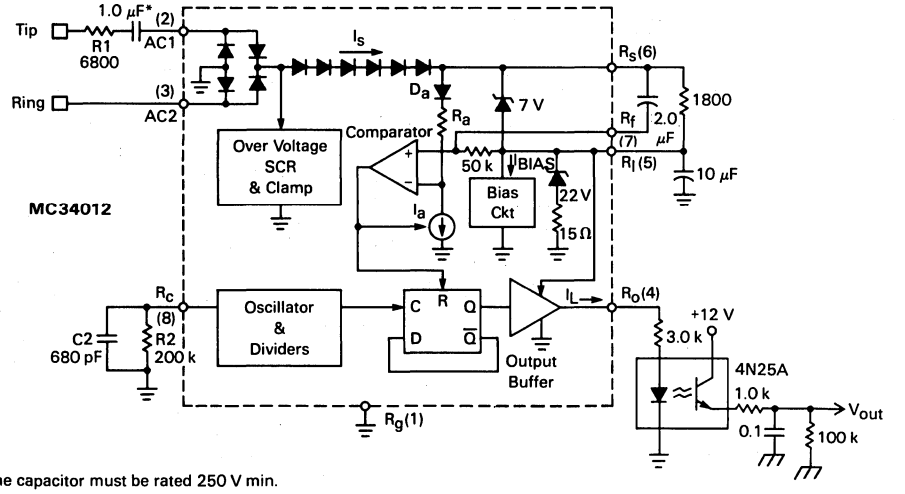


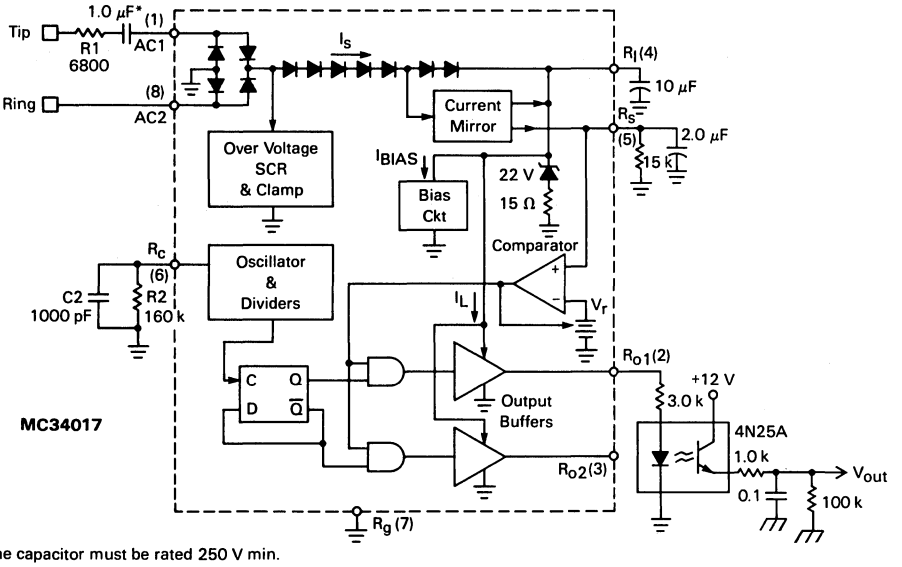
FIGURE 10 — Audio Frequency Sweeper Using MC34017



*The capacitor must be rated 250 V min. and be non-polarized. It is necessary to meet FCC requirements.

— Numbers in parentheses are pin numbers.

FIGURE 11 — Ring Detector Circuit Using MC34012



*The capacitor must be rated 250 V min. and be non-polarized. It is necessary to meet FCC requirements.

— Numbers in parentheses are pin numbers.

FIGURE 12 — Ring Detector Circuit Using MC34017

The circuit of Figure 13 will count the number of times the ringing voltage is sent to the telephone, and will not allow the piezo transducer to sound until a certain number of ring cycles (selected by S1) have passed. The circuit values are based on a typical ringing cadence of 2 seconds on, 4 seconds off. The outputs of the MC14017 counter (Q1-Q9) become active sequentially with each cycle of the ringing signal. When the selected output becomes active, the MC14013 flip-flop changes state, and the piezo transducer sounds. The Q output of the MC14013 can be used to activate other circuitry such as an answering machine. After the ringing signal stops due to answering the phone, or the caller hangs up, the counters and the flip-flop are reset. Note the two separate grounds - the telephone line must be kept separate from the circuit ground.

As a final note, many applications will be enhanced by the addition of a volume control. Simply connect a 10 k potentiometer in series with the piezo sound transducer. The sound output level will then be controllable over a substantial range. Additionally, if the particular transducer being used has a high frequency shrill in its sound, the series resistance can remove the high frequencies, and produce a more pleasant sound.

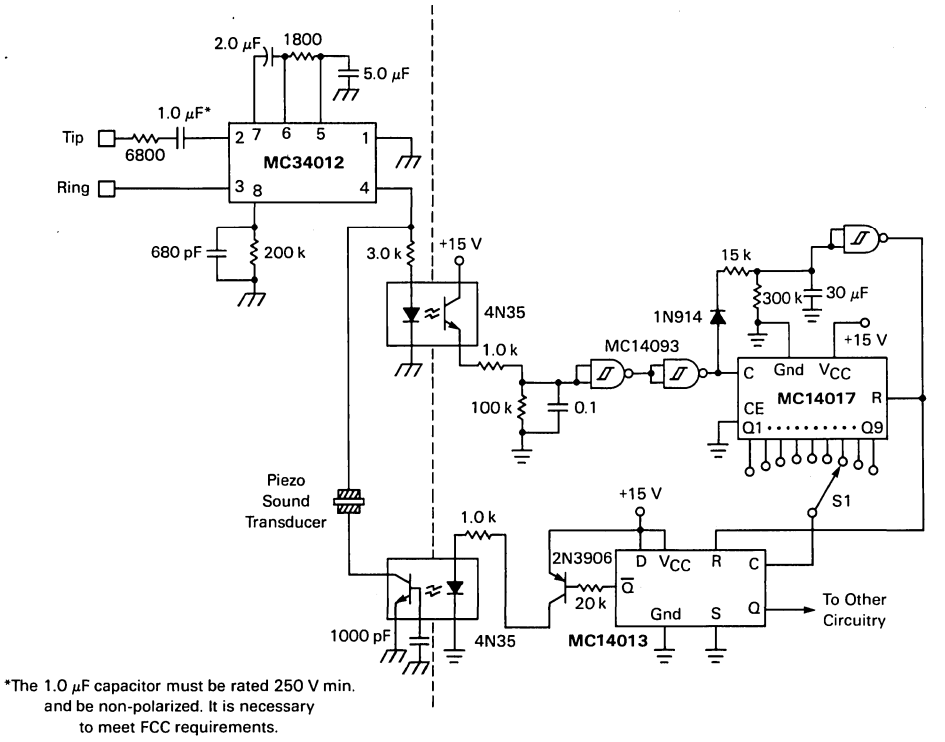


FIGURE 13 — Ring Signal Counter

A TELEPHONE RINGER WHICH COMPLIES WITH FCC AND EIA IMPEDANCE STANDARDS

Prepared by
Dennis Morgan

INTRODUCTION

The MC34012 and MC34017 Tone Ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and the EIA, simply stated, are that a ringer circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing signals, noise) are on the line. This application note discusses how the IC's operate, the specific operational requirements to be met, and how they are met. Only "on-hook" requirements are discussed since off-hook operation is not applicable.

ON HOOK IMPEDANCE REQUIREMENTS

The FCC Rules & Regulations, Part 68, define the on-hook impedance (while ringing) requirements, as well as the ringing voltages and frequencies. EIA Standard RS-470 expands upon the requirements to include minimum impedance during the non-ringing (quiescent) state. The FCC requirements were promulgated so that any newly designed equipment, meant for connection to the Tip and Ring lines, be compatible with the already existing Bell Telephone network and central office equipment. The measured impedance, in all cases, is defined as the quotient of the applied rms ac voltage divided by the true rms measured current.

For the quiescent state, EIA Standard RS-470 provides the minimum impedance requirements at low voltages (<10 V_{rms}) in the 5-3200 Hz range to provide for the loading presented by an on-hook extension phone's ringer circuit to the dialing and speech signals coming from a parallel off-hook phone. Table 1 and Figures 1 & 2 indicate the minimum values. The dc resistance limits of Table 1 keep the telephone from consuming significant power when idle since most phones are on-hook the majority of the time. The lower frequency range of the ac resistance limits includes all of the standard ringing frequencies, and so has a higher applied voltage limit than the upper frequency range, which covers the speech and DTMF signals.

In the ringing state, the limitations for ringer impedance are based on the REN (Ringer Equivalence Number), which is an indication of the power consumed by the ringer circuit during ringing. The FCC regulations state that the total REN for any individual telephone line cannot exceed 5.0, where the total REN is the sum of the REN of each device connected to the line (answering machine, protection devices, as well as each telephone). The specific impedance values listed in the FCC Regulations (Section 68.312, paragraphs b & c, and Table 1) correspond to a REN of 5.0, and are therefore the minimum allowable system impedances. EIA Standard RS-470 provides the same information for the on-hook dc and ac resistance (while ringing), except that the listed values differ by a factor of 5 from those listed in the FCC Rules. The EIA information is, therefore, not a set of limits, but rather a definition of a 1.0 REN. (Originally the 1.0 REN was defined as the load presented by the electromechanical type ringer of a standard Bell Telephone Co. 2500 series telephone.)

TABLE 1

QUIESCENT STATE LIMITS
DC RESISTANCE (between Tip and Ring)
>50 Mohms for 0 - 100 VDC
>150 kohms for 100-200 VDC
AC RESISTANCE (between Tip and Ring)
For 5 Hz<f<200 Hz, 1-10 V_{rms}, see Figure 1
For 200 Hz<f<3200 Hz, 0-3 V_{rms}, see Figure 2
At 24 Hz, Z at 2.5 V_{rms} > 4 x Z at 10 V_{rms}

The specifications of Table 2 includes not only the ringing impedance guidelines of RS-470, but also the voltages and frequencies at which the ringer circuit MUST ring. When testing a circuit to the conditions of Table 2, the minimum measured impedance within each voltage and frequency range is divided into the impedance listed for that range. The largest number obtained over the full set of ranges for a ringing type is the REN for that circuit. In addition to the specifications of Table 2, RS-470 and the FCC Rules require that the ac ringing impedance of an individual device be less than 40 kohms, unless that requirement is already provided for by some other parallel device.

In addition to the above ac specifications, the dc requirements impose an upper limit of 0.6 dc mA when any of the Table 2 ringing signals are applied.

(NOTE: The type A ringers mentioned in Table 2 refer to the inherently frequency selective electro-mechanical type ringers used for decades in the typical single-line (non-party line) telephone. Type B ringer specifications cover a wider frequency range, and were developed with the advent of electronic ringers which are generally not frequency selective. Ringer types C through Q, listed in the FCC and EIA specifications, are selective to specific frequency ranges for the purpose of party line applications, and are not discussed here.)

TABLE 2

RINGING CHARACTERISTICS

Ringing Type	Frequency (Hz)	Voltage (V_{rms})	Bias (Vdc)	Impedance (kohms)
A	17	40-130	0-105	7
A, B	17	55	0-105	10
A	20	40-130	0-105	7
A	20	40	0-105	8
A	23	40-130	0-105	6
A	27-33	40-130	0-52.5	5
B	15.3-68	40-150	0-105	8

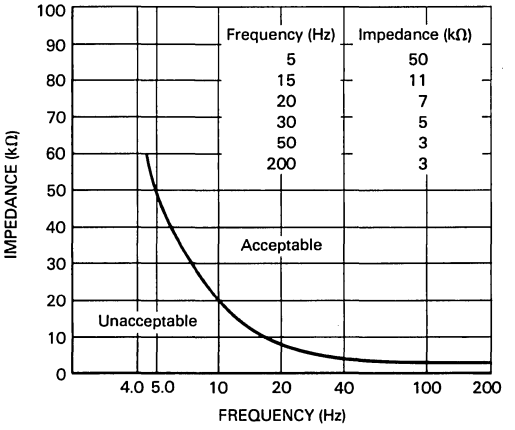


FIGURE 1 — Quiescent State Minimum Impedance (1-10 V_{rms}) (EIA Standard RS-470)

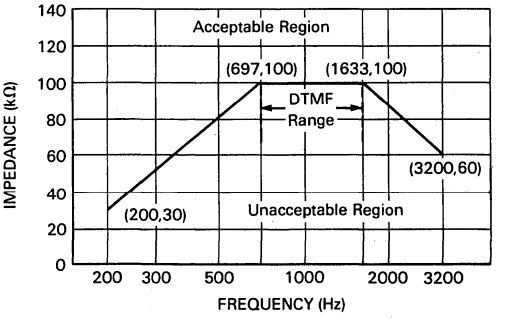


FIGURE 2 — Quiescent State Minimum Impedance (0-3 V_{rms}) (EIA Standard RS-470)

CIRCUIT DESCRIPTION - MC34012

A block diagram is shown in Figure 3 (R1-R3, C1-C4, and the piezo transducer are external). A ringing signal (From Table 2) is applied to the Tip and Ring terminals, and the current is rectifed by the full wave bridge. The string of six diodes following the bridge provide the high impedance required at low voltage (non-ringing) levels (see Figures 1 & 2). When the voltage across AC1-AC2 exceeds approximately 5.6 volts (8 diode drops) current will flow (several microamps), primarily through R3 and into the Bias Circuit block (I_a is relatively small). As the current reaches approximately 0.5 mA, the internal biasing becomes well established, and so further increases in voltage result in little increase in current. When the voltage at pin R_I reaches 22 volts, the zener diode conducts and the current increases rapidly with voltage.

The two inputs of the comparator are referenced to pin R_S (the output of the diodes), rather than to ground. The inverting input is kept at 1.5 volts below R_S by I_a, R_a, and D_a. The voltage at the non-inverting input depends on the current through R3. When the voltage at this input is more than 1.5 volts below R_S the output of the comparator changes state, allowing the oscillator's signals to reach the piezo transducer. On-Off hysteresis of the comparator is provided for in two ways: 1) the comparator's output (when low) reduces the value of I_a, thus reducing the voltage across D_a and R_a to 1.2 volts; and 2) The load current (I_L) passes through R3, increasing the voltage across it. When the current through R3 is reduced sufficiently to turn off the comparator, I_a is returned to the higher value, and the flip-flop is reset, turning off the output.

Capacitor C3 filters the waveform across R3 so that the comparator does not turn on & off with every cycle of the applied ringing signal. In effect, the comparator responds to the AVERAGE voltage across R3. C3 also filters out transient voltages and noise to prevent false ringing. C3 should be large enough (typically 1.0 μF) to reject dialing transients, as well as to ensure the comparator stays on at the lowest ringing voltage and frequency listed in Table 2 (40 V_{rms}, 15.3 Hz). Values larger than 3.0 μF will significantly affect the response time of the circuit.

C4 is a filter for the internal 22 volt supply. With a 5.0 μF capacitor, a ripple of about 3 volts p-p (at 15.3 Hz) results at the R_I pin, which shows up on the output pin. With a 2.0 μF capacitor, the ripple increases to 6 volts p-p, with a slight reduction in output sound level of the piezo transducer, since the output's average value is lowered. Values less than 2.0 μF are not recommended. Neither C3 nor C4 affect the impedance of the overall circuit during ringing.

The values of C3 and R3 determine the turn-on trip point of the circuit, while the turn-off trip point is determined by R3, C3, and the load (piezo transducer) since the load current (I_L) passes through R3. (The line input resistor and capacitor, R1 and C1, also affect the on-off trip points, and will be discussed later). 1800 ohms is the recommended value for R3. A higher value will lower the trip points, but will make the circuit more susceptible to noise. Additionally, if R3 is too large, it is possible the comparator may turn on the output before the internal circuitry is fully biased, resulting in erratic operation. R3 must therefore be selected to pass sufficient current to supply the bias current, AND some

through the 22 volt zener diode, BEFORE the comparator switches the output on. On the other hand, a lower value of R3 will increase the circuit's noise rejection, while raising the on-off trip voltages.

Components R2 and C2 set the base frequency of the oscillator, and have no effect on the on-off trip points, or circuit impedance. Refer to the data sheet for proper component values.

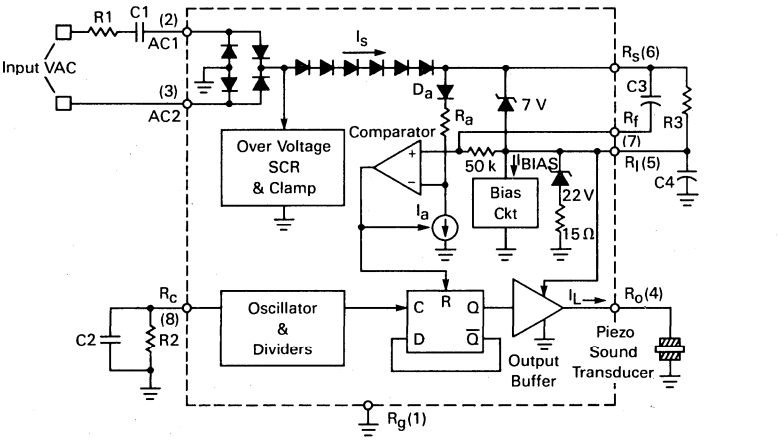


FIGURE 3 — MC34012 Block Diagram

CIRCUIT DESCRIPTION - MC34017

A block diagram is shown in Figure 4. The external components are labeled the same as in Figure 3. The following provides a functional comparison of the MC34017 with that of the MC34012:

- The output to the piezo transducer is a push-pull configuration, rather than single ended, providing 40 volts p-p.
- The comparator's inputs are referenced to ground rather than to the supply voltage. V_r is 1.2 volts when the comparator's output is off (low), and 0.9 volts when the output is on.
- The configuration consisting of the comparator, R3, and C3 sense the incoming current (I_S) to determine the turn-on and turn-off trip points. Since I_S contains the load current (I_L), the same hysteresis effect that exists in the MC34012 is provided for in this circuit.
- Five diodes are shown in series with the input bridge rather than six. The Current Mirror block provides an effective sixth diode, providing the same high impedance at low voltage as provided for by the MC34012.
- Typical values for R3 and C3 are 15 kohms and 2.2 μF, respectively.

MC34012/34017 IMPEDANCE CHARACTERISTICS

The circuit of Figure 5 was used to determine the dc characteristics, and the results are shown in Figure 6. The component values (R2, R3, C2-C4) are typical recommended values, and the 0.047 μF capacitor and 390 ohms resistor simulate a typical piezo transducer. The circuit is obviously very non-linear, resembling, in effect, a 29 volt zener diode in series with a 450 ohm resistor (for $V_{in} > 29$ volts).

QUIESCENT STATE IMPEDANCE

The very high dc impedance requirements, and the fairly high ac impedance requirements (particularly at the lowest frequencies) of Table 1, require the use of a capacitor in series with the input to the I_C. A series resistor is not practical because of the values involved. Figure 7 depicts the circuit configuration. The maximum capacitor value (for C1), which results in the circuit exceeding the EIA requirements, was experimentally determined. Figures 8 & 9 indicate the impedance curves of the resulting circuit. Figure 8 shows the results at 10 V_{rms} only since any lower input voltage results in a higher circuit impedance.

Typically, mylar, polycarbonate, and Teflon capacitors are best suited to meet the dc impedance requirements.

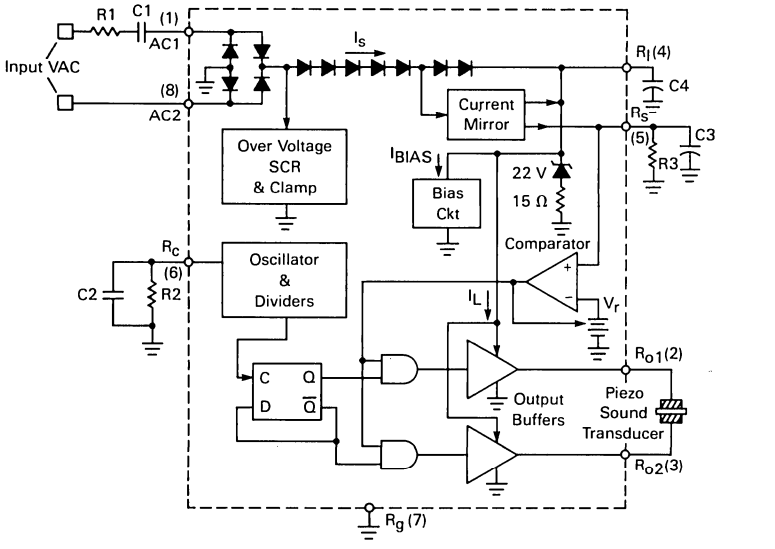


FIGURE 4 — MC34017 Block Diagram

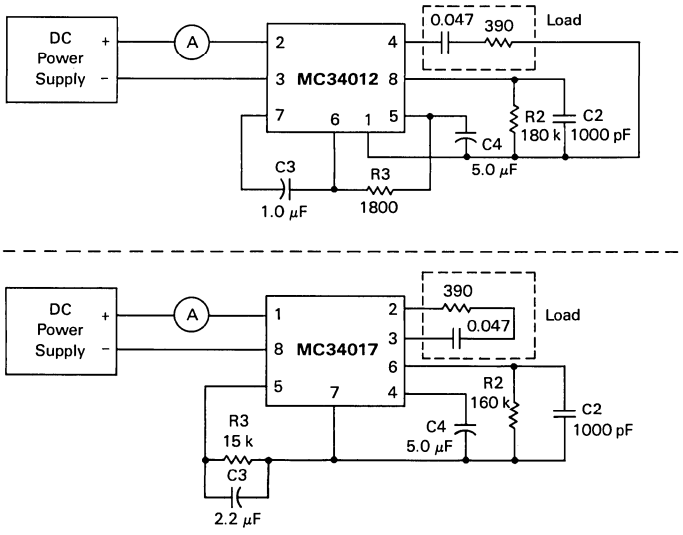


FIGURE 5 — DC Test Circuit

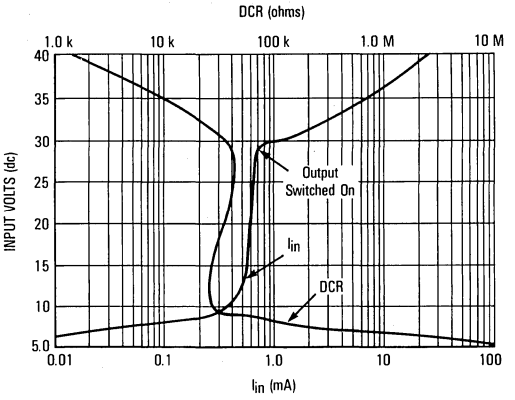


FIGURE 6 — DC Characteristics

RINGING STATE

Considering (temporarily) the impedance values of Table 2 as minimums in order to guarantee a REN of 1.0 or less, reasoning will indicate that the circuit of Figure 7 will not provide the necessary impedance since: 1) the impedance of the ringer I_C drops off quickly at the higher voltages (Figure 6); and 2) the impedance of the capacitor (C1) drops off at the higher frequencies. (The capacitor's impedance can be roughly estimated using $1/2\pi fC$, but this is a VERY rough estimate since the current through the capacitor is anything but sinusodial.) A series resistor (R1) is therefore added (Figure 10) to provide the additional impedance. The limits on the value of R1 are that it must be low enough to allow the circuit to operate (output on) at the lowest voltage AND frequency of Table 2, and yet high enough to provide sufficient impedance at the highest voltage AND frequency. Since an optimum value for R1 is difficult to calculate, different values were tested experimentally with the following results:

1) 7200 ohms is the maximum value which will allow the circuit to turn on at 40 V_{rms}, 15.3 Hz.

2) 7800 ohms is the maximum value which will allow the circuit to turn on at 40 V_{rms}, 17 Hz.

3) 2000 ohms is the minimum value which will result in a REN of 1.0 for a type A ringer.

4) 5500 ohms is the minimum value which will result in a REN of 1.0 for a type B ringer.

5) With R1 chosen within the above mentioned range of values, the highest measured circuit impedance was approximately 23 kohms, well below the maximum allowable of 40 kohms. Choosing a value of 6200 or 6800 ohms (2 watts) for R1 will then result in a circuit which is functional at all of the voltages and frequencies listed in Table 2, but also provides a REN of less than 1.0 for both type A and B ringers.

The allowable values for C1 are fairly narrow. Reducing C1 will increase the circuit impedance and lower the REN, but testing indicated that 0.6 μF is the lowest value which will allow the circuit to turn on at 40 V_{rms} and 17 Hz. It was previously determined (see Figure 8) that C1's value could not be much higher than 1.0 μF and still meet the quiescent state impedance requirements. The voltage rating for C1 must be at least 250 volts, and must be non-polarized.

The load (represented in Figure 10 by the 0.047 μF capacitor and the 390 ohm resistor) affects the overall circuit impedance when ringing since the load current must be supplied on the Tip and Ring lines, and so the actual sound transducer must be installed when making the impedance measurements of a production circuit.

Variations in performance over temperature (-20° C to +60° C) are minor, and generally do not present a problem in most applications. Variations in R1, C1, R3, and C3 will affect input impedance, and the on-off trip points, if they drift with temperature.

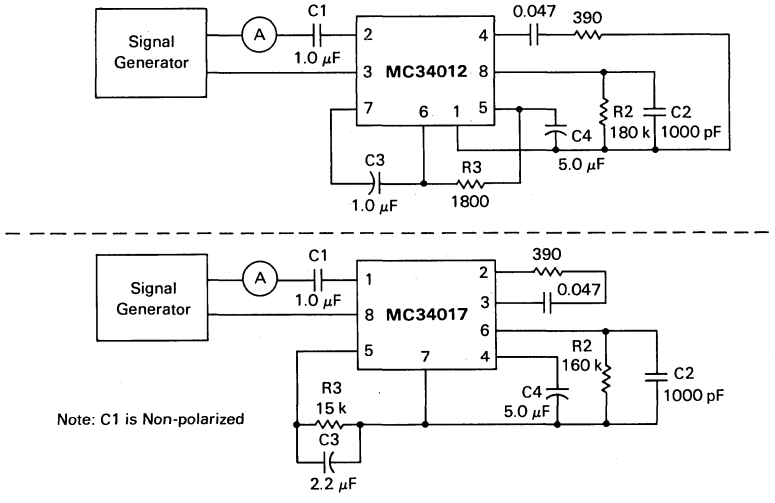


FIGURE 7

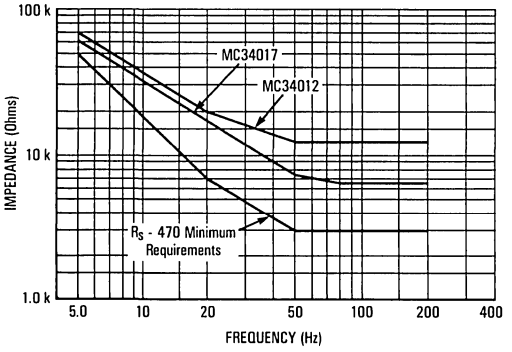


FIGURE 8 — AC Impedance at 10 V_{rms}

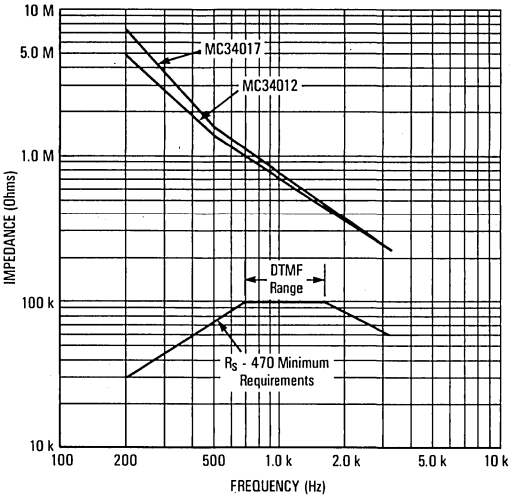


FIGURE 9 — AC Impedance at 3.0 V_{rms}

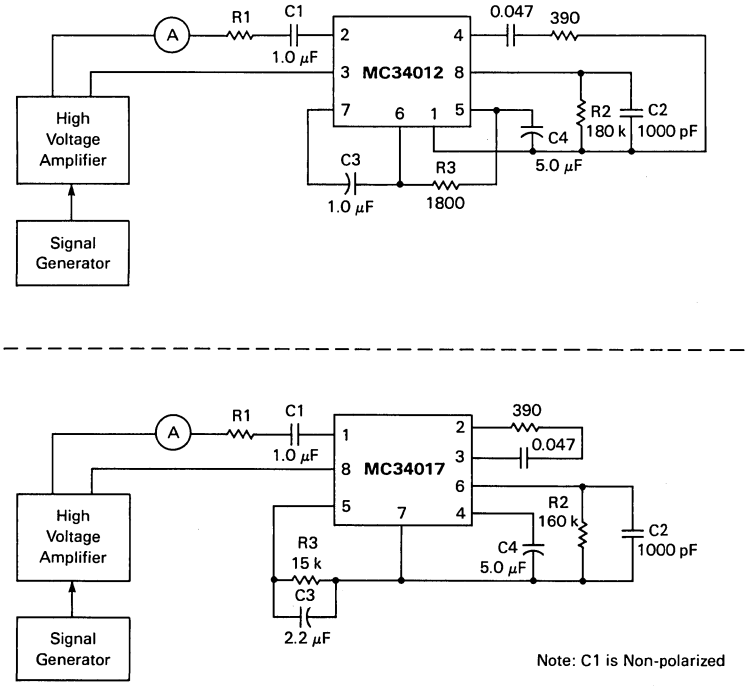


FIGURE 10 — Ringing State Test Circuits

SUMMARY

The MC34012 and MC34017 provide a simple and inexpensive means to construct a telephone ringer which meets the FCC and EIA impedance and operational requirements. The output frequencies to the sound transducer are selectable over a 6.5:1 range, and three different warble rates are available by appropriate suffix choice (-1, -2, or -3). The circuits are designed for use with piezo sound transducers, rather than a bulky speaker/transformer arrangement. Only 3 resistors and 4 capacitors (all standard values) are required to make the circuit operational.

A REN of 1.0 is easily obtained for a type B ringer, as is a REN of 0.5 for a type A ringer.

ACKNOWLEDGEMENT

Figures 1 and 2 were taken from RS Standard 470 with permission of the Electronic Industries Association, 2001 Eye St. NW, Washington, DC 20006. (202-457-4900).

BIBLIOGRAPHY

Electronic Industries Standard RS-470, "Telephone Instruments With Loop Signaling For Voiceband Applications", (Issue 1), January 1981.

Federal Communications Commission Rules and Regulations, Part 68 "Connection of Terminal Equipment to the Telephone Network", October 1982.

MC34012 Data Sheet, Motorola Inc., 1983.

MC34017 Data Sheet, Motorola Inc., 1984.

DEFINITION OF TERMS

RINGER CIRCUIT -
The bell, or other alerting device (circuit) in a telephone.

ON-HOOK -
The circuit condition of a telephone when it is not in use (handset is on-hook).

OFF-HOOK -
The circuit condition of a telephone when it is in use (handset is off-hook).

DTMF -
Dual Tone MultiFrequency - The dialing system where (somewhat musical) tones are produced by a pushbutton telephone.

REN -
Ringer Equivalence Number - see text.

TIP, RING -
The connection points whereby an individual telephone is connected to a switching network. Ring is traditionally negative with respect to Tip.

TURN-ON TRIP POINT -
The voltage (at Tip & Ring) at which the ringer circuit switches on.

TURN-OFF TRIP POINT -
The voltage (at Tip & Ring) at which the ringer circuit switches off.

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN940
Application Note

TELEPHONE DIALING TECHNIQUES USING THE MC6805

Prepared by
Robert Fischer
Downsview, Ontario, Canada

INTRODUCTION

Telephones and associated ancillary equipment providing intelligent features are fast becoming commonplace. Often, it is necessary for the microprocessor providing the intelligence to also dial a telephone number.

The M6805 Family microcomputers (MCU), with their proven hardware/software versatility, are ideal candidates for such applications. Illustrated here are two cost-effective methods of telephone dialing. Hardware and software is given for both Dual Tone Multi-Frequence (DTMF) and rotary-pulse type dialing.

DEMONSTRATION BOARD DESCRIPTION

Figure 1 shows the schematic of the demonstration board designed around a MC68705P3 single-chip MCU. This board is capable of pulse or DTMF dialing. The type of dialing is selected by switch S1. A 12-contact keyboard is used for input. While this is an extravagant use of I/O, it is acceptable for the purposes of a demonstration board.

Pulse dialing requires a direct connection to the telephone line. Interface to the line is made by a 600-ohm, 1:1 line transformer and a relay that provides on/off hook capability. An indicator light (LED #1) shows the current hook status.

After a power-on reset, the board is in an on-hook state (LED #1 off). The pressing of any key will result in an off-hook state without the digit being dialed. Subsequent key presses will result in the dialing of the corresponding digit. Pressing of the cancel button (S2) returns the board to the on-hook state.

The hardware and software to accomplish either form of dialing is readily applicable to any number of the M6805 Family.

ROTARY PULSE DIALING

From both a hardware and software viewpoint, pulse dialing is by far the simplest form of dialing to implement.

Pulse dialing requires that the telephone line circuit receive a make/break sequence at a 10-pulse-per-second (PPS) rate (see Figure 2). The dialing of the digit 3, for example, requires three make/break sequences. The 10-PPS rate requires the use of either a transistor or high speed relay for line looping. Note that if a low current reed relay is used, port B may be capable of driving the relay directly (eliminating the 2N3904 driver).

Subroutine PDIAL provides the proper timing sequences for pulse dialing. The routine is called with the digit to be dialed resident in the accumulator. Because the timing is not particularly critical, interrupts that can be quickly serviced are permissible.

DTMF DIALING

Dual tone multi-frequency tone dialing is considerably more complex in terms of ROM usage and external hardware. The M6805 MCU is required to generate two simultaneous sine waves of different frequencies. Table 1 shows the key pad digit and the frequencies of the corresponding tone pairs. Note that the tones fall into two groups:

Group	Frequency (Hz)
Low Tones	697, 770, 852, 941
High Tones	1209, 1336, 1477, 1633

TABLE 1 — Keypad Digit and Frequencies for Tone Pairs

Keypad Digit	DTONE Entry	Tone Pair (Hz)	
0	$0	941	1336
1	$1	697	1209
2	$2	697	1336
3	$3	697	1477
4	$4	770	1209
5	$5	770	1336
6	$6	770	1477
7	$7	852	1209
8	$8	852	1336
9	$9	852	1477
A	$A	697	1633
B	$B	770	1633
C	$C	852	1633
D	$D	941	1633
*	$E	941	1209
#	$F	941	1477

Also note that if the seldom used keys A, B, C, and D are not required, it is not necessary to generate a 1633-Hz tone.

The method used to generate the tones uses a series of 3-bit look-up tables. Consider a sine wave that has been sampled

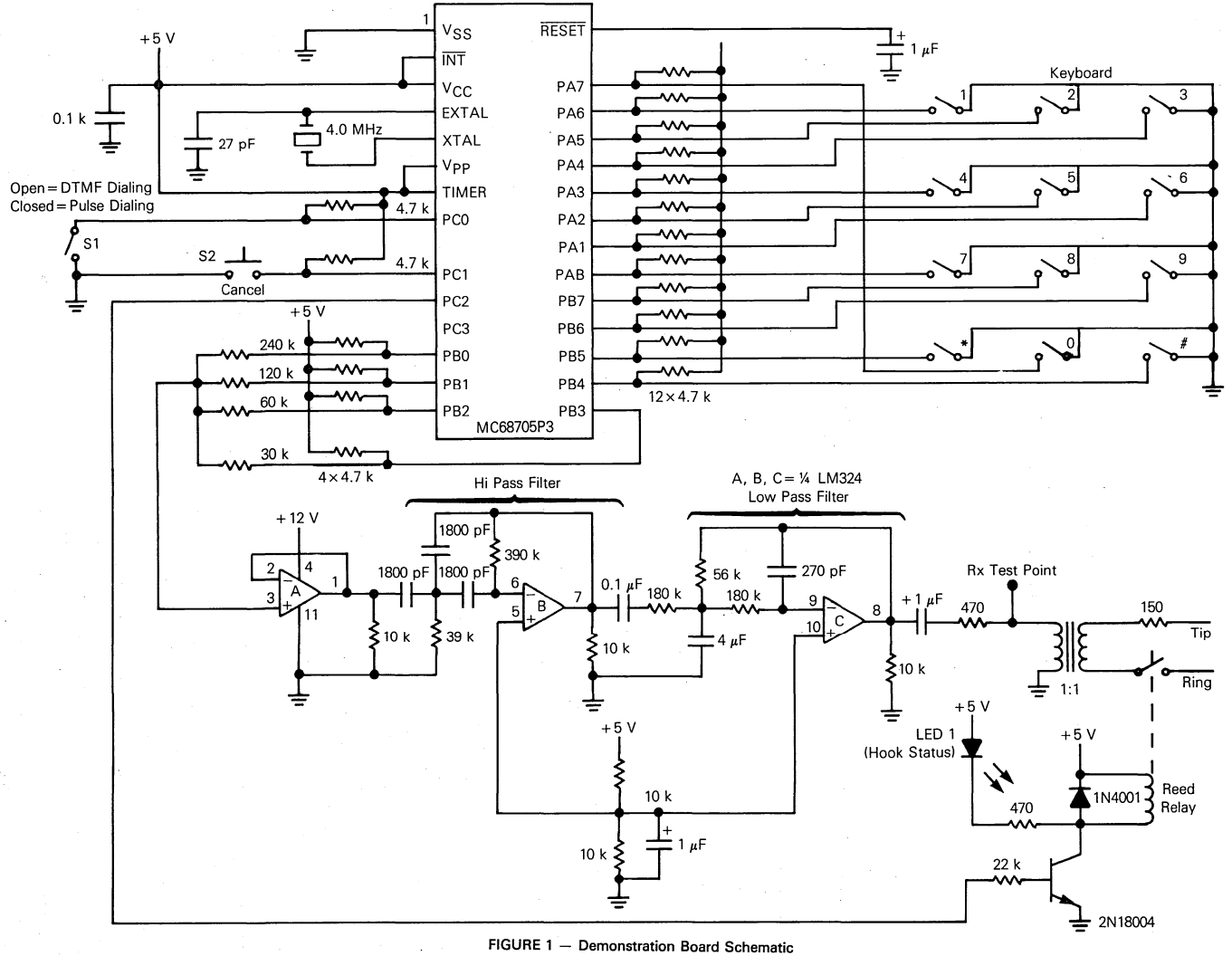


FIGURE 1 — Demonstration Board Schematic

at a constant interval, starting at the positive peak (see Figure 3). Sampling is continued until the next positive peak is encountered. There is, of course, some quantization error associated with this next found peak. If this group of samples were to be continuously cycled, a frequency error would result.

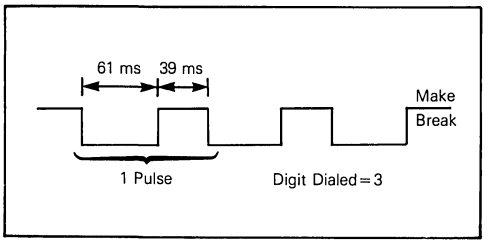


FIGURE 2 — Timing for Rotary Pulse Dialing

To cure this, continue sampling until the next peak is encountered and determine if the resultant frequency error falls within acceptable limits. Figure 3 is actually the output of a program written in BASIC for the EXORciser. This listing is included at the end of this application note. This program is used to design the look-up table for incorporation into the M6805 program according to the error rates acceptable in the end equipment.

This program prompts the user for the sample interval and the frequency of the tone which is to be generated. Sampling of the tone is thus automated and after a peak is encountered, the cumulative frequency error is calculated and displayed along with the sample count. If the user is satisfied with the percentage error, a table of the samples is generated. If the error is still unacceptable, the program continues sampling until the next peak is encountered. Note that the samples have all been "dc shifted".

This program was used to generate the look-up tables for all the tones given in Table 1 with a criteria of 1% maximum frequency error.

The subroutine DTONE actually operates on these tables to generate the DTMF tone pairs. The routine is entered with the DTMF digit (see Table 1) is resident in the accumulator. Note that interrupts cannot be tolerated by this routine.

The first task of this routine is to convert the digit into the table start addresses for the high and low tones. This routine requires that the tables be resident in page 0 ROM to allow use of indexed addressing with 0 offset. The structure chosen for the tables puts the high group tones in the right nibble and the low group tones in the left nibble. Because the tables are all of different lengths, the table end is marked by an entry of $F. In defiance of Murphy's Law, the DTMF tables fit exactly into page 0 ROM.

Generation of the tones involves cycling around a loop which plucks a 3-bit low tone sample and adds it to the 3-bit high tone sample. The 4-bit sum is then output to a D/A converter. If the end of the table marker is encountered for either sample, the pointer must be reset to the table start. This loop also keeps track of the duration of the tone burst by counting loops in TIMEH and TIMEL.

Notice that every program path through the loop takes a constant time (122 microseconds). The actual sequence of program development was to first write the loop, determine the execution time, and then, with the sample interval defined, generate the tone tables.

The 4-bit D/A converter is economically implemented with standard 5% resistors (60 kilohms = 30 kilohms + 30 kilohms). Port B was used because of its slightly superior high output voltage drive. It is still necessary to supplement the high drive with pull-up resistors.

One unfortunate by-product of this tone generation technique is the production of subharmonics (and, of course, harmonics). This necessitates the use of an active bandpass filter. This filter consists of separate high pass and low pass sections. The filter response is shown in Figure 4.

The output level to the telephone line is adjusted with a 470-ohm resistor in series with the line transformer primary. This also provides the RX point, where received audio can be obtained for duplex communication.

Using the BASIC software at the end of this application note, the generation of custom tone groups is readily accomplished. Single tone generation is also possible by using the table entry TNOFF at the end of the given DTMF tables. This allows the muting of either the high or low group tones.

EXORciser is a registered trademark of Motorola Inc.

```
  :
7 :*          **          **          *
6 :          *  *        *  *        *
5 : *           *                    *
4 :        *          *     *
3 :   *          *          *     *
2 :    *   *            *
1 :        *        *  *        *  *
0 :     **          **          **
  ::::::::::::::::::::::::::::::::::::::::::::::::::
                HORIZONTAL = 122.000  uSEC

FREQUENCY    = 697.000  Hz
ERROR        = 0.800  %
NO. SAMPLES = 35.000
NO. CYCLES   = 3.000

SAMPLE 1  = 7        SAMPLE 2  = 5
SAMPLE 3  = 3        SAMPLE 4  = 2
SAMPLE 5  = 0        SAMPLE 6  = 0
SAMPLE 7  = 1        SAMPLE 8  = 2
SAMPLE 9  = 4        SAMPLE 10  = 6
SAMPLE 11  = 7       SAMPLE 12  = 7
SAMPLE 13  = 6       SAMPLE 14  = 5
SAMPLE 15  = 3       SAMPLE 16  = 1
SAMPLE 17  = 0       SAMPLE 18  = 0
SAMPLE 19  = 1       SAMPLE 20  = 2
SAMPLE 21  = 4       SAMPLE 22  = 6
SAMPLE 23  = 7       SAMPLE 24  = 7
SAMPLE 25  = 6       SAMPLE 26  = 4
SAMPLE 27  = 3       SAMPLE 28  = 1
SAMPLE 29  = 0       SAMPLE 30  = 0
SAMPLE 31  = 1       SAMPLE 32  = 3
SAMPLE 33  = 5       SAMPLE 34  = 6
SAMPLE 35  = 7
```

FIGURE 3 — Sine Wave Sampling

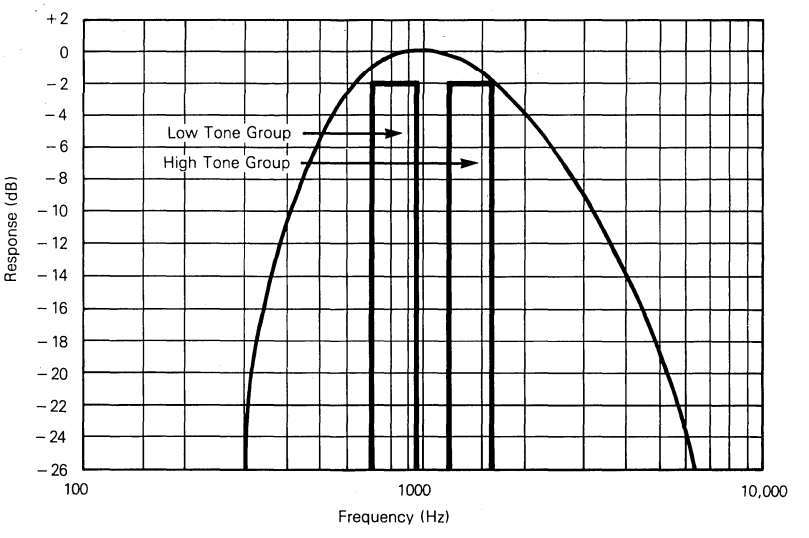


FIGURE 4 — Cumulative High-Pass, Low-Pass, and Line Transformer Response

```
PAGE  001  DEMO    .SA:2  DEMO   - MC68705P3 SOURCE FOR DIALER DEMO

00001                              NAM     DEMO
00002                              TTL     - MC68705P3 SOURCE FOR DIALER DE
00003                              OPT     ABS,CRE


00005                              ********************************************
00006                              *                                          *
00007                              *      DIALER DEMONSTRATION PROGRAM        *
00008                              *           MC68705P3 VERSION              *
00009                              *             ROBERT FISCHER               *
00010                              *  MOTOROLA SEMICONDUCTOR PRODUCTS INC.    *
00011                              *             TORONTO, CANADA              *
00012                              *               11/23/83                   *
00013                              ********************************************


00015                              *
00016                              *   SET MOR
00017                              *
0018A 0784                                 ORG     $784
0019A 0784    5F          A                FCB     %01011111


00021                              *
00022                              *       PORT DEFINITION
00023                              *


00025              0000      A PORTA  EQU     $0          PORT A I/O
00026              0001      A PORTB  EQU     $1          PORT B I/O
00027              0002      A PORTC  EQU     $2          PORT C I/O
00028              0004      A PORTAD EQU     $4          PORT A DDR
00029              0005      A PORTBD EQU     $5          PORT B DDR
00030              0006      A PORTCD EQU     $6          PORT C DDR
00031              0008      A TMRDAT EQU     $8          TIMER DATA REGISTER
00032              0009      A TMRCON EQU     $9          TIMER CONTROL REGISTER


00034                              *
00035                              *       RAM ALLOCATION
00036                              *
0037A 0040                                 ORG     $40
0038A 0040    0001        A TIMEH  RMB     1           TONE TIME (MS)
0039A 0041    0001        A TIMEL  RMB     1           TONE TIME (LS)
0040A 0042    0001        A STARTH RMB     1           HI TONE TABLE START
0041A 0043    0001        A STARTL RMB     1           LO TONE TABLE START
0042A 0044    0001        A TONEH  RMB     1           HI TONE CURRENT POINTER
0043A 0045    0001        A TONEL  RMB     1           LO TONE CURRENT POINTER
0044A 0046    0001        A SCRTCH RMB     1           TEMPORARY SCRATCH
0045A 0047    0001        A LSTKEY RMB     1           LAST DIALED DIGIT USED
```

```
PAGE  002  DEMO     .SA:1  DEMO   - MC68705P3 SOURCE FOR DIALER DEMO

00047                       *
00048                       *                  MAIN ROM
00049                       *
00050A 0100                         ORG     $100
00051                       *
00052                       *     COLD START.
00053                       *     INITIALIZE PORTS.
00054                       *
00055A 0100 3F 00        A START  CLR     PORTA
00056A 0102 3F 01        A        CLR     PORTB
00057A 0104 3F 02        A        CLR     PORTC
00058A 0106 A6 0F        A        LDA     #%00001111
00059A 0108 B7 05        A        STA     PORTBD    SET PORT B DDR
00060A 010A A6 04        A        LDA     #%00000100
00061A 010C B7 06        A        STA     PORTCD    SET PORTC DDR
00062                       *
00063                       *  CHECK KEYBOARD FOR CLOSURE
00064                       *
00065A 010E CD 01B5      A SCAN   JSR     KEYIN
00066A 0111 25 07     011A        BCS     DIAL
00067                       * NO CLOSURE- CHECK "ON HOOK" SWITCH
00068A 0113 02 02 F8 010E         BRSET   1,PORTC,SCAN
00069A 0116 15 02        A        BCLR    2,PORTC   GO ON HOOK
00070A 0118 20 F4     010E        BRA     SCAN
00071                       *
00072                       * DIGIT HAS BEEN PUSHED.
00073                       * IF PREVIOUSLY ON-HOOK, COME OFF-HOOK
00074                       * AND WAIT FOR NEXT KEY.
00075                       *
00076A 011A 04 02 04 0121 DIAL    BRSET   2,PORTC,DODIAL
00077A 011D 14 02        A        BSET    2,PORTC   OFF-HOOK
00078A 011F 20 ED     010E        BRA     SCAN
00079                       *
00080                       * SEE IF PULSE DIALING OR DTMF
00081                       *
00082A 0121 01 02 05 0129 DODIAL  BRCLR   0,PORTC,PULSE
00083A 0124 CD 013B      A        JSR     DTONE     DTMF DIAL
00084A 0127 20 E5     010E        BRA     SCAN
00085                       *
00086                       * PULSE DIALING
00087                       * "*" AND "#" KEYS ARE NOT RECOGNIZED
00088                       *
00089A 0129 A1 0A        A PULSE  CMP     #$A
00090A 012B 22 E1     010E        BHI     SCAN
00091A 012D CD 01F5      A        JSR     PDIAL
00092A 0130 20 DC     010E        BRA     SCAN
```

```
00094                          ********************************************
00095                          *                                          *
00096                          *              SUBROUTINES                 *
00097                          *                                          *
00098                          ********************************************



00100                          *
00101                          *                  WAITMS
00102                          *   WAITS THE NUMBER OF mSECS GIVEN IN ACC.
00103                          *   BOTH ACC AND X ARE DESTROYED.
00104                          *
00105A 0132 AE 7C          A WAITMS LDX    #124
00106A 0134 5A             A WAIT1  DECX
00107A 0135 26 FD     0134        BNE    WAIT1
00108A 0137 4A                    DECA
00109A 0138 26 F8     0132        BNE    WAITMS
00110A 013A 81                    RTS



00112                          *
00113                          *                  DTONE
00114                          *    GENERATES 2 TONE BURST OF 65 MSEC
00115                          *    FOLLOWED BY A FORCED 25 mSEC SILENT
00116                          *    PERIOD FOR DTMF DIALING.
00117                          *    DTMF DIGIT ($0-$F) IS GIVEN IN ACC.
00118                          *
00119                          *    INTERRUPTS MUST BE MASKED BEFORE ENTRY.
00120                          *
00121A 013B A4 0F          A DTONE  AND    #$F
00122A 013D 97                      TAX
00123A 013E 58                      LSLX              X 2 FOR DISPLACEMENT
00124A 013F D6 0195        A        LDA    TTAB,X
00125A 0142 B7 42          A        STA    STARTH     HI TONE START POINTER
00126A 0144 B7 44          A        STA    TONEH      HI TONE CURRENT POINTER
00127A 0146 D6 0196        A        LDA    TTAB+1,X
00128A 0149 B7 43          A        STA    STARTL     LO TONE START POINTER
00129A 014B B7 45          A        STA    TONEL      LO TONE CURRENT POINTER
00130                            *
00131                            * SET TONE TIME COUNTER
00132                            *
00133A 014D A6 FD          A        LDA    #$FD
00134A 014F B7 40          A        STA    TIMEH      MS
00135A 0151 A6 EC          A        LDA    #$EC
00136A 0153 B7 41          A        STA    TIMEL      LS
00137                            *
00138                            *    TONE GENERATION LOOP.
00139                            *    CONSTANT LOOP TIME OF 122 uSECS.
00140                            *
00141A 0155 3C 41          A TONELP INC    TIMEL
00142A 0157 26 08     0161        BNE    NCARRY
00143A 0159 3C 40          A        INC    TIMEH
00144A 015B 26 07     0164 CONT   BNE    GETLO
00145                            *
00146                            *  ALL DONE
00147                            *
```

```
PAGE  004  DEMO     .SA:1  DEMO   - MC68705P3 SOURCE FOR DIALER DEMO

00148A 015D A6 19       A          LDA     #25
00149A 015F 20 D1    0132          BRA     WAITMS
00150                          *
00151A 0161 9D                 NCARRY NOP                NO CARRY- BURN 6 uSECS
00152A 0162 20 F7    015B          BRA     CONT
00153                          *
00154                          * GET LO TONE
00155                          *
00156A 0164 BE 45       A GETLO   LDX     TONEL     LO TONE CURRENT POINTER
00157A 0166 F6                    LDA     ,X        GET BYTE
00158                          * LO TONES ARE IN LEFT NIBBLE
00159                          * SEE IF TABLE END (MS BIT =1)
00160A 0167 2B 04    016D          BMI     GETNLO
00161A 0169 9D                     NOP
00162A 016A 9D                     NOP               FILL FOR CONSTANT TIME
00163A 016B 20 03    0170          BRA     SHFLO
00164                          *
00165                          * TABLE END- RESET TO TABLE START
00166                          *
00167A 016D BE 43       A GETNLO LDX     STARTL
00168A 016F F6                    LDA     ,X
00169                          *
00170                          *   SWAP NIBBLES
00171                          *
00172A 0170 44                 SHFLO  LSRA
00173A 0171 44                        LSRA
00174A 0172 44                        LSRA
00175A 0173 44                        LSRA
00176                          * LO BYTE VALID- SAVE
00177A 0174 B7 46       A              STA     SCRTCH
00178                          * FIX POINTER AND SAVE
00179A 0176 5C                         INCX
00180A 0177 BF 45       A              STX     TONEL
00181                          *
00182                          *   GET HI TONE
00183                          *
00184A 0179 BE 44       A              LDX     TONEH     HI TONE CURRENT POINTER
00185A 017B F6                         LDA     ,X        GET BYTE
00186                          * SEE IF TABLE END
00187A 017C A4 0F       A              AND     #$F
00188A 017E A1 0F       A              CMP     #$F
00189A 0180 27 04    0186              BEQ     GENHI
00190A 0182 9D                         NOP
00191A 0183 9D                         NOP               FILL FOR CONSTANT TIME
00192A 0184 20 03    0189              BRA     ADDNUM
00193                          *
00194                          * HI TABLE END- RESET TO START
00195                          *
00196A 0186 BE 42       A GENHI   LDX     STARTH
00197A 0188 F6                    LDA     ,X
00198                          * GOT HI NIBBLE- FIX X
00199A 0189 5C                 ADDNUM INCX
00200A 018A BF 44       A              STX     TONEH
00201                          *
00202                          * ADD LO AND HI TONES
00203                          *
00204A 018C BB 46       A              ADD     SCRTCH
00205                          * OUTPUT THIS SAMPLE
```

```
PAGE  005  DEMO     .SA:1  DEMO   - MC68705P3 SOURCE FOR DIALER DEMO

00206A 018E B7 01        A          STA     PORTB
00207                               *
00208                               * KEEP GOING
00209                               *
00210A 0190 9D                      NOP
00211A 0191 9D                      NOP
00212A 0192 9D                      NOP                FILL FOR 122 uSEC LOOP
00213A 0193 20 C0     0155          BRA     TONELP


00215                               *
00216                               *   TONE PAIR LOOK-UP TABLE
00217                               *
00218A 0195     9C        A TTAB    FCB     TN1336   (0)
00219A 0196     E3        A         FCB     TN941
00220A 0197     80        A         FCB     TN1209   (1)
00221A 0198     80        A         FCB     TN697
00222A 0199     9C        A         FCB     TN1336   (2)
00223A 019A     80        A         FCB     TN697
00224A 019B     C2        A         FCB     TN1477   (3)
00225A 019C     80        A         FCB     TN697
00226A 019D     80        A         FCB     TN1209   (4)
00227A 019E     A4        A         FCB     TN770
00228A 019F     9C        A         FCB     TN1336   (5)
00229A 01A0     A4        A         FCB     TN770
00230A 01A1     C2        A         FCB     TN1477   (6)
00231A 01A2     A4        A         FCB     TN770
00232A 01A3     80        A         FCB     TN1209   (7)
00233A 01A4     C5        A         FCB     TN852
00234A 01A5     9C        A         FCB     TN1336   (8)
00235A 01A6     C5        A         FCB     TN852
00236A 01A7     C2        A         FCB     TN1477   (9)
00237A 01A8     C5        A         FCB     TN852
00238A 01A9     D9        A         FCB     TN1633   (A)
00239A 01AA     80        A         FCB     TN697
00240A 01AB     D9        A         FCB     TN1633   (B)
00241A 01AC     A4        A         FCB     TN770
00242A 01AD     D9        A         FCB     TN1633   (C)
00243A 01AE     C5        A         FCB     TN852
00244A 01AF     D9        A         FCB     TN1633   (D)
00245A 01B0     E3        A         FCB     TN941
00246A 01B1     80        A         FCB     TN1209   (*)
00247A 01B2     E3        A         FCB     TN941
00248A 01B3     C2        A         FCB     TN1477   (#)
00249A 01B4     E3        A         FCB     TN941


00251                               *
00252                               *          KEYIN
00253                               * SCANS KEYBOARD FOR PRESSED KEY.
00254                               * WHEN A NEW KEY IS PRESSED, RETURN
00255                               * WITH CARRY SET AND KEY VALUE IN ACC.
00256                               *
00257A 01B5 AD 1F     01D6 KEYIN    BSR     CHECK    CHECK FOR INPUT
00258A 01B7 25 15     01CE          BCS     KEY1     ANY KEY?
00259                               *
```

```
PAGE  006  DEMO    .SA:1  DEMO   - MC68705P3 SOURCE FOR DIALER DEMO

00260                       * NO KEY PRESSED.
00261                       * IF FIRST TIME, WAIT OUT DEBOUNCE.
00262                       *
00263A 01B9 B6 47        A          LDA     LSTKEY
00264A 01BB A1 0A        A          CMP     #$A
00265A 01BD 27 0D     01CC          BEQ     KEY22
00266                       * FIRST TIME
00267A 01BF A6 19        A          LDA     #25
00268A 01C1 CD 0132      A          JSR     WAITMS
00269A 01C4 AD 10     01D6          BSR     CHECK
00270A 01C6 25 06     01CE          BCS     KEY11
00271                       * STILL NO KEY
00272A 01C8 A6 0A        A          LDA     #$A
00273A 01CA B7 47        A          STA     LSTKEY
00274A 01CC 98                   KEY22  CLC
00275A 01CD 81                          RTS
00276                       *
00277                       * GOT A KEY.
00278                       * CHECK THAT IT IS FIRST TIME.
00279                       *
00280A 01CE B1 47        A KEY11    CMP     LSTKEY
00281A 01D0 27 FA     01CC          BEQ     KEY22
00282A 01D2 B7 47        A          STA     LSTKEY
00283A 01D4 99                          SEC
00284A 01D5 81                          RTS



00286                       *
00287                       *       CHECK
00288                       * SCANS KEYBOARD FOR CLOSURE.
00289                       * IF KEY CLOSED, RETURNS WITH KEY
00290                       * VALUE IN ACC AND CARRY SET.
00291                       *
00292A 01D6 4F                   CHECK  CLRA
00293A 01D7 BE 00        A          LDX     PORTA     GET KEYS
00294A 01D9 58                   KEY1   LSLX
00295A 01DA 24 17     01F3          BCC     GOTKEY    KEY CLOSED?
00296A 01DC 4C                          INCA              NO
00297A 01DD A1 08        A          CMP     #8
00298A 01DF 26 F8     01D9          BNE     KEY1
00299                       * CHECK BALANCE OF KEYS ON PORTB
00300A 01E1 0F 01 0F 01F3            BRCLR   7,PORTB,GOTKEY "8"?
00301A 01E4 4C                          INCA
00302A 01E5 0D 01 0B 01F3            BRCLR   6,PORTB,GOTKEY "9"?
00303A 01E8 A6 0E        A          LDA     #$E
00304A 01EA 0B 01 06 01F3            BRCLR   5,PORTB,GOTKEY "*"?
00305A 01ED 4C                          INCA
00306A 01EE 09 01 02 01F3            BRCLR   4,PORTB,GOTKEY "*"?
00307                       *
00308                       * NO KEY PRESSED.
00309                       *
00310A 01F1 98                          CLC
00311A 01F2 81                          RTS
00312                       *
00313                       *   GOT A KEY.
00314                       *
00315A 01F3 99                   GOTKEY SEC
```

```
00316A 01F4 81                      RTS


00318                               *
00319                               *     PDIAL
00320                               * PULSE DIALS THE DIGIT GIVEN IN
00321                               * ACC. FOLLOWED BY A 200 MSEC. WAIT.
00322                               *
00323A 01F5 4D                      PDIAL   TSTA                BNE PDIAL1
00324A 01F6 26 02     01FA          BNE     PDIAL1
00325                               * CHANGE "0" TO #$A
00325A 01F8 A6 0A           A       LDA     #$A
00327A 01FA B7 46           A PDIAL1 STA    SCRTCH   SAVE
00328                               * MAKE A PULSE
00329A 01FC 15 02           A PDIAL2 BCLR   2,PORTC  ON HOOK
00330A 01FE A6 3D           A       LDA     #61
00331A 0200 CD 0132         A       JSR     WAITMS
00332A 0203 14 02           A       BSET    2,PORTC  OFF HOOK
00333A 0205 A6 27           A       LDA     #39
00334A 0207 CD 0132         A       JSR     WAITMS
00335A 020A 3A 46           A       DEC     SCRTCH
00336A 020C 26 EE     01FC          BNE     PDIAL2
00337                               * WAIT 200 MSEC INTER-DIGIT
00338A 020E A6 C8           A       LDA     #200
00339A 0210 CC 0132         A       JMP     WAITMS
```

```
00341                           *
00342                           *       TOUCH TONE GENERATOR TABLE
00343                           *


00345A 0080                             ORG     $80
00346A 0080     77          A TN697     FCB     $77
00347A 0081     76          A           FCB     $76
00348A 0082     53          A           FCB     $53
00349A 0083     30          A           FCB     $30
00350A 0084     21          A           FCB     $21
00351A 0085     03          A           FCB     $03
00352A 0086     06          A           FCB     $06
00353A 0087     17          A           FCB     $17
00354A 0088     25          A           FCB     $25
00355A 0089     42          A           FCB     $42
00356A 008A     60          A           FCB     $60
00357A 008B     71          A           FCB     $71
00358A 008C     74          A           FCB     $74
00359A 008D     67          A           FCB     $67
00360A 008E     57          A           FCB     $57
00361A 008F     34          A           FCB     $34
00362A 0090     11          A           FCB     $11
00363A 0091     00          A           FCB     $00
00364A 0092     02          A           FCB     $02
00365A 0093     15          A           FCB     $15
00366A 0094     27          A           FCB     $27
00367A 0095     46          A           FCB     $46
00368A 0096     64          A           FCB     $64
00369A 0097     71          A           FCB     $71
00370A 0098     70          A           FCB     $70
00371A 0099     62          A           FCB     $62
00372A 009A     45          A           FCB     $45
00373A 009B     3F          A           FCB     $3F
00374A 009C     17          A TN1336    FCB     $17
00375A 009D     05          A           FCB     $05
00376A 009E     02          A           FCB     $02
00377A 009F     10          A           FCB     $10
00378A 00A0     31          A           FCB     $31
00379A 00A1     55          A           FCB     $55
00380A 00A2     67          A           FCB     $67
00381A 00A3     F6          A           FCB     $F6
00382A 00A4     72          A TN770     FCB     $72
00383A 00A5     60          A           FCB     $60
00384A 00A6     51          A           FCB     $51
00385A 00A7     34          A           FCB     $34
00386A 00A8     17          A           FCB     $17
00387A 00A9     06          A           FCB     $06
00388A 00AA     03          A           FCB     $03
00389A 00AB     20          A           FCB     $20
00390A 00AC     41          A           FCB     $41
00391A 00AD     54          A           FCB     $54
00392A 00AE     77          A           FCB     $77
00393A 00AF     76          A           FCB     $76
00394A 00B0     63          A           FCB     $63
00395A 00B1     40          A           FCB     $40
00395A 00B2     20          A           FCB     $20
```

```
00397A 00B3    13          A          FCB    $13
00398A 00B4    06          A          FCB    $06
00399A 00B5    17          A          FCB    $17
00400A 00B6    24          A          FCB    $24
00401A 00B7    41          A          FCB    $41
00402A 00B8    60          A          FCB    $60
00403A 00B9    73          A          FCB    $73
00404A 00BA    76          A          FCB    $76
00405A 00BB    57          A          FCB    $57
00406A 00BC    34          A          FCB    $34
00407A 00BD    11          A          FCB    $11
00408A 00BE    00          A          FCB    $00
00409A 00BF    03          A          FCB    $03
00410A 00C0    16          A          FCB    $16
00411A 00C1    3F          A          FCB    $3F
00412A 00C2    57          A TN1477   FCB    $57
00413A 00C3    65          A          FCB    $65
00414A 00C4    F1          A          FCB    $F1
00415A 00C5    70          A TN852    FCB    $70
00416A 00C6    63          A          FCB    $63
00417A 00C7    46          A          FCB    $46
00418A 00C8    27          A          FCB    $27
00419A 00C9    03          A          FCB    $03
00420A 00CA    00          A          FCB    $00
00421A 00CB    11          A          FCB    $11
00422A 00CC    35          A          FCB    $35
00423A 00CD    57          A          FCB    $57
00424A 00CE    75          A          FCB    $75
00425A 00CF    72          A          FCB    $72
00426A 00D0    60          A          FCB    $60
00427A 00D1    42          A          FCB    $42
00428A 00D2    16          A          FCB    $16
00429A 00D3    07          A          FCB    $07
00430A 00D4    04          A          FCB    $04
00431A 00D5    20          A          FCB    $20
00432A 00D6    41          A          FCB    $41
00433A 00D7    64          A          FCB    $64
00434A 00D8    7F          A          FCB    $7F
00435A 00D9    77          A TN1633   FCB    $77
00436A 00DA    55          A          FCB    $55
00437A 00DB    31          A          FCB    $31
00438A 00DC    11          A          FCB    $11
00439A 00DD    05          A          FCB    $05
00440A 00DE    17          A          FCB    $17
00441A 00DF    25          A          FCB    $25
00442A 00E0    51          A          FCB    $51
00443A 00E1    61          A          FCB    $61
00444A 00E2    F4          A          FCB    $F4
00445A 00E3    77          A TN941    FCB    $77
00446A 00E4    65          A          FCB    $65
00447A 00E5    41          A          FCB    $41
00448A 00E6    21          A          FCB    $21
00449A 00E7    04          A          FCB    $04
00450A 00E8    07          A          FCB    $07
00451A 00E9    25          A          FCB    $25
00452A 00EA    51          A          FCB    $51
00453A 00EB    70          A          FCB    $70
00454A 00EC    74          A          FCB    $74
```

```
PAGE  010  DEMO     .SA:1  DEMO    - MC68705P3 SOURCE FOR DIALER DEMO

00455A 00ED    67        A          FCB     $67
00456A 00EE    35        A          FCB     $35
00457A 00EF    11        A          FCB     $11
00458A 00F0    00        A          FCB     $00
00459A 00F1    14        A          FCB     $14
00460A 00F2    37        A          FCB     $37
00461A 00F3    55        A          FCB     $55
00462A 00F4    71        A          FCB     $71
00463A 00F5    70        A          FCB     $70
00464A 00F6    54        A          FCB     $54
00465A 00F7    37        A          FCB     $37
00466A 00F8    15        A          FCB     $15
00467A 00F9    01        A          FCB     $01
00468A 00FA    10        A          FCB     $10
00469A 00FB    44        A          FCB     $44
00470A 00FC    6F        A          FCB     $6F
00471A 00FD    FF        A          FCB     $FF
00472A 00FE    00        A TNOFF    FCB     $00
00473A 00FF    FF        A          FCB     $FF


00475          0080      A TN1209   EQU     TN697     (SHARE START ADDRESS)
```

```
00478                           *
00479                           *     INTERRUPT VECTORS
00480                           *
00481A 07F8                             ORG     $7F8
00482A 07F8     0100      A             FDB     START     TIMER INERRUPT
00483A 07FA     0100      A             FDB     START     HARDWARE INTERRUPT
00484A 07FC     0100      A             FDB     START     SWI
00485A 07FE     0100      A             FDB     START     RESET
00486                                   END
TOTAL ERRORS 00000--00000
```

```
0189 ADDNUM 00192 00199*
01D6 CHECK  00257 00269 00292*
015B CONT   00144*00152
011A DIAL   00066 00076*
0121 DODIAL 00076 00082*
013B DTONE  00083 00121*
0186 GENHI  00189 00196*
0164 GETLO  00144 00156*
016D GETNLO 00160 00167*
01F3 GOTKEY 00295 00300 00302 00304 00306 00315*
01D9 KEY1   00294*00298
01CE KEY11  00258 00270 00280*
01CC KEY22  00265 00274*00281
01B5 KEYIN  00065 00257*
0047 LSTKEY 00045*00263 00273 00280 00282
016A NCARRY 00142 00151*
01F5 PDIAL  00091 00323*
01FA PDIAL1 00324 00327*
01FC PDIAL2 00329*00336
0000 PORTA  00025*00055 00293
0004 PORTAD 00028*
0001 PORTB  00026*00056 00206 00300 00302 00304 00305
0005 PORTBD 00029*00059
0002 PORTC  00027*00057 00068 00069 00076 00077 00082 00329 00332
0006 PORTCD 00030*00061
0129 PULSE  00082 00089*
01BE SCAN   00065*00068 00070 00078 00084 00090 00092
0046 SCRTCH 00044*00177 00204 00327 00335
0170 SHFLO  00163 00172*
0100 START  00055*00482 00483 00484 00485
0042 STARTH 00040*00125 00196
0043 STARTL 00041*00128 00167
0040 TIMEH  00038*00134 00143
0041 TIMEL  00039*00136 00141
0009 TMRCON 00032*
0008 TMRDAT 00031*
0080 TN1209 00220 00226 00232 00246 00475*
009C TN1336 00218 00222 00228 00234 00374*
00C2 TN1477 00224 00230 00236 00248 00412*
00D9 TN1633 00238 00240 00242 00244 00435*
```

```
PAGE  012  DEMO    .SA:1  DEMO   - MC68705P3 SOURCE FOR DIALER DEMO

   0080 TN697   00221 00223 00225 00239 00346*00475
   00A4 TN770   00227 00229 00231 00241 00382*
   00C5 TN852   00233 00235 00237 00243 00415*
   00E3 TN941   00219 00245 00247 00249 00445*
   00FE TNOFF   00472*
   0044 TONEH   00042*00126 00184 00200
   0045 TONEL   00043*00129 00156 00180
   0155 TONELP  00141*00213
   0195 TTAB    00124 00127 00218*
   0134 WAIT1   00106*00107
   0132 WAITMS  00105*00109 00149 00268 00331 00334 00339
```

```
PAGE 001  TONCAL  .SA:1

0100 DIM T(100)
0101  H=1
0102  P=122E-6
0110  C=0
0120  W=P*1E6
0121 PRINT "PERIOD = ";W;"uSECS (Y/N)";
0122 INPUT A$
0123 IF A$="Y" THEN GOTO 130
0124 IF A$()"N" THEN GOTO 121
0125 INPUT "PERIOD (uSECES)=",P
0126  P=P*1E-6
0130 PRINT "TONE FREQ=";
0140 INPUT F
0150  X=2*3.141593*F*P
0160 FOR N=1 TO 100
0170  T(N)=INT(3.5*COS(N*X)+4)
0171 GOSUB 8000
0190 IF T(N)(7 THEN GOTO 370
0200 REM GOT A CREST- CALCULATE CUMULATIVE ERROR
0220  Q=N*P
0230  E=(C/F-Q)*100/Q
0240 GOSUB 7000
0260 PRINT "ERROR       =";E;"%"
0270 PRINT "SAMPLE COUNT=",N
0275 PRINT "FREQUENCY   =";F;"Hz"
0280 PRINT "CONTINUE (Y/N)";
0290 INPUT A$
0300 IF A$="Y" THEN GOTO 370
0310 IF A$()"N" THEN GOTO 280
0320 REM DONE- PRINT SAMPLE LIST
0330 GOSUB 9000
0332 GOTO 110
0370 NEXT N
0380 PRINT "SAMPLE COUNT ) 100"
0390 END
7000 REM PLOT SUBROUTINE
7001 PRINT CHR$(27);"a"
7002 FOR I=1 TO 50
7003 NEXT I
7005 PRINT
7006 PRINT "  |"
7010 FOR I = 1 TO 8
7020  L=8-I
7030 PRINT L;"|";
7040 REM PRINT THIS LINE
7050 FOR J=1 TO N
7060 IF T(J)=L THEN GOTO 7090
7070 PRINT " ";
7080 GOTO 7100
7090 PRINT "*";
7100 NEXT J
7110 PRINT
7120 NEXT I
7130 PRINT "  ";
7140 FOR I=1 TO 70
7150 PRINT ":";
7160 NEXT I
7165  W=P*1E6
```

```
PAGE 002  TONCAL  .SA:1

7170 PRINT "                              HORIZONTAL =";W;"uSEC"
7180 PRINT
7190 PRINT
7200 RETURN
8000 REM CREST COUNT ROUTINE- LOOK FOR A ZERO CROSSING
8010 IF T(N) )3 THEN GOTO 8040
8020  H=0
8030 RETURN
8040 IF H=0 THEN C=C+1
8050  H=1
8060 RETURN
9000 REM PRINTER OUTPUT SUBROUTINE
9011 FOR J=1 TO 4
9012 PRINT #2
9013 NEXT J
9020 PRINT #2
9030 PRINT #2,"  :"
9040 FOR I=1 TO 8
9050  L=8-I
9060 PRINT #2,L;":";
9070 FOR J=1 TO N
9080 IF T(J)=L THEN GOTO 9110
9090 PRINT #2," ";
9100 GOTO 9120
9110 PRINT #2,"*";
9120 NEXT J
9130 PRINT #2
9140 NEXT I
9150 PRINT #2,"  ";
9160 FOR I=1 TO 70
9170 PRINT #2,":";
9180 NEXT I
9190  W=P*1E6
9191 DIGITS= 3
9192 PRINT #2
9200 PRINT #2,"                              HORIZONTAL = ";W;" uSEC"
9210 PRINT #2
9220 PRINT #2
9230 PRINT #2,"FREQUENCY    = ";F;" Hz"
9240 PRINT #2,"ERROR        = ";E;" %"
9250 PRINT #2,"NO. SAMPLES  = ";N
9260 PRINT #2,"NO. CYCLES   = ";C
9270 PRINT #2
9271 DIGITS= 0
9280 PRINT #2
9290 FOR J=1 TO N STEP 2
9300 PRINT #2,"SAMPLE ";J;" = ";T(J);
9310  B=J+1
9320 IF B)N THEN GOTO 9340
9330 PRINT #2,"        SAMPLE ";B;" = ";T(B);
9340 PRINT #2
9350 NEXT J
9360 PRINT #2,CHR$(12)
9370 RETURN
```

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

Interfacing The Speakerphone To The MC34010/11/13 Speech Networks

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INTRODUCTION

Interfacing the MC34018 speakerphone circuit to the MC34010 series of telephone circuits is described in this application note. The series includes the MC34010, MC34011, MC34013, and the newer "A" version of each of those. The interface is applicable to existing designs, as well as to new designs.

FUNCTIONAL REQUIREMENTS

Figure 1 shows the basic MC34010 telephone circuit as described in the data sheet. It is a completely functional telephone meant for use with a handset, and provides the additional function of a microprocessor interface for the DTMF dialing function. The MC34011 does not have the microprocessor interface, but otherwise is identical, including the pin numbers. The MC34013 has the same speech network, dialer, and line interface circuit as the MC34010, but does not have the microprocessor interface or the tone ringer. Except for a minor difference between the speech networks of the "A" version parts and the "non-A" parts, the interface to the speakerphone circuit is virtually the same for all 6 parts.

Figure 2 shows the basic MC34018 speakerphone circuit as described in the data sheet. It is NOT a complete telephone, but provides only the speakerphone functions. It requires a speech network, such as the MC34010, to transfer the speech signals to/from the Tip & Ring lines, and to provide the required supply voltage. The four external connections — transmit output, receive input, dc line input, and chip select — are the points which must be interfaced to the speech network.

In the following text, only the MC34010 interface will be described. The interface to the other parts is the same except where noted.

When combining a speech network which operates a handset, with a speakerphone circuit, certain changes are required in the circuit operation when switching between the handset mode and the speakerphone mode, and additionally when the dialing mode is in effect. The four modes to be considered are: 1) using the handset for speech, 2) using the speakerphone for speech, 3) dialing in the handset mode, and 4) dialing in the speakerphone mode. The requirements are summarized in the following table:

Mode	MC34018	Vlr	Handset Mike	Speaker-phone Mike
Handset-Speech	Unpowered	Low	Live	N/A
Spkrphone Speech	Powered	High	Dead	Live
Handset-Dialing	Unpowered	Low	Dead	N/A
Spkrphone Dialing	Powered	High	Dead	Dead

Since the entire circuit is to be powered by the phone line, the speakerphone circuit is powered up only when it is to be used since it uses a portion of the loop current, (a significant portion on long loops). The MC34010, however, must be powered all the time since it is the interface to the phone line. The Vlr voltage mentioned in the table is the voltage across the resistor at the LR pin of the MC34010, which sets the dc characteristics of the circuit. By increasing that resistor, the dc supply voltage (and the voltage at Tip & Ring) will be increased in the speakerphone modes, where additional power is required.

The handset mike is to be functional only in the handset-speech mode. If it were functional in the speakerphone-speech mode, system oscillations and/or additional echoes could occur. Disabling the microphone is accomplished by activating the MM (Mike Mute) pin on the MC34010. On the MC34010A, activating the MM pin results in disabling the transmit amplifier, so in that case, a transistor is added to the microphone circuit as the means to disable it. In both dialing modes, muting is automatic whenever the dialer is activated, so the DTMF tones are not distorted by sounds entering the microphone.

The speakerphone mike is listed as N/A in the handset modes since the MC34018 circuit is unpowered, effectively disabling the mike. In the speakerphone dialing mode it must be non-functional for the same reason as mentioned above. That is accomplished by the fact that the MC34010 (and MC34010A) transmit amplifier is inoperative when its DTMF dialer is activated.

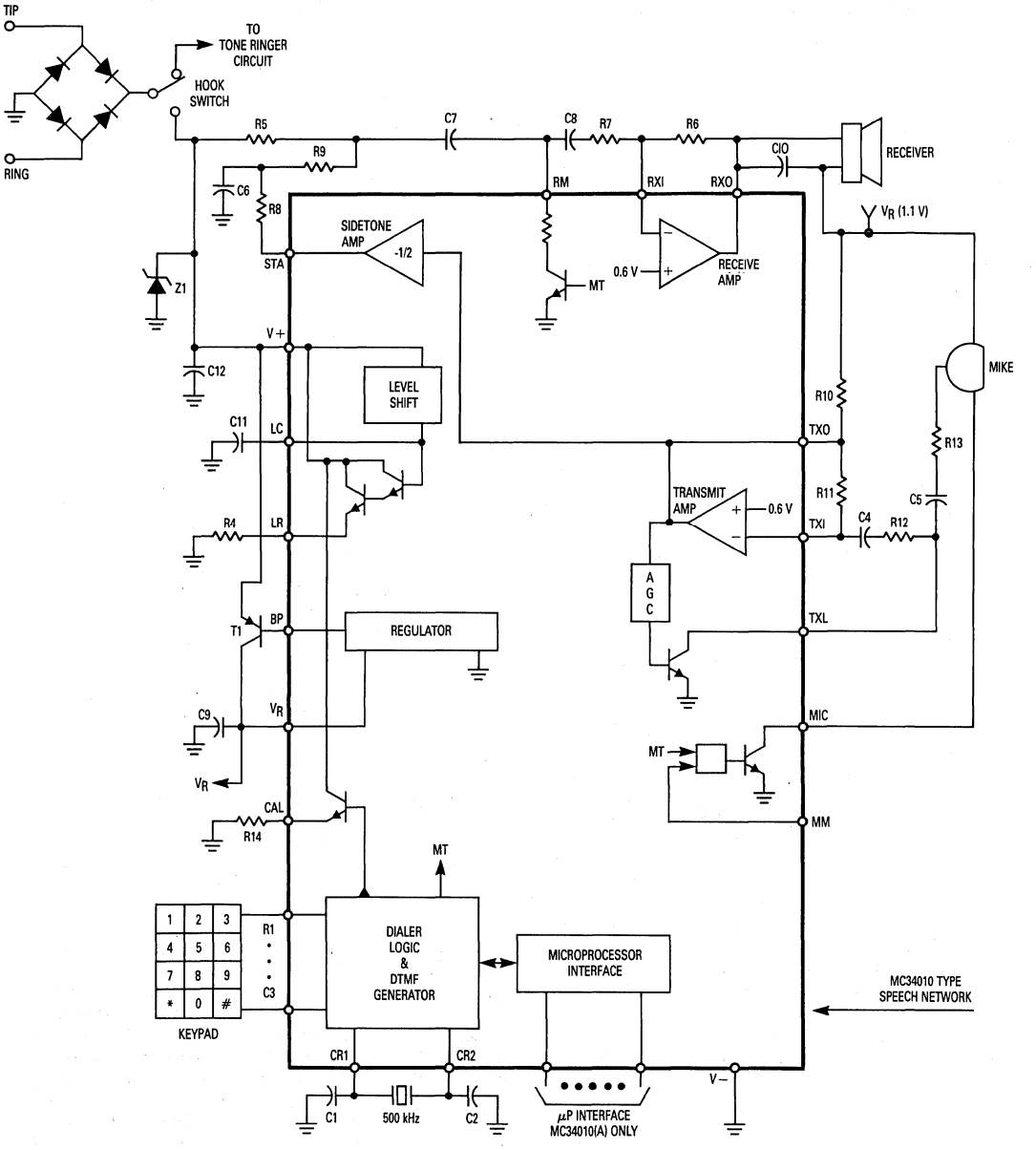


Figure 1. Basic MC34010 Type Telephone

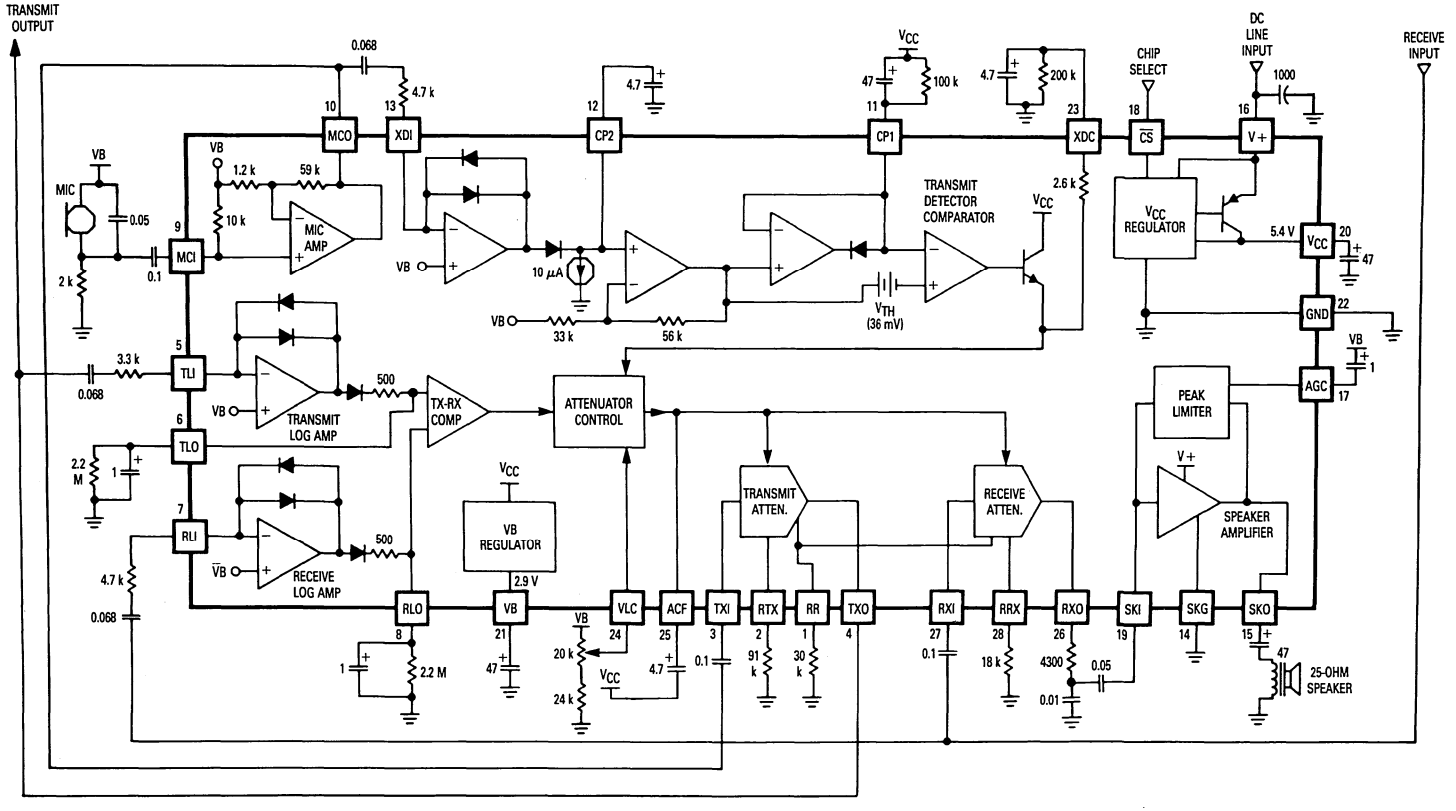


Figure 2. MC34018 Speakerphone Circuit

CIRCUIT DESCRIPTION

SWITCHING ARRANGEMENT

Figure 3 indicates the switching arrangement for going off-hook in either the handset mode or speakerphone mode, and for switching between them. S1 (a two pole switch) is the normal hook switch activated by lifting the handset. S2 (a two pole switch) is a manually operated switch which activates the speakerphone.

Whenever the handset is off-hook, and S2 is in the off position, power from Tip & Ring is applied to the MC34010 through the diode bridge and S1A. S1B's position is of no consequence in this mode. Should S2 be switched on while the handset is off-hook, power is then applied to the speakerphone IC through S2B. However, since S1B is open, the MC34018's $\overline{CS}$ pin (Chip Select) is taken high through R33, disabling the IC.

Anytime the handset is on-hook, and S2 is on (both poles closed), power is applied to both the MC34010 and the MC34018. Since S1B is closed, $\overline{CS}$ is taken low, enabling the speakerphone circuit. Anytime the handset is taken off-hook the circuit will revert back to the handset mode.

The 1.0 Henry inductor isolates the speech signals at Tip & Ring from the V+ pin of the MC34018, preventing an oscillatory loop from forming. The diode bridge, B2, is added for the tone ringer circuit of the MC34010(A), or MC34011(A), to keep the switches S1 and S2 from requiring 3 poles each.

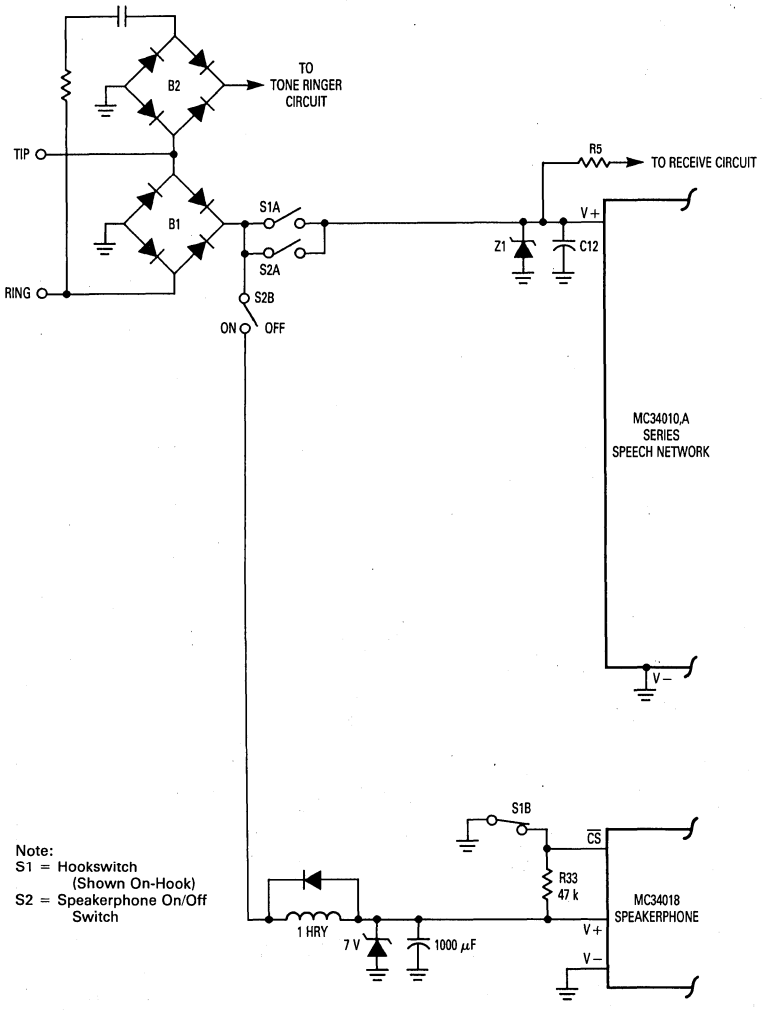


Figure 3. Handset/Speakerphone Power Switching

VIr SHIFT

Since a speakerphone requires more power than a handset, it is necessary, particularly on long loops, to increase the Tip-Ring voltage. Since on long loops the Tip & Ring lines act more like a current source than a voltage source, increasing the voltage does not significantly decrease the available loop current. In order to shift the dc voltage, the additional components shown in Figure 4 are used. The voltage at the output of the diode bridge (B1) is equal to the voltage across the LR resistor, plus an internal level shift of approximately 3 volts between V+ and LR.

In the handset mode, the transistor T2 is on, and the equivalent LR resistance is approximately 80 ohms. The majority of the loop current (all except about 10 mA) flows through the LR resistor. In the speakerphone mode, the transistor is off, and the dc voltage is determined by the 390 ohm resistor, the internal 3 volt level shift, the resistance of the 1 Henry inductor, the 7 volt zener diode, the current draw of the two ICs, and the loop current. Figure 5 indicates the Tip-Ring voltage versus loop current for the two modes (the inductor resistance is 38 ohms).

To facilitate the design of the base drive to T2, diode D1 is added to the collector of T1, providing approximately 1.8 volts at that point. At the cathode of D1, the voltage is still regulated at 1.1 volts.

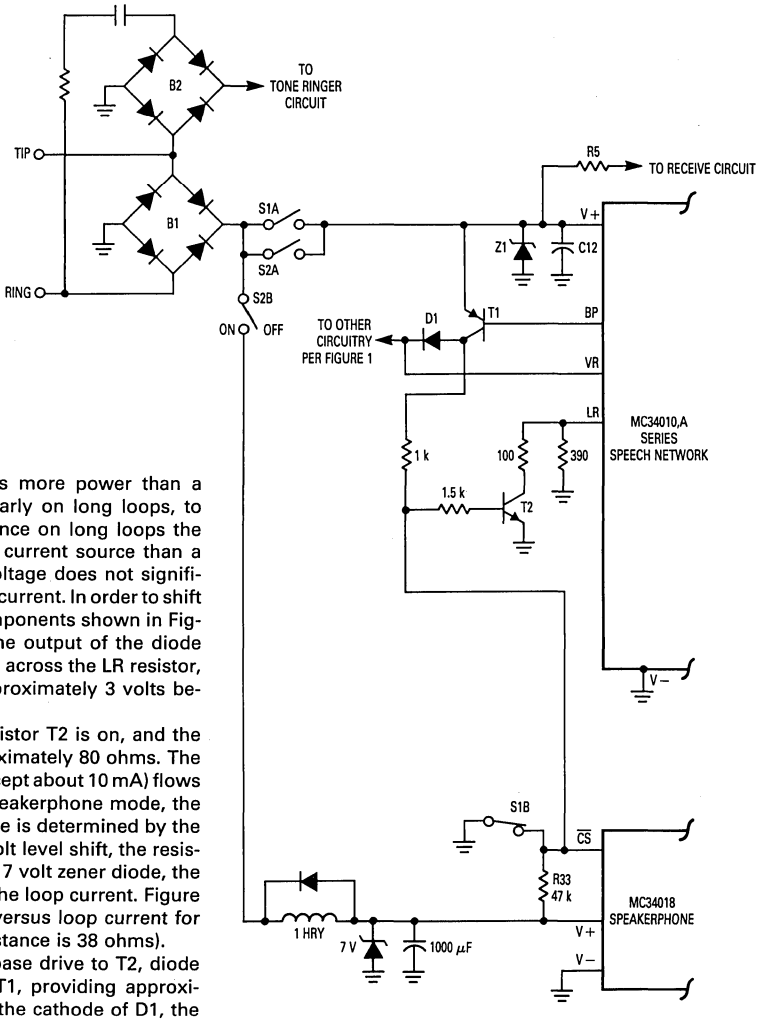


Figure 4. DC Level Shift

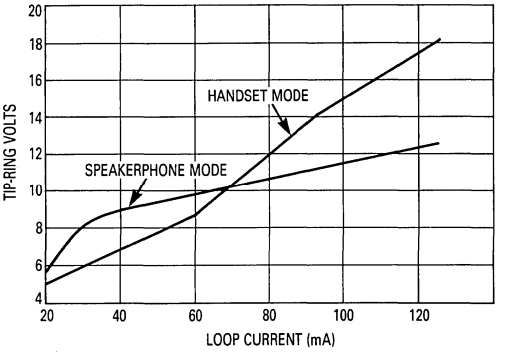


Figure 5. Tip-Ring Voltage versus Loop Current

MICROPHONE CONTROLS

To mute the handset microphone when the speakerphone speech mode is in effect, the circuit of Figure 6 is used for the MC34010 (MC34011, MC34013), and the circuit of Figure 7 is used for the MC34010A (MC34011A, MC34013A).

In Figure 6, when the handset mode is in effect, S1B takes the MM pin low, enabling the handset microphone by turning on the MIC pin (to ground). When the speakerphone mode is in effect, MM is taken high through R32, disabling the handset microphone (MIC pin is open).

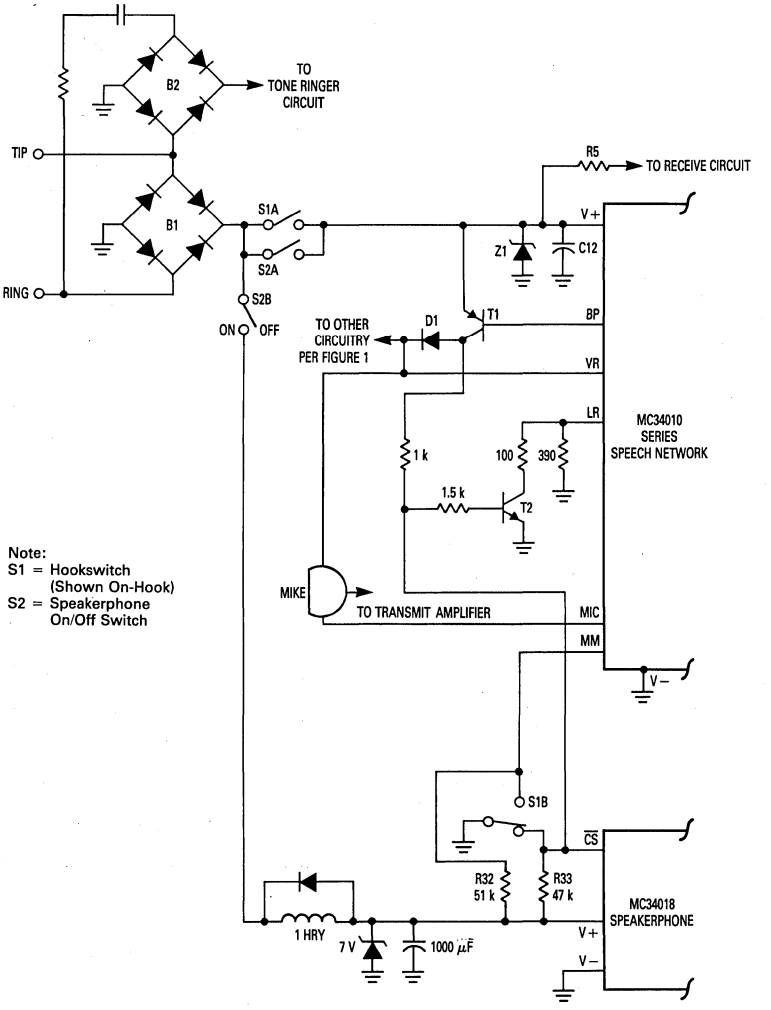


Figure 6. Microphone Muting — MC34010 Series

In Figure 7, in the handset mode, S1B is open, T3 is on, and the microphone bias current flows through the MIC pin. In the speakerphone mode, S1B is closed, turning off T3, disabling the microphone. T3 is required for disabling the microphone with the "A" series speech networks since the transmit amplifier is disabled when the MM pin is taken high.

In both the "non-A" and the "A" version circuits, the handset microphones are muted during dialing due to the fact that the MIC pin is opened by the dialer circuit.

SPEECH SIGNALS

Referring to the complete schematics (Figures 8, 9, 10, and 11) the receive signals coming in on Tip & Ring are sent to the handset receiver (at RXO) and to the speakerphone circuit's "receive input" path by the MC34010's hybrid function. It is not necessary to mute the handset receiver during speakerphone operation.

The transmit signals from the handset microphone are put onto the Tip & Ring lines through the MC34010's hybrid function, with a gain determined by resistors R27–R30. In the speakerphone mode, the transmit output signals (at TXO of the MC34018) are attenuated by R35 before being applied to the MC34010's transmit amplifier. The level of the speakerphone transmit signals at Tip & Ring can be adjusted by varying R35.

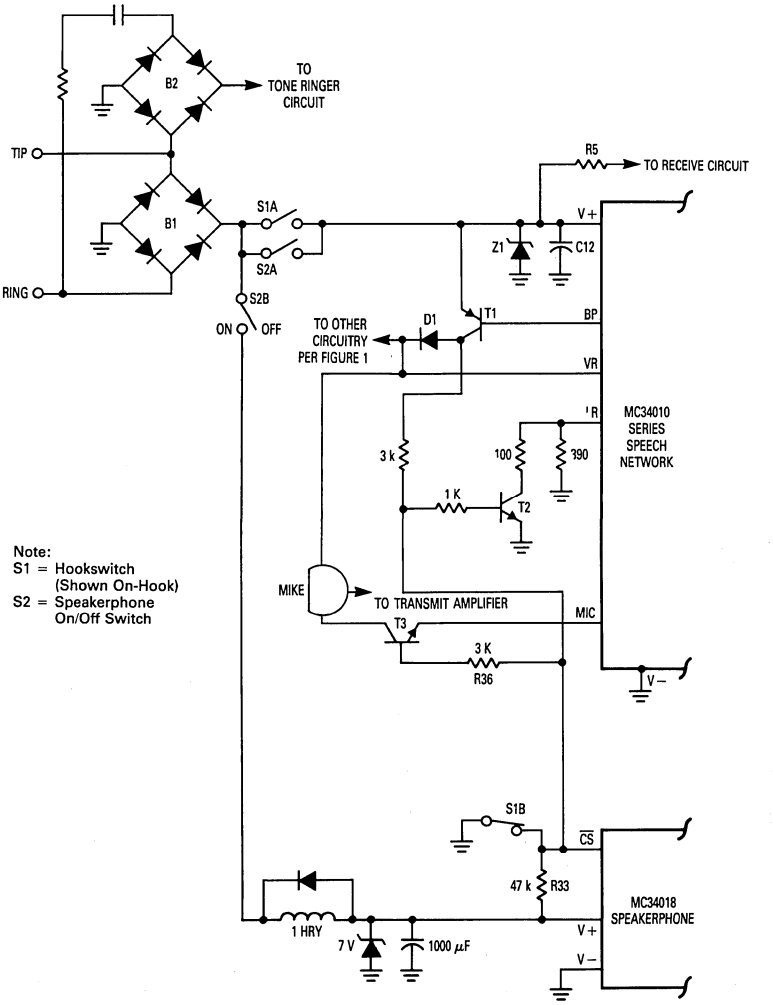
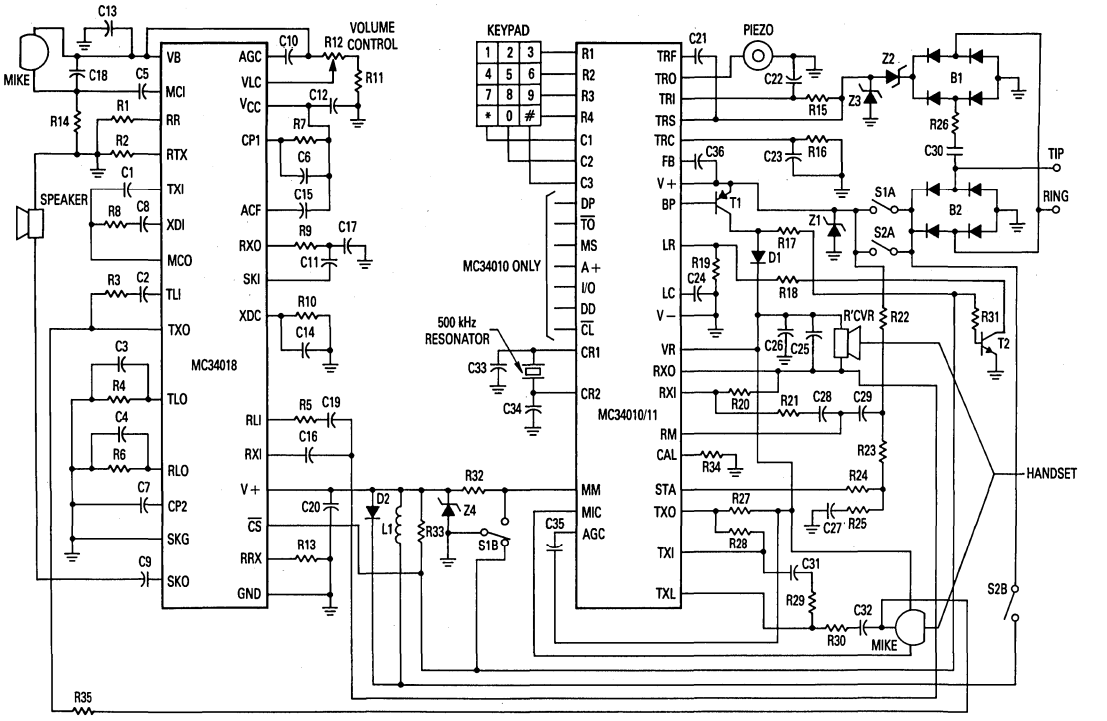


Figure 7. Microphone Muting — MC34010A Series



MC34010/11 and MC34018
COMPONENT VALUES

R1 — 30 k
R2 — 91 k
R3 — 3.3 k
R4 — 1 M
R5 — 4.7 k
R6 — 1 M
R7 — 100 k
R8 — 4.7 k
R9 — 4.3 k
R10 — 200 k
R11 — 24 k
R12 — 20 k
R13 — 18 k
R14 — 2 k
R15 — 1.8 k
R16 — 200 k
R17 — 1 k
R18 — 100
R19 — 390
R20 — 200 k
R21 — 56 k
R22 — 150 k
R23 — 56 k
R24 — 1.5 k
R25 — 1.5 k
R26 — 6.8 k
R27 — 270
R28 — 200 k
R29 — 4.7 k
R30 — 4.7 k
R31 — 1.5 k
R32 — 51 k
R33 — 47 k
R34 — 36
R35 — 33 k

C1 — 0.1
C2 — 0.068
C3 — 2.2 μF
C4 — 2.2 μF
C5 — 0.1
C6 — 47 μF
C7 — 4.7 μF
C8 — 0.068
C9 — 47 μF
C10 — 1 μF
C11 — 0.05
C12 — 47 μF
C13 — 47 μF
C14 — 4.7 μF
C15 — 4.7 μF
C16 — 0.05
C17 — 0.01
C18 — 0.05
C19 — 0.1
C20 — 1000 μF
C21 — 1 μF
C22 — 4.7 μF
C23 — 620 pF
C24 — 0.01
C25 — 0.01 μF
C26 — 2.2 μF
C27 — 0.1
C28 — 0.05
C29 — 0.05
C30 — 1 μF, NP
C31 — 0.1
C32 — 0.1
C33 — 100 pF
C34 — 100 pF
C35 — 1 μF
C36 — 0.1

L1 — 1 Hry, < 100 Ω

Z1 — 18 V
Z2 — 4.7 V
Z3 — 30 V
Z4 — 7 V
D1, D2 — 1N4001

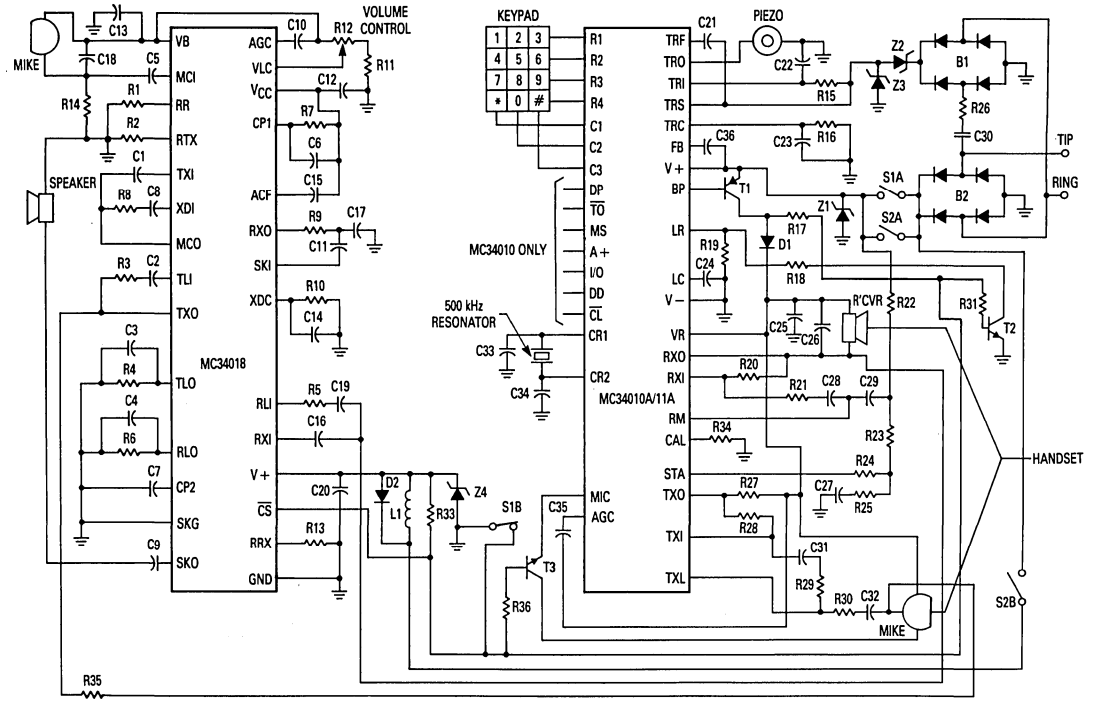
T1 — 2N4126
T2 — 2N2222A

B1 — 1N4004's
B2 — 1N4004's

S1 — DPDT (Hookswitch)
S2 — DPST (Speakerphone switch)

Handset R'cvr — 300 Ω
Handset Mike — Electret
Spkr'phone Speaker — 25 Ω, 0.3 W
Spkr'phone Mike — Electret

Figure 8. Handset/Handsfree System Using the MC34010/11 and MC34018



MC34010A/11A and MC34018
COMPONENT VALUES

R1 — 30 k
R2 — 91 k
R3 — 3.3 k
R4 — 1 M
R5 — 4.7 k
R6 — 1 M
R7 — 100 k
R8 — 4.7 k
R9 — 4.3 k
R10 — 200 k
R11 — 24 k
R12 — 20 k
R13 — 18 k
R14 — 2 k
R15 — 1.8 k
R16 — 200 k
R17 — 3 k
R18 — 100
R19 — 390
R20 — 200 k
R21 — 56 k
R22 — 150 k
R23 — 56 k
R24 — 1.5 k
R25 — 1.5 k
R26 — 6.8 k
R27 — 270
R28 — 200 k
R29 — 4.7 k
R30 — 4.7 k
R31 — 1 k
R33 — 47 k
R34 — 36
R35 — 33 k
R36 — 3 k

C1 — 0.1
C2 — 0.068
C3 — 2.2 μF
C4 — 2.2 μF
C5 — 0.1
C6 — 47 μF
C7 — 4.7 μF
C8 — 0.068
C9 — 47 μF
C10 — 1 μF
C11 — 0.05
C12 — 47 μF
C13 — 47 μF
C14 — 4.7 μF
C15 — 4.7 μF
C16 — 0.05
C17 — 0.01
C18 — 0.05
C19 — 0.1
C20 — 1000 μF
C21 — 1 μF
C22 — 4.7 μF
C23 — 620 pF
C24 — 0.1
C25 — 2.2 μF
C26 — 0.01
C27 — 0.1
C28 — 0.05
C29 — 0.05
C30 — 1 μF, NP
C31 — 0.1
C32 — 0.1
C33 — 100 pF
C34 — 100 pF
C35 — 1 μF
C36 — 0.1

L1 — 1 Hry, < 100 Ω

Z1 — 18 V
Z2 — 4.7 V
Z3 — 30 V
Z4 — 7 V

D1, D2 — 1N4001

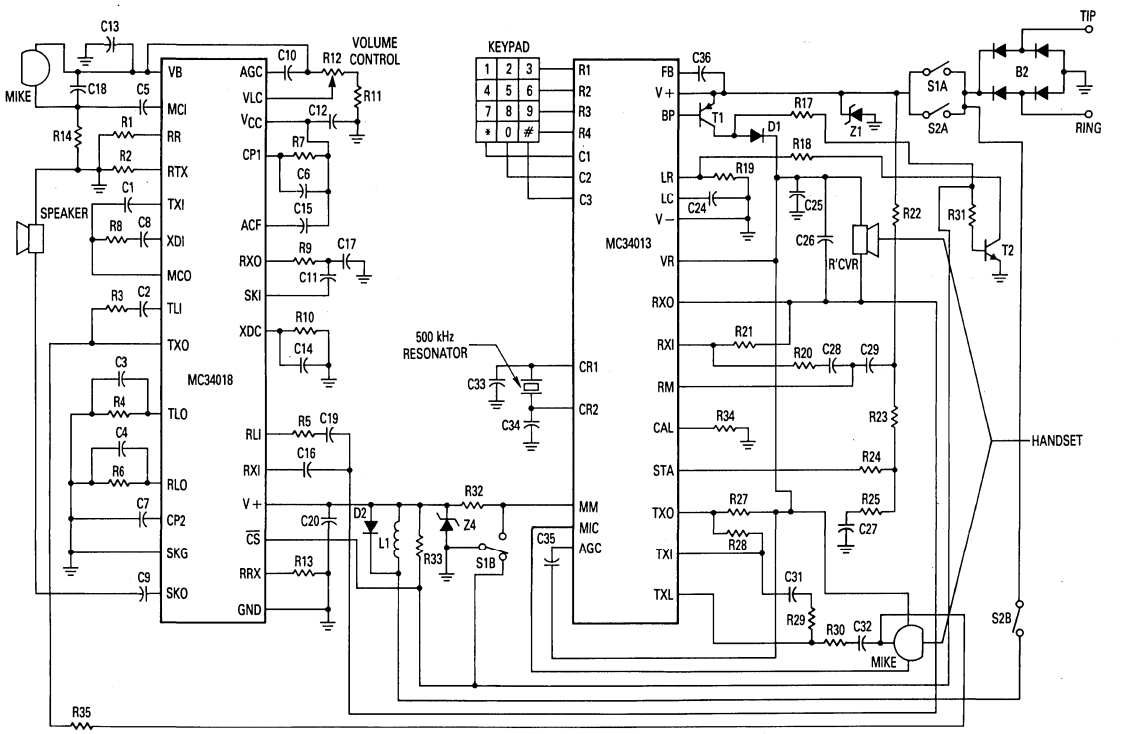
T1 — 2N4126
T2, T3 — 2N2222A

B1 — 1N4004's
B2 — 1N4004's

S1 — DPDT (Hookswitch)
S2 — DPST (Speakerphone switch)

Handset R'cvr — 300 Ω
Handset Mike — Electret
Spkr'phone Speaker — 25 Ω, 0.3 W
Spkr'phone Mike — Electret

Figure 9. Handset/Handsfree System Using the MC34010A/11A and MC34018



MC34013 and MC34018
COMPONENT VALUES

R1 — 30 k
R2 — 91 k
R3 — 3.3 k
R4 — 1 M
R5 — 4.7 k
R6 — 1 M
R7 — 100 k
R8 — 4.7 k
R9 — 4.3 k
R10 — 200 k
R11 — 24 k
R12 — 20 k
R13 — 18 k
R14 — 2 k
R17 — 1 k
R18 — 100
R19 — 390
R20 — 56 k
R21 — 200 k
R22 — 150 k
R23 — 56 k
R24 — 1.5 k
R25 — 1.5 k
R27 — 270
R28 — 200 k
R29 — 4.7 k
R30 — 4.7 k
R31 — 1.5 k
R32 — 51 k
R33 — 47 k
R34 — 36
R35 — 33 k

C1 — 0.1
C2 — 0.068
C3 — 2.2 μF
C4 — 2.2 μF
C5 — 0.1
C6 — 47 μF
C7 — 4.7 μF
C8 — 0.068
C9 — 47 μF
C10 — 1 μF
C11 — 0.05
C12 — 47 μF
C13 — 47 μF
C14 — 4.7 μF
C15 — 4.7 μF
C16 — 0.05
C17 — 0.01
C18 — 0.05
C19 — 0.1
C20 — 1000 μF
C24 — 0.1
C25 — 2.2 μF
C26 — 0.01
C27 — 0.1
C28 — 0.05
C29 — 0.05
C31 — 0.1
C32 — 0.1
C33 — 100 pF
C34 — 100 pF
C35 — 1 μF
C36 — 0.1

L1 — 1 Hry, < 100 Ω

Z1 — 18 V
Z4 — 7 V

D1, D2 — 1N4001

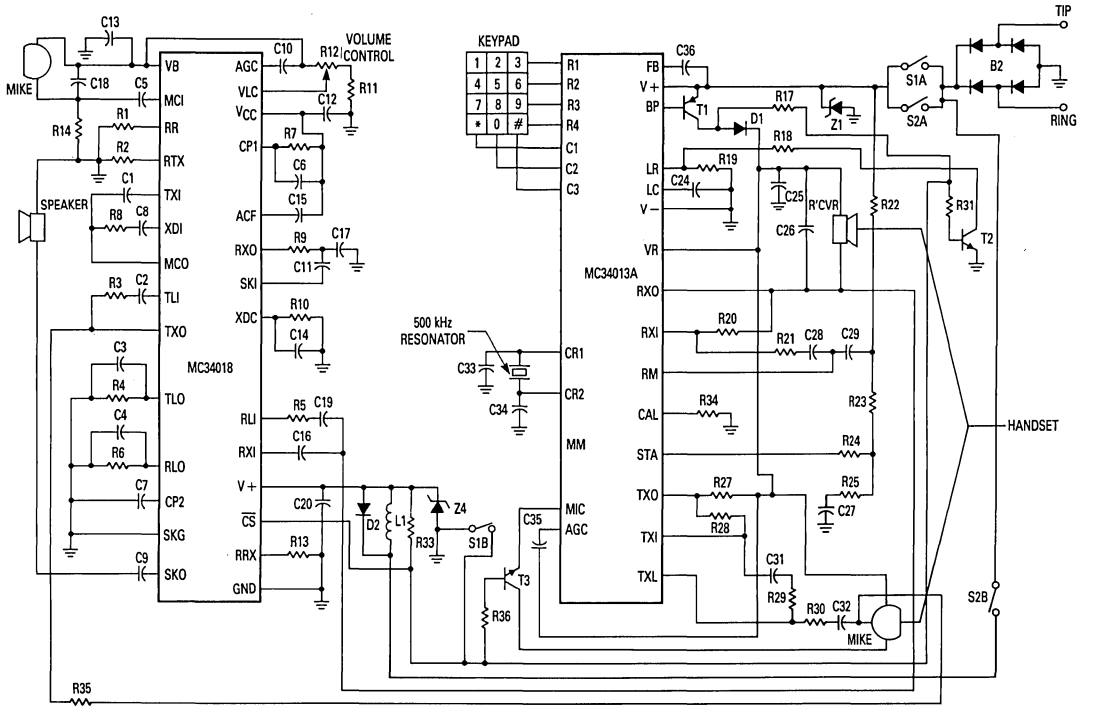
T1 — 2N4126
T2 — 2N2222A

B2 — 1N4004's

S1 — DPDT (Hookswitch)
S2 — DPST (Speakerphone switch)

Handset R'cvr — 300 Ω
Handset Mike — Electret
Spkr'phone Speaker — 25 Ω, 0.3 W
Spkr'phone Mike — Electret

Figure 10. Handset/Handsfree System Using the MC34013 and MC34018



MC34013A and MC34018 COMPONENT VALUES

R1 — 30 k
R2 — 91 k
R3 — 3.3 k
R4 — 1 M
R5 — 4.7 k
R6 — 1 M
R7 — 100 k
R8 — 4.7 k
R9 — 4.3 k
R10 — 200 k
R11 — 24 k
R12 — 20 k
R13 — 18 k
R14 — 2 k
R17 — 3 k
R18 — 100
R19 — 390
R20 — 56 k
R21 — 200 k
R22 — 150 k
R23 — 56 k
R24 — 1.5 k
R25 — 1.5 k
R27 — 270
R28 — 200 k
R29 — 4.7 k
R30 — 4.7 k
R31 — 1 k
R33 — 4.7 k
R34 — 36
R35 — 33 k
R36 — 3 k

C1 — 0.1
C2 — 0.068
C3 — 2.2 μF
C4 — 2.2 μF
C5 — 0.1
C6 — 47 μF
C7 — 4.7 μF
C8 — 0.068
C9 — 47 μF
C10 — 1 μF
C11 — 0.05
C12 — 47 μF
C13 — 47 μF
C14 — 4.7 μF
C15 — 4.7 μF
C16 — 0.05
C17 — 0.01
C18 — 0.05
C19 — 0.1
C20 — 1000 μF
C24 — 0.1
C25 — 2.2 μF
C26 — 0.01
C27 — 0.1
C28 — 0.05
C29 — 0.05
C31 — 0.1
C32 — 0.1
C33 — 100 pF
C34 — 100 pF
C35 — 1 μF
C36 — 0.1

L1 — 1 Hry, < 100 Ω

Z1 — 18 V
Z4 — 7 V

D1, D2 — 1N4001

T1 — 2N4126
T2, T3 — 2N2222A

B2 — 1N4004's

S1 — DPDT (Hookswitch)
S2 — DPST (Speakerphone switch)

Handset R'cvr — 300 Ω
Handset Mike — Electret
Spkr'phone Speaker — 25 Ω, 0.3 W
Spkr'phone Mike — Electret

Figure 11. Handset/Handsfree System Using the MC34013A and MC34018

CONCLUSION

Interfacing the MC34018 speakerphone circuit to the MC34010 series of speech networks has been shown to be simple and straightforward. The interface requires the addition of 2 diodes, 5 resistors, either 1 or 2 transistors (depending on the speech network), and one diode bridge for the tone ringer circuit in the MC34010(A) and the MC34011(A). Any existing MC34010 type circuit can be easily modified to accept the speakerphone circuit.

REFERENCES

MC34010 Data Sheet, Dec. 1983, Motorola, Inc.
MC34010A Data Sheet, May, 1985, Motorola, Inc.
MC34013 Data Sheet, Nov. 1983, Motorola, Inc.
MC34013A Data Sheet, Feb. 1985, Motorola, Inc.
MC34018 Data Sheet, Apr. 1985, Motorola, Inc.

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN958

Transmit Gain Adjustments For The MC34014 Speech Network

By
Scott Bader and Dennis Morgan
Bipolar Analog IC Division

INTRODUCTION

The MC34014 telephone speech network provides for direct connection to an electret microphone and to Tip and Ring. In between, the circuit provides gain, drive capability, and determination of the ac impedance for compatability with the telephone lines. Since different microphones have different sensitivity levels, different gain levels are required from the microphone to the Tip and Ring lines. This application note will discuss how to change the gain level to suit a particular microphone while not affecting the other circuit parameters.

CIRCUIT DESCRIPTION

Refer to Figure 1. The microphone is assumed to be an electret type, characterized by a high dynamic impedance. It is therefore considered to be an ac current source rather than a voltage source. If the microphone used has a dynamic impedance which is not high (compared to R_8), then the microphone must be modeled as a current source paralleled by its dynamic impedance. That impedance value must then be considered to be in parallel with R_8 in the following equations. The T_X amplifier has a fixed gain of -20, and the EQ amplifier gain varies from 0.25 to 0.75, depending on the loop current. Z_L is the line impedance. The transmit gain is defined as $V+/I_{mic}$ and is equal to:

$$\frac{V+}{I_{mic}} = \frac{R_6 \times Z_L \times A_{TX}}{(1 + R_6/R_A)R_9 + (A_{TX})\ (A_{EQ})\ (Z_L)}$$

where A_{TX} = gain of the transmit amplifier (20 V/V)
A_{EQ} = gain of the equalization amp. (0.25 to 0.75 V/V)
R_A = R_8//10 kΩ (10 kΩ = input impedance of Tx amp.)

The ac impedance of the circuit is defined as:

$$Zac = \frac{R_9\ (1 + R_6/R_A)}{(A_{TX})\ (A_{EQ})}$$

The receive gain (see data sheet for the equivalent circuit) is defined as:

$$Grx = \frac{R_4}{R_1} + \frac{(X_C//R_2)\ (A_{EQ})\ (A_{TXO})\ (A_{STA}) \times R_4}{((X_C//R_2) + R_3)\ (1 + R_6/R_A) \times R_2}$$

As can be seen from the above equations, changing R_6 while maintaining the R_6/R_A ratio constant will result in a transmit gain change (proportional to R_6) but will not affect the other parameters. For example, increasing R_8 and R_6 by a factor of 3 will increase the transmit gain by ≈10 dB.

Using the above procedure to increase the transmit gain results in increasing R_8, which supplies the bias current to the microphone. If the higher value of R_8 results in insufficient bias voltage at the microphone, then the alternate biasing scheme of Figure 2 should be used.

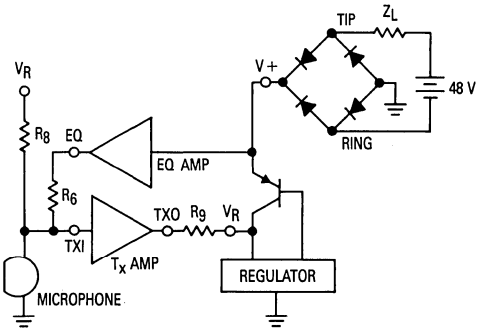


Figure 1. MC34014 Transmit Section

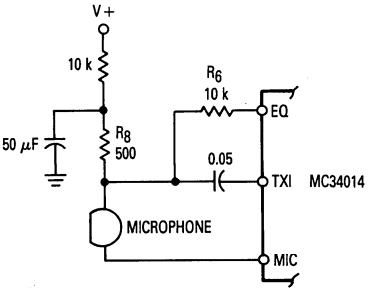


Figure 2. Alternate Biasing Scheme for Higher Voltage Microphones

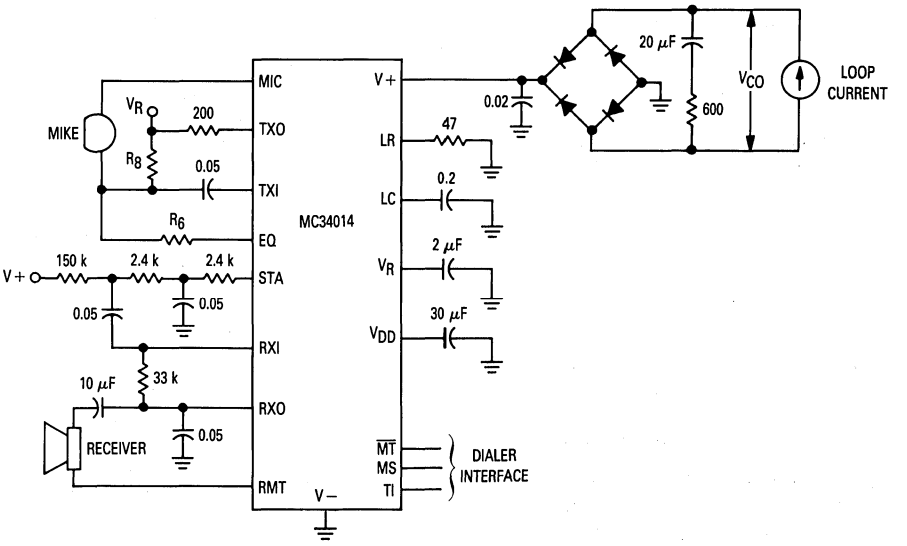
TEST RESULTS

Tests were conducted with a Primo EM-95A microphone, having a sensitivity of −53 dB ±3 dB (0 dB = 1 V/μbar), and a Hosiden KUC2123 microphone which has a sensitivity of −60 dB ±3 dB. The test circuit is shown in Figure 3. The tests consisted of applying a constant sound level to the microphones, and measuring the output at V_{CO}, while simulating line lengths of 0–21 Kfeet. The outputs of the two circuits were nearly identical at all line lengths.

CONCLUSION

Although the designs of the various parameters (transmit gain, receive gain, ac impedance, etc.) of the MC34014 speech network are not mutually exclusive due to the commonality of various components, it is possible to adjust the transmit gain independently to suit a particular microphone.

For further information on the MC34014 speech network, refer to the data sheet.



For Primo EM-95A microphone R_8 = 500 Ω, R_6 = 10 k
For Hosiden KUC2123 microphone R_8 = 1.5 k, R_6 = 30 k

Figure 3. Microphone Gain Test Circuit

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

A Speakerphone With Receive Idle Mode

By
Dennis Welty and Dennis Morgan
Bipolar Analog IC Division

INTRODUCTION

The MC34018 speakerphone system operates on the principle of comparing the transmit and receive signals to determine which is stronger, and then switching the circuit into that mode. Under conditions where noise from the telephone line (in the receive path) exceeds the background noise in the transmit path, the speakerphone will switch easily, or even lock, into the receive mode. Under these conditions the conversation will sound "dead" to the party at the far-end. It will also be more difficult for the near-end party to activate the transmit channel since the transmit detection is at the output of the transmit attenuator, which will be at maximum attenuation during this time. The addition of a receive idle mode can alleviate this problem by ensuring that the transmit and receive gains will be approximately equal when no voice signals are present. This allows the far-end party to hear ambient noises, and also increases the sensitivity to transmit signals.

CIRCUIT DESCRIPTION

The additional circuitry is shown in Figure 1. The receive signal normally applied to RXI also drives XDI through a 2.7 kΩ resistor and a 0.1 μF capacitor. XDC is connected to VLC through the NPN and PNP emitter followers. When voice signals in the receive channel exceed the background noise by 4.6 dB, XDC switches high and turns off the PNP transistor (the 4.6 dB threshold is built into the MC34018). The voltage at VLC is then determined by the volume control potentiometer. When voice signals are no longer present, XDC decays to 0.5 VB and turns on the emitter followers. The voltage at VLC is now determined by the voltage at XDC. By decreasing the VLC voltage with the emitter followers the transmit and receive gains are adjusted to produce a receive-idle mode.

A peak detector using an external voltage comparator and diode is required to hold the receive attenuator fully on (out of the idle mode) when constant level signals, such as dial tone, are intentionally presented to the re-

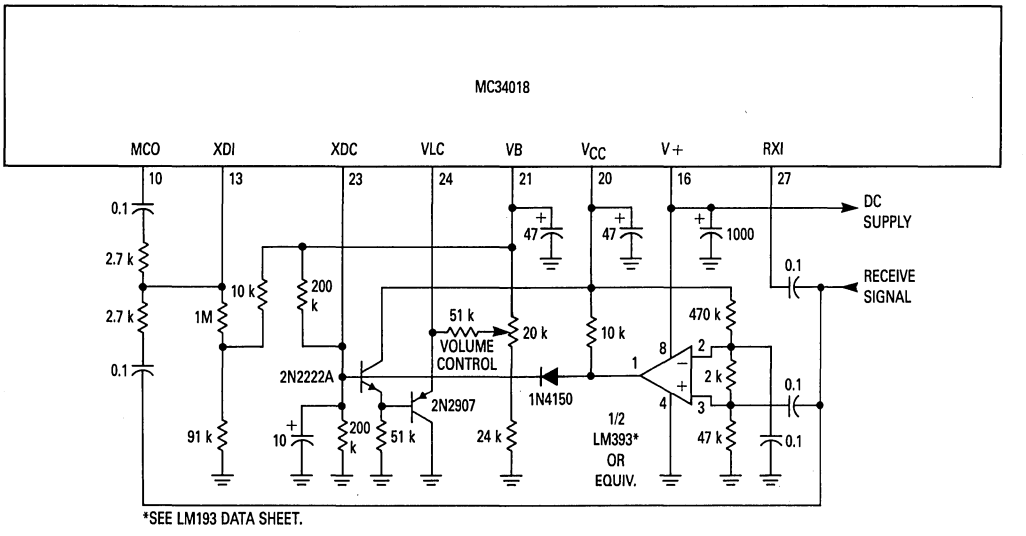


Figure 1. Receive-Idle Circuit

ceive channel. When the receive signal at the receive input exceeds the threshold on the comparator (typically 20 mV) the peak detector charges the capacitor at XDC which prevents the speakerphone from relaxing to the idle mode. The PNP transistor is turned off and the voltage at VLC is then determined by the volume control potentiometer. Under these conditions the speakerphone will be in the receive mode.

The sensitivity threshold of the voice detector circuitry can be changed by applying a dc current to XDI. The threshold current (nominally 250 nA) also prevents XDC from switching sporadically in quiet signal conditions. The threshold current is determined by the 1 Megohm resistor between XDI and the 10 kΩ/91 kΩ divider referenced to VB. Whenever receive signal currents exceed the threshold current by 4.6 dB, the voice detector will respond and allow XDC to switch high.

CONCLUSION

The receive-idle mode is simple to implement, and improves the performance of the speakerphone system by allowing noise rejection in both the receive and transmit channels. The voice-switching function operates only on valid speech, and ignores background noises.

REFERENCES

MC34018 data sheet, Motorola, 1985
LM193 data sheet, Motorola

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

Equalization of DTMF Signals Using the MC34014

by
Scott Bader and Dennis Morgan
Bipolar Analog IC Division

INTRODUCTION

This application note will describe how to obtain equalization (line length compensation) of the DTMF dialing tones using the MC34014 speech network. While the MC34014 does not have an internal dialer, it has the interface for a dialer so as to provide the means for putting the DTMF tones onto the Tip & Ring lines. The Equalization amplifier, whose gain varies with loop current, was meant primarily to equalize the speech signals. However, by adding one resistor, it can be used to equalize the DTMF signals as well.

CIRCUIT DESCRIPTION

Referring to Figure 1, the gain of the equalization amplifier varies with loop current as it is a function of the voltage at the LR pin (Pin 13). The gain varies from a minimum of −12 dB at low loop currents (long line), to −2.5 dB at high loop currents (short line). The output at EQ (Pin 6) is in phase with the signals going out onto Tip & Ring, but is out of phase with the DTMF input signals from the dialer at R7 (see Figure 2). Because of the out-of-phase relationship, the signal at EQ can be used to partially cancel the signals at the Tone Input (Pin 16). The addition of resistor R10 provides the path for this function, with the result that the DTMF gain increases as loop current decreases.

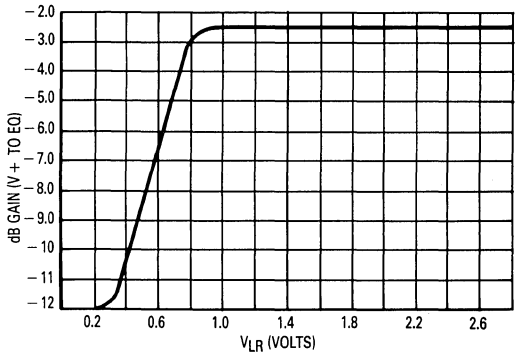


Figure 1. Equalization Amplifier Gain

Because the addition of R10 cancels some of the signal going into Pin 16, resistor R7 must be decreased in order to restore the overall gain from the dialer to Tip & Ring.

The DTMF gain values indicated in Figures 3 and 4 is the gain from the tone dialer (input at R7) to the Tip & Ring lines terminated with a 600 ohm resistor. Figure 3 indicates the gain CHANGE (as the loop current is varied from 60 to 20 mA) versus different values of R10. The gain change is a function of R10, and independent of R7. Figure 4 indicates the DTMF gain versus R7 for different values of R10 at a loop current of 20 mA.

Because the typical telephone line is not purely resistive, there will be a phase shift of other than 180° from the DTMF dialer to Tip & Ring in most applications. For this reason, the values of R10 and R7 will have to be adjusted slightly from those in the graphs to compensate for the phase shift.

The MC34014 data sheet mentions that a dc bias current of 20–50 μA is required into Pin 16 in order to bias the DTMF amplifier. The addition of R10 will provide the bias current from the EQ output for most applications, in which case it may be desirable to ac couple the dialer to R7 with a 0.5 μF capacitor. Excessive bias current will result in clipping of the signals at Tip & Ring. If just the addition of R10 results in excessive bias current, then the EQ output should be ac coupled to R10 with a 0.5 μF capacitor, and the bias current supplied either from the dialer or from an additional resistor as shown in Figure 5.

For further information on the MC34014, refer to its' data sheet.

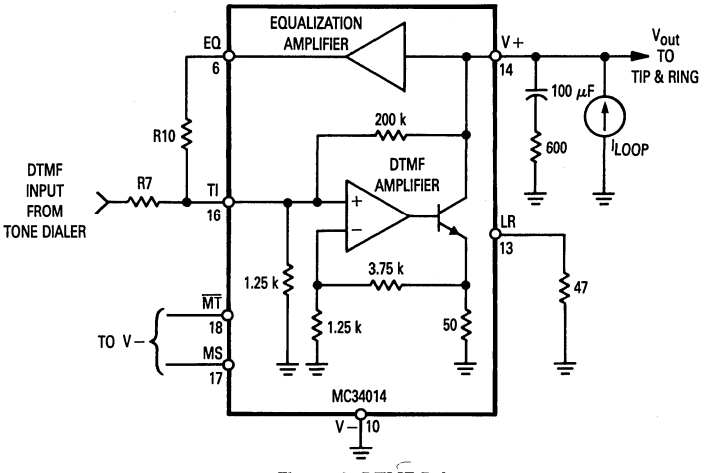


Figure 2. DTMF Driver

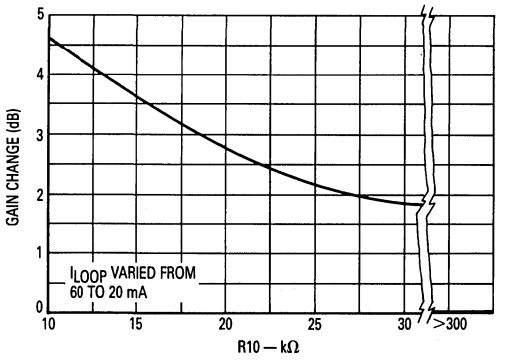


Figure 3. Gain Change

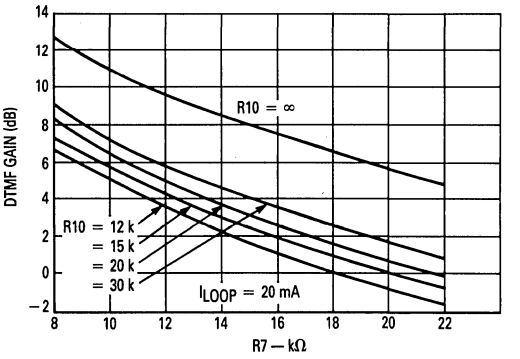


Figure 4. DTMF Gain

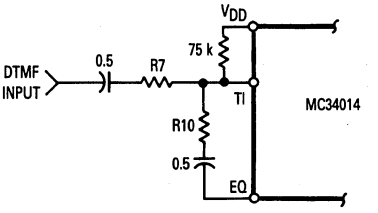


Figure 5. Alternate Biasing

AN1002

A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34018 Speakerphone ICs

Prepared by
Dennis Morgan
Bipolar Analog IC Division

INTRODUCTION

This application note describes the procedure for combining the MC34114 speech network with the MC34018 speakerphone circuit into a featurephone which includes the following functions: ten number memory pulse/tone dialer, tone ringer, a "Privacy" (Mike Mute) function, and line length compensation for both handset and speakerphone operation.

Three circuits are developed in this discussion: a line-powered featurephone, a line-powered featurephone with a booster (for using the speakerphone on long lines), and one powered from a power supply. The circuits are nearly identical, except for the Tip/Ring interface. Their performance, however, differs noticeably, particularly in the low loop current range. Initially, the discussion will focus on the line-powered circuit.

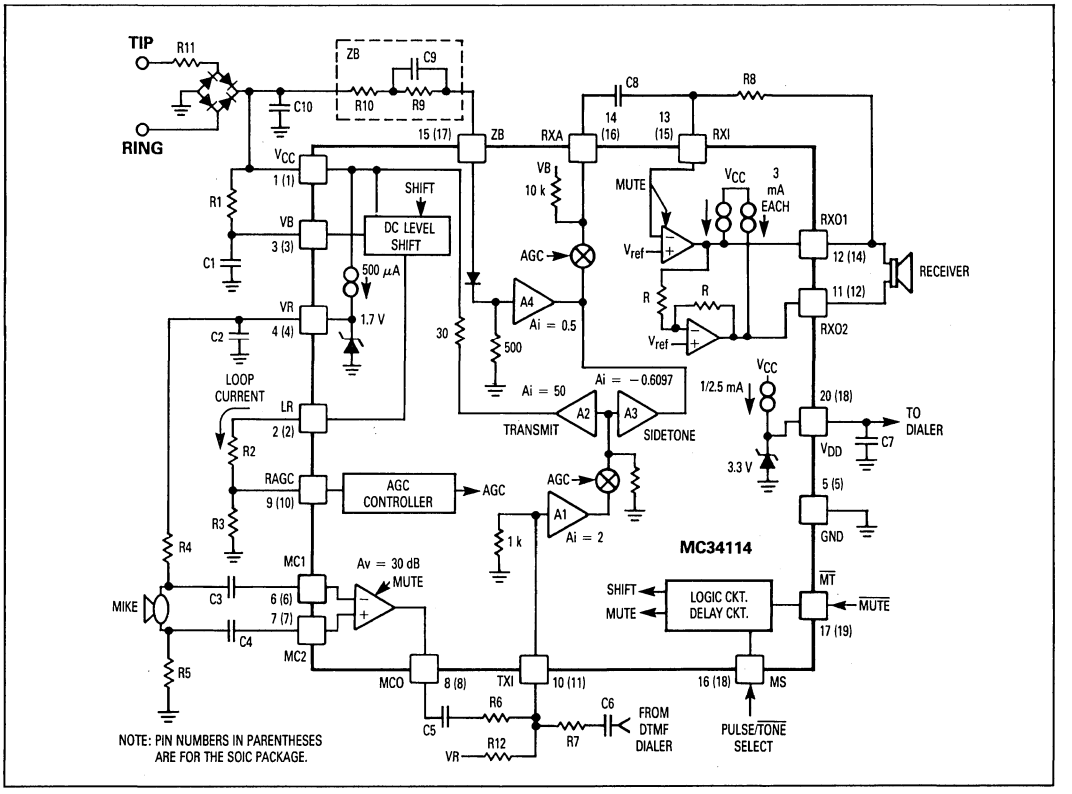


Figure 1. MC34114 Block Diagram

DESCRIPTION OF THE BUILDING BLOCKS

NOTE: Several pins on the ICs used in this application note have identical nomenclature (V_{CC}, VB, TXI, MS, V_{DD} and RXI). They provide separate functions, and are not to be connected together, unless so noted.

MC34114 Speech Network

The MC34114 is a speech network which interfaces with Tip & Ring and provides the 2-to-4 wire conversion (see Figure 1). The transmit gain is determined by the microphone amplifier (fixed gain of 30 dB), R6, C5, the internal current gains of A1, A2, the AGC, and the line impedance in parallel with R1. The receive gain is determined by ZB, the internal current gains of A4 and AGC, C8 and R8. The sidetone cancellation is determined by A3 and the ZB network. The AGC points have a current gain of 1 at low loop current, and decrease to 0.5 (−6 dB) at higher loop currents, thus providing line length compensation. R1 (typically 600 Ω) sets the circuit's terminating impedance for ac (return loss) purposes.

The $\overline{\text{MUTE}}$ input (when low) disables the microphone amplifier, and partially mutes the receive amplifier (with an internal 1 k feedback resistor), when dialing. DTMF dialing signals are injected at TXI through R7 and C6. The Mode Select (MS) input (when low, and $\overline{\text{MT}}$ is low) provides a voltage boost at V_{CC} to ensure adequate voltage during DTMF dialing at low loop currents. The 3.3 volt regulated output (V_{DD}) powers the dialer, and the 1.7 volt regulated output (VR) is used to bias the microphone.

The dc characteristics at Tip & Ring are determined by the diode bridge (1.4 volts), a level shift of approximately 2.9 volts from V_{CC} to LR, and the voltage across R2 + R3 (typically 43 Ω and 13 Ω). All the loop current, minus ≈10 mA, flows through those two resistors. The level shift (V_{CC} − LR) increases to ≈3.9 volts when both $\overline{\text{MUTE}}$ and MS are low (tone dialing mode). The voltage at RAGC, when within the range of 0.5 to 1 volt, controls the internal AGC as a function of loop current.

MC34018 Speakerphone

The MC34018 speakerphone IC (see Figure 2) provides all of the necessary functions for a complete speakerphone circuit in a single integrated circuit. Included are the transmit and receive attenuators, which operate in a complementary manner, to provide the necessary half-duplex function. The two level detectors, in conjunction with the background noise monitor and control algorithm, provide a two point sensing and decision making system to control the attenuators based on the levels and timing of the transmit and receive signals. Additional functions include the microphone amplifier, speaker amplifier, volume control for the receive path, and a chip select pin. The gain of the speaker amplifier, normally +34 dB, is reduced by the AGC circuit in the presence of strong signals to prevent clipping at SKO. The component values shown are typical.

Connections to the speakerphone circuit are made to the four points at the right end of Figure 2 (Receive Input, DC Supply, Chip Select, & Transmit Output).

The DC supply requires 4 to 11 volts dc, and it must be well filtered to prevent oscillations when the speaker amp is operating. In a typical line powered circuit, an inductor (1H) is used, in conjunction with the 1000 μF capacitor shown, to filter the voltage derived from the loop current.

The Receive Input of Figure 2 is derived from the 4-wire side of the speech network. The gain from RXI to the speaker is +40 dB when in the receive mode at maximum volume (+6 dB in the attenuator, +34 dB in the speaker amp). At minimum volume, the attenuator's gain reduces by ≈30 dB, for an overall gain of +10 dB. In the transmit mode, the receive gain is ≈−4 dB.

The transmit gain, from the microphone to Transmit Output, is +40 dB (+34 dB in the mike amp, +6 dB in the attenuator), and does not vary with the volume control. In the receive mode, the transmit gain is ≈−4 dB. The Transmit Output will connect to the 4-wire side of the speech network.

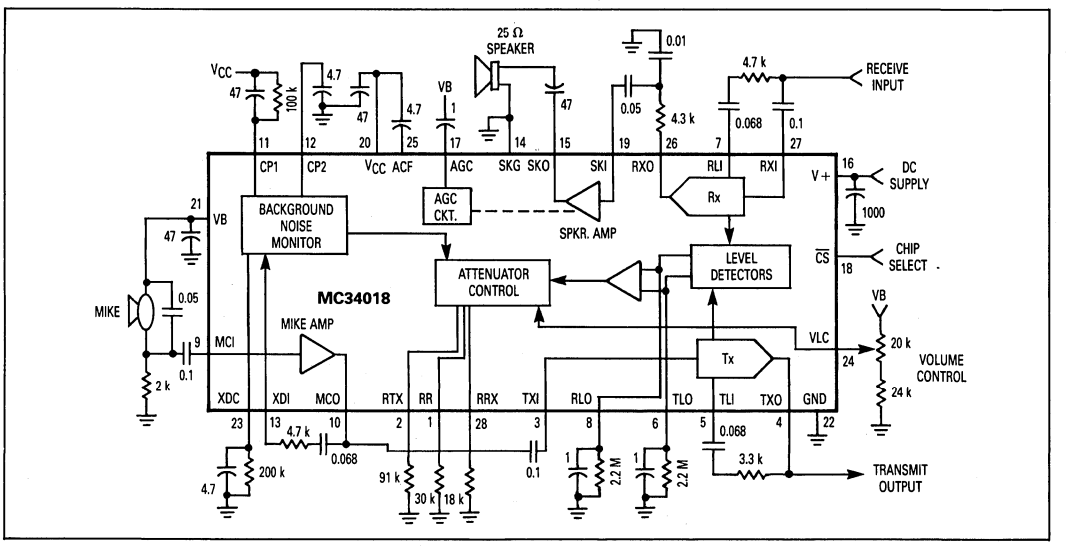


Figure 2. MC34018 Block Diagram

The overall speakerphone's transmit and receive gains to/from Tip & Ring will be adjusted at the interface from Figure 2 to the speech network.

Chip Select enables the MC34018 when at a logic low. The MC34018's supply current is normally ≈5 mA. When $\overline{CS}$ is taken higher than 1.6 volts, the IC is disabled, and the supply current drops to ≈500 μA.

V_{CC} (Pin 20) is a regulated 5.4 volt output, and VB (Pin 21) is a regulated 2.9 volt output. VB is typically used to bias the microphone.

MC145412 Dialer

The dialer is a pulse/tone dialer with 10 number memory, including last number redial (Figure 3). The pulse and tone functions are selectable by Pin 10 (MS). The circuit uses a standard 3.58 MHz crystal, and a standard 3x4 or 4x4 keypad.

The NPN transistor at Pin 12 indicates the on-hook/off-hook status to the IC. Power for the dialer is the MC34114's V_{DD} (3.3 volts), diode connected with a memory sustaining battery. The DTMF output goes to C6/R7 of Figure 1, which sets the gain.

The $\overline{OPL}$ ($\overline{OUTPULSING}$) pin is used to interrupt the loop current when pulse dialing. The pin is active low, open drain. TSO (Tone Signal Output) provides a pacifier tone during pulse dialing. The tone is a 500 Hz square wave, which swing from V_{DD} to V_{SS}.

The $\overline{Mute\ Output}$ ($\overline{MO}$) is active low, open drain, and pulls to ground while dialing. It is used to mute the speech paths during dialing.

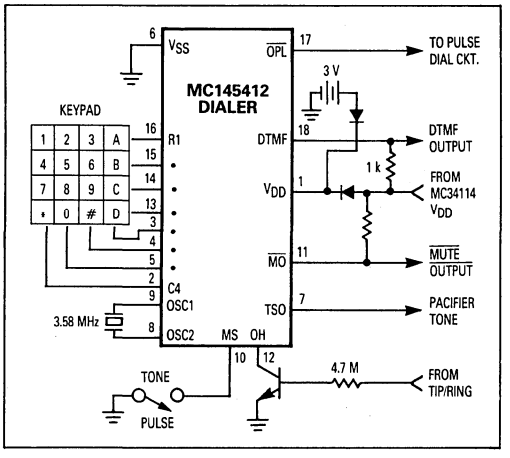


Figure 3. Pulse/Tone Dialer

SWITCHING THE CIRCUIT AROUND

The logic functions involve: a) switching the circuit from handset mode to/from speakerphone mode, b) switching in and out of either dialing mode while in either handset or speakerphone mode, and c) muting the two microphones for the "Privacy" function. Table 1 tabulates the fundamental requirements applicable to any featurephone:

Table 1.

Function	HANDSET		SPEAKERPHONE	
	Mike	R'cvr	Mike	Speaker
Handset Speech	On	On	Off	Off
Handset Dialing	Off	Mute	Off	Off
Handset Mike Mute	Off	On	Off	Off
Speakerphone Speech	Off	Off	On	On
Speakerphone Dialing	Off	Off	Off	Mute
Speakerphone Mike Mute	Off	Off	Off	On

In Table 1, "ON" means fully functional, "OFF" means non-functional, and "MUTE" means partially muted (10 to 20 dB). To apply Table 1 to the specific ICs described above, the requirements are expanded as follows:

Table 2.

Function	MC34114 $\overline{MT}$	MC34114 MS	MC34018 $\overline{CS}$	Loop Current	MC145412 MS
Handset Speech	Hi	X	Hi	Thru MC34114	X
Handset Pulse Dialing	Lo	Hi	Hi	Thru MC34114	Open
Handset Tone Dialing	Lo	Lo	Hi	Thru MC34114	Gnd
Handset Mike Mute	Lo	X	Hi	Thru MC34114	X
Speakerphone Speech	Lo	X	Lo	To MC34018	X
Speakerphone Pulse Dialing	Lo	Hi	Lo	To MC34018	Open
Speakerphone Tone Dialing	Lo	Lo	Lo	To MC34018	Gnd
Speakerphone Mike Mute	Lo	X	Lo	To MC34018	X

X = Don't Care

A summary of Table 2 is:

a) The MC34114 speech network is put into the Mute mode ($\overline{MT}$ = Lo) not only for dialing, but also to mute the microphone and receiver for the Privacy function (Mike Mute), and when in the speakerphone mode.
b) The MC34018 is disabled for all the handset functions, and enabled for all the speakerphone functions.
c) The loop current, which normally flows through the LR pin of the MC34114 (see Figure 1), is directed instead to the MC34018 in the speakerphone mode so as to make the power available to the speaker.
d) The MS pins of the dialer, and of the MC34114, are significant only during dialing.

PUTTING IT ALL TOGETHER

Switching Between Handset and Speakerphone Modes

To switch between modes, two actions are necessary: 1) Divert the excess loop current, which normally flows through the MC34114, to the MC34018 during speakerphone mode, and 2) enable and disable the speech network and speakerphone circuits appropriately. The circuit of Figure 4 fullfills those requirements:

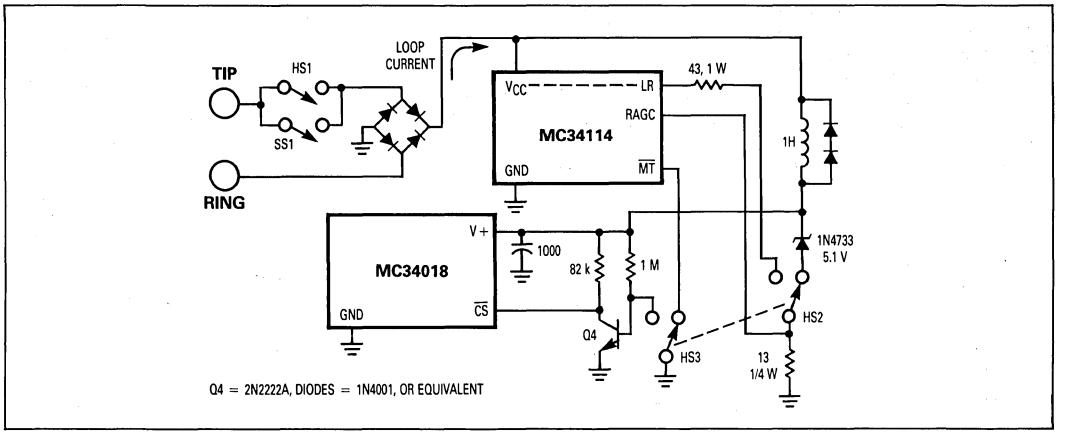


Figure 4. Switching Between Modes

HS (3 poles) is the hookswitch operated by lifting the handset. SS (1 pole) activates the speakerphone when the handset is on-hook. The switches are shown on-hook in Figure 4.

If the handset is lifted (HS transfers), the MC34114 consumes ≈10 mA internally, and the excess loop current flows out of the LR pin and through the 43 Ω and 13 Ω resistors. The voltage across the 13 Ω resistor controls the AGC function. The configuration in this position is similar to that of Figure 1. Additionally, Q4 is off, allowing $\overline{CS}$ to be pulled high, disabling the MC34018.

If the handset is on-hook, and switch SS is closed, the MC34114 still consumes ≈10 mA internally, but the excess loop current now flows through the 1 Henry choke, the zener diode, and the 13 Ω resistor. The voltage across the 13 Ω resistor still controls the AGC function of the MC34114. The MC34018's $\overline{CS}$ is held low by Q4, enabling the speakerphone, and the MC34114's $\overline{MT}$ is low, muting its microphone and receive amplifiers. If the handset is lifted while the speakerphone is in operation, the circuit reverts to the handset mode.

It may appear that $\overline{CS}$ and $\overline{MT}$ could be connected together and to HS3 to provide the same functions, thereby eliminating Q4. The fact, however, that other parts of the circuit will be connected to $\overline{MT}$ in subsequent sections of this application note negates that possibility.

Joining the Receive Paths

Refering to Figure 1, receive signals arriving at Tip & Ring generate a current through the ZB network, into Pin 15. That current is modified by A4, the AGC, made available (as a current) at RXA, and coupled to RXI, where it is converted to a voltage by the receive amplifiers and R8. The ZB network is typically 12 kΩ, and R8 is typically 3.9 kΩ. The receive gain to the handset receiver is therefore nominally −10 dB at low loop currents.

To feed the receive signals to the speakerphone, the circuit of Figure 5 is used.

The current out of RXA is now split (by the 1 kΩ resistors) so that approximately half goes to RXI (of the MC34114) via C8, and the other half is converted to a voltage (by the op amp) for the speakerphone's Receive Input (Figure 2). The MC33171 was chosen for its very low supply current (typically 180 μA). The op amp is powered from the MC34018's V_{CC} output (5.4 volts), and biased by the MC34018's VB (2.9 volts). The receive gain for the speakerphone is determined by the following equation:

$$G_{RX} = 20 \log \left(\frac{R_{RSP} \times A4 \times AGC \times 0.5}{ZB + 500\ \Omega} \right) + 40\ dB$$

The terms A4, ZB, and AGC (from Figure 1) are set at 0.5, 12 kΩ, and 1 respectively for low loop currents. The 0.5 in the above equation is due to the current splitting of Figure 5, and the +40 dB is the gain of the MC34018's receive attenuator and speaker amp. For a nominal overall gain of +30 dB, R_{RSP} calculates to ≈18 kΩ. At higher loop currents, the overall gain will be ≈ +24 dB. The above equation assumes the volume control is set to maximum.

To compensate for the reduced current going to the MC34114's receive amplifiers, R8 (Figure 1) is increased to 8.2 kΩ.

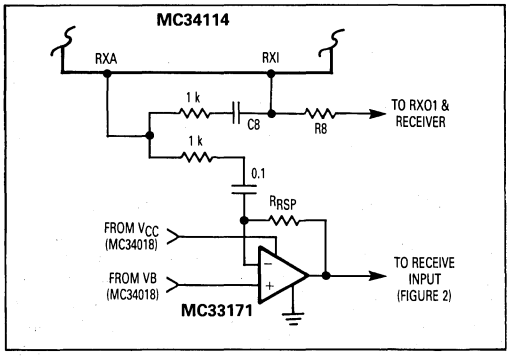


Figure 5. Joining the Receive Paths

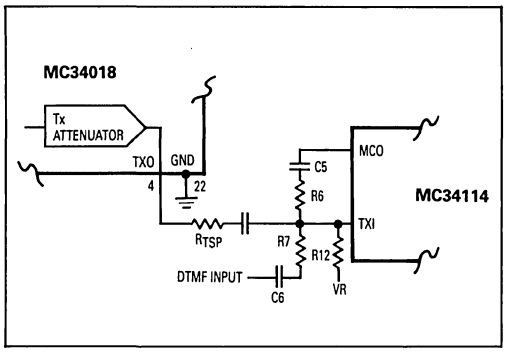


Figure 6. Joining the Transmit Paths

Joining the Transmit Paths

In the transmit path of Figure 1, the microphone signals are gained up by 30 dB by the mike amplifier. The output at MCO creates a current into TXI through R6 and C5. That current is gained up by 100 by A1 and A2 (assume AGC = 1), and A2's output current then acts on the parallel combination of R1 and the line's ac impedance. Typical values are: R6 = 15 kΩ, R1 = 600 Ω, and 600 Ω for the line's impedance. Neglecting the slight loading of R7, R12, and ZB, the overall handset transmit gain is ≈+36 dB at low loop currents.

The transmit output (voltage signals) from the speakerphone circuit (Figure 2) is applied to the speech network at TXI (a current input) in Figure 1, through a resistor (R_{TSP}) and a coupling capacitor (see Figure 6). For a nominal gain of +44 dB (from the microphone to the MC34114's V_{CC}), R_{TSP} calculates to be ≈18 kΩ. The coupling capacitor (nominally 0.1 μF) can be varied to set the low frequency rolloff.

Fitting in the Dialer and Another Switch

The Mute Output of Figure 3 must mute three items: 1) The MC34114 by pulling its $\overline{MT}$ pin low, 2) the MC34018's transmit path, and 3) the MC34018's receive path. This is accomplished with the circuit of Figure 7:

During dialing, Q1–Q3 are turned on by the dialer. Q1 mutes the MC34114, which shuts off its microphone amplifier, and mutes the receive amplifier by ≈27 dB. To mute the speakerphone's transmit path, R_{TSP} (of Figure 6) is divided into two resistors, and the junction pulled low by Q2, providing ≈35 dB muting of TXO's signal. Since the MC34018 will switch to the receive mode during DTMF dialing, the transmit attenuator will provide an additional muting of 44 dB, for a total of ≈79 dB. The speakerphone's receive path is muted by reducing the effective resistance at RRX (MC34018's Pin 28) from 18 kΩ to ≈3.7 kΩ with Q3. From Figure 3 of the MC34018's data sheet, the receive attenuator's gain is reduced by ≈23 dB. The 1 μF capacitor on Q3 softens any "pops" in the speaker when switching out of muting.

The DTMF output in Figure 3 is simply connected to C6/R7 of Figure 1 (or Figure 6) to get the DTMF signals to Tip & Ring. Using 24 kΩ for R7, and 0.1 μF for C6, DTMF levels of ≈−3.8 dBm will result at Tip & Ring.

For pulse dialing, Pin 17 of the MC145412 dialer ($\overline{OPL}$) is connected to a standard two transistor network to interrupt the loop current (Figure 8). The 12 volt zener diode protects the circuitry from voltage spikes during pulse dialing, and whenever a hook switch is opened.

The TSO output (pacifier tone), which is generated only when a keypad button is depressed in the pulse dialing mode, is injected to the MC34114's ZB pin so as to make it available to both the handset receiver and the speakerphone. This tone is not generated during DTMF dialing.

To select between pulse and tone dialing modes, the switch on the dialer's Pin 10 (Figure 3) is connected to the MC34114's MS pin (Pin 16). Since the MC34114's MS pin requires a pull-up resistor for a logic high, a diode must be added (Figure 8) so the dialer's MS pin is open when the switch is in the pulse position.

Switching in Some Privacy

The Privacy function (Mike Mute of Tables 1 and 2) requires only a 2 pole switch. One pole mutes the MC34114 to disable its microphone amplifier. The other pole is wired directly across the speakerphone's microphone.

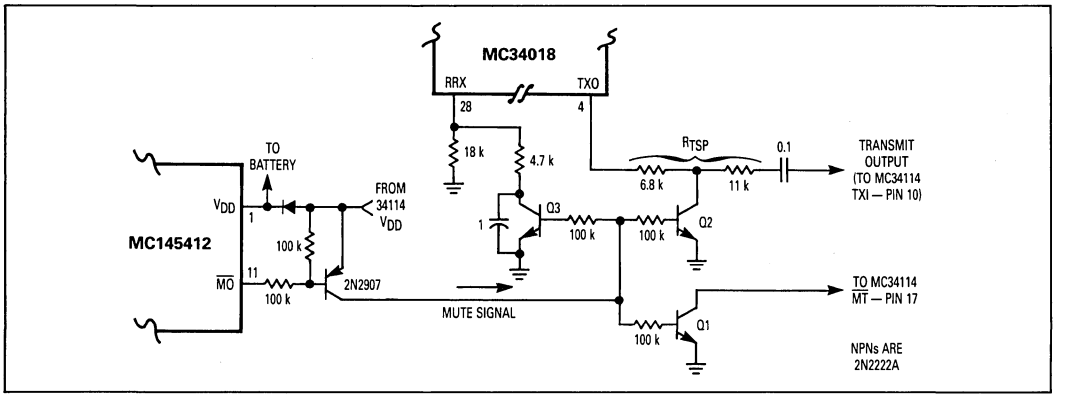


Figure 7. Muting Circuit

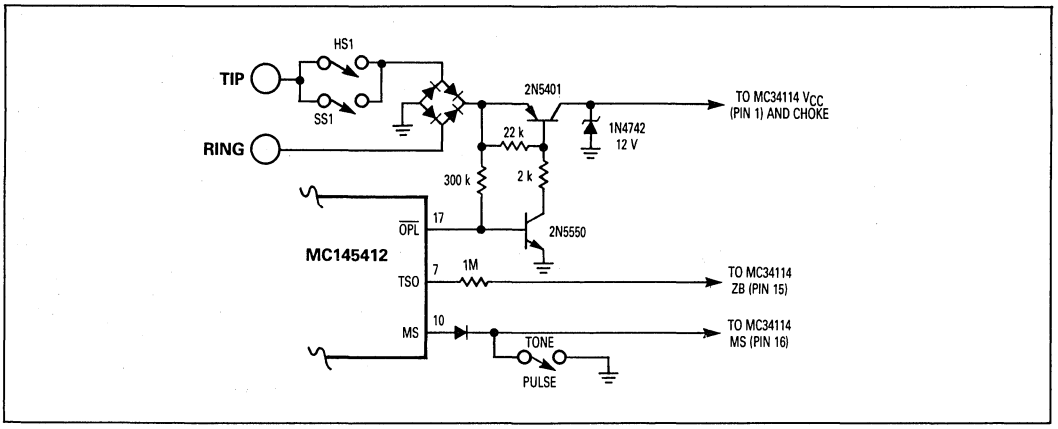


Figure 8. Pulse Dialing Circuit

Adding the Tone Ringer

The MC34017 tone ringer circuit, shown in Figure 9, is added to the circuit by simply connecting it directly across Tip & Ring. It is not necessary to disconnect the tone ringer when off-hook. This circuit will provide a ringer with an REN of ≈0.5, and meet all the EIA-470 and Bell system requirements for impedance, anti-bell tapping, and turn-on/off thresholds.

Finally, the Complete Circuit

The complete line-powered featurephone is shown in Figure 10. The performance curves for this circuit are shown in Figures 11–16. The "Speaker Amp Max Output Swing" is the maximum rms voltage available at the speaker amp output (Pin 15) of the MC34018 (its internal AGC circuit limits the maximum output to prevent clipping). The transmit gain tests involved replacing each microphone with a signal generator, and adjusting for a level of approximately −11 dBm at Tip & Ring into a 600 Ω resistive load. The receive tests involve applying approximately −27 dBm to Tip & Ring, and measuring the gain to the receiver or speaker.

As can be seen in Figure 12, the maximum available speaker power is a function of the loop current since all of the speaker current must come from the loop. Consequently, the receive gain for the speakerphone (Figure 15) shows a marked decrease at low loop currents. It must be remembered that in a line powered speakerphone, as the speaker draws current in response to a receive signal, the voltage at Tip & Ring decreases quickly. As the MC34018's V+ falls with the Tip & Ring voltage, the speaker amp's output capability is reduced. Consequently, a 25 Ω speaker is recommended for a line powered speakerphone as this makes the best use of the power available from the phone line. A lower impedance speaker will require more current, causing V+ to sag further for a given signal level. A higher impedance speaker draws less current, but produces less sound power.

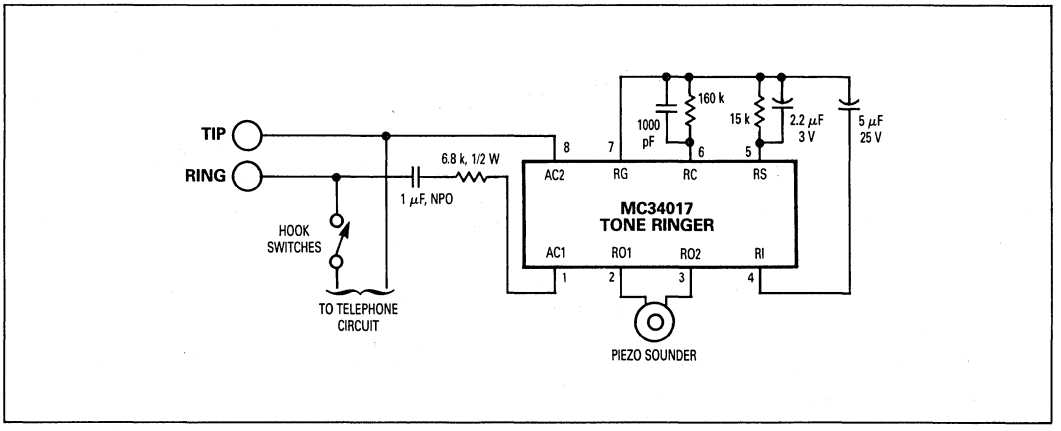
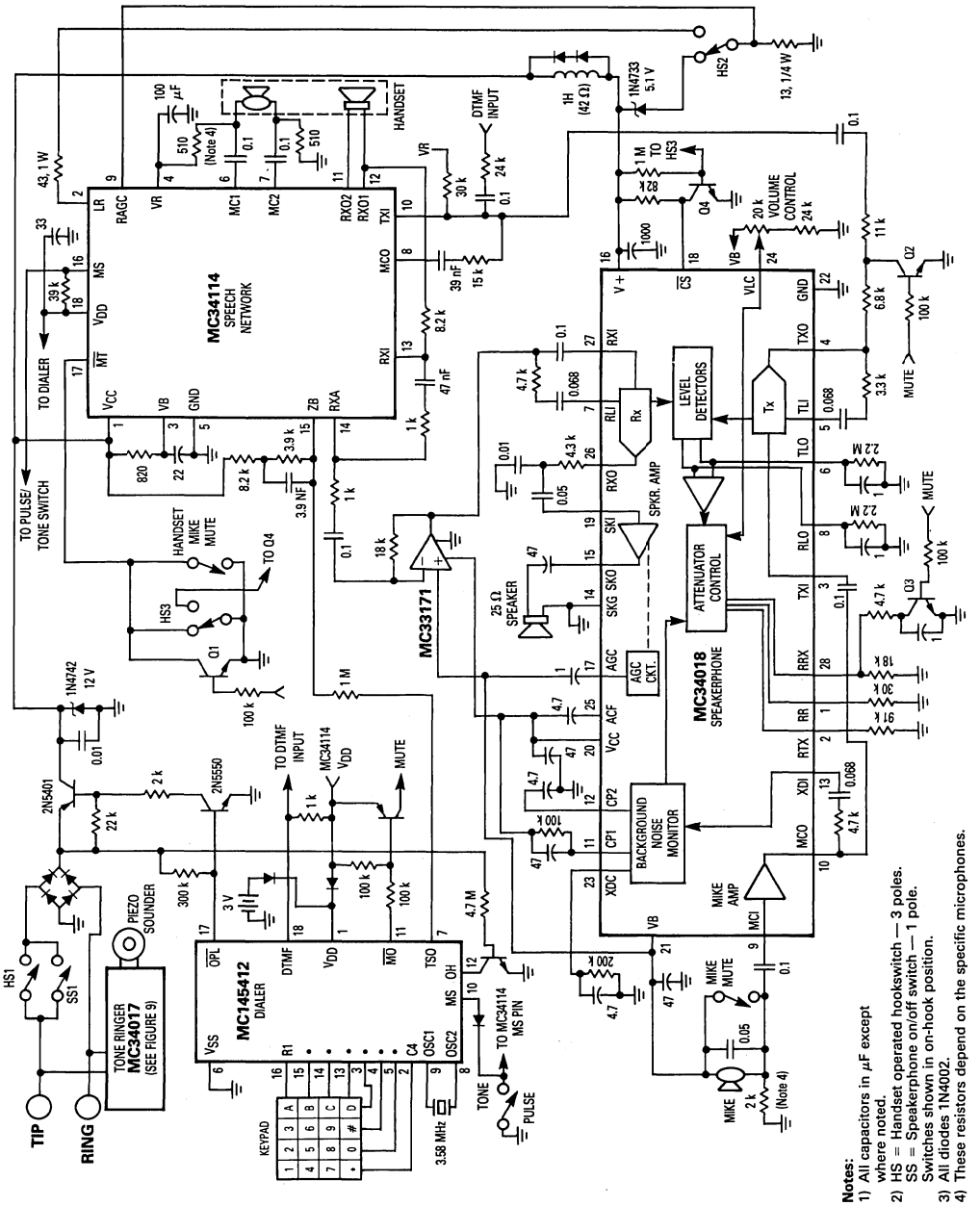


Figure 9. Tone Ringer Circuit

Additionally, the following muting specs apply:

1) **Handset microphone:** ≈62 dB while dialing, in speakerphone mode, or when Mike mute switch is closed.
2) **Speakerphone microphone:** ≈35 dB while dialing, plus an additional 44 dB due to the MC34018 switching to the receive mode. >60 dB while in the handset mode, or when the Mike mute switch is closed.
3) **Handset receiver:** ≈27 dB while dialing, or when in the speakerphone mode.
4) **Speaker:** ≈23 dB while dialing, >100 dB when in handset mode.



Notes:
1) All capacitors in μF except where noted.
2) HS = Handset operated hookswitch — 3 poles.
SS = Speakerphone on/off switch — 1 pole.
Switches shown in on-hook position.
3) All diodes 1N4002.
4) These resistors depend on the specific microphones.

Figure 10. Pulse/Tone Featurephone w/Memory — Line Powered

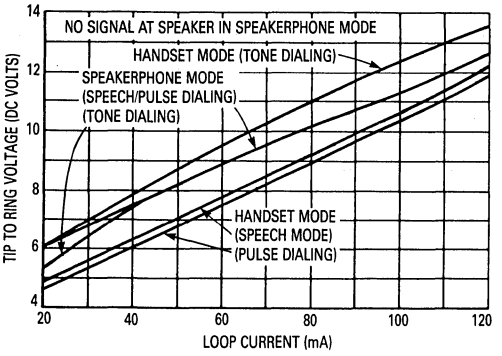


Figure 11. Tip to Ring DC Voltage versus Loop Current

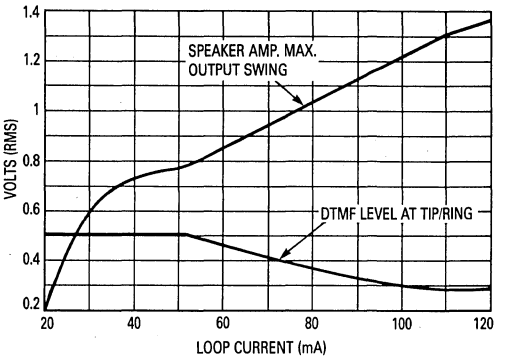


Figure 12. Speaker Amplifier Output and DTMF Level versus Loop Current

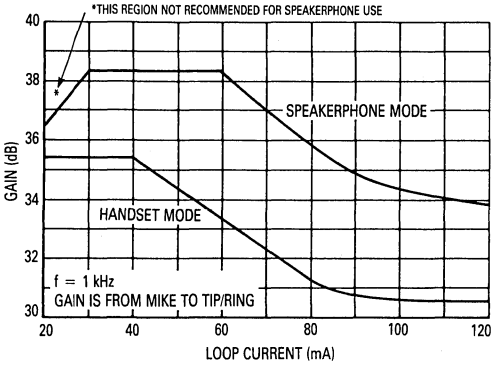


Figure 13. Transmit Gain versus Loop Current

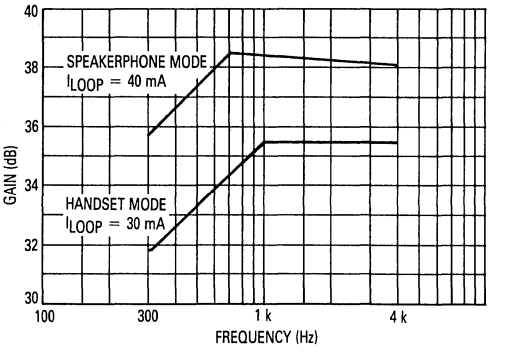


Figure 14. Transmit Gain versus Frequency

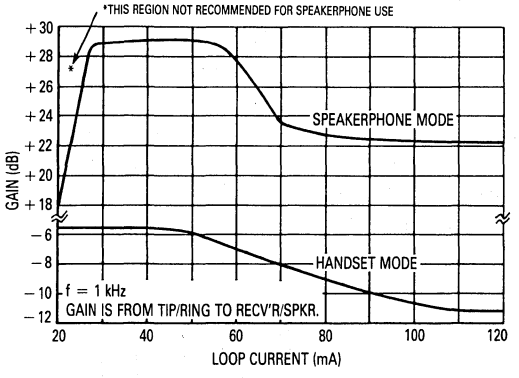


Figure 15. Receive Gain versus Loop Current

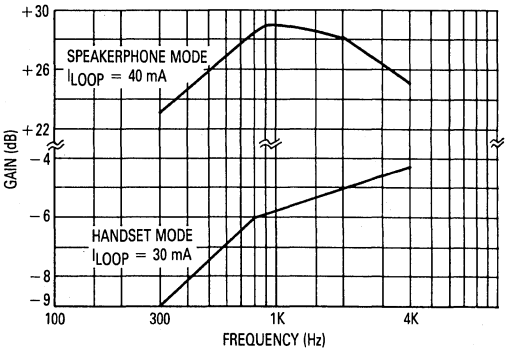


Figure 16. Receive Gain versus Frequency

BOOSTING THE SPEAKERPHONE AT LOW LOOP CURRENTS

Adding a Booster

To improve the performance of the speakerphone at low loop currents (below 30 mA), a minimal cost approach is to add an optional booster to the power supply portion of the MC34018. The approach in this application note is to use a wall mount transformer, similar to calculator chargers. A 9 volt ac Adapter, Radio Shack model #273-1455A, which contains the diode bridge and filter capacitor, was used to minimize the additional circuitry within the speakerphone itself. Since this particular ac adapter is specified for use with Radio Shack's speakerphones (model Duofone 102), it is this author's assumption that it complies with applicable FCC specifications, although that is not so stated on the transformer.

This application does not require a regulated voltage from the ac adapter, which further simplifies the design. The circuit of Figure 17 adds the ac adapter to the circuit of Figure 10:

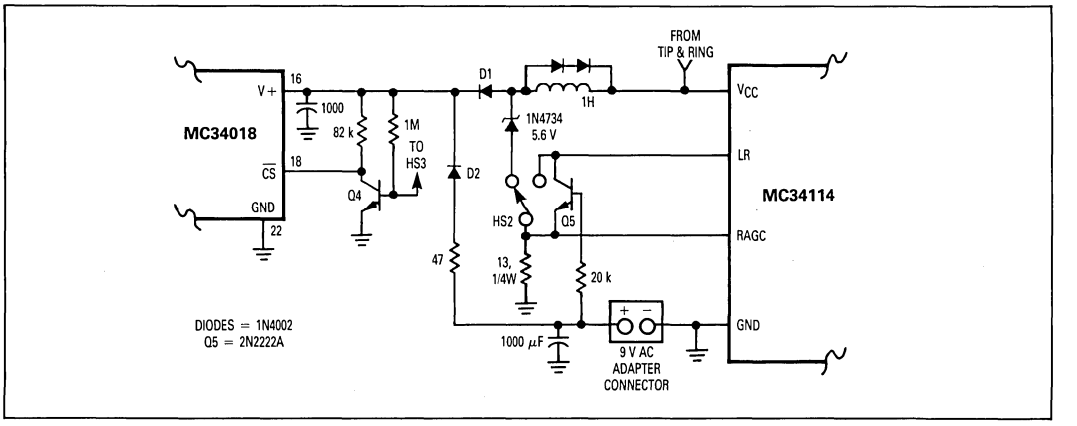


Figure 17. Adding a Speakerphone Booster

The circuit is the same as in Figure 10, but with the addition of Q5, the 20 k and 47 Ω resistors, 2 diodes, the 1000 μF capacitor, and the power supply connector for the ac adapter. The zener diode is changed to 5.6 volts to provide slightly more voltage to the MC34018 when the ac adapter is not used (at higher loop currents). The 47 Ω resistor provides short circuit protection for the ac adapter, and also aids in filtering 60 Hz ripple from the MC34018.

At low loop currents, and with the adapter plugged in, and the circuit in the speakerphone mode (HS2 as shown in Figure 17), D1 is reverse biased by the adapter's higher voltage. All of the speakerphone's current is now supplied by the ac adapter. Q5 is on, allowing the excess loop current to flow through the MC34114's LR pin. The dc characteristics at Tip & Ring are similar for the handset mode and the speakerphone mode.

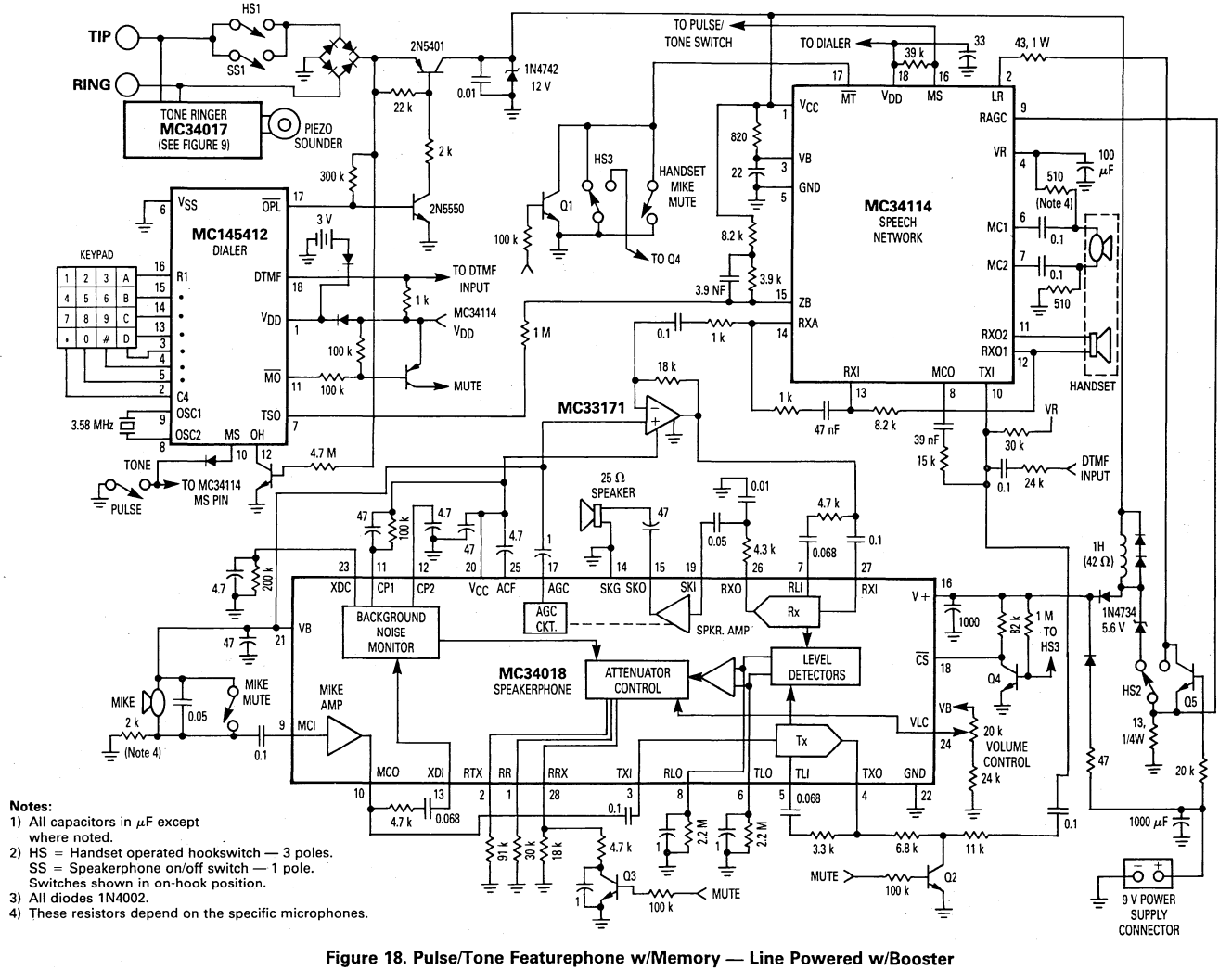
At higher loop currents, the dc characteristics of the two modes will differ slightly as some of the MC34018's current may be supplied by the loop.

Without the adapter plugged in, the circuit will act the same as that of Figure 10. Diode D2 prevents Q5 from being turned on.

In the handset mode, the circuit operates the same as that in Figure 10 when it is in the handset mode.

The Complete Circuit with the Booster

The complete circuit is shown in Figure 18. A quick comparison shows it is identical to that of Figure 10, except for the booster section in the lower right hand corner. The performance curves for this circuit are shown in Figures 19–24. As can be seen in Figures 20 and 23, the speakerphone's performance does not degrade below 30 mA as had happened in Figures 12 and 15. The muting specs for this circuit are the same as for Figure 10.



Notes:
1) All capacitors in µF except where noted.
2) HS = Handset operated hookswitch — 3 poles.
   SS = Speakerphone on/off switch — 1 pole.
   Switches shown in on-hook position.
3) All diodes 1N4002.
4) These resistors depend on the specific microphones.

Figure 18. Pulse/Tone Featurephone w/Memory — Line Powered w/Booster

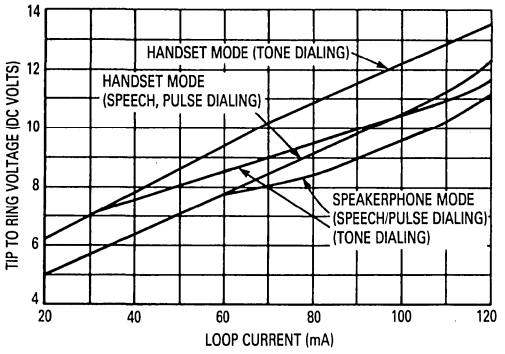


Figure 19. Tip to Ring DC Voltage versus Loop Current

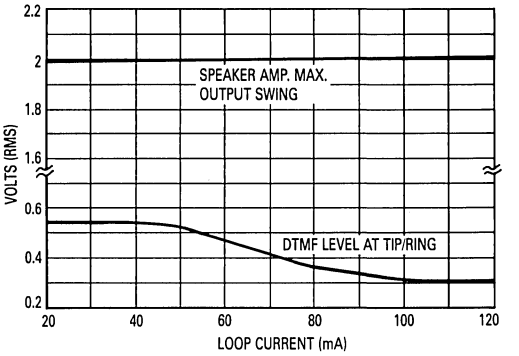


Figure 20. Max. Speaker Amplifier Output and DTMF Level versus Loop Current

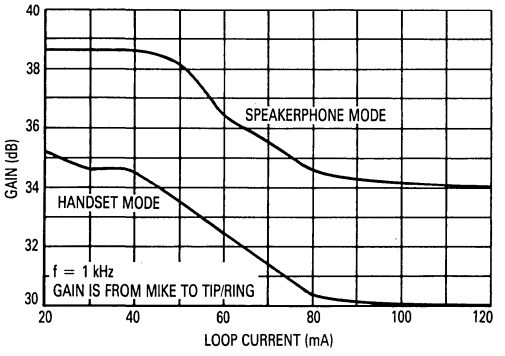


Figure 21. Transmit Gain versus Loop Current

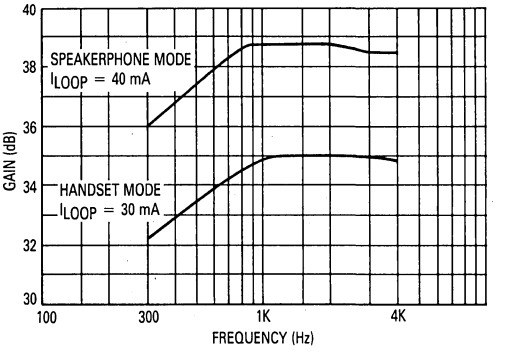


Figure 22. Transmit Gain versus Frequency

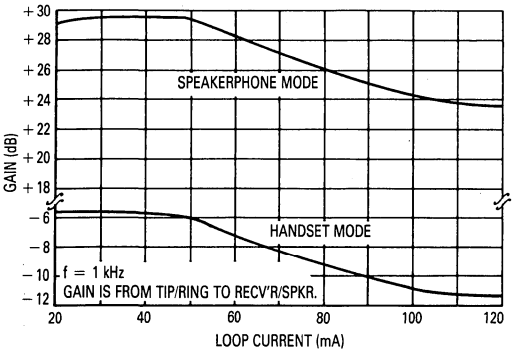


Figure 23. Receive Gain versus Loop Current

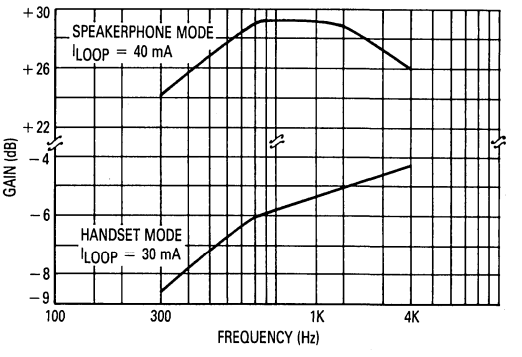


Figure 24. Receive Gain versus Frequency

USING A POWER SUPPLY INSTEAD OF LINE POWER

Using A Transformer

For those cases where it is desireable to power the featurephone from a regulated power supply, rather than from loop current, a transformer is required to provide the isolation needed between the phone line and any ac power and earth ground. The primary change to the circuit of Figure 10 is in the area of the Tip & Ring interface, as shown in Figure 25. It must be remembered that loop length compensation is not possible in this circuit since the loop current is not monitored. The MC34114's RAGC pin is grounded in this circuit, setting the transmit and receive gains to maximum.

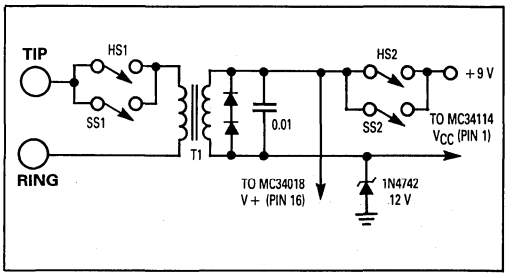


Figure 25. Tip/Ring Interface with a Power Supply

The +9 volt supply powers the MC34114 through the transformer winding. In this manner the speech signals are coupled between the MC34114 and Tip/Ring. The two diodes provide transient clamping, as does the 12 volt zener diode. The MC34018 is powered directly from the +9 volt supply, eliminating the need for the 1H choke.

The SS switch (speakerphone on/off) requires one more pole now, as shown in Figure 25. (Note: Although a +9 volt supply is shown, a lower voltage supply could be used as well.)

Changes in the Dialer and Logic Circuit

To reduce the parts count of the logic portion of the previous circuits, Q1–Q3 were replaced with logic gates. A triple 3-input AND gate, with open collector outputs (74LS15), fulfills the requirements of Tables 1 and 2. (The use of an LSTTL logic gate was not feasible in the previous two circuits due to the current consumption of the LS device.) The 5 volt power for the gates is derived from the +9 volt supply using a 1N4733 zener diode. Since the dialer's mute output drives the gate inputs, it is necessary to power the dialer from the same +5 volt supply, rather than the MC34114's V_{DD} supply. The resulting logic circuit is shown in Figure 26.

The use of the logic gate also simplifies the selection of handset versus speakerphone mode of operation. The diversion of the excess loop current is not an issue in this circuit, so the switching of that current is eliminated, along with Q4. The Mike Mute function can now be provided from a single pole switch, rather than the two pole switch of the previous circuits.

With this circuit, the handset operated switch (HS) remains a 3-pole switch.

Because of the isolation requirement, the MC145412 dialer requires a relay to break the loop current during pulse dialing. Figure 27 depicts this circuit.

The relay is normally off, and energized only for the pulse dialing function. The 1 μF capacitor (rated 250 volts min., NPO) helps absorb the transients generated during pulse dialing.

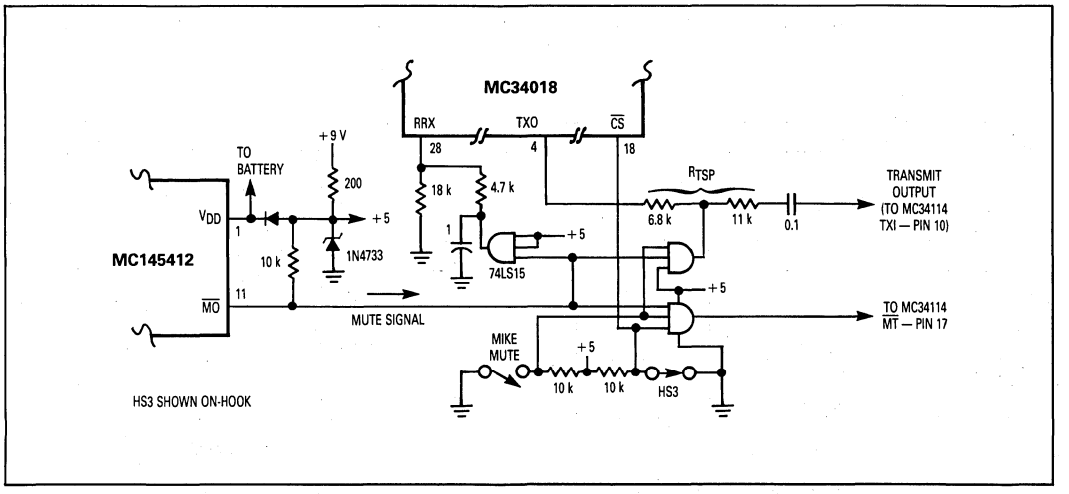


Figure 26. Switching Modes Using Logic Gates

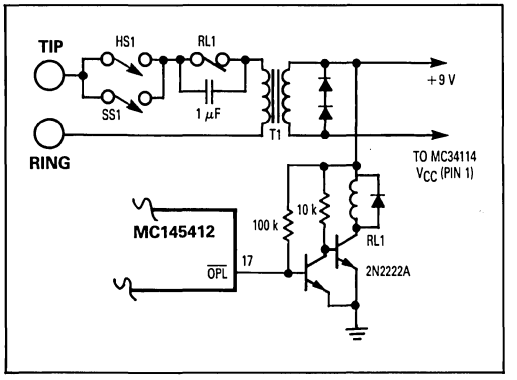


Figure 27. Pulse Dialer Circuit

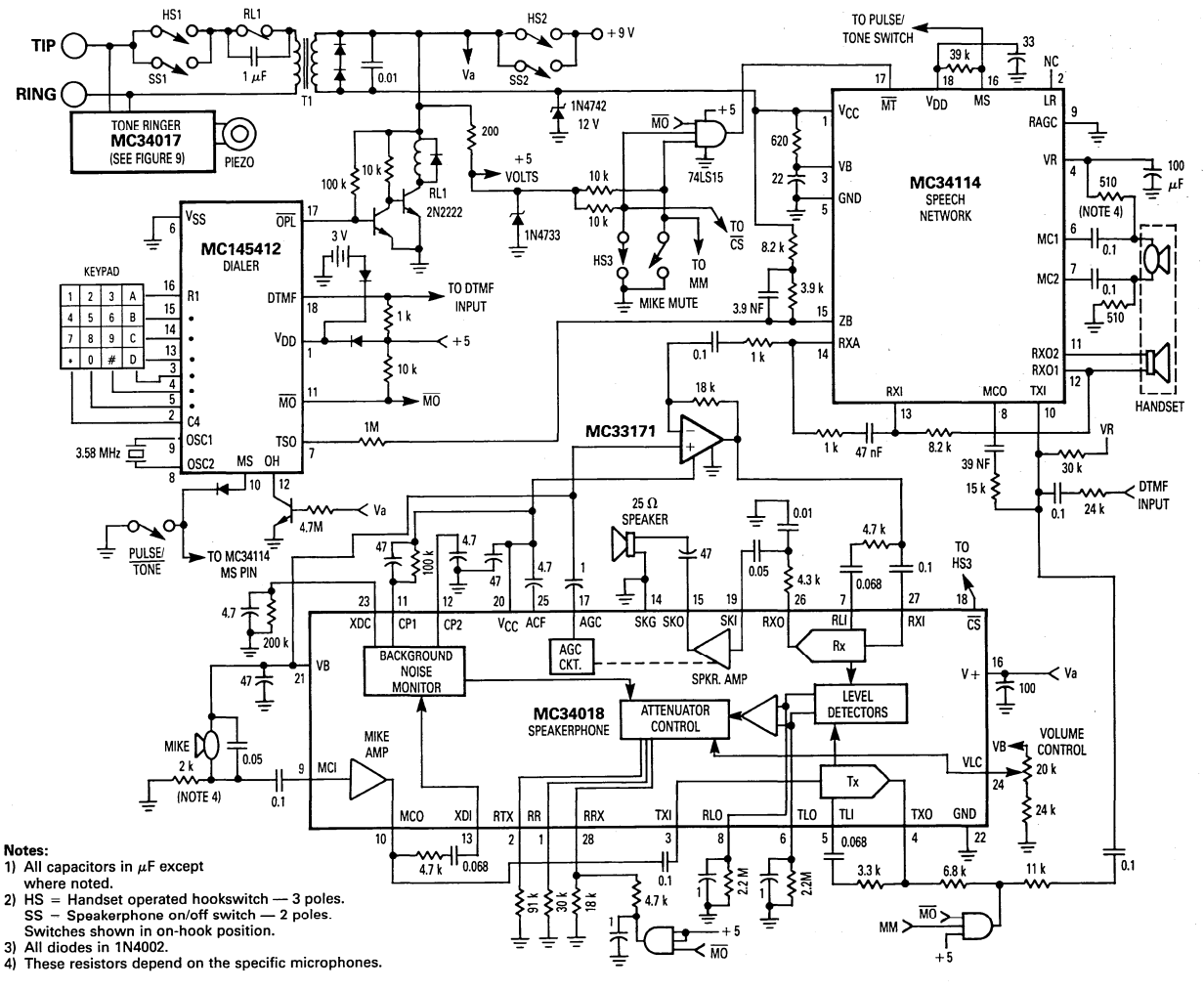
The Complete Circuit with the Power Supply

The complete circuit is shown in Figure 28. The performance curves are shown in Figures 29–34. The Tip to Ring dc voltage (Figure 29), determined solely by the dc resistance of the transformer winding, is somewhat lower than in the previous circuits. Figures 30, 31, and 33 show the performance is fairly constant with loop current, except for a slight reduction in gain at the higher currents. This is due to the characteristics of the transformer used in developing this circuit (model #TTPC-13 from Stancor, Inc.). Also noticeable in the curves, compared to Figures 11–16 and 19–24, is the lack of loop length compensation — a natural consequence of this type of circuit.

The muting specifications for this circuit are the same as for the line powered circuit. The current required from the +9 volt power supply is as follows:

a) Handset mode: ≈32 mA.
b) Speakerphone mode (no sound at the speaker): ≈41 mA.
c) Speakerphone mode (max. volume at the speaker): ≈82 mA.

Although Figure 28 indicates the use of a 25 ohm speaker, any impedance speaker within the range of 16 to 40 Ω can be used, since this circuit is not line powered. The receive gain may have to be adjusted, however, if a different speaker is used.



Notes:
1) All capacitors in μF except where noted.
2) HS = Handset operated hookswitch — 3 poles.
   SS = Speakerphone on/off switch — 2 poles.
   Switches shown in on-hook position.
3) All diodes in 1N4002.
4) These resistors depend on the specific microphones.

Figure 28. Pulse/Tone Featurephone w/Memory — Powered From a Power Supply

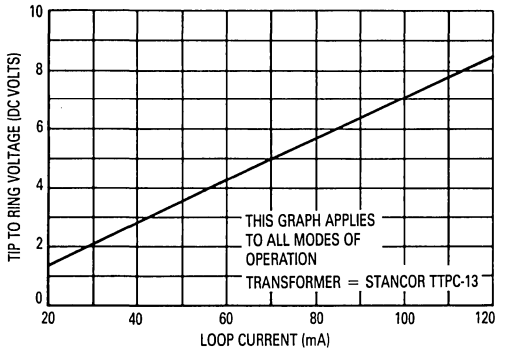


Figure 29. Tip to Ring DC Voltage versus Loop Current

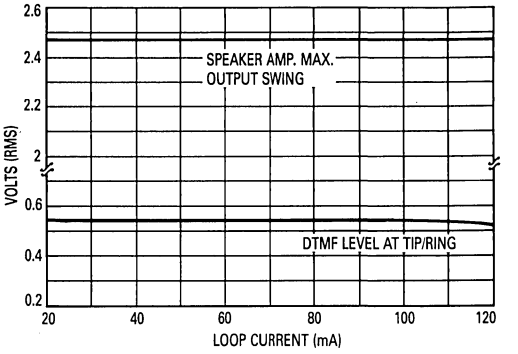


Figure 30. Max. Speaker Amplifier Output and DTMF Level versus Loop Current

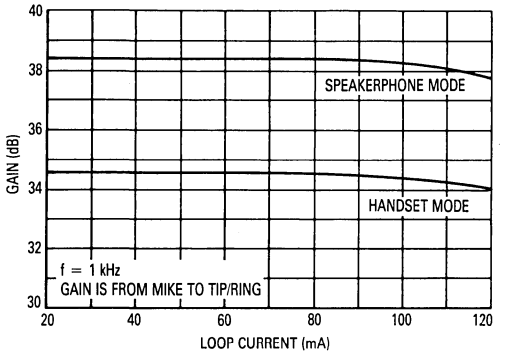


Figure 31. Transmit Gain versus Loop Current

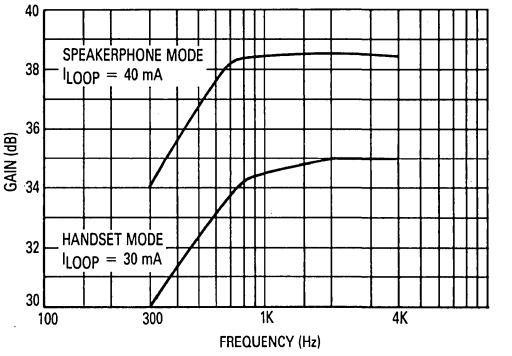


Figure 32. Transmit Gain versus Frequency

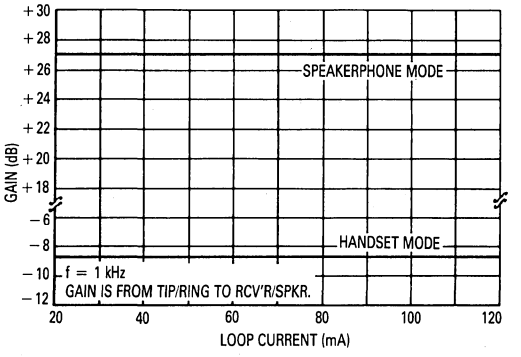


Figure 33. Receive Gain versus Loop Current

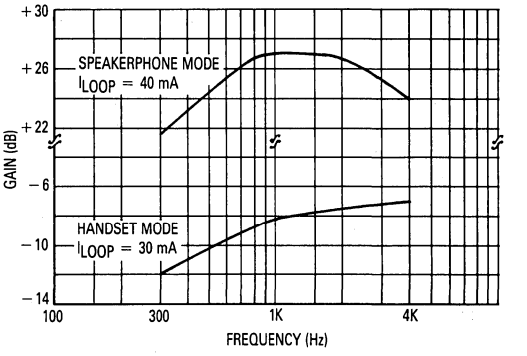


Figure 34. Receive Gain versus Frequency

CONSTRUCTION HINTS

Board Layout

The filter capacitor for the MC34018 speakerphone IC (typically 1000 μF) must be physically adjacent to Pin 16 of the IC, within 1". This is particularly important in the line-powered versions, where V_{CC} can vary with the speech intensity. Since most of the current is used in the speaker amplifier, the PC board track leading to Pin 16 of the MC34018 should be laid out with care, preferably close to the zener diode, or the power supply connector. The ground tracks should be as wide as possible, and laid out with care.

EMI Susceptibility

Potential EMI susceptibility problems should be addressed early in the electrical and mechanical design of the speakerphone. EMI may enter the circuit through Tip & Ring, through the microphone wiring to the amplifiers, or through any of the PC board traces. The most sensitive pins on the MC34108 are the inputs to the level detectors (RLI, TLI), since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. These board traces should be kept short, and the resistor and capacitor for each input should be physically close to the pins. Other high impedance input pins (MCI, VLC) should be considered sensitive to EMI signals.

The microphone wires within the handset cord can act as an antenna, and pick up nearby radio stations. If this is a problem in the final design, adding RF filters (consisting of ferrite beads and small (0.001 μF) ceramic capacitors) to the PC board where the wires attach to the board can generally reduce the problem.

Acoustics

a) In the design of any speakerphone, acoustics are extremely important, and **must** be considered from the very beginning. Building a breadboard with the microphone and speaker "hanging out in mid air" simply **will not work!!!** One of the most common problems in a speakerphone design is acoustic feedback (the speaker is closely coupled to the microphone) which results either in oscillations (2–10 kHz) or "motor-boating" (1–10 Hz switching). A properly designed enclosure for the finished product should provide at least 50 dB of acoustic loss (speaker drive voltage to microphone output voltage). The physical location of the microphone, along with the characteristics of the microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

b) The quality of the speaker, and the acoustic cavity in which it resides, have a major impact on the quality of the sound. A little time spent here can go a long way towards improving the sound of the finished speakerphone. As a general rule, good electronics cannot compensate for poor acoustics and/or low speaker quality.

In the Final Analysis . . .

In the final analysis, the circuits shown in this application note will have to be "fined tuned" to match the acoustics of the enclosure, and the specific microphone and speaker selected. The component values shown in this application note should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at key points in the circuits (see appropriate text). The switching response of the speakerphone can then be fine tuned by varying (in small steps) the components at the level detector inputs until satisfactory operation is obtained for both long and short lines. The references can be consulted for additional speakerphone design theory.

GLOSSARY

Attenuation — A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth — The range of information carrying frequencies of a communication system.

C-Message Filter — A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

Central Office — Abbreivated CO, it is a main telephone office, usually within a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A typical CO can handle up to 10,000 subscriber numbers.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:
10 x log (P_1/P_2) for power measurements, and
20 x log (V_1/V_2) for voltage measurements.

dBm — An indication of signal power. 1 mW across 600 Ω, or 0.775 volts rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:
dBm = 20 x log (Vrms/0.775), or
dBm = [20 x log (Vrms)] + 2.22.

dBmp — Indicates dBm measurement using a psophometric weighting filter.

dBrn — Indicates a dBm measurement relative to 1 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = −90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

dBrnC0 — Noise measured in dBrnC referred to zero transmission level.

DTMF — Dual Tone Multi-Frequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad.

Four Wire Circuit — The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the Transmit path (generally from the microphone), and one pair is for the Receive path (generally to the receiver).

Full Duplex — A transmission system which permits communication in both directions simultaneously. The standard handset telephone is full duplex.

Gain — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Half Duplex — A transmission system which permits communication in one direction at a time. CB radios, with "push-to-talk" switches, and voice activated speakerphones, are half duplex.

Hookswitch — A switch which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Line Length Compensation — Also referred to as loop compensation, it involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less, and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length.

Loop — The loop formed by the two subcriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or ac power.

Loop Current — The dc current which flows through the subscriber loop. Typically provided by the central office or PBX, it ranges from 20 to 120 mA.

Off Hook — The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the dc current as an indication that the phone is busy.

On Hook — The condition when the telephone is disconnected from the phone system, and no dc loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange. In effect, a miniature central office, it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

Pulse Dialing — A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 times per second. The old rotary phones, and many new pushbutton phones, use pulse dialing.

REN — Ringer Equivalence Number. An indication of the impedance, or loading factor, of a telephone bell or ringer circuit. An REN of 1 equals ≈8 k ohms. The Bell system typically permits a maximum of 5 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

Ring — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

Sidetone — The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2-to-4 wire conversion system. Widetone was recognized by Alexander Graham Bell as necessary for a person to be able to speak properly while using a handset.

Speech Network — A circuit which provides 2-to-4 wire conversion, i.e. connects the microphone and receiver (or the transmit and receive paths) to the Tip and Ring phone lines. Additionally it provides sidetone control, and in many cases, the dc loop current interface.

Subscriber Line — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

Tip — One of the two wires connecting to the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

Tone Ringer — The modern solid state equivalent of the old electromechanical bell. It provides the sound when the central office alerts the subscriber that someone is calling. Ringing voltage is typically 80–90 Vrms, 20 Hz.

Two-Wire Circuit — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

Voiceband — That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300–3400 Hz.

REFERENCES

MC34018 Data Sheet, March, 1988, Motorola Inc.
MC34017 Data Sheet, January, 1984, Motorola Inc.
MC34114 Product Preview Data Sheet, Sept. 1987, Motorola Inc.
MC33171 Data Sheet, February, 1988, Motorola Inc.
MC145412 Data Sheet, February, 1987, Motorola Inc.
Busala, A., Fundamental Considerations in the Design of a Voice Switched Speakerphone, B.S.T.J., 39, 1960, p. 265.

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, Ill. 60106
312-595-1022
Model EM-60

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

Hosiden America Corp.
Elk Grove Village, Ill. 60007
312-981-1144
Model KUC2123

25 Ω Speakers

Panasonic Industrial Co.
Seacaucus, N.J. 07094
201-348-5233
Model EAS-45P19S

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
516-561-6050
Various models — ask for catalog and Applications Bulletin F232

Stancor Products
Logansport, IN 46947
219-722-2244
Various models — ask for catalog

PREM Magnetics, Inc.
McHenry, Ill. 60050
815-385-2700
Various models — ask for catalog

Onan Power/Electronics
Minneapolis, MN 55437
612-921-5600
Model TC 38-6

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MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

A Featurephone Design, with Tone Ringer and Dialer, Using the MC34118 Speakerphone IC

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INTRODUCTION

This application note describes how to add a handset, dialer and tone ringer to the MC34118 speakerphone circuit. Although any one of several speech networks could be used as an interface between the MC34118 and the phone line (those possibilities are discussed in separate application notes) this application note covers the case where simplicity and low cost are paramount. A "Privacy" (Mike Mute) function is included, but not pulse dialing, nor line length compensation.

Two circuits are developed in this discussion: a line-powered featurephone and one powered from a power supply. The circuits are nearly identical, except for the Tip and Ring interface. Their parameters however, differ noticeably, particularly in the low loop current range.

MC34118 DESCRIPTION

The MC34118 speakerphone IC provides all of the necessary functions for a complete speakerphone circuit, except for the speaker amplifier, in a single integrated circuit. Included are the transmit and receive attenuators, which operate in a complementary manner, to provide the half-duplex function. The four level detectors, in conjunction with the background noise monitors and the control algorithm, provide a four point sensing and decision making system to control the attenuators based on the levels and timing of the transmit and receive signals. A filter, user selectable to be high pass, low pass, or bandpass, is included for filtering either the transmit or receive signals. Additional functions include volume control for the receive path, a Mute input for the microphone amplifier and a chip disable pin. A simplified block diagram is shown in Figure 1.

Unlike many other speakerphone ICs, the MC34118 includes the hybrid amplifiers for the two-to-four wire conversion when used in conjunction with a transformer. Figure 2 depicts a basic line powered speakerphone using the MC34119 speaker amplifier. When used in parallel with any standard telephone, all of the necessary telephone functions are then provided.

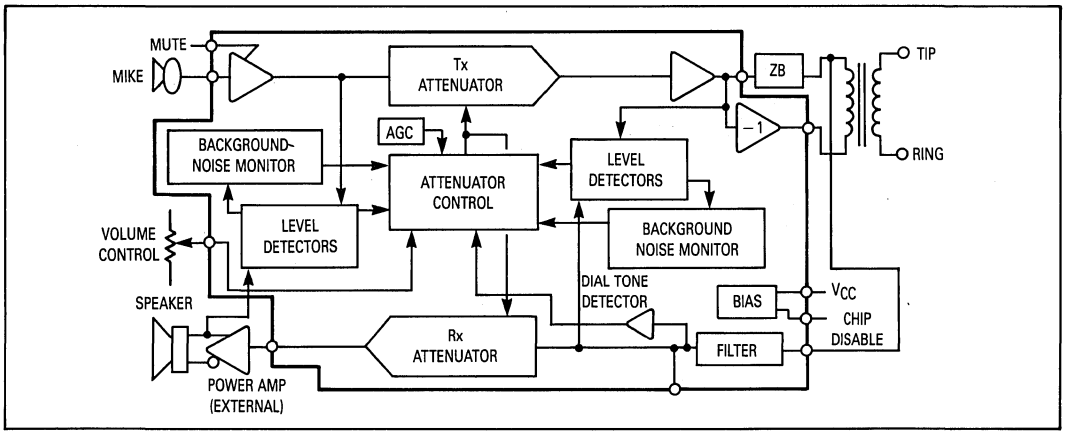


Figure 1. Simplified Block Diagram

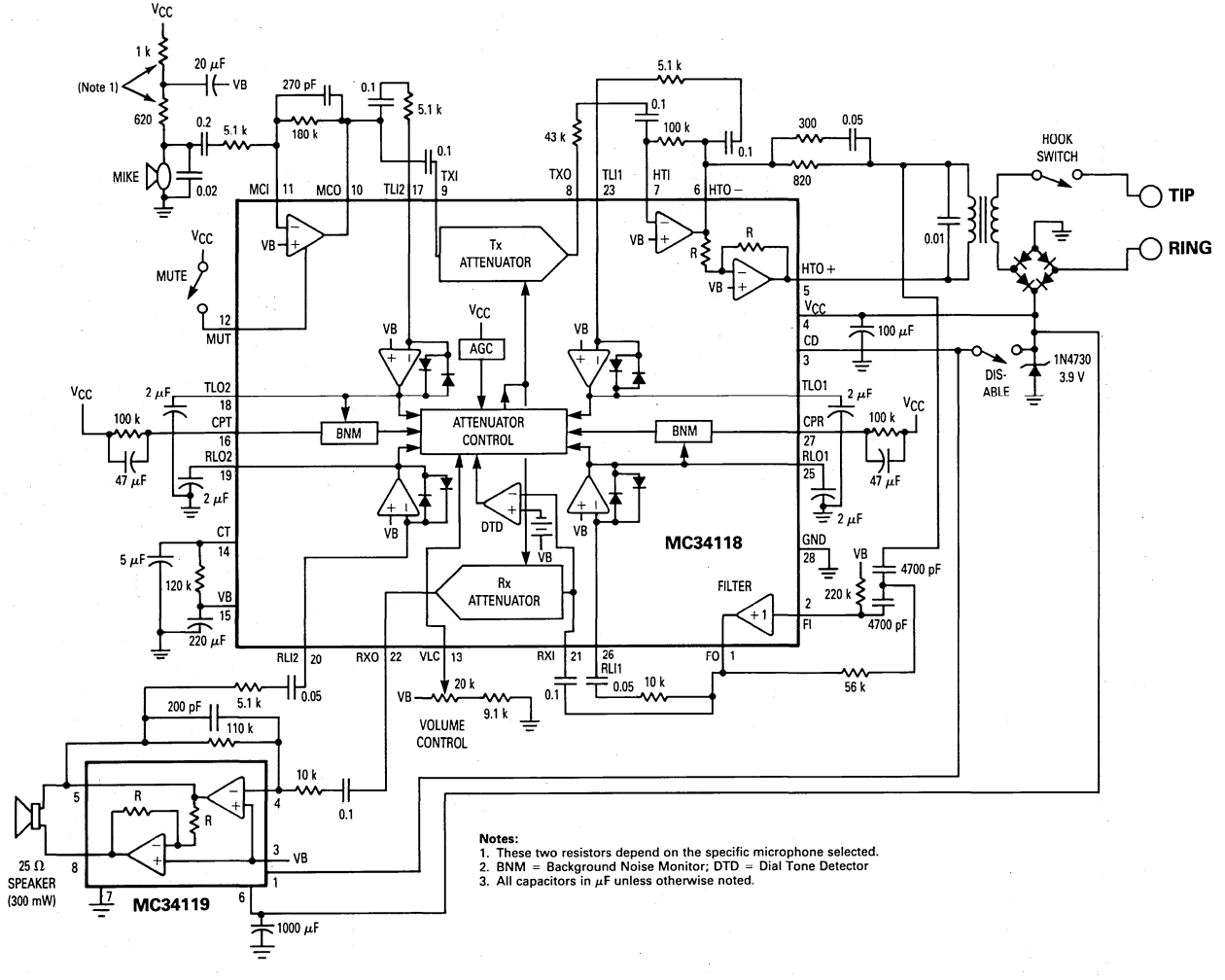


Figure 2. Basic Line-Powered Speakerphone

LINE-POWERED FEATUREPHONE

DC Characteristics

The DC characteristics of the circuit (Figure 2) are determined by the resistance of the transformer winding (Stancor TTPC-13 in this circuit development), the diode bridge and the zener diode. Using a 3.9 volt zener diode (to power the speakerphone and the various parts of the circuit) the voltage at Tip and Ring is within the EIA-470 guidelines.

With a V_{CC} of 3.9 volts, the MC34118 provides a VB voltage (Pin 15) of ≈1.6 volts. The VB voltage is used as an AC ground for the entire circuit.

Adding the Handset Microphone

The microphone used in developing this circuit was the Primo EM-95 which operates with a bias current of 500 μA to 1 mA. The bias current is obtained from the V_{CC} supply voltage, but the bias resistor is composed of two resistors, with the center tap AC coupled to VB, as shown in Figure 3. The AC output level of the microphone is determined by the 3.9 kΩ resistor, while the DC bias level is determined by the sum of the 3.9 k and 3 k resistors, and V_{CC}. The 0.047 μF capacitor provides high frequency roll-off. The AC output of the above circuit goes to Pin 7 (HTI) of the MC34118, which is the summing junction of the first hybrid amplifier. The 1 k resistor, in conjunction with the 100 k feedback resistor on the amplifier (Figure 3), sets the gain. In this way, the microphone signals are fed to Tip and Ring. The gain of this circuit can be adjusted by varying the 1 k or the 3.9 k resistor, or both. Different microphone models generally have different biasing requirements for optimum output levels.

The transistor, activated by an active high Mute signal, will shut off the microphone when it is to be inoperative, such as during dialing and during speakerphone operation.

Adding the Handset Receiver

Although the receive signals are available at the filter's output (FO, Pin 1), the low impedance of a typical receiver (100–150 Ω) requires a separate amplifier, depicted in Figure 4, to drive it. The MC33171 was chosen due to its low supply current (typically 180 μA). It is biased from VB and set for a gain of ≈0.43 (−7.3 dB). Low frequency roll-off is provided by the 0.047 μF input capacitor, as well as by the filter. High frequency roll-off is not provided since the presence of high frequencies generally make the sound "crisper" and therefore easier to understand. If roll-off is desired, simply add a capacitor across the 4.3 k feedback resistor.

The addition of the op amp facilitates providing sidetone control, which is obtained by sampling the transmit signal at HTO− (Pin 6) and using that to cancel part of the sidetone signal. The 20 k resistor and 0.02 μF capacitor provide a phase shift to compensate for the signal's phase shift at FO relative to HTO−, caused by the transformer and the line's complex impedance. The combination of the phase shift and the 10 k resistor (RS) determine the amount of sidetone cancellation.

Since the op amp is driving an inductive receiver at the end of a 2 to 3 foot cord, the 0.01 μF capacitors at the inputs are necessary for stability.

The diode provides a simple means for disabling this circuit during speakerphone operation. With "Shutoff" at ground, the amplifier is disabled.

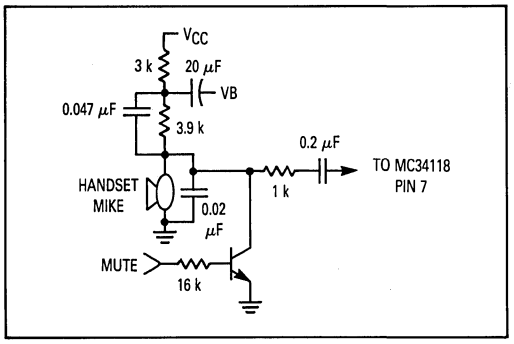


Figure 3. Handset Microphone Circuit

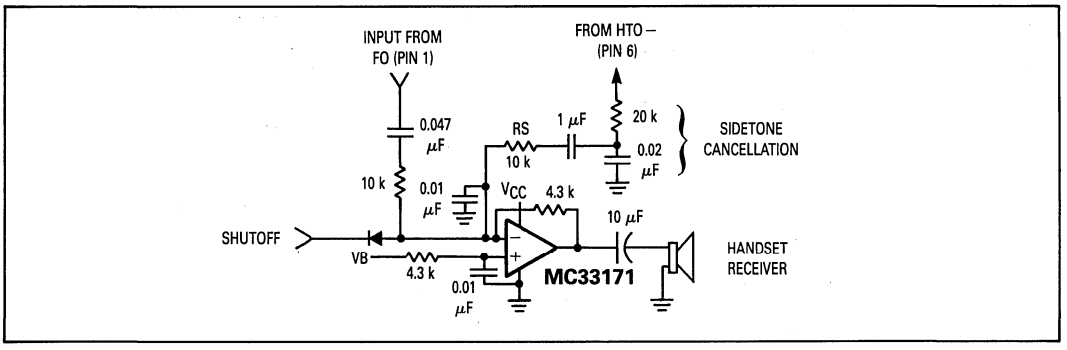


Figure 4. Handset Receiver Circuit

Adding the Dialer

The dialer is the MC145412 pulse/tone dialer with 10 number memory. Since the pulse dialing function is not used, the MS pin is grounded and the OPL (Outpulsing) and TSO (Pacifier tone) outputs are not used. The circuit uses a standard 3.58 MHz crystal and standard 3 x 4 or 4 x 4 keypads.

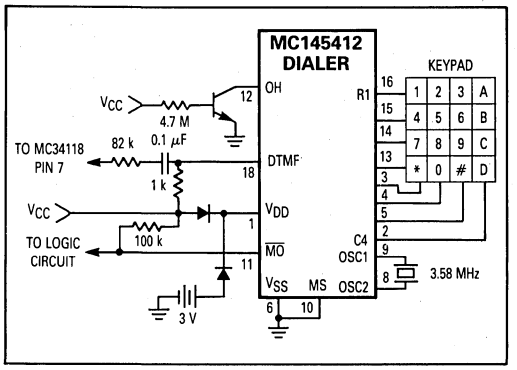


Figure 5. Dialer Circuit

Referring to Figure 5, the NPN transistor at Pin 12 indicates the on-hook/off-hook status to the IC. Power for the dialer is V_{CC}, diode connected with a memory sustaining battery. The DTMF output goes to Pin 7 (HTI) of the MC34118, which is the summing junction of the first hybrid amplifier. The 82 k resistor, in conjunction with the 100 k feedback resistor on the amplifier, determines the gain. With the values shown, the DTMF output at Tip and Ring is approximately 550 mVrms (−3 dBm). To change the output level, vary the 82 k resistor appropriately.

The Mute Output ($\overline{MO}$) is active low, open drain and pulls to ground while dialing. It is used to mute the speech paths during dialing.

Switching the Circuit Around

The logic functions involve: a) switching the circuit from handset mode to/from speakerphone mode, b) switching in and out of the dialing mode while in either handset or speakerphone mode and c) muting the two microphones for the "Privacy" function. Table 1 tabulates the requirements:

Table 1.

	Handset		Speakerphone	
Function	**Mike**	**R'cvr**	**Mike**	**Speaker**
Handset Speech	On	On	Off	Off
Handset Dialing	Off	Mute	Off	Off
Handset Mike Mute	Off	On	Off	Off
Speakerphone Speech	Off	Off	On	On
Speakerphone Dialing	Off	Off	Off	Mute
Speakerphone Mike Mute	Off	Off	Off	On

In Table 1, "ON" means fully functional, "OFF" means non-functional and "MUTE" means partially muted (10 to 20 dB).

To provide the logic functions and with the intent of keeping the number of mechanical switches to a minimum and simplicity at an optimum, an MC14023 triple 3-input CMOS NAND gate was used. See Figure 6.

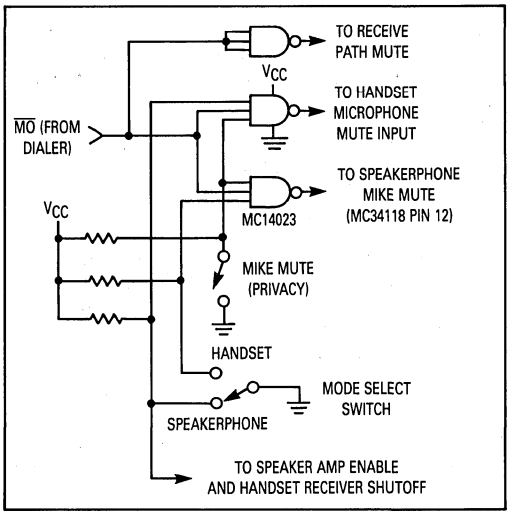


Figure 6. Logic Circuit

The inputs are the Mute Output ($\overline{MO}$) from the dialer (described above), the Mike Mute switch and the Mode Select switch. The outputs are:

1. An active low output which enables the MC34119 speaker amplifier (at its Pin 1) and disables the handset receiver;
2. An active high output which disables the speakerphone microphone at the MC34118's Pin 12 (MUT);
3. An active high output which disables the handset microphone;
4. An active high output which partially mutes the receive path during dialing. The circuit which does the partial muting is shown in Figure 7.

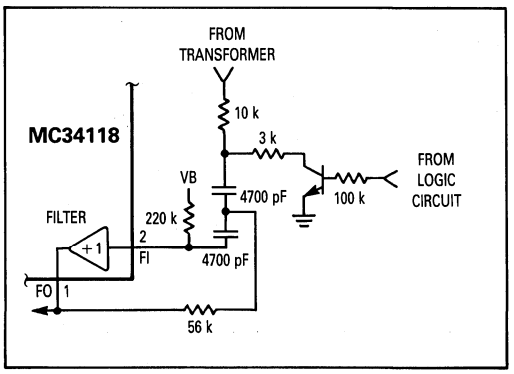


Figure 7. Receive Path Muting

The muting circuit, consisting of the transistor and the 3 k and 10 k resistors, is inserted in the line from the transformer to the filter. Normally the transistor is off and the 10 k resistor has little effect on the circuit due to the high input impedance of the filter (>200 kΩ @ 1 kHz). When Mute is asserted, the signal to the filter is muted by ≈12.7 dB.

The MC34118's Disable pin (Pin 3) is hard wired to ground since the MC34118 must be functional for both the speakerphone and handset modes.

Adding the Tone Ringer

The MC34017 tone ringer circuit, shown in Figure 8, is added to the circuit by simply connecting it across Tip and Ring. It is not necessary to disconnect the tone ringer when off-hook. This circuit will provide a ringer with an REN of ≈1 and meet all the EIA-470 and Bell System requirements for impedance, anti-bell tapping and turn-on/off thresholds.

Finally, the Complete Circuit

The complete line-powered featurephone is shown in Figure 9. HS1 and HS2 are the two poles of the hook-switch activated by lifting the handset off-hook (HS2 is the Mode Select Switch of Figure 6). SS1 is a single pole switch which, when closed (and the handset is on-hook), powers up the circuit into the speakerphone mode. Should the handset be taken off-hook, the circuit reverts to the handset mode.

The performance curves for the circuit are shown in Figures 10–15. The "Speaker Amp Max Output Swing" is the maximum rms voltage available across pins 5 and 8 of the MC34119 without noticeable clipping. The transmit gain tests involved replacing each microphone with a signal generator and adjusting for a level of approximately −11 dBm at Tip and Ring into a 600 Ω resistive load. The receive tests involve applying approximately −27 dBm to Tip and Ring, and measuring the gain to the receiver or speaker.

As can be seen in Figure 11, the maximum available speaker power is a function of the loop current since all of the speaker current must come from the loop. Consequently, the receive gain for the speakerphone (Figure 14) shows a marked decrease at low loop currents. It must be remembered that in a line powered speakerphone, as the speaker draws current in response to a receive signal, the voltage at Tip and Ring decreases quickly. As V_{CC} falls with the Tip and Ring voltage, not only is the speaker amp's output capability reduced, but the MC34118's AGC circuit automatically reduces the receive gain as V_{CC} falls below 3.5 volts. This feature prevents slow oscillations (motor-boating) due to the speaker's current demands. A 25 Ω speaker is recommended as this makes the best use of the power available from the phone line. A lower impedance speaker will require more current, causing V_{CC} to sag further for a given signal level. A higher impedance speaker draws less current, but produces less sound power.

The slight degradation of DTMF levels in Figure 11 and in the transmit levels in Figure 12, at higher loop currents is a function of the transformer's performance at those current levels.

Additionally, the following muting specs apply:

1. **Handset microphone:** ≈37 dB while dialing, in speakerphone mode, or when Mike mute switch is closed.
2. **Speakerphone microphone:** >60 dB while dialing or due to Mike Mute switch, plus an additional 52 dB due to the MC34118 switching to the receive mode. >60 dB while in the handset mode.
3. **Handset receiver:** ≈12.7 dB while dialing, ≈45 dB when in the speakerphone mode.
4. **Speaker:** ≈12.7 dB while dialing, >100 dB when in handset mode.

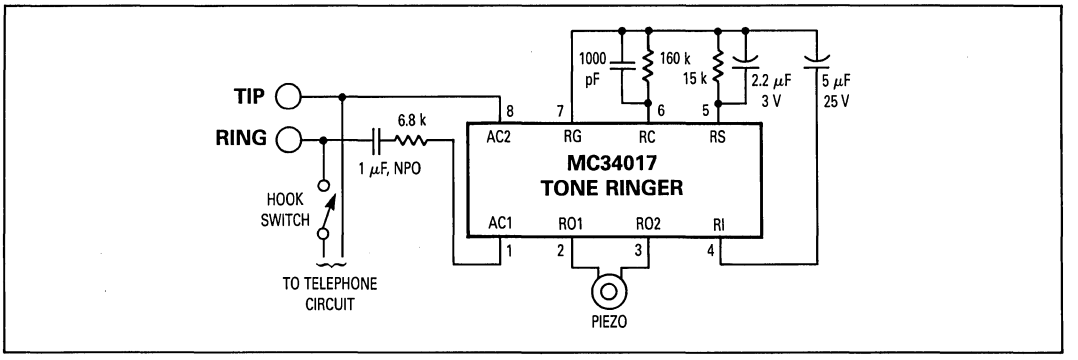
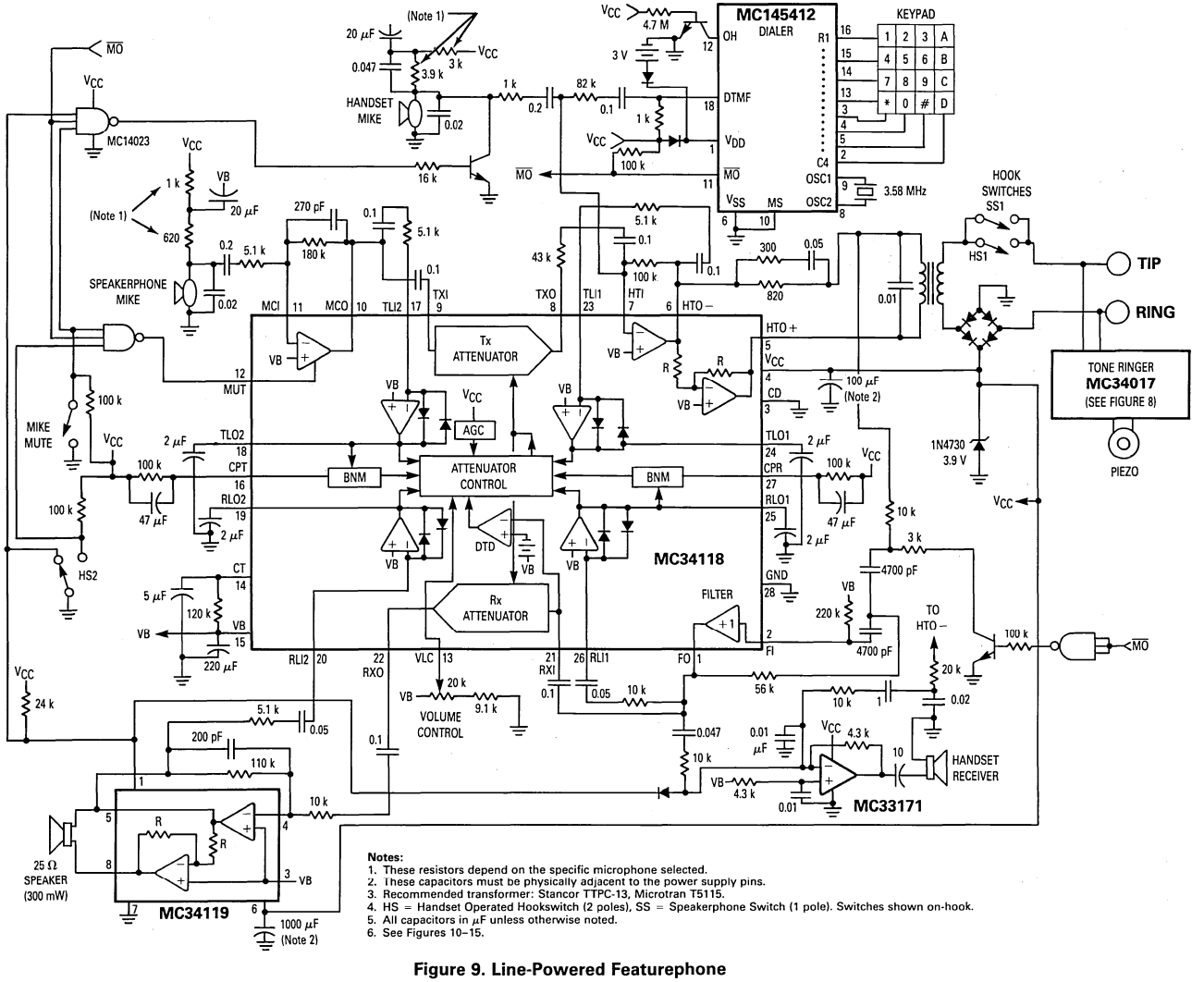


Figure 8. Tone Ringer Circuit



Notes:
1. These resistors depend on the specific microphone selected.
2. These capacitors must be physically adjacent to the power supply pins.
3. Recommended transformer: Stancor TTPC-13, Microtran T5115.
4. HS = Handset Operated Hookswitch (2 poles), SS = Speakerphone Switch (1 pole). Switches shown on-hook.
5. All capacitors in μF unless otherwise noted.
6. See Figures 10–15.

Figure 9. Line-Powered Featurephone

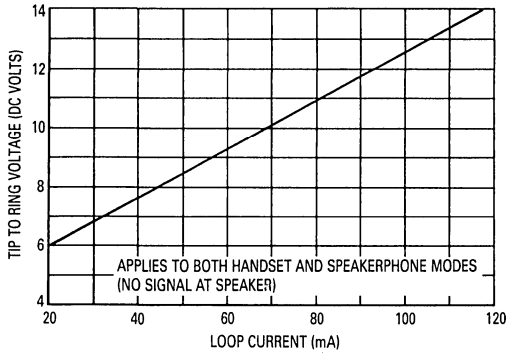


Figure 10. Tip to Ring DC Voltage versus Loop Current

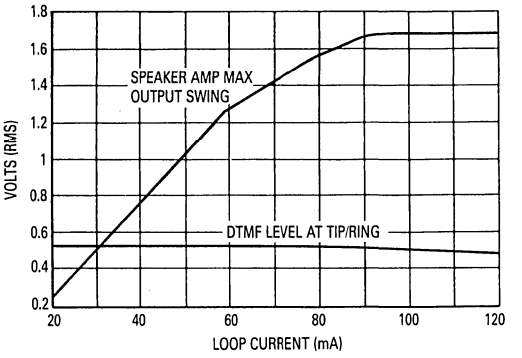


Figure 11. Speaker Amp. Output and DTMF Level versus Loop Current

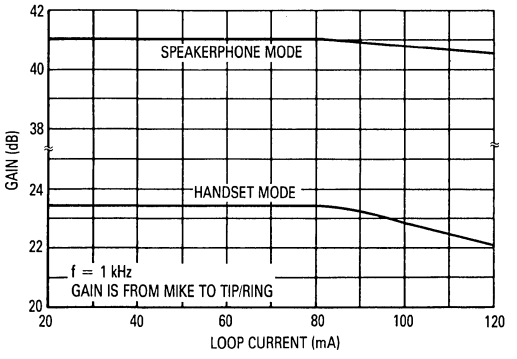


Figure 12. Transmit Gain versus Loop Current

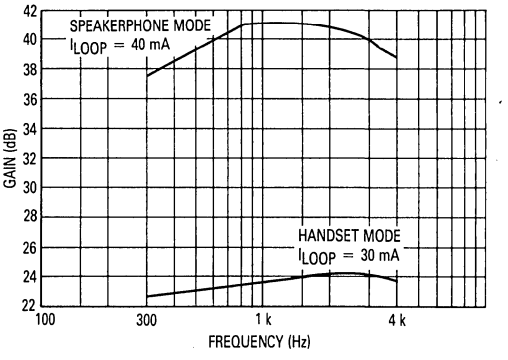


Figure 13. Transmit Gain versus Frequency

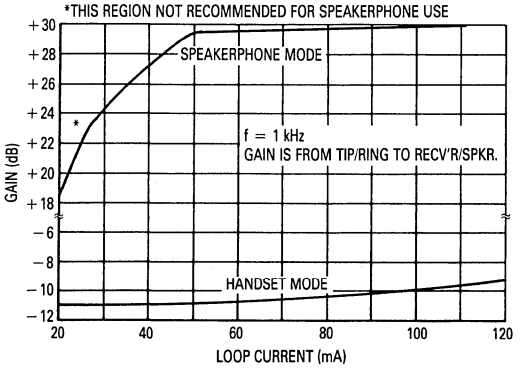


Figure 14. Receive Gain versus Loop Current

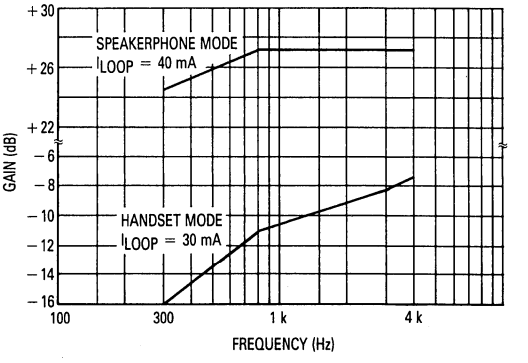


Figure 15. Receive Gain versus Frequency

USING A POWER SUPPLY INSTEAD OF LINE POWER

Figure 16 shows the circuit of Figure 9 modified for use with a +5 volt power supply. The only changes are at the Tip and Ring interface where the zener diode and bridge have been eliminated, but the two hook switches (HS and SS) require one more pole each. The transformer is used to pass the speech signals and to provide the required isolation.

Current required from the +5 volt power supply is as follows:

1. Handset speech mode: 6 mA.
2. Handset dialing mode: 11 mA
3. Speakerphone speech mode (no speech signals): 9 mA.
4. Speakerphone receive mode, −27 dBm at Tip and Ring: 51 mA.
5. Speakerphone receive mode, −9 dBm at Tip and Ring: 100 mA.
6. Speakerphone dialing mode: 19 mA.

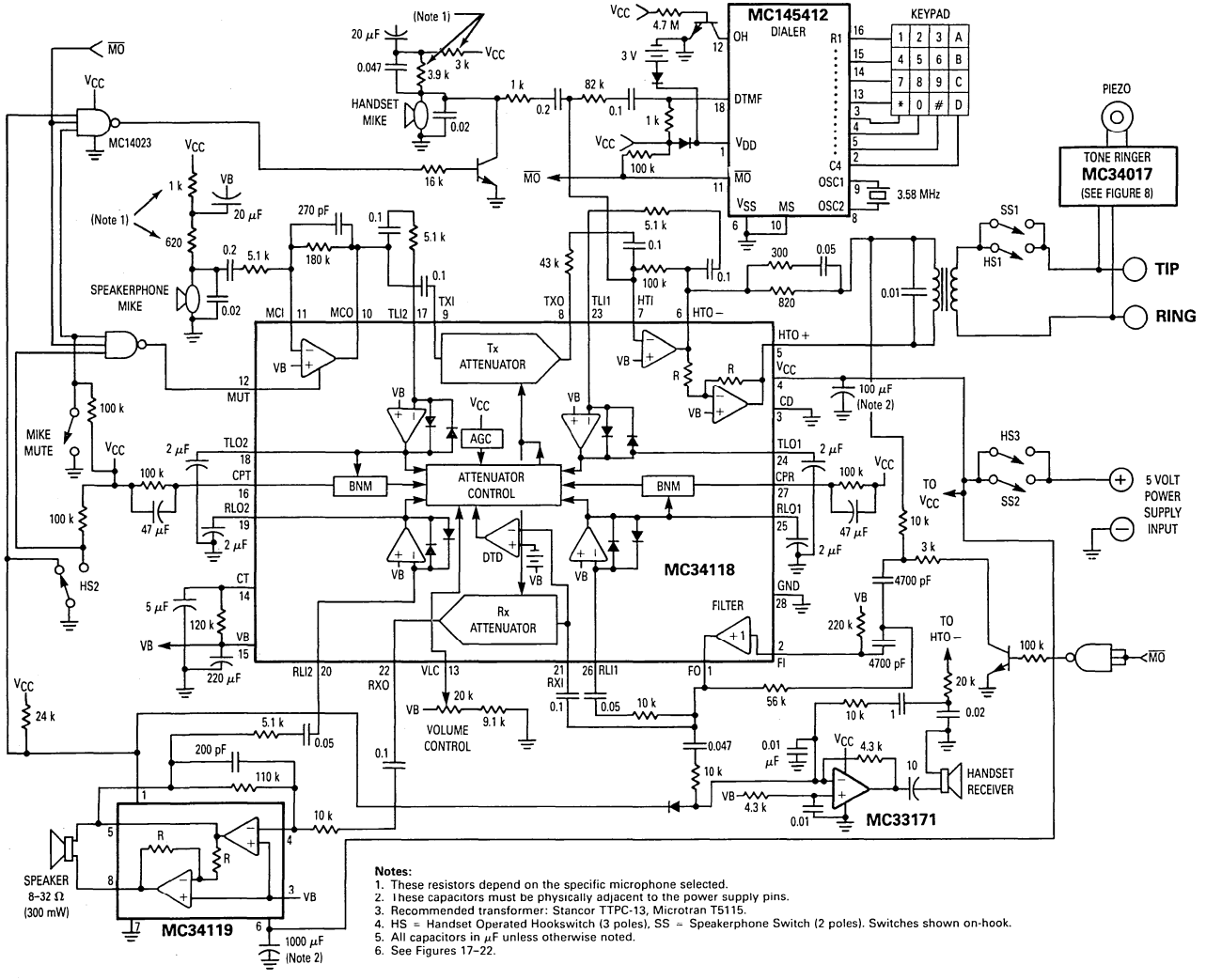
Items 4, 5 and 6 above were measured with a 25 Ω speaker and the volume control set to maximum.

The performance characteristics are shown in Figures 17–22. The Tip and Ring DC voltage (Figure 17) is now a function only of the transformer winding resistance and so is somewhat lower than in the previous circuit.

The speakerphone performance (Figures 18 and 21) is now constant with respect to loop current since V_{CC} is fixed. Performance at 20 mA is similar to that at higher loop currents, unlike the previous circuit. Although the speaker can be 25 Ω as in the previous circuit, it need not be since the available power is not limited as before. The recommended range for speaker impedance is 8–32 Ω. For different speaker impedances, however, the gain of the speaker amplifier may have to be changed to compensate for the different power level.

The slight degradation in the transmit curves at high loop currents is evident in Figures 18 and 19, as was in the previous circuit.

The muting specs of the transmit and receive paths are the same for this circuit as for the previous one.



Notes:
1. These resistors depend on the specific microphone selected.
2. These capacitors must be physically adjacent to the power supply pins.
3. Recommended transformer: Stancor TTPC-13, Microtran T5115.
4. HS = Handset Operated Hookswitch (3 poles), SS = Speakerphone Switch (2 poles). Switches shown on-hook.
5. All capacitors in μF unless otherwise noted.
6. See Figures 17–22.

Figure 16. Featurephone With Power Supply

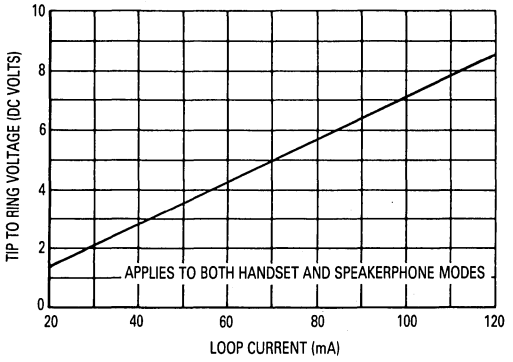


Figure 17. Tip to Ring DC Voltage versus Loop Current

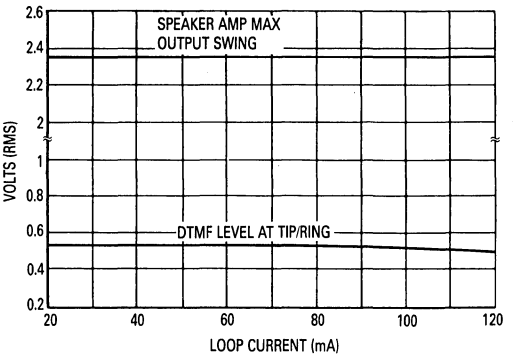


Figure 18. Speaker Amp. Output and DTMF Level versus Loop Current

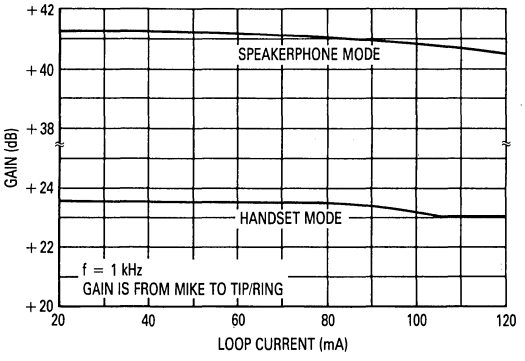


Figure 19. Transmit Gain versus Loop Current

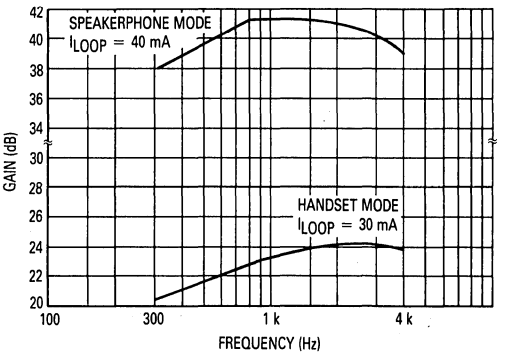


Figure 20. Transmit Gain versus Frequency

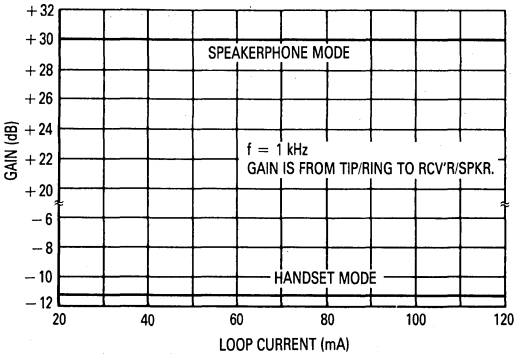


Figure 21. Receive Gain versus Loop Current

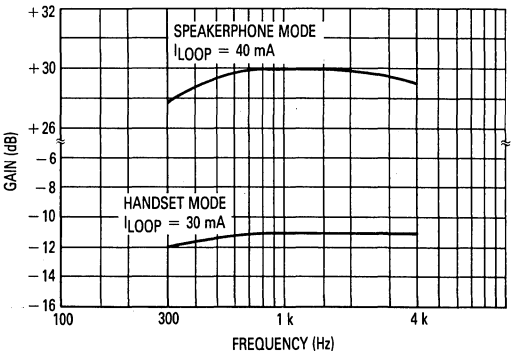


Figure 22. Receive Gain versus Frequency

CONSTRUCTION HINTS

Board Layout

The filter capacitors for the speakerphone IC and the speaker amplifier IC (100 μF and 1000 μF respectively) must be physically adjacent to the pins of the ICs, within 1". This is especially important in the line-powered version, where V_{CC} varies with the speech intensity. Since most of the current is used in the speaker amp, the PC board track leading to Pin 6 of the MC34119 should be laid out with care, preferrably close to the zener diode, or the power supply connector. The ground tracks should be as wide as possible, and laid out with care.

RFI Interference

Potential radio frequency interference problems should be addressed early in the electrical and mechanical design of the speakerphone. RFI may enter the circuit through Tip and Ring, through the microphone wiring to the amplifiers, or through any of the PC board traces. The most sensitive pins on the MC34118 are the inputs to the level detectors (RLI1, RLI2, TLI1 and TLI2) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. These board traces should be kept short and the resistor and capacitor for each input should be physically close to the pins. Other high impedance input pins (MCI, HTI, FI and VLC) should be considered sensitive to RFI signals.

The microphone wires within the handset cord can act as an antenna and pick up nearby radio stations. If this is a problem in the final design, adding RF filters (consisting of ferrite beads and small (0.001 μF) ceramic capacitors) to the PC board where the wires attach to the board can generally reduce the problem.

Acoustics

a. In the design of any speakerphone, acoustics are extremely important and **must** be considered from the very beginning. Building a breadboard and having the microphone and speaker "hanging out in mid air" simply **will not work!** One of the most difficult problems in a speakerphone design is acoustic feedback (the speaker talks to the microphone) which results either in oscillations (2–10 kHz) or "motor-boating" (1–10 Hz switching). A properly designed enclosure for the finished product should provide at least 50 dB of acoustic loss (speaker voltage to microphone output voltage). The physical location of the microphone, along with the characteristics of the microphone, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

b. The quality of the speaker and the acoustic cavity in which it resides, have a major impact on the quality of the sound. A little time spent here can improve the sound of the finished speakerphone. As a general rule, good electronics cannot compensate for poor acoustics and/or low speaker quality.

In The Final Analysis . . .

In the final analysis, the circuits shown in this application note will have to be "fine tuned" to match the acoustics of the enclosure and the specific microphone and speaker selected. The component values shown in this application note should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at the microphones and speaker/receiver amplifiers, respectively. The switching response of the speakerphone can then be fine tuned by varying (in small steps) the components at the level detector inputs until satisfactory operation is obtained for both long and short lines. The MC34118 data sheet should be consulted for additional speakerphone design theory.

GLOSSARY

Attenuation — A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth — The range of information carrying frequencies of a communication system.

C-Message filter — A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

Central Office — Abbreviated CO, it is a main telephone office, usually within of a few miles of its subscribers, that houses switching gear for interconnection within its exchange area and to the rest of the telephone system. A typical CO can handle up to 10,000 subscriber numbers.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:
10 x log (P_1/P_2) for power measurements and
20 x log (V_1/V_2) for voltage measurements.

dBm — An indication of signal power. 1 mW across 600 Ω, or 0.775 volts rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:
dBm = 20 x log (Vrms/0.775), or
dBm = [20 x log (Vrms)] + 2.22.

dBmp — Indicates dBm measurement using a psophometric weighting filter.

dBrn — Indicates a dBm measurement relative to 1 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = −90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

dBrnCO — Noise measured in dBrnC referred to zero transmission level.

DTMF — Dual Tone MultiFrequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad.

Four wire circuit — The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the Transmit path (generally from the microphone) and one pair is for the Receive path (generally to the receiver).

Full duplex — A transmission system which permits communication in both directions simultaneously. The standard handset telephone is full duplex.

Gain — The change in signal amplitude (increase or decrease) after passing through an amplifier or other circuit stage. Usually expressed in dB, an increase is a positive number and a decrease is a negative number.

Half duplex — A transmission system which permits communication in one direction at a time. CB radios, with "push-to-talk" switches and voice activated speakerphones, are half duplex.

Hookswitch — A switch which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Line length compensation — This is also referred to as loop compensation. It involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length.

Loop — The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or ac power.

Loop Current — The dc current which flows through the subscriber loop. Typically provided by the central office or PBX, it ranges from 20 to 120 mA.

Off hook — The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the dc current as an indication that the phone is busy.

On hook — The condition when the telephone is disconnected from the phone system and no dc loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange. This is a customer owned switching system servicing the phones within a facility. It is in effect, a miniature central office. A portion of the PABX connects to the Bell (or other local) telephone system.

Pulse dialing — A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed and the interruption rate is typically 10 times per second. The old rotary phones and many new pushbutton phones, use pulse dialing.

REN — Ringer Equivalence Number. This is an indication of the impedance, or loading factor, of a telephone bell or ringer circuit. A REN of 1 equals ≈8 k ohms. The Bell system typically permits a maximum of 5 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

Ring — This is one of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

Sidetone — The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2-to-4 wire conversion system. Sidetone was recognized by Alexander Graham Bell as being necessary for a person to be able to speak properly while using a handset.

Speech network — A circuit which provides 2-to-4 wire conversion, i.e. connects the microphone and receiver (or the transmit and receive paths) to the Tip and Ring phone lines. Additionally it provides sidetone control and in many cases, the dc loop current interface.

Subscriber Line — This is the system consisting of the user's telephone, the interconnecting wires and the central office equipment dedicated to that subscriber. It is also referred to as a loop.

Tip — One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

Tone Ringer — The modern solid state equivalent of the old electromechanical bell. It provides the sound when the central office alerts the subscriber that someone is calling. Ringing voltage is typically 80–90 Vrms, 20 Hz.

Two wire circuit — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

Voiceband — That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300–3400 Hz.

REFERENCES

MC34118 Data Sheet, April, 1987, Motorola Inc.
MC34119 Data Sheet, October, 1986, Motorola Inc.
MC33171 Data Sheet, July, 1985, Motorola Inc.
MC145412 Data Sheet, February, 1987, Motorola Inc.
Busala, A., Fundamental Considerations in the Design of a Voice Switched Speakerphone, B.S.T.J., 39, 1960, p. 265.

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, Ill. 60106
312-595-1022
Model EM-60

Hosiden America Corp.
Elk Grove Village, Ill. 60007
312-981-1144
Model KUC2123

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

25 Ω Speakers

Panasonic Industrial Co.
Seacaucus, N.J. 07094
201-348-5233
Model EAS-45P19S

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
516-561-6050
Various models — ask for catalog and applications Bulletin F232

PREM Magnetics, Inc.
McHenry, Ill. 60050
815-385-2700
Various models — ask for catalog

Stancor Products
Logansport, IN 46947
219-722-2244
Various models — ask for catalog

Onan Power/Electronics
Minneapolis, MN 55437
612-921-5600
Model TC 38-6

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AN1004

A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34118 Speakerphone ICs

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INTRODUCTION

This application note describes the procedure for combining the MC34114 speech network with the MC34118 speakerphone circuit into a featurephone which includes the following functions: ten number memory pulse/tone dialer, tone ringer, a "Privacy" (Mike Mute) function and line length compensation for both handset and speakerphone operation.

Three circuits are developed in this discussion: a line-powered featurephone, a line-powered featurephone with a booster (for using the speakerphone on long lines), and one powered from a power supply. The circuits are nearly identical, except for the Tip and Ring interface. Their performance however, differs noticeably, particularly in the low loop current range. Initially, the discussion will focus on the line-powered circuit.

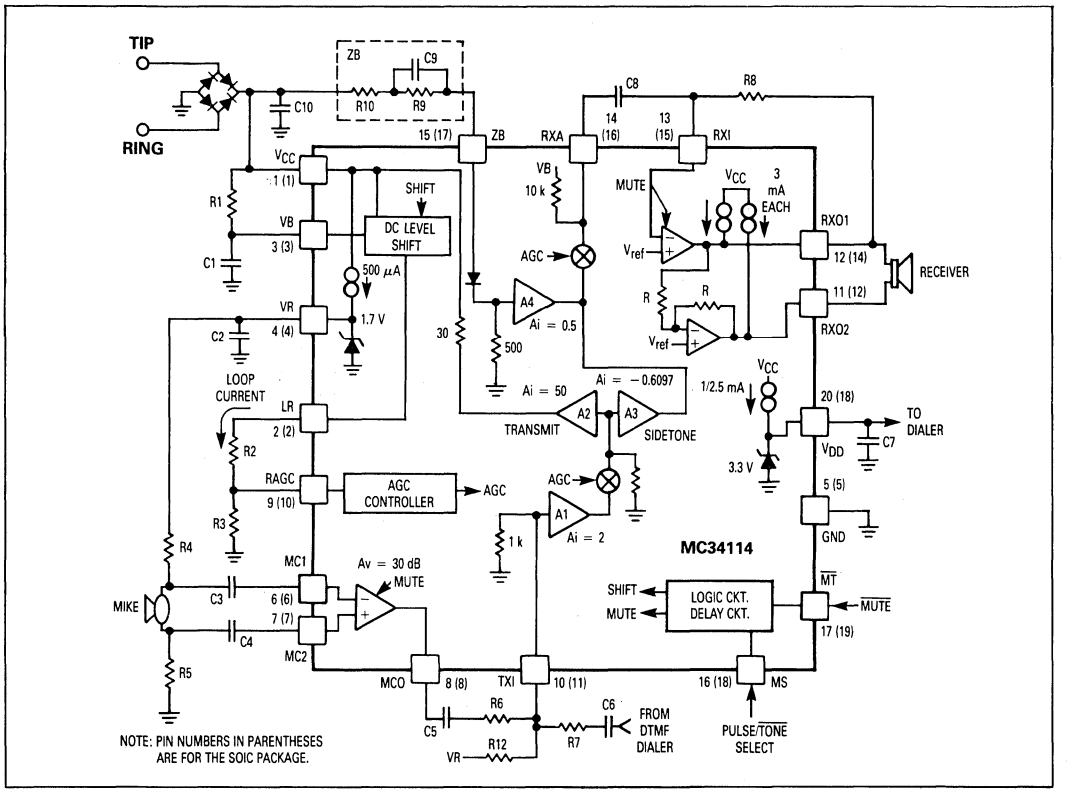


Figure 1. MC34114 Block Diagram

DESCRIPTION OF THE BUILDING BLOCKS

NOTE: Several pins on the ICs used in this application note have identical nomenclature (V_{CC}, VB, TXI, MS, V_{DD} and RXI). They provide separate functions, and are not to be connected together unless so noted.

MC34114 Speech Network

The MC34114 is a speech network which interfaces with Tip and Ring, and provides the 2-to-4 wire conversion (see Figure 1). The transmit gain is determined by the microphone amplifier (fixed gain of 30 dB), R6, C5, the internal current gains of A1, A2, the AGC, and the line impedance in parallel with R1. The receive gain is determined by ZB, the internal current gains of A4 and the AGC, C8 and R8. The sidetone cancellation is determined by A3 and the ZB network. The AGC points have a current gain of 1 at low loop current, and decrease to 0.5 (−6 dB) at higher loop currents, thus providing line length compensation. R1 (typically 600 Ω) sets the circuit's terminating impedance for ac (return loss) purposes.

The $\overline{\text{MUTE}}$ input (when low) disables the microphone amplifier, and partially mutes the receive amplifier (with an internal 1 k feedback resistor), when dialing. DTMF dialing signals are injected at TXI through R7 and C6. The Mode Select (MS) input (when low, and $\overline{\text{MT}}$ is low) provides a voltage boost at V_{CC} to ensure adequate voltage during DTMF dialing at low loop currents. The 3.3 volt regulated output (V_{DD}) powers the dialer, and the 1.7 volt regulated output (VR) is used to bias the microphone.

The dc characteristics at Tip and Ring are determined by the diode bridge (1.4 volts), a level shift of approximately 2.9 volts from V_{CC} to LR, and the voltage across R2 + R3 (typically 43 Ω and 13 Ω). All the loop current, minus ≈10 mA, flows through those two resistors. The level shift (V_{CC} − LR) increases to ≈3.9 volts when both $\overline{\text{MUTE}}$ and MS are low (tone dialing mode). The voltage at RAGC, when within the range of 0.5 to 1 volt, controls the internal AGC as a function of loop current.

MC34118 Speakerphone

The MC34118 speakerphone IC (see Figure 2) provides all the necessary functions for a complete speakerphone circuit in a single integrated circuit. Included are the transmit and receive attenuators, which operate in a complementary manner, to provide the necessary half-duplex function. The four level detectors, in conjunction with the two background noise monitors and control algorithm, provide a four point sensing and decision making system to control the attenuators based on the levels and timing of the transmit and receive signals. Additional functions include the microphone amplifier, a Mute input for the microphone amplifier, volume control for the receive path, a filter, and a Chip Disable pin. The gain of the receive attenuator, normally +6 dB at max. volume, is reduced by the AGC circuit as V_{CC} falls below 3.5 volts to control the amount of voltage sag in a line powered application. The component values shown are typical.

Connections to the MC34118 circuit are made to several points around the circuit as follows:

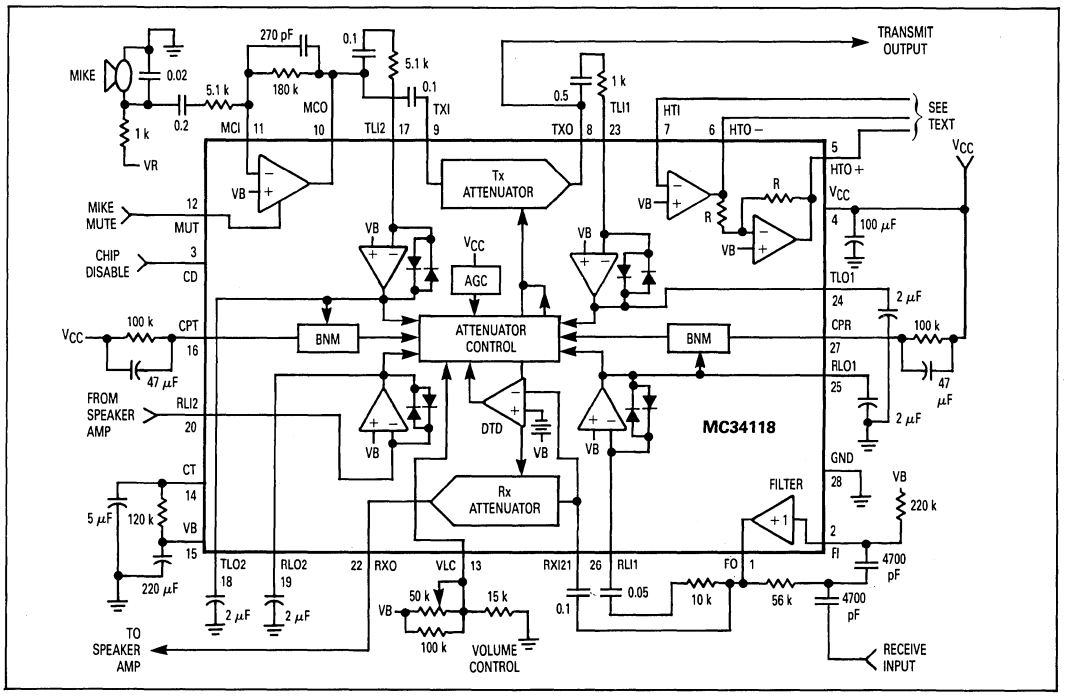


Figure 2. MC34118 Block Diagram

The TRANSMIT OUTPUT (upper right) connects to the 4 wire side of the speech network. The transmit gain, from the microphone to TRANSMIT OUTPUT, is +37 dB (+31 dB in the mike amp, +6 dB in the Tx attenuator), and does not vary with the volume control. In the receive mode, the transmit gain is ≈−15 dB.

The RECEIVE INPUT (lower right) is derived from the 4 wire side of the speech network. The gain from RXI to RXO is +6 dB when in the receive mode at maximum volume. At minimum volume, the attenuator's gain reduces by ≈46 dB, for an overall gain of −40 dB. In the transmit mode, the gain is ≈−46 dB. Pins 22 (Receive out) and 20 (Receive level detector input) connect to the external speaker amplifier (MC34119).

The overall speakerphone's transmit and receive gains to and from Tip and Ring are adjusted at the mike and speaker amplifier and at the 4-wire interface.

The MIKE MUTE input disables the mike amplifier when at a logic high. $\overline{\text{Chip Disable}}$ disables the MC34118 when at a logic high, reducing the MC34118's supply current from a normal ≈5.5 mA to ≈600 μA.

The two op amps (pins 5, 6, 7) are available for a variety of uses. Figure 23 of the MC34118 data sheet, for example, indicates their use with a transformer to form a standalone speakerphone. Later in this application note however, they will be used with the MC34114 as part of the receive path.

V_{CC} (Pin 4) is the power supply input, requiring 3 − 6.5 volts @ ≈5.5 mA. The 100 μF capacitor must be physically adjacent to pin 4 in the board layout to prevent oscillations.

VB is the ac ground for the IC, and must be well filtered, as shown.

MC34119 Speaker Amplifier

The MC34119 (Figure 3) is a 400 mW speaker amplifier, capable of 500 mW peaks. With a supply voltage range down to 2 volts, it is well suited for speakerphone applications. The gain is adjustable from less than 0 dB (it is unity gain stable) to a maximum of ≈46 dB to cover the voiceband. It provides a differential output to the speaker, eliminating the bulky series capacitor normally needed with single-ended outputs. Additionally, the device has a Chip Disable pin which, when taken high, sets the outputs to a high impedance state.

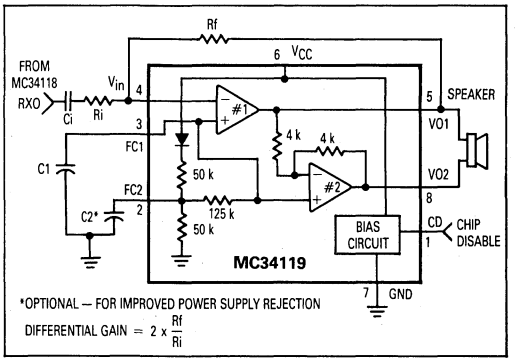


Figure 3. Speaker Amplifier

The dc supply at V_{CC} must be well filtered to prevent oscillations when the speaker amplifier is operating. In a typical line powered circuit, an inductor (1H) is used, in conjunction with a 1000 μF capacitor at V_{CC}, to filter the voltage derived from the loop current. Capacitors C1 and C2 shown in Figure 3 are not used in this application. Instead, bias is provided to Pin 3 from the MC34118's VB pin.

MC145412 Dialer

The dialer is a pulse/tone dialer with 10 number memory, including last number redial (Figure 4). The pulse/tone functions are selectable at Pin 10 (MS). The circuit uses a standard 3.58 MHz crystal, and a standard 3x4 or 4x4 keypad.

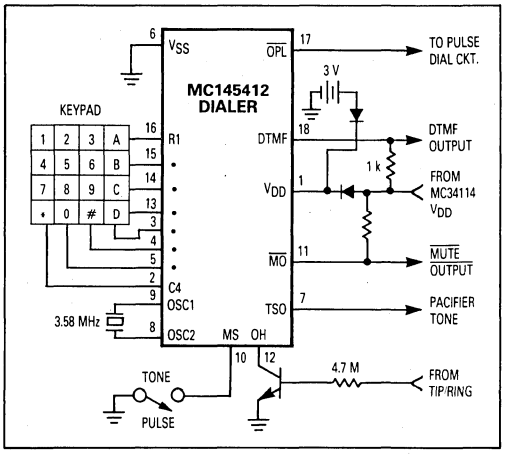


Figure 4. Pulse/Tone Dialer

The NPN transistor at Pin 12 indicates the on-hook/off-hook status to the IC. Power for the dialer is the MC34114's V_{DD} (3.3 volts), diode connected with a memory sustaining battery. The DTMF output goes to C6/R7 of Figure 1.

The $\overline{\text{OPL}}$ ($\overline{\text{OUTPULSING}}$) pin is used to interrupt the loop current when pulse dialing. The pin is an active low open drain. TSO (Tone Signal Output) provides a 500 Hz pacifier tone during pulse dialing. The tone is a square wave, which swing from V_{DD} to V_{SS}.

The $\overline{\text{Mute Output}}$ ($\overline{\text{MO}}$) is active low, open drain and pulls to ground while dialing. It is used to mute the speech paths during dialing.

SWITCHING THE CIRCUIT AROUND

The logic functions involve: a) switching the circuit from handset mode to and from speakerphone mode, b) switching in and out of either dialing mode while in either handset or speakerphone mode, and c) muting the two microphones for the "Privacy" function. Table 1 tabulates the fundamental requirements applicable to any featurephone:

Table 1.

Function	HANDSET		SPEAKERPHONE	
	Mike	R'cvr	Mike	Speaker
Handset Speech	On	On	Off	Off
Handset Dialing	Off	Mute	Off	Off
Handset Mike Mute	Off	On	Off	Off
Speakerphone Speech	Off	Off	On	On
Speakerphone Dialing	Off	Off	Off	Mute
Speakerphone Mike Mute	Off	Off	Off	On

In Table 1, "ON" means fully functional, "OFF" means non-functional, and "MUTE" means partially muted (10 to 20 dB). To apply Table 1 to the specific ICs described previously, the requirements are expanded in Table 2:

Table 2.

Function	MC34114		MC34118		MC34119	Loop	MC145412
	$\overline{MT}$	MS	CD	MUT	CD	Current	MS
Handset Speech	Hi	X	Hi	X	Hi	Thru MC34114	X
Handset Pulse Dialing	Lo	Hi	Hi	X	Hi	Thru MC34114	Open
Handset Tone Dialing	Lo	Lo	Hi	X	Hi	Thru MC34114	Gnd
Handset Mike Mute	Lo	X	Hi	X	Hi	Thru MC34114	X
Speakerphone Speech	Lo	X	Lo	Lo	Lo	To MC34119	X
Speakerphone Pulse Dialing	Lo	Hi	Lo	Hi	Lo	To MC34119	Open
Speakerphone Tone Dialing	Lo	Lo	Lo	Hi	Lo	To MC34119	Gnd
Speakerphone Mike Mute	Lo	X	Lo	Hi	Lo	To MC34119	X

X = Don't Care

A summary of Table 2 is:

a) The MC34114 speech network is put into the Mute mode ($\overline{MT}$ = Lo) not only for dialing, but also to mute the microphone and receiver for the Privacy function (Mike Mute), and when in the speakerphone mode.
b) The MC34118 and MC34119 are disabled for all the handset functions, and enabled for all the speakerphone functions.
c) The MC34118's Mike Mute function is activated for dialing and for the Privacy function.
d) The loop current, which normally flows through the LR pin of the MC34114 (see Figure 1), is directed instead to the MC34119 in the speakerphone mode so as to make the power available to the speaker.
d) The MS pins of the dialer and of the MC34114, are significant only during dialing.

PUTTING IT ALL TOGETHER

Switching Between Handset and Speakerphone Modes

To switch between modes, two actions are necessary: 1) Divert the excess loop current, which normally flows through the MC34114, to the MC34119 during speakerphone mode, and 2) enable and disable the speech network and speakerphone circuits appropriately. The circuit of Figure 5 fullfills those requirements:

HS (3 poles) is the hookswitch operated by lifting the handset. SS (1 pole) activates the speakerphone when the handset is on-hook. The switches are shown on-hook in Figure 5.

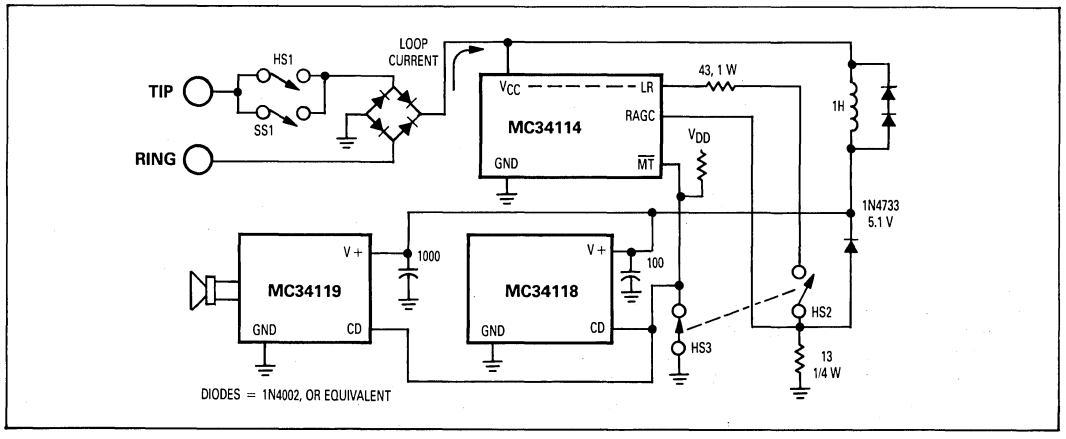


Figure 5. Switching Between Modes

If the handset is on-hook, and switch SS1 is closed (speakerphone mode), the MC34114 uses ≈10 mA internally, but the excess loop current flows through the 1 Henry choke, the zener diode and the 13 Ω resistor. The voltage across the 13 Ω resistor controls the line length compensation function of the MC34114. The MC34118 and MC34119's CD pins are held low by $\overline{HS3}$, enabling the speakerphone circuit. The MC34114's $\overline{MT}$ is low, muting its microphone and receive amplifiers. If the handset is lifted while the speakerphone is in operation, the circuit automatically switches to the handset mode.

When the handset is lifted (HS transfers), the MC34114 consumes ≈10 mA internally, but the excess loop current now flows through the MC34114, out of the LR pin and through the 43 Ω and 13 Ω resistors. The voltage across the 13 Ω resistor still controls the line length compensation. This configuration is similar to that of Figure 1. Since the MC34118 and MC34119 are disabled (their CD pins are pulled high), their current consumption is reduced to <1 mA.

Joining the Receive Paths

Referring to Figure 1, receive signals arriving at Tip and Ring generate a current through the ZB network, into pin 15. That current is modified by A4 and the AGC, made available (as a current) at RXA, and coupled to RXI, where it is converted to a voltage by the receive amplifiers and R8. The ZB network is typically 12 kΩ, and R8 is typically 3.9 kΩ. The receive gain to the handset receiver is therefore nominally −10 dB at low loop currents.

To feed the receive signals to the speakerphone, the circuit of Figure 6 is used.

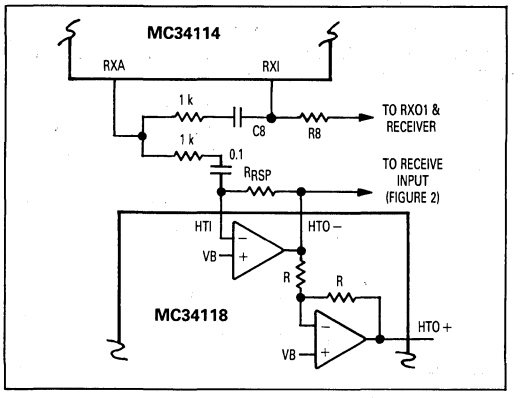


Figure 6. Joining the Receive Paths

The current out of RXA is now split by the 1 kΩ resistors so that approximately half goes to RXI (of the MC34114) via C8, and the other half is converted to a voltage (by the op amp) for the speakerphone's Receive Input (Figure 2). The second op-amp (at HTO+) is unused in this application. The receive gain for the speakerphone (from Tip/Ring to the speaker) is determined by the following equation:

$$G_{RX} = 20 \log \left(\frac{R_{RSP} \times A4 \times AGC \times 0.5}{ZB + 500\ \Omega} \right) + 6\ dB + 20 \log \left(\frac{2 \times Rf}{Ri} \right)$$

The terms A4, ZB, and AGC (from Figure 1) are set at 0.5, 12 kΩ, and 1 respectively for low loop currents. The 0.5 in the first term is due to the current splitting of Figure 6. The +6 dB is the gain of the MC34118's receive attenuator at maximum volume. The third term is the gain of the speaker amplifier.

It is desirable to have as much gain as possible early in the receive path to minimize the effects of noise generated or picked up by the circuit. Since the maximum allowable input at RXI is 350 mVrms, a gain of 3.5 (10.9 dB) was chosen for the first term above, in order to accommodate receive signals of 100 mVrms (−17.8 dBm) at Tip and Ring. R_{RSP} calculates to approximately 160 kΩ. For an overall gain of ≈+30 dB, Rf/Ri must be ≈2.2. At higher loop currents, the overall gain will be ≈+24 dB, due to the line length compensation function.

Joining the Transmit Paths

In the transmit path of Figure 1, the microphone signals are gained up by 30 dB by the mike amplifier. The output at MCO creates a current into TXI through R6 and C5. That current is gained up by 100 by A1 and A2 (assume AGC = 1), and A2's output current then acts on the parallel combination of R1 and the line's ac impedance. Typical values are: R6 = 15 kΩ, R1 = 600 Ω, and 600 Ω for the line's impedance. Neglecting the slight loading of R7, R12, and ZB, the overall handset transmit gain is ≈+36 dB at low loop currents.

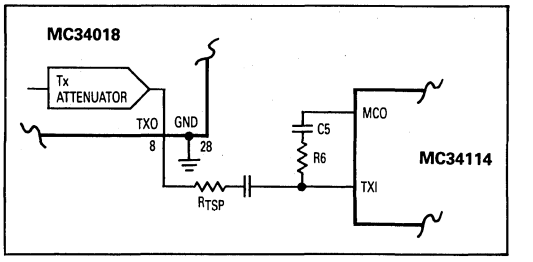


Figure 7. Joining the Transmit Paths

The transmit output from the speakerphone circuit (Figure 2) is applied to the speech network at TXI in Figure 1, through a resistor (R_{TSP}) and a coupling capacitor (see Figure 7). For a nominal gain +40 dB (from the microphone to the MC34114's V_{CC}), R_{TSP} calculates to be ≈11 kΩ. The coupling capacitor (typically 0.1 μF) can be adjusted to set the low frequency rolloff.

Fitting in the Dialer

The DTMF output in Figure 4 is simply connected to C6 and R7 of Figure 1 to get the DTMF signals to Tip and Ring. Using 20 kΩ for R7, and 0.1 μF for C6, DTMF levels of ≈−2.2 dBm will result at Tip and Ring at low loop currents.

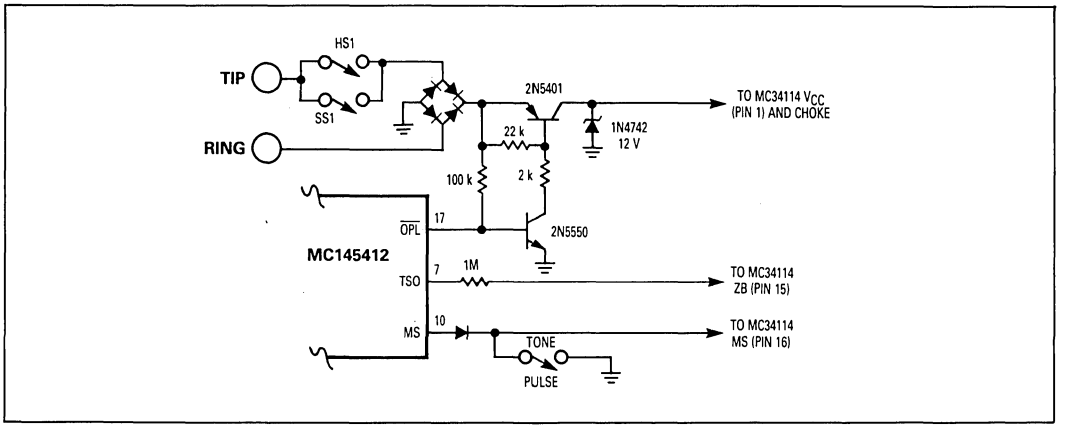


Figure 8. Pulse Dialing Circuit

For pulse dialing, Pin 17 of the MC145412 dialer ($\overline{OPL}$) is connected to a standard two transistor network to interrupt the loop current (Figure 8). The 12 volt zener diode protects the circuitry from voltage spikes during pulse dialing (and whenever a hook switch is opened).

The TSO output (pacifier tone), which is generated only when a keypad button is depressed in the pulse dialing mode, is injected to the MC34114's ZB pin so as to make it available to both the handset receiver and the speakerphone. This tone is not generated during DTMF dialing.

To select between pulse and tone dialing modes, the switch on the dialer's Pin 10 (Figure 4) is connected to the MC34114's MS pin (Pin 16). Since the MC34114's MS pin requires a pull-up resistor for a logic high, a diode must be added (Figure 8) so the dialer's MS pin is open when the switch is in the pulse position.

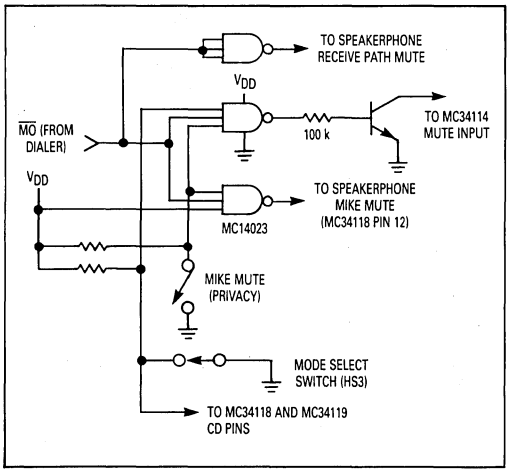


Figure 9. Muting Circuit

Muting and Privacy

The Mute Output of Figure 4 must mute (by at least 45 dB) both microphone paths, and partially mute (10–20 dB) both receive paths during dialing. The privacy (Mike Mute) function requires muting the microphones only by at least 55 dB. This is accomplished with the circuit of Figure 9 using an MC14023 CMOS triple NAND gate. The inputs to the logic circuit are the Mute Output ($\overline{MO}$) from the dialer, the Mike Mute (Privacy) switch and the speakerphone/handset mode select switch HS3 (same as that of Figure 5). The outputs are to the speakerphone's receive path, the MC34114's Mute (which mutes both its transmit and receive paths), the speakerphone's microphone, and to the speakerphone and speaker amp's CD pins. The MC14023 is powered by the MC34114's V_{DD} output.

The circuit of Figure 9 will:

a) Mute the receiver and speaker and disable both microphones during dialing;

b) Disable both microphones when the Privacy switch is closed;

c) Enable either the MC34114 or the MC34118/MC34119 combination in response to the Mode Select

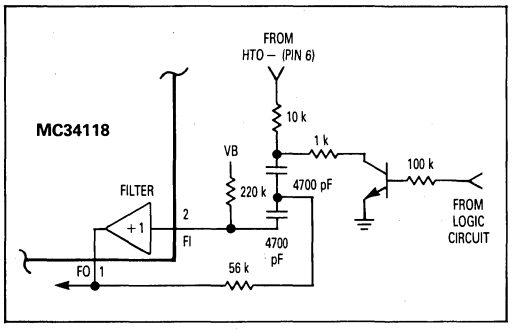


Figure 10. Receive Path Muting

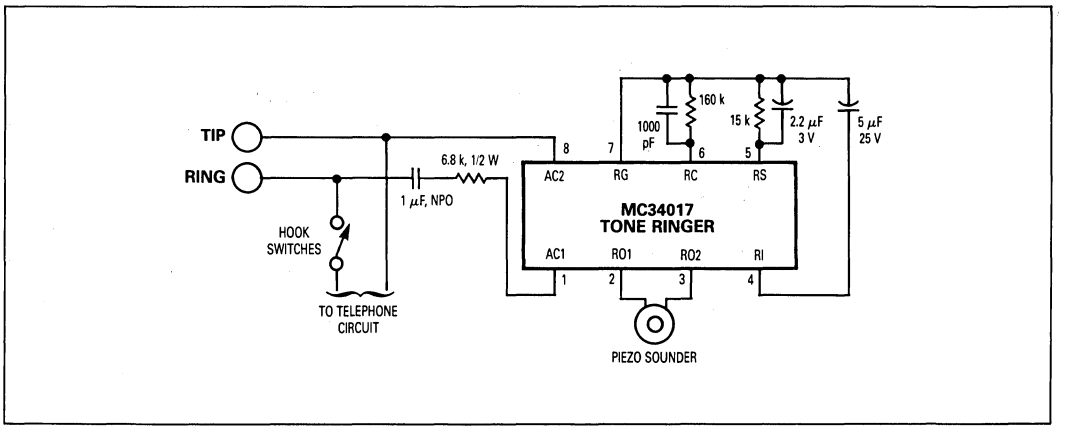


Figure 11. Tone Ringer Circuit

Switch. HS3 is shown on-hook in Figure 9, which enables the speakerphone when SS1 of Figure 5 is closed. (Note: In Figure 5, HS3 is shown controlling the MC34114's $\overline{MT}$ pin directly. In Figure 9 the same function is achieved through the NAND gate).

Muting of the speakerphone's receive path (from the above circuit) is accomplished with the circuit of Figure 10. The muting is inserted in the speakerphone's receive path leading to the filter. Normally, the transistor is off and the 10 k resistor has little effect on the circuit due to the filter's high input impedance (>200 kΩ @ 1 kHz). When Mute is asserted, the signal to the filter is muted by ≈20 dB.

Adding the Tone Ringer

The MC34017 tone ringer circuit, shown in Figure 11, is simply connected directly across Tip and Ring. It is not necessary to disconnect the tone ringer when off-hook. This circuit will provide a ringer with an REN of ≈0.5, and meet all the EIA-470-A and Bell system requirements for impedance, anti-bell tapping and turn-on/off thresholds.

Finally, the Complete Circuit

The complete line-powered featurephone is shown in Figure 12. Some notes concerning this circuit:

a) The resistor and capacitor (R6/C5 shown in Figure 1) between MCO and TXI of the MC34114 was replaced with the network of Figure 12 to provide high frequency roll off.

b) The 13 Ω resistor normally spec'd for R3 of the MC34114 (and shown in Figure 5) was increased to 18 Ω to decrease the point at which line length compensation begins.

c) A 470 μF capacitor was added across the 18 Ω resistor to suppress interaction which occurs between the line length compensation function of the MC34114 and the AGC function of the MC34118.

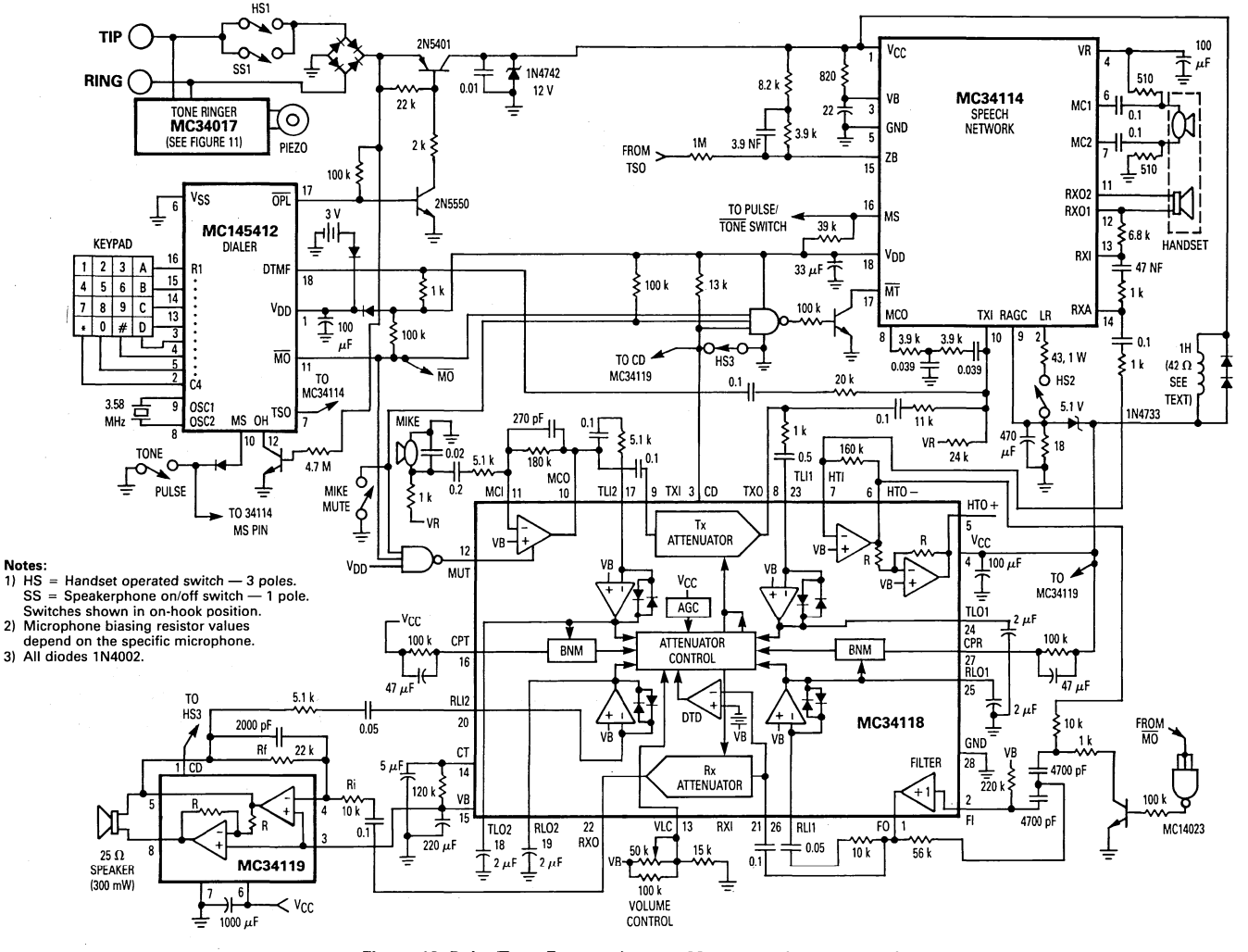
d) The dc resistance of the 1 Henry inductor must be kept below 50 Ω to keep the dc voltage at Tip and Ring and at the MC34114's V_{CC} pin within safe bounds at both low and high loop current values.

The performance curves for this circuit are shown in Figures 13–18. The "Speaker Amp Max Output Swing" is the maximum rms voltage available at the speaker terminals. The transmit gain tests involved replacing each microphone with a signal generator and adjusting for a level of approximately −11 dBm at Tip and Ring into a 600 Ω resistive load. The receive tests involve applying approximately −27 dB to Tip and Ring, and measuring the gain to the receiver or speaker.

As can be seen in Figure 14, the maximum available speaker power is a function of the loop current since all of the speaker current must come from the loop. Consequently, the receive gain for the speakerphone (Figure 17) shows a marked decrease at low loop currents. It must be remembered that in a line powered speakerphone, as the speaker draws current in response to a receive signal, the voltage at Tip and Ring decreases quickly. As the V_{CC} at the MC34119 falls with the Tip and Ring voltage, the speaker amp's output capability is reduced. Consequently, a 25 Ω speaker is recommended for a line powered speakerphone as this makes the best use of the power available from the phone line. A lower impedance speaker will require more current, causing V+ to sag further for a given signal level. A higher impedance speaker draws less current, but produces less sound power.

Additionally, the following muting specs apply:

1) **Handset microphone:** >70 dB while dialing, or when Mike mute switch is closed. 80 dB in speakerphone mode.
2) **Speakerphone microphone:** >90 dB while dialing, in the handset mode, or when the Mike mute switch is closed.
3) **Handset receiver:** ≈17 dB while dialing, or when in the speakerphone mode.
4) **Speaker:** ≈20 dB while dialing, >100 dB when in handset mode.



Notes:
1) HS = Handset operated switch — 3 poles.
   SS = Speakerphone on/off switch — 1 pole.
   Switches shown in on-hook position.
2) Microphone biasing resistor values depend on the specific microphone.
3) All diodes 1N4002.

Figure 12. Pulse/Tone Featurephone w/Memory — Line Powered

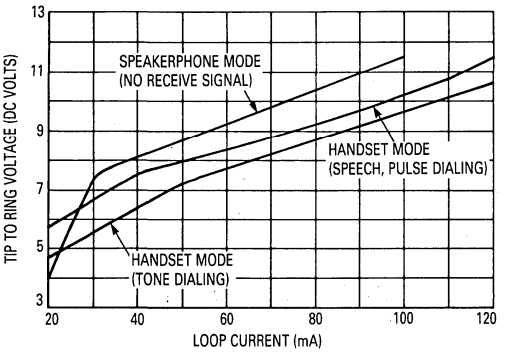


Figure 13. Tip to Ring DC Voltage versus Loop Current

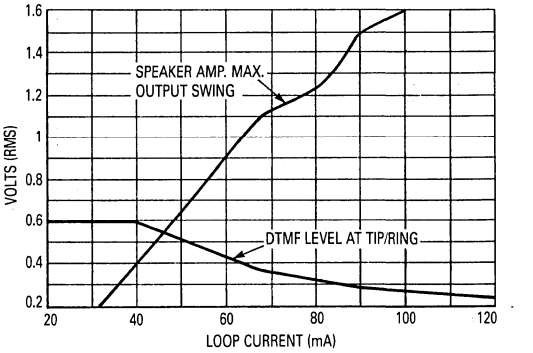


Figure 14. Speaker Amplifier Output and DTMF Level versus Loop Current

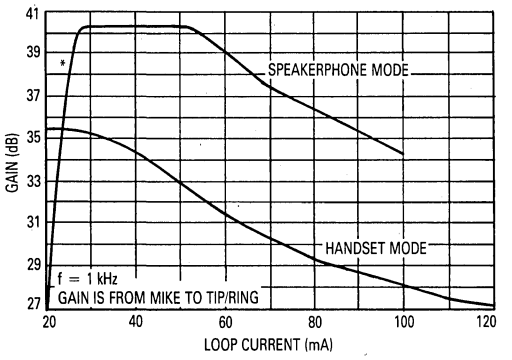


Figure 15. Transmit Gain versus Loop Current

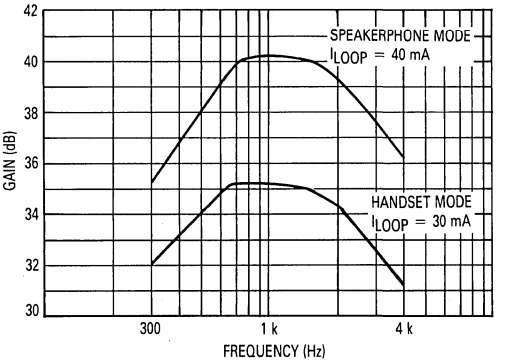


Figure 16. Transmit Gain versus Frequency

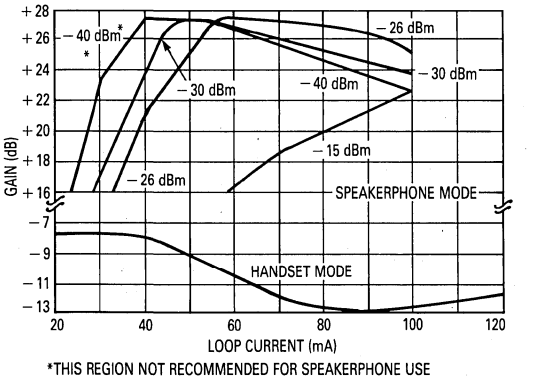


Figure 17. Receive Gain versus Loop Current and Input Signal

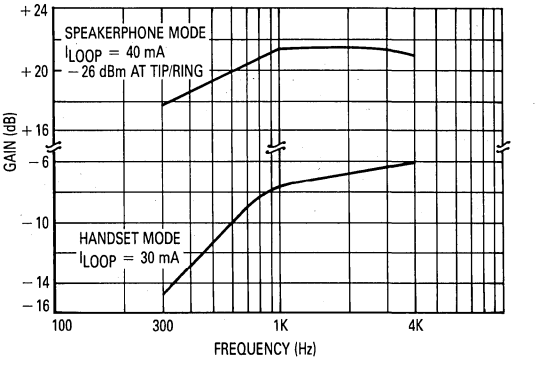


Figure 18. Receive Gain versus Frequency

BOOSTING THE SPEAKERPHONE AT LOW LOOP CURRENTS

Adding a Booster

To improve the performance of the speakerphone at low loop currents (below 40 mA), a minimal cost approach is to add an optional booster to the power supply portion of the MC34119. The approach in this application note is to use a wall mount transformer, similar to calculator chargers. A 6 volt ac Adapter, Radio Shack model #273-1454A, which contains the diode bridge and filter capacitor, was used to minimize the additional circuitry within the speakerphone itself. Since this particular ac adapter is specified for use with Radio Shack's speakerphones, it is this author's assumption that it complies with applicable FCC specifications, although that is not so stated on the transformer.

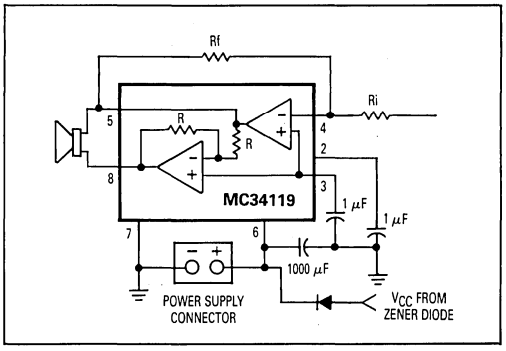


Figure 19. Adding a Speakerphone Booster

This application does not require a regulated voltage from the ac adapter, which further simplifies the design. The circuit of Figure 19 adds the ac adapter to the circuit of Figure 12.

The power supply connector is added to the MC34119 V_{CC} pin, and diode connected to the system's 5.1 volt zener diode of Figure 12. Pin 3 of the MC34119, which previously had been connected to the VB bias line of the MC34118, now is biased from an internal circuit. The 1 μF capacitors on pins 2 and 3 provide power supply noise and ripple rejection.

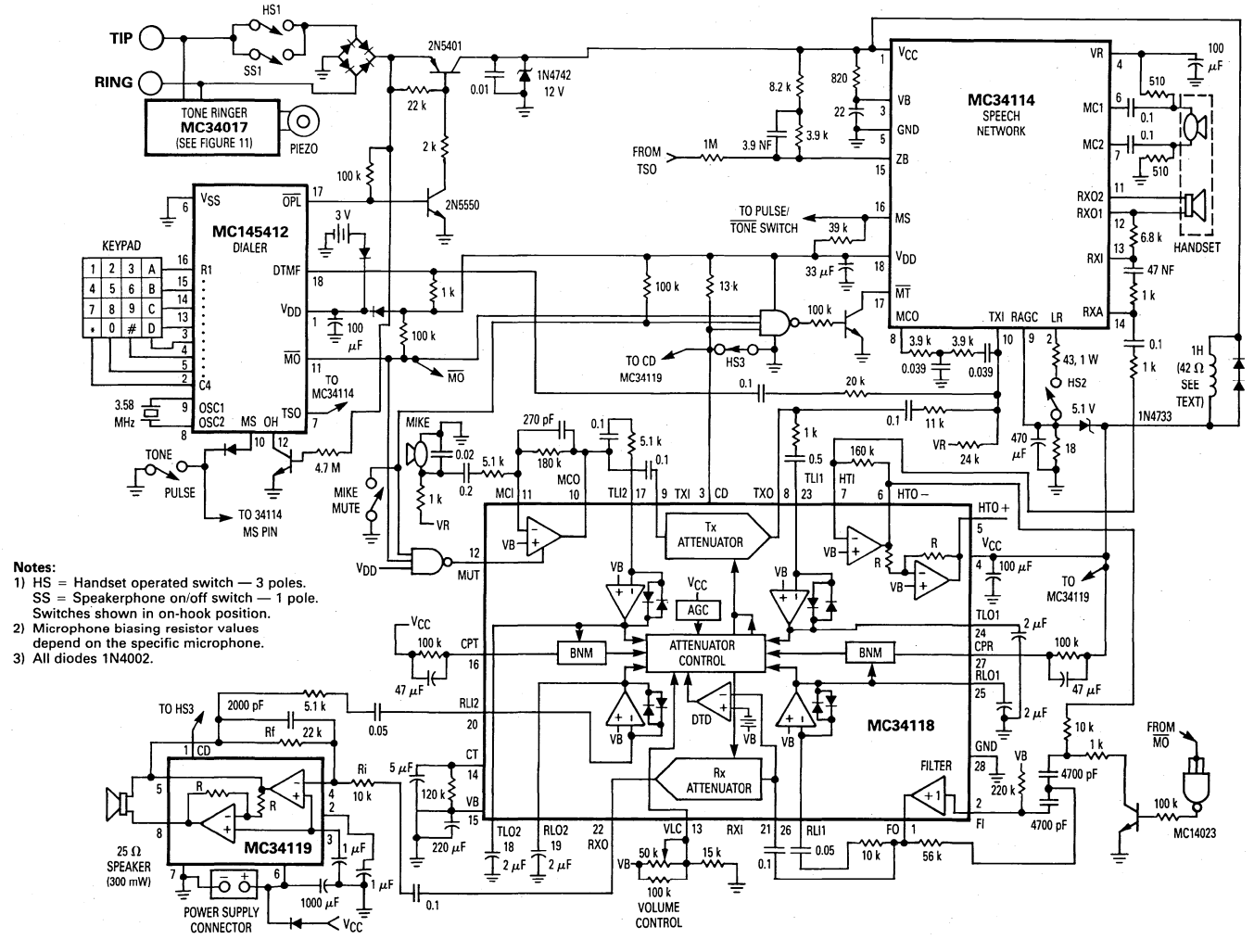
On long lines, where the system V_{CC} tends to sag easily in the presence of receive signals, the booster provides the current to the speaker amplifier. The system V_{CC}, in turn, does not sag, but remains at a stable and consistent level over all values of loop current.

Without the adapter plugged in, the circuit will act similar to that of Figure 12. In the handset mode, the circuit characteristics are the same as that of Figure 12 when it is in the handset mode.

The Complete Circuit with the Booster

The complete circuit is shown in Figure 20. A quick comparison shows it is identical to that of Figure 12, except for the booster section in the lower left hand corner. The performance curves for this circuit are shown in Figures 21–26. As can be seen in Figures 22, 23 and 25, the speakerphone's performance does not degrade below 40 mA as had happened in Figures 14, 15 and 17. The muting specs for this circuit are the same as for Figure 12.

The current required from the booster varies from ≈3 mA (no receive signal) to ≈120 mA with a −15 dBm signal at Tip and Ring.



Notes:
1) HS = Handset operated switch — 3 poles.
   SS = Speakerphone on/off switch — 1 pole.
   Switches shown in on-hook position.
2) Microphone biasing resistor values depend on the specific microphone.
3) All diodes 1N4002.

Figure 20. Pulse/Tone Featurephone w/Memory — Line Powered w/Booster

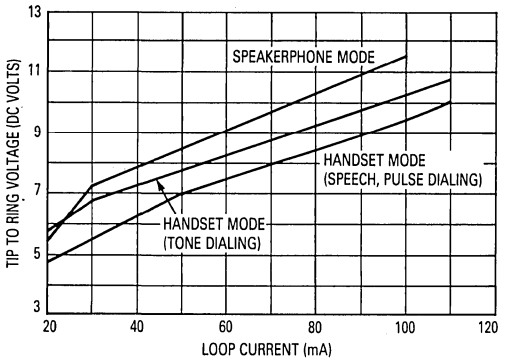


Figure 21. Tip to Ring DC Voltage versus Loop Current

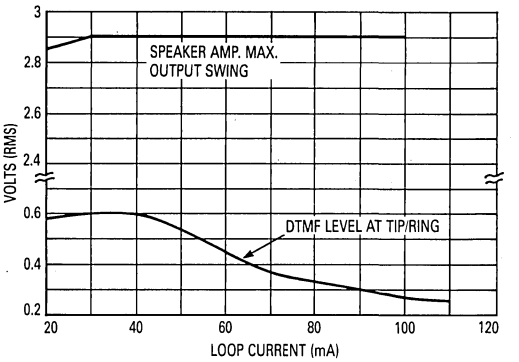


Figure 22. Speaker Amplifier Output and DTMF Level versus Loop Current

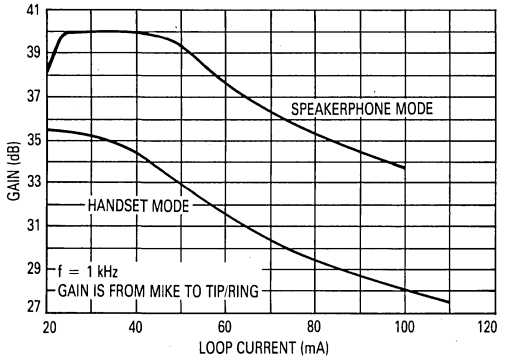


Figure 23. Transmit Gain versus Loop Current

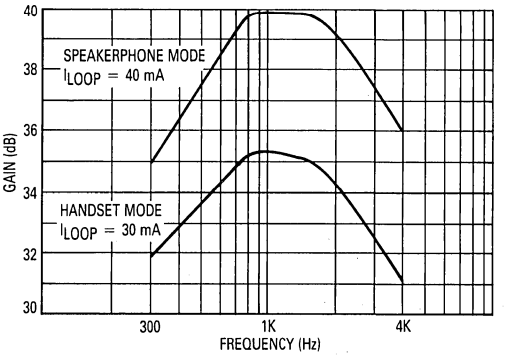


Figure 24. Transmit Gain versus Frequency

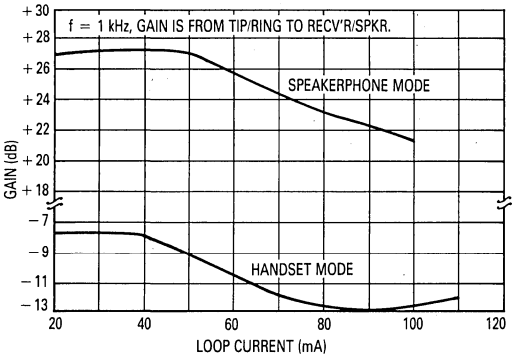


Figure 25. Receive Gain versus Loop Current

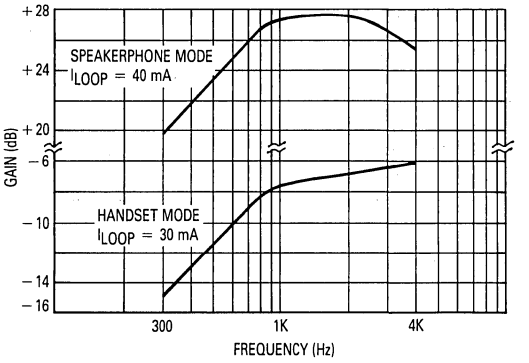


Figure 26. Receive Gain versus Frequency

USING A POWER SUPPLY INSTEAD OF LINE POWER

Using A Transformer

For those cases where it is desirable to power the featurephone from a regulated power supply, rather than from loop current, a transformer is required at Tip and Ring to provide the isolation needed between the phone line and any ac power and earth ground. The primary change to the circuit of Figure 12 is in the area of the Tip and Ring interface, as shown in Figure 27. It must be remembered that loop length compensation is not possible in this circuit since the loop current is not monitored. The MC34114's RAGC pin is grounded in this circuit, setting the transmit and receive gains to maximum.

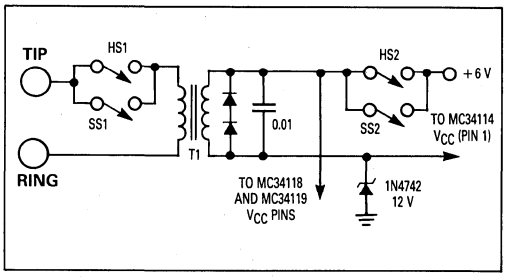


Figure 27. Tip/Ring Interface with a Power Supply

The +6 volt supply powers the MC34114 through the transformer winding. In this manner the speech signals are coupled between the MC34114 and Tip and Ring. The two diodes provide transient clamping, as does the 12 volt zener diode. The MC34118 and MC34119 are powered directly from the +6 volt supply, eliminating the need for the 1H choke. The SS switch (speakerphone on/off) requires one more pole, as shown in Figure 27. The tolerance on the +6 volt supply is ±0.5 volt.

Changes in the Switching and the Dialer

The use of a power supply simplifies the selection of handset versus speakerphone mode of operation. The diversion of the excess loop current is not an issue in this circuit, so the switching of that current is eliminated, along with 5.1 volt zener diode.

Because of the isolation requirement, the MC145412 dialer requires a relay to break the loop current during pulse dialing. Figure 28 depicts this circuit.

The relay is normally off, and energized only for the pulse dialing function. The 1 μF capacitor (rated 250 volts min., NPO) helps absorb the transients generated during pulse dialing.

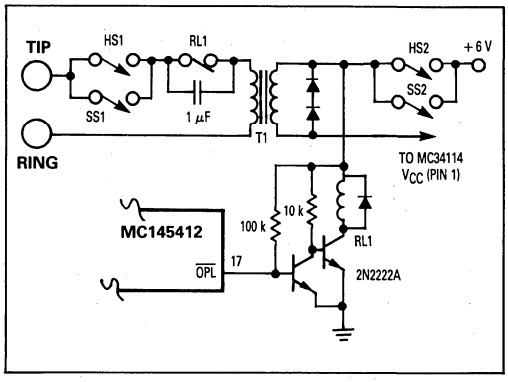


Figure 28. Pulse Dialer Circuit

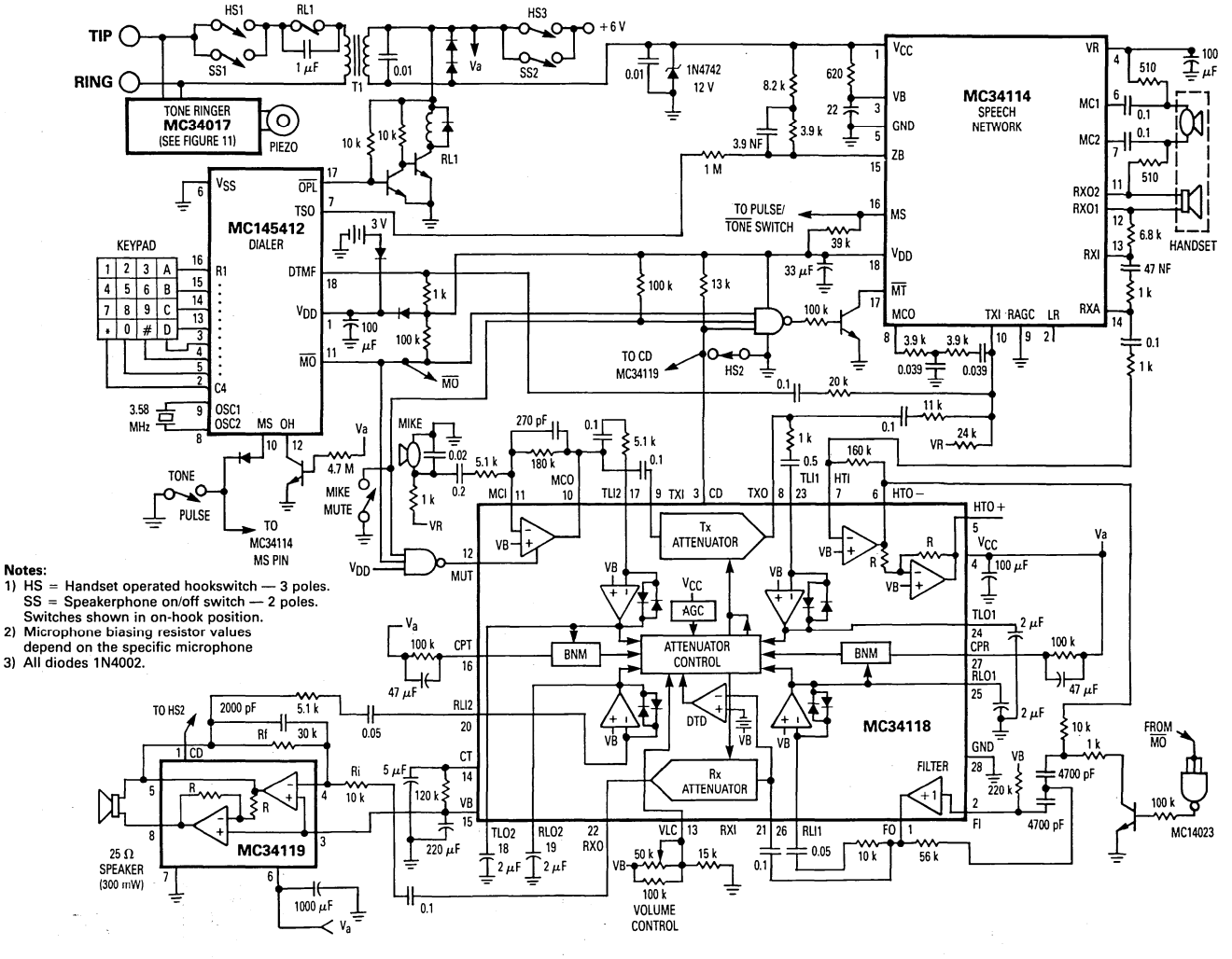
The Complete Circuit with the Power Supply

The complete circuit is shown in Figure 29. The performance curves are shown in Figures 30–35. The Tip to Ring dc voltage (Figure 30), determined solely by the dc resistance of the transformer winding, is somewhat lower than in the previous circuits at low loop currents. Figures 31, 32, and 34 show the performance is fairly constant with loop current, except for a slight reduction in gain at the higher currents. This is due to the characteristics of the transformer used in developing this circuit (model #TTPC-13 from Stancor, Inc.). Also noticeable in the curves, compared to Figures 13–18 and 21–26, is the lack of loop length compensation — a natural consequence of this type of circuit.

The muting specifications for this circuit are the same as for the line powered circuit. The current required from the +6 volt power supply is as follows:

a) Handset mode: ≈13 mA.
b) Speakerphone mode (no sound at the speaker): ≈24 mA.
c) Speakerphone mode (max. volume at the speaker): ≈144 mA.

Although Figure 29 indicates the use of a 25 ohm speaker, any impedance speaker within the range of 8 to 50 Ω can be used, since this circuit is not line powered. The receive gain may have to be adjusted, however, if a different speaker is used.



Notes:
1) HS = Handset operated hookswitch — 3 poles.
   SS = Speakerphone on/off switch — 2 poles.
   Switches shown in on-hook position.
2) Microphone biasing resistor values depend on the specific microphone
3) All diodes 1N4002.

Figure 29. Pulse/Tone Featurephone w/Memory — Powered From a Power Supply

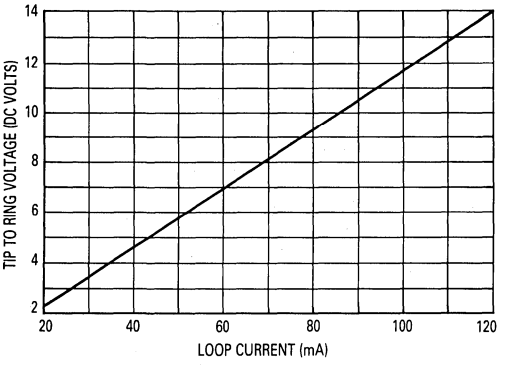


Figure 30. Tip to Ring DC Voltage versus Loop Current

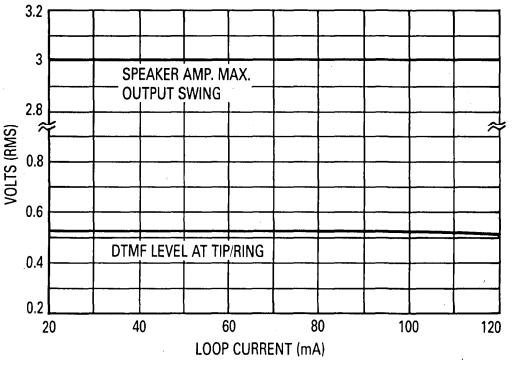


Figure 31. Speaker Amplifier Output and DTMF Level versus Loop Current

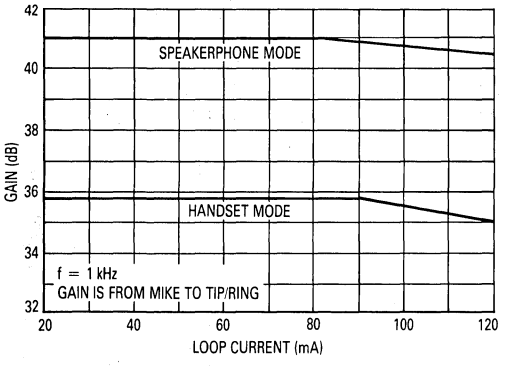


Figure 32. Transmit Gain versus Loop Current

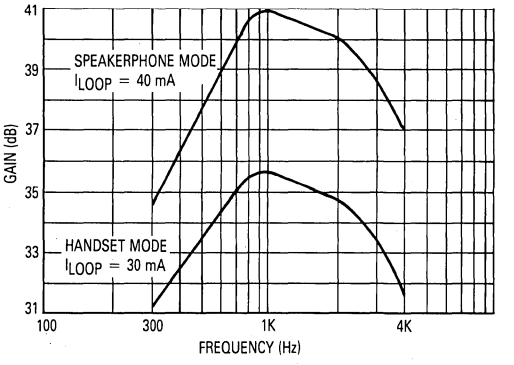


Figure 33. Transmit Gain versus Frequency

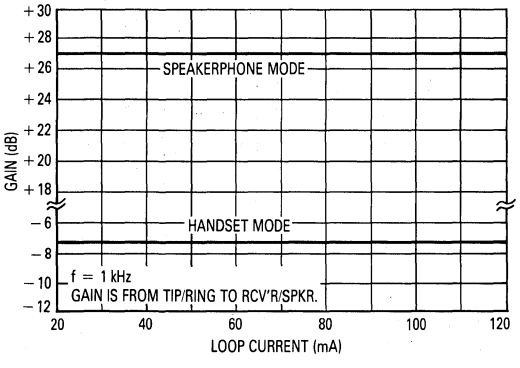


Figure 34. Receive Gain versus Loop Current

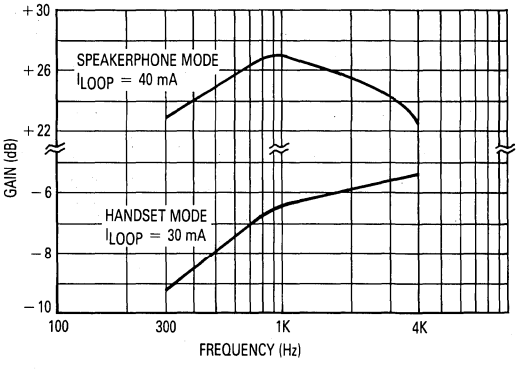


Figure 35. Receive Gain versus Frequency

CONSTRUCTION HINTS

Board Layout

The filter capacitor for the speakerphone IC and for the speaker amp (typically 100 μF and 1000 μF respectively) must be physically adjacent to the ICs, within 1". This is particularly important in the line-powered versions, where V_{CC} can vary with the speech intensity. Since most of the current is used in the speaker amplifier, the PC board track leading to Pin 6 of the MC34119 should be laid out with care, preferably close to the zener diode, or the power supply connector. The ground tracks should be as wide as possible, and laid out with care.

EMI Susceptibility

Potential EMI susceptibility problems should be addressed early in the electrical and mechanical design of the speakerphone. EMI may enter the circuit through Tip and Ring, through the microphone wiring to the amplifiers, or through any of the PC board traces. The most sensitive pins on the MC34118 are the inputs to the level detectors (RLI1, RLI2, TLI1, and TLI2) since, when there is no speech present, the inputs are high impedance and these op amps are in a near open loop condition. These board traces should be kept short, and the resistor and capacitor for each input should be physically close to the pins. Other high impedance input pins (MCI, VLC, HTI, FI) should be considered sensitive to EMI signals.

The microphone wires within the handset cord can act as an antenna, and pick up nearby radio stations. If this is a problem in the final design, adding RF filters (consisting of ferrite beads and small (0.001 μF) ceramic capacitors) to the PC board where the wires attach to the board can generally reduce the problem.

Acoustics

a) In the design of any speakerphone, acoustics are extremely important, and **must** be considered from the very beginning. Building a breadboard with the microphone and speaker "hanging out in mid air" simply **will not work!!!** One of the most common problems in a speakerphone design is acoustic feedback (the speaker is closely coupled to the microphone) which results either in oscillations (2–10 kHz) or "motor-boating" (1–10 Hz switching). A properly designed enclosure for the finished product should provide at least 50 dB of acoustic loss (speaker drive voltage to microphone output voltage). The physical location of the microphone, along with its characteristics, will play a large role in the quality of the transmitted sound. The microphone and speaker vendors can usually provide additional information on the use of their products.

b) The quality of the speaker, and the acoustic cavity in which it resides, have a major impact on the quality of the sound. A little time spent here can go a long way towards improving the sound of the finished speakerphone. As a general rule, good electronics cannot compensate for poor acoustics and/or low speaker quality.

In the Final Analysis . . .

In the final analysis, the circuits shown in this application note will have to be "fined tuned" to match the acoustics of the enclosure, and the specific microphone and speaker selected. The component values shown in this application note should be considered as starting points only. The gains of the transmit and receive paths are easily adjusted at key points in the circuits (see appropriate text). The switching response of the speakerphone can then be fine tuned by varying (in small steps) the components at the level detector inputs until satisfactory operation is obtained for both long and short lines. The references can be consulted for additional speakerphone design theory.

GLOSSARY

Attenuation — A decrease in magnitude of a communication signal, usually expressed in dB.

Bandwidth — The range of information carrying frequencies of a communication system.

C-Message Filter — A frequency weighting which evaluates the effects of noise on a typical subscriber's system.

Central Office — Abbreviated CO, it is a main telephone office, usually within a few miles of its subscribers, that houses switching gear for interconnection within its exchange area, and to the rest of the telephone system. A typical CO can handle up to 10,000 subscriber numbers.

dB — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:
10 x log (P_1/P_2) for power measurements, and
20 x log (V_1/V_2) for voltage measurements.

dBm — An indication of signal power. 1 mW across 600 Ω, or 0.775 volts rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:
dBm = 20 x log (Vrms/0.775), or
dBm = [20 x log (Vrms)] + 2.22.

dBmp — Indicates dBm measurement using a psophometric weighting filter.

dBrn — Indicates a dBm measurement relative to 1 pW power level into 600 Ω. Generally used for noise measurements, 0 dBrn = −90 dBm.

dBrnC — Indicates a dBrn measurement using a C-message weighting filter.

dBrnC0 — Noise measured in dBrnC referred to zero transmission level.

DTMF — Dual Tone Multi-Frequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad.

Four Wire Circuit — The portion of a telephone, or central office, which operates on two pairs of wires. One pair is for the Transmit path (generally from the microphone), and one pair is for the Receive path (generally to the receiver).

Full Duplex — A transmission system which permits communication in both directions simultaneously. The standard handset telephone is full duplex.

Gain — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Half Duplex — A transmission system which permits communication in one direction at a time. CB radios, with "push-to-talk" switches, and voice activated speakerphones, are half duplex.

Hookswitch — A switch which connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Line Length Compensation — Also referred to as loop compensation, it involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less, and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length.

Loop — The loop formed by the two subcriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or ac power.

Loop Current — The dc current which flows through the subscriber loop. Typically provided by the central office or PBX, it ranges from 20 to 120 mA.

Off Hook — The condition when the telephone is connected to the phone system, permitting the loop current to flow. The central office detects the dc current as an indication that the phone is busy.

On Hook — The condition when the telephone is disconnected from the phone system, and no dc loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange. In effect, a miniature central office, it is a customer owned switching system servicing the phones within a facility, such as an office building. A portion of the PABX connects to the Bell (or other local) telephone system.

Pulse Dialing — A dialing system whereby the loop current is interrupted a number of times in quick succession. The number of interruptions corresponds to the number dialed, and the interruption rate is typically 10 times per second. The old rotary phones, and many new pushbutton phones, use pulse dialing.

REN — Ringer Equivalence Number. An indication of the impedance, or loading factor, of a telephone bell or ringer circuit. An REN of 1 equals ≈8 k ohms. The Bell system typically permits a maximum of 5 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

Ring — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

Sidetone — The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2-to-4 wire conversion system. Sidetone was recognized by Alexander Graham Bell as necessary for a person to be able to speak properly while using a handset.

Speech Network — A circuit which provides 2-to-4 wire conversion, i.e. connects the microphone and receiver (or the transmit and receive paths) to the Tip and Ring phone lines. Additionally it provides sidetone control, and in many cases, the dc loop current interface.

Subscriber Line — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

Tip — One of the two wires connecting to the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to Ring.

Tone Ringer — The modern solid state equivalent of the old electromechanical bell. It provides the sound when the central office alerts the subscriber that someone is calling. Ringing voltage is typically 80–90 Vrms, 20 Hz.

Two-Wire Circuit — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

Voiceband — That portion of the audio frequency range used for transmission across the telephone system. Typically it is 300–3400 Hz.

REFERENCES

MC34118 Data Sheet, April, 1987, Motorola Inc.
MC34119 Data Sheet, March, 1988, Motorola Inc.
MC34017 Data Sheet, January, 1984, Motorola Inc.
MC34114 Product Preview Data Sheet, Sept. 1987, Motorola Inc.
MC145412 Data Sheet, February, 1987, Motorola Inc.
Busala, A., Fundamental Considerations in the Design of a Voice Switched Speakerphone, B.S.T.J., 39, 1960, p. 265.

SUGGESTED VENDORS

Microphones

Primo Microphones Inc.
Bensenville, Ill. 60106
312-595-1022
Model EM-60

MURA Corp.
Westbury, N.Y. 11590
516-935-3640
Model EC-983-7

Hosiden America Corp.
Elk Grove Village, Ill. 60007
312-981-1144
Model KUC2123

25 Ω Speakers

Panasonic Industrial Co.
Seacaucus, N.J. 07094
201-348-5233
Model EAS-45P19S

Telecom Transformers

Microtran Co., Inc.
Valley Stream, N.Y. 11528
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Ask for Applications
Bulletin F232

Stancor Products
Logansport, IN 46947
219-722-2244

PREM Magnetics, Inc.
McHenry, Ill. 60050
815-385-2700

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Minneapolis, MN 55437
612-921-5600

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MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

Linearize the Volume Control of the MC34118 Speakerphone

Prepared by
Dennis Morgan
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The volume control level of the MC34118 speakerphone IC has a nonlinear relationship with respect to the position of the volume control potentiometer, evident in Figure 14 of the data sheet. Since the input impedance at VLC (Pin 13) is very high, the horizontal axis in the graph of Figure 14 can be said to represent the potentiometer's mechanical position (using a linear taper potentiometer), with the two extreme ends of the potentiometer's position at 0.3 and 1.0. As can be seen, the gain changes at a slow rate when near maximum volume, but changes rapidly when near the minimum volume setting.

By changing the potentiometer/resistor circuit to that shown in Figure 1 (below), the volume control relationship is linearized to an almost perfect straight line (the values were selected to maintain [VLC = 0.3 x VB] at minimum volume). The result is shown in Figure 2 (below), with the only nonlinearity near the maximum volume end (the vertical axis is the gain of the receive attenuator). The circuit requires the addition of only one resistor. The potentiometer can be rotary, or a linear movement type, as long as it has a linear taper.

Figure 1.

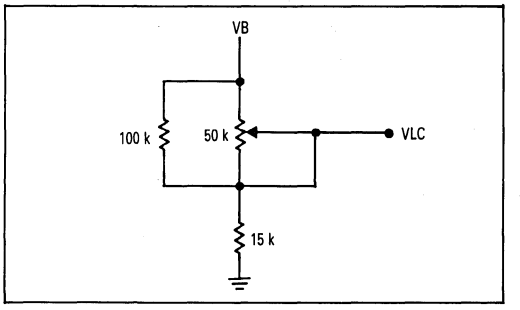
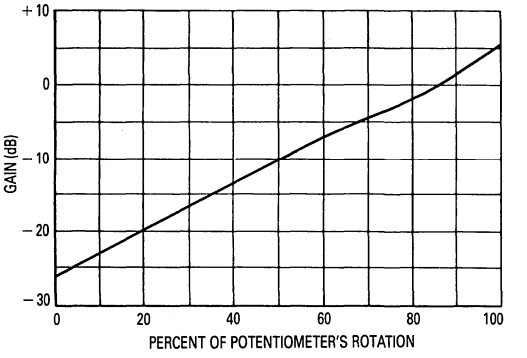


Figure 2.



Thanks to Alan Long (Motorola, Toulouse) for this circuit idea.

Engineering Bulletin

By Tanya Tussing and Glen Zoerner
Telecommunication Applications
Austin, Texas

THE APPLICATION OF A TELEPHONE TONE RINGER AS A RING DETECTOR

Telephone ringers are driven by high voltage, low frequency ac signals which are superimposed on the 48 volt dc tip-ring feed voltage. An electronic ring detector must sense the presence of an ac signal on the line and produce a dielectrically isolated logic level to the system processor. To isolate the line from the system, an on-chip piezoelectric driver drives the LED of an optocoupler. A 1 μF capacitor filters the transistor output of the optocoupler, creating a solid logic 0 when a ring signal is present. Figure 1 depicts the schematic of the ring detector. The peripheral components around the MC34012 set trigger levels and the ringing impedance signature for FCC Part 68 compliance.

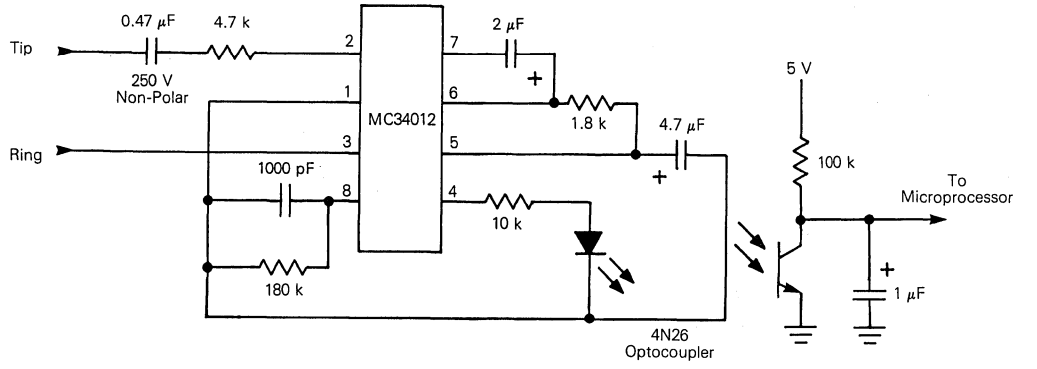


FIGURE 1 — Ring Detector Schematic

LSI for Telecommunications

a one-chip telephone

W. DAVID PACE
Motorola, Inc.
Tempe, Arizona

In recent years, a number of integrated circuits — such as DTMF dialers, speech networks, and tone ringers — have been developed for telephone applications. These products have replaced electromagnetic elements of the telephone because of performance and cost improvements achievable with integrated systems. In addition, the use of integrated circuits in telephones provides considerable freedom in the external design of telephone sets from both the practical and aesthetic points of view.

With these objectives in mind, a single-chip telephone circuit has been developed. The MC34010 Electronic Telephone Circuit (ETC) provides all the functions of a standard tone-dialing telephone. In addition, a microprocessor interface port facilitates automatic dialing features. An important characteristic of the ETC is its ability to operate with instantaneous input voltages as low as 1.4 V. Low-voltage operation is a key requirement in North American telephone networks, where parallel connections are common.

FUNCTIONAL BLOCKS OF THE MC34010 ETC

Figure 1 shows the elements of the ETC:

- **Line Voltage Regulator:** provides the dc termination of the subscriber loop and a bias voltage for the DTMF dialer and speech network.
- **DTMF Dialer:** generates the appropriate dual-tone multi-frequency (DTMF) signals for dialing.
- **MPU Interface:** allows the DTMF generator to be controlled by a separate microprocessor, which may be programmed to provide automatic dialing features.
- **Speech Network:** provides the two-wire to four-wire interface between the telephone line and the receiver and microphone of the handset.
- **Tone Ringer:** converts the ac ringing signals from the exchange into a warbled tone emitted through a piezo sound element.

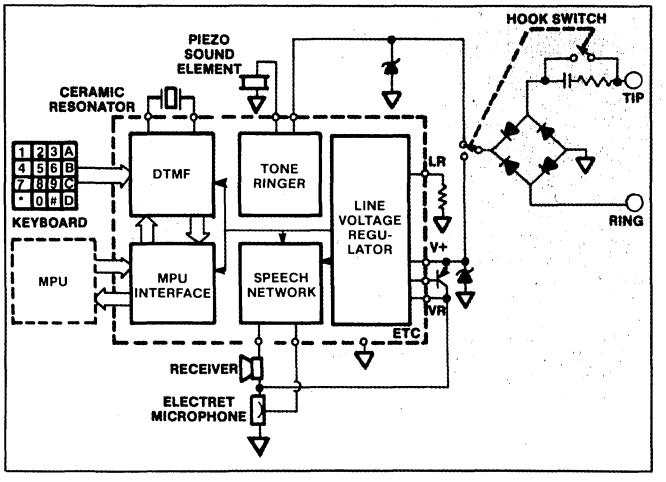


Fig. 1 Major elements of the MC34010 ETC.

Line Voltage Regulator

The line voltage regulator provides a regulated bias voltage at the VR terminal of 1.1 V to other sections of the ETC. The low saturation voltage of an external PNP pass transistor allows the line input voltage to fall within 300 mV of VR voltage without clipping signals on the line. Thus, the DTMF and speech circuits maintain specified performance with instantaneous line voltages as low as 1.4 V.

The circuit associated with the LR terminal determines the dc resistance of the telephone. At low line voltages (corresponding to operation in parallel with nonelectronic telephones), the ETC draws only 5 mA of bias current for the speech network and keypad interface circuits. When the V+ terminal voltage exceeds 3 V, excess line current flows through an external resistor at terminal LR. The 3-kV level shift from V+ to LR prevents saturation of the dc termination circuit with signals up to 2 V peak (+5 dBm) on the line.

An internal constant current sink nominally equal to the bias current of the DTMF dialer also flows through the dc termination circuit. When the DTMF dialer is activated, this current sink is disabled to reduce the line current transient and dialer clicks.

DTMF Dialer

Inexpensive telephone keypads have switches of the single pole/single throw (SPST) type that connect the row and column terminals corresponding to the selected digit. A keypad interface circuit within the ETC, consisting of input resis-

tors, comparators, and decoding logic, activates the DTMF tone generators whenever two keypad input terminals are connected.

When the keypad interface activates the DTMF generator, it also produces a mute signal for the speech network. This mute signal disables the transmit amplifier and reduces the DTMF sidetone in the receiver. Muting the receiver also suppresses clicks associated with DTMF turn-on and turn-off transients.

The row and column tone generators include a programmable counter, an encoder, and a digital-to-analog (D/A) converter. The output of the D/A converter is a stair-step approximation of a sine wave with 16-step intervals per period. Fourier analysis of such a waveform reveals that the time intervals corresponding to the positive and negative peaks (first and ninth intervals) can be shortened or lengthened with little impact on distortion. By modifying the division ratio of the programmable counter during these peak intervals, output frequency errors are reduced. The periods of the DTMF tones are adjusted to the desired value within the resolution afforded by the 500-kHz oscillator frequency.

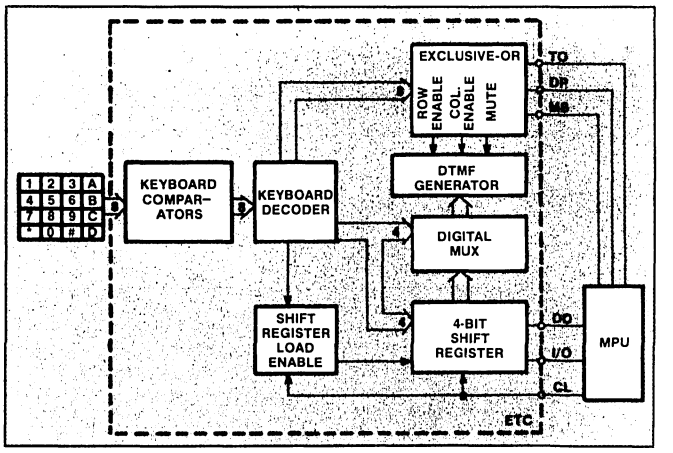


Fig. 3 The MPU interface circuit.

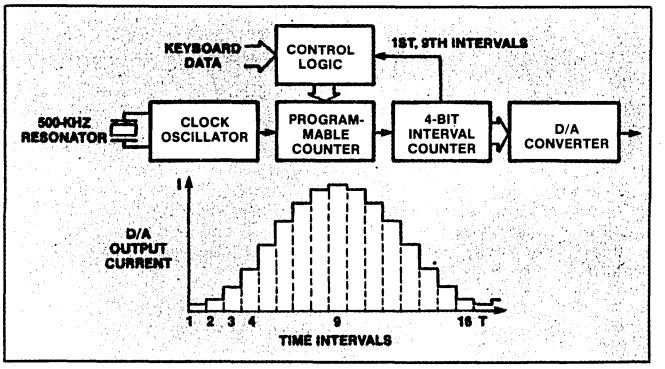


Fig. 2 The DTMF frequency synthesis technique.

Figure 2 depicts the implementation of this error reduction technique. The programmable counter divides the 500-kHz clock frequency by a number N that is loaded by the control logic at the beginning of each step. The output frequency of the programmable counter is further divided by the 4-bit interval counter. It is this counter which distinguishes the 16 waveform intervals. The output of the 4-bit counter drives the D/A converter through an encoder (not shown in **Figure 2** for simplicity).

Consider, for example, the generation of the 697-Hz Row 1 tone. For 14 of the 16 waveform intervals the control logic loads the programmable counter with a divisor of 45. For the first and the ninth intervals, however, feedback from the 4-bit interval counter causes the control logic to program the counter to divide by 44. This combination of divisors reduces the 500-kHz clock frequency to 11.14 kHz at the output of the programmable counter. The interval counter divides this signal by 16, producing a 696.4-Hz Row 1 tone. The desired frequency of 697 Hz, therefore, is synthesized with an error of only 0.09 percent.

Other DTMF tones are generated by loading the programmable counters with appropriate pairs of divisors. The worst-case frequency-division error for the eight dialing tones is 0.16 percent. Reducing the divider errors permits an inexpensive 500-kHz ceramic resonator to be used for DTMF clock generation instead of a more precise quartz crystal. In addition, the lower clock frequency allows the counter to be fabricated in a linear-compatible integrated injection logic (I^2L) technology which enhances the performance of the analog sections of the ETC.

The outputs of the row and column D/A converters are summed in the proper proportion (with a 2-dB twist) and amplified to drive the telephone line. The amplitude of the line's signal is determined by an external resistor. Feedback around the DTMF output amplifier reduces the dialing-mode output impedance to 2 kΩ to satisfy return-loss specifications.

MPU Interface

The MPU interface permits communication between the telephone keypad, the DTMF dialer, and a microprocessor. Through this port, telephone numbers may be stored in the microprocessor and later retrieved for automatic dialing. **Figure 3** shows the major blocks of the MPU interface section and the connections between the keypad, DTMF dialer, and microprocessor.

Each button of a 12- or 16-number keypad is represented by a 4-bit code. This same code controls the programmable counters to generate

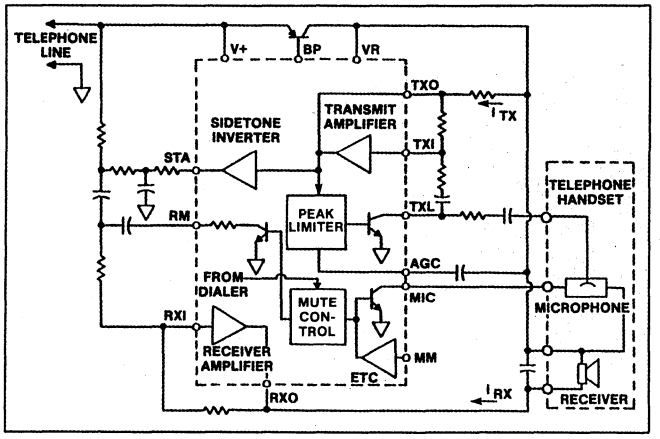


Fig. 4 Speech network block diagram.

the appropriate row and column tones. Binary words corresponding to keypad digits are transmitted serially to or from the microprocessor via the 4-bit shift register. The direction of data flow is determined by the state of the DD terminal input.

In the manual dialing mode, DD is a logic "0"; the 4-bit code from the keypad is fed to the DTMF generator and also loaded into the shift register. The microprocessor-controlled clock shifts the data through the I/O terminal on negative clock transitions. The shift register load-enable circuit cycles the register between the load and shift modes such that multiple read cycles may be provided to the microprocessor for a single key closure. Six complete clock cycles will output a 4-bit word from the ETC and reload the shift register for a second look.

In the automatic dialing mode, DD is a logic "1" and a 4-bit code is entered from the microprocessor into the ETC. The shift register load-enable circuit is disabled in this mode. Only four clock cycles are required to transfer a digit to be dialed into the ETC. A logic "1" on the TO terminal disables the DTMF output until valid data from the microprocessor is in place. Subsequently, TO is switched to a logic "0" to generate a DTMF tone pair on the line.

An exclusive OR circuit in the keypad interface logic determines if more than one key is depressed. Single tones may be initiated by depressing two keys in the same row or column. The exclusive OR circuit also generates the DP and MLS output signals. DP indicates when one and only one key is depressed, thereby signaling the microprocessor that valid data are available. MS indicates when the DTMF generator is enabled and the speech network is muted.

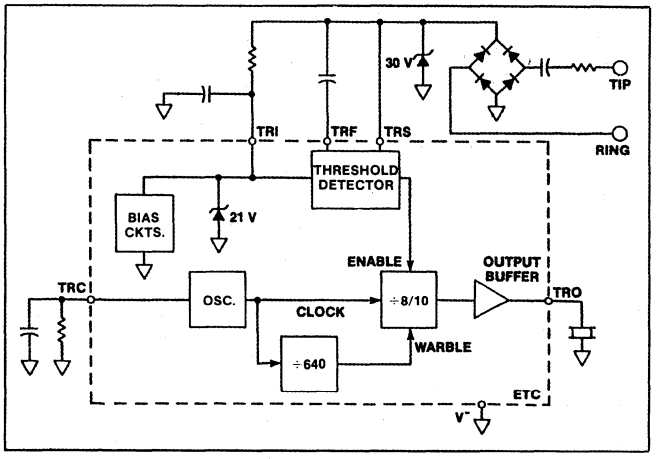


Fig. 5 Tone ringer block diagram.

Speech Network

The speech network illustrated in **Figure 4** provides the two- to four-wire interface between the telephone line and the transmit and receive transducers. The key feature of this circuit is its ability to operate with instantaneous line voltages as low as 1.4 V. Satisfactory operation has been demonstrated in parallel with a carbon microphone telephone for loop resistances of up to 2200 Ω. This corresponds to 27,000 ft of 26 AWG cable between the subscriber terminal and the local exchange.

An electret microphone biased by the VR regulator drives the transmit amplifier. The microphone is muted internally by the dialer during DTMF signaling and may be muted by the control signal on the MM terminal.

For very loud talkers, the peak limiter reduces the transmit amplifier input level to maintain low harmonic distortion. Transmit gain control is achieved by varying the saturation resistance of the transistor which drives the TXL terminal. This transistor operates as a variable resistance because its collector terminal is unbiased. The peak limiter circuit determines when the transmit amplifier output approaches the clipping level and drives the transistor at TXL to attenuate the amplifier input. The peak limiter typically provides 30-dB additional dynamic range with approximately 1 percent total distortion.

As shown in **Figure 4,** the transmit amplifier output signal is inverted at the STA terminal to provide sidetone cancellation at the receiver. The signals from the telephone line and the STA terminal are summed at the input at the receive amplifier. When transmitting, these signals are nominally 180° out of phase and the proper choice of external components will nullify the

transmitted signal in the receiver. In practice, phase shift from the transmit amplifier output to the line due to reactive line impedances limits the degree of sidetone cancellation achieved.

The receive amplifier output produces a signal current in the receive transducer that also flows through the VR regulator to the telephone line. This ac current determines the impedance of the telephone at the interface with the line. The input impedance is set by the proper choice of receive amplifier gain and receiver impedance. A 300-Ω receiver driven with a gain of one-half results in a 600-Ω input impedance and satisfactory receive sensitivity.

Tone Ringer

The tone ringer responds to large signal ac input voltages with a warbled two-tone output signal which may drive a piezo transducer or speaker. This warbled tone is produced by dividing the tone ringer oscillator frequency alternately by 8 or 10 as shown in **Figure 5.** The warble rate is the oscillator frequency divided by 640. In a typical application, an 8-kHz oscillator produces 800-Hz and 1000-Hz tones warbling at 12.5 Hz.

The tone ringer output is enabled by the threshold detector when a ringing signal greater than 35 Vrms is applied at tip and ring. The ringing signal level is measured by monitoring the voltage across the external resistor at the TRI terminal. When the average voltage across this resistor exceeds a threshold level, the output buffer commences driving the piezo element at the TRO terminal. The additional current drawn from the line to drive the piezo also flows through the external resistor at TRI. Therefore, the voltage across this resistor increases when the output is enabled. Increasing the voltage applied to the threshold detector creates hysteresis between the turn-on and turn-off levels that ensures clean on/off transitions.

DESCRIPTION

The MC34010 ETC incorporates 300 bipolar transistors and 520 I^2L gates on a 125 x 146 mil die. The chip is fabricated using a two-layer metal, Linear/I^2L process and packaged in a 40-pin plastic package. Combining a dialer, speech network, and tone ringer on a single chip represents a major step forward in the modernization and cost reduction of analog telephones. □

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Adding Digital Volume Control To Speakerphone Circuits

Prepared by
Dennis Morgan
Bipolar Analog IC Division

INTRODUCTION

The volume control provided on many speakerphones is a potentiometer, some rotary and some linear, wired so the wiper provides a varying DC voltage to a variable gain stage. This application note will describe how to replace the potentiometer with a digital circuit which allows control of the speaker volume from a set of "UP" and "DOWN" pushbutton switches. The circuit uses only 3 standard CMOS ICs.

THE MC34018 AND MC34118

The volume control pins (VLC) on the MC34018 and MC34118 speakerphone ICs (Pins 24 and 13 respectively) are similar in they have a very high input impedance (>10 MΩ) and low bias current (+0.2 μA for the MC34018, −60 nA for the MC34118). Additionally, they both function similarly in that the volume control operation is based on the ***ratio*** of the voltage at VLC to the internally generated reference voltage (V_B shown in Figure 1). The ratio is 1.0 (VLC = V_B) for maximum volume, and less than 1 for reduced volume. The minimum recommended setting is 0.55 V_B for the MC34018, and 0.3 V_B for the MC34118.

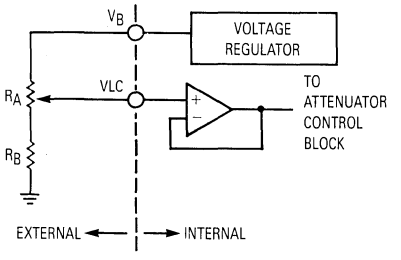

Figure 1. Analog Volume Control Interface

To achieve the same voltage range at VLC with a digital circuit, a binarily weighted resistor network is employed (see Figure 2).

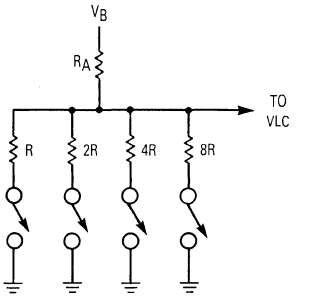

Figure 2. Digital Volume Control Resistor Network

With all switches open, VLC equals V_B (maximum volume). The minimum setting occurs when all switches are closed, and the R_B in Figure 1 is represented by the parallel combination of the four lower resistors (0.533R). The exact value of the resistors will be determined later.

USING UP/DOWN SWITCHES

Controlling the resistor network of Figure 2 is done with the circuit of Figure 3. The four switches of Figure 2 are replaced with the four outputs of the MC14516 Up/Down binary counter and 1N914 diodes. Each of the resistors is "on" when the corresponding output is low, and disconnected (by means of the diode) when the output is high, providing 16 volume levels for the speakerphone. The circuit may be used in a line-powered speakerphone, or one which is powered from a power supply.

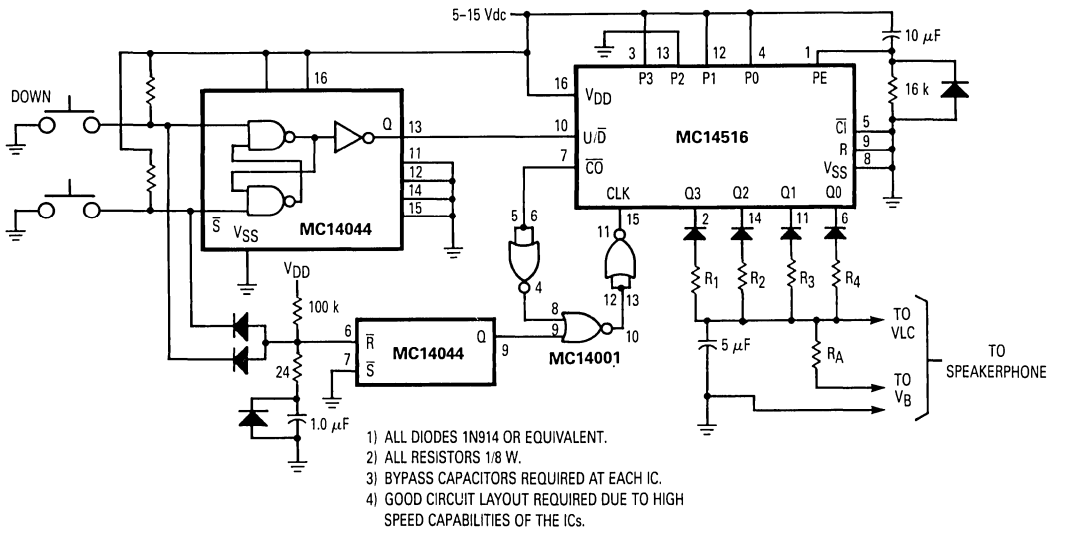

Figure 3. Up/Down Free Standing Digital Volume Control

The circuit works as follows:

- When one of the switches is closed, pin 13 of the MC14044 RS flip-flop is set either high (for UP) or low (for DOWN), and this sets the U/$\overline{D}$ input of the counter.
- Upon closing the switch, the 1.0 μF capacitor is discharged (the 24 Ω resistor limits the current during discharge), and pin 9 of the MC14044, and the counter's CLK input are taken low (assuming the $\overline{CO}$ output of the counter is high).
- Upon releasing the closed switch, the 1.0 μF capacitor will charge up slowly, and the CLK input of the counter will switch high approximately 80 milliseconds later, incrementing or decrementing the counter. The time delay provides for switch de-bounce.
- When maximum count is reached while up-counting, the $\overline{CO}$ output (Pin 7) switches low, preventing any more clock pulses from reaching the counter. The $\overline{CO}$ output returns to high when the U/$\overline{D}$ input changes state (by pressing the DOWN switch), allowing the counter to count down. A similar sequence occurs when minimum count is reached while down-counting.
- The Preset Enable (PE) input receives an active high pulse during power up, thus presetting the outputs to 1011 (in this example). In this way the speakerphone's volume is set to a known state each time the phone is taken off-hook. The preset level may be any of the 16 states by appropriately wiring P3–P0.

As the counter is sequenced up or down, the voltage at VLC will vary between a maximum of V_B and a minimum determined by the resistors (R_A, R_1–R_4). The 5.0 μF capacitor at VLC smooths the transition to the new level, preventing clicks or pops from being heard in the speaker. The power supply voltage can be obtained from the V_{CC} pin of the MC34118 (Pin 4), or from the V_{CC} output pin of the MC34018 (Pin 20). The circuit of Figure 3 requires less than 1.0 μA of supply current when idle, and typically less than 200 μA during a transition.

CALCULATING THE RESISTOR NETWORK

The resistor network values will be calculated for each of the three following situations:

1) The MC34018 speakerphone circuit, which has a fixed V_B of 2.9 Volts, and requires a minimum VLC of 0.55 V_B (1.59 Volts).
2) The MC34118 speakerphone circuit with a **fixed** supply voltage, resulting in a fixed V_B equal to $\approx$ (V_{CC} – 0.7)/2, and requiring a minimum VLC of 0.3 V_B.
3) The MC34118 speakerphone circuit with a **variable** supply voltage (such as in a line powered phone), resulting in a V_B voltage which can range from 1.3 to 2.8 V, and requiring a minimum VLC of 0.3 V_B.

The reason for the differentiation between #2 and #3 above is due to the voltage drop of the 1N914 diodes ($\approx$0.5 V), which is a significant part of V_B. The voltage drop of the counter's outputs, when a logic "0," is typically <10 mV, and is considered negligible. The resistor network for situations 1 and 2 is shown in Figure 4. Situation 3 will require a slightly different circuit.

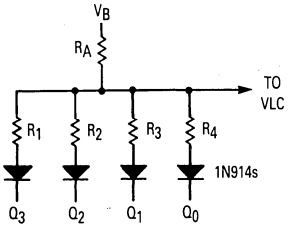

Figure 4. Network for Constant Voltage V_B Circuits

Situation 1

For the MC34018, R_A is selected to be 20 kΩ, as that is the same as the potentiometer's value shown in its data sheet. The voltage at VLC is equals:

$$VLC = \frac{(V_B - 0.5) \times R_B}{20\ k + R_B} + 0.5\ V$$

where R_B is the parallel combination of the "on" resistors. To achieve a minimum VLC of 0.55 V_B, R_B calculates to be 16.8 kΩ. The "R" value for Figure 2 is then 16.8 k/0.533, or 31.5 kΩ. The next lower standard resistor value of 30 kΩ is then chosen for "R," which is R_1 in Figures 3 and 4. Using standard values for the other resistors yields R_2 = 62 kΩ, R_3 = 120 kΩ, and R_4 = 240 kΩ. The resulting performance of this network is shown in the following tabulation:

Q_3–Q_0	"On" Resistors	VLC	VLC/V_B	Δ	dB Gain	Comments
0	R_1 R_2 R_3 R_4	1.57	0.542		−25.5	Min
1	R_1 R_2 R_3	1.61	0.556	0.014	−24.6	Volume
2	R_1 R_2 R_4	1.66	0.571	0.015	−23.5	
3	R_1 R_2	1.71	0.588	0.017	−22.4	
4	R_1 R_3 R_4	1.75	0.604	0.016	−21.3	
5	R_1 R_3	1.81	0.624	0.020	−19.9	
6	R_1 R_4	1.87	0.645	0.021	−18.5	
7	R_1	1.94	0.669	0.024	−16.8	
8	R_2 R_3 R_4	2.02	0.698	0.029	−14.8	
9	R_2 R_3	2.11	0.728	0.030	−12.7	
10	R_2 R_4	2.21	0.761	0.033	−10.5	
11	R_2	2.31	0.798	0.037	−7.9	
12	R_3 R_4	2.42	0.834	0.036	−5.4	
13	R_3	2.55	0.881	0.047	−2.2	
14	R_4	2.71	0.936	0.055	+1.6	Max
15	None	2.9	1.0	0.064	+6.0	Volume

The Δ column indicates the difference in the VLC/V_B ratio as the count is increased. The steps are larger at the high volume end compared to the low volume end. It is believed that this is not objectionable in most applications, and in fact, some users consider it desirable. The "dB Gain" column indicates the gain of the receive attenuator derived from Figure 5 of the data sheet.

Situation 2

For the MC34118 with a fixed supply voltage, the value of the resistors will depend on the specific voltage used for V_{CC}. Since the minimum VLC is 0.3 V_B, R_A was raised and the equivalent R_B lowered (from the values of situation 1) to achieve the lower ratio. The values for the five resistors can be found from the following chart:

V_{CC}	V_B	R_A	R_1	R_2	R_3	R_4	Min VLC/V_B
6.5	2.8	39K	15K	30K	62K	120K	0.298
6.0	2.54	43K	15K	30K	62K	120K	0.298
5.5	2.29	47K	15K	30K	62K	120K	0.303
5.0	2.04	56K	15K	30K	62K	120K	0.296
4.5	1.79	39K	7.5K	15K	30K	62K	0.296
4.0	1.54	51K	7.5K	15K	30K	62K	0.301

Testing of the circuit with V_{CC} = 5.0 V yielded the following results:

Q_3–Q_0	VLC	VLC/V_B	Δ	dB Gain
0	0.607	0.296		−33.0
1	0.628	0.306	0.010	−29.4
2	0.643	0.313	0.007	−26.1
3	0.669	0.322	0.009	−23.1
4	0.680	0.332	0.010	−20.1
5	0.712	0.347	0.015	−17.0
6	0.740	0.361	0.014	−14.0
7	0.783	0.375	0.014	−11.0
8	0.796	0.389	0.014	−8.5
9	0.856	0.417	0.028	−5.6
10	0.915	0.446	0.029	−2.9
11	1.01	0.489	0.043	−0.4
12	1.10	0.536	0.047	+1.6
13	1.28	0.624	0.088	+3.6
14	1.52	0.741	0.117	+5.0
15	2.05	1.00	0.259	+5.8

In this case, the fact that the step sizes are smaller at the minimum volume end is particularly advantageous since the MC34118 has a non-linear relationship between the VLC/V_B ratio and the amount of signal attenuation (see Figure 5).

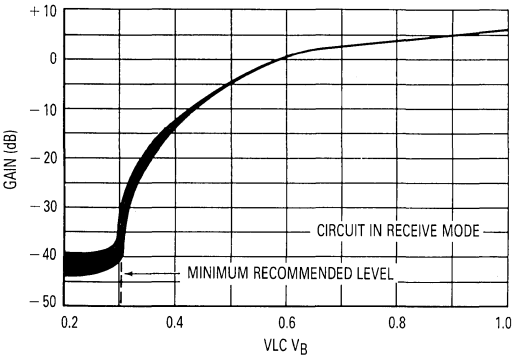

Figure 5. Receive Attenuator versus Volume Control — MC34118

As can be seen from the "dB" column (which is the MC34118's receive attenuator gain setting), the step size, in terms of the dB attenuation, is fairly constant throughout most of the range.

Situation 3

For the case where the MC34118 is used in a line powered speakerphone, V_{CC} can vary from 3.5 to 6.5 V, with a range for V_B of 1.3 to 2.8 V. If the circuit of Figure 4 is used, and set to provide a minimum VLC/V_B ratio of 0.3 when V_B = 2.8 V, the minimum ratio will be considerably higher (≈0.43) when V_B is reduced to 1.3 V. From the graph of Figure 5, it can be seen that the minimum gain will then be −10 dB rather than −33 dB. The problem stems from the ≈0.5 V drop of the diodes, which is a significant part of V_B. To reduce the effects of this voltage drop, the diodes are replaced with NPN transistors which have a saturation voltage of only ≈0.05 V (see Figure 6). The outputs of the MC14516 counter drive the 2N2222A transistors through the 100 kΩ base resistors. Because of the logic inversion of the transistors, the function of the UP and DOWN switches of Figure 3 is reversed. Additionally, because of the inversion, the preset inputs (P_3–P_0) must be changed to 0100 to achieve the same power-up setting as that of Figure 3.

With the circuit of Figure 6, the minimum VLC/V_B ratio ranges from a low of 0.298 (V_{CC} = 6.5 V) to a high 0.312 (V_{CC} = 3.5 V). The tested performance of this circuit, with V_{CC} = 5.0 V, is as follows:

Q_3–Q_0	VLC	VLC/V_B	Δ	dB Gain
0	0.615	0.300		−30
1	0.645	0.314	0.014	−26.5
2	0.674	0.329	0.015	−23.3
3	0.709	0.346	0.017	−20.4
4	0.755	0.368	0.022	−17.4
5	0.800	0.390	0.022	−15.1
6	0.847	0.413	0.023	−13.1
7	0.904	0.441	0.028	−11.1
8	0.970	0.473	0.032	−9.1
9	1.04	0.507	0.034	−7.2
10	1.13	0.551	0.044	−5.4
11	1.24	0.605	0.054	−3.5
12	1.39	0.678	0.073	−1.6
13	1.56	0.761	0.083	+0.7
14	1.77	0.863	0.102	+3.3
15	2.05	1.00	0.137	+5.9

IF YOU HAVE A MICROPROCESSOR . . .

If a microprocessor is included in the speakerphone design, the above circuit can be simplified by letting the processor do the switch de-bouncing, the up/down counting, and the off-hook preset. The critical part of Figure 3's circuit is the resistor network, and it can be controlled from a port through a CMOS latch (see Figure 7).

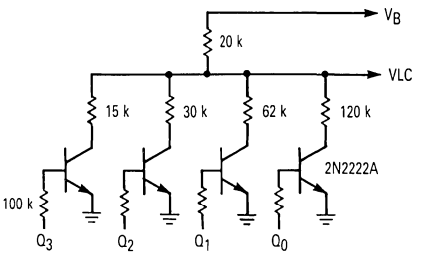

Figure 6. Network for MC34118 Variable Supply Situation

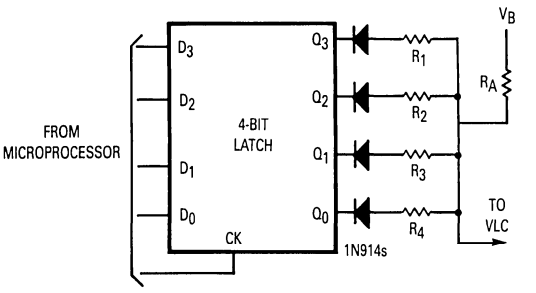

Figure 7. Microprocessor Interface

Recommended latches are the MC14042, MC14076, MC14174, and MC14175. The resistor values depends on which speakerphone circuit is used.

IN SUMMARY . . .

The circuit presented is fairly simple and straightforward without any critical components involved. The accuracy requirements of the resistor network depend on the accuracy requirements of the application. 5% resistors should suffice for most applications. The power supply current required for the additional circuitry is minimal (<1.0 μA) since all CMOS ICs are recommended. Additionally, the wide range of power supply voltages allowed by CMOS devices makes this circuit suitable for use with line-powered speakerphones.

REFERENCES

MC34018 Data Sheet, Motorola, 1985
MC34118 Data Sheet, Motorola, 1987
MC14516 Data Sheet, Motorola
MC14044 Data Sheet, Motorola
MC14001 Data Sheet, Motorola

Minimize the "pop" in the MC34119 Low Power Audio Amplifier

Prepared by
Dennis Morgan and Ron Friedman
Bipolar Analog IC Division

INTRODUCTION

In some instances, when the MC34119 speaker amplifier is re-enabled, a "pop" can be heard in the speaker. The cause can be due to the IC, or the PC board, or both. Whatever the cause, some users consider the "pop" objectionable. This application note describes how to minimize the "pop" to satisfy the most demanding user. The remedy, fortunately is very simple and inexpensive.

CIRCUIT DESCRIPTION

Referring to Figure 1, during normal operation (chip enabled), the input capacitor (C_i) has a DC voltage on it due to the DC bias of the MC34119 on its right side, and the DC bias of the audio source on its left side. The charging path for this DC bias is from Pin 5 through R_f and R_i, and the right side voltage is equal to that on Pin 4, which is the same voltage as that on Pins 2 and 3 ($\{V_{CC} - 0.7\}/2$).

When the IC is disabled (Pin 1 taken to a logic high), the internal bias is removed from the two op amps, and the two outputs go to a high impedance state. If the output pins are perfect in that no leakage exists at V_{O1} or V_{O2}, then the charge will remain unchanged on C_i. Upon re-enabling the IC, there will be no "pop" at the speaker as there will be no need to re-establish bias levels.

Leakage does exist, however, either internal and/or external to the IC. Internally, it can be due to normal reverse bias leakage currents, and can go either to Gnd or V_{CC}. Externally, leakage can be due to solder flux on the board, or other contaminants (fingerprints, air pollutants, etc.) which deposit on the board during the course of its use at the customer's location, and can go to Gnd or V_{CC}. Referring to Figure 2, and assuming a leakage to ground, C_i will now discharge through R_i, R_f, and R_{LK} (which is generally several megohms) with a time constant determined (essentially) by C_i and R_{LK} — the voltage at Pin 4 drops accordingly. (Current out of Pin 4 is insignificant for this discussion, and is ignored.) The bias voltage on Pins 2 and 3 is not removed during the disable period, and so the voltage at Pin 3 is unchanged.

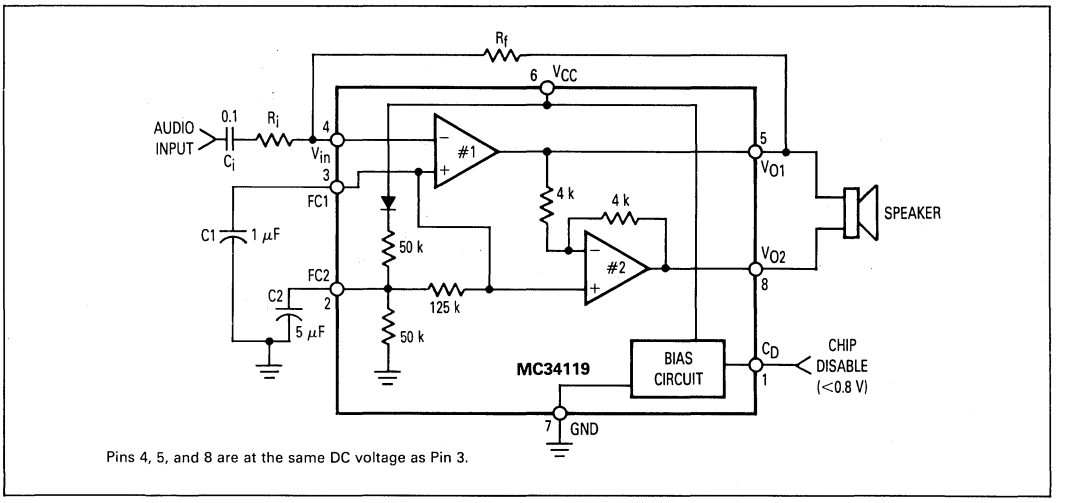

Figure 1. Normal Operation

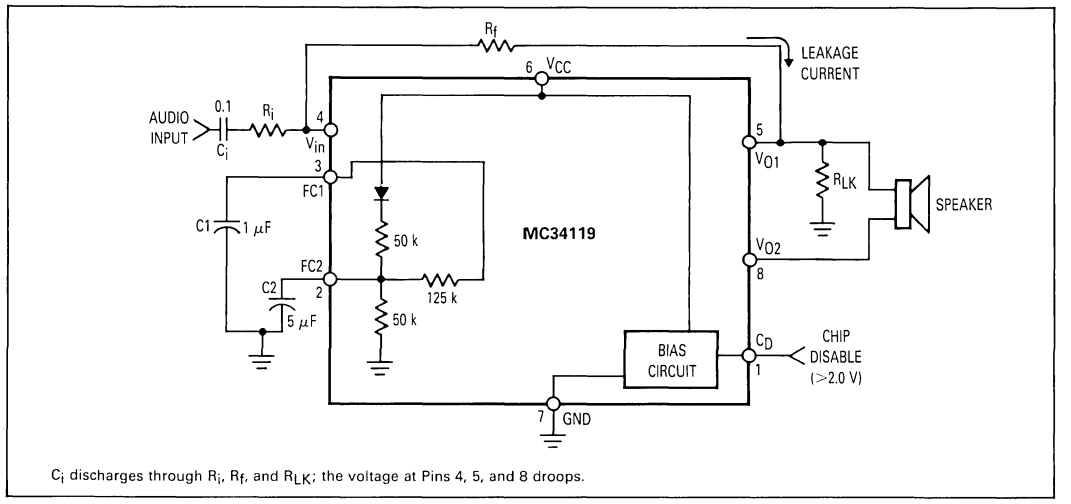

Figure 2. Disabled Mode

Upon re-enabling the MC34119, bias is returned to the op amps immediately, and op amp #1 finds the voltage at Pin 4 somewhat lower than that at Pin 3. Its output (Pin 5) is therefore driven near the upper rail (V_{CC}), and this causes op amp #2 output (Pin 8) to be driven near the lower rail (Gnd). The result is a large sudden voltage change across the speaker, hence the "pop." The outputs will then stay at these levels as C_i is recharged (by Pin 5 through R_f and R_i) until the voltage at Pin 4 is equal to that at Pin 3, bringing op amp #1 back into its linear operating region. Then the circuit is once again considered turned on. Figure 3 is a scope photo of the transient across the speaker ($V_{O1} - V_{O2}$) when the circuit is enabled. For this photo, V_{CC} = 6 volts, R_f = 270 k, R_i = 24 k, C_i = 0.1 μF, and R_{LK} = 5 MΩ.

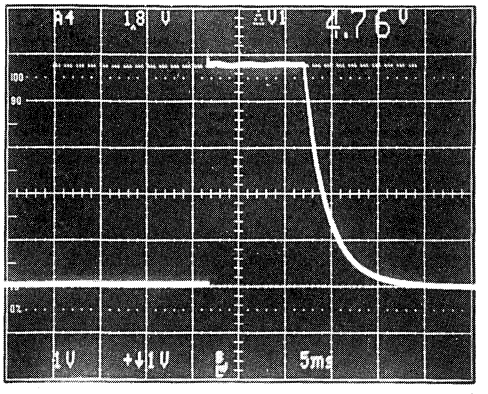

Figure 3. Output Transient Due To Leakage

THE SOLUTION ? — ONE RESISTOR

The solution involves keeping C_i from discharging in the first place. By placing a resistor from Pin 3 to 4, Pin 3 will supply the leakage current, relieving C_i of that duty (see Figure 4). Due to the voltage divider effect of R_X, R_f, and R_{LK}, C_i does discharge a small amount however, and upon re-enabling, requires a small amount of recharge. So the "pop" is not eliminated, but is considerably reduced. Figure 5 is a scope photo of the same circuit used for Figure 3, but with a 10 kΩ resistor added between Pins 3 and 4. The combination of reduced amplitude and pulse width means the transient energy has been reduced by a factor of almost 12, thereby considerably reducing the sound level of the "pop."

Experimentation has shown that values of 10 kΩ to 40 kΩ for R_X reduce the "pop" a very significant amount (Note: quantifying the amount of improvement is difficult, and could have been done by using an SPL meter. The real issue is what is an acceptable "pop," and what is objectionable — a purely subjective matter). Values greater than 40 kΩ have a progressively lower effect on the transient amplitude. Values less than 10 kΩ can actually increase the transient, and can also interfere with the normal operation of the amplifiers in the voiceband, most notably distortion.

CONCLUSION

Because of the possibility of contaminants on the PC board, the "pop" can occur even if a "perfect" IC is used. This solution will considerably reduce the problem, but will not completely eliminate it. This is due to the voltage divider effect of R_X, R_f, and R_{LK} which allows C_i to discharge slightly during the disable mode. Most applications should, however, find this solution a sufficient improvement to consider the problem resolved.

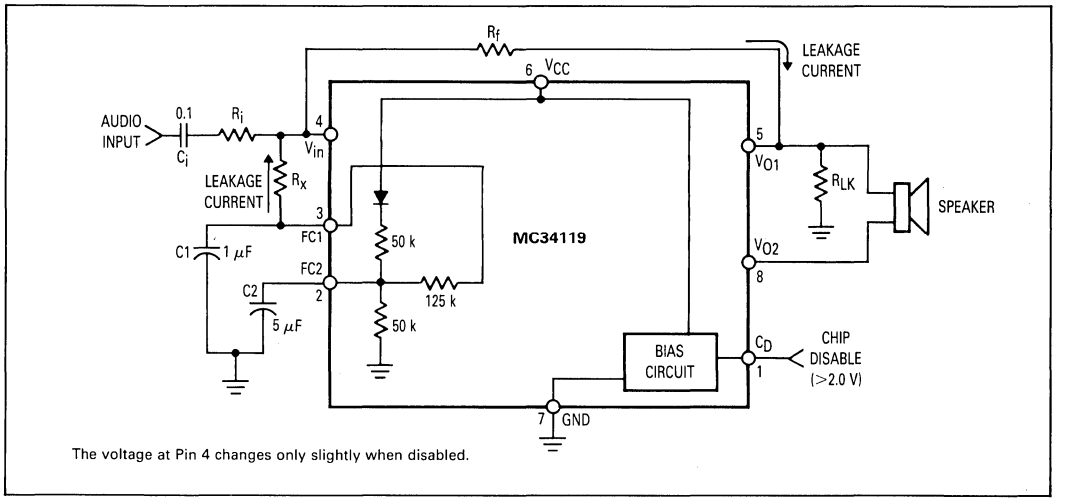

Figure 4. Disabled Mode With Resistor Solution

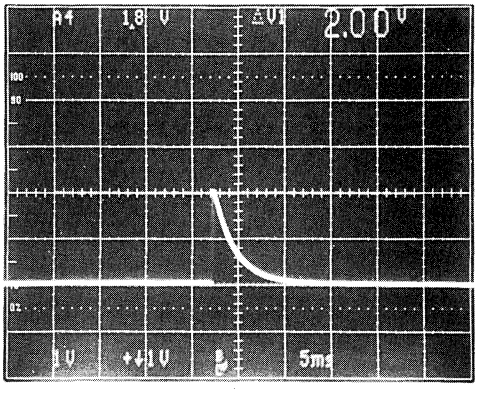

Figure 5. Output Transient With Resistor Fix

Limited Distance Modem
Using the Universal Digital Loop Transceiver Chip Family

OVERVIEW

The introduction of the Universal Digital Loop Transceiver (UDLT) family of integrated circuits aids the design of a high speed Limited Distance Modem (LDM). With an external clock, the LDM will transmit asynchronous data at rates up to 80 kbps. As shown here with an internal clock, the LDM can send as much as 38.4 kbps of asynchronous full duplex data up to two kilometers on 26 AWG twisted pair wire. The data transfer is controlled by the following RS-232C handshake signals: Request to Send (RTS), Clear to Send (CTS), Data Set Ready (DSR) and Carrier Detect (CD). If the data link is operating, CTS goes active in response to RTS going active. DSR is active if the LDM is powered up. If synchronization is lost, the CD signal goes inactive. Figure 1 shows a block diagram of the LDM. Figure 10 is a photostat of the LDM Demonstration Board - front, and Figure 11 is a photostat of the LDM Demonstration Board - back. Table 1 is a parts list for the slave and master LDM.

UNIVERSAL DIGITAL LOOP TRANSCEIVER

The heart of the LDM is the UDLT master/slave chip set. This chip set transmits data at a 256 kbps burst rate using a "ping pong" approach. As shown in Figure 2, a Modified Differential Phase Shift Keyed (MDPSK) data burst is transmitted from the master to the slave. Then after a slight delay, a burst is transmitted from the slave to the master. Since an eight kHz clock is typically applied to the Master Sync Input (MSI) pin, and ten bits are sent to the master and the slave every MSI period (every 125 μs), the transceiver is effectively transmitting 80 kbps of full duplex synchronous data.

The burst's ten bits of digital data are input on three different pins of the UDLT master. The first eight bits are serially received from the Receive Data Input (Rx) pin. The ninth bit is from the Signaling Bit Input (SI1) and the tenth bit is from the SI2 pin. These ten bits are formatted together and shipped out from the chip on the LO1 and the LO2 pins (Line Driver Outputs). After being transmitted across the line and received on the LI pin of the slave UDLT, eight bits of data are serially output through the slave's Transmit Data Output (Tx) pin, one bit on the SO1 and one bit on the SO2 (Signaling Bit Output). Then the slave UDLT sends a similar burst to the master UDLT.

DLT VS. UDLT

Since the MC145418/19 Digital Loop Transceiver (DLT) chip set is very similar to the UDLT, it is not difficult to adapt

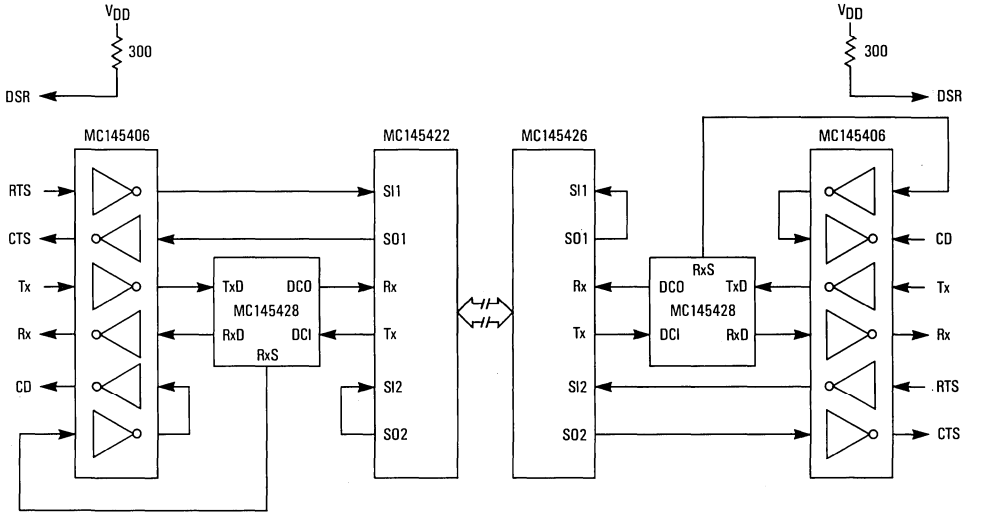

Figure 1. Limited Distance Modem Block Diagram

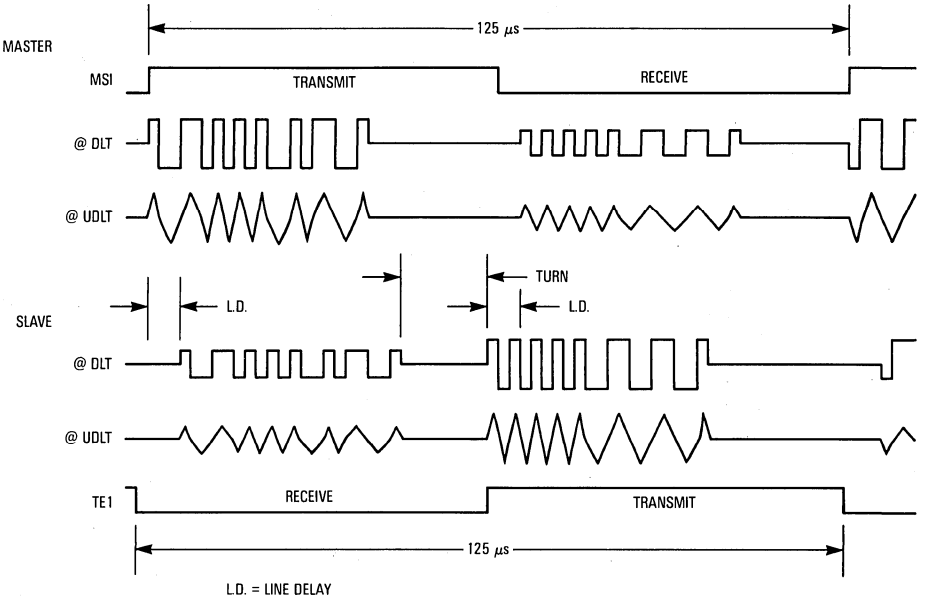

Figure 2. 80 kbps MDPSK Timing Diagram

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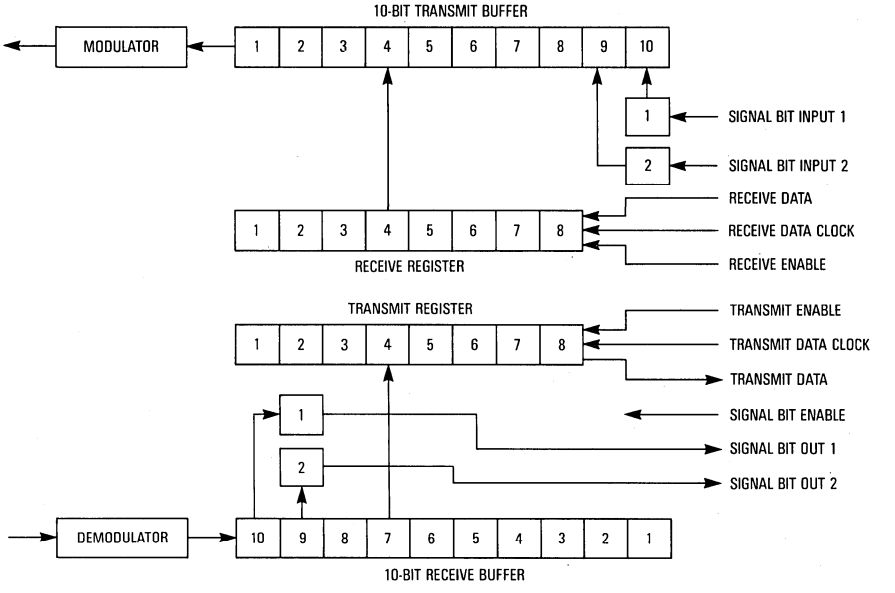

Figure 3. UDLT Receive and Transmit Registers

AA8929-1

this LDM to use the DLT. There are three main differences between the UDLT and the DLT chips. The most important difference between the chips is that the UDLT automatically adjusts the thresholds on the receive circuitry. This allows the UDLT to optimize its reception to a particular line's attenuation level. The DLTs threshold is externally set , so typically this receive optimization will not be achieved, unless some rather complex circuitry is implemented. Also, the DLT requires external drivers and transmits square waves instead of triangular waves. In conclusion, the UDLT has on board driver and threshold adjust circuitry, but the DLTs basic approach allows driver and threshold design flexibility.

SIGNALING PINS FOR RTS/CTS HANDSHAKE

This LDM uses the SI1, SI2, SO1 and SO2 pins of the master and slave for a RTS/CTS handshake. To perform this task, the signaling channels are used for transmitting the RTS/CTS handshake. The input at SI1 of the master UDLT is the RTS signal. This information is transmitted to the SO1 of the slave UDLT chip. At this point, the signal is looped around into SI1 of the slave UDLT, and it is transmitted to SO1 of the master UDLT. This signal at SO1 is the master's CTS signal. A similar configuration is used for the slave's RTS/CTS handshake on the SI2/SO2 channel. This allows the RTS/CTS handshake to verify that the communication link is operating.

DATA SET INTERFACE

Since most data from a terminal is an asynchronous format, the Data Set Interface (DSI) is needed to convert data from an asynchronous to a synchronous format and vice versa. At TxD of the DSI, the asynchronous signal should begin with a start bit (logic 0). After following with an eight or nine bit data word, the format ends with one or more stop bits (logic 1). The rate that the data is loaded into the DSI is determined by the internal bit rate generator, whose rate, if 38.4 kbps or less, is selected by BR1, BR2 and BR3 (Baud Rate Select Pins). An external bit rate generator can be used for data rates higher than 38.4 kbps.

Once in the DSI, the data is stripped of its start and stop bits and loaded in a register. Next, the data is checked for a break condition, and one of three types of words is sent, under the timing control of the DC, CM and DOE pins. If a break condition is recognized, the break flag (11111110) is transmitted. If data is in the register, it is dispatched. Finally, if no data is in the register, a synchronizing flag (01111110) is sent. However, regardless of data being in the transmit register, a synchronizing flag is also transmitted on a regular basis to verify that synchronization is intact. Furthermore, the transmit circuitry inserts a binary 0 after five continuous 1's of data, so neither pattern, (11111110) or (01111110), can be sent as data.

At DCI, DC, CM and DIE control the synchronous data's receive loading into the DSI. Once loaded, the DSI's receiver determines if the data is break or synchronizing information. If it is a break or synchronizing flag, the appropriate action is taken. If it is not, the data is loaded into a receive register. From this register, data words are taken, start and stop bits are added and the asynchronous word is output on RxD (Receive Data) at the baud rate selected by BR1, BR2 and BR3. Figure 4 is a block diagram of the DSI.

MC145428
DATA SET INTERFACE

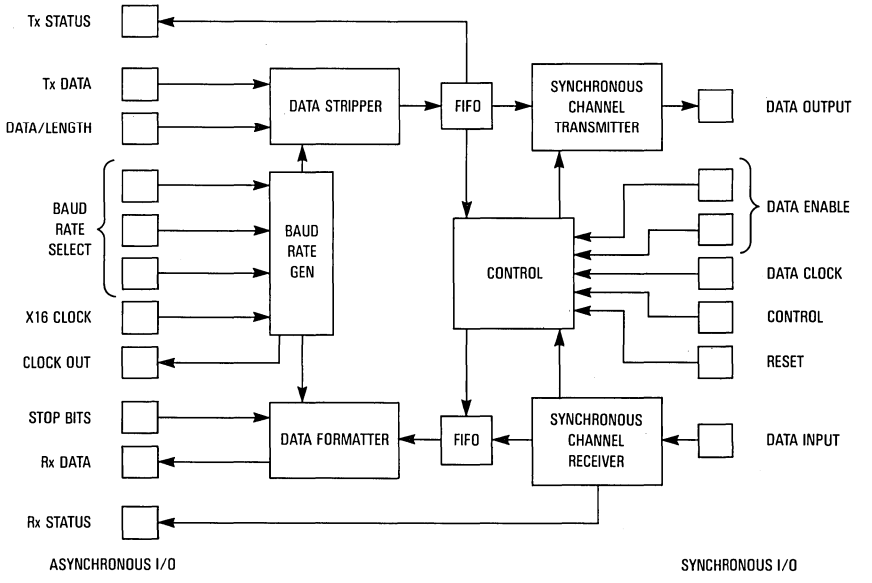

Figure 4. DSI Block Diagram

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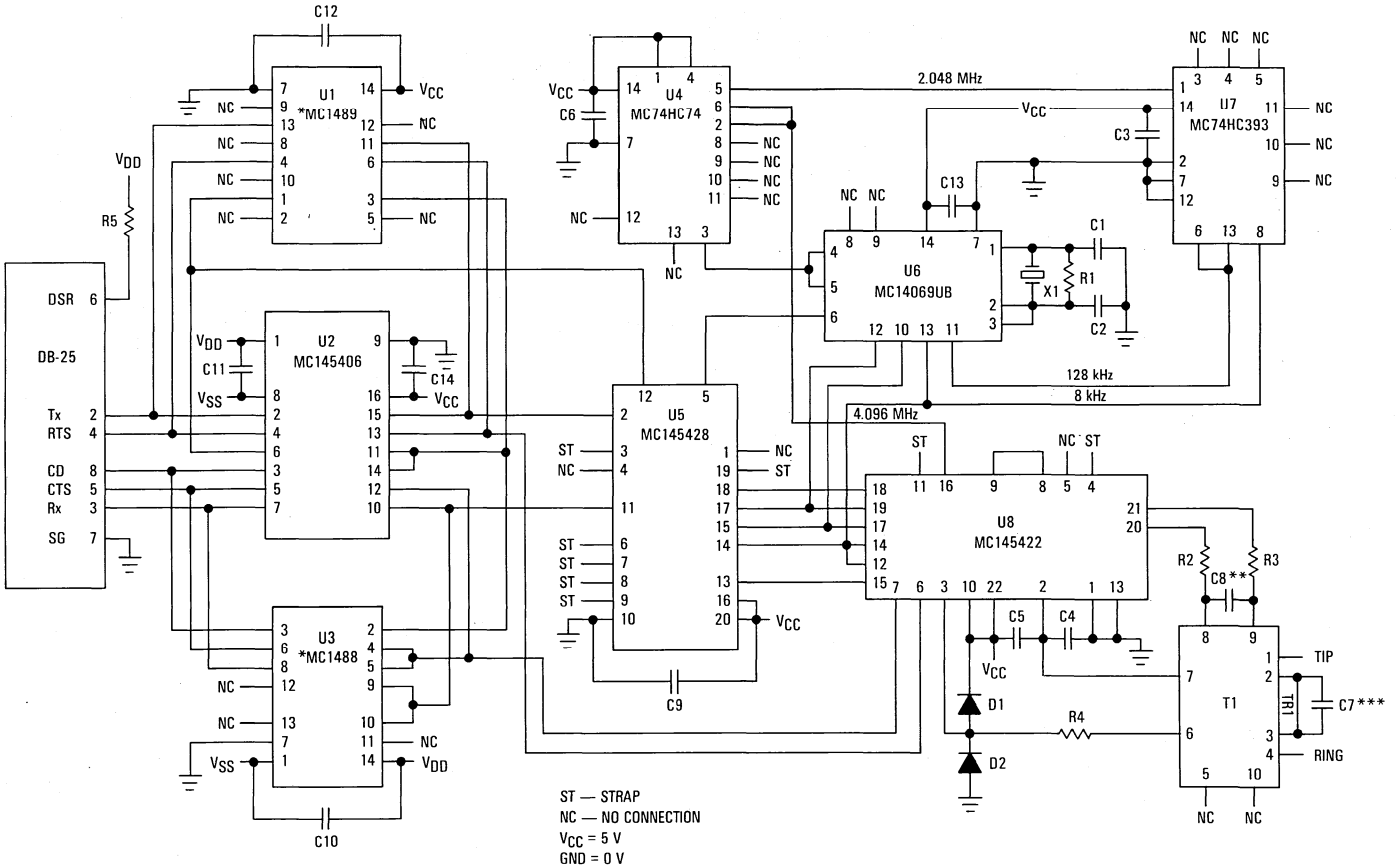
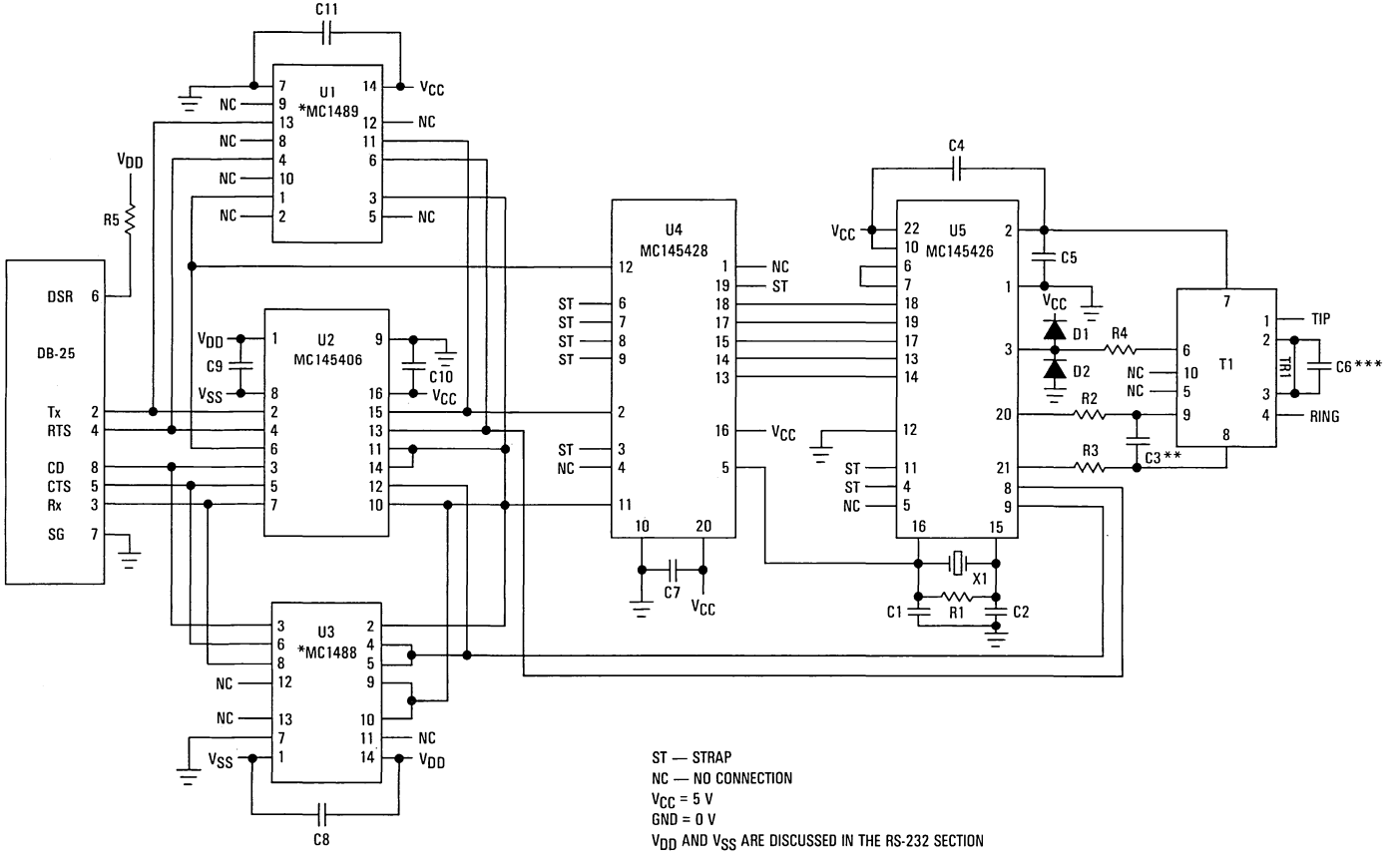


ST — STRAP
NC — NO CONNECTION
V_{CC} = 5 V
GND = 0 V
V_{DD} AND V_{SS} ARE DISCUSSED IN THE RS-232 SECTION

*MC1489 and MC1488 used when MC145406 not used
**C8 is optional filtering.
***TR1 should be cut when C7 is used

Figure 5. Master Limited Distance Modem



*MC1489 and MC1488 used when MC145406 not used

**C3 is optional filtering.

***TR1 should be cut when C6 is used

Figure 6. Slave Limited Distance Modem

RS-232C DRIVER/RECEIVER

The last integrated circuit discussed is the RS-232C interface. Either the MC145406 or the MC1488/MC1489 Driver/Receiver, which both fulfill the electrical specifications of EIA Standard RS-232C and CCITT Recommendation V. 28, can be used. The receivers invert the signal and convert the RS-232 signals to standard five volt logic levels, and the drivers invert the signal and convert five volt logic levels to RS-232 voltage levels.

The MC145406 is a CMOS RS-232 chip with three drivers and three receivers. This chip operates with a five volt supply and ±5 to ±12 volt supplies. Although the MC145406 chip will work with ±5 volt supplies in most systems, the voltage supplies should be at least ±7 volts to meet the RS-232 driver specification. For full RS-232 compliance, the driver's output must be between 5 volts and 15 volts for a logical 0, and it must be between –5 volts to –15 volts for a logical 1.

The MC1488 is a quad line driver. For the MC1488 to comply with the RS-232 driver requirements, a minimum power supply of ±8 volts must be used. However, the chip will operate effectively in most systems with the positive supply voltage varying from +7 to +15 volts. The MC1489 is a five volt quad line receiver.

RS-232C CONTROL AND SIGNALS

As seen in Figure 5, the master LDM schematic, and Figure 6, the slave LDM schematic, asynchronous control and data signals enter the LDM at RS-232 voltage levels through a DB-25 connector. Figure 7 shows a DB-25 connector which is the standard computer terminal connector. Pins 2,3,4,5,6,7,8 transmit the following information:

Pin 2: Transmit Data (Tx)
Pin 3: Receive Data (Rx)
Pin 4: Request to Send (RTS)
Pin 5: Clear to Send (CTS)
Pin 6: Data Set Ready (DSR)
Pin 7: Signal Ground (GND)
Pin 8: Carrier Detect (CD)

The Tx and RTS signals are fed into the receivers, and the Rx, CTS and CD signals are outputs of the driver. For the CD signal, one of the receivers inverts the signal from the RxS pin of the DSI. When the DSI is in asynchronous status, this inversion gives the CD a logic 0. The output of that receiver is then put into a driver to obtain RS-232 voltage levels. The DSR pin is connected to the RS-232 positive power supply through a 300 ohm resistor. Therefore, DSR will go active whenever the power supply is on. The GND pin is connected to the system's ground. The remaining pins used of the DB-25 connector are routed to the RS-232 Driver/Receiver.

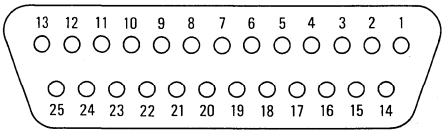


Figure 7. DB-25 Connector

TRANSFORMER INTERFACE

The transformer interface greatly affects the UDLTs capabilities. It performs the functions of impedance matching, bandwidth limiting, increasing receive voltages to required threshold levels and input protection. At 256 kHz, 26 AWG wire's characteristic impedance is 110 ohms. The source resistors from the LO1 and LO2 pins are chosen to be 220 ohms. With a transformer turns ratio of 2:1, the line side's characteristic impedance is 110 ohms. This configuration impedance matches the twisted pair.

The UDLTs minimum output voltage from the LO1 and the LO2 pins is 2.25 volts peak. Half of the voltage is lost across the 220 ohm source resistor. That voltage of 1.12 volt peak is halved again by the 2:1 turns ratio of the transformer to 0.56 volts peak. At 256 kHz, 26 AWG wire attenuates a signal level of 18 decibels-per-kilometer. After traveling a distance of two kilometers the signal will have attenuated 36 decibels. At the line side of the transformer, the minimum signal level is 8.9 millivolts peak. A turns ratio of 1:4 in the transformer windings brings the signal level up to 35.6 millivolt peak. This voltage is divided between a resistor from the transformer to the LI pin and an internal resistance. At worst case, 29 millivolt peak are at the LI pin — within the 25 millivolts peak minimum allowed signal.

The UDLTs maximum voltage output is 3.0 volts peak. Because of the voltage being halved by the source resistors and the transformer windings, the transmit signal level at the line side is 0.75 volt peak. With a short loop, the signal level drop is negligible, so the signal level at the receiving transformer is about 0.75 volts peak. With the 1:4 turns ratio at the receiving transformer, the signal level at LI will be 3.0 volts peak, which exceeds the 2.5 volt peak maximum input at LI. A signal level greater than 2.5 volts peak will inject current into the UDLTs substrate. This action will distort the modulator's output, thus creating bit errors. Consequently, protection diodes and resistors are needed to clamp the input at LI. The demonstration board's transformer configuration is shown in Figure 8. The LI pin's protection includes a 1 kilohm resistor between the LI pin and the diodes. This resistor is not on the

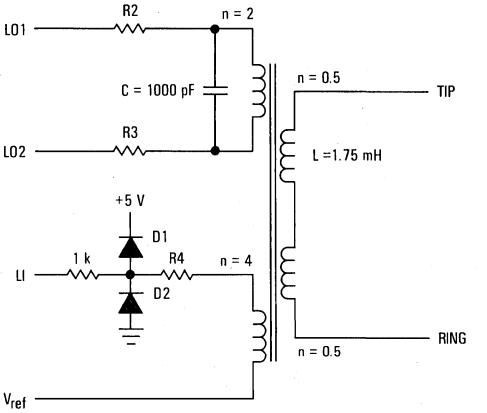


Figure 8. Transformer Configuration Used in LDM Schematic

demonstration board. Typically, the external diodes will turn on before the chip's internal diodes, so the external diodes will shunt most of the current. However, the 1 kilohm resistor will further ensure that the external diodes turn on first.

The maximum power bandwidth of the UDLT is 8 to 512 kHz, but to improve line settling, it is desirable to use a 20 to 512 kHz bandwidth. To make the lower corner of the bandwidth 20 kHz, the inductance of the transformer windings is chosen to be 1.75 millihenries. To make the upper corner of the bandwidth 512 kHz, a 0.001 microfarad capacitor is placed in parallel with the transmit tap. If battery feed is used, further input protection is advised. Figure 9 shows a more durable transformer configuration. Transformers fulfilling these specification can be obtained from:

Leonard Electric Products Company
85 Industrial Drive
Brownsville, Texas 78521

Part Number: P/N P-1358-A

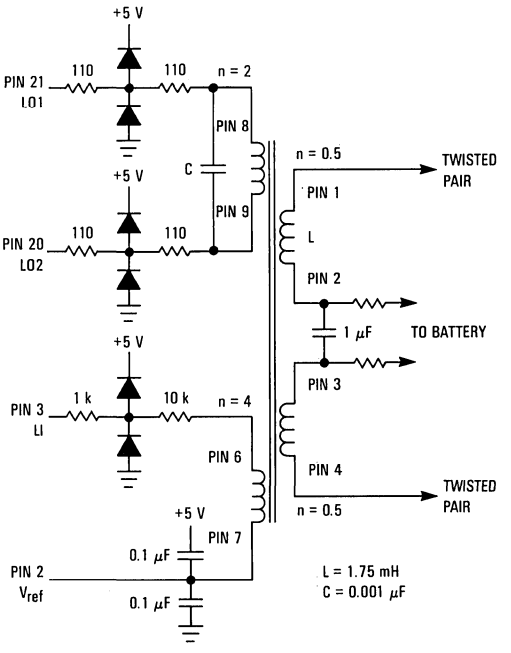


Figure 9. Battery Feed Transformer Configuration

LDM BOARD OPTIONS

A picture of the LDM demonstration board is shown in Figure 10 and 11. Many of the UDLT and DSI features are made available on the demonstration board using straps. These UDLT features include:

$\overline{LB}$: In the master, a low disconnects the LI pin from the internal circuitry, drives LO1, LO2 to V_{ref} and internally ties the modulator to the demodulator. In the slave, a low on the $\overline{LB}$ pin makes the incoming demodulated data going to Tx replace the incoming data on Rx.

$\overline{PD}$: A low powers down the UDLT, except for the receive circuitry.

The DSI features that can be controlled using the straps include:

SB: A low selects outputting one stop bit per data word, and a high selects outputting two stop bits.

DL: A low selects operating with eight bit data words, and a high selects operating with nine bit data words.

Reset: A low clears the internal FIFO, disables TxD, and forces TxS and RxS low.

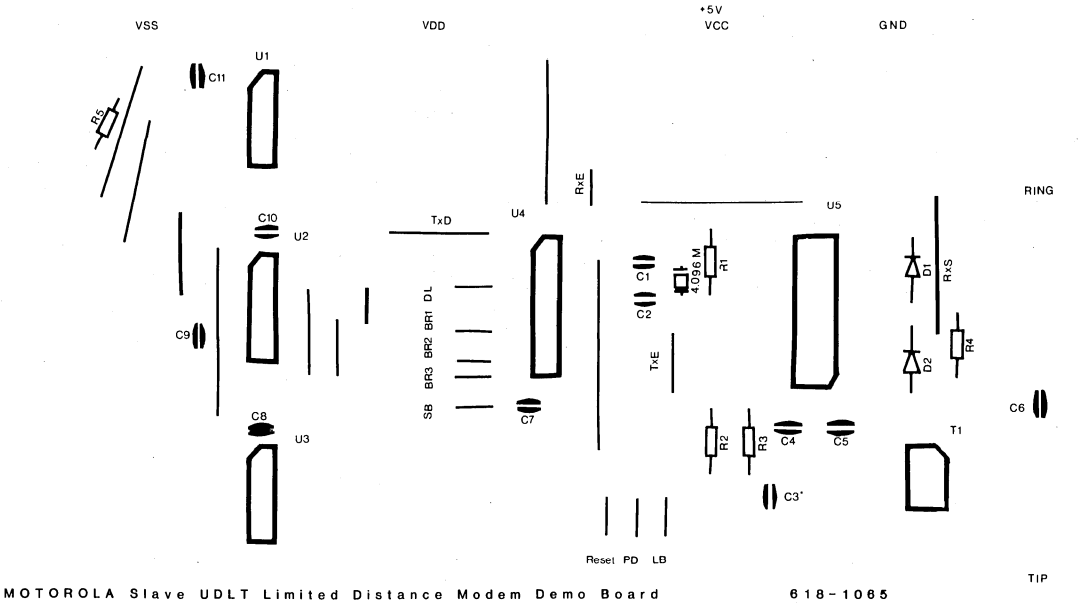
BR1, BR2, BR3: These pins select the asynchronous data rate.

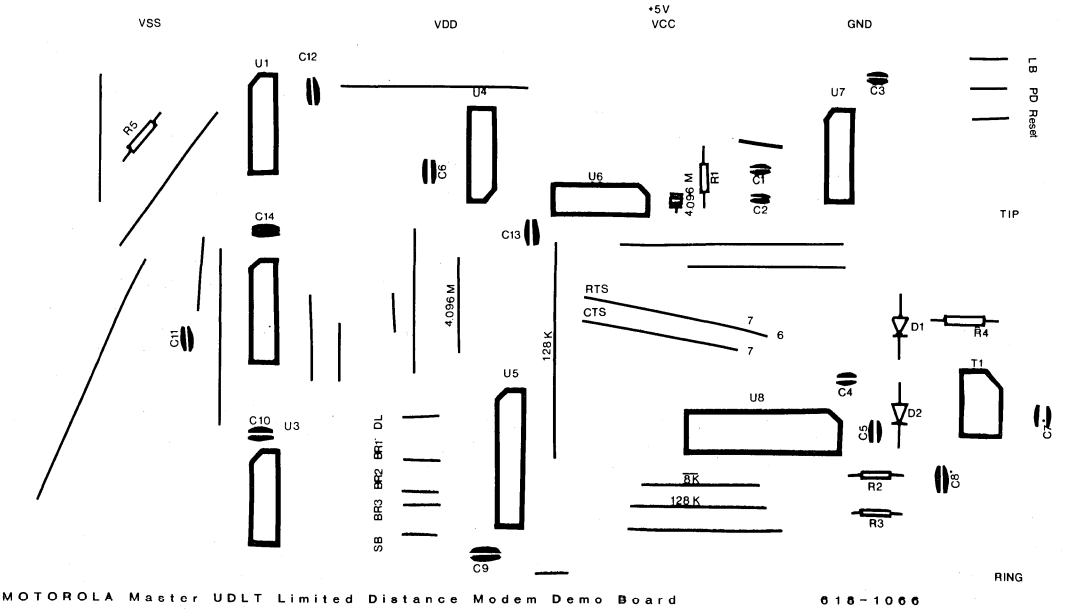
For more information, refer to the individual data sheets. The top of the LDM board shows suggested straps for these functions. These straps select one stop bit, an eight data word, an inactive Reset, a 9600 baud asynchronous data rate, an inactive loop-back and an inactive power-down.

For battery feed applications, C6 of the slave LDM and C7 of the master LDM can be inserted, and the trace between these pins should be broken. This capacitor allows ac signals to pass through the transformer, but keeps dc power across the capacitor to be fed into the system's power supply. C3 of the slave LDM and C8 of master LDM provide filtering for the upper corner of the bandwidth. If this filtering is not desired, these capacitors may be omitted, but their insertion is recommended.

CONNECTORS

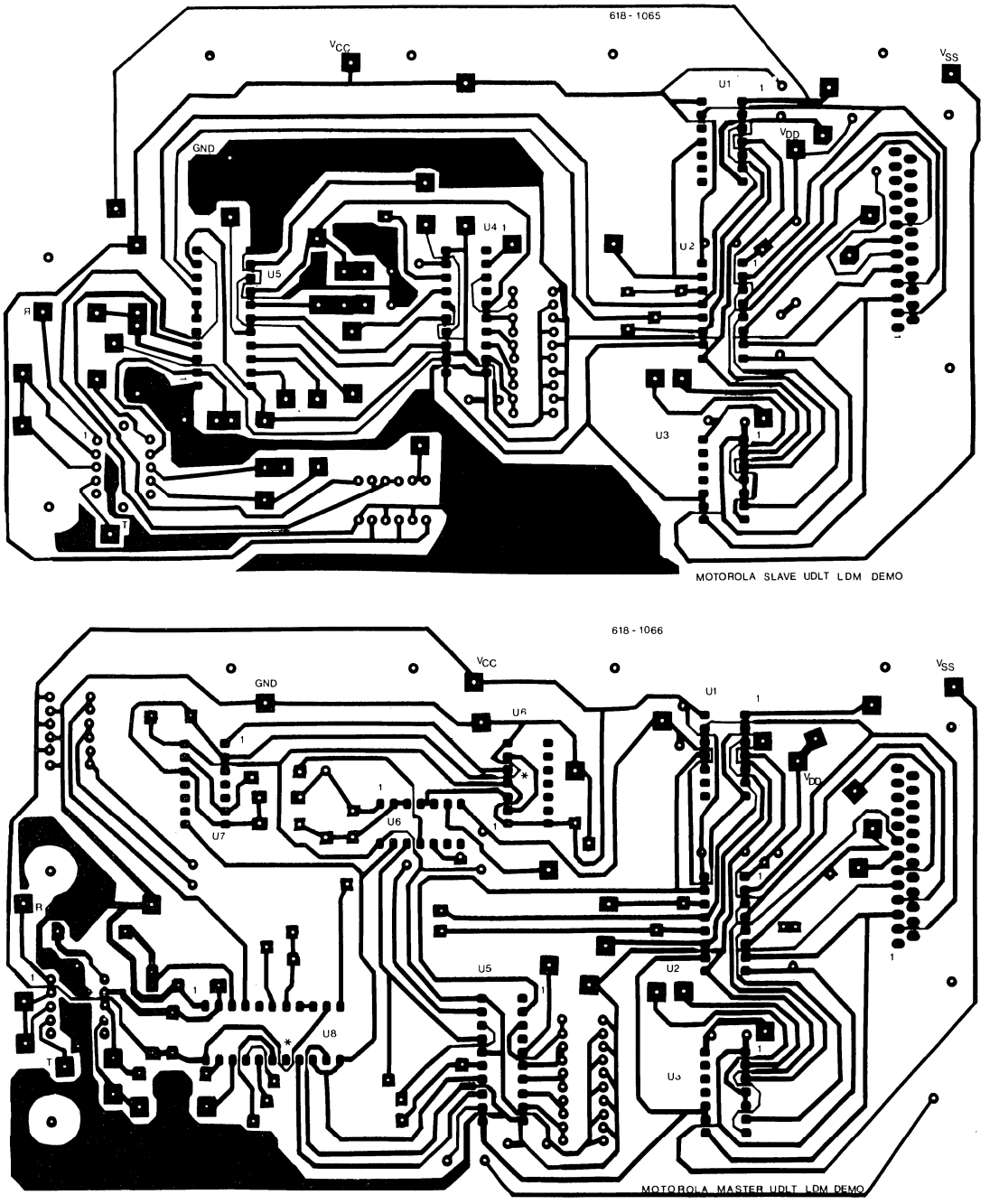
On the demonstration board, V_{SS} and V_{DD} are only used to power the RS-232 circuitry. V_{SS} is the most negative power supply, and V_{DD} is the most positive power supply. The RS-232C Driver/Receiver section explains the appropriate voltage ranges for using either the MC145406 or the MC1488/MC1489. V_{CC} is the board's five volt supply, and GND is the board's digital ground. Tip and Ring are the connections for the twisted pair wire. The 25 pins on the left side of both the slave and the master board is for the DB-25 connector.





NOTE: Drawings are not actual size.

Figure 10. Photostat of LDM Demonstration Board - Front



*External to the demonstration board-back, pin 6 of the MC74HC74 should be connected to pin 16 of the MC145422

NOTE: Drawings are not actual size.

Figure 11. Photostat of LDM Demonstration Board - Back

Table 1. Limited Distance Modem Parts List

Master LDM		Slave LDM	
R1: 10 MΩ	R4: 10 kΩ	R1: 10 MΩ	R4: 10 kΩ
R2: 220 Ω	R5: 300 Ω	R2: 220 Ω	R5: 300 Ω
R3: 220 Ω		R3: 220 Ω	
C1: 20 pF	C8: 1000 pF	C1: 20 pF	C7: 0.1 μF
C2: 20 pF	C9: 0.1 μF	C2: 20 pF	C8: 0.1 μF
C3: 0.1 μF	C10: 0.1 μF	C3: 0.001 μF	C9: 0.1 μF
C4: 0.1 μF	C11: 0.1 μF	C4: 0.1 μF	C10: 0.1 μF
C5: 0.1 μF	C12: 0.1 μF	C5: 0.1 μF	C11: 0.1 μF
C6: 0.1 μF	C13: 0.1 μF	C6: 1.0 μF	
C7: 1.0 μF	C14: 0.1 μF		
D1: 1N914	D2: 1N914	D1: 1N914	D2: 1N914
X1: 4.096 MHz		X1: 4.096 MHz	
U1: MC1489		U1: MC1489	
U2: MC145406		U2: MC145406	
U3: MC1488		U3: MC1488	
U4: MC74HC74		U4: MC145428	
U5: MC145428		U5: MC145426	
U6: MC14069UB			
U7: MC74HC393			
U8: MC145422			
T1: Lepco P/N P-1358-A		T1: Lepco P/N P-1358-A	

Data Multiplexing
Using the Universal Digital Loop Transceiver and the Data Set Interface

INTRODUCTION

Data multiplexers find applications where clusters of terminals are connected to a central computer and in systems where modems are pooled at a common location. Combining the signals from the various terminals onto one multiplexed data link simplifies wiring and reduces expenses. Sharing the cost of the multiplexer among the several terminals results in a lower net cost compared to installing and maintaining individual cables for each terminal. While present day multiplexers are economical, new ICs from Motorola make possible enhanced performance multiplexers for a fraction of the cost of existing devices.

This Application Note will describe the design of a short-haul multiplexer for asynchronous data at rates up to 9600 baud. The mux combines eight full-duplex data channels along with eight end-to-end RS-232 control signals onto a single pair of telephone wire for distances up to 2 km. Motorola's Universal Digital Loop Transceivers (MC145422/26 UDLTs) master/slave high-speed synchronous data transceivers and Data Set Interface (MC145428 DSI) full-duplex asynchronous to synchronous converter form the heart of this multiplexer. A few MSI CMOS ICs complete the design.

Figure 1 illustrates a typical system with the terminals in a departmental situation multiplexed onto one high-speed data link. RS-232 control signals are passed transparently through the multiplexer so the terminals have direct access to the controls of the modems. This multiplexer system transports one control signal bidirectionally for each data channel. As will be described below, other configurations may easily be constructed with simple wiring changes.

CHARACTERISTICS OF THE UDLTs

The UDLTs are synchronous data transceivers capable of transporting 80 kbps of full-duplex data over ordinary twisted pair 26 to 19 gauge telephone wire at distances of up to 2 km. These devices utilize a 256 kilobaud MDPSK ping-pong burst modulation technique for transmission. Three logical data channels, one of 64 kbps and two of 8 kbps each are exchanged in bursts of 10 bits every 125 μs frame. MDPSK timing is shown in Figure 2. The master initiates a ping-pong frame by bursting 10 bits of data to the slave beginning on the rising edge of an externally generated Master Sync Input (MSI). The modulator's analog output signal (LO1, LO2) is shown referenced to MSI. Upon receiving the last bit from the master, the slave responds with a 10 bit burst of its own after a four baud delay. The slave's modulator output (LO1, LO2) is shown referenced to its own Transmit Enable 1 (TE1). Depending on the transmission line characteristics and length, the actual time of arrival of the slave's return burst at the master will vary due to the propagation time of the signal

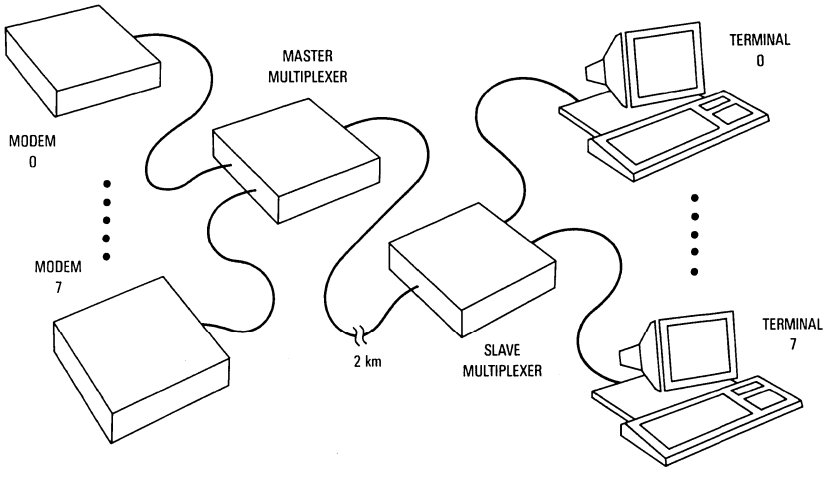


Figure 1. Typical Multiplexer Application

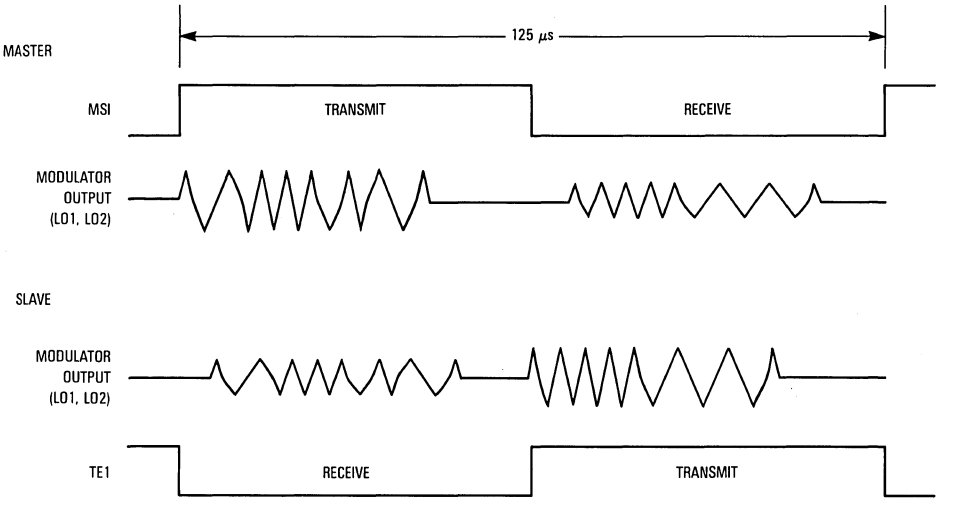


Figure 2. UDLT Timing

between UDLTs. On excessively long lines, propagation time down the transmission line results in collisions between the master and slave bursts so maximum line length is limited to 2 km with 26 gauge wire. The slave's TE1 is generated internally upon completion of demodulation of the burst from the master. TE1 remains high for eight data clock (128 kHz) periods and returns low until another burst is received. This process is repeated every 125 μs. Since both master and slave devices exchange data every frame in a half-duplex manner at a 256 kilobaud rate, an effective full-duplex rate of 80 kilobaud is accessible to the user.

The bursts of data on the transmission line use Modified DPSK signals to reduce EMI and susceptibility to crosstalk from other signals in telephone cables. The frequency spectrum consists of peaks at 128 kHz and 256 kHz and their odd harmonics. Only a small amount of energy is present in the frequency bands used by analog telephone service, so UDLT signals may be placed on adjacent pairs in cables with ordinary telephone signals with no degradation of performance. The power spectral density at 76 kHz is approximately 18 dBm and at 28 kHz the level is less than −30 dBm. Because there is no signal energy at very low frequencies, dc energy may be transported on the transmission line to power the remote multiplexer unit. Details of this feature will be described later.

The UDLTs have internal buffers to store and prepare synchronous data for transmission. Eight bits for the 64 kbps channel are serially input and output every 125 μs frame. The two 8 kbps channels each have one bit input and output every frame. The master and slave UDLTs synchronous timing is shown in Figures 3 and 4 respectively. Both figures illustrate the transmit and receive timing for the eight bit words on Tx and Rx, and the timing for the two signalling bits, both inputs (SI1, SI2) and outputs (SO1, SO2).

The master UDLT timing shown in Figure 3 requires external timing signals of 8 kHz for MSI, TE1, RE1, and 64 kHz up to 2.56 MHz may be used for the TDC/RDC pin. This application uses 128 kHz. Eight bits of the 64 kbps data channel received from the slave are output on the Tx pin on the first eight rising edges of TDC/RDC while TE1 is high. Data to be sent to the slave is input on the Rx pin on the first eight falling edges of TDC/RDC while RE1 is high. In this application TE1 and RE1 are connected together so data is input and output simultaneously. Data on the 8 kHz signalling channels are input on SI1 and SI2 pins and output on SO1 and SO2 pins on MSI's rising edge.

The slave UDLT timing (shown in Figure 4) is similar to the master except that the slave synchronizes to the master's bursts and generates its own clocks and enables. The eight bits of the 64 kbps data channel received from the master are presented on the Tx pin on the rising edges of CLK while TE1 is high. Data to be transmitted to the master is loaded in on the Rx pin on the falling edges of CLK while RE1 is high. Signalling bits on the 8 kbps channels to and from the master are input at SI1, SI2 and output at SO1, SO2 on TE1's rising edge.

The master UDLT has pin controlled Power-Down ($\overline{PD}$) and Loop-Back ($\overline{LB}$) features which can be used for system testing. Also available on the master is Signal Insert Enable (SIE) which enables the insertion and extraction of an 8 kbps channel into the LSB of the 64 kbps channel. In this application SIE is unused and held low. The signal enable pin (SE) is a three-state control pin which when held high enables $\overline{PD}$, $\overline{LB}$, and the two signalling bits (SO1 and SO2) allowing these signals to be bussed to a microprocessor.

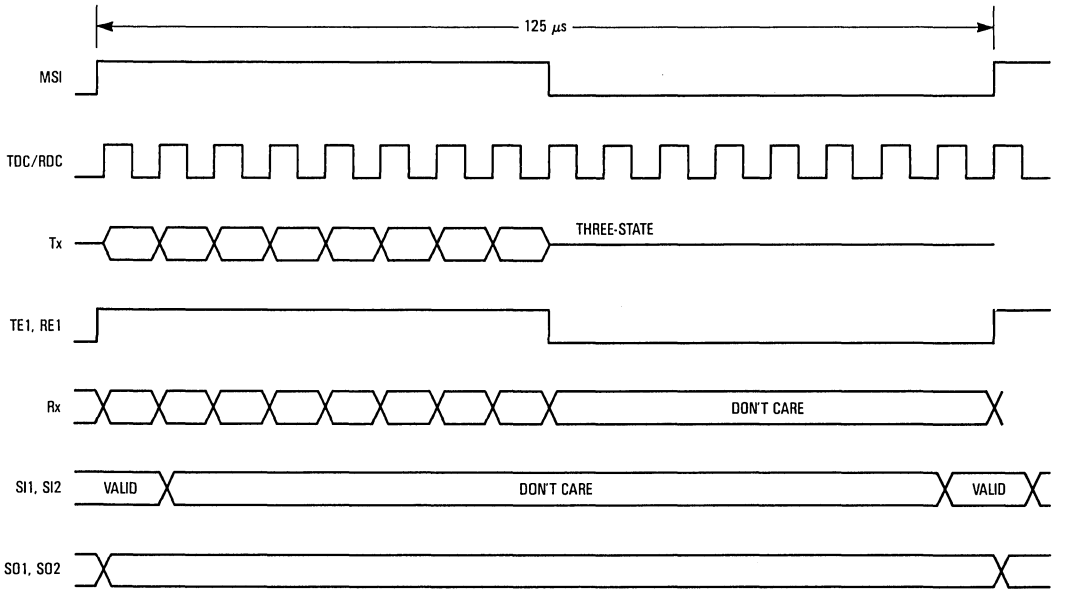


Figure 3. Master Timing

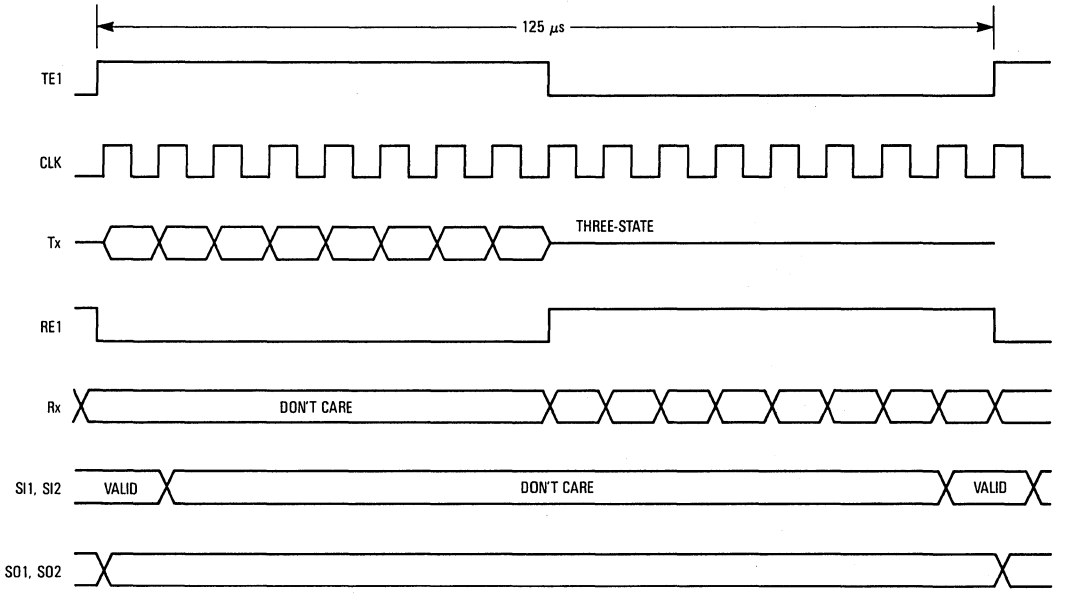


Figure 4. Slave Timing

Figure 5. Master Unit Interconnect

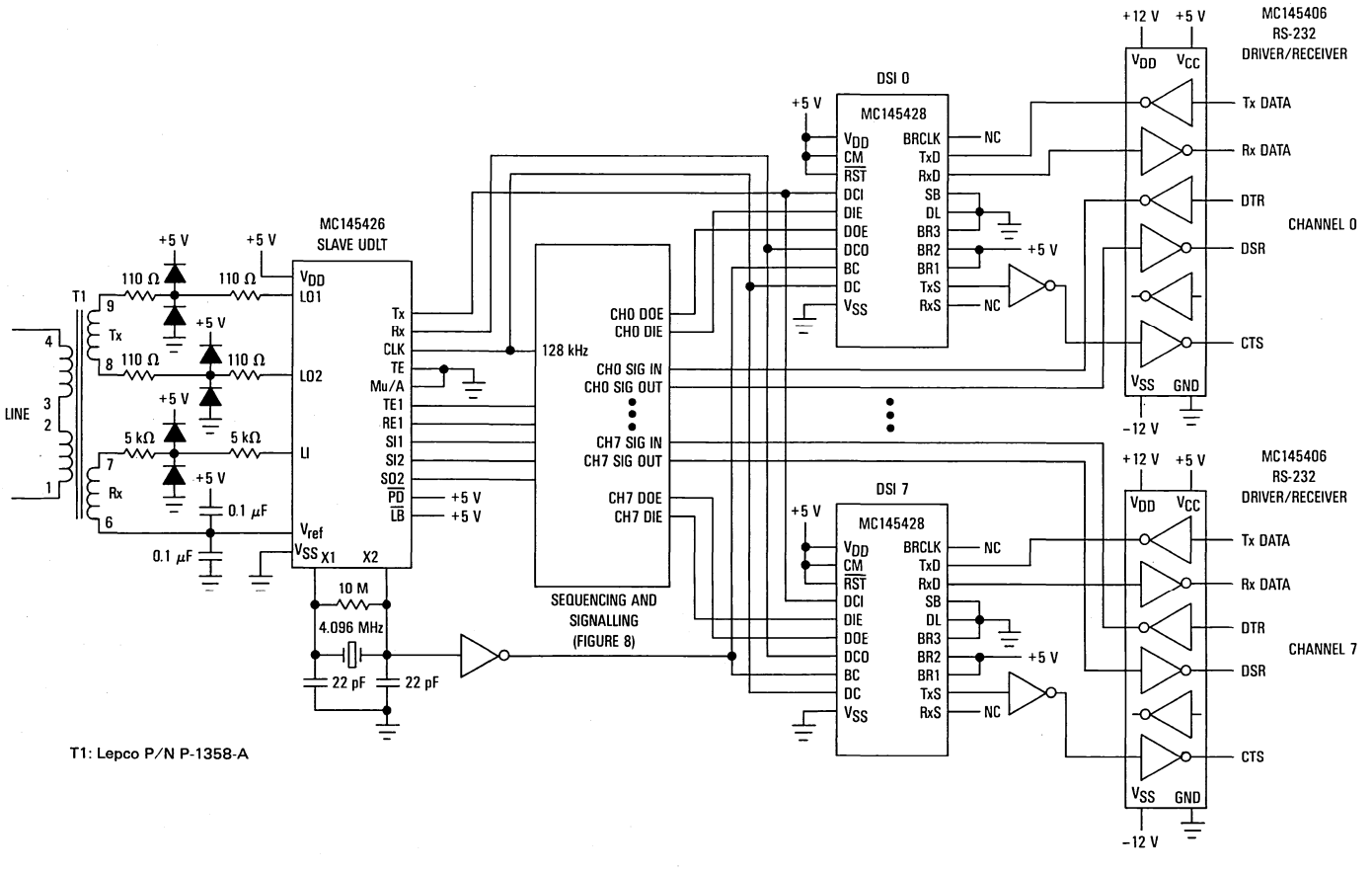


Figure 6. Slave Unit Interconnect

TRANSFORMER INTERFACE

The duplexer function, separating transmit and receive bursts on a single twisted pair wire is automatic with UDLTs. The receiver input is blanked while the transmitter is active so the transmitted signal is ignored by the demodulator circuits. The receiver unblanks when the transmitter finishes its burst to search for the return burst from the other end. Automatic duplexer action allows a simple transformer to be used for the interface between the transmission media and UDLTs shown in Figures 5 and 6. The transformer Tx winding and the associated padding network match the transmitter output to the impedance of the transmission line. The Rx winding steps up the signal from the far end to compensate for the loss in the matching network. The characteristic impedance of twisted pair telephone wire in the frequency range used by the UDLTs is approximately 110 ohms. Matching this impedance requires resistors of 220 ohms in each leg of the Tx winding. The impedance of 440 ohms when transformed through a 2:1 turns ratio results in a match to 110 ohms. 12 dB of loss is also introduced. The 12 dB is made up in the Rx winding which has a 4:1 step-up from line to receiver input.

Protection of the UDLTs against transients induced onto the transmission line is accomplished by adding clamp diodes to the padding networks. It is convenient to split the 220 ohm resistors into two 110 ohm resistors and place the clamps at the junction of the resistors. The same technique is used at the receiver inputs.

CHARACTERISTICS OF THE DSI

The DSI is a device which provides full-duplex asynchronous to synchronous conversion. It allows the user to select asynchronous data formats and baud rates. The synchronous port has selectable timing for easy interfacing to a variety of systems. The asynchronous port characteristics are controlled by the Stop Bit select (SB), Data Length select (DL), Baud Rate select (BR1-BR3) pins. Synchronous data is under the control of the Data Output Enable (DOE), Data Input Enable (DIE), Data Clock (DC), and Clock Mode (CM) pins. Asynchronous data is sampled at 16 times the selected baud rate. Logic circuits search the asynchronous data for a start bit, eight or nine data bits and one or two stop bits. When valid start and stop bits are found, they are removed from the character and the remaining eight or nine data bits are loaded into the transmit FIFO for transmission on the synchronous port. The Tx Status pin goes low when the transmit FIFO is more than half full. This signal may be used for a local Clear-To-Send indication to the data device on the asynchronous port. Special characters are generated and transmitted on the synchronous port to synchronize the receiver of the remote DSI to the character boundaries. At the remote DSI synchronous data is reassembled into eight or nine bit characters, start and stop bits are added and the data is transmitted out on the asynchronous port.

Since start and stop bits are removed from the asynchronous data before transmission on the synchronous port, some data compression is achieved. For example, asynchronous data at 9600 baud with eight data bits and one stop bit is compressed to 7680 baud on the synchronous channel. This makes possible the use of an 8 kbps synchronous channel to transport 9600 baud data. However, since sync and break characters consisting of data patterns 01111110 and 11111110 respectively are exchanged between DSIs every so often, the effective data compression is somewhat reduced. Zero bit insertion on the synchronous data between DSIs is used to eliminate the possibility of data imitating either of these characters (the inserted zeros are removed by the synchronous receiver). The multiplexer allocates the UDLTs 64 kbps synchronous channel to each DSI for one 125 μs ping-pong frame out of every 1 ms data frame. This results in an 8 kbps synchronous channel for each DSI. Under certain circumstances, with binary data, zero insertion may cause the transmit FIFO to overrun. If hex 'FF' characters are input to the DSI on the asynchronous port at 9600 baud with minimum time between characters, inserted zeros and sync characters cause the effective data rate to increase from 7680 baud to approximately 9400 baud. Since the synchronous channel supports only 8 kilobaud, an overrun of the Tx FIFO will occur. The TxS pin will go low approximately 5 ms before an overrun occurs and this indication may be used to stop the flow of new asynchronous data until the FIFO clears out. When ASCII data is used, only 6 characters (>(3E hex), ?(3F hex), I(7C hex), ~(7E hex), DEL(7F hex), and Blank(7D hex)) generate stuffed zeros. Fortunately, it is unlikely that these characters will be sent in large enough groups to cause FIFO overruns. In applications where ASCII data is transported, eight 9600 baud channels may be multiplexed onto this system's 64 kbps synchronous channel. If binary data is transported, a 16 kbps synchronous channel must be allocated for each DSI, resulting in a four channel multiplexer. This guarantees that even with maximum zero insertions, FIFO overruns will not occur.

OCTAL MULTIPLEXER SYSTEM DESCRIPTION

This multiplexer system fully exploits the DSI chips and the UDLT transceiver pair. The UDLTs 64 kbps channel transports the synchronous data from the DSIs. One of the UDLTs 8 kbps channels is used to synchronize the multiplexing of the eight data channels, and the other 8 kbps channel is used to transport eight RS-232 control signals.

The multiplexer system consists of two units, a master and a slave. Figure 5 illustrates the interconnection of the various devices within the master unit. The transformer interface to the twisted pair is shown with the previously described impedance matching and protection circuitry. The master UDLT is shown with the Tx, Rx lines along with the 128 kHz and the 4.096 MHz clocks bussed to the eight DSIs. The data channel enables and signalling lines are shown connecting the DSIs and the RS-232 driver/receivers to the sequencing and signalling block. Each DSI is shown configured for 9600 baud with eight bit character lengths and one stop bit which may be made switch selectable, if desired.

Figure 6 shows the complementing slave unit. Protection circuitry and the transformer interface are the same as the master unit. The slave UDLT generates its own clocks derived from an on-chip crystal oscillator circuit. An inverter is used to drive the eight clock inputs to the DSIs. Also shown is the sequencing and signalling interconnect to the DSIs and the RS-232 driver/receivers.

Circuitry in the sequencing and signalling blocks is shown in Figures 7 and 8 for the master and slave units respectively. All pertinent timing of the multiplexer system is shown in Figure 9. Master timing is shown in the top section, master and slave bursts on the twisted pair are shown on the line

labeled 'Transmission Line'. Slave timing is illustrated on the bottom half of the figure.

Clocks for the master UDLT are created by a 12-stage ripple counter (MC74HC4040) which is driven by a 4.096 MHz crystal oscillator. Taps at Q1, Q5, and Q9 create the 2.048 MHz (CCI), 128 kHz (TDC/RDC) and 8 kHz (MSI,TE1,RE1) clocks respectively. Inverters are needed on each line so the rising edges coincide. A pulse which synchronizes the master and slave data channel sequencing circuitry is generated when a count of 0 is reached by Q10, Q11, and Q12 of the ripple counter. This pulse is shifted through the enable shift register (MC14015B) to create eight non-overlapping enables for the DSIs. A latch (MC14013B) is used to delay the pulse so that it can be properly input into SI1 of the UDLT on the next rising edge of MSI. The delayed pulse on SI1 and the data channel enables (CH0-CH7 DOE, DIE) are shown on the timing diagram. RS-232 control data is routed to a latch by an addressable data selector (MC14051B). RS-232 control data received from the slave unit is written into an addressable latch (MC14051B). Notice that the first Q0 of the shift register is the enable to the DSI of data channel 1. Since the sync pulse arrives at the input of the shift register slightly after the clock, a one-channel offset is used to address the proper channel. This offset is transparent to the system.

Data input on the Rx pin of the UDLT is buffered until the next rising edge of MSI, when it is burst out on the transmission line. Data on SI1 and SI2 are latched in on the rising edge of MSI and transmitted in the burst which was initiated by that MSI edge. The bursts from the master (boxes with M) and the return bursts from the slave (boxes with S) on the twisted pair wire are illustrated on the 'Transmission Line'. The numbers indicate which channel's data is transported in that burst.

The system sync pulse arrives at the slave unit on the SO1 pin of the UDLT (Figure 8). It is shifted through a shift register (MC14015B) which is clocked by the RE1 pin. The Q's from this shift register enable the transmission of data from the DSIs to the UDLT. The sync pulse is delayed and shifted through another shift register clocked by TE1. The Q's from this shift register enable the DSIs to accept data from the UDLT. RS-232 control data is handled in the slave unit in a similar manner as the master with a data selector and an addressable latch. Simply offsetting the connections to the RS-232 driver/receivers realigns the data to the proper

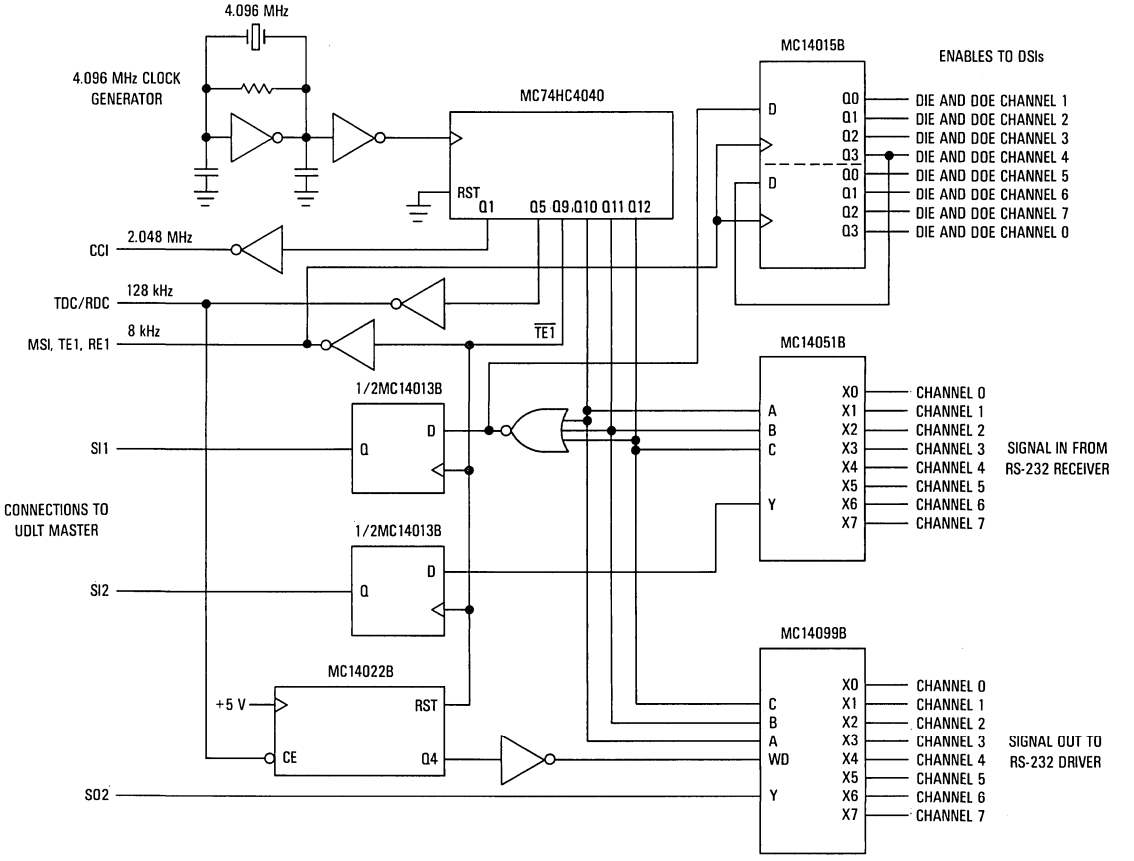


Figure 7. Master Sequencing and Signalling

channels eliminating any superfluous circuitry. Offsetting the connections to the data selector (MC14051B) similarly aligns the channels so that the data arrives at the master in the correct time slot. Following the channels on the timing diagram illustrates the concept.

ADDITIONAL CONSIDERATIONS

This multiplexer design is quite modular. If RS-232 control signalling is not desired then the circuitry can be simplified by removing the write pulse generator (MC14022B), addressable latches (MC14099B) and data selectors (MC14051B) from both units. The address generator (MC14163B) on the slave unit may also be removed. In applications where data rates of less than 9600 baud are used, the Baud Rate select pins on the DSIs need simply be reconfigured. A DIP switch can be conveniently used to set the Baud Rate, Data Length and Stop Bit pins on the DSIs. Note that the DSIs must not be set for 19.2 or 38.4 kilobaud when eight channels are multiplexed. If data rates higher than 9600 baud are desired, the individual data channels must be serviced more often by the UDLT. Because the high-speed synchronous channel between UDLTs is 64 kbps, the total bandwidth required by all of the channels must be at or below 64 kbps. The multiplexer may also be converted into a single channel limited-distance modem where data rates of up to 56 kbps can be attained.

This multiplexer, because it is all CMOS, consumes only about 175 mW per unit. One of the units may be powered by dc energy transported on the transmission line itself eliminating a power cord. The line interface transformer is designed to pass dc energy by separating the two line windings and installing a 1 μF capacitor between pins 2 and 3. Now, dc current may be passed to the twisted pair. A switching power supply may be installed in the remote unit to convert the line power to voltage levels useable by the digital circuitry. Recall that the dc resistance of 2 km of 26 AWG wire is approximately 575 ohms. This necessitates a relatively high voltage on the sending side to keep the I^2R losses in the twisted pair to a tolerable level. Usually 36 to 40 volts is satisfactory to furnish enough voltage to the remote unit. Since the transmission line is balanced, there is no ground reference between master and slave units. dc power to the twisted pair must be fed from an isolated winding on the mains transformer, so that a ground reference may be established at the remote unit. Connecting the ground references of the two units through the twisted pair will result in poor data performance due to longitudinal currents in the line.

References

Motorola Telecommunications Device Data Book DL136, 1984.

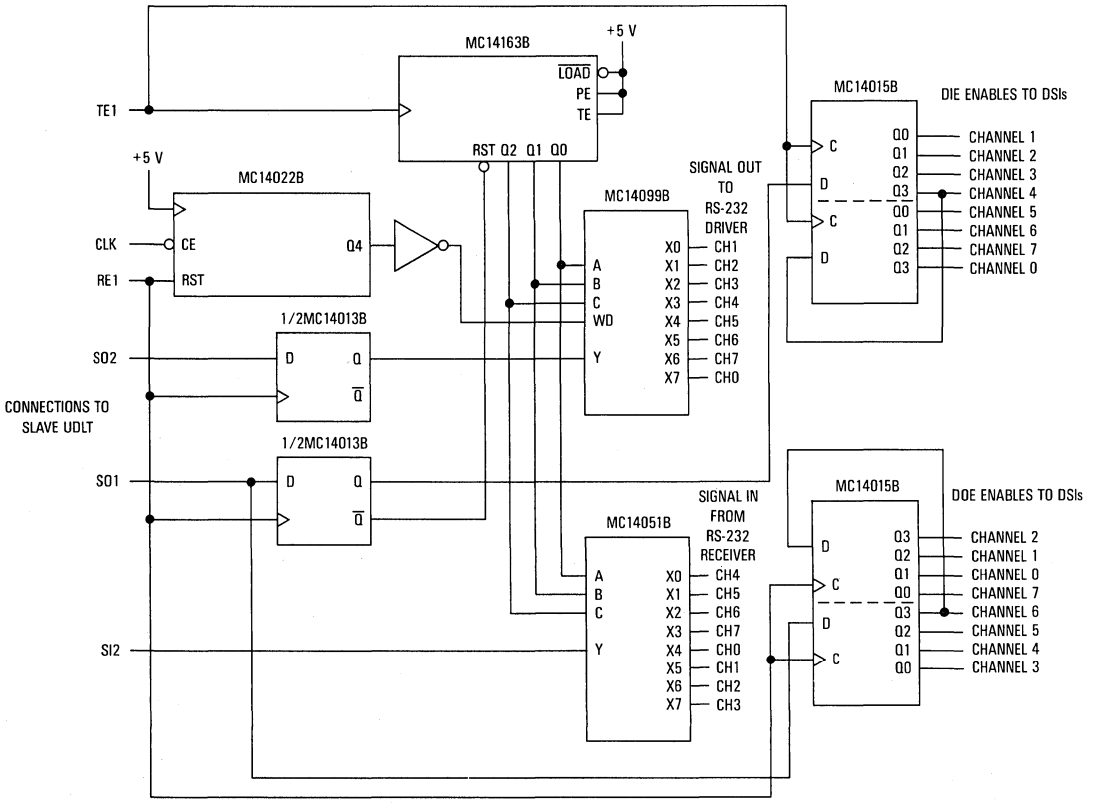


Figure 8. Slave Sequencing and Signalling

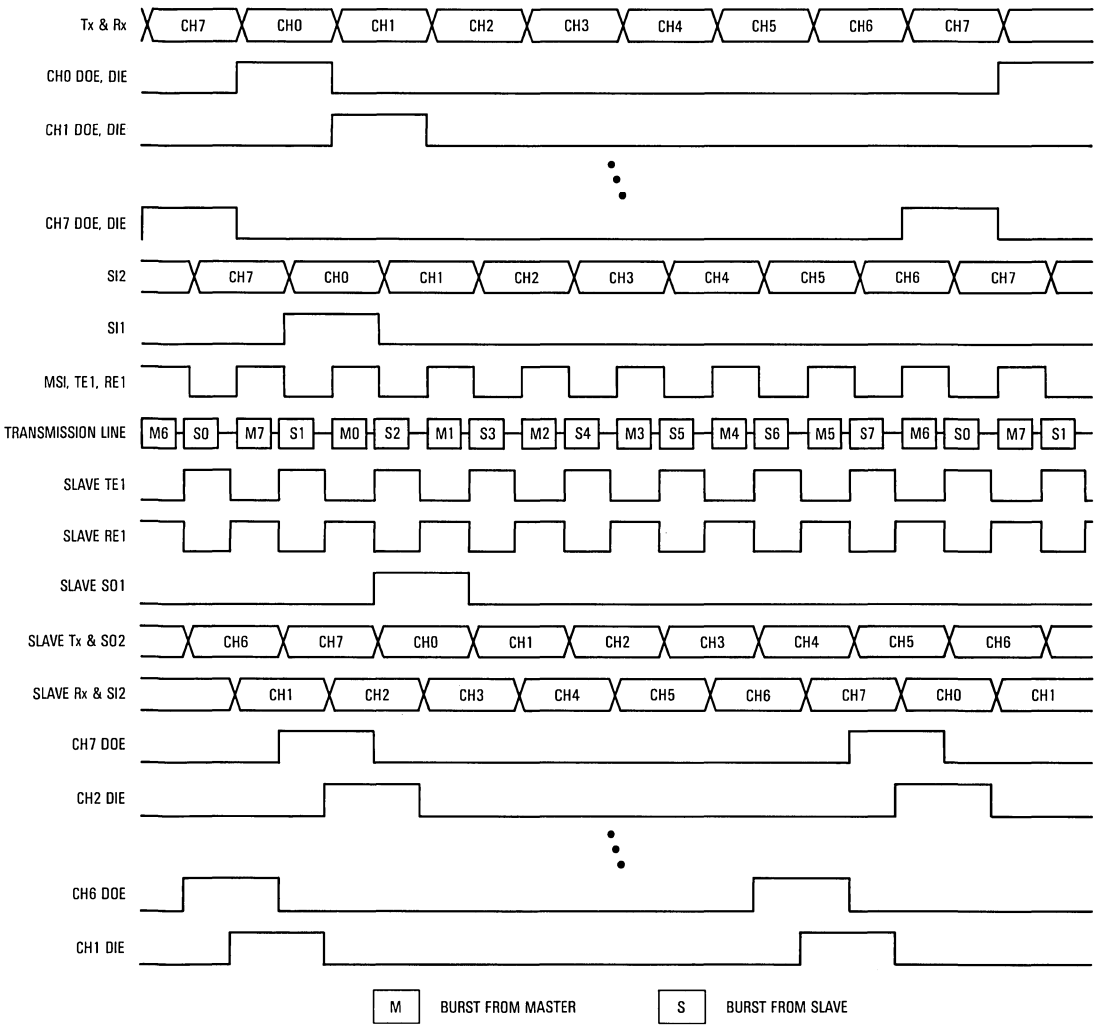


Figure 9. System Timing

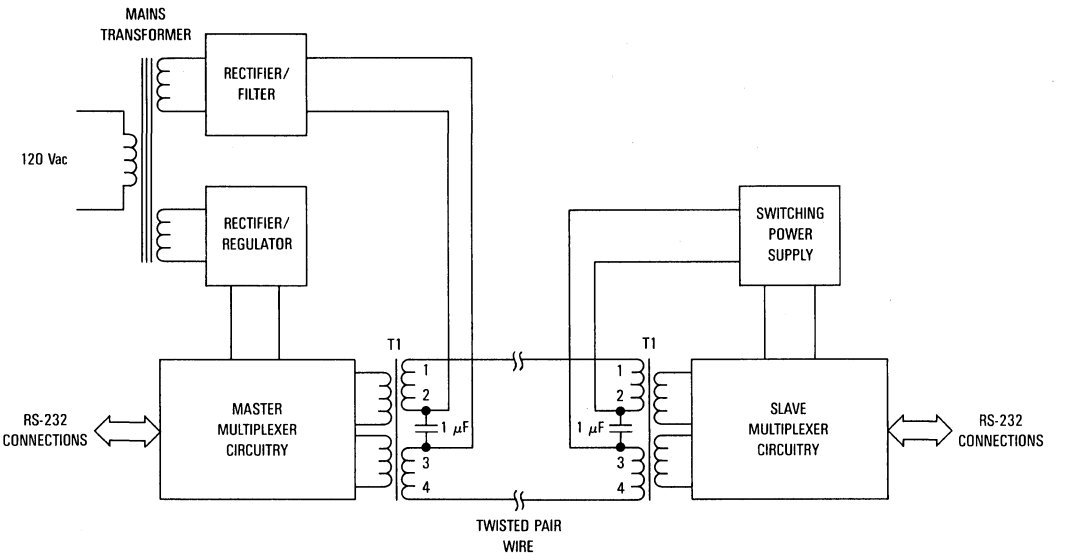


Figure 10. Powering Slave Unit From the Twisted Pair

Engineering Bulletin

By Vince Deems
Telecommunication Applications
Austin, Texas

THE APPLICATION OF A DUPLEXER

The purpose of this document is to explain the application and operation of a duplexer circuit, to show how to balance a duplexer, and to discuss the duplexer's operation analysis when used with two different transformers and with variable components.

The duplexer circuit shown in Figure 1 is a fundamental circuit that is used to help reject the transmit energy from the receive signal. The circuit in Figure 1 is set up for a standard 600 ohm system.

This circuit eliminates the transmit signal from the receiving point by sending a combination of both signals into the inputs of a differential amplifier. This tends to cancel out the transmit signal leaving only the receive signal. A signal is transmitted into Pin 3, the noninverting input, while a signal is being received across Pins 5 and 8 of the transformer, from the same line. There is a 600 ohm impedance when looking into Pins 1 and 4 of the transformer. With R1 tweaked to approximately 600 ohms, a voltage divider network is established with the 600 ohm impedance of the transformer. Thus, the signal at the noninverting input, Pin 5, is Rx + (Tx/2). The signal at the inverting input, Pin 6, is Tx/2 due to the virtual ground concept. When these inputs are added together, the transmit signal cancels leaving Rx, the receive signal, at the output Pin 7.

There are several ways of balancing or tuning duplexers but only one technique will be explained for this application. The transmit Pin 3 is grounded while a 600 ohm signal source with a predetermined level and frequency is connected to Pins 5 and 8 of the transformer. A signal with a level of − 10 dBm (0.6938 Vp-p) and a frequency of 1700 Hz was used in this circuit. R1 is then tweaked such that the voltage across Pins 5 and 8 of the transformer is half the signal voltage or until there is exactly a 6 dB loss across Pins 5 and 8, (i.e., − 16 dBm at Pins 5 and 8). Next, the 600 ohm signal source set at the same level and frequency is connected to Tx (Pin 3) across a 10 kilohm resistor. A 600 ohm resistor is connected to Pins 5 and 8 of the transformer. Then, R2 is tweaked until there is a minimum signal at Rx. Next, several different values of capacitance are tried for C1 until the smallest null is found at Rx. Once the best value of capacitance has been found, the duplexer has been balanced for that particular input signal and the best possible rejection of the transmission signal to the receive signal has been found. This is called the Transhybrid Rejection and is shown with different values of capacitance in Figure 2.

There are several noisy signals that this duplexer can not eliminate at the receive Pin 7. For instance, deflection of the transmit signal off of the transformer returns out of phase and tends to leak through onto the receive signal. For this particular circuit, curve 1 shows the best rejection over the spectrum.

It is worth noting the difference in performance of this duplexer with respect to the type of transformer used. The rejection versus frequency plot shown in Figure 2 was the result obtained when the Midcom 671-0018 was incorporated. This transformer has winding resistances of 14 ohms on the primary coil and 18 ohms on the secondary. The same test was run with a different transformer (Midcom 671-0915) and the results are shown in Figure 3. This transformer has winding resistances of 178 ohms on the primary coil and 67 ohms on the secondary coil giving it a much larger insertion loss than the Midcom 671-0018. This difference is displayed in Figure 3 as there is not as much rejection with the Midcom 671-0915 over the spectrum as with the Midcom 671-0018 (Figure 2).

It can be seen from Figures 2 and 3 that changing the capacitance changes the amount of rejection. This is due to the fact that the coil (Pins 1 and 4) not only has a resistance but also has an inductive reactance. If there is not a proper sized capacitance in parallel with this inductance, then the overall impedance of the coil increases. This impedance changes the voltage divider with R1 which in turn allows a larger Tx at Pin 5 which is slightly out of phase with the Rx + Tx/2 at Pin 6. This allows more leakage of the transmission onto the receive signal thus decreasing the rejection. This difference between the size of the capacitance and the type of transformer to use is a tradeoff which is left to the designer's judgement.

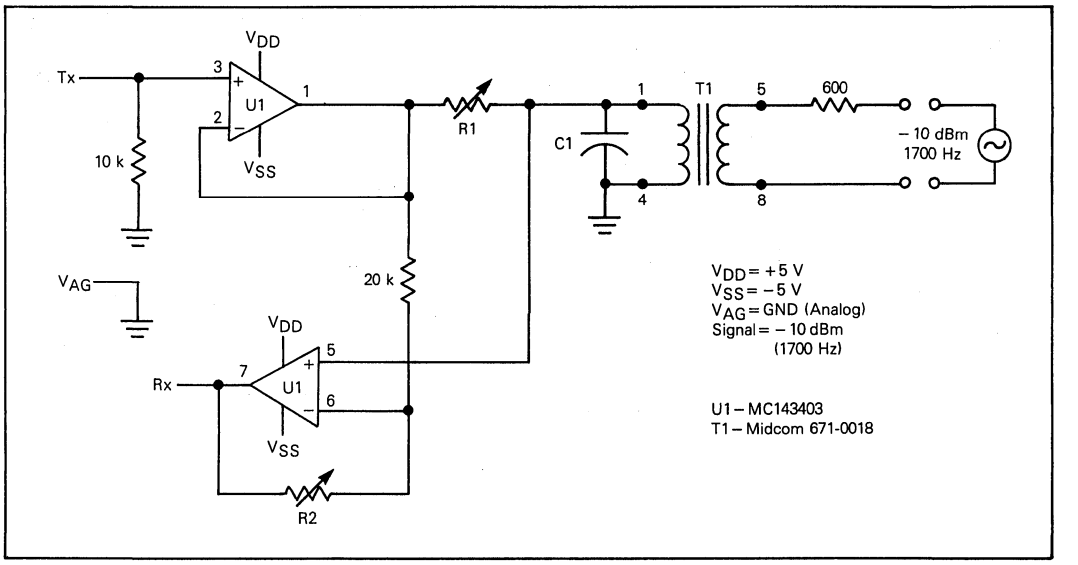


FIGURE 1 — Duplexer Circuit

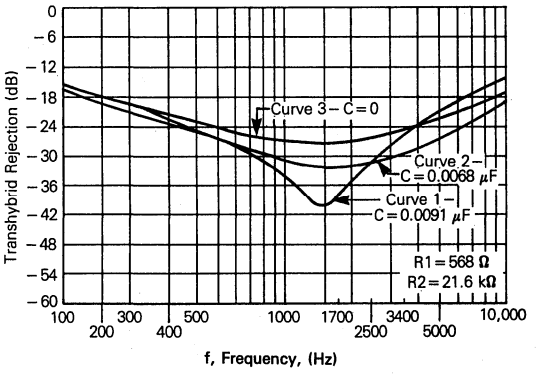


FIGURE 2 — Transhybrid Loss with Midcom 671-0018

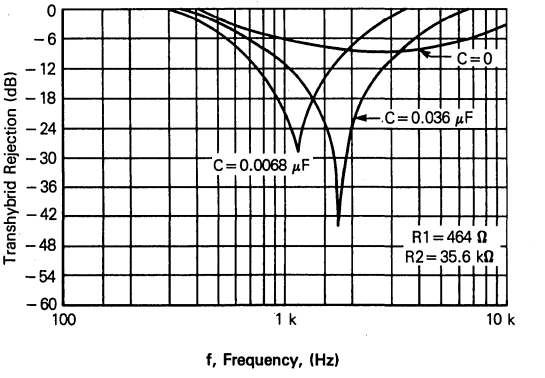


FIGURE 3 — Transhybrid Loss with Midcom 671-0915

IC trio simplifies speech synthesis

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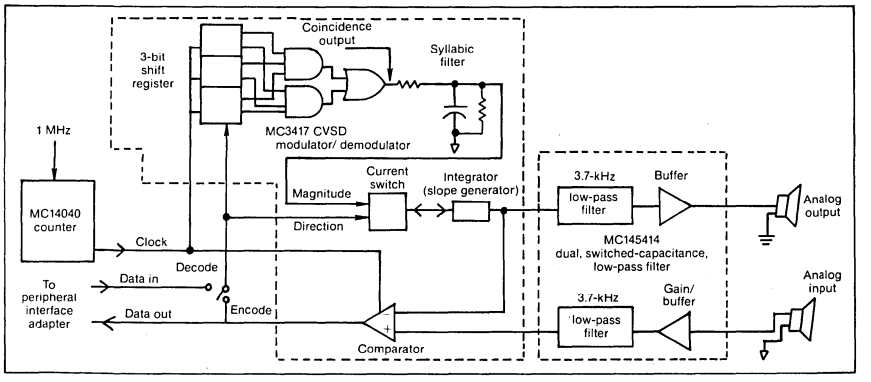
Despite the emergence of special-purpose speech chips, the details of adding voice output to a system are still foreign to most designers. However, they should be happy to learn that highly intelligible speech is possible using a low-cost microprocessor and three readily available integrated circuits.

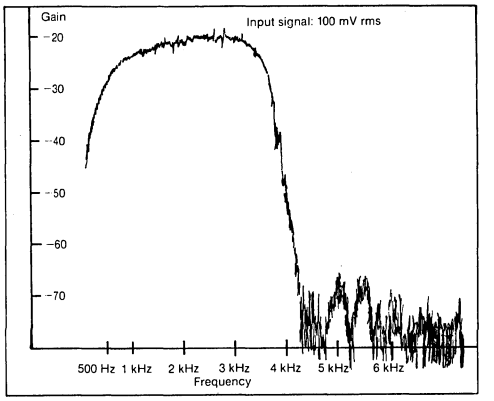
The speech peripheral, which contains an MC3417 continuously variable-slope delta modulator-demodulator, an MC145414 tunable, dual switched-capacitor, low-pass filter, and an MC14040 counter, encodes analog signals into a serial bit stream at a rate of 15,625 bits/s (Fig. 1). The bit stream is then stored in CPU memory. On demand, the peripheral will reproduce an analog signal well enough to be understood easily by an untrained listener.

Such a speech peripheral will enhance the I/O capability of industrial systems, consumer service systems, and games tremendously. Although more CPU memory is required than for linear predictive coding, stored words are easily changed than with LPC. Furthermore, no special memories or complicated calculations are required and no special-purpose synthesizer chips are needed. The encoded speech signals are simply recorded into and played out of CPU memory as any other data. Even the software is simple: words can be packed into ROM or a disk and need only be selected by the microprocessor software for output.

Since the three-IC circuit is designed for speech applications, the bandwidth ranges from 500 Hz to 3.7 kHz (Fig. 2). However, different filter time constants, data rates, and integrator designs can change the frequency range and with it the circuit's



1. At the heart of a three-chip speech peripheral is an MC3417 continuously variable-slope delta modulator-demodulator, which converts an audio waveform into a serial bit stream. The second and newest of the three is an MC145414 dual switched-capacitor low-pass filter with on-board operational amplifiers. An MC14040 12-bit binary counter completes the trio.

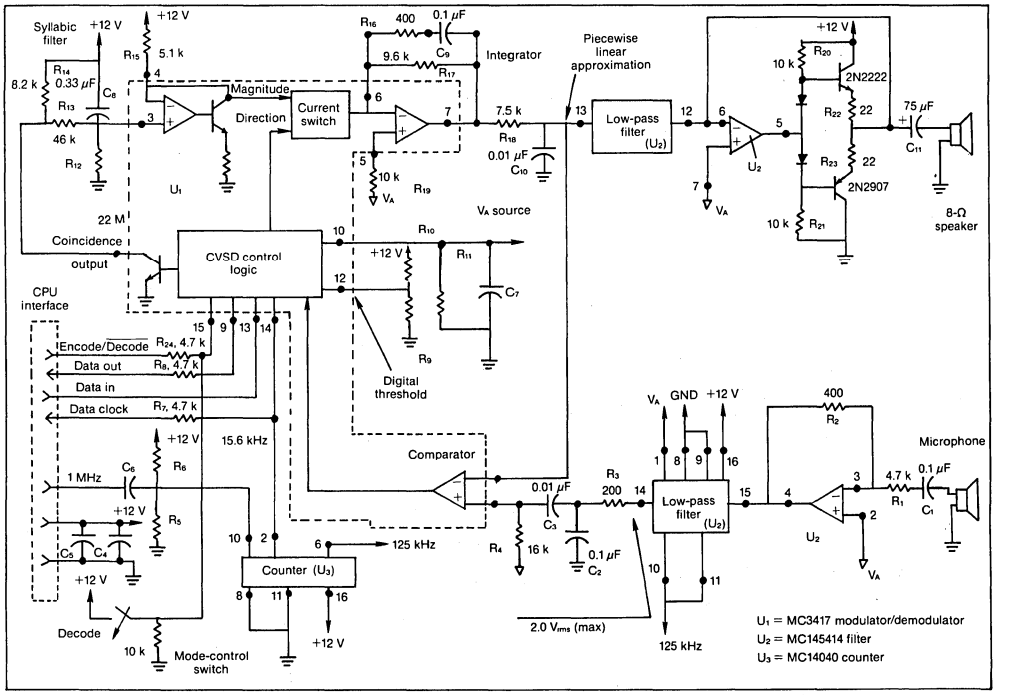


2. The switched-capacitor low-pass filter limits both input and output frequencies to about 3.7 kHz, as reflected by the system frequency response curve. Input frequencies are limited to prevent aliasing; filtering the output smooths it out. Bandwidth for the circuit ranges from 500 Hz to 3.7 kHz.

application. The tradeoffs made for this circuit make it suitable for many industrial applications as well.

About the key chip

Of the three ICs, the key one is the CVSD modulator-demodulator. On board, a current-controlled integrator generates a ramped voltage to linearly approximate the encoded analog waveform in piecewise fashion. Whenever the ramped voltage becomes greater than the input voltage, an on-board comparator switches the direction of the ramp. Digitally, an increasing slope is represented by a 1; a decreasing slope, by a 0. This process is called delta modulation because the slopes change, or delta, is detected. However, the MC3417 does more than simple delta modulation; it performs what is called continuously variable-slope delta modulation (and demodulation). Thus the slope of the ramp voltage —that is, the gain of the chip's integrator—is infinitely variable. This way, in tracking the analog input voltage, the output slope can change more quickly when changes in the analog input demand it. As a result, tracking is more accurate than with any constant-slope delta modulation scheme.



3. A continuously variable slope gives the MC3417 the accuracy to reproduce analog signals. When necessary, the syllabic filter changes the rate of integration and with it the slope. The three basic chips, a simple audio amplifier, and a microprocessor interface complete the speech peripheral circuit.

The MC145414 contains two filters and two operational amplifiers. One filter provides anti-aliasing by cutting off input frequencies above 3.7 kHz. It has a gain of 18 dB. The other filter smooths output noise, but has no inherent gain. One of the chip's on-board operational amplifiers augments the signal from a microphone to about 1 V rms to drive the MC3417's comparator input. At the output, a second op amp and several discrete components drive an 8-Ω speaker.

The MC145414 uses switched-capacitor filters, which need no precise external components for accurate, low-pass analog filtering. Both filters are five-pole, elliptic, low-pass types whose cutoff frequency depends on the sampling clock frequency.

For producing speech, the break frequency (3.7 kHz) requires a 125-kHz clock. The clock is generated by the third IC, a CMOS MC14040 divider, and a 1-MHz master clock derived from the CPU. The three ICs interface with a CPU system, in this case, through an MC6821 peripheral interface adapter (PIA).

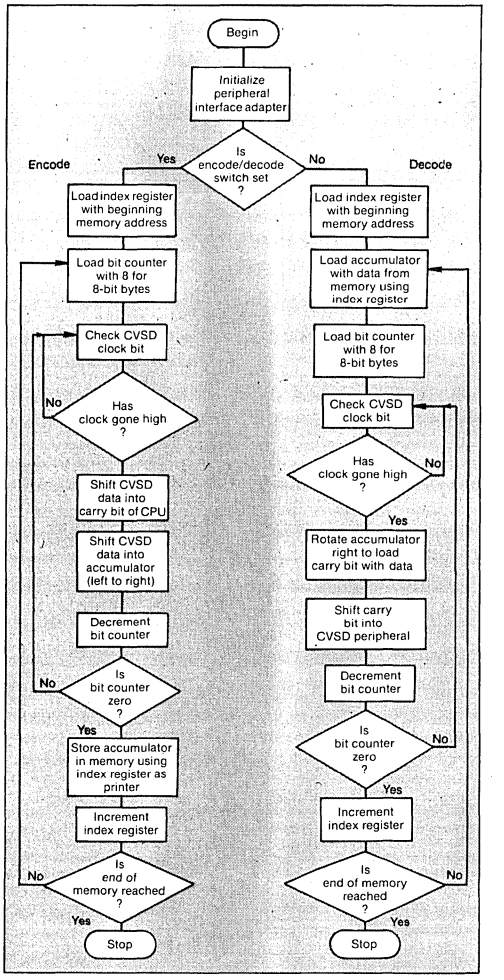
Figure 3 details the entire speech circuit and its two functions: encoding the analog signal into a serial bit stream for the CPU to record and decoding the bit stream into a reconstructed analog waveform. Switch S_1 determines which function to perform by supplying a corresponding level to both the CPU and the CVSD chip.

When switched to encode, analog signals from the microphone are amplified and filtered by one of the op amps and a low-pass filter on board the MC145414. The filtered audio is then fed to the MC3417, where the analog-to-digital conversion produces the serial bit stream. Each high bit means the integrator slope is positive, and each low signals a negative slope. Later, the stored bits are used to control the integrator, whose output approximates the audio signal. In this way, the integrator uses straight lines to reconstruct the original analog waveform.

Thus, when the circuit is set to decode—that is, to output speech—the sequence of bits that translates the serial bit stream into a linear approximation of the original audio is fed to the MC3417, which sends it to the second low-pass filter and op amp on board the MC145414 to smooth out the sequence of linear approximations and provide enough gain to drive a loud-speaker. As a result, with the CPU selecting the sequence of bits (representing words) previously stored in memory, spoken sentences are put out through the peripheral.

Since the speech quality is dramatically affected by the sampling rate, the feedback loop gain, the signal level, and the filtering, there is room to tweak and adjust the sound to suit an application. The circuit represents several tradeoffs to produce highly intelligible speech using a reasonable amount of CPU memory for speech storage, yet requires reasonably few readily available parts.

For example, the transfer function in this application has two poles—one at 160 Hz and one at 280 Hz—and a zero at 4.0 kHz. The pole at 160 Hz provides the long time constant necessary for following relatively linear portions of the original analog



4. The speech peripheral and the controlling microprocessor communicate through a peripheral interface adapter. In addition, clocking and serializing are software tasks, but since the transfer of data between the program and the peripheral is asynchronous, changing the software does not create a timing problem.

```
00001                   ************ MC6800 SPEECH PERIPHERAL DRIVER ************
00002                   *         FOR MC145414 / MC3417 PERIPHERAL CIRCUIT.
00003                   *
00004                   * A PROGRAM TO RECORD AND PLAY SERIAL CVSD DATA.
00005                   *
00006                   * ENTER STARTING MEMORY LOCATION FOR DATA STORAGE
00007                   *  AT LOCATIONS $A000 - $A001.
00008                   *
00009                   * ENTER ENDING MEMORY LOCATIONS FOR DATA STORAGE
00010                   *  AT LOCATIONS $A002 - $A003.
00011                   *
00012                   * PIA IS LOCATED AT ADDRESSES $8004 - $8007.
00013                   *  PIA PB7, PIN 17 IS DATA FROM MC3417 PIN 9.
00014                   *  PIA PB4, PIN 14 IS LEVEL FROM ENCODE/DECODE
00015                   *                SWITCH (ENCODE = ''1'').
00016                   *  PIA PB0, PIN 10 IS DATA TO MC3417 PIN 13.
00017                   *  PIA CB1, PIN 18 IS DATA CLOCK FROM MC14040 PIN 2
00018                   *  PIA PIN 25 IS 1.0000 MHz CLOCK TO MC14040 PIN 10
00019                   *  PIA PIN 20 IS +5.0 VOLTS.
00020                   *  PIA PIN 1 IS GROUND.
00021                   *
00022                   *
00023  8004     PIAA    EQU   $8004
00024  8005     PIACRA  EQU   $8005
00025  8006     PIAB    EQU   $8006
00026  8007     PIACRB  EQU   $8007
00027                   *
00028  A000     DATSRT  EQU   $A000
00029  A002     DATEND  EQU   $A002
00030  A004     COUNTR  EQU   $A004
00031                   *
00032                   *
00033                   ********************************************INITIALIZE PIA
00034 C000              ORG   $C000
00035 C000 86 00        LDA A #$00          ACCESS DATA DIRECTION REG.
00036 C002 B7 8007      STA A PIACRB
00037 C005 86 01        LDA A #$01          BIT FOR OUTPUT.
00038 C007 B7 8006      STA A PIAB
00039 C00A 86 0E        LDA A #$0E          CB1 INTERRUPT ACTIVE GOING HI
00040 C00C B7 C007      STA A PIACRB
00041                   *
00042                   *
00043                   ********************DETERMINE WHICH FUNCTION FROM SWITCH
00044 C00F 86 10        LDA A #$10          SET MASK FOR ENCODE.
00045 C011 B4 8006      AND A PIAB          LOOKS FOR ENCODE SWITCH SET.
00046 C014 27 20        BEQ   DECODE        BRANCH TO APPROPRIATE ROUTINE
00047                   *
00048                   ********************************************ENCODE ROUTINE
00049                   *
00050 C016 FE A000      ENCODE LDX   DATSRT         GET STARTING ADDRESS.
00051 C019 C6 08        BYTLP1 LDA B #$08           SET UP BIT COUNTER.
00052 C01B F7 A004              STA B COUNTR
00053 C01E F6 8007      BITLP1 LDA B PIACRB         CHECK FOR CLOCK TRANSITION.
00054 C021 57                  ROL B
00055 C022 24 FA                BCC   BITLP1        GO BACK FOR CLOCK.
00056 C024 76 8006              ROR   PIAB          SHIFT CODE TO CARRY.
00057 C027 46                   ROR A               SHIFT CARRY TO ACCUMULATOR.
00058 C028 7A A004              DEC   COUNTR        DECREMENT BIT COUNTER.
00059 C02B 26 F1                BNE   BITLP1
00060 C02D A7 00                STA A 0,X           PUT BYTE IN MEMORY.
00061 C02F 08                   INX                 POINT TO NEXT BYTE.
00062 C030 BC A002              CPX   DATEND        CHECK FOR END OF MEMORY BLOCK
00063 C033 26 E4                BNE   BYTLP1
00064 C035 3F                   SWI
00065                   *
00066                   *
00067                   ********************************************DECODE ROUTINE
00068                   *
00069 C036 FE A000      DECODE LDX   DATSRT         GET STARTING ADDRESS.
00070 C039 C6 08        BYTLP2 LDA B #$08           SET UP BIT COUNTER.
00071 C03B F7 A004              STA B COUNTR
00072 C03E A6 00                LDA A 0,X           GET A BYTE FROM MEMORY.
00073 C040 F6 8007      BITLP2 LDA B PIACRB         CHECK FOR CLOCK TRANSITION.
00074 C043 57                  ROL B
00075 C044 24 FA                BCC   BITLP2
00076 C046 46                   ROR A               ROLL DATA INTO CARRY BIT.
00077 C047 79 8006              ROL   PIAB          ROLL CARRY BIT OUT
00078 C04A 7A A004              DEC   COUNTR
00079 C04D 26 F1                BNE   BITLP2
00080 C04F 08                   INX                 POINT TO NEXT BYTE.
00081 C050 BC A002              CPX   DATEND        CHECK FOR END OF MEMORY BLOCK
00082 C053 26 E4                BNE   BYTLP2
00083 C055 3F                   SWI
00084      0000                 END

TOTAL ERRORS 00000
```

5. Conspicuous by its small size, the program for running the speech peripheral circuit performs both encoding and decoding functions in 84 lines, including comments. The routine "reads" the encoding-decoding switch position and branches to the corresponding routine.

waveform; the pole at 280 Hz prevents instantaneous reversals of the integrator's output voltage. The latter action avoids a sawtoothlike peak at extreme values of the audio sine wave, which enables the output to follow rapid changes in the audio waveform more closely.

Finally, the zero at 4.0 kHz improves the phase margin of the MC3417's feedback loop. In a simple delta modulation-demodulation system, the slope of the output signal used to approximate the input is constant. Acceptable speech quality, however, calls for a continuously variable slope—one that increases or decreases with the input. The MC3417 performs continuously variable slope modulation and demodulation so that the slope of the approximating line segments depends on the last three bits clocked into the decoder.

To do that, the MC3417's internal 3-bit shift register monitors the serial bit stream of the comparator. If the comparator detects a series of three or more 1s or three or more 0s in a row, its coincidence pin will go active and the slope of the integrator's output line segments will be made slightly steeper. If three or more consecutive 1s or 0s are detected, a capacitor off the chip will charge up, and the control current of the integrator will be increased continuously.

When the stream of all 1s or all 0s ends, the capacitor is discharged by an external resistor (R_{17}), which, with capacitor C_9, forms a so-called syllabic filter. (Incidentally, the values of R and C are not critical and in this application, the time constant provided by the pair is 50 ms.)

Simple software

As Fig. 4 indicates, the software to record and play speech using this peripheral is simple. The assembly listing for an MC6800 system is given in Fig. 5. In this case, a switch on the CPU board selects the encoding or decoding by setting a high or low level, respectively, at pin 14 of the PIA and pin 15 of the CVSD chip. The encoding routine reads bits serially from the peripheral, performs serial-to-parallel conversion, and saves the encoded data in memory. The program operates asynchronously with the peripheral, allowing different clock rates without changing the software. The CPU simply waits for a data clock edge, then reads the data. The decoding routine works in the same way. The CPU waits for a data clock edge, then sends a bit from memory to the peripheral, which converts it into speech.□

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Turn I/O data port into speech port

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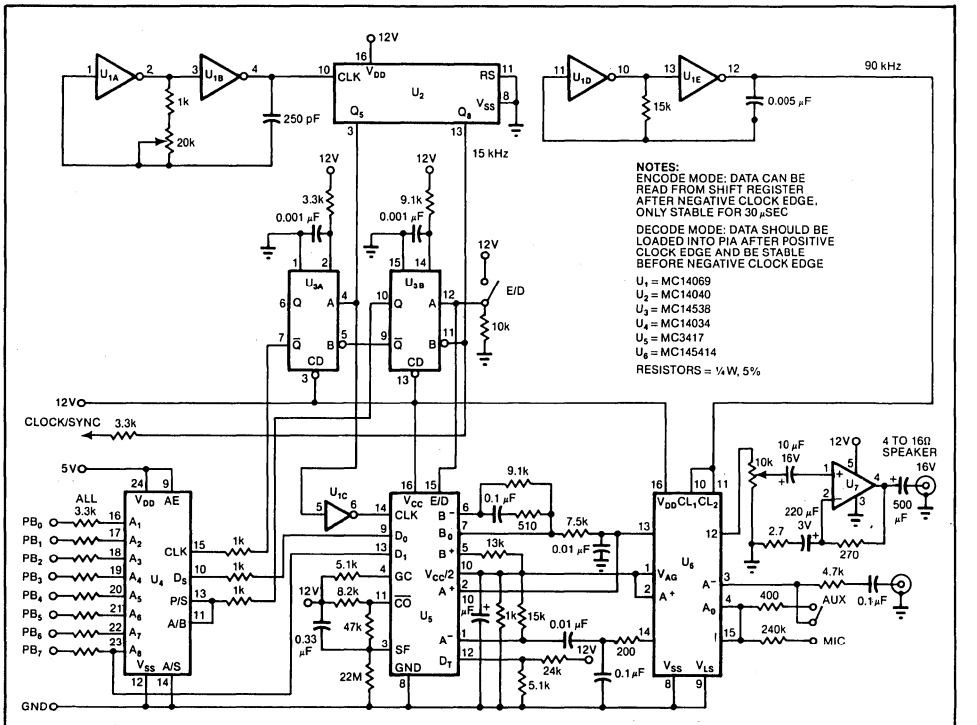
This low-cost, low-power μP peripheral circuit (**figure**) converts an 8-bit I/O data port into a high-quality speech port, using continuously variable slope-delta (CVSD) modulation to encode and decode waveforms per μP direction. The μP can play back any segment of recorded speech; 1 sec of intelligible speech requires ~1.5k bytes of memory. You can trade off between voice quality and memory-storage requirements by adjusting the data-clock rate for the CVSD chip.

To encode speech, an MC145414 CMOS dual switched-capacitor filter/dual op amp (U_6) buffers the signal and band-limits the input to ~2.9 kHz. U_5, an MC3417 linear CVSD modulator/demodulator, encodes the CVSD word and creates a bit stream at ~12k bps. This serial bit stream loads into U_4, where the μP reads it in parallel.

For decoding and outputting speech, the μP loads the MC14014 8-bit shift register (U_4) with parallel data. U_4 shifts the data to U_5 for CVSD decoding. U_6 performs low-pass filtering and buffers the resultant voice waveform.

CMOS ICs U_1, U_2 and U_3 clock the filter and CVSD chips, and U_7 drives a loudspeaker. Four control lines connect with the μP to control data direction and synchronize data clocking. **EDN**



This 8-bit speech circuit *encodes and decodes analog waveforms. Adjust the data-clock rate to trade off between voice quality and memory overhead.*

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AN1510

A Mode Indicator for the MC34118 Speakerphone Circuit

Prepared by: Dennis Morgan

Introduction

In most applications involving a normal conversation, the operating mode (receive, transmit, idle) of the MC34118 speakerphone IC is obvious to the users of the speakerphone. There are some applications, however, where it is beneficial to have an indication of the operating mode. This indication may have to be visual, or logic levels to a microprocessor or other circuitry. This application note describes how to create a mode indicator for use with the MC34118 speakerphone circuit.

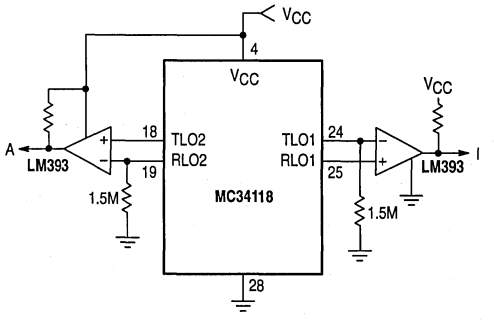
Concept

Within the MC34118 are two comparators driven by the level detectors which are sensing the speech signals (see MC34118/D Data Sheet, Figure 24). The comparators' outputs drive the attenuator control block which sets the operating mode. The circuit described below parallels the internal comparators with external ones.

Circuit

Figure 1 shows the additional circuitry. The two comparators parallel the two which are inside the IC, located at the outputs of the level detectors. Output A will be high when the level detectors on the left side sense a transmit condition, and low when they sense a receive condition. Output B has the opposite polarity.

Figure 1. Mode Indicator Circuit



The two 1.5 MΩ resistors create a slight offset by draining a trickle current out of Pins 19 and 24 in order to well define the idle state. This is necessary due to the fact that when in an idle state (no signal on either side) TLO2 and RLO2 will be very similar in voltage (within a few millivolts of each other). The same is true of TLO1 and RLO1. This, coupled with the normal offset which exists at the comparator inputs, would make it difficult to predict the state of the A and B outputs during idle.

Table 1 defines the comparator outputs. The fast idle mode is uncommon, occurring rarely. Only the slow idle mode is of concern here.

Table 1

Mode	Output	
	A	B
Transmit	High	Low
Receive	Low	High
Slow Idle	High	High
Fast Idle	Low	Low

Circuit Variations

The outputs (A and B) in Figure 1 can be connected to additional circuitry in a variety of ways. Figures 2 to 4 provide a few suggestions. In Figure 2, the A and B outputs are simply directed to a microprocessor for decoding. In Figure 3, LED A will be ON in the receive mode, and LED B will be ON in the transmit mode. In Figure 4, the outputs are decoded to provide an idle/non-idle indication, and a Transmit/Receive indication. Another alternative is to drive LEDs from the decoded outputs of this circuit.

The value of the pull-up resistors at the comparator outputs depends on the circuit which follows the comparators. When driving CMOS logic, for example, 43 kΩ resistors are adequate.

When driving LEDs, they must generally be under 1.0 kΩ, depending on the specific LEDs which must be illuminated. If the circuit is phone-line powered, the pull-up resistors must be as high a value as possible to minimize the drain on the loop current.

The LM393 comparator was chosen due to its low input bias current, as well as its low supply current and input offset. The low bias current is very necessary so as to not upset the level detector outputs any more than absolutely necessary. The resistors at the level detector inputs (Pins 17, 20, 23, 26) will generally have to be readjusted slightly after adding the Figure 1 circuit to compensate for the slight offset which has been added to the system. In most cases, it will be necessary only to slightly increase the resistor at TL12 (Pin 17).

Figure 2

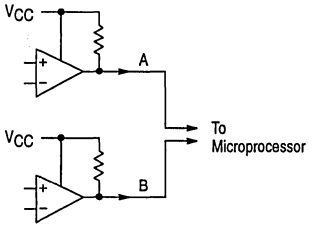


Figure 3

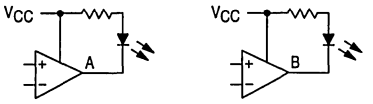
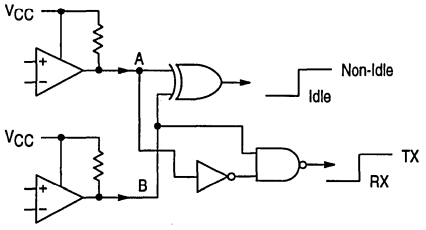


Figure 4



Phase-Locked Loop

Application Notes and Technical Articles

4

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MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN-535
Application Note

PHASE-LOCKED LOOP DESIGN FUNDAMENTALS

INTRODUCTION

The purpose of this application note is to provide the electronic system designer with the necessary tools to design and evaluate Phase Locked Loops (PLL) configured with integrated circuits. The majority of all PLL design problems can be approached using the Laplace transform technique. Therefore, a brief review of Laplace is included to establish a common reference with the reader. Since the scope of this article is practical in nature all theoretical derivations have been omitted hoping to simplify and clarify the content. A bibliography is included for those who desire to pursue the theoretical aspect.

PARAMETER DEFINITION

The Laplace Transform permits the representation of the time response f(t) of a system in the complex domain F(s). This response is twofold in nature in that it contains both the transient and steady state solutions. Thus, all operating conditions are considered and evaluated. The Laplace transform is valid only for positive real time linear parameters; thus, its use must be justified for the PLL which includes both linear and nonlinear functions. This justification is presented in Chapter Three of Phase Lock Techniques by Gardner.[1]

The parameters in Figure 1 are defined and will be used throughout the text.

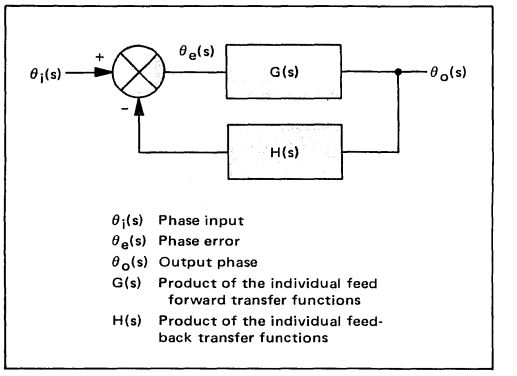

FIGURE 1 – Feedback System

Using servo theory, the following relationships can be obtained.[2]

$$\theta_e(s) = \frac{1}{1 + G(s)\,H(s)}\ \theta_i(s) \qquad (1)$$

$$\theta_O(s) = \frac{G(s)}{1 + G(s)\,H(s)}\ \theta_i(s) \qquad (2)$$

These parameters relate to the functions of a PLL as shown in Figure 2.

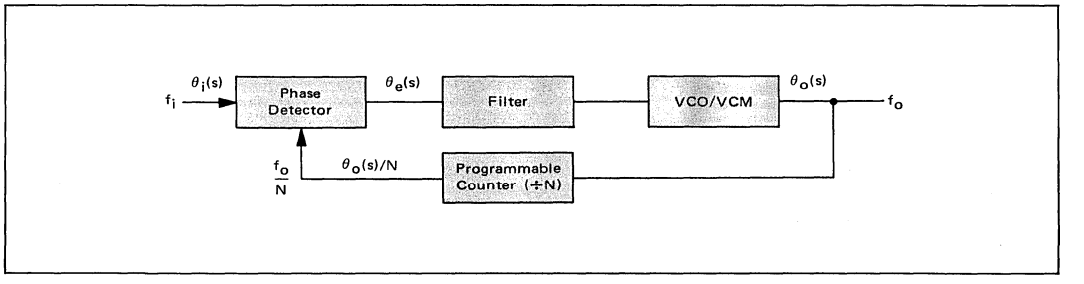

FIGURE 2 – Phase Locked Loop

The phase detector produces a voltage proportional to the phase difference between the signals θ_i and θ_o/N. This voltage upon filtering is used as the control signal for the VCO/VCM (VCM - Voltage Controlled Multivibrator).

Since the VCO/VCM produces a frequency proportional to its input voltage, any time variant signal appearing on the control signal will frequency modulate the VCO/VCM. The output frequency is

$$f_o = N f_i \tag{3}$$

during phase lock. The phase detector, filter, and VCO/VCM compose the feed forward path with the feedback path containing the programmable divider. Removal of the programmable counter produces unity gain in the feedback path (N = 1). As a result, the output frequency is then equal to that of the input.

Various types and orders of loops can be constructed depending upon the configuration of the overall loop transfer function. Identification and examples of these loops are contained in the following two sections.

TYPE – ORDER

These two terms are used somewhat indiscriminately in published literature, and to date there has not been an established standard. However, the most common usage will be identified and used in this article.

The type of a system refers to the number of poles of the loop transfer function G(s) H(s) located at the origin. Example:

$$\text{let} \quad G(s)\,H(s) = \frac{10}{s(s+10)} \tag{4}$$

This is a type one system since there is only one pole at the origin.

The order of a system refers to the highest degree of the polynomial expression

$$1 + G(s)\,H(s) = 0 \triangleq \text{C.E.} \tag{5}$$

which is termed the Characteristic Equation (C.E.). The roots of the characteristic equation become the closed loop poles of the overall transfer function.
Example:

$$G(s)\,H(s) = \frac{10}{s(s+10)} \tag{6}$$

then

$$1 + G(s)\,H(s) = 1 + \frac{10}{s(s+10)} = 0 \tag{7}$$

therefore

$$\text{C.E.} = s(s+10) + 10 \tag{8}$$

$$\text{C.E.} = s^2 + 10s + 10 \tag{9}$$

which is a second order polynomial. Thus, for the given G(s) H(s), we obtain a type 1 second order system.

ERROR CONSTANTS

Various inputs can be applied to a system. Typically these include step position, velocity, and acceleration. The response of type 1, 2, and 3 systems will be examined with the various inputs.

$\theta_e(s)$ represents the phase error that exists in the phase detector between the incoming reference signal $\theta_i(s)$ and the feedback $\theta_o(s)/N$. In evaluating a system, $\theta_e(s)$ must be examined in order to determine if the steady state and transient characteristics are optimum and/or satisfactory. The transient response is a function of loop stability and is covered in the next section. The steady state evaluation can be simplified with the use of the final value theorem associated with Laplace. This theorem permits finding the steady state system error $\theta_e(s)$ resulting from the input $\theta_i(s)$ without transforming back to the time domain.[3]

Simply stated

$$\lim_{t \to \infty} [\theta(t)] = \lim_{s \to o} [s\,\theta_e(s)] \tag{10}$$

Where

$$\theta_e(s) = \frac{1}{1 + G(s)\,H(s)}\ \theta_i(s) \tag{11}$$

The input signal $\theta_i(s)$ is characterized as follows:

$$\text{Step position:} \quad \theta_i(t) = C_p \quad t \geq 0 \tag{12}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{C_p}{s} \tag{13}$$

where C_p is the magnitude of the phase step in radians. This corresponds to shifting the phase of the incoming reference signal by C_p radians:

$$\text{Step velocity:} \quad \theta_i(t) = C_v t \quad t \geq 0 \tag{14}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{C_v}{s^2} \tag{15}$$

where C_v is the magnitude of the rate of change of phase in radians per second. This corresponds to inputing a frequency that is different than the feedback portion of the VCO frequency. Thus, C_v is the frequency difference in radians per second seen at the phase detector.

$$\text{Step acceleration:} \quad \theta_i(t) = C_a t^2 \quad t \geq 0 \tag{16}$$

$$\text{Or, in Laplace notation:} \quad \theta_i(s) = \frac{2\,C_a}{s^3} \tag{17}$$

C_a is the magnitude of the frequency rate of change in radians per second per second. This is characterized by a time variant frequency input.

Typical loop G(s) H(s) transfer functions for types 1, 2, and 3 are:

$$\text{Type 1} \quad G(s)\,H(s) = \frac{K}{s(s+a)} \tag{18}$$

$$\text{Type 2}\quad G(s)\,H(s) = \frac{K(s+a)}{s^2} \tag{19}$$

$$\text{Type 3}\quad G(s)\,H(s) = \frac{K(s+a)(s+b)}{s^3} \tag{20}$$

The final value of the phase error for a type 1 system with a step phase input is found by using Equations 11 and 13.

$$\theta_e(s) = \left(\frac{1}{1+\frac{K}{s(s+a)}}\right)\left(\frac{C_p}{s}\right)$$

$$= \frac{(s+a)C_p}{(s^2+as+K)} \tag{21}$$

$$\theta_e(t=\infty) = \lim_{s\to o}\left[s\left(\frac{s+a}{s^2+as+K}\right)C_p\right] = 0 \tag{22}$$

Thus the final value of the phase error is zero when a step position (phase) is applied.

Similarly applying the three inputs into type 1, 2 and 3 systems and utilizing the final value theorem, the following table can be constructed showing the respective steady state phase errors.

TABLE I — Steady State Phase Errors for Various System Types

	Type 1	Type 2	Type 3
Step Position	Zero	Zero	Zero
Step Velocity	Constant	Zero	Zero
Step Acceleration	Continually Increasing	Constant	Zero

A zero phase error identifies phase coherence between the two input signals at the phase detector.

A constant phase error identifies a phase differential between the two input signals at the phase detector. The magnitude of this differential phase error is proportional to the loop gain and the magnitude of the input step.

A continually increasing phase error identifies a time rate change of phase. This is an unlocked condition for the phase loop.

Using Table I the system type can be determined for specific inputs. For instance, if it is desired for a PLL to track a reference frequency (step velocity) with zero phase error, a minimum of type 2 is required.

STABILITY

The root locus technique of determining the position of system poles and zeroes in the s-plane is often used to graphically visualize the system stability. The graph or plot illustrates how the closed loop poles (roots of the characteristic equation) vary with loop gain. For stability all poles must lie in the left half of the s-plane. The relationship of the system poles and zeroes then determine the degree of stability. The root locus contour can be determined by using the following guidelines.[2]

Rule 1 - The root locus begins at the poles of G(s) H(s) (K = 0) and ends at the zeroes of G(s) H(s) (K = ∞). Where K is loop gain.

Rule 2 - The number of root loci branches is equal to the number of poles or number of zeroes, whichever is greater. The number of zeroes at infinity is the difference between the number of finite poles and finite zeroes of G(s) H(s).

Rule 3 - The root locus contour is bounded by asymptotes whose angular position is given by

$$\frac{(2n+1)}{\#P - \#Z}\pi;\ n = 0, 1, 2, \ldots \tag{23}$$

Where #P (#Z) is the number of poles (zeroes).

Rule 4 - The intersection of the asymptotes is positioned at the center of gravity C. G.

$$C.G. = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} \tag{24}$$

Where ΣP (ΣZ) denotes the summation of the poles (zeroes).

Rule 5 - On a given section of the real axis, root loci may be found in the section only if the #P + #Z to the right is odd.

Rule 6 - Breakaway points from negative real axis is given by:

$$\frac{dK}{ds} = 0 \tag{25}$$

Again where K is the loop gain variable factored from the characteristic equation.

Example:

The root locus for a typical loop transfer function is found as follows:

$$G(s)\,H(s) = \frac{K}{s(s+4)} \tag{26}$$

The root locus has two branches (Rule 2) which begin at s = 0 and s = –4 and ends at the two zeroes located at infinity (Rule 1). The asymptotes can be found according to Rule 3. Since there are two poles and no zeroes the equation becomes:

$$\frac{2n+1}{2}\pi = \begin{cases} \frac{\pi}{2} & \text{for } n = 0 \\ \frac{3\pi}{2} & \text{for } n = 1 \end{cases} \tag{27}$$

The position of the intersection according to the Rule 4 is:

$$s = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} = \frac{(-4-0) - (0)}{2-0}$$

$$s = -2 \qquad (28)$$

The breakaway point as defined by Rule 6 can be found by first writing the characteristic equation.

$$\text{C.E.} = 1 + G(s)\,H(s) = 0$$

$$= 1 + \frac{K}{s(s+4)} = s^2 + 4s + K = 0 \qquad (29)$$

Now solving for K yields

$$K = -s^2 - 4s \qquad (30)$$

Taking the derivative with respect to s and setting it equal to zero then determines the breakaway point.

$$\frac{dK}{ds} = \frac{d}{ds}(-s^2 - 4s) \qquad (31)$$

$$\frac{dK}{ds} = -2s - 4 = 0 \qquad (32)$$

or

$$s = -2 \qquad (33)$$

is the point of departure. Using this information, the root locus can be plotted as in Figure 3.

This second order characteristic equation given by Equation 29 has been normalized to a standard form[2]

$$s^2 + 2\zeta\,\omega_n s + \omega^2_n \qquad (34)$$

where the damping ratio $\zeta = \text{Cos}\,\phi$ ($0^o \leqslant \phi \leqslant 90^o$) and ω_n is the natural frequency as shown in Figure 3.

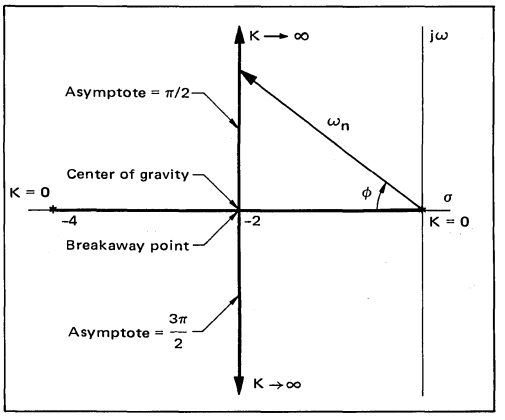

FIGURE 3 – Type 1 Second Order Root Locus Contour

The response of this type 1, second order system to a step input is shown in Figure 4. These curves represent the phase response to a step position (phase) input for various damping ratios. The output frequency response as a function of time to a step velocity (frequency) input is also characterized by the same set of figures.

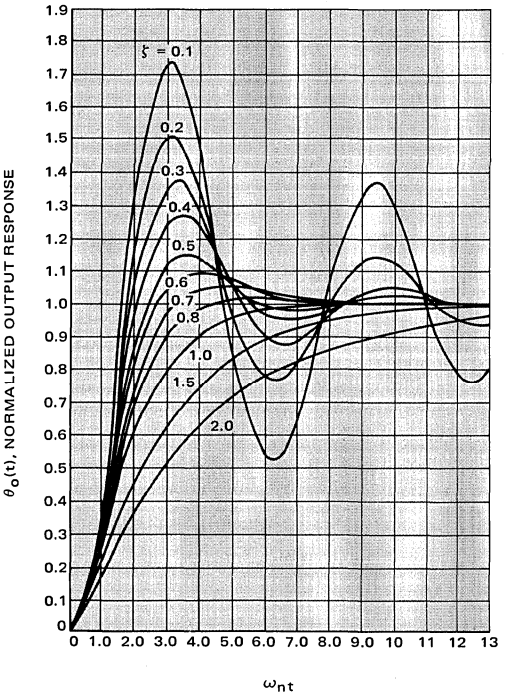

FIGURE 4 – Type 1 Second Order Step Response

The overshoot and stability as a function of the damping ratio ζ is illustrated by the various plots. Each response is plotted as a function of the normalized time $\omega_n t$. For a given ζ and a lock-up time t, the ω_n required to achieve the desired results can be determined. Example:

Assume $\zeta = 0.5$
error $< 10\%$
for $t > 1$ ms

From $\zeta = 0.5$ curve the error is less than 10% of final value for all time greater than $\omega_n t = 4.5$. The required ω_n can then be found by:

$$\omega_n t = 4.5 \qquad (35)$$

or

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5 \text{ k rad/s} \qquad (36)$$

ζ is typically selected between 0.5 and 1 to yield optimum overshoot and noise performance.

Example:

Another common loop transfer function takes the form

$$G(s)\,H(s) = \frac{(s+a)k}{s^2} \qquad (37)$$

This is a type 2 second order system. A zero is added to provide stability. (Without the zero the poles would move along the $j\omega$ axis as a function of gain and the system would at all times be oscillatory in nature.) The root locus shown in Figure 5 has two branches beginning at the origin with one asymptote located at 180 degrees. The center of gravity is s = a; however, with only one asymptote there is no intersection at this point. The root locus lies on a circle centered at s = -a and continues on all portions of the negative real axis to left of the zero. The breakaway point is s = -2a.

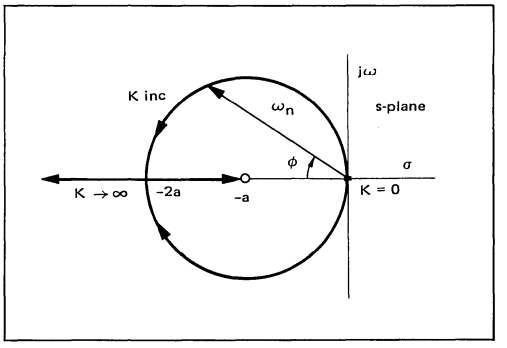

FIGURE 5 — Type 2 Second Order Root Locus Contour

The respective phase or output frequency response of this type 2 second order system to a step position (phase) or velocity (frequency) input is shown in Figure 6. As illustrated in the previous example the required ω_n can be determined by the use of the graph when ζ and the lock up time are given.

BANDWIDTH

The -3 dB bandwidth of the PLL is given by

$$\omega_{-3\ dB} = \omega_n\left(1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (38)$$

for a type 1 second order[4] system, and by

$$\omega_{-3\ dB} = \omega_n\left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (39)$$

for a type 2 second order[1] system.

PHASE-LOCKED LOOP DESIGN EXAMPLE

The design of a PLL typically involves determining the type of loop required, selecting the proper bandwidth, and establishing the desired stability. A fundamental approach

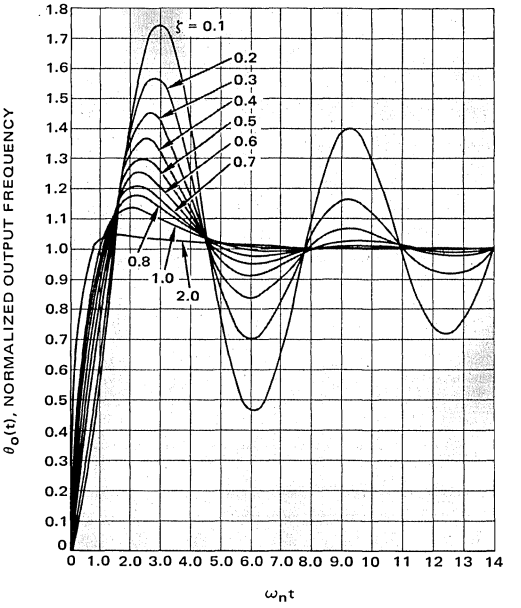

FIGURE 6 — Type 2 Second Order Step Response

to these design constraints is now illustrated. It is desired for the system to have the following specifications:

Output frequency	2.0 MHz to 3.0 MHz
Frequency steps	100 kHz
Phase coherent frequency output	—
Lock-up time between channels	1 ms
Overshoot	< 20%

NOTE: These specifications characterize a system function similar to a variable time base generator or a frequency synthesizer.

From the given specifications the circuit parameters shown in Figure 7 can now be determined.

The devices used to configure the PLL are:

Frequency-Phase Detector	MC4044/4344
Voltage Controlled Multivibrator (VCM)	MC4024/4324
Programmable Counter	MC4016/4316

The forward and feedback transfer functions are given by:

$$G(s) = K_p\,K_f\,K_o \qquad H(s) = K_n \qquad (40)$$

where $K_n = 1/N$ (41)

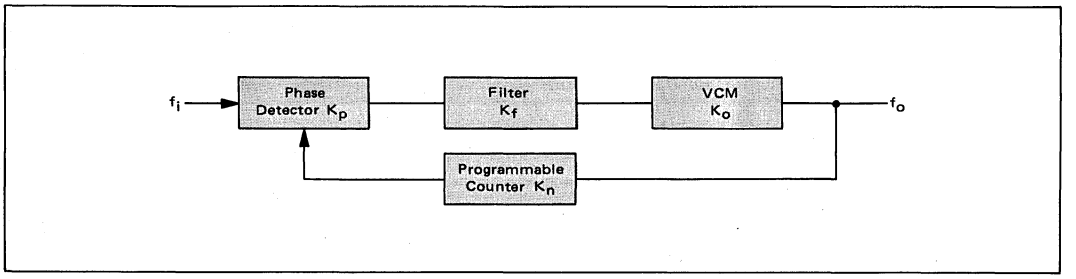

FIGURE 7 – Phase Locked Loop Circuit Parameters

The programmable counter divide ratio K_n can be found from Equation 3.

$$N_{min} = \frac{f_{o\,min}}{f_i} = \frac{f_{o\,min}}{f_{step}} = \frac{2\text{ MHz}}{100\text{ kHz}} = 20 \qquad (42)$$

$$N_{max} = \frac{f_{o\,max}}{f_{step}} = \frac{3\text{ MHz}}{100\text{ kHz}} = 30 \qquad (43)$$

$$K_n = \frac{1}{20} \text{ to } \frac{1}{30} \qquad (44)$$

A type 2 system is required to produce a phase coherent output relative to the input (see Table I). The root locus contour is shown in Figure 5 and the system step response is illustrated by Figure 6.

The operating range of the MC4024/4324 VCM must cover 2 MHz to 3 MHz. Selecting the VCM control capacitor according to the rules contained on the data sheet yields C = 100 pF. The desired operating range is then centered within the total range of the device. The input voltage versus output frequency is shown in Figure 8.

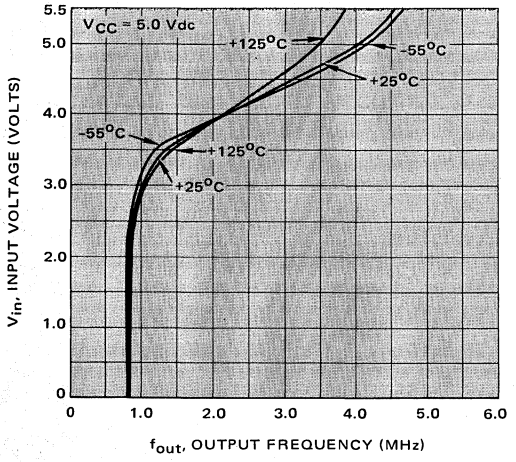

FIGURE 8 – MC4324 Input Voltage versus Output Frequency (100 pF Feedback Capacitor)

The transfer function of the VCM is given by

$$K_o = \frac{K_v}{s} \qquad (45)$$

Where K_v is the sensitivity in radians per second per volt. From the curve in Figure 8, K_v is found by taking the reciprocal of the slope.

$$K_v = \frac{4\text{ MHz} - 1.5\text{ MHz}}{5\text{ V} - 3.6\text{ V}}\ 2\pi \text{ rad/s/V}$$

$$K_v = 11.2 \text{ X } 10^6 \text{ rad/s/V} \qquad (46)$$

Thus

$$K_o = \frac{11.2 \text{ X } 10^6}{s} \text{ rad/s/V} \qquad (47)$$

The s in the denominator converts the frequency characteristics of the VCM to phase, i.e., phase is the integral of frequency.

The gain constant for the MC4044/4344 phase detector is found by [5]

$$K_p = \frac{\text{DF High - UF Low}}{2(2\pi)} = \frac{2.3\text{ V} - 0.9\text{ V}}{4\pi} = 0.111\text{ V/rad} \qquad (48)$$

Since a type 2 system is required (phase coherent output) the loop transfer function must take the form of Equation 19. The parameters thus far determined include K_p, K_o, K_n leaving only K_f as the variable for design. Writing the loop transfer function and relating it to Equation 19

$$G(s)\,H(s) = \frac{K_p\,K_v\,K_n\,K_f}{s} = \frac{K(s+a)}{s^2} \qquad (49)$$

Thus K_f must take the form

$$K_f = \frac{s+a}{s} \qquad (50)$$

in order to provide all the necessary poles and zeroes for

the required G(s) H(s). The circuit shown in Figure 9 yields the desired results.

K_f is expressed by

$$K_f = \frac{R_2Cs + 1}{R_1Cs} \quad \text{for large A} \qquad (51)$$

where A is voltage gain of the amplifier.

R_1, R_2, and C are then the variables used to establish the overall loop characteristics.

The MC4044/4344 provides the active circuitry required to configure the filter K_f. An additional low current high β buffering device or FET can be used to boost the input impedance thus minimizing the leakage current from the capacitor C between sample updates. As a result longer sample periods are achievable.

Since the gain of the active filter circuitry in the MC4044/4344 is not infinite, a gain correction factor K_c must be applied to K_f in order to properly characterize the function. K_c is found experimentally to be $K_c = 0.5$.

$$K_{fc} = K_f K_c = 0.5 \left(\frac{R_2Cs + 1}{R_1Cs} \right) \qquad (52)$$

(For large gain, Equation 51 applies.)

The PLL circuit diagram is shown in Figure 10 and its Laplace representation in Figure 11.

The loop transfer function is

$$G(s)\,H(s) = K_p K_{fc} K_o K_n \qquad (53)$$

$$G(s)\,H(s) = K_p (0.5) \left(\frac{R_2Cs + 1}{R_1Cs} \right) \left(\frac{K_v}{s} \right) \left(\frac{1}{N} \right) \qquad (54)$$

The characteristic equation takes the form

$$C.E. = 1 + G(s)\,H(s) = 0$$

$$= s^2 + \frac{0.5\,K_p K_v R_2}{R_1 N} s + \frac{0.5\,K_p K_v}{R_1 CN} \qquad (55)$$

Relating Equation 55 to the standard form given by Equation 34

$$s^2 + \frac{0.5\,K_p K_v R_2}{R_1 N} s + \frac{0.5\,K_p K_v}{R_1 CN}$$

$$= s^2 + 2\zeta \omega_n s + \omega_n^2 \qquad (56)$$

Equating like coefficients yields

$$\frac{0.5\,K_p K_v}{R_1 CN} = \omega_n^2 \qquad (57)$$

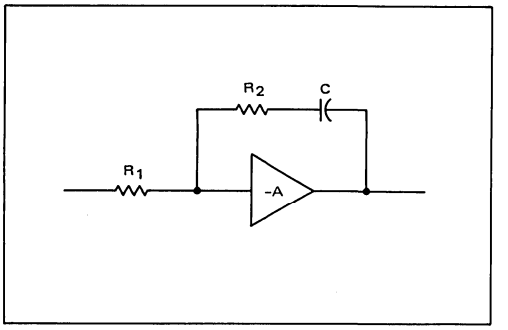

FIGURE 9 – Active Filter Design

and $$\frac{0.5\,K_p K_v R_2}{R_1 N} = 2\zeta \omega_n \qquad (58)$$

With the use of an active filter whose open loop gain (A) is large ($K_c = 1$), Equations 57 and 58 become

$$\frac{K_p K_v}{R_1 CN} = \omega_n^2 \qquad (59)$$

$$\frac{K_p K_v R_2}{R_1 N} = 2\zeta \omega_n \qquad (60)$$

The percent overshoot and settling time are now used to determine ω_n. From Figure 6 it is seen that a damping ratio $\zeta = 0.8$ will produce a peak overshoot less than 20% and will settle to within 5% at $\omega_n t = 4.5$. The required lock-up time is 1 ms.

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5 \text{ k rad/s} \qquad (61)$$

Rewriting Equation 57

$$R_1 C = \frac{0.5\,K_p K_v}{\omega_n^2 N} \qquad (62)$$

$$= \frac{(0.5)\,(0.111)\,(11.2 \times 10^6)}{(4500)^2\,(30)}$$

$$R_1 C = 0.00102$$

(Maximum overshoot occurs at N_{max} which is minimum loop gain)

Let $C = 0.5\ \mu F$

Then $$R_1 = \frac{0.00102}{0.5 \times 10^{-6}} = 2.04\ k\Omega$$

Use $R_1 = 2\ k\Omega$

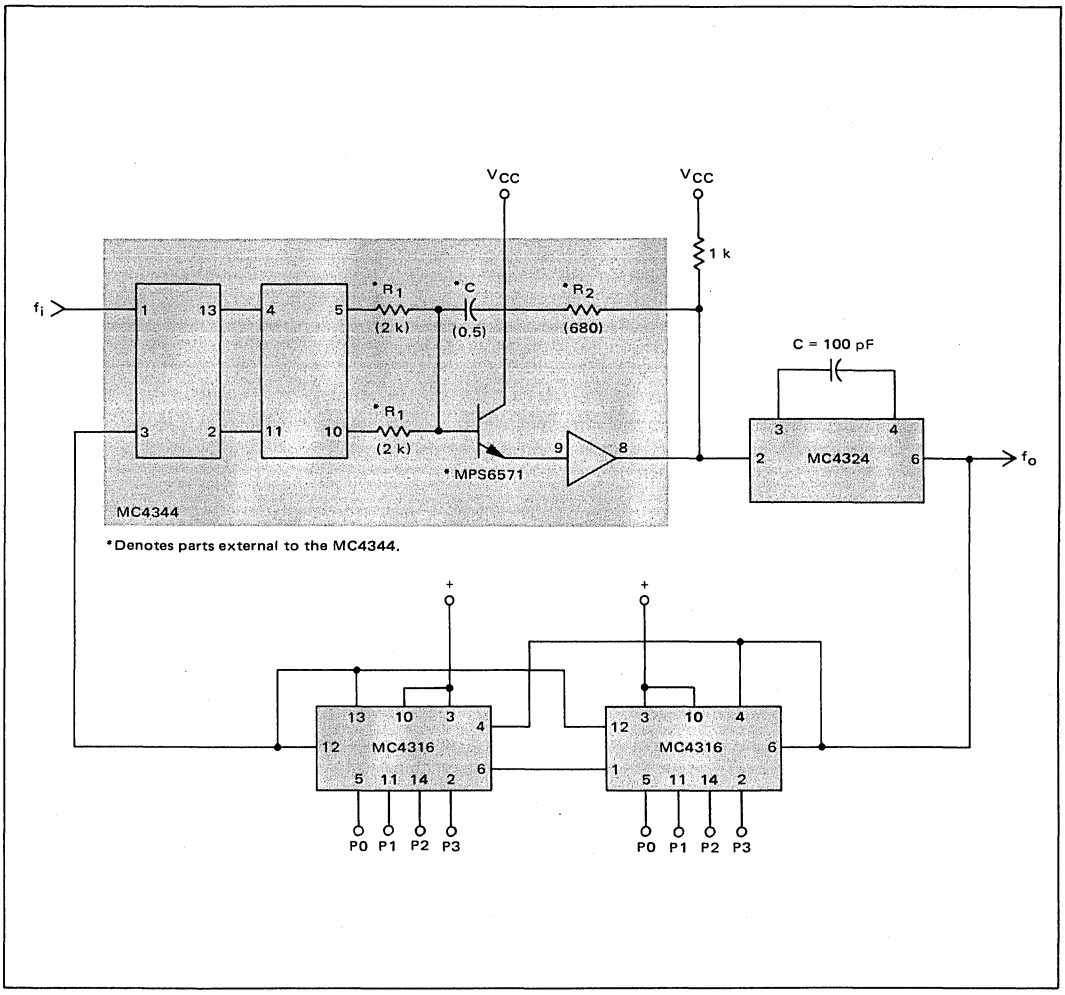

FIGURE 10 – Circuit Diagram of Type 2 Phase Locked Loop

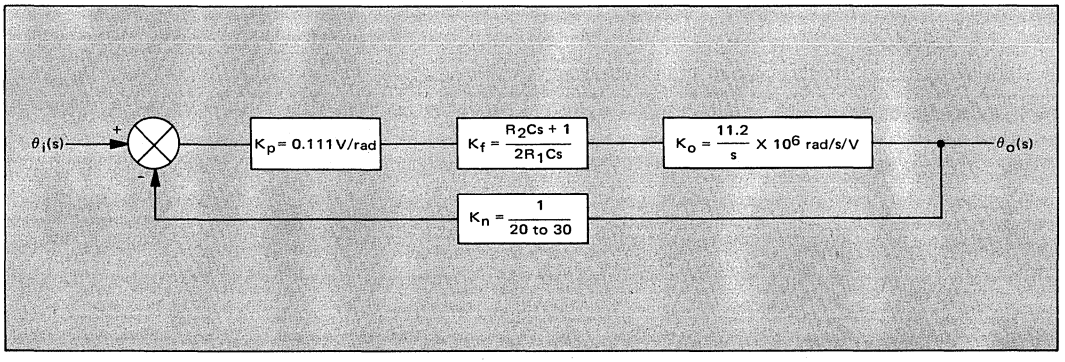

FIGURE 11 – Laplace Representation of Diagram in Figure 10

R_1 is typically selected greater than 1 kΩ.

Solving for R_2 in Equation 58

$$R_2 = \frac{2\zeta\,\omega_n R_1 N}{K_p K_v (0.5)} = \frac{2\zeta}{C\,\omega_n} \qquad (63)$$

$$= \frac{2(0.8)}{(0.5 \times 10^{-6})(4.5\text{ k})}$$

$$= 711\ \Omega$$

use $R_2 = 680\ \Omega$

All circuit parameters have now been determined and the PLL can be properly configured.

Since the loop gain is a function of the divide ratio K_n, the closed loop poles will vary is position as K_n varies. The root locus shown in Figure 12 illustrates the closed loop pole variation.

The loop was designed for the programmable counter N = 30. The system response for N = 20 exhibits a wider bandwidth and larger damping factor, thus reducing both lock-up time and percent overshoot (see Figure 14).

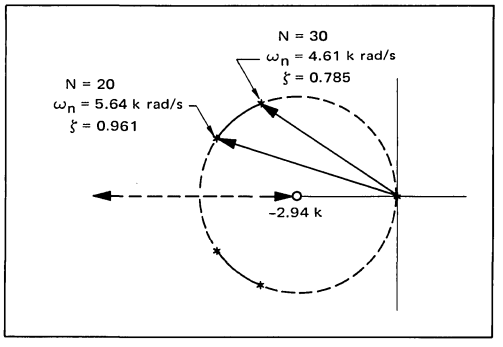

FIGURE 12 – Root Locus Variation

NOTE: The type 2 second order loop was illustrated as a design example because it provides excellent performance for both type 1 and 2 applications. Even in systems that do not require phase coherency a type 2 loop still offers an optimum design.

EXPERIMENTAL RESULTS

Figure 13 shows the theoretical transient frequency response of the previously designed system. The curve N = 30 illustrates the frequency response when the programmable counter is stepped from 29 to 30 thus producing a change in the output frequency from 2.9 MHz to 3.0 MHz. An overshoot of 18% is obtained and the output frequency is within 5 kHz of the final value one millisecond after the applied step. The curve N = 20 illustrates the output frequency change as the programmable counter is stepped from 21 to 20.

Since the output frequency is proportional to the VCM control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 2 of the VCM. The average frequency response as calculated by the Laplace method is found experimentally by smoothing this voltage at pin 2 with a simple RC filter whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time. With the programmable counter set at 29 the quiescent control voltage at pin 2 is approximately 4.37 volts. Upon changing the counter divide ratio to 30 the control voltage increases to 4.43 volts as shown in Figure 14. A similar transient occurs when stepping the programmable counter from 21 to 20. Figure 14 illustrates that the experimental results obtained from the configured system follows the predicted results shown in Figure 13. Linearity is maintained for phase errors less than 2π, i.e. there is no cycle slippage at the phase detector.

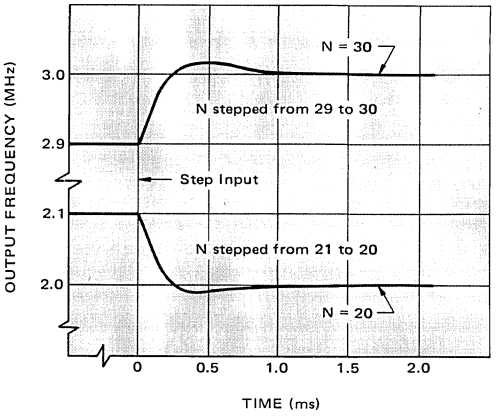

FIGURE 13 – Frequency-Time Response

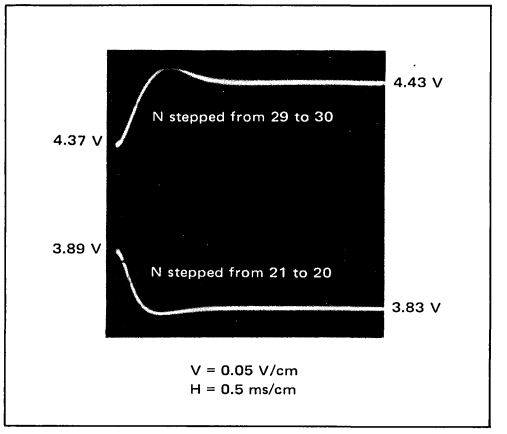

FIGURE 14 – VCM Control Voltage (Frequency) Transient

*THE PARAMETERS LISTED BELOW APPLY TO THE FOLLOWING PLOT

PHASE DETECTOR GAIN CONSTANT	P1 = 0.111 VOLTS PER RADIAN
VCM GAIN CONSTANT	V1 = 1.12 E+7 RAD PER VOLT
FILTER INPUT RESISTOR	R1 = 3900 OHMS ($R1_C$ = 2 k)
FILTER FEEDBACK RESISTOR	R2 = 680 OHMS
FILTER CAPACITOR	C1 = 0.5 MICROFARADS
DIVIDER VALUE	N1-N2 = 29 - 30
REFERENCE FREQUENCY	F1 = 100000 CPS
OUTPUT FREQUENCY CHANGE	F5 = 100000 CPS

P2 = 0.111	C2 = 0.5
V2 = 1.12 E+7	N3 - N4 = 21 - 20
R3 = 3900 ($R1_C$ = 2 k)	F2 (F6) = 100000 (100000)
R4 = 680	

PLOT OF FUNCTIONS

(NOTE: Y(T) IS PLOTTED '+', Z(T) IS '*', AND '0' IS COMMON)

FOR T: TOP = 0 BOTTOM = 0.0015 INCREMENT = 0.00005
FOR FCTS: LEFT = 0 RIGHT = 0.12 INCREMENT = 0.002

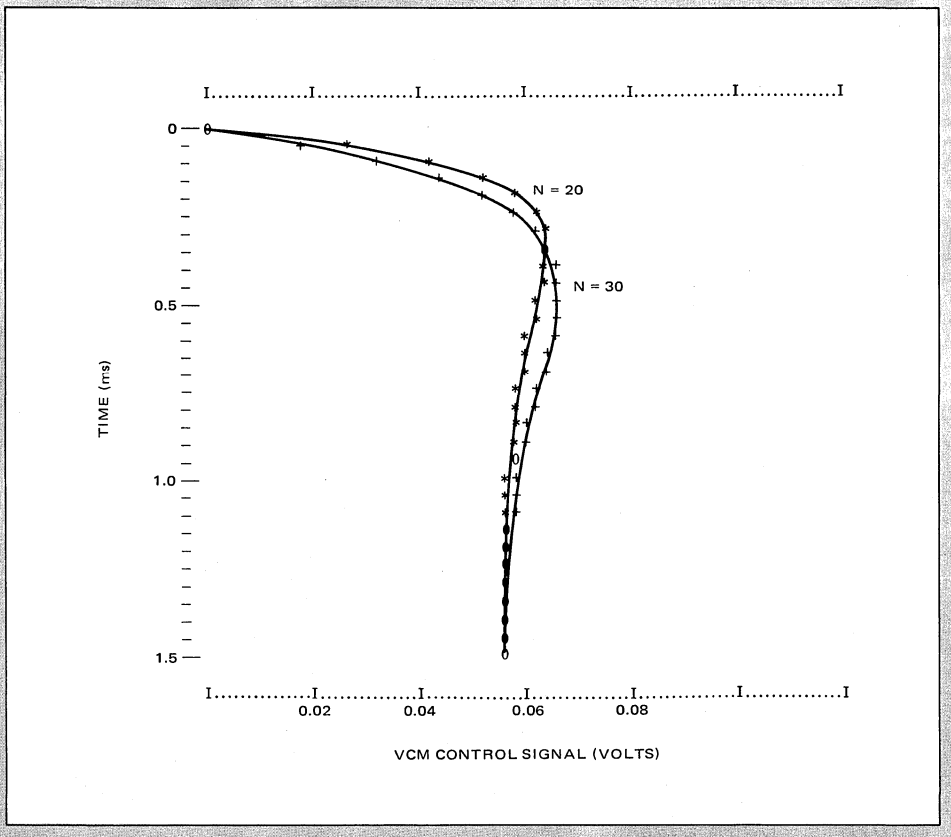

FIGURE 15 – VCM Control Signal Transient

Figure 15 is a theoretical plot of the VCM control voltage transient as calculated by a computer program. The computer program is written with the parameters of Equations 58 and 59 (type 2) as the input variables and is valid for all damping ratios of $\zeta \leqslant 1.0$. The program prints or plots the control voltage transient versus time for desired settings of the programmable counter. The lock-up time can then be readily determined as the various parameters are varied. (If stepping from a higher divide ratio to a lower one the transient will be negative.) Figures 14 and 15 also exhibit a close correlation between the experimental and analytical results.

SUMMARY

This application note describes the basic control system techniques required for phase-locked loop design. Criteria for the selection of the optimum type of loop and methods for establishing the desired performance characteristics are presented. A design example is illustrated in a step-by-step approach along with the comparison of the experimental and analytical results.

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MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN-827
Application Note

THE TECHNIQUE OF DIRECT PROGRAMMING BY USING A TWO-MODULUS PRESCALER

Prepared by
PLL Applications

INTRODUCTION

The MC12009, MC12011, or MC12013 can be used as part of a variable modulus (divisor) prescaling subsystem used in certain Digital Phase-Locked Loops (PLL).

More often than not, the feedback loop of any PLL contains a counter-divider. Many methods are available for building a divider, but not all are simple, economical, or convenient in a particular application.

The technique and system described here offer a new approach to the construction of a phase-locked loop divider. In addition to using either the MC12009, MC12011, or the MC12013 variable modulus prescaler, this system requires an MC12014 Counter Control Logic Function, together with suitable programmable counters (e.g., MC4016s or SN74LS716s). Data sheets for these additional devices should be consulted for their particular functional descriptions.

DESIGN CONSIDERATIONS

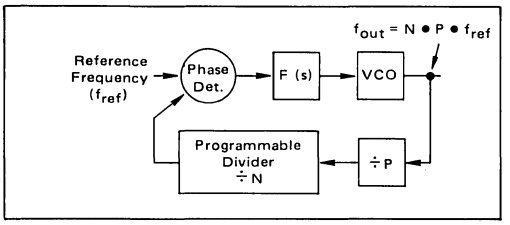
The disadvantage of using a fixed modulus (÷ P) for frequency division in high-frequency phase-locked loops (PLL) is that it requires dividing the desired reference frequency by P also (desired reference frequency equals channel spacing).

The MC12009/11/13 are especially designed for use with a technique called "variable modulus prescaling". This technique allows a simple MECL two-modulus prescaler to be controlled by a relatively slow MTTL programmer counter. The use of this technique permits direct high-frequency prescaling without any sacrifice in resolution since it is no longer necessary to divide the reference frequency by the modulus of the high-frequency prescaler.

The theory of "variable modulus prescaling" may be explained by considering the system shown in Figure 1. For the loop shown:

$$f_{out} = N \bullet P \bullet f_{ref} \quad (1)$$

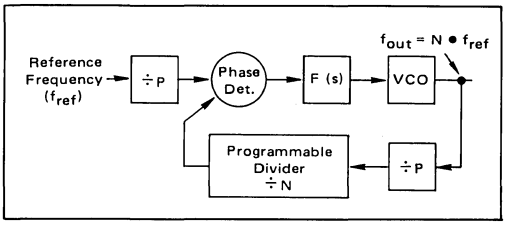
FIGURE 1 – FREQUENCY SYNTHESIS BY PRESCALING



where P is fixed and N is variable. For a change of 1 in N, the output frequency changes by $P \bullet f_{ref}$. If f_{ref} equals the desired channel spacing, then only every P channel may be programmed using this method. A problem remains: how to program intermediate channels.

One solution to this problem is shown in Figure 2.

FIGURE 2 – FREQUENCY SYNTHESIS BY PRESCALING



A ÷ P is placed in series with the desired channel spacing (frequency) to give a new reference frequency: channel spacing/P.

Another solution is found by considering the defining equation (1) for f_{out} of Figure 1. From the equation it may be seen that only every P channel can be programmed simply, because N is always an integer. To obtain intermediate channels, P must be multiplied by an integer plus a fraction. This fraction would be of the form: A/P. If N is defined to be an integer number, Np, plus a fraction, A/P, N may be expressed as:

$$N = Np + A/P.$$

Substituting this expression for N in equation 1 gives:

$$f_{out} = (Np + A/P) \bullet P \bullet f_{ref} \quad (2)$$

or:

$$f_{out} = (Np\ P + A) \bullet f_{ref} \quad (3)$$

$$f_{out} = Np \bullet P \bullet f_{ref} + A \bullet f_{ref}. \quad (4)$$

Equation 4 shows that all channels can be obtained directly if N can take on fractional values. Since it is difficult to multiply by a fractional number, equation 4 must be synthesized by some other means.

Taking equation 3 and adding ±AP to the coefficient of f_{ref}, the equation becomes:

$$f_{out} = (Np \bullet P + A + A \bullet P - A \bullet P)\ f_{ref}. \quad (5)$$

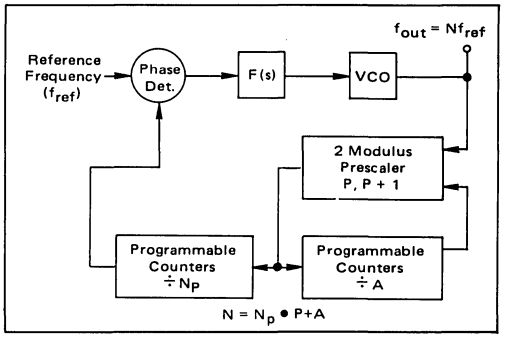
Collecting terms and factoring gives:

$$f_{out} = [(Np - A)\ P + A\ (P + 1)]\ f_{ref} \quad (6)$$

From equation 6 it becomes apparent that the fractional part of N can be synthesized by using a two-modulus counter (P and P + 1) and dividing by the upper modulus, A times, and the lower modulus (Np - A) times.

This equation (6) suggests the circuit configuration in Figure 3. The A counter shown must be the type that

FIGURE 3 – FREQUENCY SYNTHESIS BY TWO MODULUS PRESCALING



counts from the programmed state (A) to the enable state, and remains in this state until divide by Np is completed in the programmable counter.

In operation, the prescaler divides by P + 1, A times. For every P + 1 pulse into the prescaler, both the A counter and Np counter are decremented by 1. The prescaler divides by P + 1 until the A counter reaches the zero state. At the end of (P + 1) • A pulses, the state of the Np counter equals (Np - A). The modulus of the prescaler then changes to P. The variable modulus counter divides by P until the remaining count, (Np - A) in the Np counter, is decremented to zero. Finally, when this is completed, the A and Np counters are reset and the cycle repeats.

To further understand this prescaling technique, consider the case with P = 10. Equation 6 becomes:

$$f_{out} = (A + 10\ Np) \bullet f_{ref} \quad (7)$$

If Np consists of 2 decades of counters then:

$$Np = 10\ N_{P1} + N_{P0}$$

(N_{P1} is the most significant digit),

and equation 7 becomes:

FIGURE 4 – DIRECT PROGRAMMING UTILIZING TWO-MODULUS PRESCALER

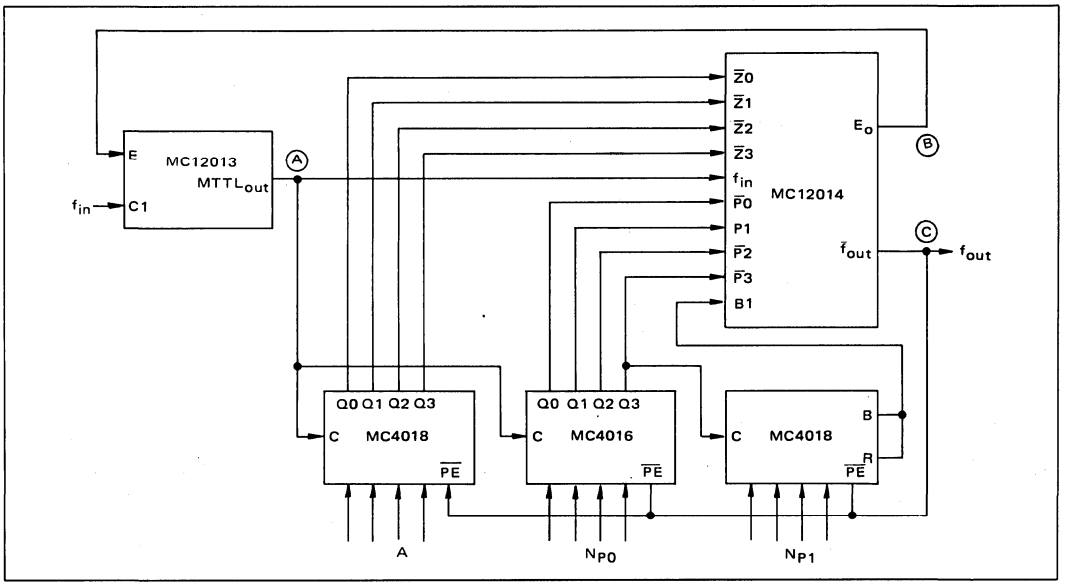


FIGURE 5 – WAVEFORMS FOR DIVIDE BY 43

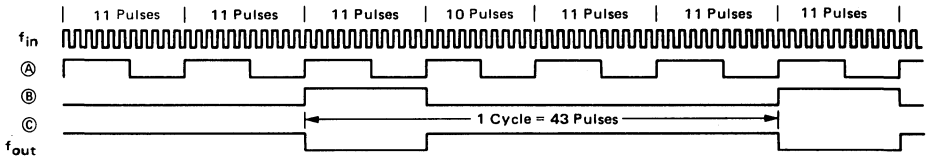


FIGURE 6 – WAVEFORMS FOR DIVIDE BY 42

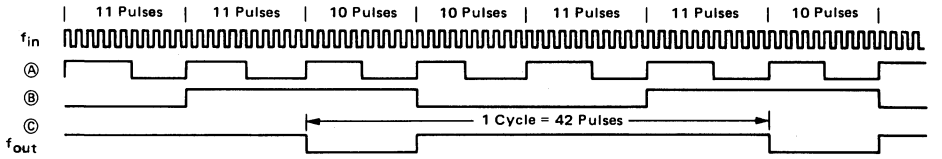
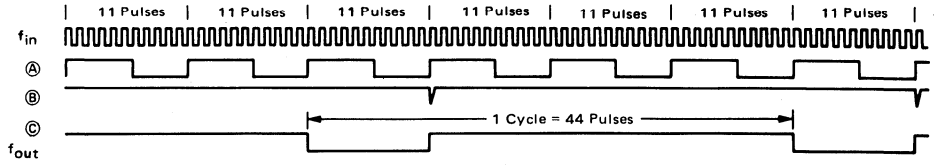


FIGURE 7 – WAVEFORMS FOR DIVIDE BY 44



$$f_{out} = (100\,N_{P1} + 10\,N_{P0} + A)\,f_{ref}.$$

To do variable modulus prescaling using the variable modulus prescalers (MC12009/11/13) and programmable divide by N counters (MC4016, MC4018) one additional part is required: the MC12014 (Counter Control Logic).

In variable modulus prescaling the MC12014 serves a dual purpose: it detects the terminal (zero) count of the A counter, to switch the modulus of the MC12013; and it extends the maximum operating frequency of the programmable counters to above 25 MHz. (See the MC12014 data sheet for a detailed description of the Counter Control Logic).

Figure 4 shows the method of interconnecting the MC12013, MC12014, and MC4016 (or MC4018) for variable modulus prescaling. To understand the operation of the circuit shown in Figure 4, consider division by 43. Division by 43 is done by programming $N_{P1} = 0$, $N_{P0} = 4$, and $A = 3$.

Waveforms for various points in the circuit are shown in Figure 5 for this division. From the waveforms it may be seen that the two-modulus prescaler starts in the divide by 11 mode, and the first input pulse causes point A to go high. This positive transition decrements the Np counter to 3, and counter A to 2.

After 11 pulses, point Ⓐ again goes high; the Np counter decrements to 2 and the A counter to 1. The "2" contained in the Np counter enables the inputs to the frequency extender portion of the MC12014. After 11 more pulses point Ⓐ goes high again.

With this position transition at Ⓐ, the output (f_{out}) of the MC12014 goes low, the Np counter goes to 1, and the A counter goes to 0. The zero state of the A counter is detected by the MC12014, causing point Ⓑ to go to 1 and changing the modulus of the MC12013 to 10 at the start of the cycle.

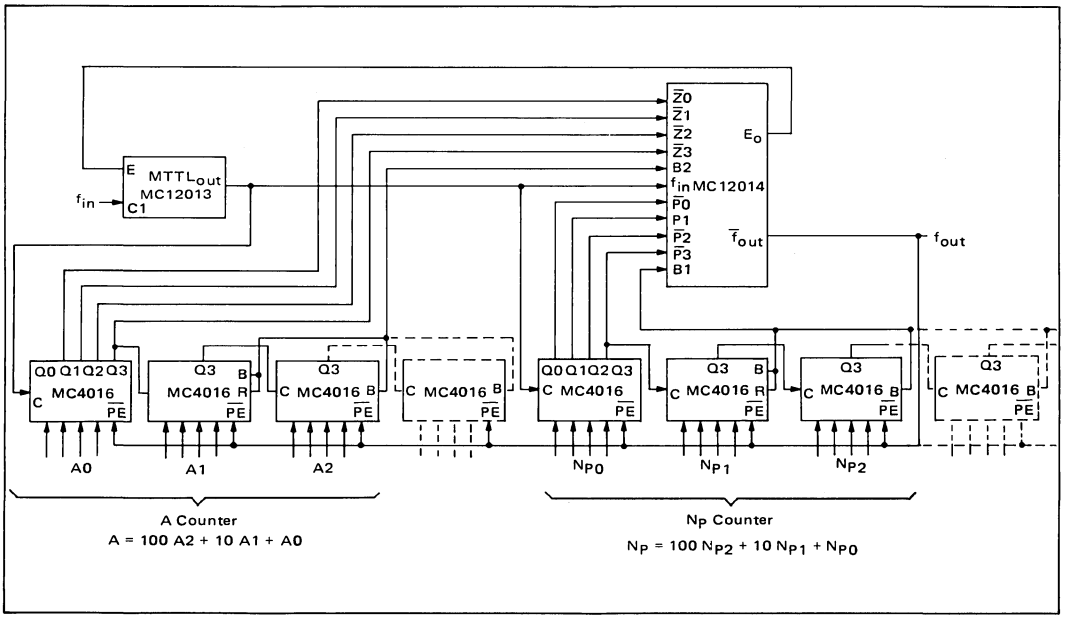
When f_{out} goes low, the programmable counters are reset to the programmed number. After 11 pulses (the enable went high after the start of the cycle and therefore doesn't change the modulus until the next cycle), point Ⓐ makes another positive transition. This positive transition causes f_{out} to return high, release the preset on the counter, and generates a pulse to clear the latch (return point Ⓑ to 0).

After 10 pulses the cycle begins again (point Ⓑ was high prior to point Ⓐ going high). The number of input pulses that have occured during this entire operation is: 11 + 11 + 11 + 10 = 43. Figures 6 and 7 show the waveforms for divide by 42 and divide by 44 respectively.

The variable modulus prescaling technique may be used in any application as long as the number in the Np counter is greater than or equal to the number in the A counter. Failure to observe this rule will result in erroneous results. (For example, for the system shown in Figure 4 if the number 45 is programmed, the circuit actually will divide by 44. This is not a serious restriction since Np is greater than A in most applications).

It is important to note that the A counter has been composed of only one counter for discussion only; where required, the A counter may be made as large as needed by cascading several programmable counters. Figure 8 shows the method of interconnecting counters. Operation is previously described. The number of stages in the A counter should not exceed the number of stages for the

FIGURE 8 – METHOD OF INTERCONNECTING COUNTERS



Np counters. As many counters as desired may be cascaded, as long as fan-in and fan-out rules for each part are observed.

The theory of "variable modulus prescaling" developed above, examined a case in which the upper modulus of the two-modulus prescaler was 1 greater than the lower modulus. However, the technique described is by no means limited to this one special case. There are applications in which it is desirable to use moduli other than P/(P + 1).

It can be shown that for a general case in which the moduli of the two-modulus prescaler are P and P + M, equation 6 becomes:

$$f_{out} = [(Np - A)\,P + A\,(P + M)] \bullet f_{ref}$$

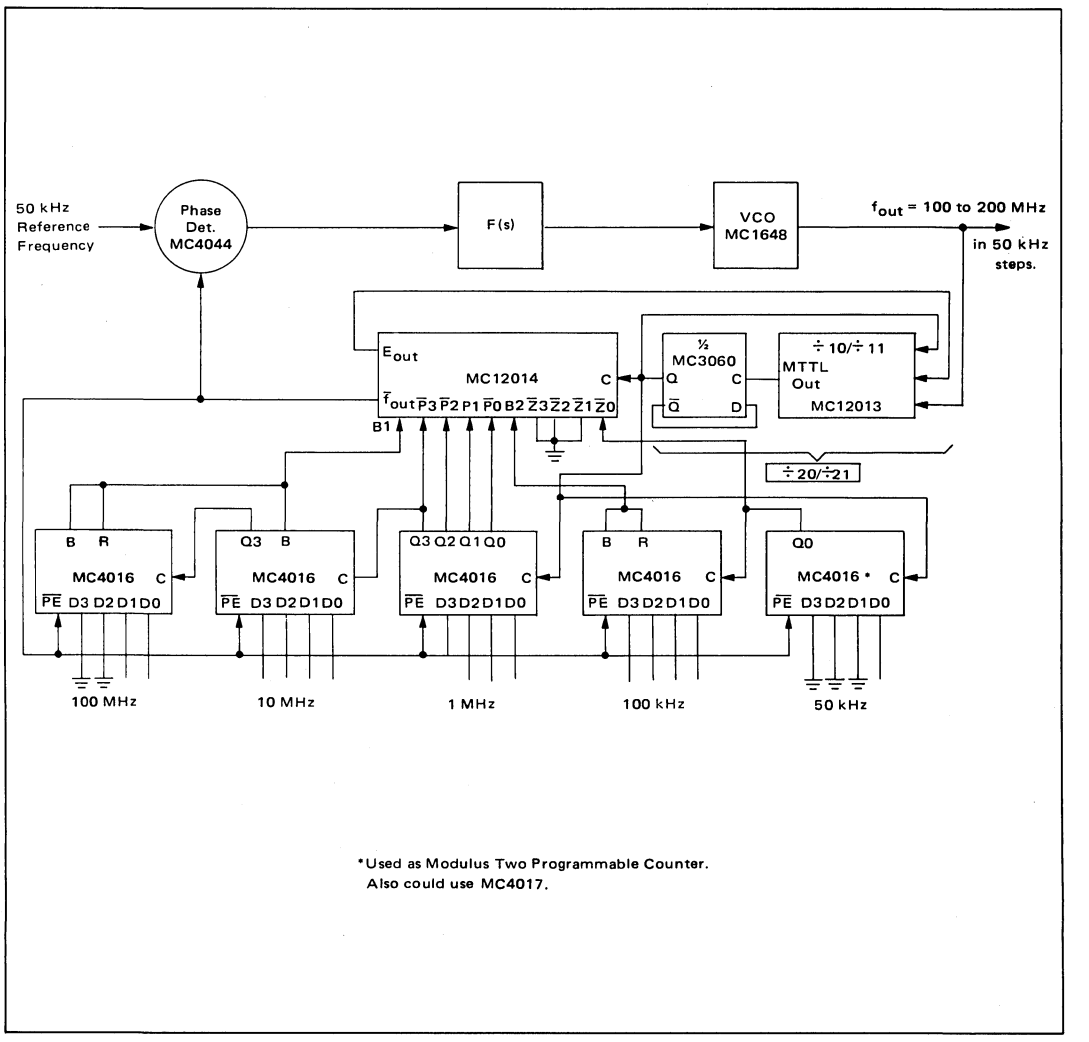
or

$$f_{out} = [Np \bullet P + M \bullet A] \bullet f_{ref}. \qquad (8)$$

From equation 8 it may be seen that the upper modulus of the two-modulus prescaler has no effect on the Np counter, and that the number programmed in the A counter is simply multiplied by M.

There is no one procedure which will always yield the best counter configuration for all possible applications. Each designer will develop his own special design for the counter portion of his PLL system.

FIGURE 9 – DIRECT PROGRAMMING 100-200 MHz SYNTHESIZER IN 50 kHz STEPS



*Used as Modulus Two Programmable Counter.
Also could use MC4017.

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Operation of the MC145159 PLL Frequency Synthesizer with Analog Phase Detector

INTRODUCTION

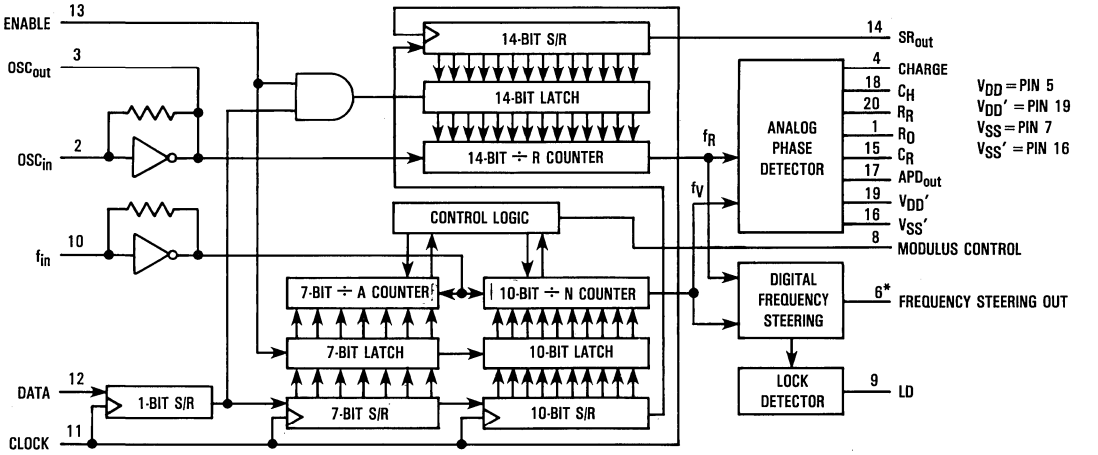
The MC145159 is a phase-locked loop frequency synthesizer with an analog, or more specifically a sample-and-hold, phase detector. The output of this phase detector (APD_{out}) is used as a fine error signal. The synthesizer also contains a digital frequency steering phase comparator for coarse adjustment of loop frequency, separate power supply pins for the analog phase detector, a lock detect output, and on-chip logic for control of a dual-modulus prescaler. (See Figure 1.)

Other features of the MC145159 are a 14-bit reference counter, as well as a 10-bit divide-by-N counter and a 7-bit divide-by-A counter. All three counters are programmed via a serial data stream which is compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs. The device also has on-chip circuitry to support an external crystal. OSC_{in} may also serve as an input for an externally-generated reference signal. This signal is typically ac coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels), dc coupling may be used.

With the features listed above, the MC145159 finds general purpose applications in such areas as 2-way radios, cellular radiotelephones, and avionics equipment.

As stated earlier, the MC145159 has a sample-and-hold phase detector. As opposed to standard digital phase comparators with fixed gain, the gain of the sample-and-hold phase comparator is programmable. Four external components, two resistors and two capacitors, help set the gain and drive levels of the phase detector. Higher gain is achievable with the MC145159 phase detector versus digital phase detectors.

Because a high degree of filtering compromises overall loop performance, phase detectors which provide an error signal that is as clean as possible prior to filtering are extremely advantageous. One obvious benefit of the sample-and-hold phase comparator is that its output is analog, and therefore already resembles the required control voltage necessary to drive the loop's voltage-controlled oscillator (VCO), thereby minimizing filtering requirements. Ideally, this control voltage is a perfectly clean signal with no undesired perturbations. Any of these disturbances cause unwanted modulation on the VCOs output signal. For high performance radio equipment, the sidebands resulting from this modulation must be very low. The analog output reduces VCO modulation sidebands and also allows for wider loop bandwidths than are normally possible with digital phase detector outputs.



*NOTE: Pin 6 is not and cannot be used as a digital phase detector output.

Figure 1. Logic Diagram

TRADITIONAL SAMPLE-AND-HOLD PHASE DETECTORS

Before examining the method by which the MC145159 performs a sample-and-hold function, the theory of operation of traditional sample-and-hold phase detectors will be reviewed.

The reference signal (divided-down OSC_{in} signal) and current source are used to establish the sawtooth voltage on the ramp capacitor, C_R. (See Figures 2 and 3.) C_R is charged by the current source and quickly discharged by a switch that is controlled by the reference signal. In this way, the period of the sawtooth voltage is equal to the period of the reference signal. The divided-down VCO signal is used to sample the sawtooth voltage by closing a sampling switch for a window of time and letting the hold capacitor, C_H, charge to the sampled voltage. Neglecting leakage current, the charge established on C_H at the end of the sample time remains constant until the next sample. If for some reason the VCO frequency begins to rise above the desired value, the phase of the sampling pulse falls back and sampling is done at a lower sawtooth voltage. This action, in effect, lowers the control voltage to slow down the VCO and keep the divided-down VCO frequency locked to the reference frequency. Likewise, if the VCO frequency falls below the desired value, the phase of the sampling pulse advances and sampling is done at a higher sawtooth voltage. This action raises the control voltage which speeds up the VCO to keep the divided-down VCO frequency locked to the reference frequency.

One serious side effect of this scheme is that an undesired ripple voltage occurs on C_H. This rippling is caused by the ramp waveform charging from level V_A to level V_B during the sample window. Upon opening of the sampling switch, C_H is charged to V_B and remains at V_B until the switch is closed again and voltage V_A is applied to the hold capacitor. Therefore, the hold capacitor is charged to V_B and discharged to V_A while in a locked condition. In effect, a ripple-free lock voltage cannot be established on C_H. The magnitude of this ripple is a function of the ramp charging slope, sample window time, and hold capacitor charge/discharge times.

To mask out the rippling effect, one solution is to follow C_H by a second sampling switch and hold capacitor combination along with the necessary control signals. However, this additional circuitry introduces more switching transients and consumes more chip and/or board space.

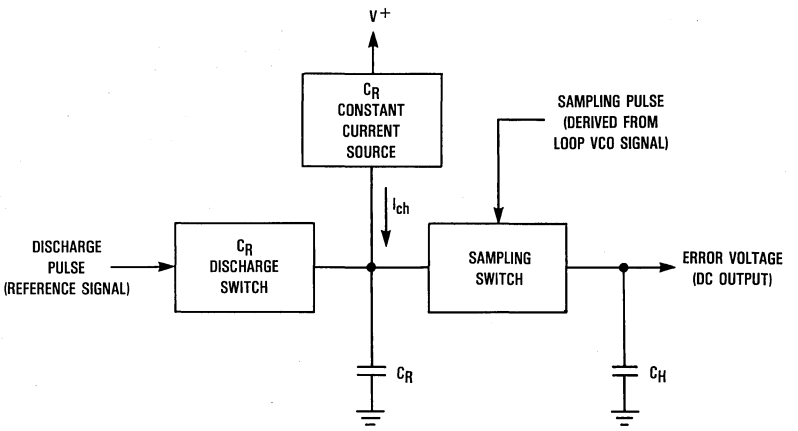


Figure 2. Traditional Sample-And-Hold Phase Detector Block Diagram

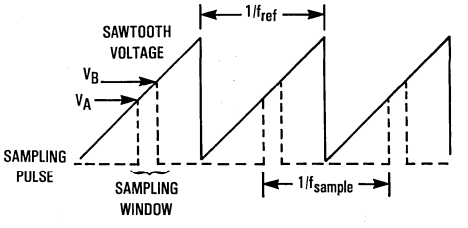


Figure 3. Traditional Sample-And-Hold Phase Detector Timing Diagram

OPERATION OF THE MC145159

THEORY

The MC145159 uses a new, patented design approach for sample-and-hold phase detectors called ramp clamping, which results in improved performance over the traditional approach. Ramp clamping minimizes the need for a second hold capacitor, and in most applications only one hold capacitor is needed. When the loop is in frequency lock, the rising edge of f_R (divided-down OSC_{in} signal) activates a constant current source to initiate charging of the ramp capacitor. (See Figures 4 and 5.) The slope of this ramp waveform is also known as the phase detector gain. The ramp voltage continues to build, at a rate determined by R_R, C_R, and V_{DD}', until the rising edge of f_V (divided-down VCO signal) terminates the charge signal, thereby establishing a constant voltage on C_R. After a predetermined delay (equal to two clock cycles of f_{in}) this ramp voltage is sampled onto the hold capacitor during a sample window lasting four periods of f_{in}. C_H is then isolated from C_R and, after a delay of two clock cycles of f_{in}, C_R is discharged. This cycle repeats every f_R period. The f_V edge relative to the f_R edge in time therefore determines how long the ramp charges before being clamped and sampled onto C_H. This establishes the hold voltage necessary to maintain loop lock. The voltage on C_H feeds an N-channel source follower, the output of which (APD_{out}) controls an external VCO.

When the loop is out of frequency lock, that is when f_R and f_V are not in a one-to-one relationship over a 2π window with respect to f_R, the Frequency Steering Output (FSO) becomes active. As a general rule, f_R and f_V must differ by 2% for the FSO to become active. However, as the reference frequency decreases, the frequency steering sensitivity increases. If the divided-down VCO frequency, f_V, is lower than the divided-down oscillator frequency, f_R, ($f_V < f_R$) then FSO pulses high. If $f_V > f_R$, then FSO pulses low. The FSO pulse width is approximately equal to the period of time between two f_V pulses if $f_V > f_R$, or two f_R pulses if $f_R > f_V$. FSOs repetition rate is equal to the difference frequency between f_R and f_V. When $f_V = f_R$ over a 2π window with respect to f_R, then the FSO remains in a high-impedance state and phase lock is maintained by the analog phase detector output. (See Figure 6.) By combining APD_{out} and FSO, the required low-noise VCO control voltage is provided by APD_{out} while the FSO provides a coarse error signal to achieve fast frequency lock.

The ramp clamp approach to phase detector design, which is implemented on the MC145159, offers significant advantages over the traditional method of sample-and-hold phase comparators. In traditional sample-and-hold detectors, ramp slewing during the sample window causes rippling on the hold capacitor. Therefore, a second hold capacitor and sampling switch may be needed. The ramp clamp technique however, alleviates the need for a second hold capacitor and all of its related circuitry. This becomes very significant in the production of monolithic integrated circuits due to the savings in chip area that result.

Another benefit of ramp clamping is that the ramp amplitude is not allowed to go beyond the value reached when sampling occurs. The traditional method permits the ramp capacitor to charge all the way up to the positive supply voltage value; in most cases well after sampling has occurred. This extends the ramp amplitude beyond that allowed with the ramp clamp approach. A lower ramp pulse results in less ripple in the output error signal caused by parasitic ramp feed-through. With ramp clamping, the ramp amplitude is limited to only that value necessary to keep the loop locked and, more importantly, it provides a constant voltage to the hold capacitor during the entire sample window.

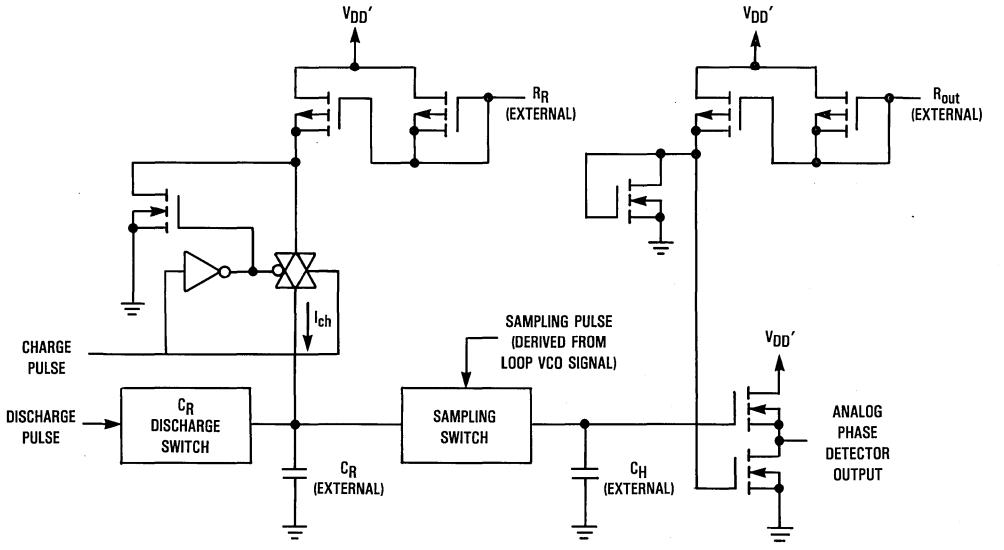


Figure 4. Analog Phase Detector Logic Detail

A word of caution exists for the analog phase detector power supply pins, V_{DD}' and V_{SS}'. These two pins are provided to help isolate the analog section from noise coming from the digital sections of this device and also noise from the surrounding circuitry. Ensure that V_{DD}' and V_{DD} are at the same voltage potential at all times. Likewise, V_{SS}' and V_{SS} must be at the same potential at all times. Otherwise, damage to the MC145159 may occur due to latch up.

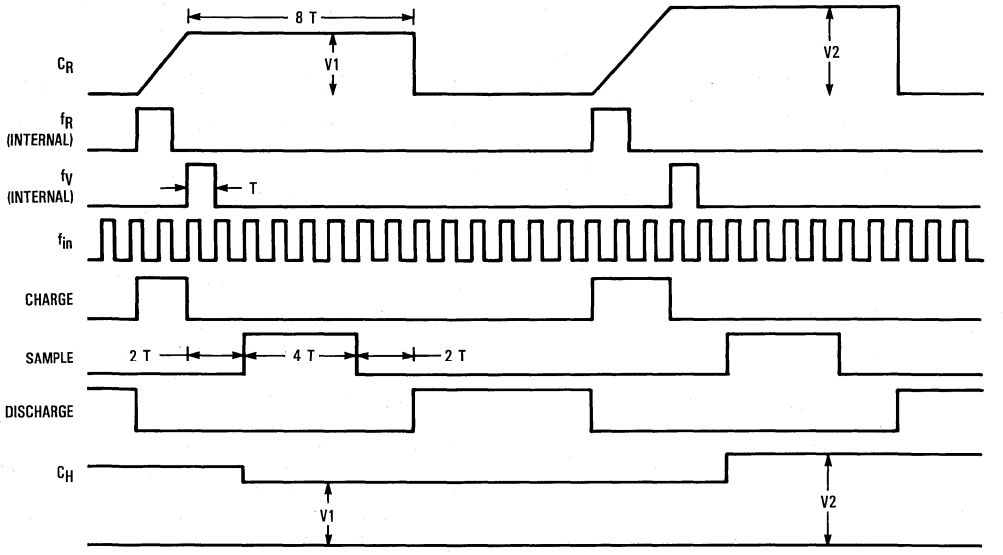
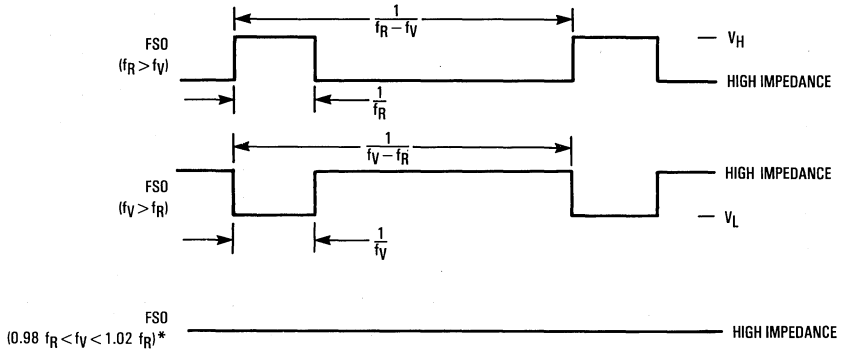


Figure 5. Analog Phase Detector Timing Diagram (N = 17)



NOTE: $f_R = \frac{f_{OSC}}{R}$, $f_V = \frac{f_{in}}{N}$. The R and N counter outputs are not externally available.

*The FSO sensitivity limits are not guarantees, but are design aids.

Figure 6. Frequency Steering Output Timing Diagram

PHASE DETECTOR GAIN

As stated earlier, the gain of the analog phase detector on the MC145159 is programmable. The gain is set by V_{DD}' and two external components; the ramp resistor, R_R, and the ramp capacitor, C_R. The user must therefore determine the optimal value of gain for his or her system.

To select the optimal gain for the phase detector, let us assume a PLL system with a reference frequency of 10 kHz. (See Figure 7a.) With this frequency going into the phase detector, consecutive f_R pulses occur 100 μs apart. Assuming that the Frequency Steering Out pin has already pulled the system into frequency lock and turned off, the Analog Phase Detector Output is in complete control. Therefore, the rising edges of f_R and f_V can be nearly 100 μs apart. Because f_R initiates the ramp waveform and f_V terminates the charging cycle, the ramp should be at most 100 μs, or 2π radians wide. Moreover, the ramp should be capable of charging from V_{SS}' to V_{DD}' during this time. The design equation for phase detector gain given in the data sheet is stated as:

$$K_\phi = \frac{I_{charge}}{2\pi\ f_R\ C_R} \quad [V/rad]$$

Substituting in for K_ϕ and f_R and selecting a value for C_R, one can solve for I_{charge}. From I_{charge}, the value of ramp resistance, R_R, is taken from Figure 8.

In this example, the gain of the phase detector is $V_{DD}'/2\pi$ [V/rad]. Larger values of gain can certainly be used. In fact, higher gain results in faster lock times. (See Figure 7b.) There is, however, an upper limit to the amount of gain selected. Higher gain is achieved by increasing V_{DD}' or reducing R_R or C_R (or some combination thereof). Increasing phase detector gain by reducing the size of the ramp capacitor leads to increased noise induced into the ramp, and consequently, hold capacitors.

On the other hand, too little gain results in the ramp capacitor taking slightly longer to reach the required error voltage level,

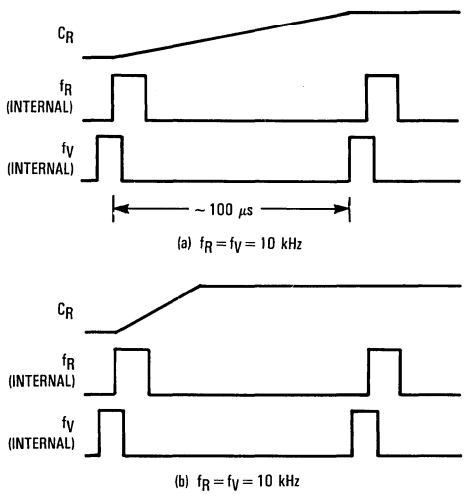


Figure 7. Determining the Gain of the Analog Phase Detector

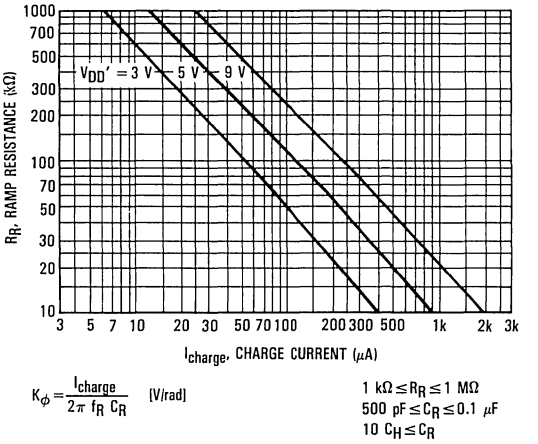


Figure 8. Charge Current versus Ramp Resistance

thereby widening the ramp waveform. This increased area under the curve represents more energy being transferred to the hold capacitor. The result is an increased potential to modulate the control voltage, yielding higher sidebands on the VCO output. Therefore, each system must be carefully analyzed and optimized for the gain/noise tradeoff.

The analog phase detector of the MC145159 can track changes in its input over a 2π range with respect to f_R. The digital frequency steering portion of the device produces error signals over a wide range of input frequency differences.

OUTPUT BIAS CURRENT RESISTOR

Included on the MC145159 is a pin dedicated for use with an external component, called the output bias current resistor. A resistor connected from this pin (R_O) to V_{SS}' biases the output N-channel transistor, thereby setting a current sink on the analog phase detector output. With larger values of output resistance, the analog output bias current decreases (See Figure 9.)

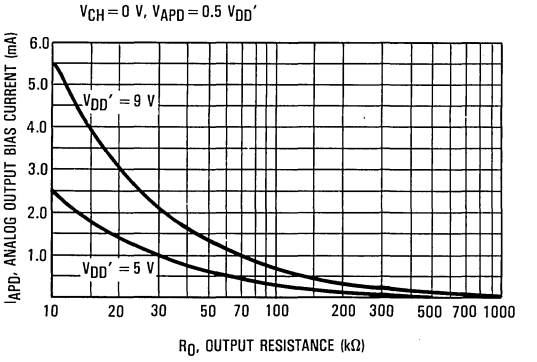


Figure 9. APD_{out} Bias Current versus Output Resistance

METHOD OF PROGRAMMING THE COUNTERS

The MC145159 contains three fully-programmable counters. The R, N, and A counters are programmed by a serial data bit stream. (See Figure 10.) Perusing the logic diagram of the device gives insight as to how the counters are loaded with data. (See Figure 1.)

First, the desired values for R, N, and A must be converted to binary form with the proper amount of bit positions. Note that the R counter is 14 bits long, the N counter 10 bits long, and the A counter 7 bits long. To load the data, the Enable pin must be taken low to isolate the counters from changes that occur in the shift registers. With Enable low, data is then loaded into the shift registers on the rising edge of the clock input. Care must be taken to ensure that Data, Clock, and Enable voltage levels and rise, fall, setup, hold, and recovery times are not violated. The divide-by-R word is loaded first with its most-significant bit as the first bit entered. The divide-by-N word follows immediately, again with its most-significant bit as the first bit entered. Next is word A, similarly with its most-significant bit entering first. The last bit of the string is the control bit. A logic one for the control bit allows all the counters to be loaded with shift register information when Enable is taken high. A logic zero entered as the control bit inhibits a reference counter latch load. Therefore, only the N and A counters are loaded when Enable is taken high.

Finally, after all the data is properly loaded into the shift registers and the control bit is at the desired logic state, Enable is taken high to program the counters. After satisfying the minimum input pulse width for Enable, that pin must then be taken low to isolate the counters from outside disturbances.

For example, suppose system requirements dictate that the R, N, and A counters be programmed with 40, 200, and 72, respectively. The steps to load the counters are outlined below.

R = 40 (14 bits)

0 0 0 0 0 0 0 0 1 0 1 0 0 0
MSB LSB

N = 200 (10 bits)

0 0 1 1 0 0 1 0 0 0
MSB LSB

A = 72 (7 bits)

1 0 0 1 0 0 0
MSB LSB

Action	Comment
1. Take Enable low ($<0.3\ V_{DD}$)	Isolate the counters
2. Shift in eight 0s	Start loading R word
3. Shift in one 1	
4. Shift in one 0	
5. Shift in one 1	
6. Shift in five 0s	R word entered; start loading N word
7. Shift in two 1s	
8. Shift in two 0s	
9. Shift in one 1	
10. Shift in three 0s	N word entered
11. Shift in one 1	Start loading A word
12. Shift in two 0s	
13. Shift in one 1	
14. Shift in three 0s	A word entered
15. Shift in one 1	Control bit high
16. Take Enable high ($>0.7\ V_{DD}$)	Load the three counters
17. Take Enable low ($<0.3\ V_{DD}$)	Isolate the counters

Now that the counters are loaded with the correct information and the system is working properly, changing the output frequency is desired. New values of N and A are chosen while keeping R the same. (R is only used in this case to set up the system resolution.) The same method can be used to program the N and A counters while simply ignoring the R counter. Take Enable low, shift in the appropriate binary data for N and A, shift in a control bit of logic zero to isolate the R counter form the Enable line, and pulse high the Enable input.

For example, suppose the new values for N and A are 178 and 13, respectively. The steps to load the counters are outlined below.

N = 178 (10 bits)

0 0 1 0 1 1 0 0 1 0
MSB LSB

A = 13 (7 bits)

0 0 0 1 1 0 1
MSB LSB

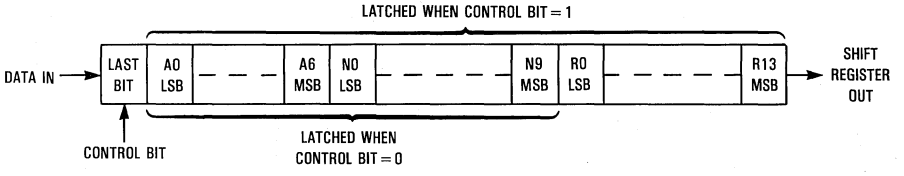


Figure 10. Data Entry Format

Action	Comment
1. Take Enable low	Isolate the counters
2. Shift in two 0s	Start loading N word
3. Shift in one 1	
4. Shift in one 0	
5. Shift in two 1s	
6. Shift in two 0s	
7. Shift in one 1	
8. Shift in four 0s	N word entered; start loading A word
9. Shift in two 1s	
10. Shift in one 0	
11. Shift in one 1	A word entered
12. Shift in one 0	Control bit low
13. Take Enable high	Load the two counters
14. Take Enable low	Isolate the counters

As is evident, the two prior routines are serial in nature. A microprocessor is therefore best suited to program the counters. Also, note that the counter outputs are not available on the MC145159 for checking correct counter operation. However, a shift register output, SR_{out}, is available. (See Figure 1.) Therefore, the same microprocessor that programs the counters can also be used to verify the contents of the shift registers to ensure that the correct data has been loaded. Enable must be held low while verifying shift register contents to avoid affecting the counters.

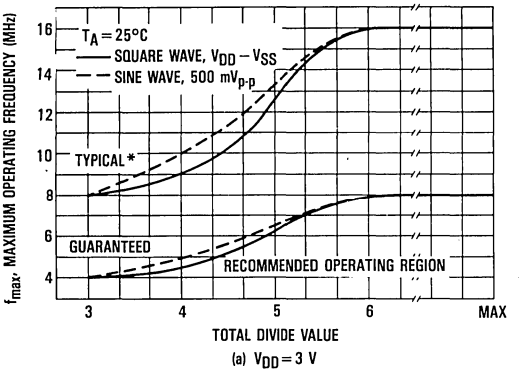
Although the MC145159 has on-chip logic for control of an external dual modulus prescaler, the device is capable of performing in a single modulus mode simply by leaving the modulus control output unconnected. In this case, the 10-bit divide-by-N counter performs the loop divide-by-N function. The A counter must still be loaded with data, but that data is a don't care. However, loading the A counter with all 0s is strongly recommended. In that way, the modulus control output is stuck high and cannot cause any possible interference by switching periodically.

f_{in}, OSC_{in} LIMITS

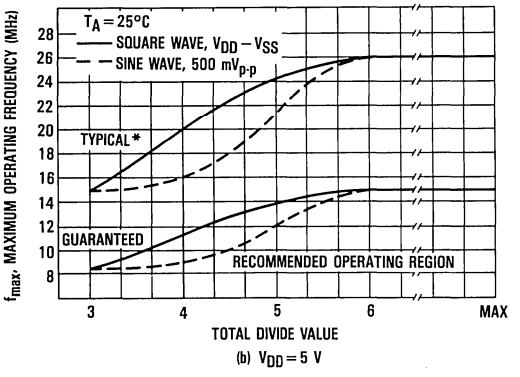
Although not stated on the data sheet, the f_{in} and OSC_{in} limits for the MC145159 are about the same as the rest of the silicon-gate MC1451XX family of frequency synthesizers. (See Figures 11 and 12.) One limit is 15 MHz for a supply voltage of 5 V and a divide value of six or greater for the N and R counters. Refer to the graphs for frequency limits of the MC145159 counters at other supply voltages.

The analog phase detector component values play a small role in determining the input frequency limits at the input to the phase detector. For high reference frequencies, a large value of I_{charge} is most likely required. Make certain that component values are in specified ranges. For best results, the following limits are recommended. (Low-leakage polystyrene or Mylar capacitors are recommended for C_R and C_H.)

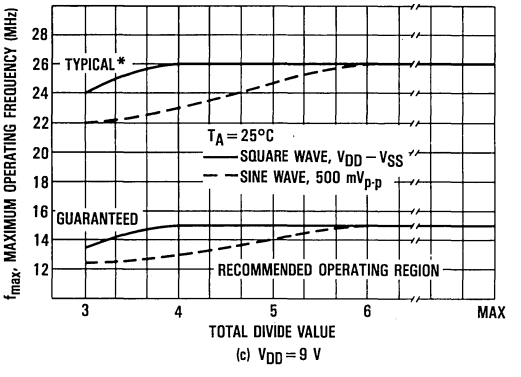
$$1\ k\Omega \le R_R \le 1\ M\Omega$$
$$500\ pF \le C_R \le 0.1\ \mu F$$
$$10\ C_H \le C_R$$
$$10\ k\Omega \le R_O \le 1\ M\Omega$$



(a) $V_{DD} = 3$ V



(b) $V_{DD} = 5$ V



(c) $V_{DD} = 9$ V

*Data labelled "Typical" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

Figure 11. OSC_{in} and f_{in} Maximum Frequency versus Total Divide Value ($R_{min} = 3$, $N_{min} = 16$)

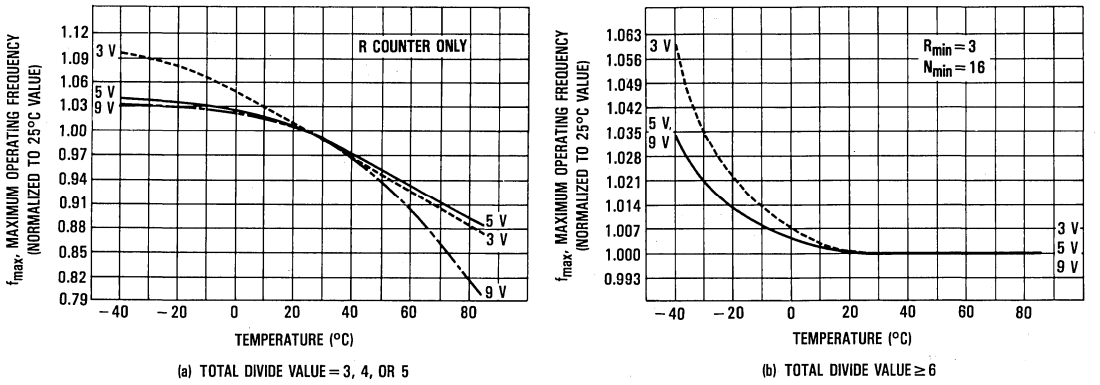


Figure 12. OSC_{in} and f_{in} Maximum Frequency versus Temperature for Sine and Square Wave Inputs

DUAL-MODULUS PRESCALING CONSTRAINTS

The MC145159 contains all the necessary logic for control of an external dual-modulus prescaler. Dual-modulus prescaling is a solution to some of the shortcomings associated with single-modulus prescaling. Inherent in the design of synthesizers using single-modulus prescaling is the fact that the value of the reference frequency into the phase detector is multiplied by the prescale value P, as well as by the counter value, N. (See Figure 13.) This results in a loss of system resolution because any unitary change of N results in the output frequency of the VCO changing by the reference frequency times P, which may be undesired.

Dual-modulus prescaling is a solution to this problem. It allows VCO step sizes equal to the value of the phase detector reference frequency to be obtained. This technique utilizes an additional A counter and a special prescaler which divides by any one of two values, depending upon the state of its control line. (See Figure 14.) In dual-modulus prescaling, the lower speed counters are uniquely configured. Special control logic is necessary to select the divide value, P or P + 1, in the prescaler for the required amount of time.

The modulus control signal is low at the beginning of a count cycle, enabling the prescaler to divide by P + 1, until the A counter has counted down to zero. At this time, modulus control goes high, enabling the prescaler to divide by P, until the N counter counts down the rest of the way to zero; N minus A additional counts.

$$N_{tot} = (P+1)A + P(N-A)$$

$$= NP + A$$

Modulus Control is then set back low, the counters preset to their respective programmed values, and the sequence is repeated.

This provides for a total programmable divide value of (N times P) + A. To have a range of total divide values in sequence, the A counter is programmed from zero through P − 1 for a particular value N in the N counter. N is then incremented by 1 and the A counter is sequenced from zero to P − 1 again.

Certain constraints apply when using dual-modulus prescaling: 1) N is greater than or equal to A always applies; 2) the value of P must be large enough so that the maximum frequency of the VCO divided by P must not exceed the frequency capability of the N and A counters; also, 3) P times the period of the maximum VCO frequency must be greater than the sum of the prop delay through the dual-modulus prescaler plus the prescaler setup or release time relative to its control signal plus the propagation delay of frequency in (f_{in}) to Modulus Control.

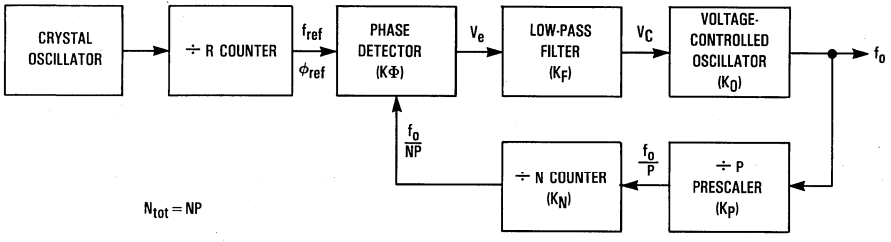


Figure 13. Single-Modulus Prescaling

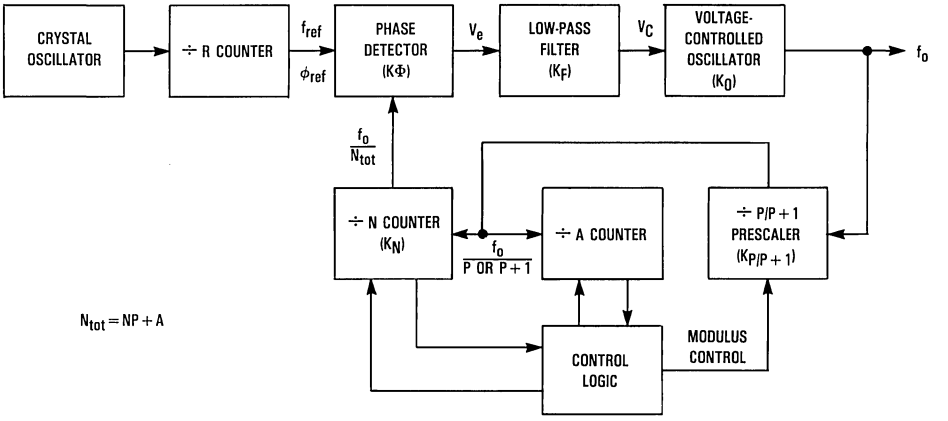


Figure 14. Dual-Modulus Prescaling

FREQUENCY SYNTHESIZER EXAMPLE

Suppose the MC145159 is to be used in a system which operates from 118.000 to 135.975 MHz in 25 kHz steps, i.e., aircraft communication transceivers. (See Figure 15.) A prescaler is needed to divide down the maximum VCO output frequency to a frequency that the MC145159 can handle (15 MHz maximum at $V_{DD} = 5$ V). A minimum prescale value of 10 is required. However, if a divide-by-10 single-modulus prescaler is used, the reference frequency would have to be adjusted to 2.5 kHz in order to maintain the 25 kHz step size. Therefore, dual-modulus prescaling is desired and the MC12016 divide-by-40/41 prescaler is selected due to an input frequency capability of 225 MHz and the ability to divide down the VCO frequency to well under 15 MHz.

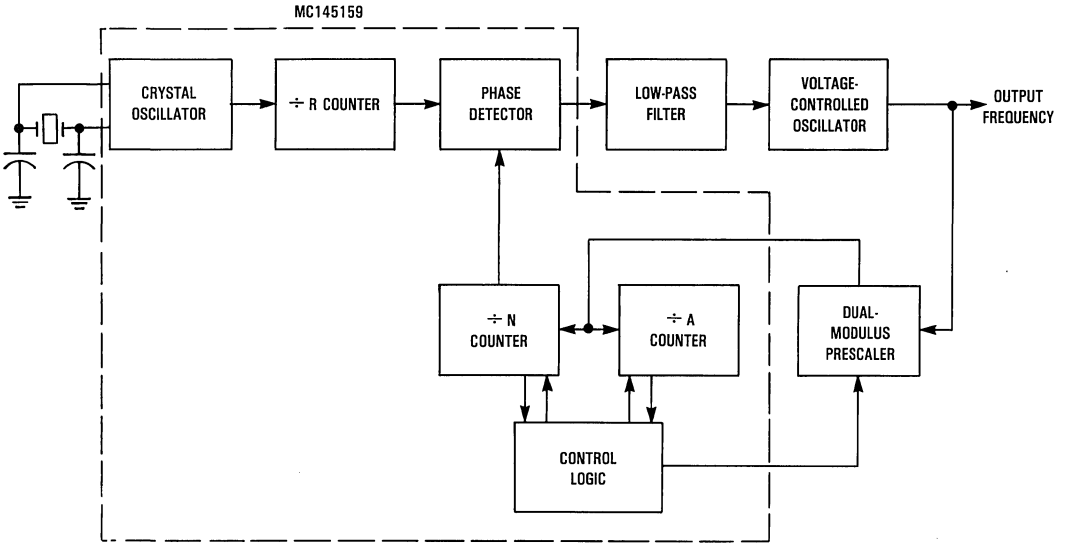


Figure 15. Typical System Application

With a reference frequency of 25 kHz, the N and A counters must be loaded with the proper values to achieve 118 to 135.975 MHz at the loop output. For example, at f_{max}:

$$N_{tot} = \frac{135.975\ MHz}{25\ kHz}$$

$$N_{tot} = 5{,}439$$

To arrive at programming values for N and A, use:

$$N_{tot} = NP + A$$

Substituting in, and for now, letting A = 0:

$$5{,}439 = N(40)$$

$$N = 135.975$$

Therefore, N = 135 is used. Now, A must be determined.

$$A = N_{tot} - NP$$

$$A = 5{,}439 - (135)(40)$$

$$A = 39$$

Similarly, at f_{min}:

$$N_{tot} = \frac{118\ MHz}{25\ kHz}$$

$$N_{tot} = 4{,}720$$

$$N_{tot} = NP + A$$

$$N = \frac{4{,}720}{40}$$

$$N = 118$$

Therefore N = 118 and A = 0.

A table can be built up showing the values of N and A and their corresponding loop output frequencies.

Table 1. Output Frequencies and Their Corresponding N and A Counter Values (f_{ref} = 25 kHz, P = 40)

Output Frequency (MHz)	N_{tot}	N	A
118.000	4,720	118	0
118.025	4,721	118	1
118.050	4,722	118	2
.	.	.	.
.	.	.	.
.	.	.	.
118.975	4,759	118	39*
119.000	4,760	119	0
119.025	4,761	119	1
.	.	.	.
.	.	.	.
.	.	.	.
135.950	5,438	135	38
135.975	5,439	135	39

*Note that because P = 40, the maximum value of A = 39.

In the example above, a 25 kHz reference frequency is used. This frequency is generally established at the reference input of the phase detector by an on-chip oscillator used with an external crystal. The R counter is programmed to divide down the crystal frequency to the required reference frequency, in this case 25 kHz. With the MC145159, the divide-by-R range is from 3 to 16,383. Therefore, the designer has many options in choosing the crystal frequency. One example is a 3.2 MHz crystal with a divide-by-R of 128 to yield a reference frequency of 25 kHz. Obviously, many other combinations are possible.

Now, a suitable gain must be chosen for the phase detector. With a 25 kHz reference frequency, successive f_R pulses occur 40 μs apart. For the first attempt, the ramp capacitor is chosen to charge up to V_{DD}' in one-eighth the time, or 5 μs. (The slope with which the ramp capacitor charges is the phase detector gain.) Therefore, the selected gain is 6.4 V/rad with a 5 V supply. Larger values of gain can be selected to speed up lock times; however, induced noise in the loop may be increased.

Values of phase detector components can now be determined using the equation for phase detector gain.

$$K_\phi = \frac{I_{charge}}{2\pi\ f_R\ C_R} \quad [V/rad]$$

letting C_R = 500 pF and solving for I_{charge} yields

$$I_{charge} = 500\ \mu A$$

Figure 8 shows that the graph for V_{DD} = 5 V crosses the 500 μA axis at R_R = 20 kΩ. With C_R = 500 pF, C_H is chosen to be 50 pF. Slightly larger values for hold capacitance may be required for noise considerations. Finally, the output resistor (R_O) can be any value between 10 kΩ and 1 MΩ, as long as the analog output bias current is compatible with the employed low-pass filter. (See Figure 9.)

A major concern in designs with the MC145159 is combining the analog phase detector output with the Frequency Steering Output properly. Three possible methods are shown in Figure 16. It should be noted that these three connection schemes are theoretical only and have not been tested in the lab. Methods of connecting these two outputs will be the subject of a forthcoming application note.

The low-pass filter and voltage-controlled oscillator must also be planned out carefully for optimal loop performance. For the MC145159, the loop filter can be combined with the connection scheme for the phase detector outputs. Further filtering may be necessary if dictated by the system requirements. In the previous example of aircraft communication transceivers, a VCO must be chosen for the loop. The Motorola MC1648 is a good choice due to an output frequency capability above the f_{max} constraint of 135.975 MHz. Consult the MC1648 data sheet for VCO design considerations.

With the loop all in place and powered up, the counters must be programmed for the synthesizer to tune to the desired channel. From Table 1, suppose 135.975 MHz is the VCO output frequency desired. The N counter should be programmed to 135 and the A counter to 39. Also, with a 3.2 MHz crystal and 25 kHz channel spacing, the R counter should be programmed to 128.

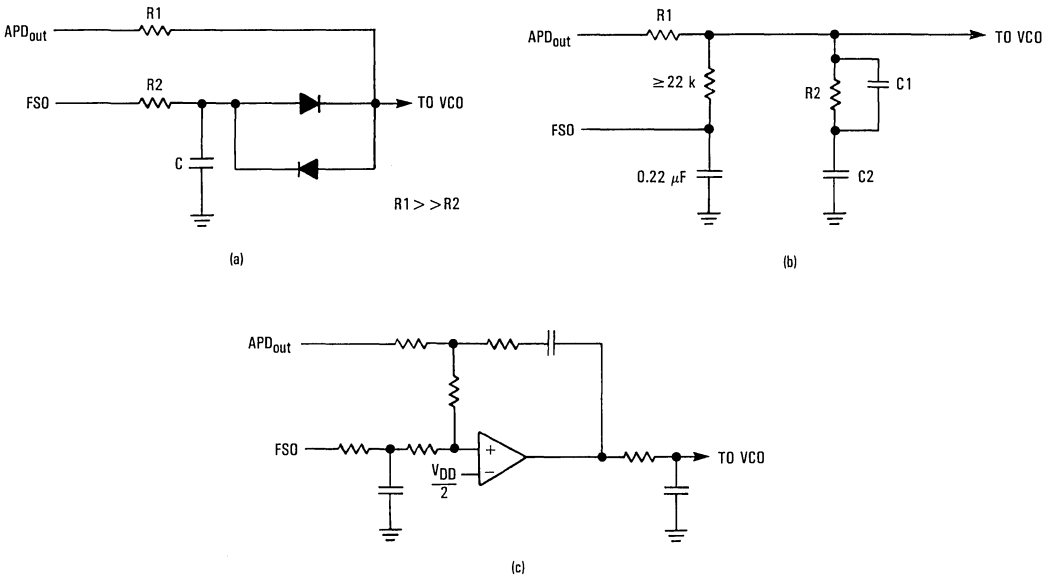


Figure 16. Possible Methods for Combining Analog Phase Detector Output and Frequency Steering Output

CONCLUSION

This application note discussed the open-loop characteristics of the MC145159 PLL frequency synthesizer with analog phase detector. The MC145159 uses an improved method over the traditional sample-and-hold technique while providing an alternative to digital phase detectors in frequency synthesis applications. The Frequency Steering Output together with the Analog Phase Detector Output combine to produce an error signal without the introduction of excessive noise. In fact, this phase detector scheme minimizes filtering requirements, reduces VCO modulation sidebands, and allows for wider loop bandwidths than are normally possible with digital phase detector outputs.

An additional application note is planned to cover the closed-loop application of the MC145159, especially the methods for combining the two phase detector outputs.

REFERENCES AND ACKNOWLEDGMENTS

1. *CMOS/NMOS Special Functions Data*, Motorola Inc.
2. Manassewitsch, Vadim, *Frequency Synthesizers—Theory and Design*, Wiley and Sons, 1980, pp. 401-407.
3. Sample and Hold Phase Detectors/Comparators, Motorola internal memo, signed by John Hatchett and Roy Jones, 10/3/79.
4. Sample and Hold Phase Detector Timing, Motorola internal memo, Andy Olesin and John Hatchett, 10/23/79.

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

VHF Narrowband FM Receiver Design Using the MC3362 and the MC3363 Dual Conversion Receivers

Prepared by: Bipolar Analog Applications

Motorola has developed a series of low power narrowband FM dual conversion receivers in monolithic silicon integrated circuits. The MC3362 and the MC3363 are manufactured in Motorola's MOSAIC process technology. This process develops NPN transistors with f_T = 4 + GHz, which allows the MC3362 and the MC3363 to have excellent very high frequency (VHF) operation with low power drain. They are ideal for application in cordless phones, narrowband voice and data receivers, CB and amateur band radios, radio frequency (RF) security devices and other applications through 200 MHz.

Features of the MC3362/3 Receiver ICs:

- Broadband RF input frequency capability (to 200 MHz using internal oscillator, over 450 MHz using external oscillator)
- Single supply operation from V_{CC} = 2 to 7 Vdc
- Low power consumption (I_{CC} = 3 mA typical at V_{CC} = 2 Vdc)
- Internally biased NPN RF transistor amplifier (MC3363)
- Complete dual conversion circuitry — first mixer and oscillator included
- First local oscillator (LO) includes buffered output and varactor diode to allow phase locked-loop (PLL) frequency synthesis for multichannel operation.
- Buffered second local oscillator output available for PLL reference input (MC3362)
- Multistage limiter and quadrature detection circuitry included
- RSSI (Received Signal Strength Indicator) with Carrier Detect logic included
- Built-in data slicing comparator detects zero crossings of FSK data transmission
- Inverting operational amplifier included for audio muting or active filtering (MC3363)

SCOPE

This application note contains functional descriptions and applications information pertaining to the various functional blocks of the MC3362/3 receiver circuits. Four receiver application circuits are shown. A single channel receiver and a 10 channel frequency synthesized receiver designed for the 49 MHz cordless telephone band are shown. A 256 channel "2 Meter" (144–148 MHz) amateur band receiver is also shown, including an appropriate PLL frequency synthesizer design to control the receiver's local oscillator. Finally, a low cost application featuring the MC3362 as a single chip manually tunable 162 MHz weatherband receiver is shown. A directory of external component manufacturers is included as an appendix.

COMPARISON OF THE MC3362 AND THE MC3363

Figures 1A and 1B show the system block diagrams of MC3362 and MC3363, respectively. The MC3362 and the MC3363 are made from the same die, but a final metal mask difference allows different features to be made available on each. Data pertaining to the common functional blocks are identical on both circuits.

The MC3363 is a complete VHF dual conversion FM receiver including RF amplifier, two mixers and oscillators, limiting IF amplifier and quadrature detection circuitry, received signal strength indicator (RSSI) circuitry, squelch circuitry and a data shaping comparator for detecting FM frequency shift keyed (FSK) data transmissions. Receivers using the MC3363 alone can achieve better than 0.3 μV input sensitivity for 12 dB SINAD, from a 50 Ω source. The MC3363 comes in a 28-lead plastic wide SOIC package only.

The MC3362 is optimized for cordless telephone applications and as such does not contain the RF preamplifier or squelch circuitry. In addition, the second local oscillator contains a buffered output so that it can serve as the system frequency reference in applications where a 10.240 MHz or 10.245 MHz reference is needed. In general, the MC3362 can be substituted for the MC3363 where:

- A receiver with sensitivity of 0.7 μV at the input for 12 dB SINAD is adequate.
- An external RF preamplifier with AGC is desired (such as MOSFET's 3N211 and MPF211).
- Receiver squelch is not needed.
- Surface mount technology cannot be used. The MC3362 is available in two 24-lead plastic packages (DIP and wide SOIC surface mount).

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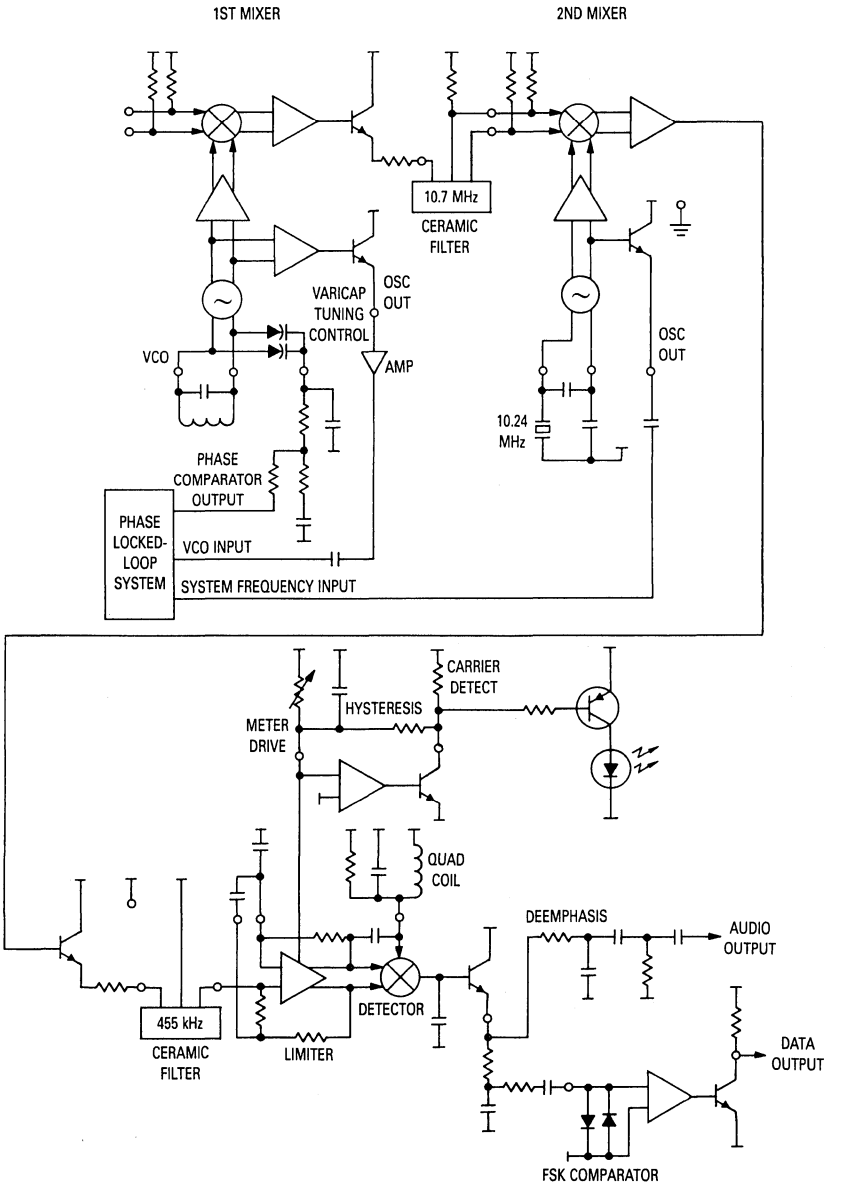


Figure 1A. MC3362 Internal Block Diagram

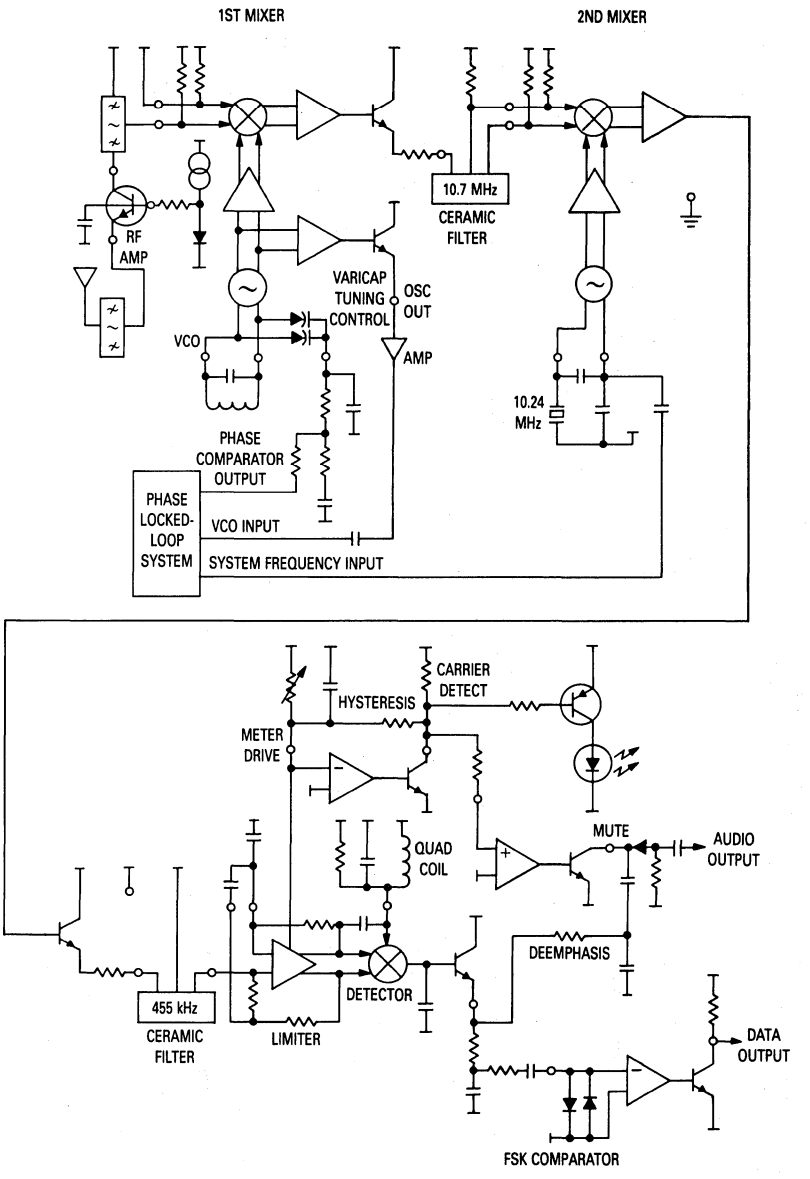


Figure 1B. MC3363 Internal Block Diagram

FEDERAL REGULATIONS, RECOMMENDED STANDARDS

Radios built for certain VHF and UHF bands may qualify under the FCC Code of Federal Regulations Title 47, Part 15, for use by unlicensed operators. It is important to know the federal regulations concerning a particular frequency channel or band of channels before a receiver or transmitter circuit is designed. **Contact the FCC/Government Printing Office to order a copy of the Code of Federal Regulations, Title 47, Parts 0–20 which contains Part 15, before designing a radio receiver or transmitter for unlicensed utility applications.**

Professional (landmobile) radios come under another part (Part 90) of the Title 47 code. There are a set of standards, published by the Electronic Industries Association, which dictate recommended operating specifications for two way communication equipment. These standards provide useful information about radio performance, terminology and measurement techniques and are useful even if professional radios are not a designer's primary goal. Contact the EIA at (202) 457-4900 to order the standards listed below. The FCC/GPO can be reached at (202) 275-2054 or (213) 894-5841. The pertinent documents are:

Number	Description	Parts Referenced
FCC Title 47, Part 15	Code of Federal Regulations	Radio Frequency Devices
FCC Title 47, Part 90	Code of Federal Regulations	Landmobile Radios
RS-204-C	EIA Recommended Standard	FM/PM Receiver Standards
EIA-152-B	EIA Recommended Standard	FM/PM Transmitter Standards
EIA-316-B	EIA Recommended Standard	Test Conditions, Radio Standards

REFERENCE LITERATURE

The following Motorola literature may be useful when designing with the MC3362/3 receivers:

Number	Description	Parts Referenced
DL128, Rev. 2	Linear and Interface Device Data	MC3362, MC3363, MC34119, MC2831A, MC2833, MC13060, MC33171
DL130	CMOS/NMOS Special Functions Data	MC1451XX CMOS PLL's
DL122	MECL Device Data	MC12XXX ECL Prescalers
DL126	Small Signal Transistor Data	3N211, MPF211

COMPANION DEVICES

- The MC2831A and the MC2833 low power FM transmitter ICs provide all essential functions for cordless telephone and general transmitter and oscillator applications through 60 MHz (MC2831A) and 200 MHz (MC2833, using internal very high frequency [VHF] transistors as frequency multipliers).
- The MC34119 low power audio amplifier with differential outputs provides efficient power transfer and eliminates the need for the typical large audio coupling capacitor.
- The MC13060 Mini-Watt audio amplifier (for higher powered audio output).
- The MC33171 low power single supply operational amplifier for use as an RSSI buffer or active integrator.
- The MC14516X series of dual PLL frequency synthesizers for development of 10 channel cordless telephone band transceivers.
- The MC12XXX series of ECL prescalers and
- MC1451XX series of CMOS Frequency Synthesizers for development of VHF "high band" radios to 200 MHz
- The MC145442/3 single chip 300 baud modems which allow audio frequency shift keyed (AFSK) RF modem design for very reliable data transmission.
- The 3N211 and MPF211 dual gate MOSFET's for MC3362 RF preamplification with AGC capability.

BLOCK DESCRIPTION

RF Amplifier (MC3363 only)

The MC3363 contains an internal NPN bipolar RF amplifier transistor. The base of the transistor is biased internally to approximately 0.8 Vdc, which simplifies common-emitter amplifier design. Grounding the emitter yields an emitter current I_E = 1.5 mA and voltage gain A_V = 20 dB with a collector load R_L = 1 kΩ.

Emitter degeneration resistors can be added to lower current drain, with R_E decoupling used to preserve the gain. With the emitter grounded the input at Pin 2 looks like 180 Ω in parallel with 20 pF at 50 MHz. The noise figure at 50 MHz and unity gain frequency (f_T) of the NPN transistor are approximately 2 dB and 3 GHz, respectively, at I_E = 1.5 mA. The collector load can be resistive, as shown in Figure 10, or tuned as shown in Figure 14. When both input and output are tuned and/or impedance matched care must be taken to prevent unwanted oscillations — this is why the 2 kΩ resistor is included in the collector load of Figure 14.

First Mixer

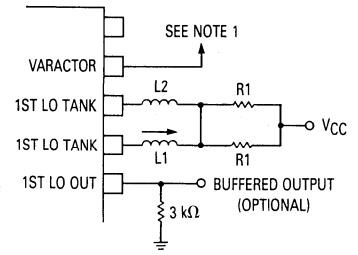
The first mixer is a doubly balanced multiplier, driven directly from the RF input and from the first local oscillator via a cascode amplifier. It is used to convert the RF input frequency down to the first IF of 10.7 MHz. The input admittance seen at either RF input pin is 670 ohms in parallel with 7 pF at 50 MHz; that is, Rp = 670 Ω and Cp = 7 pF. The series equivalent impedance at 50 MHz is Rs = 210 Ω and Cs = 10.2 pF. The first mixer's input is differential, but can be driven single-ended with no loss in system gain. If a single-ended input is used, be sure to AC ground the unused pin. This can be done with a bypass capacitor to the negative rail (V_{EE}) or by connecting the pin directly to the V_{CC} supply.

The isolation of the mixer is shown in Table 1, and of particular value in many applications will be the strong attenuation (41 dB) of the local oscillator at the mixer input. The isolation is due to the fully balanced mixer configuration used and helps to reduce LO radiation at the receiver's antenna.

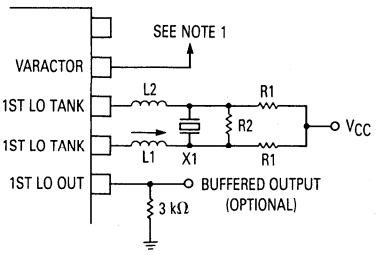
Table 1. First Mixer Isolation Level (in dB) at:

Signal	LO Tank	Mixer Out (IF)	Mixer In (RF)
LO	0	−17	−41
RF	−16	−9	0
IF	−29	0	<−40

Initial Alignment of LC Tank



Final Configuration



NOTES:

1. The varactor control pin controls the net capacitance across the local oscillator tank pins. The net capacitance will be approximately 20–25 pF when this pin is left open and 10–15 pF when connected to V_{CC}, depending upon strays and the V_{CC} value used. If the V_{CC} supply is regulated, connect the varactor control pin to V_{CC}; otherwise, bypass via a 0.01 μF capacitor to ground.
2. Connect the oscillator as shown in the left hand drawing (Initial Alignment) and adjust L1 so that the tank resonates approximately 2–3 MHz below the crystal frequency. The frequency should be checked by examining the buffered output using a high impedance probe or by some sort of inductive pickup which will not push the oscillator off frequency. The frequency should be:

$$f_{LO} \approx \frac{1}{2\pi \sqrt{(L1 + L2)\, C_{varactor}}}$$

3. Break the L1–L2 connection and add X1 and R2. Verify that the LO operates at the desired frequency by applying an RF input of 10.7 MHz above or below the crystal frequency and checking for receiver quieting. Make sure that there is proper LO amplitude. Also there should be approximately 200 mVpp seen at either LO tank pin. The buffered LO output should yield 200–600 mVpp depending on the V_{CC} value used.
4. The R2 resistor must be included or else the oscillator will latch.
5. This method has been proven effective up to 65 MHz using 3rd overtone crystals, but has proven unreliable at higher frequencies (usually using 5th and 7th overtone types). For higher frequency operation on a single channel, a signal can be injected into the local oscillator port. (See the "First Mixer and Oscillator" section.)
6. Component values: The R1 resistors should be 10 to 50 kΩ and are included in order to add some current and gain to the local oscillator. L1 should equal L2 in nominal value and a fixed value might be used but startup with different crystals might be degraded. R2 should be 300 to 1500 Ω. X1 should be 3rd overtone, series mode resonant (no load capacitance specified).

Figure 2. Running the MC3362/3 First Local Oscillator on a Single Channel Under Crystal Control

The open circuit conversion voltage gain of the first mixer is typically 24 dB, flat to 7 MHz. Internal rolloff is provided above 7 MHz to suppress RF and LO signals and spurious products sent on to the second mixer. The gain at 10.7 MHz is typically 18 dB. The output circuit is an emitter follower which is impedance-matched to 330 ohms to drive 10.7 MHz ceramic filters which typically have 330 ohm input and output impedances. For applications which require a high impedance crystal filters, impedance matching will likely need to be added at the first mixer's output to preserve the filter's response.

First Local Oscillator and Varactor Diodes

Associated with the first mixer is the first local oscillator (LO). It is a complete voltage controlled oscillator and only requires an external LC tank circuit (no external varactor diode). For multichannel applications, the oscillator includes varactor tuning and a buffered output suitable for interfacing to a PLL frequency synthesizer. This is the approach used in the receivers of Figures 10 and 11. The maximum oscillation frequency obtained has been approximately 190 MHz, achieved by injecting extra current into the oscillator. To inject current into the local oscillator, connect pull-up resistors of 10–50 kΩ from V_{CC} to each LO tank pin. The LO buffered output varies from 400 mVpp to 1100 mVpp with supply voltage and the output waveform appears best with R_{pd} = 3 kΩ, as shown in Figure 3.

There are internal varactor diodes which have capacitance which appears across the local oscillator tank pins. The internal capacitance can range from 10 to 25 pF depending on the control voltage applied to the varactor control pin (MC3362 Pin 23, MC3363 Pin 27). The capacitance is maximum when the voltage applied is at the minimum (0.7 V) value. Applying voltages greater than V_{CC} and lower than 0.7 V to the varactor control pin can cause the oscillator to stop.

The first local oscillator can be crystal controlled to run on a single channel. The procedure of Figure 2 shows how to do this for applications through 65 MHz. The receiver of Figure 10 uses this approach.

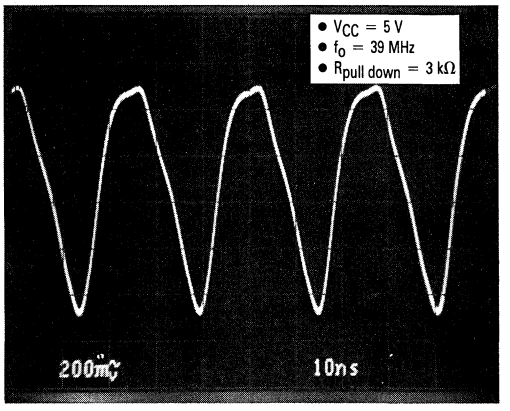


Figure 3. First Local Oscillator Buffered Output

A third application of the local oscillator is to drive it from an external source. This is recommended for applications from 75 MHz to 200 MHz and beyond which do not require PLL frequency synthesis. The inputs are differential and they must be driven using a wideband RF transformer or balun. The input voltage seen at either tank pin should be roughly 100 mVrms to ensure proper operation of the mixer and care should be taken so that any inductance present at the LO tank pins does not resonate with the internal varactor capacitance (a small valued resistor of 50–100 Ω should ensure this does not occur). Using this approach, no loss in mixer gain is seen until the RF and LO inputs are taken over 450 MHz. The RF and LO inputs should be run with a 10.7 MHz difference in frequency to accommodate the first IF bandwidth, so image frequency considerations (preselector filter quality) may limit the maximum RF input frequency to less than 450 MHz.

Second Mixer and Second Local Oscillator

After the 10.7 MHz IF signal is filtered using a ceramic filter, it is applied to the second mixer input. The second mixer is also doubly balanced to reduce spurious responses and typically is used to convert the 10.7 MHz IF down to 455 kHz for application to the limiting amplifier and detection circuitry. In the typical low cost application, the mixer is driven single-endedly from a ceramic filter, with one of the mixer inputs bypassed directly to the V_{CC} supply. The open circuit conversion voltage gain is typically 25 dB. For applications which require a high impedance crystal filter, impedance matching will likely need to be added at the second mixer input to preserve the filter response. The second mixer output is rolled off above 500 kHz, to reduce spurious response and idle noise.

The second local oscillator is a Colpitts type which is typically run under crystal control. The crystal used is specified for fundamental mode operation, calibrated for parallel resonance with a load capacitance of 30–40 pF. The typical waveform seen at the base is shown in Figure 4. The oscillator can be run at 10.240 MHz or 10.245 MHz, depending on the first local oscillator frequency desired.

The MC3362 second local oscillator has a buffered output available which can be used to drive the reference frequency input of a PLL synthesizer or a prescaler. An external local oscillator signal can be injected into the local oscillator's base, with the emitter pin left open. The signal should be sinusoidal and should be approximately 300 mVpp to 500 mVpp in level.

The output admittance of the second mixer at 500 kHz is 1500 Ω in parallel with 50 pF; that is, Rp = 1500 Ω and Cp = 50 pF. The series equivalent impedance is Rs = 1420 Ω and Cs = 1065 pF. This impedance matches the typical input impedance of standard 455 kHz ceramic filters, which have 1500–2000 Ω typical input and output impedances.

Limiting IF Amplifier and Quadrature Detector

The 455 kHz IF signal is applied to the limiting IF amplifier, where it is amplified and limited before application to the quadrature detection circuitry. The limiting IF amplifier input has an input impedance of approximately 1.5 kΩ, which provides good power transfer from 1.5 kΩ ceramic filters. The limiting IF circuitry has 10 μV input sensitivity for −3 dB limiting, flat to 1 MHz. In order to preserve overall power supply current drain, the limiting IF and the receiver in general are not designed for wideband applications.

The coupling capacitor from limiter output to quadrature tank and detector input is provided internally and its value is 5 pF. The 455 kHz oscillator circuit is typically built around an LC tank circuit, with Cp = 180 pF, Lp = 680 μH. **Typical ceramic resonators can not be driven from the quadrature tank pin.** A waveform like that of Figure 5 should appear at the quadrature tank pin during periods of full receiver quieting and no modulation.

Meter Drive (RSSI)

The amplitude of the RF input signal at the appropriate frequency is monitored by meter drive circuitry. This circuitry detects the amount of limiting in the limiting IF amplifier and produces a linear change in current (nominally 0.1 μA) at the meter drive pin for each decibel of change in the RF input. The meter drive circuitry is fairly

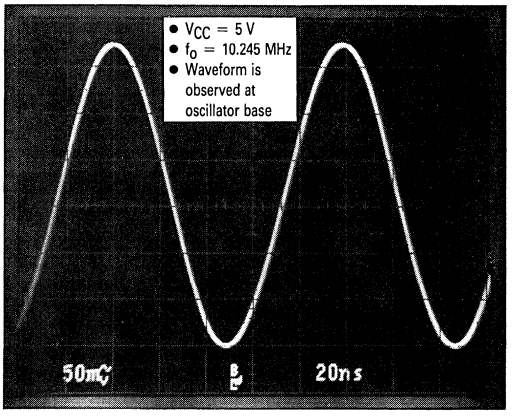


Figure 4. Second Local Oscillator Waveform

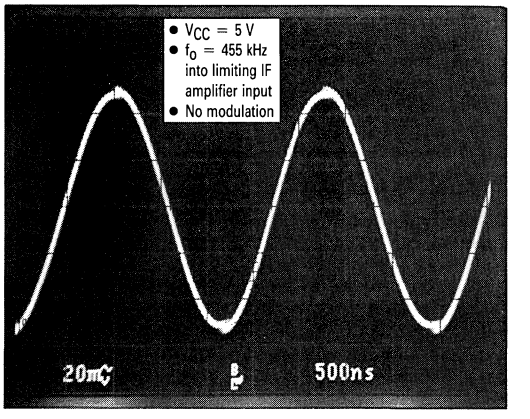


Figure 5. Quadrature Tank Pin Waveform Under Strong Received Signal Condition

linear for input signal levels over a 60 dB range. This output can be used as a meter drive or Received Signal Strength Indicator (RSSI) and needs to be bufffered. In order to provide a linear, wide ranging RSSI output voltage, three things must be accomplished:

1. The Meter Drive pin (MC3362 Pin 10, MC3363 Pin 12) should be clamped to within $V_{BE}/2$ (approximately 300 mV) of the MC3362/3 supply voltage, or loading of the Meter Drive's current source will occur. **The carrier detect output is disabled (high output) when the Meter Drive pin is clamped in this manner.** There are diodes present at the Meter Drive pin which can interfere with the Meter Drive. (See Figure 6 for a schematic representation.) With these diodes present the voltage swing possible at the Meter Drive pin is limited to a diode drop above and below the V_{CC} supply.
2. Some type of current to voltage conversion must take place. The RSSI output is typically 4 to 12 μA.
3. Negative feedback must be provided in the output buffer to counteract buffer amplifier gain variations. Some method of output level adjustment may be desirable.

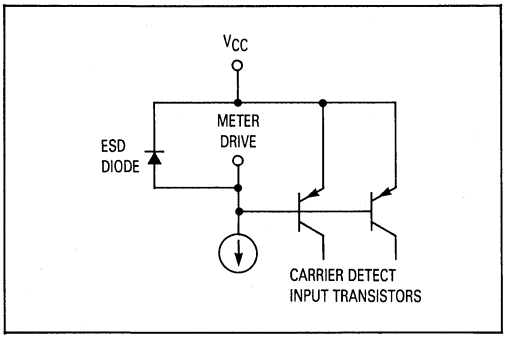


Figure 6. Schematic Representation of Meter Drive "Parasitic Circuits"

Carrier Detect

Another configuration for the meter drive and carrier detect circuitry, is to program the carrier detect output using a resistor from the meter drive pin to the V_{CC} supply. The carrier detect pin is an open collector output so a pull-up resistor is required. The carrier detect is active low, meaning that an RF input above the programmed trip level will yield a low output (<0.1 V) at the carrier detect pin. When the RF input is below the trip level (or is detuned) the carrier detect pin will be at the supply voltage. The trip level is set by the resistor value used between the meter drive pin and supply. A resistor of 130 kΩ sets the trip level to approximately -110 dBm at the first mixer's input, which is roughly the 12 dB SINAD point of the receivers with no external RF amplification. It should be noted that the meter drive current will not have the same linear 0.1 μA/dB current-input level relationship as when the meter drive is buffered as discussed above, so an analog RSSI output is not really achievable when Carrier Detect is used.

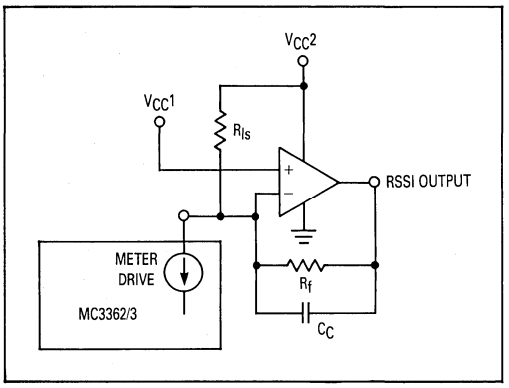


Figure 7. Sample RSSI Buffer

- Recommend MC33171 as the operational amplifier. The MC33171 is a low-power single supply single op amp with offset adjustment capability.
- $V_{CC}1$ = MC3363 supply (2 V to 7 V)
- $V_{OUT} = V_{CC}1 + I_{meter}(R_f)$
- $V_{CC}2$ = Op amp supply. Make this high enough to stay within the op amp's common mode input range — equal to $V_{CC}1 + 2.2$ V for the MC33171. This voltage also must be high enough to provide the maximum V_{OUT} desired.
- R_{IS} can be added to level shift the output, and is optional. The output voltage will be adjusted downward by a factor of $(V_{CC}1 - V_{CC}2)(R_f/R_{IS})$.
- Compensation capacitor C_C is added to ensure stability and will limit the circuit's response time.
- This circuit is not recommended for general purpose AM detection.

Muting (MC3363 only)

Audio muting can be provided in two ways. The carrier detect output can be DC coupled to the MC3363 muting op amp input (Pin 15) and the op amp output can serve to mute the audio. That is, the op amp output (Pin 19) serves as a switch to ground in the audio signal path. When the carrier level decreases below the carrier detect trip point, the carrier detect pin will go to V_{CC} and the op amp output will go into saturation, muting the audio. This yields a simple squelch with minimum external components and is shown in Figures 10 and 14.

Another way to mute the audio on MC3363 is to use the op amp as an active filter for detecting noise above the audio passband. The recovered audio is fed through the active filter, rectified, integrated and compared to a reference level. When the level rises above the reference, a squelch gate is triggered. The data slicing comparator on the MC3363 might be used as a squelch gate. This noise triggered squelch would be executed similarly to the squelch in MC3357/59/61 FM IF applications. (See the MC3359 data sheet for details.) This type of squelch frees the Meter Drive circuit to provide a linear output as noted under "Meter Drive (RSSI)" above.

Data Recovery

Both receivers contain a data slicing comparator which provides data shaping and limiting of frequency-shift keyed (FSK) serial data transmissions. The data slicer is a non-inverting type, with the negative input terminal biased internally to $V_{CC}/2$. Typically the data slicer is AC coupled to the recovered audio pin via a 0.01 μF to 0.1 μF capacitor. Larger coupling capacitors can cause distortion of the detected output and this is seen as negative slew rate limiting in Figures 8 and 9. A pull down resistor from the detector output pin to V_{EE} will reduce this effect if objectionable. The comparator output is an open collector so a pull-up resistor is required.

Comparator hysteresis is available by connecting the comparator output and input using a high-valued resistor. This helps maintain data integrity as the recovered audio becomes noisy, or for long bit strings of one polarity. Resistor values below 120 kΩ are not recommended as the comparator input signal will not be able to overcome the large hysteresis induced. Figure 8A shows data jitter resulting from noisy demodulated data signal. The improvement seen when hysteresis was added is shown in Figure 8B.

The maximum usable FSK data rate for any narrowband FM system is typically 1200 baud subject to IF and quadrature bandwidth and adjacent channel spacing limitations. The approximate bandwidth required to generate or receive a frequency modulated signal is:

BW $\approx$ 2 (f_{mod} + f_{dev}) kHz, where f_{mod} is the modulating frequency and f_{dev} is the frequency deviation.

This is known as Carson's Rule and is fairly accurate. Any modulating signal which exceeds the available IF bandwidth will be attenuated and/or distorted. For proper recovery of square waves including the leading and trailing edges approximately the 7th harmonic should be present. For a 1200 baud (600 Hz) square wave with f_{dev} = 3 kHz, f_{mod} = 4.2 kHz (7th harmonic of 600 Hz square wave), the bandwidth needed is: BW $\approx$ 2(4.2 + 3) kHz = 14.4 kHz = $\pm$7.2 kHz, which is acceptable in narrowband FM channels. Figures 9A and 9B show the effect of trying to pass a 9600 baud modulated carrier through a narrowband channel, with resulting degradation of recovered data.

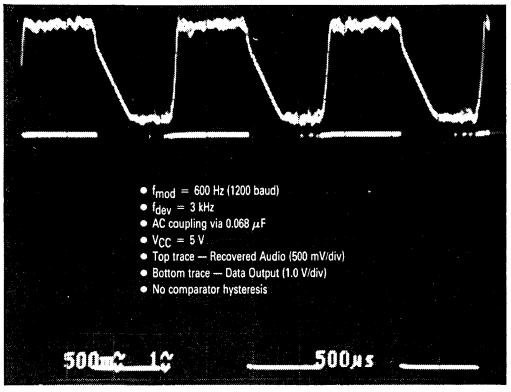


Figure 8A. Noisy Recovered Data Signal Causes Data Jitter

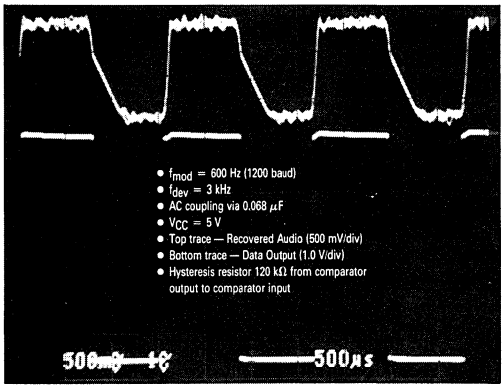


Figure 8B. Improvement in Data Jitter Through Addition of Hysteresis

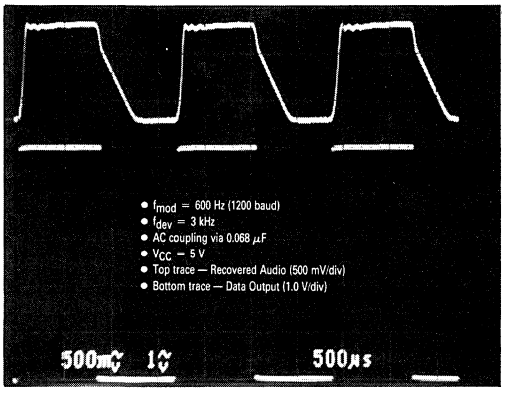


Figure 9A. FSK Data Recovery at 1200 Baud

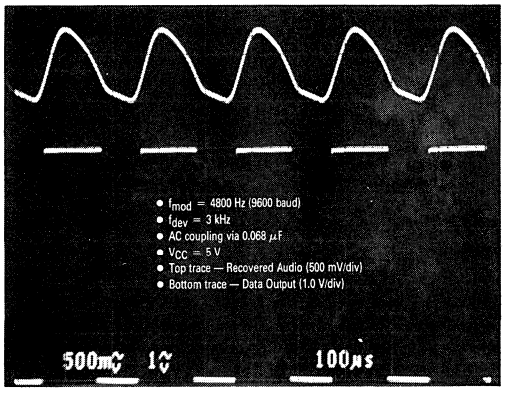


Figure 9B. Distortion of Recovered Audio with 9600 Baud Modulation

For narrowband RF modems where 300 baud is adequate, an audio frequency shift keyed (AFSK) approach is recommended. In this application two audio tones (for Logic "0" and Logic "1") are modulated onto an RF carrier and transmitted to the receiver, which reproduces the audio tone sequence. The audio tones can be generated at the transmitter and decoded after the receiver by the MC145442/3 single chip 300 baud modems.

BREADBOARDING

Do not attempt to build a high frequency radio circuit using a wirewrap or plug-in prototype board. While the MC3362 and the MC3363 are "tame" as high gain receivers go, high frequency layout techniques are critical to obtaining optimal receiver performance. This means (typically) a one- or two-sided copper clad board with adequate ground plane connected to V_{EE} potential. **It is also important that all V_{CC} interconnections are made using copper traces on the board. Do not use "free floating" point to point wiring for the V_{CC} interconnections!** In general, keep all lead lengths as short as possible, with an emphasis on minimizing the highest frequency pathlengths. Decoupling capacitors should be placed close to the IC. If these techniques are not followed then the receiver sensitivity and noise quieting will suffer, and oscillations can occur.

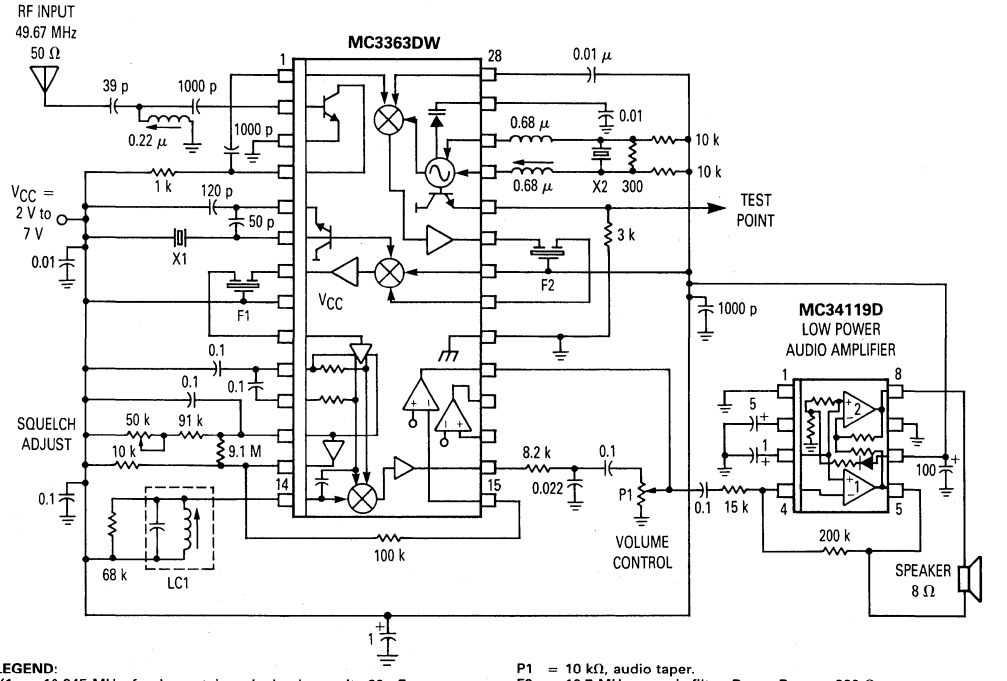
APPLICATIONS CIRCUITS

Single Channel VHF FM Narrowband Receiver

The first application shown is of a complete single channel VHF receiver operating at 49.67 MHz. This application includes a suitable circuit for running the first local oscillator under crystal control on a single channel, which is particularly useful for dedicated remote control links and low cost two-way radios through 75 MHz. The circuit contains a simple carrier level based squelch circuit and audio amplification.

The 49.67 MHz receiver frequency is within the 49 MHz USA cordless telephone band. Radios built for this band may qualify under FCC Code of Federal Regulations Title 47, Part 15, for use by unlicensed operators. It is important to know the federal regulations concerning a particular frequency channel or band of channels before a receiver circuit is design **(see the notes on FEDERAL REGULATIONS, RECOMMENDED STANDARDS above).**

Figure 10 shows the complete receiver schematic. The LC network shown is used to match the input impedance



LEGEND:
X1 = 10.245 MHz, fundamental mode, load capacity 32 pF.
F1 = 455 kHz ceramic filter, $R_{in} = R_{out} = 1.5\ k\Omega$ to $2\ k\Omega$. Part numbers are muRata CFU455X or CFW455X — suffix denotes bandwidth.
LC1 = 455 kHz quadrature tank circuit. Part numbers are Toko RMC2A6597 HM or 5SVLC-0637BGT (smaller). Ceramic discriminators cannot be used with the MC3362/3, as their input impedance is too low.
P1 = 10 kΩ, audio taper.
F2 = 10.7 MHz ceramic filter, $R_{in} = R_{out} = 330\ \Omega$. Part numbers are muRata SFE10.7MJ-A, SFA10.7MF5, or SFE10.7MS2-A.
X2 = 38.97 MHz, 3rd overtone, series mode (no load capacity specified).

All capacitors in microfarads, inductors in Henries and resistors in Ohms unless otherwise specified.

Figure 10. Single Channel FM VHF Receiver at 49.67 MHz

of the RF amplifier to 50 Ω at this frequency. The amplifier collector load is a single resistor for simplicity and in order to enhance stability. The method of Figure 2 was used to develop the crystal controlled oscillator circuit at 38.97 MHz. The RC integrator rolls off the audio above 2 kHz in order to minimize unwanted noise output. This enhances receiver sensitivity and provides proper audio deemphasis. The receiver, without the audio amplifier, has 6.2 mA current drain at V_{CC} = 5 V for a total dissipation of 31 mW. Using a 455 kHz filter with a 6 dB bandwidth of ±10 kHz the receiver has a 12 dB SINAD point of 0.28 μV, modulation acceptance of 10.4 kHz and distortion below 1.2% with f_{mod} = 1 kHz and modulation deviation f_{dev} = 3 kHz. The maximum (S+N)/N ratio obtained is 60 dB.

The MC34119 audio amplifier adds 3 mA quiescent current drain at 5 V, can deliver 250 mW into an 8 Ω speaker and has differential outputs which eliminate the need for the typical large audio coupling capacitor. It also has a chip disable input which provides muting and power conservation.

Ten Channel Frequency Synthesized Cordless Telephone Receiver

A demonstration receiver circuit has been built featuring the MC3362 and the MC145160 dual phase locked loop (DPLL). This receiver features frequency synthesis to cover the ten channels allocated in the USA for cordless telephone (CT) receivers in the 46 MHz (handset) and 49 MHz (base station) frequency ranges. The MC14516X series DPLL's feature two complete loops which control both the transmitter output and receiver first LO frequencies.

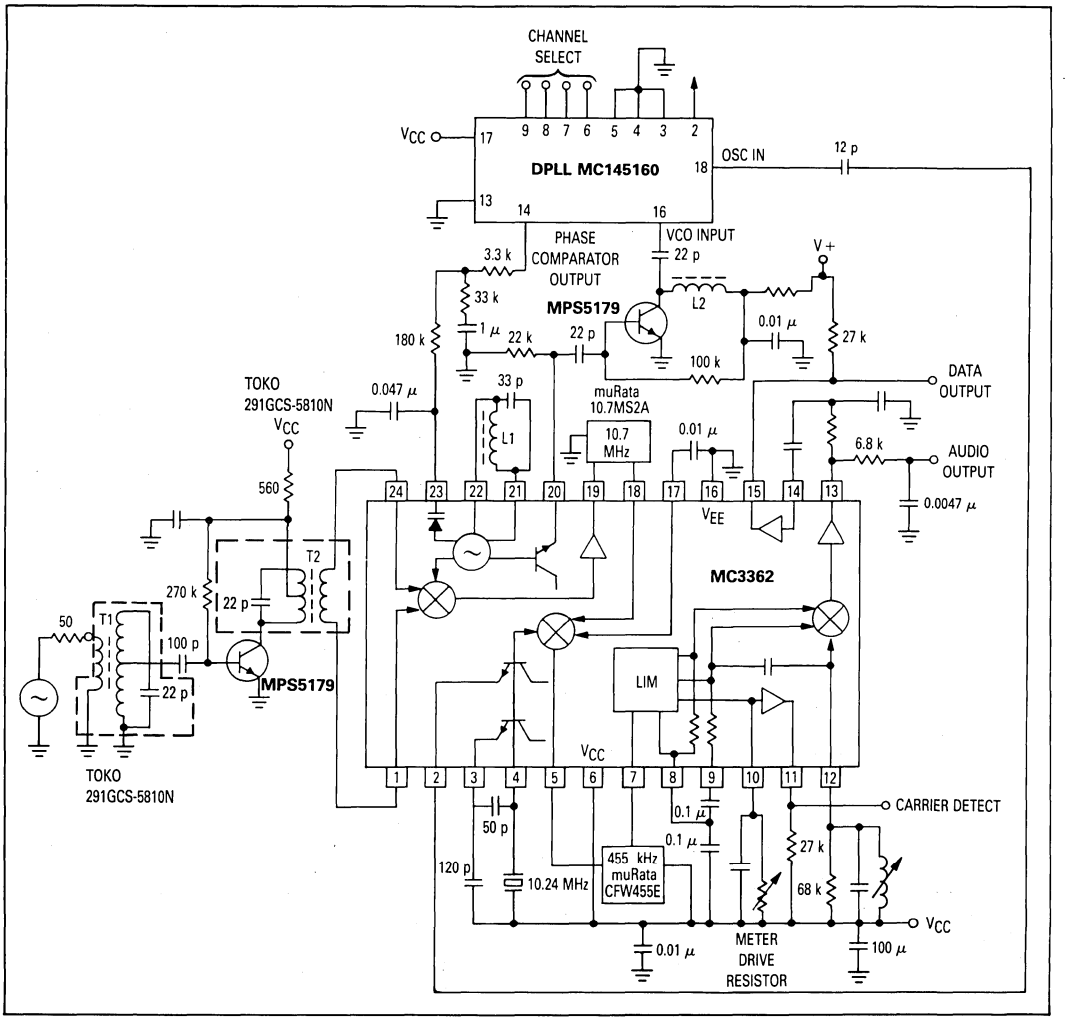


Figure 11. Ten Channel Frequency Synthesized Receiver

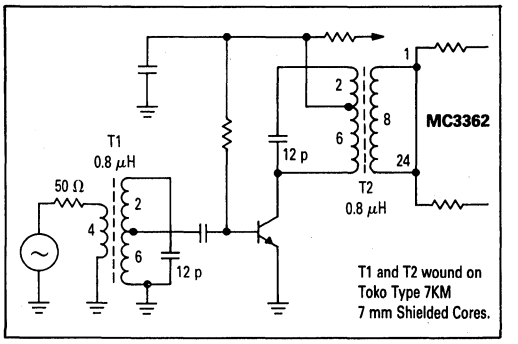


Figure 12. Information on T1 and T2 of Figure 11

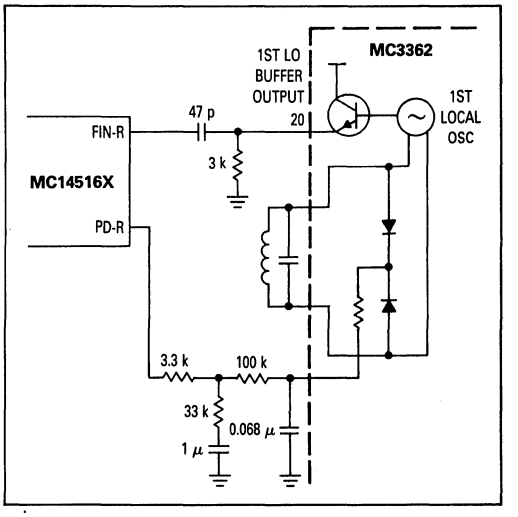


Figure 13. Simple Interface of MC3362/3 To DPLL MC14516X

Figure 11 shows the complete schematic diagram. A simple RF transistor amplifier is included to overcome antenna and RF preselector losses. The output of the VCO buffer is amplified by an external transistor amplifier so that the VCO signal strength is large enough to drive the receiver input pin (Fin-R) of the DPLL properly. Gain of the VCO is set at approximately 400 kHz using the LC values shown. The SB (Pin 3) of the MC145160 is grounded to disable the transmit loop to simplify development of the circuit and reduce power consumption. The DC voltage at the varactor control input of the MC3362 (Pin 23) is adjusted to $V_{CC}/2$. The system reference frequency of 10.240 MHz is generated in the MC3362 second LO and fed into the Osc-In (Pin 18) of the MC145160.

With a supply voltage of V_{CC} = 3 V and modulating signal f_{mod} = 1 kHz, f_{dev} = 3 kHz the receiver yields an input sensitivity of 0.6 μV for 20 dB noise quieting and 0.2 μV for 12 dB SINAD from a 50 Ω source. The audio distortion is less than 3 percent. The minimum noise floor is less than 80 μV and the maximum (S+N)/N ratio is 53 dB.

There is a simpler way to interface the MC3362/3 to the MC145160 DPLL as shown in Figure 13. The VCO signal (about 400 mVpp with V_{CC} = 3 V using a pull-down resistor of 3 kΩ from the MC3362 Pin 20 to V_{EE}) is fed directly into the Fin-R input (Pin 16) of the MC145160. With this configuration, the noise floor is raised to 245 μV, 10 dB higher than the circuit of Figure 11.

256 Channel Frequency Synthesized Two Meter Amateur Band Receiver

A more traditional PLL frequency synthesizer approach is needed to provide frequency flexibility and to allow the MC3362/3 receivers to operate in the VHF "high band" (130 MHz to 172 MHz). A receiver is shown which covers the entire Two Meter (referring to radio wavelength) amateur radio band from 144 MHz to 148 MHz in 256 channels spaced at 20 kHz. The complete receiver and PLL frequency synthesizer are shown in Figures 14 and 15. The receiver achieved the same specifications as the 49.67 MHz MC3363 receiver discussed above.

The MC3363 receiver was chosen because squelch and good sensitivity with minimum component count were desired. To obtain good operation of MC3363 VCO above 75 MHz, the first local oscillator must be running well. To ensure this, the V_{CC} supply voltage is kept above 3 V which increases the current in the local oscillator circuitry. Extra current is also injected into the local oscillator via pull-up resistors of 10 kΩ from each of the local oscillator tank pins to the V_{CC} supply. With the components of Figure 14, the receiver VCO had an average gain of 1.5 MHz/V.

The VCO output is amplified and fed into an MC12017 dual modulus prescaler which drives the input of the PLL frequency synthesizer. The MC145152-2 PLL frequency synthesizer was chosen for its ease of use and parallel input format. The MC33171 bipolar operational amplifier was chosen as the active integrator (loop filter) because of its low power drain, offset adjustment capability and ability to operate from a single supply voltage. The design equations and assumptions used to determine loop filter components are shown below. The MC145152-2 data sheet and other sources go into much more detail on PLL theory and performance.

Calculations of Loop Filter For VCO PLL Frequency Synthesis

Assumptions:

f_o = 135.3 MHz (local oscillator center frequency)
f_s = 20 kHz (channel spacing)
f_b = 0.01 f_s (loop bandwidth)
f_{rc} = 20 f_b (filter cutoff frequency)
§ = 0.707 (loop damping factor)
V_{DD} = 5 V (PLL supply voltage)
K_{VCO} = 9.4 x 10^6 rad/V (VCO gain, measured on MC3363 receiver)
C1 = 0.1 μF (active integrator component)

Results:

$f_b = 0.01\ f_s = 0.01\ (20\ kHz) = 200\ Hz$

$f_{rc} = 20\ f_b = 20\ (200) = 4\ kHz$

$K_\phi = V_{DD} / 2\pi = 0.796$ (phase detector gain)

$$\frac{w_n = 2\pi f_b}{\{2\S^2 + 1 + [(2\S^2 + 1)^2 + 1]^{0.5}\}^{0.5}} = \left(\frac{1257}{2.06}\right) = 610\ rad/sec$$

$N_t = f_o / f_s = 135.3\ MHz / 20\ kHz = 6765$

$R_1 = K_\phi K_{VCO} / (C1\ w_n^2\ N_t) = 29.7\ k\Omega \approx 30\ k\Omega$

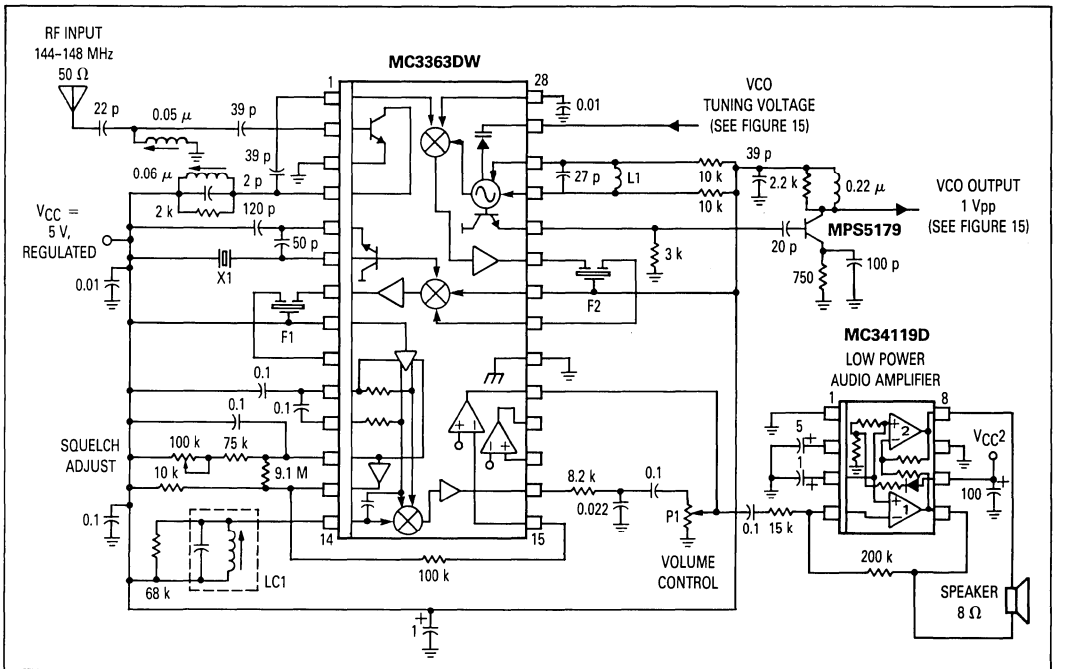
$R_2 = 2\ \S \div (w_n\ C1) = 23.2\ k\Omega \approx 24\ k\Omega$

$C_C = 4 \div (2\ R_1 f_{rc}) \approx 0.017\ \mu F$

With an 8 bit parallel input format several possible switch settings and resultant counter values and receiver frequencies are shown in Table 2 below (Note: N_t = NP + A, where P = 64 for the MC12017).

Table 2. PLL Frequency Synthesizer Switch Settings and Frequencies

Switches	N	P	A	N_t	f_{VCO} (MHz) = $N_t f_s$	f_{rx} (MHz) = f_{VCO} + 10.7 MHz
00000000	104	64	0	6656	133.12	143.82
00000001	104	64	1	6657	133.32	143.84
01000000	105	64	0	6720	134.40	145.10
01111111	105	64	63	6783	135.66	146.36
10000000	106	64	0	6784	135.68	146.38
10001101	106	64	13	6797	135.94	146.64
10011100	106	64	28	6812	136.24	146.94
11010001	107	64	17	6865	137.30	148.00
11111111	107	64	63	6911	138.22	148.92



LEGEND:

X1 = 10.245 MHz, fundamental mode, load capacity 32 pF.

F1 = 455 kHz ceramic filter, $R_{in} = R_{out} = 1.5\ k\Omega$ to 2 kΩ. Part numbers are muRata CFU455X or CFW455X — suffix denotes bandwidth.

LC1 = 455 kHz quadrature tank circuit. Part numbers are Toko 7MC-8128Z or 5SVLC-0637BGT (smaller). Ceramic discriminators cannot be used with the MC3362/3, as their input impedance is too low.

P1 = 10 kΩ, audio taper.

F2 = 10.7 MHz ceramic filter, $R_{in} = R_{out} = 330\ \Omega$. Part numbers are muRata SFE10.7MJ-A, SFA10.7MF5, or SFE10.7MS2-A.

L1 = 3 Turns #18 AWG, 0.25" diam., 0.125" spacing, air wound.

$V_{CC}2$ = 2–12 V, must be well decoupled from the V_{CC} source for the MC3363.

All capacitors in microfarads, inductors in Henries and resistors in Ohms unless otherwise specified.

Figure 14. 2 Meter Frequency Synthesized FM Receiver

Single Chip Weatherband Receiver

An application of the MC3362 as a simple receiver tuned to the NOAA Weatherband (162.4 MHz to 162.55 MHz) is shown in Figure 16. The RF input is applied directly to the mixer input, using a simple "L network" to provide impedance matching of the mixer input to 50 Ω. The system sensitivity for 12 dB SINAD is 0.67 μV at the input from a 50 Ω source in this application, which is as good as most inexpensive weather cubes and the dual conversion design allows for excellent image protection to be provided.

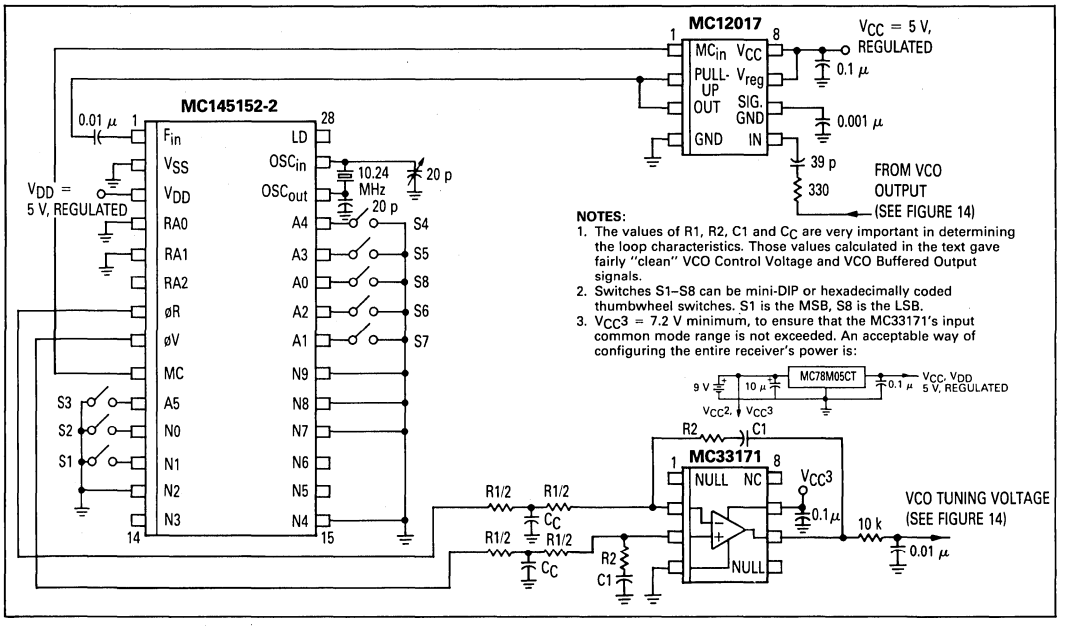


Figure 15. 256 Channel VCO Control Using PLL Frequency Synthesizer

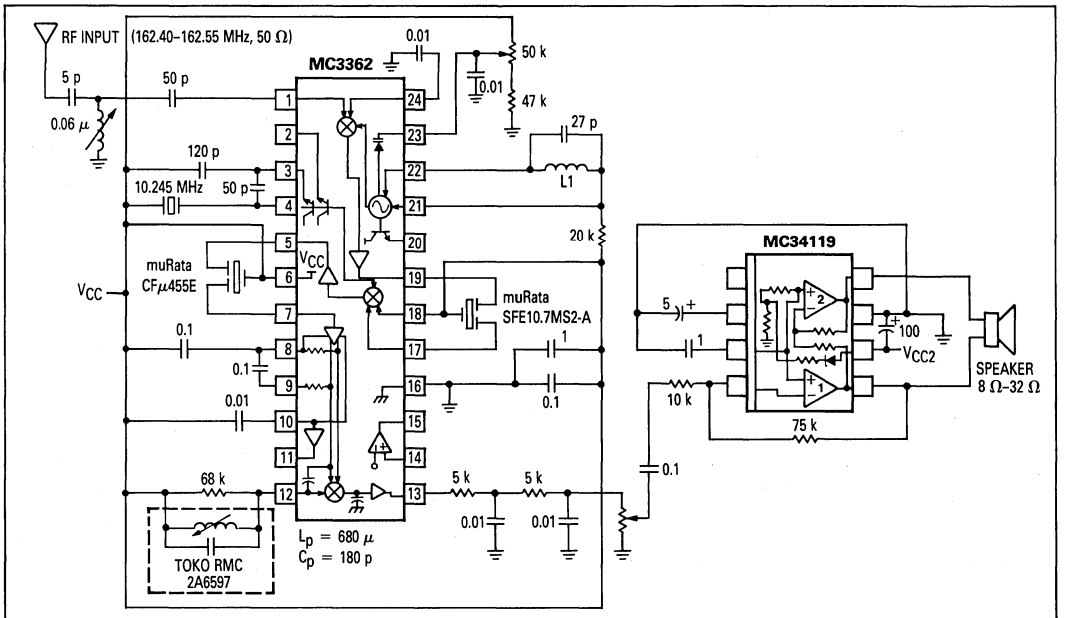


Figure 16. MC3362 Application as a Tunable Weather Band Receiver

The first local oscillator is free-running in this application and the receiver is manually tunable over a range of ±1 MHz. The oscillator's frequency and tuning range are determined by the external tank circuit values chosen. Keep in mind that the internal varactor diodes add 10–25 pF of capacity across the tank pins, depending on the varactor control voltage applied.

This circuit is easily built to vefify receiver characteristics on the lab bench, but as shown is not suited for mass production. The local oscillator temperature stability is not nearly adequate in this free-running configuration and microphonic pickup is difficult to avoid. Before a narrowband receiver is production-ready, the first local oscillator must be stable to within approximately ±100 Hz. The "First Mixer and Oscillator" section provides notes on driving the first mixer using an external oscillator signal above 50 MHz. The MC2833 FM transmitter IC might serve as the local oscillator source up to 200 MHz.

SUMMARY

The high degree of integration and MOSAIC process used in the MC3362/3 receivers give the radio designer new levels of space and power economy, while providing high performance and considerable design flexibility. The receivers shown and alternate configurations discussed should interest designers of cordless phones, VHF two way radios, remote control receivers, wireless data links and home security systems.

APPENDIX — DIRECTORY OF COMPONENT MANUFACTURERS

muRata-Erie 2200 Lake Park Drive Smyrna, GA 30080	(404) 436-1300 ceramic filters
Toko America Inc. 1250 Feehanville Drive Mount Prospect, IL 60056 **Distributor — Digikey** **Distributor — Inductor Supply**	(708) 297-0070 quadrature coils coils, transformers (800) 344-4539 (800) 854-1881 (800) 472-8421 (California)
Coilcraft 1102 Silver Lake Road Cary, IL 60013	(708) 639-6400 coils
California Crystal Laboratories	(800) 333-9825 crystals
Fox Electronics	(813) 693-0099 crystals
International Crystals	(405) 236-3741 crystals
Standard Crystal Corporation	(818) 443-2121 crystals

Note: Design-in kits including printed circuit boards are available from analog marketing. Call (602) 897-3820

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AN1207

The MC145170 in Basic HF and VHF Oscillators

Prepared by: David Babin and Mark Clark

Phase-locked loop (PLL) frequency synthesizers are commonly found in communication gear today. The carrier oscillator in a transmitter and local oscillator (LO) in a receiver are where PLL frequency synthesizers are utilized. In some cellular phones, a synthesizer can also be used to generate 90 MHz for an offset loop. In addition, synthesizers can be used in computers and other digital systems to create different clocks which are synchronized to a master clock.

The MC145170 is available to address some of these applications. The frequency capability of the MC145170 is very broad — from a few hertz to 160 MHz.

ADVANTAGES

Frequency synthesizers, such as the MC145170, use digital dividers which can be placed under MCU control. Usually, all that is required to change frequencies is to change the divide ratio of the N Counter. Tuning in less than a millisecond is achievable.

The MC145170 can generate many frequencies based on the accuracy of a single reference source. For example, the reference can be a low-cost basic crystal oscillator or a temperature-compensated crystal oscillator (TCXO). Therefore, high tuning accuracies can be achieved. Boosting of the reference frequency by 100x or more is achievable.

ELEMENTS IN THE LOOP

The components used in the PLL frequency synthesizer of Figure 1 are the MC145170 PLL chip, low-pass filter, and voltage-controlled oscillator (VCO). Sometimes a voltage-controlled multivibrator (VCM) is used in place of the VCO. The output of a VCM is a square wave and is usually integrated before being fed to other sections of the radio. The VCM output can be directly used in computers and other digital equipment. The output of a VCO or VCM is typically buffered, as shown.

As shown in Figure 2, the MC145170 contains a reference oscillator, reference counter (R Counter), VCO/VCM counter (N Counter), and phase detector. A more detailed block diagram is shown in the data sheet.

HF SYNTHESIZER

The basic information required for designing a stable high-frequency PLL frequency synthesizer is the frequencies required, tuning resolution, lock time, and overshoot. For the example design of Figure 3, the frequencies needed are 9.20 MHz to 12.19 MHz. The resolution (usually the same as the frequency steps or channel spacing) is 230 kHz. The lock time is 8 ms and a maximum overshoot of approximately 15% is targeted. For purposes of this example, lock is considered to be when the frequency is within about 1% of the final value.

HF SYNTHESIZER LOW-PASS FILTER

In this design, assume a square wave output is acceptable. To generate a square wave, a MC1658 VCM chip is chosen. Per the transfer characteristic given in the data sheet, the MC1658 transfer function, K_{VCM}, is approximately 1×10^8 radians/second/volt. The loading presented by the MC1658 control input is large; the maximum input current is 350 μA. Therefore, an active low-pass filter is used so that loading does not affect the filter's response. See Figure 3. In the filter, a 2N7002 FET is chosen because it has very high transconductance (80 mmhos) and low input leakage (100 nA).

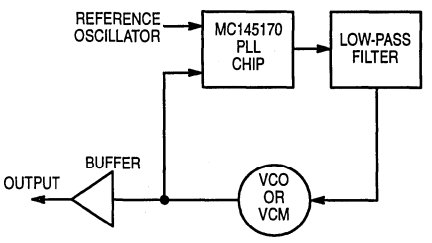


Figure 1. PLL Frequency Synthesizer

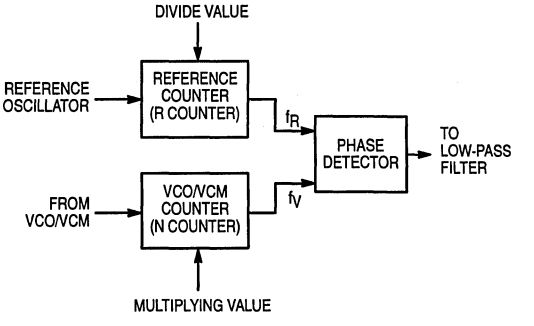


Figure 2. Detail of the MC145170

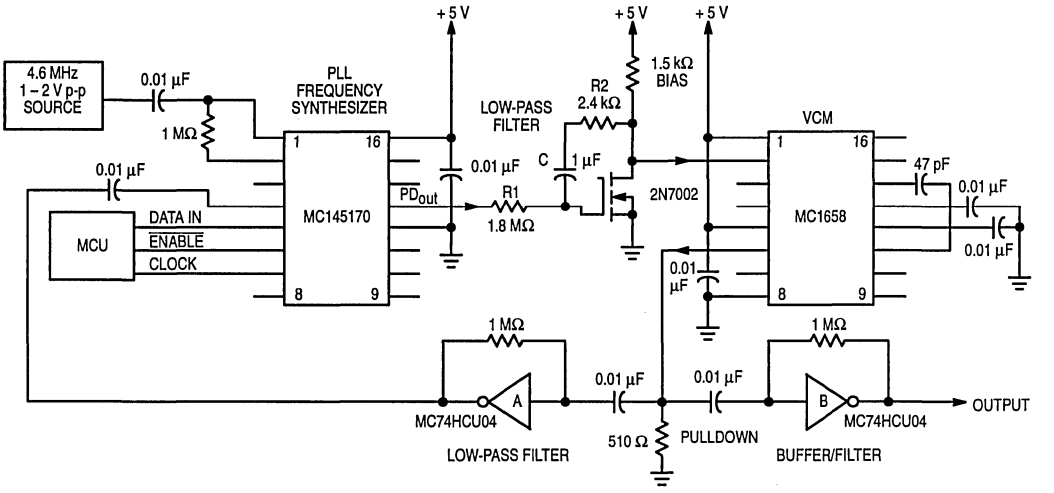


Figure 3. HF Synthesizer

In order to calculate the average divide value for the N Counter, follow this procedure. First, determine the average frequency; this is (12.19 + 9.2)/2 = 10.695 MHz or approximately 10.7 MHz. Next, divide this frequency by the resolution: 10.7 MHz/230 kHz = about 47.

Next, reference application note AN535 (see book DL130/D Rev 1). The active filter chosen takes the form shown in Figure 9 of the application note. This filter is used with the single-ended phase detector output of the MC145170, PD_{out}. The phase detector associated with PD_{out} has a gain $K_\phi = V_{DD}/4\pi$. For a supply of 5 V, this is $5/4\pi = 0.398$ V/rad. The system's step response is shown in Figure 4. To achieve about 15% overshoot, a damping factor of 0.8 is used. This causes frequency to settle to within 1% at $\omega_n t = 5.5$.

The information up to this point is as follows.

f_{ref} = 230 kHz

f_{VCM} = 9.2 to 12.19 MHz; the average is 10.7 MHz, average N = 47

power supply = 5 V for the phase detector

$K_{VCM} = 1 \times 10^8$ rad/s/V

overshoot = approximately 15%, yields a damping factor = 0.8

lock time t = 8 ms settling to within 1%, $\omega_n t = 5.5$

$K\phi$ or $K_p = 0.398$ V/rad.

From the application note, equation 61, $\omega_n = 5.5/t = 5.5/0.008 = 687.5$ rad/s.

Equation 59 is $R1C = (K_p K_v)/\omega_n^2 N$

$= (0.398 \times 1 \times 10^8)/687.5^2 \times 47$

$= 1.79$

Equation 59 is used because of the high-gain FET.

Next, the capacitor C is picked to be 1 µF. Therefore, R1 = 1.79/C which is 1.79 MΩ. The standard value of 1.8 MΩ is used for R1.

Equation 63 is $R2 = (2\zeta)/C\ \omega_n$

$= (2 \times 0.8)/(1 \times 10^{-6} \times 687.5)$

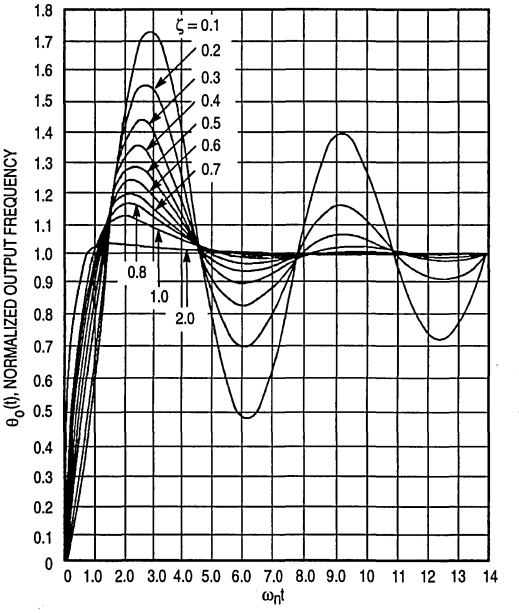


Figure 4. Type 2 Second Order Step Response

$= 2.33$ kΩ.

A standard value for R2 of 2.4 kΩ is utilized.

HF SYNTHESIZER PROGRAMMING

Programming the MC145170 is straightforward. The three registers may be programmed in a byte-oriented fashion. The registers retain their values as long as power is applied. Thus,

usually both the C and R Registers are programmed just once, right after power up.

The C Register, which configures the device, is programmed with $C0 (1 byte). This sets the phase detector to the proper polarity and activates PD_{out}. This also turns off the unused outputs. The phase detector polarity is determined by the filter and the VCM. For this example, the MC1658 data sheet shows that a higher voltage level is needed if speed is to be increased. However, the low-pass filter inverts the signal from the phase detector (due to the active element configuration). Therefore, the programming of the polarity for the phase detector means that the POL bit must be a "1."

The R Register is programmed for a divide value that results in the proper frequency at the phase detector reference input. In this case, 230 kHz is needed. Therefore, with the 4.6 MHz source shown in Figure 3, the R Register needs a value of $000014 (3 bytes, 20 in decimal).

The N Register determines the frequency tuned. Tuning 9.2 MHz requires the proper value for N to multiply up the reference of 230 kHz to 9.2 MHz. This is 40 decimal. For 12.19 MHz, the value is 53 decimal. To tune over the range, change the value in the N Register within the range of 40 to 53 with a 2-byte transfer. Table 1 shows the possible frequencies.

Table 1. The HF Oscillator Frequencies

N Value	Frequency, MHz
40	9.20
41	9.43
42	9.66
43	9.89
44	10.12
45	10.35
46	10.58
47	10.81
48	11.04
49	11.27
50	11.50
51	11.73
52	11.96
53	12.19

EXTRA FILTERING FOR THE HF LOOP

When the HF oscillator was built, the proper frequencies could not be tuned. The output of the MC1658 was examined with an oscilloscope and the switching edges were discovered to be "ragged." That is, the output did not appear to be a square wave with clean transitions.

The f_{in} input of the MC145170 is sensitive to 500 mV p-p signals, and the ragged edges were being amplified and counted down by the N Counter. Therefore, the edges needed cleaning up. One method would have been to add a low-pass filter between the MC1658 and MC145170. However, because an additional buffer was needed elsewhere in the circuit, an MC74HCU04 inverter was used in place of the filter. This inverter's frequency response is low enough to clean up the ragged edges. That is, filtering of the ragged edges occurred, and the output had smoother transitions. As mentioned previously, one of the elements in the inverter package was used to buffer the output of the VCM before feeding it to the outside world. See Figure 3.

VHF SYNTHESIZER

The MC145170 may be used in VHF designs, also. The range for this next example is 140 to 160 MHz in 100 kHz increments.

VHF SYNTHESIZER LOW-PASS FILTER

To illustrate design with the doubled-ended phase detector, the ϕ_R and ϕ_V outputs are used. This requires an operational amplifier, as shown in Figure 5. From the design guidelines shown in the MC145170 data sheet, the following equations are used:

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{N C R_1}} \quad (1)$$

damping factor $$\zeta = \frac{\omega_n R_2 C}{2} \quad (2)$$

where, from the data sheet, the equation for the ϕ_R and ϕ_V phase detector,

$$K_\phi = \frac{V_{DD}}{2\pi} = \frac{5}{2\pi} = 0.796 \text{ V/rad} \quad (3)$$

$\zeta = 0.707$,

$$\omega_n = \frac{2\pi f_R}{50} = \frac{2\pi \times 100 \text{ kHz}}{50} = 12{,}566 \text{ rad/s} \quad (4)$$

and

$$K_{VCO} = \frac{2\pi \Delta f_{VCO}}{\Delta V_{VCO}} = \frac{2\pi \times (160 - 140 \text{ MHz})}{10 - 2}$$

$$= 1.57 \times 10^7 \text{ rad/s/V} \quad (5)$$

The control voltage range on the input to the VCO is picked to be 2 to 10 V.

The average frequency = (140 + 160)/2 = 150 MHz. Therefore, the average N = 1500.

The above choices for ζ and ω_n are rules of thumb that are a good design starting point. A larger ω_n value results in faster loop lock times and higher reference frequency VCO sidebands for similar sideband filtering. (See Advanced Considerations.)

Choosing C_1 to be 4700 pF, R_1 is calculated from the rearranged expression for ω_n as:

$$R_1 = \frac{K_\phi K_{VCO}}{C_1 \omega_n^2 N} = \frac{(0.796 \text{ V/rad})(1.57 \times 10^7 \text{ rad/s/V})}{(4700 \text{ pF})(12{,}566 \text{ rad/s})^2 (1500)}$$

$$= 11.23 \text{ k}\Omega \quad (6)$$

Therefore, chose an 11 kΩ standard value resistor.

R_2 is determined from:

$$R_2 = \frac{2\zeta}{\omega_n C_1} = \frac{(2)(0.707)}{(12{,}566)(4700 \text{ pF})}$$

$$= 23.94 \text{ k}\Omega \text{ or}$$
$$2.4 \text{ k}\Omega \text{ (standard value)} \quad (7)$$

VHF SYNTHESIZER EXTRA FILTERING

For more demanding applications, extra filtering is sometimes added. This reduces the VCO sidebands caused by a small amount of the reference frequency feeding through the filter. One form of this filtering consists of spitting R1 into two resistors; each resistor is one-half the value of R1, as indicated by R1/2 in Figure 5. Capacitors C_C are added from the midpoints to ground to further filter the reference sidebands. The value of C_C is chosen so that the corner frequency of this added net-

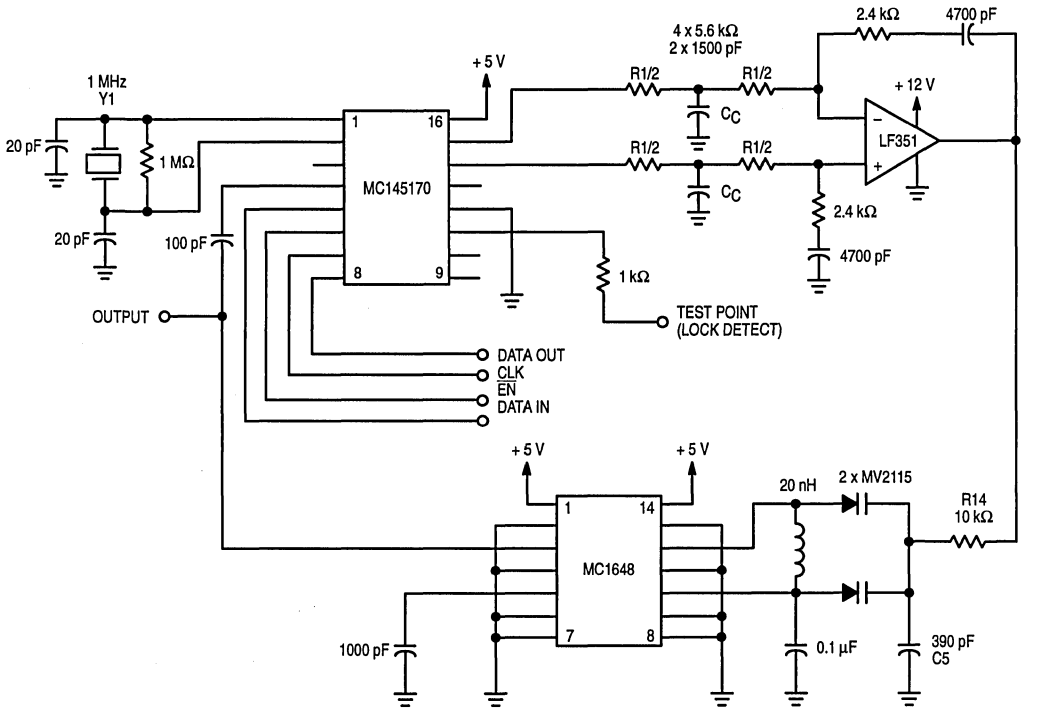


Figure 5. VHF Synthesizer

work does not significantly affect the original loop bandwidth ω_B.

The rule of thumb for an initial value is $C_C = 4 / (R1\ \omega_{RC})$, where ω_{RC} is the filter cutoff frequency. A good value is to choose ω_{RC} to be 10 x ω_B, so as to not significantly impact the original filter.

$$\omega_B = \omega_n \sqrt{1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}} \quad (8)$$

$$= 12{,}566\sqrt{1+(2)(0.707)^2+ \sqrt{2+(4)(0.707)^2+ (4)(0.707)^4}}$$

$$= 25{,}760 \text{ rad/s}$$

$$\omega_{RC} = 10\ \omega_B = (10)(25{,}760) = 257{,}600 \text{ rad/s} \quad (9)$$

$$C_C = \frac{4}{R1\omega_{RC}} = \frac{4}{(11.23\ k\Omega)(257{,}600 \text{ rad/s})} \quad (10)$$

$$= 1383 \text{ pF} \approx 1500 \text{ pF}$$

There is also a filter formed at the input to the VCO. Again, this should be selected to ensure that it does not significantly affect the loop bandwidth. For this example, the filter is dominated by R14 with C5. The capacitance of the varactors (in series with the rest of the circuit) is much smaller than C5 and can therefore be neglected for this calculation.

As above, let ω_{RC} = 257,600 rad/s be the cutoff of this filter. R1 was previously chosen to be 10 kΩ. Therefore,

$$C_5 = \frac{1}{\omega_{RC}R_{14}} = \frac{1}{(257{,}600)(10\ k\Omega)} \quad (11)$$

$$= 388 \text{ pF} \approx 390 \text{ pF}$$

THE VARACTOR

The MV2115 was selected for its tuning ratio of 2.6 to 1. The capacitance can be changed from 49.1 pF to 127.7 pF over a reverse bias swing of 2 to 30 volts. Contact your Motorola representative for information regarding the MV2115 varactor diode.

For example, three parameters are considered.

C_T = Nominal capacitance
CR = Capacitance ratio
fR = Frequency ratio

$$CR = \frac{C_V min}{C_V max} = \left(\frac{V_{max}}{V_{min}}\right)^{\rho} \quad (12)$$

where ρ = the capacitance exponent

Therefore,

$$CR = 2.6 = \left(\frac{30}{2}\right)^{\rho} \quad (13)$$

$$\log(2.6) = \rho\log(15) \quad (14)$$

$$\rho = \log(2.6)/\log(15) = 0.3528 \quad (15)$$

Using the nominal capacitance of 100 pF at 4 volts:

$$\frac{100\text{ pF}}{C_V\text{max}} = \left(\frac{10}{4\text{ V}}\right)^{0.3528} \quad (16)$$

$$\frac{100\text{ pF}}{C_V\text{max}} = 1.382$$

Solving for $C_V$max:

$$\frac{100\text{ pF}}{1.382} = 72.4\text{ pF}$$

Solving for $C_V$min:

$$2.6 = \frac{C_V\text{min}}{49.1\text{ pF}} \quad (17)$$

$$C_V\text{min} = (2.6)(49.1\text{ pF})$$

$$C_V\text{min} = 127.7\text{ pF}$$

THE VCO

For convenience, the MC1648 VCO is selected. The tuning range of the VCO may be calculated as

$$\frac{f_{max}}{f_{min}} = \frac{(C_d\text{max} + C_S)^{0.5}}{(C_d\text{min} + C_S)^{0.5}} \quad (18)$$

where

$$f_{min} = \frac{1}{2\pi[L(C_d\text{max} + C_S)]^{0.5}} \quad (19)$$

As shown in Figure 8 of the data sheet, the VCO tank circuit is comprised of two varactors and an inductor. Typically, a single varactor might be used in either a series or parallel configuration. However, the second varactor has a two-fold purpose. First, if the 10 kΩ isolating impedance is left in place, the varactors add in series for a smaller capacitance. Second, the added varactor acts to eliminate distortion due to the tank voltage changing.

Therefore, with the two varactors in series, $C_d$max′ = $C_d$max/2. The shunt capacitance (input plus external capacitance) is symbolized by C_S.

Therefore, solving for the inductance:

$$L = \frac{1}{(2\pi f_{min})^2(C_d\text{max}' + C_S)} = 19.9\text{ nH} \approx 20\text{ nH} \quad (20)$$

The Q of the inductor should be more than 100 for best performance.

$$f_{min} = \frac{1}{2\pi[(19.9\text{ nH})(69.85\text{ pF})]^{0.5}} = 135\text{ MHz} \quad (21)$$

$$f_{max} = \frac{1}{2\pi[(19.9\text{ nH})(42.2\text{ pF})]^{0.5}} = 173\text{ MHz} \quad (22)$$

The frequency ratio is 1.5 to 1 and is impacted by the tuning range of the MV2115 varactor diode used in the tank circuit. Therefore, the required range of 140 to 160 MHz is not limited by this VCO design.

A pc board should be used to obtain favorable results with this VHF circuit. The lead lengths in the tank circuit should be kept short to minimize parasitic inductance. The length of the trace from the VCO output to the PLL input should be kept as short as possible. In addition, use of surface-mount components is recommended to help minimize strays.

VHF SYNTHESIZER PROGRAMMING

Again, programming the three registers of the MC145170 is straightforward. Also, usually both the C and the R Registers are programmed only once, after power up.

The C Register configures the device and is programmed with $80 (1 byte). This sets the phase detector to the correct polarity and activates the ϕ_R and ϕ_V outputs while turning off the other outputs. Like the HF oscillator, the phase detector polarity is determined by how the filter is hooked up and the VCO.

The R Register is programmed for a divide value that delivers the proper frequency at the phase detector reference input. In this case, 100 kHz is needed. Therefore, with the 1 MHz crystal shown, the R Register needs a value of $00000A (3 bytes, 10 in decimal).

The N Register determines the frequency tuned. To tune 140 MHz, the value required for N to multiply up the reference of 100 kHz to 140 MHz is 1400 decimal. For 160 MHz, the value is 1600 decimal. To tune over the range, simply change the value in the N Register with a 2-byte transfer.

ADVANCED CONSIDERATIONS

The circuit of Figure 5 may not function at very-high temperature. The reason is that the MC145170 is guaranteed to a maximum frequency of 160 MHz at 85°C. Therefore, there is no margin for overshoot (reference Figure 4) at high temperature. There are two possible solutions: (1) maintain the ambient temperature at less than 60°C, or (2) limit the tuning to less than 160 MHz.

Operational amplifiers are usually too noisy for critical applications. Therefore, if an active element is required in the integrator, one or more discrete transistors are utilized. These may be FETs or bipolar devices. However, active filter elements are not needed if the VCO loading is not severe, such as is encountered with most discrete VCO designs. Because active elements add noise, some performance parameters are improved if they are not used. On the other hand, an active filter can be used to scale up the VCO control voltage. For example, to tune a wide range, the control voltage may have to range up to 10 V. For a 5 V PLL output, this would be scaled by 2x via use of active elements.

Some applications have requirements that must be met in the areas of phase noise and reference suppression. These parameters are in conflict with fast lock times. That is, as lock times are reduced, reference suppression becomes more difficult. Both reference suppression and phase noise are advanced areas that are covered in several publications. As an example, consider that the VCO input voltage range for the above VHF loop was merely picked to be 8 V. Advanced techniques demand a trade off between this voltage range and

the spectral purity of the VCO output. This is because the lower the control voltage range, the more sensitive the VCO is to noise coming into its control input.

A VCO IC may not offer enough performance for some applications. Therefore, the VCO may have to be designed from discrete components.

Figure 6 shows the performance of the VHF Oscillator prototype on a spectrum analyzer. Note that the reference sidebands appear at 100 kHz as expected, and are 50 dB down.

REFERENCES

CMOS Application-Specific Standard ICs, book DL130/D, Motorola, 1990, MC145170 data sheet and AN535 application note.

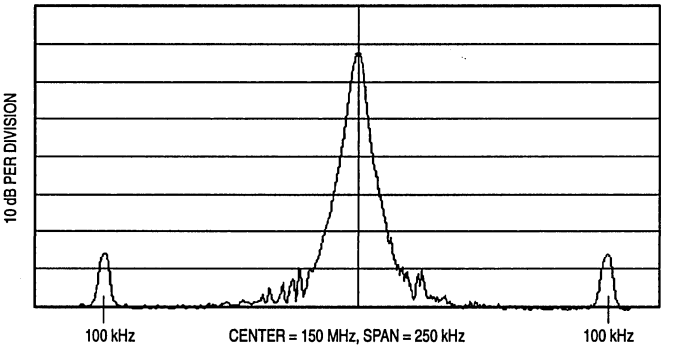


Figure 6. VHF Oscillator Performance

Analyze, don't estimate, phase-lock-loop

performance of type-2, third-order systems. You can do the job with a programmable-calculator in 48 steps, or less.

Phase-lock loops certainly have many uses, especially in frequency synthesizers, but exact mathematical calculation of their transfer functions is difficult. This is particularly true for type-2, third-order systems (Fig. 1), which don't produce steady-state phase errors for step-position or velocity signal inputs. However, a small programmable calculator, the HP-25, easily —and exactly—determines the complete loop transfer function in 48 steps. In addition, the program data reveals the noise reduction you can expect for the loop's voltage-controlled oscillator (VCO), as well as the loop's stability.

Most other design approaches must resort to second-order loop approximations to simplify calculations; a more exact method manually would take too long.

Unlike a type-1 loop, a type-2 loop has two *true* integrators within the loop—a VCO and an integrator/filter after the phase detector. Replacing the integrator/filter with a passive-RC, low-pass filter results in the more common type-1 response, which doesn't have the phase coherence for step and velocity inputs between the two signal inputs to the phase comparator that the type-2 has.

Moreover, a third-order loop—the order is usually determined by the transfer function of the integrator/filter ($F_{(s)}$)—can reduce VCO noise substantially, without increasing reference-frequency sidebands in the output signal. These sidebands hamper simpler loop-circuit performance.

The transfer function of a generalized phase-lock loop can be represented as follows (Fig. 2):

$$\frac{\theta_o\ (s)}{\theta_i\ (s)} = \frac{G_{(s)}}{1 + G_{(s)}H_{(s)}} \qquad (1)$$

where, from Fig. 1

$$G_{(s)} = (K_p)(F_{(s)})(K_v/s) \qquad (2)$$

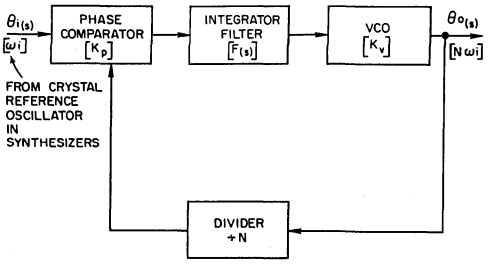
and

$$H_s = 1/N. \qquad (3)$$

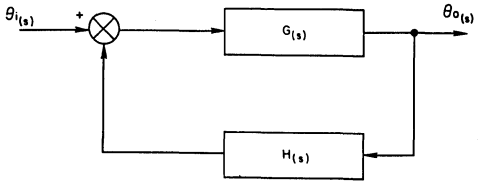
The phase comparator transfer function is K_p and N is a digital counter/divider factor.

A typical integrator/filter built around an op amp (Fig. 3) has a transfer function determined by the amplifier-circuit's closed-loop gain,

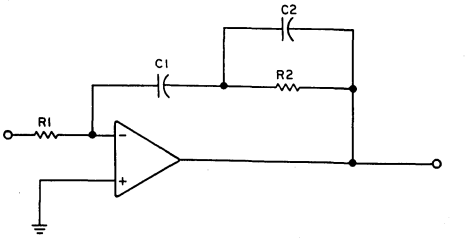
$$A_{CL} = -\frac{Z_f}{Z_1},$$



1. **A type-2 phase-lock loop** has two true integrators—the integrator/filter (F_s) and the VCO (K_v). Replacing the integrator/filter with a passive-RC network converts the circuit to a type-1 system.



2. **The phase-lock loop's generalized open-loop transfer function,** $G_{(s)}$ $H_{(s)}$, has a third-order denominator—from which the circuit's name is derived.



3. **An integrator/filter circuit** can be built with a wideband op amp and RC feedback network.

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Table 1. Third order type-2 PLL

Display Line	Display Code	Key Entry	Remarks	Registers
00				R_0
01	1573	(g)π		
02	61	x		
03	02	2		R_1 T_1
04	61	x		
05	2307	STO 7		
06	2403	RCL 3		R_2 T_2
07	61	x		
08	01	1		
09	1509	(g)→P		R_3 T_3
10	2304	STO 4		
11	22	R↓		
12	2402	RCL 2		R_4
13	2407	RCL 7		
14	61	x		
15	32	CHS		R_5 $\frac{K_p K_v}{N}$
16	01	1		
17	32	CHS		
18	1509	(g)→P		R_6
19	2404	RCL 4		
20	71	÷		
21	2405	RCL 5		R_7
22	61	x		
23	2401	RCL 1		
24	71	÷		
25	2407	RCL 7		
26	1502	(g) x^2		
27	71	÷		
28	2304	STO 4		
29	1408	(f) log		
30	02	2		
31	00	0		
32	61	x	$\lvert G_{j\omega}H_{j\omega}\rvert$	
33	74	R/S		
34	22	R↓		
35	21	x ≷ y		
36	41	—	∠ θ	
37	74	R/S		
38	2404	RCL 4		
39	1409	(f)→R		
40	01	1		
41	51	+		
42	1509	(g)→P		
43	1522	(g) 1/x		
44	1408	(f) log		
45	02	2		
46	00	0		
47	61	x	e/en	
48	1300	GTO 00		
49				

where $Z_1 = R_1$ (4)

Z_f = impedance of feedback network

The transform of the feedback network is

$$Z_f(s) = \frac{s(C_1+C_2)+\frac{1}{R_2}}{sC_1(sC_2+\frac{1}{R_2})}, \quad (5)$$

and the integrator/filter transfer function is then

$$F_{(s)} = -\frac{s(C_1+C_2)+\frac{1}{R_2}}{C_1R_1(sC_2+\frac{1}{R_2})}, \quad (6)$$

Multiply Eq. 6 by R_2/R_2, then

$$F_{(s)} = -\frac{s(C_1R_2+C_2R_2)+1}{sC_1R_1(sC_2R_2+1)} \quad (7)$$

or

$$F_{(s)} = -\frac{sT_2+1}{sT_1(sT_3+1)}, \quad (8)$$

where $T_1 = R_1C_1$

$T_2 = R_2(C_1 + C_2)$

$T_3 = R_2C_2$

The open-loop transfer function of Fig. 2 is $G_{(s)}H_{(s)}$; therefore, from Eqs. 2, 3 and 8

$$G_{(s)}H_{(s)} = \frac{s(T_2)(K_vK_p) + K_vK_p}{s^3NT_1T_3 + s^2NT_1} \quad (9)$$

Note the third-order denominator, from which the circuit's name—third-order-loop—is derived. Note also the deletion of the minus sign: the circuit configuration (a phase inverter) provides the negative feedback. Both K_p and K_v are positive.

If you substitute jω for s in Eq. 9, you can get the equation for plotting the magnitude and phase of the circuit's open-loop gain as a function of frequency:

$$G_{(j\omega)}H_{(j\omega)} = -\frac{j\omega(T_2)(K_vK_p) + K_vK_p}{j\omega^3NT_1T_3 + \omega^2NT_1}. \quad (10)$$

Step	Instructions	Input Data/ Units	Keys			Output Data/ Units
1	Enter program					
2	Store T_1	R_1	ENTER			
		C_1	X	STO	1	
	T_2	C_1	ENTER			
		C_2	+			
		R_2	X	STO	2	
	T_3	R_2	ENTER			
		C_2	X	STO	3	
	(Kp Kv)/N	K_p	ENTER			
		K_v	X			
		N	=	STO	5	
3	Calculate	F	(f)	PRGM	R/S	$G_{j\omega}H_{j\omega}$ ∠ θ (e/en)
			R/S			
			R/S			
4	Repeat step 3 for other values of frequency, F					

Table 2. Calculated loop response

Frequency Hz	Open-loop response dB	Open-loop response ∠θ	Loop response to VCO noise dB
100	116.01	−179.94	−116.01
1000	76.01	−179.44	−76.01
10,000	36.06	−174.44	−35.92
94,650	0*	−139.85	3.27
100,000	−0.71	−138.58	3.30**
1,000,000	−26.25	−139.59	0.32
10,000,000	−63.21	−174.68	0.01

*Unity-gain point **Maximum overshoot

A servo-loop damping factor that appears in lower-order loops is not defined in third-order loops. Instead you determine stability by the phase margin between −180° and the phase at a frequency where the gain is unity in the open-loop gain function, $G_{j\omega}H_{j\omega}$. The larger the phase margin, the more stable the system. A phase margin of about 45° produces an adequately damped loop. More than 45° means greater stability and, of course, the system may oscillate when the margin approaches zero.

Feedback also reduces noise

Not only does feedback determine the system's stability, but it also delineates its noise-output characteristics. When running free, the VCO is considerably more "noisy" than is the circuit's reference crystal oscillator. But the circuit's feedback loop substantially reduces the VCO's output-noise spectrum, especially, at low frequencies. This particular reduction is fortunate, because the VCO's noise output has 1/f characteristics: high-frequency noise tends to fall off without outside help, but the low frequency needs the help.

An approximate expression for the loop's output phase noise is

$$\sqrt{[(|e/e_n|)(e_v)]^2 + [(N)(e_x)]^2}, \quad (11)$$

where e_x = crystal-oscillator noise.

e_v = VCO noise.

(e/e_n) = loop's response to VCO noise.

And the loop's response to the VCO noise is

$$(e/e_n) = \frac{1}{1 + G_{(s)}H_{(s)}}. \quad (12)$$

Although $G_{(s)}H_{(s)}$ determined from Eq. 9 is complex, only the magnitude of (e/e_n) from Eq. 12 is used in Eq. 11. Note: The greater the open-loop transfer function, $G_{(s)}H_{(s)}$, the smaller the (e/e_n), and the lower the loop's output noise. However, note also that the reference crystal oscillator's noise contribution is multiplied by the divider constant, N, though, hopefully, the crystal-oscillator noise is low.

In addition, you can get a check on the system's stability by plotting the loop's response to VCO noise (e/e_n), obtained from Eq. 12, versus frequency. You'll find that the curve has a high-pass response with a 12-dB/octave slope. For best stability, any overshoot at the cutoff frequency should be less than 6 dB. Of course, lower overshoot represents higher stability.

Clearly, the loop's mathematical analysis depends mainly upon calculation of $G_{(j\omega)}H_{(j\omega)}$ in Eq. 10.

Now comes the program

To make the calculator program simpler, rewrite Eq. 10 as follows:

$$G_{(j\omega)}H_{(j\omega)} = \frac{K_vK_p}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega T_3 + 1}\right] \quad (13)$$

Table 1 contains the program that solves Eq. 13. It provides both the magnitude and phase angle, ∠θ, of the open-loop response, $G_{(j\omega)}H_{(j\omega)}$, given T_1, T_2, T_3, K_pK_v/N and frequency, $f(\omega=2\pi f)$. The open-loop response magnitude is given in dB and its phase in degrees. Also, the magnitude of the loop's VCO noise response (Eq. 12) is given in dB. If answers in dB aren't required, however, seven steps can be eliminated.

To see how the program works, consider a 960-MHz transmitter recently proposed for a Navy application. It calls for a phase-lock loop with the following characteristics to generate the 960 MHz:

$N = 64$
$R_1 = 10{,}000\ \Omega$
$C_1 = 4700 \times 10^{-12}$ F
$R_2 = 330\ \Omega$
$C_2 = 470 \times 10^{-12}$ F
$K_p = 0.25$ V/rad
$K_v = 3 \times 10^9$ (rad/s)/V

The stable crystal-oscillator reference frequency used is 15 MHz. The frequency divider and phase comparator are built with ECL logic. From the circuit component values and transfer constants we obtain:

$T_1 = 4.7 \times 10^{-5}$ s
$T_2 = 1.706 \times 10^{-6}$ s
$T_3 = 1.551 \times 10^{-7}$ s
$(K_vK_p)/N = 11.72 \times 10^6$/s

The calculator program provided the results in Table 2. Note that the phase margin at unity gain corresponding to 94,650 Hz is 40.15°; thus the loop is fairly stable. Further, the loop's response to VCO noise shows a maximum overshoot of 3.30 dB at 100,000 Hz, which confirms the loop's stability (less than 6-dB overshoot). If the phase margin is too small or you want overdamped loop operation, the program allows you to check the effects of parameter changes and get the performance you want, quickly. However, keep all additional circuit poles above the area of interest, since they reduce phase margin and stability. In addition, don't ignore the effects of stray capacitances. And use a high-gain op amp with a wide frequency response and a VCO with a wide modulation bandwidth. ■■

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Optimize phase-lock loops to meet your needs—or determine why you can't

The time constants of a PLL's integrator/filter are the keys to controlling a loop's performance. In the integrator/filter, you can trade off circuit parameters most easily to meet your needs. The other loop components (Fig. 1) have simple, real-valued transfer functions (K_v, K_p, N) that can't be changed as easily. But the integrator/filter's transfer function (F_s), detailed in Fig. 1c is the source of the high-order complex function in the following equation for open-loop gain:

$$G(j\omega)\,H(j\omega) = \frac{K_v K_p}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega T_3 + 1}\right], \qquad (1)$$

where

T_1, T_2, T_3 = time constants defined in Fig. 1c, seconds

K_p = phase-detector gain constant, volts/radian

K_v = voltage-controlled-oscillator (VCO) sensitivity, radians/second/volt

N = frequency devisor

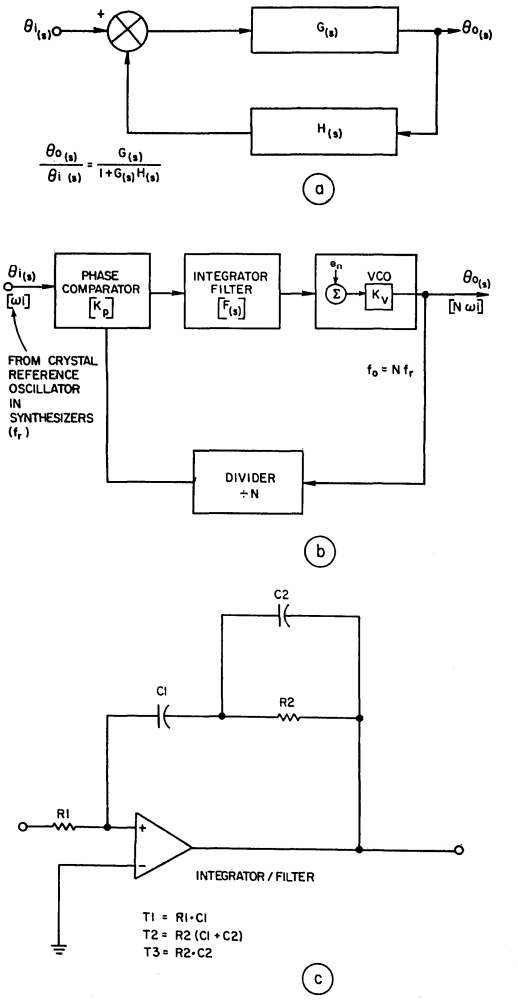
$\omega = (2\pi f)$ frequency, radians

Usually, K_p, K_v and N are given, but you can choose T_1, T_2 and T_3 to give you the loop performance you want. Generally, of course, you want the loop to be stable, to attenuate the reference frequency and to reduce VCO noise. But stability, being an absolute necessity, gets priority. The other two requirements, unfortunately, are inversely dependent and must be traded off against each other.

A damping factor to control stability as in simpler second-order loops can't be readily defined in the third-order loop of Fig. 1. Instead, the phase margin

In ED No. 10, May 10, 1978, p. 120, A. B. Przedpelski advised: "Analyze, don't estimate, phase-lock-loop performance." He showed how to calculate the performance of a given type-2, third-order PLL system with a 48-step program for an HP-25 programmable calculator. This article will show you how to optimize such a PLL to your requirements. But you will discover that you may not be able to get all requirements simultaneously. Compromises may be necessary.

Andrzej B. Przedpelski, Vice President of Development, A.R.F. Products Inc., 2559 75th St., Boulder, CO 80301.



1. **A phase-lock loop** (a) with two integrators (b) is classified type 2. And the order—third, in this case—is established by the characteristics of the integrator/filter (c). Time constants T_1, T_2 and T_3 determine the integrator/filter's detailed performance.

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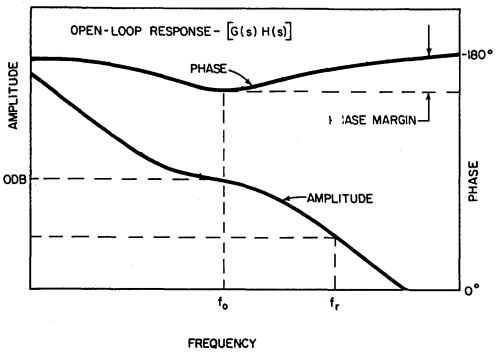
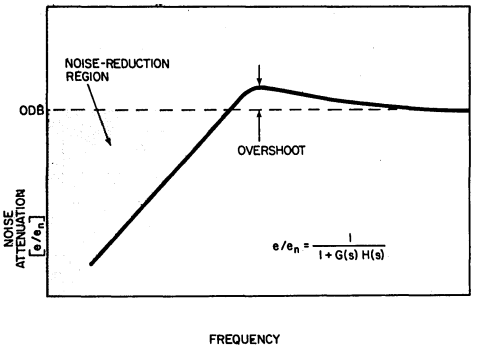


2. **This open-loop gain/phase plot** shows a typical phase displacement from −180°. When the frequency, f_o, which corresponds to 0-dB gain, is made to align with the maximum phase displacement, calculating T_1, T_2 and T_3 is simplified.



3. **Increase f_0 and you increase the noise-reduction region** —the shaded area bounded by the 0-dB line and the noise-attenuation curve.

—the difference between 180° and the phase of the open-loop transfer function, where the gain is one—becomes the criterion for stability. Fig. 2 is a typical open-loop response curve showing both amplitude and phase response, and the phase margin.

The asymptotic slope of the amplitude curve is fixed at 40 dB per octave by the loop's integrator/filter and VCO. The phase delay would be constant at −180°, except for the phase lead introduced at middle frequencies by the transfer function F(s). This phase lead provides the phase margin that ensures loop stability.

45°—a good compromise

The phase margin should be between 30° and 70° for most applications. The larger the phase margin, the more stable the loop. But a large phase margin not only slows the response, it also increases output sidebands and reduces the loop's VCO-noise suppression capability. Thus, a phase margin of about 45° is a good compromise between desired stability and the other generally undesired effects.

Ideally, a phase comparator provides an error signal that is proportional to the phase difference between its two inputs, and nothing else. But in practice, some of the reference frequency, f_r, always leak through the comparator, which frequency modulates the output signal to produce undesirable sideband frequencies. Shifting the open-loop gain-amplitude curve of G (jω) H (jω) Fig. 2 to the left would attenuate f_r and the sidebands. But such a shift also would weaken the circuit's VCO-noise suppression capability.

A typical VCO noise-reduction plot is shown in Fig. 3. Noise attentuates in the region that lies to the left of the curve and below the 0-dB line (shown crosshatched). The unity-gain frequency, f_o, defines the noise reduction: It's directly proportional to f_o. Clearly, then, shifting the G (jω) H (jω) curve to the right by increasing f_o will also increase the VCO noise-reduction region—which is opposite the requirement for reducing the sidebands. Thus, as so often happens, you must compromise. Locate the point of minimum phase shift (inflection point of the phase response, Fig. 2) exactly at f_o, the unity-gain value.

The inflection point is strategic

Locating f_o at the phase inflection point is strategically valuable, because it will help solve for the value of T_1. But first you must determine T_3. Accordingly, from Eq. 1 the phase margin, ϕ, is

$$\phi = \tan^{-1}\omega T_2 - \tan^{-1}\omega T_3 + 180°. \quad (2)$$

Differentiate ϕ with respect to ω and set the result equal to zero to locate ω_o, and the result is

$$\frac{d\phi}{d\omega} = \frac{T_2}{1+(\omega T_2)^2} - \frac{T_3}{1+(\omega T_3)^2} = 0 \quad (3)$$

Solving Eq. 3 then gives you

$$\omega_o = \frac{1}{\sqrt{T_2 T_3}} \quad (4)$$

And substituting Eq. 4 into Eq. 2 gives you

$$\tan\phi = \frac{T_2 - T_3}{2\sqrt{T_2 T_3}} \quad (5)$$

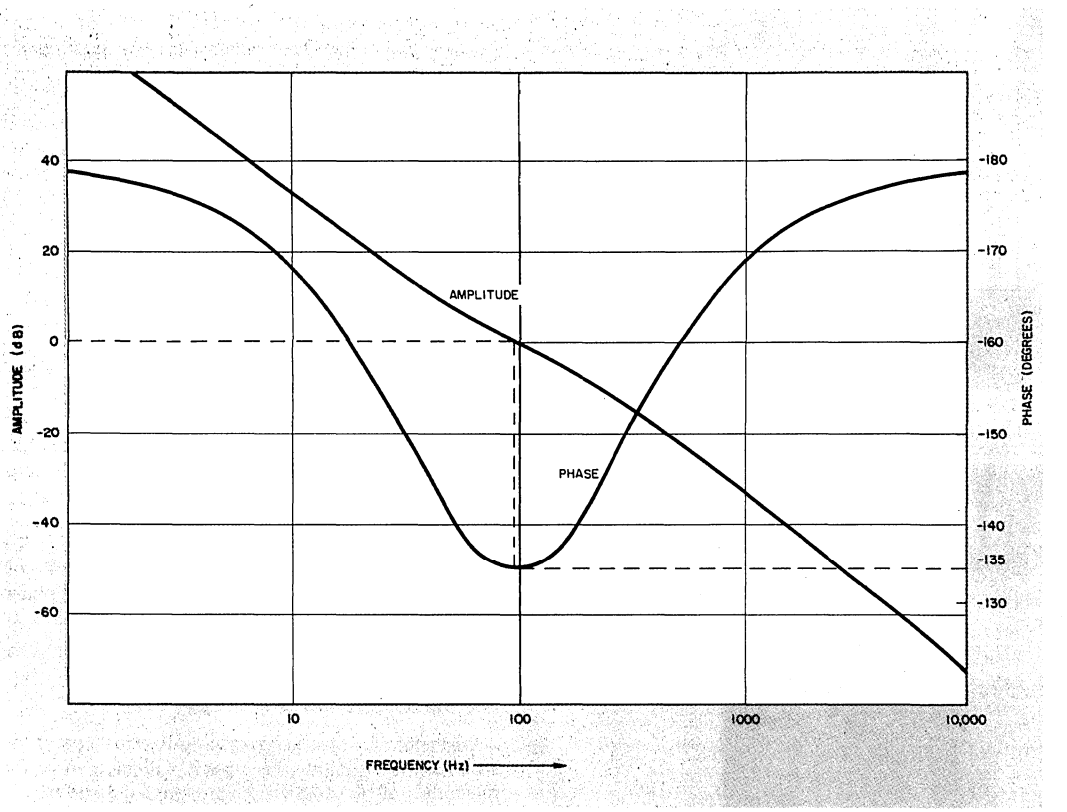
Finally, plug Eq. 4 into Eq. 5 and re-arrange to get

$$T_3 = \frac{\sec\phi - \tan\phi}{\omega_o} \quad (6)$$

Then re-arrange Eq. 5 to get

$$T_2 = \frac{1}{\omega_o^2 T_3} \quad (7)$$

Since you want the gain to be one at the phase-



4. **This plot of a PLL's open-loop transfer function** confirms the design-parameter choices—a 45° phase margin at an f_0 of 100 Hz and unity gain. The loop is stable, but some adjustments may be desirable.

inflection point, solve for T_1 in Eq. 1 with G (jω) H (jω) = 1; as a result,

$$T_1 = \frac{K_p K_v}{N\omega^2}\left[\frac{-j\omega\ T_2 - 1}{j\omega\ T_3 + 1}\right] \qquad (8)$$

The 41 steps

The program in the table solves Eqs. 6, 7 and 8 in 41 steps with an HP-25 programmable calculator. Of course, the program can be adapted to other programmable calculators.

To illustrate the program's procedure, consider a PLL that must produce an output of 16.95 MHz from a 5-kHz reference, f_r. The phase comparator, VCO and divider transfer functions are as follows:

$K_p = 0.19$ V/rad
$K_v = 10.6 \times 10^6$ rad/s/V
$N = 3390$

For stability, start with a phase margin of 45° and an f_0 of about 1/50 of f_r. Thus, with

$\phi = 45°$

and

$f_0 = 5000/50$
$= 100$ Hz,

calculate T_1, T_2 and T_3 with the program: You get

$T_1 = 3.63 \times 10^{-3}$s
$T_2 = 3.84 \times 10^{-3}$s
$T_3 = 6.59 \times 10^{-4}$s

But with those time constants you would need components with nonstandard values. However, if you select standard capacitors and resistors as follows:

$C_1 = 0.33\ \mu$F, $R_1 = 12$ k Ω,
$C_2 = 0.068\ \mu$F, $R_2 = 10$ k Ω,

you get the following time constants:

$T_1 = 3.96 \times 10^{-3}$s
$T_2 = 3.98 \times 10^{-3}$s
$T_3 = 6.8 \times 10^{-4}$s

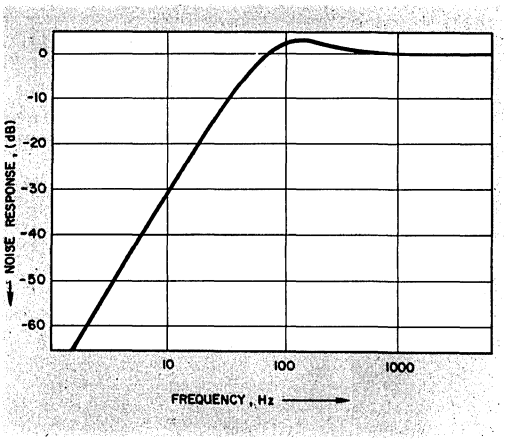
which are close enough for a first try.

Verifying the results

To verify the results, the open-loop transfer function, G (jω) H (jω), and noise response, e/e_n, were calculated with the program provided in the previous

Display Line	Display Code	Key Entry	Remarks	Registers
00				R_0
01	2407	RCL 7		
02	1406	(f) tan		
03	32	CHS		R_1
04	2407	RCL 7		
05	1405	(f) cos		
06	1522	(g) 1/x		R_2
07	51	+		
08	2406	RCL 6		
09	1573	(g) π		R_3
10	61	x		
11	02	2		
12	61	x		R_4
13	2304	STO 4		
14	71	÷		
15	2303	STO 3	3	R_5 $\frac{KpKv}{N}$
16	74	R/S		
17	2404	RCL 4		
18	1502	(g) x^2		R_6 f_o
19	61	x		
20	1522	(g) 1/x		
21	2302	STO 2	T_2	R_7 ϕ
22	74	R/S		
23	2404	RCL 4		
24	61	x		
25	01	1		
26	1509	(g)→P		
27	2403	RCL 3		
28	2404	RCL 4		
29	61	x		
30	01	1		
31	1509	(g)→P		
32	21	x≷y		
33	22	R↓		
34	71	÷		
35	2404	RCL 4		
36	1502	(g) x^2		
37	71	÷		
38	2405	RCL 5		
39	61	x		
40	2301	STO 1	T_1	
41	1300	GTO 00		

Step	Instructions	Input Data/ Units	Keys			Output Data/Units
1	Enter program					
2	Store	f_o	STO	6		
		ϕ	STO	7		
		K_p	ENTER			
		K_v	X			
		N	:	STO	5	
3	Calculate		(f)	PRGM	R/S	T_3
			R/S			T_2
			R/S			T_1
3	Recall (if desired)		RCL	1		T_1
			RCL	2		T_2
			RCL	3		T_3
			RCL	4		o



5. **The noise-response calculation** corresponding to Fig. 4 shows that VCO noise is attenuated below about 70 Hz.

article and plotted in Figs. 4 and 5. The curves confirm that the design is stable with a maximum phase margin of 45° at a frequency where the open-loop gain is about unity. And the VCO noise-reduction curve shows a moderate 3.2-dB overshoot with noise frequencies below about 70 Hz in the attenuation region.

Still, adjustments may be desired. For instance, if you want more reference-frequency (f_r) attenuation, the G (jω) H (jω) curve can be shifted to the left. Move f_o one decade (to about 10 Hz) and you'll increase the f_r attenuation by 40 dB. Or, if noise frequencies above 70 Hz are bothersome, you can shift the G (jω) H (jω) curve to the right by increasing f_o.

If you still aren't satisfied, you can change the phase margin. Reduce the margin and you improve both f_r and VCO-noise attenuation—but then you lose some stability.■■

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AR254 #3

Suppress phase-lock-loop sidebands without introducing instability

Phase-lock loops: Part Three

The first two parts of this series showed how to analyze and then optimize type-2, third-order PLL systems and provided simple calculator programs for an HP-25 to do the otherwise tedious computations.[1,2] This article takes you a step further and shows how to suppress sidebands, especially undesired when the PLL is used in frequency-synthesis systems.

Frequency synthesis, a major application of the phase-lock loop (PLL), always involves PLL-performance compromise: keeping loop bandwidth as wide as possible to reduce acquisition time and voltage-controlled oscillator noise, and at the same time suppressing reference-frequency sidebands that can pass through wide bandwidths (Fig. 1).

Fortunately, the reference frequency is considerably above the required loop bandwidth in most cases, which alleviates the sideband problem to some extent. But for heavy suppression of undesired sidebands, extra filtering is necessary. However, it must be done carefully so as not to introduce loop instability. Three filtering circuits, none of which reduce bandwidth or VCO-noise attenuation can help solve the problem. In fact, an active LP-filtering technique, the most versatile and efficient of the three, is programmed on an HP-25 to speed the design.

All methods assume that the PLL, a type-2 third-order loop,[1] meets all requirements[2] except adequate reference-frequency sideband suppression. The three approaches include RC, active-notch and active-LP filtering. The PPL's phase margin serves as a measure of loop stability, since the damping-factor concept isn't applicable to third-order loops:[2] phase margins between 30° and 45° are minimum criteria for stable operation. And the filter's action in reducing the feedforward gain, G(jω), at the sideband frequencies is the criterion for the suppression effectiveness.

Since H(jω) is equal to 1/N, a constant, then the open-loop gain, G(jω)H(jω) in Eq. 1, can be used as a measure of this sideband-suppression effectiveness:

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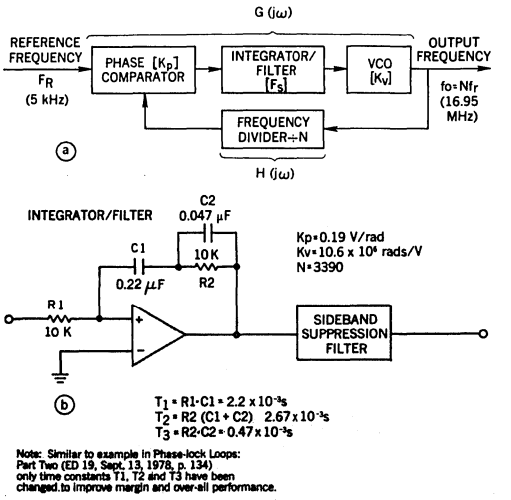

1. **A phase-lock-loop frequency synthesizer** (a) generates 16.95 MHz from a crystal-oscillator reference frequency of 5 kHz. To help suppress sidebands, a sideband-suppression filter is added in tandem with the output of the loop's original integrator/filter circuit (b).

Table 1. Filter suppression/phase margin tradeoffs

Circuit	Phase margin	Phase margin deterioration	First-sideband reduction	Second-sideband reduction
Original	44°	—	—	—
RC low-pass RC = 3 x 10^{-4}	32	12°	20 dB	26 dB
Notch filter				
Q = 10	44	0	∞*	0
Q = 1	43	1	∞*	1.5
Q = 0.1	31	13	∞*	16.5
Second-order active				
d = 0.707	34	10	28	40
d = 0.1	42	2	28	40

*Theoretical—actual value about 40 dB.

$$G(j\omega)H(j\omega) = \frac{K_v K_p}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega T_3 + 1}\right], \quad (1)$$

K_p= gain constant of the phase detector,
K_v= VCO sensitivity,

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Table 2. Third-order PLL with two-pole low-pass filter

Display Line	Display Code	Key Entry	Remarks	Registers
00				R_0 ω_o
01	2400	RCL 0		
02	1502	(g) x^2		
03	2407	RCL 7		R_1 T_1
04	1502	(g) x^2		
05	41	—		
06	2304	STO 4		R_2 T_2
07	2403	RCL 3		
08	61	x		
09	2406	RCL 6		R_3 T_3
10	2400	RCL 0		
11	61	x		
12	51	+		R_4
13	2407	RCL 7		
14	61	x		R_5 $\frac{K_v K_p}{N}$
15	2404	RCL 4		
16	2406	RCL 6		
17	2403	RCL 3		
18	61	x		R_6 $2d$
19	2400	RCL 0		
20	61	x		
21	2407	RCL 7		R_7 ω
22	1502	(g) x^2		
23	61	x		
24	41	—		
25	32	CHS		
26	1509	(g)→P		
27	21	x⇄y		
28	2407	RCL 7		
29	2402	RCL 2		
30	61	x		
31	32	CHS		
32	01	1		
33	32	CHS		
34	1509	(g)→P		
35	22	R↓		
36	51	+	∠ Phase margin	
37	74	R/S		
38	22	R↓		
39	71	÷		
40	2405	RCL 5		
41	61	x		
42	2401	RCL 1		
43	71	÷		
44	2407	RCL 7		
45	1502	(g) x^2		
46	71	÷		
47	2400	RCL 0		
48	1502	(g) x^2		
49	61	x	|G S H S|	

Step	Instructions	Input Data/ Units	Keys			Output Data/ Units
1	Enter program					
2	Store	ω_o	STO	0		
		T_1	STO	1		
		T_2	STO	2		
		T_3	STO	3		
		Kv	ENTER			
		Kp	x			
		N	÷	STO	5	
		d	ENTER	2	x	
			STO	6		
3	Enter	ω	STO	7		
4	Calculate		(f)	PRGM	R/S	∠Phase margin
			R/S			|G(s) H(s)|
5	Repeat steps 3 and 4 for other values of frequency, ω					

N = counter divide ratio,
T_1, T_2, T_3= integrator/filter time constants.

Simple but limited

The simplest approach adds in series with the Integrator/Filter an RC low-pass section (Fig. 2a), whose cutoff frequency is larger than the upper end of the loop's bandwidth. For illustration, let the value of RC be 3×10^{-4} s for the frequency-synthesizer example outlined in Fig. 1. (A larger value would reduce sidebands more, but would also decrease the phase margin too much.) With a value of 3×10^{-4} s, the phase margin remains within a "safe" 30°-to-45°.

The open-loop transfer function then becomes:

$$G(j\omega)H(j\omega) = \frac{K_v K_p}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega(T_3+T_4)+1+\omega^2 T_3 T_4}\right], \quad (2)$$

where T_4 is the additional RC time constant.

Solving Eq. 1 at frequencies of 5 and 10 kHz shows that the first sideband (at 5 kHz) is reduced a respectable 20 dB and the second sideband (at 10 kHz) even more to 26 dB. But the phase margin also is reduced to a marginal 32° (Table 1).

However, an active RC notch filter[3] (Fig. 2) gives much more attenuation at the first sideband (5 kHz) and is more flexible in some applications. Its gain is

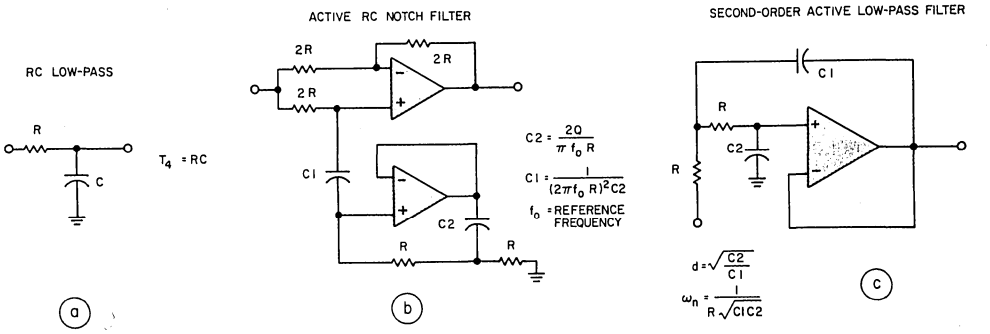
$$A(j\omega) = \frac{1}{j\omega\left[\frac{\omega_o}{Q(\omega^2-\omega_o^2)}\right]+1}, \quad (3)$$

where ω_o= the notch frequency ($2\pi f_o$),
Q= the circuit Q.

The open-loop transfer function, the product of Eqs. 1 and 3, is

$$G(j\omega)H(j\omega) = \frac{K_v K_p}{NT_1\omega^2} \times \left[\frac{-j\omega T_2 - 1}{j\omega\left(T_3 - \frac{\omega_o}{Q(\omega^2-\omega_o^2)}\right)+\omega^2 T_3\left(\frac{\omega_o}{Q(\omega^2-\omega_o^2)}\right)+1}\right], \quad (4)$$

Although the notch frequency ω_o must be fixed at the reference frequency, the value of Q can vary. Theoretically, the reference frequency receives infinite attenuation. Actually, only about 40 dB can be realized, even under ideal conditions. Evaluation of Eq. 4 for Q's of 10, 1 and 0.1 shows that high Q values produce negligible phase-margin deterioration, but



2. **Many filter configurations can be used** to suppress sidebands. The simplest is a low-pass RC circuit (a). Somewhat more flexible is an active RC notch filter (b). But of all filters, a second-order active low-pass filter (c) is most versatile, since two of its parameters are independently adjustable.

attenuation of the second harmonic of the reference frequency is small or zero (Table 1). At a Q of 0.1, however, the second harmonic is reduced 16.5 dB, but then the phase margin suffers.

Most versatile, however, is a second-order, active, low-pass filter with variable damping (Fig. 2c). Its gain (with "s" functions of its more familiar form replaced by $j\omega$) is:[3]

$$A(j\omega) = \frac{\omega_n^2}{-\omega^2+2dj\omega\omega_n+\omega_n^2}, \qquad (5)$$

where ω_n= the filter's natural pole frequency,
d= the filter's damping factor.

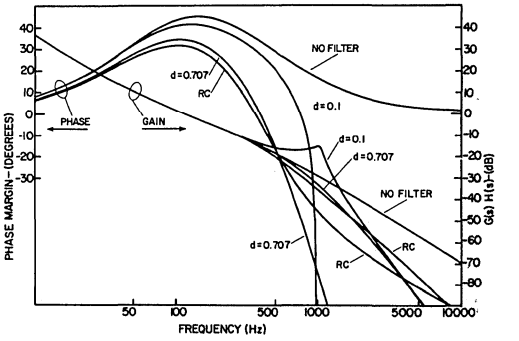
This time, multiplying Eqs. 1 and 5, the over-all open-loop transfer function becomes

$$G(j\omega)H(j\omega) = \frac{\omega_n^2 K_v K_p}{NT_1\omega^2} \times \left[\frac{-j\omega T_2-1}{j\omega[2d\omega_n+T_3(\omega_n^2-\omega)]+[\omega_n^2-\omega^2-2dT_3\omega_n\omega^2]}\right] \qquad (6)$$

If ω_n is chosen to be 6283 ($2\pi \times 1000$) at damping factors of 0.707 (Butterworth response) and 0.1 (16-dB peak Chebyshev), Eq. 6 gives the same sideband attenuation for both damping factors, but the high-ripple Chebyshev deteriorates the phase margin least (Table 1 and Fig. 3).

Since both the pole frequency and the damping factor can be varied in Eq. 5, the circuit it represents is most versatile. Therefore, Eq. 6 is programmed for easy solution on an HP-25 (Table 2) in 49 steps. However, for easier stability evaluation, the program solves directly for the phase margin—the difference between 180° and the open-loop transfer-function angle—rather than the phase angle itself.

Clearly, the simple RC circuit is least efficient. It gives the least sideband attenuation and the largest phase-margin deterioration. The notch filter, although theoretically capable of very high attenuation of the first sidebands only with very small phase-margin deterioration, generally requires component tolerances too critical for other than some special applications. The more complex, active, second-order low-pass filter, however, can be tailored to most applications—illustrating an often observed design phenomenon: the more complex the circuit the better the performance. Of course, then, more complex filter circuits than those used in the examples may offer even better solutions to sideband reduction. ■■



3. **A plot of open-loop gain and phase response** of the system in Fig. 1 compares sideband suppression at 5 and 10 kHz without an extra filter with that of a simple RC and an active, second-order filter.

References

1. Przedpelski, A.B., "Analyze, Don't Estimate, Phase-lock-loop Performance of Type-2, Third-order Systems," *Electronic Design*, May 10, 1978, p. 120.

2. Przedpelski, A.B., "Optimize Phase-lock Loops to Meet Your Needs," *Electronic Design*, Sept. 13, 1978, p. 134.

3. Stout, D.F., and Kaufman, M., *Operational Amplifier Circuit Design*, McGraw-Hill, NY, 1976.

Calculate the noise spectral density and short-term frequency stability in a PLL with a programmable calculator, and vary the parameters to trade off the noise/functional performance requirements.

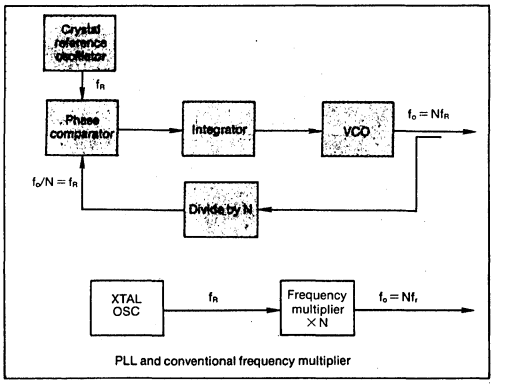
Programmable calculator computes PLL noise, stability

This article is the fourth by the author on phase-locked loops, starting with "Analyze, Don't Estimate, Phase-Lock-Loop Performance" (May 10, 1978, p. 120); then "Optimize Phase-Lock-Loops to Meet Your Needs" (Sept. 13, 1978, p. 134); followed by "Suppress Phase-Lock-Loop Sidebands without Introducing Instability" (Sept. 13, 1979, p. 142).

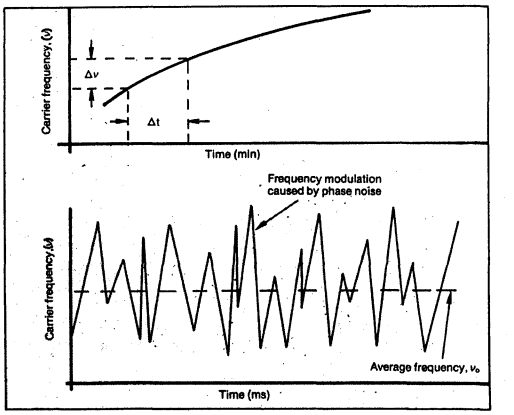
The circuit constants of a phase-lock loop can be optimized not only for performance requirements (acquisition time, sideband levels, step response, and stability, among others), but also for noise output and the resulting short-term (or "instantaneous") frequency stability. Because most other frequency-generation methods lack this versatile performance, and noise and stability control, phase-lock loops (PLLs) are preferable for frequency synthesis. Moreover, a programmable HP-19C (or 21C) calculator with the proper program makes the design tradeoffs between noise effects and functional performance requirements relatively easy to determine.

A properly designed frequency synthesizer derived from a PLL (Fig. 1, top) will offer a high degree of flexibility and long-term frequency stability. In a PLL, the frequency of the stable reference oscillator (say, a quartz-crystal circuit) can be multiplied by a precisely controlled factor over a very wide range. Although the PLL may seem more complicated than the conventional so-called frequency-multiplier circuit (Fig. 1, bottom), in practice, the PLL is more efficient, more compact, and considerably wider in bandwidth. All the advantages increase as the multiplication factor increases.

In most PLL frequency synthesizers, the primary concern is the functional performance—a problem that has been treated extensively.[1] Even the theoretical aspects of phase noise in low-noise signal sources have been extensively covered.[2,3,4] However,



1. Although the PLL frequency multiplier (top) looks more complex than the conventional multiplier (bottom), it is in fact more compact and more flexible, and can handle a much wider frequency range.



2. Short-term frequency stability can be far worse (bottom) than the long-term average of a PLL system (top).

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specific methods for calculating the noise and short-term frequency stability and details of the tradeoffs are generally not available, except for some recent work by the National Bureau of Standards on low-noise signal sources.[5,6,7]

Short-term (or "instantaneously" sampled) frequency stability, in the millisecond range, is particularly important for accuracy in position-finding applications, as in LORAN navigation and various radar and sonar Doppler systems. Even though frequency drift over a short time generally is less than the average long-term frequency drift, instantaneously measured samples show much wider variations in the frequency swings caused by phase noise in the signal source (Fig. 2).

The overall phase-noise, or spectral-density output, $S_{\phi(\omega)0}$, of a PLL[8] is found by

$$S_{\phi(\omega)0} = S_{\phi(\omega)VCO}\left|\frac{1}{1+G(\omega)H(\omega)}\right|^2 + S_{\phi(\omega)REF}\left|\frac{G(\omega)}{1+G(\omega)H(\omega)}\right|^2,$$

where $S_{\phi(\omega)VCO}$ is the open-loop spectral density of phase fluctuations in the PLL's voltage-controlled oscillator (VCO) and $S_{\phi(\omega)REF}$ is the equivalent spectral density of fluctuations in the reference oscillator. These phase fluctuations are measured in rad²/Hz, but generally plotted in dBc, which is $10 \log_{10} S_{\phi(\omega)}$. More commonly, however, vendor-supplied phase-noise data, designated $\mathcal{L}(\omega)$, and also measured in dBc, are for single-sideband noise. (The dBc designation is defined as $10 \log_{10}$ of the ratio between the output from a spectrum analyzer with a 1-Hz bandwidth and the signal's carrier level.) Accordingly,

$$\mathcal{L}(\omega) = 10 \log_{10}(\tfrac{1}{2})S_{\phi(\omega)} \text{ (per rad}^2\text{)},$$

assuming that

$$\mathcal{L}(-\omega) = \mathcal{L}(\omega).$$

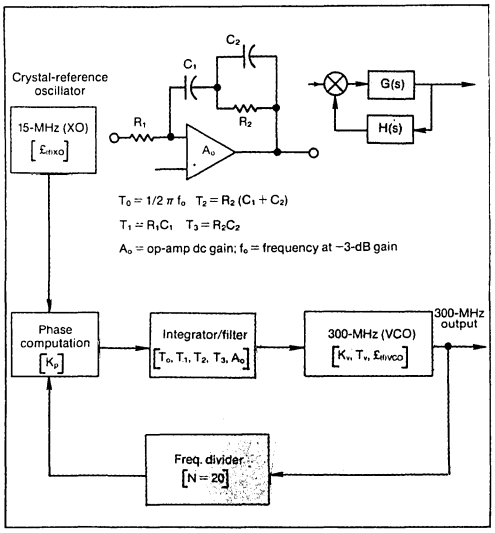
Therefore, to convert $\mathcal{L}(\omega)$ data to "straight" $S_{\phi(\omega)}$ data, add 3 dB to the $\mathcal{L}(\omega)$ data and take the antilog.

An HP-19C program (see "Noise in a 5th-order PLL") calculates this single-sideband noise, where $G(\omega)H(\omega)$ is the open-loop gain of the PLL.[1] The feedback path, $H(\omega)$, is simply 1/N; and $G(\omega)$ equals

$$\frac{(K_pK_v/\omega T_1)\ (jwT_2 + 1)}{j\left[\omega^2(\omega^2 \frac{T_o}{A_o} T_vT_3 - T_3 - T_v) + \frac{1}{A_oT_1}\right] + \omega(\omega^2T_vT_3 - 1)}$$

Optimized for functional performance, the following circuit constants are used for a typical PLL (Fig. 3):

$A_o = 320{,}000$
$T_o = 7.96 \times 10^{-4}$ s
$T_v = 1.59 \times 10^{-7}$ s
$T_1 = 2.408 \times 10^{-5}$ s
$T_2 = 2.491 \times 10^{-6}$ s
$T_3 = 4.700 \times 10^{-7}$ s
$K_p = 314 \times 10^6$ V/rad
$K_v = 0.16$ rad/V
$N = 20$.



3. For a fifth-order PLL, four of the time constants are determined by the integrator/filter circuit, and the fifth is determined by the VCO.

The single-sideband phase noise, when calculated by the program for a range of so-called Fourier frequencies (offsets from a carrier, $f = \omega/2\pi$), can be plotted as in Fig. 4 (dotted line). Although this output phase noise can be reduced by varying circuit constants to increase the loop's bandwidth, proceed with caution, because other desirable operating characteristics (such as circuit stability or speed of response) could be compromised. The program, however, offers an easy way to determine how systematic changes in the parameters affect noise.

Oscillator noise should be low

In addition to the calculated PLL noise, Fig. 4 shows a plot of the SSB-noise characteristics of the circuit's VCO and crystal-reference oscillator. The oscillators are the main source of phase noise in a PLL. The information for plotting their noise can be obtained from the manufacturers of the oscillators, or from measurements made by the user.

Where noise reduction is of prime importance, select oscillators that generate minimum noise and have noise spectral densities that complement each other (as in Fig. 5). The point at which the two curves

Noise in 5th order PLL

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Enter program			
2	Store	T_0	STO 0	
		T_1	STO 1	
		T_2	STO 2	
		T_3	STO 3	
		T_V	STO 4	
		Kp	STO 5	
		Kvo	STO 6	
		N	STO 7	
		Ao	STO 8	
		180	STO 9	
		10	STO .5	
3	Calculate	f	GSB 0	
		$S\phi ref$	R/S	
		$S\phi vto$	R/S	$S\phi o$
4	Repeat step 3 for other Fourier frequencies			

Note: Enter $S\phi ref$ and $S\phi vto$ in dB. $S\phi o$ answer is in dB.

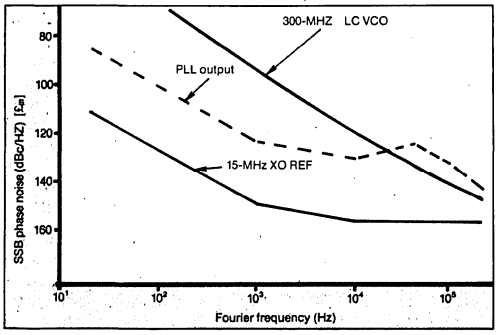
Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 0	25 14 00	050	RCL 9	55 09
002	PRx	65	051	—	31
003	(g) DEG	25 24	052	STO .1	45 .1
004	(g)π	25 63	053	R↓	12
005	x	51	054	÷	61
006	2	02	055	RCL 5	55 05
007	x	51	056	x	51
008	STO .0	45 .0	057	RCL 6	55 06
009	(g) x²	25 53	058	x	51
010	RCL 0	55 00	059	RCL 7	55 07
011	x	51	060	÷	61
012	RCL 8	55 08	061	RCL 1	55 01
013	÷	61	062	÷	61
014	RCL 4	55 04	063	RCL .0	55 .0
015	x	51	064	÷	61
016	RCL 3	55 03	065	STO .2	45 .2
017	x	51	066	RCL .1	55 .1
018	RCL 3	55 03	067	x ⇄ y	11
019	—	31	068	(f) → R	16 34
020	RCL 4	55 04	069	1	01
021	—	31	070	+	41
022	RCL .0	55 .0	071	(g) → P	25 34
023	(g) x²	25 53	072	(g) 1/x	25 64
024	x	51	073	STO .3	45 .3
025	RCL 8	55 08	074	RCL .2	55 .2
026	RCL 1	55 01	075	RCL 7	55 07
027	x	51	076	x	51
028	(g) 1/x	25 64	077	x	51
029	+	41	078	STO .4	45 .4
030	RCL .0	55 .0	079	(g) x²	25 53
031	(g) x²	25 53	080	R/S	64
032	RCL 3	55 03	081	RCL .5	55 .5
033	x	51	082	÷	61
034	RCL 4	55 04	083	(g) 10^x	25 33
035	x	51	084	x	51
036	1	01	085	RCL .3	55 .3
037	—	31	086	(g) x²	25 53
038	RCL .0	55 .0	087	R/S	64
039	x	51	088	RCL .5	55 .5
040	CHS	22	089	÷	61
041	(g) →P	25 34	090	(g) 10^x	25 33
042	x ⇄ y	11	091	x	51
043	RCL 2	55 02	092	+	41
044	RCL .0	55 .0	093	(f) log	16 33
045	x	51	094	RCL .5	55 .5
046	1	01	095	x	51
047	(g) → P	25 34	096	PRx	65
048	R↓	12	097	(g) SPC	25 65
049	+	41	098	(g) RTN	25 13

REGISTERS

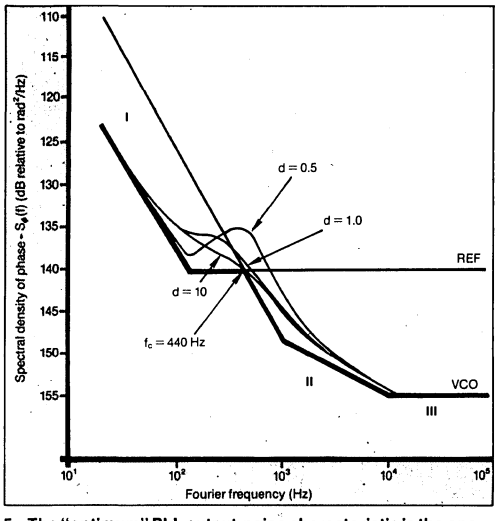
0 T_0	1 T_1	2 T_2	3 T_3	4 T_V	5 Kp	6 Kvo	7 N	8 Ao	9 180
S0	S1	S2	S3	S4	.5 10	S6	S7	S8	S9

cross is called the crossover frequency (f_c). This frequency is an important parameter for optimizing a PLL's noise characteristics.

In Fig. 5, the VCO noise-distribution plot is divided into three characteristic regions. High-quality oscillators generally exhibit this spectral-density relationship. In region I, $S_{\phi(f)}$ is typically proportional to $1/f^3$, so-called flicker-frequency noise; in region II, $S_{\phi(f)}$ is proportional to $1/f^2$, so-called white-frequency noise; and in region III, $S_{\phi(c)}$ is constant, so-called white-phase noise. Beyond region III, the bandwidth limitation of the circuit attenuates the noise to negligible levels.



4. A PLL is optimized for performance characteristics, such as stability, response time, and sideband levels; but the noise characteristics generally fall where they may, as exemplified in this plot of a fifth-order PLL.



5. The "optimum" PLL output-noise characteristic is the one that coincides most closely with the PLL's intersecting reference crystal oscillator and VCO-oscillator noise characteristics (heavy lines). A high damping-factor value (such as d = 10) makes the best correspondence with this criterion.

Region I noise stems from fluctuations in oscillator-circuit frequency-control components; region II, from thermal noise in the oscillator's gain element; and region III, from additive thermal noise from other elements of the circuit (including the gain element).

A plot of the optimum phase-noise characteristic of a PLL would coincide with the lower parts of the two oscillator curves (heavy lines in Fig. 5).

The type-2, second-order PLL circuit in Fig. 6 helps to illustrate how closely this condition can be approached. This circuit can be generalized by relating the integrator's time constants (T_1 and T_2) and the VCO's and phase comparator's transfer coefficients (K_v and K_p) with a damping factor (d), and with the reference and VCO crossover frequency ($f_c = \omega_c/2\pi$), as follows:

$$\begin{aligned} d &= (T/2)\sqrt{K_pK_v/T_1};\ d>>1 \\ T_2 &= 4d^2/\omega_c \\ T_1 &= T_2K_pK_v/\omega_c. \end{aligned}$$

When these circuit parameters are considered together with the circuit's open-loop gain (note: $H(\omega) = 1$),

$$G(\omega)H(\omega) = \frac{K_pK_v}{T_1\omega^2}(-j\omega T_2 - 1),$$

and substituted in the phase-noise equation for $S_{\phi(\omega)0}$, the PLL's spectral density becomes

$$S_{\phi(\omega)0} = S_{\phi(\omega)VCO}\left[\frac{1}{\left(1-\frac{\omega_c^2}{4d^2\omega^2}\right)+\left(\frac{\omega_c^2}{\omega}\right)}\right]+$$

$$S_{\phi(\omega)REF}\left[\frac{\left(\frac{1}{2d}\right)^2\left(\frac{\omega_c}{\omega}\right)^2+\left(\frac{\omega_c}{\omega}\right)^2}{\left(1-\frac{\omega_c^2}{4d^2\omega^2}\right)+\left(\frac{\omega_c}{\omega}\right)^2}\right]$$

The "Optimizing PLL Phase Noise" program, with its subroutine 0, solves this equation for any Fourier frequency ($f = \omega/2\pi$). In Fig. 5, solutions are shown for damping-factor values (d) of 0.5, 1.0, and 10.

The largest damping factor (d = 10) causes the noise curve to approach the "optimum" noise characteristic most closely—when it lies completely between the VCO/reference-oscillator lines and as closely as possible to the lower lines. To satisfy this criterion, the curve generally passes through the frequency crossover point previously mentioned. Larger damping values than 10 will provide little further improvement. In fact, a larger damping value would slow response more than it would lower the noise output. Special cases may require low damping

Optimizing PLL phase noise

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Enter program			
2	Store	fc	STO 2	
		d	STO 3	
		K_p	STO 7	
		K_v	STO 8	
3	Calculate phase noise	f	GSB 0	
		$S\phi_{vco}$	R/S	
		$S\phi_{ref}$	R/S	$S\phi_o$
4	Repeat step 3 for other values of Fourier frequency			
5	Calculate time constants		GSB 1	T1 T2

Note: —Sϕvco, Sϕref and Sϕo in dB

Subroutine 0 must be performed before the time constants can be calculated with subroutine 1

Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 0	25 14 00	038	(g) x^2	25 53
002	PRx	65	039	RCL 4	55 04
003	(g)π	25 63	040	+	41
004	x	51	041	RCL 5	55 05
005	2	02	042	÷	61
006	x	51	043	R/S	64
007	(g) 1/x	25 64	044	1	01
008	RCL 2	55 02	045	0	00
009	(g)π	25 63	046	+	61
010	x	51	047	(g) 10^x	25 33
011	2	02	048	x	51
012	x	51	049	+	41
013	STO 1	45 01	050	(f) log	16 33
014	x	51	051	1	01
015	(g) x^2	25 53	052	0	00
016	STO 4	45 04	053	x	51
017	RCL 3	55 03	054	PRx	65
018	(g) x^2	25 53	055	(g) SPC	25 65
019	÷	61	056	(g) RTN	25 13
020	4	04	057	(g) LBL 1	25 14 01
021	÷	61	058	RCL 3	55 03
022	STO 6	45 06	059	(g) x^2	25 53
023	CHS	22	060	4	04
024	1	01	061	x	51
025	+	41	062	RCL 1	55 01
026	(g) x^2	25 53	063	+	61
027	RCL 4	55 04	064	PRx	65
028	+	41	065	RCL 7	55 07
029	STO 5	45 05	066	x	51
030	(g) 1/x	25 64	067	RCL 8	55 08
031	R/S	64	068	x	51
032	1	01	069	RCL 1	55 01
033	0	00	070	÷	61
034	÷	61	071	PRx	65
035	(g) 10^x	25 33	072	(g) SPC	25 65
036	x	51	073	(g) RTN	25 13
037	RCL 6	55 06			

REGISTERS

0	1	2	3	4	5	6	7	8	9
		f_c	d				K_p	K_v	

factors—a value of 1 or even 0.5—to get a faster response or the special noise-distribution shapes that these lower damping factors produce.

After the phase-noise characteristics (based on the f_c of the oscillators and a selected damping factor) have been calculated, a second part of the optimizing program (subroutine 1) can then be used to calculate the time constants T_1 and T_2 for the given K_p and K_v of a type-2 second-order PLL.

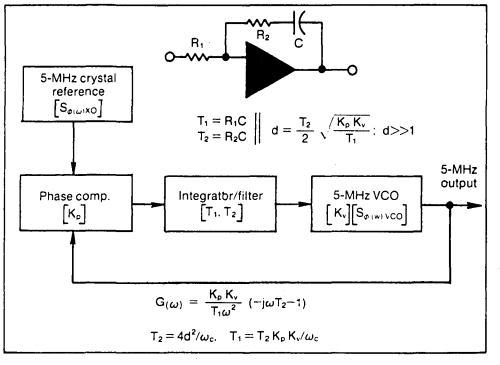
Determining a PLL's short-term frequency stability requires integration of the spectral density of the phase fluctuations to obtain the so-called Allan variance (a dimensionless measure of stability, where σ_y^2 is $\Delta f/f$ in a short sample period). Thus

$$\sigma_y^2(\tau, f_h) = \frac{2}{(\tau\nu\pi)^2} \int_0^{f_h} S_{\phi(f)} \sin^4(\pi f \tau) df,$$

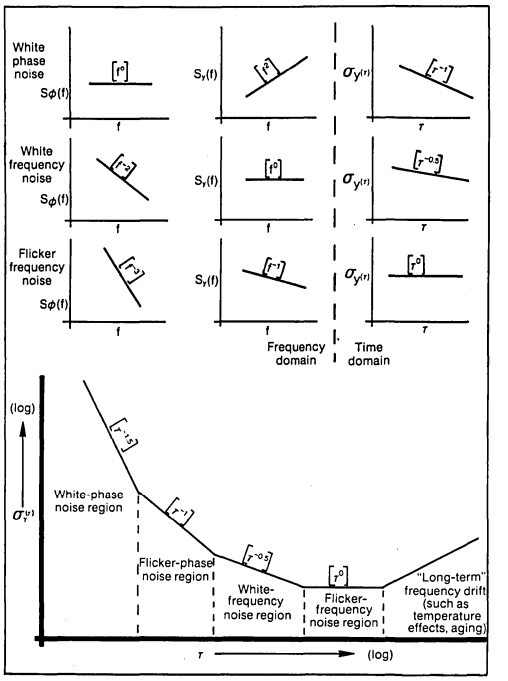
where τ is the sampling time (in seconds), ν is the long-term average frequency (in Hz), and f_h is the bandwidth, or maximum excursion of the offset from the carrier (the maximum Fourier frequency).

Figure 7 (top) shows the relationship between frequency or phase and the frequency spectral-noise densities, along with the resultant short-term frequency stabilities, for several distinct types of phase or frequency noise. A typical complex signal source (such as a PLL) could have a combined short-term frequency stability as in Fig. 7 (bottom). But such noise types generally do not obey simple integer-power curves and, therefore, pose a problem: The Allan equation does not have a closed-form solution for fractional powers, so it cannot be used directly. Nevertheless, very accurate answers can be obtained with Simpson's Rule and a programmable calculator.

Although the Allan equation requires integration over the Fourier frequency range of 0 to f_h, the low-frequency limit of 0 Hz cannot be used in a log-log Simpson's Rule integration. Fortunately, frequencies below $(2\pi\tau_h)^{-1}$, where τ_h is the longest sampling time, do not contribute appreciably to the value of the Allan variance. The longest sampling time for short-term effects is generally 1 s; therefore, for a measuring-system bandwidth of 1000 Hz, just the Fourier frequencies between about 0.16 and an f_h of 1000 Hz need be considered. (Since the manufacturer did not supply data below 2 Hz for the reference oscillator and VCO used in Fig. 5; a new oscillator with data to 0.1 Hz was substituted in Fig. 8, top.)



6. The phase-output noise in this type-2 second-order PLL can be optimized by adjusting the damping factor (d) in relation to the oscillator-noise crossover frequency (f_c).



7. The distribution of the different types of frequency and phase noise can be expressed as line segments that represent powers of frequency or time (top), and the overall distribution of a system can be shown by combining appropriate segments (bottom).

As shown in Fig. 7 (bottom) and Fig. 8 (top), the phase-noise curves can be approximated with straight-line segments. The segments are plotted on semilog paper with $S_{\phi(f)}$ measured in dBc on the vertical axis. Therefore, the segments,

$$y = ax^b,$$

can be established from the end points on their phase-noise curves—where $S_{\phi(f_1)}$ and $S_{\phi(f_2)}$ correspond to the low-frequency (f_1) and the high-frequency (f_2) end points, as follows:

and

$$b = \frac{S_{\phi(f_1)} - S_{\phi(f_2)}}{10\,(\log f_1 - \log f_2)}$$

Allan variance calculations

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Key in the program			
2	Store	b	STO 7	
		α	STO .1	
		υ	STO .0	
		τ	STO 8	
3	Enter and start program	f_1	ENT ↑	
		f_2	ENT ↑	
		n	GSB .3	$\sigma^2 y$

Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 7	25 14 07	044	RCL 4	55 04
002	RCL 4	55 04	045	STO + 5	45 41 05
003	x	51	046	RCL 5	55 05
004	x ≠ y	11	047	GSB 0	13 00
005	÷	61	048	GSB 6	13 06
006	GTO 2	14 02	049	(g) RTN	25 13
007	(g) LBL 6	25 14 06	050	(g) LBL 5	25 14 05
008	ENT ↑	21	051	3	03
009	+	41	052	RCL 0	55 00
010	STO + 0	45 41 00	053	GTO 7	14 07
011	(g) RTN	25 13	054	(g) LBL 0	25 14 00
012	(g) LBL 3	25 14 03	055	(g) RAD	25 23
013	STO 3	45 03	056	STO 6	45 06
014	R ↓	12	057	(g) π	25 63
015	STO 2	45 02	058	x	51
016	R ↓	12	059	RCL 8	55 08
017	STO 1	45 01	060	x	51
018	GSB 0	13 00	061	(f) sin	16 42
019	STO 0	45 00	062	(g) x^2	25 53
020	RCL 2	55 02	063	(g) x^2	25 53
021	GSB 0	13 00	064	RCL 6	55 06
022	STO + 0	45 41 00	065	RCL 7	55 07
023	RCL 2	55 02	066	(f) y^x	16 54
024	RCL 1	55 01	067	x	51
025	STO 5	45 05	068	(g) DEG	25 24
026	—	31	069	(g) RTN	25 13
027	RCL 3	55 03	070	(g) LBL 2	25 14 02
028	+	61	071	(g) π	25 63
029	STO 4	45 04	072	RCL 8	55 08
030	0	00	073	x	51
031	STO 9	45 09	074	RCL .0	55 .0
032	(g) LBL 8	25 14 08	075	x	51
033	GSB 4	13 04	076	(g) x^2	25 53
034	STO + 0	45 41 00	077	(g) 1/x	25 64
035	2	02	078	x	51
036	STO + 9	45 41 09	079	2	02
037	RCL 3	55 03	080	x	51
038	RCL 9	55 09	081	RCL .1	55 .1
039	(f) x = y	16 61	082	x	51
040	GTO 5	14 05	083	PRx	65
041	GSB 4	13 04	084	(g) SPC	25 65
042	GTO 8	14 08	085	(g) RTN	25 13
043	(g) LBL 4	25 14 04			

REGISTERS

0	1	2	3	4	5	6	7	8	9
							b	τ	
.0	.1	.2	.3	.4	.5	S6	S7	S8	S9
υ	α								

PLL noise and stability

$$a = 10^{\left(\frac{S_{\phi}(f_1) - 10\ b \log f_1}{10}\right)}.$$

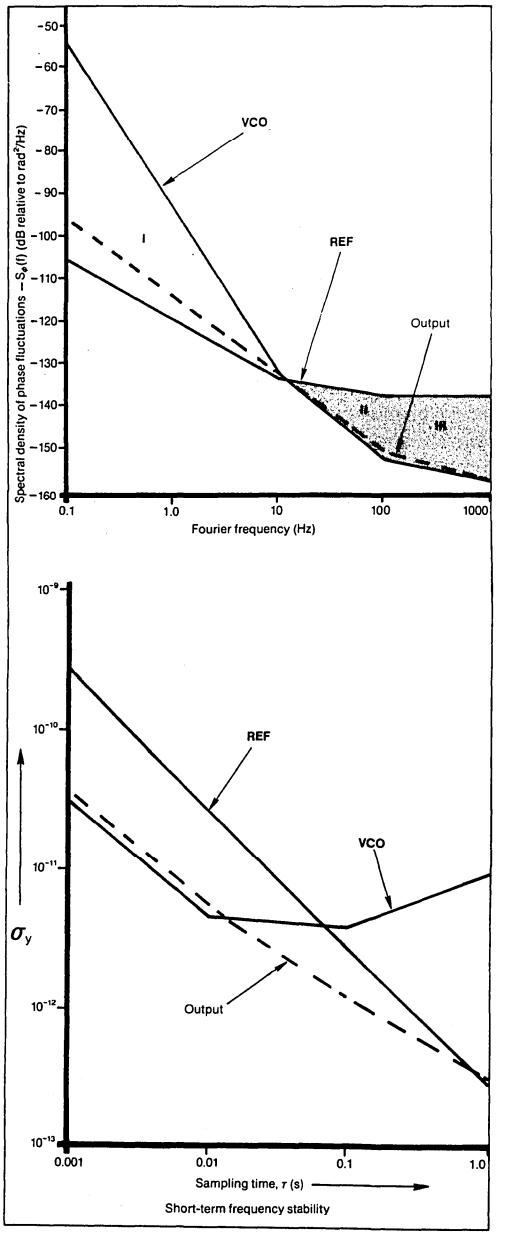
With coefficients a and b established for each line segment, the contributions of each segment to the overall Allan variance σ_y^2 can be calculated with the approximate Allan equation,

$$\sigma_y^2(\tau,f) = \frac{2a}{(\tau\nu\pi)^2} \int_{f_1}^{f_2} f^b \sin^4(\pi f \tau) df,$$

by a modified Simpson's Rule program supplied by Hewlett-Packard (HP-19C/29C *Applications' Book*, 1977). The Simpson's Rule is incorporated into the

Calculated short-term stability

Device	Segment I			
Reference oscillator	f_1 = 0.1 Hz, f_2 = 10 Hz a = 1.26×10^{-12}, b = −1.40			
	T/n	0.001/10	0.01/10	0.1/20	1/100
	σy^2	1.10×10^{-27}	1.05×10^{-25}	4.80×10^{-25}	1.76×10^{-26}
Voltage-controlled oscillator	f_1 = 0.1 Hz, f_2 = 10 Hz a = 5.01×10^{-10}, b = −3.90			
	T/n	0.001/10	0.01/10	0.1/20	1/100
	σy^2	4.49×10^{-27}	4.39×10^{-25}	1.34×10^{-23}	8.10×10^{-23}
PLL output	f_1 = 0.1 Hz, f_2 = 100 Hz a = 4.64×10^{-12}, b = −1.83			
	T/n	0.001/10	0.01/20	0.1/100	1/1000
	σy^2	2.43×10^{-24}	1.46×10^{-23}	1.19×10^{-24}	8.21×10^{-26}
Device	**Segment II**			
Reference oscillator	f_1 = 10 Hz, f_2 = 100 Hz a = 1.26×10^{-13}, b = −0.40			
	T/n	0.001/10	0.01/20	0.1/100	1/1000
	σy^2	3.27×10^{-23}	8.22×10^{-23}	7.56×10^{-25}	7.56×10^{-27}
Voltage-controlled oscillator	f_1 = 10 Hz, f_2 = 100 Hz a = 6.31×10^{-12}, b = −2.00			
	T/n	0.001/10	0.01/20	0.1/100	1/1000
	σy^2	1.59×10^{-24}	1.06×10^{-23}	1.63×10^{-25}	1.27×10^{-27}
PLL output	f_1 = 100 Hz, f_2 = 1000 Hz a = 2.51×10^{-14}, b = −0.70			
	T/n	0.001/20	0.01/100	0.1/1000	1/10,000
	σy^2	1.04×10^{-21}	1.00×10^{-23}	1.01×10^{-25}	1.01×10^{-27}
Device	**Segment III**			
Reference oscillator	f_1 = 100 Hz, f_2 = 1000 Hz a = 2.00×10^{-14}, b = 0.00			
	T/n	0.001/20	0.01/100	0.1/1000	1/10,000
	σy^2	6.08×10^{-20}	5.47×10^{-22}	5.47×10^{-24}	5.47×10^{-26}
Voltage-controlled oscillator	f_1 = 100 Hz, f_2 = 1000 Hz a = 6.31×10^{-15}, b = −0.50			
	T/n	0.001/20	0/01/100	0.1/1000	1/10,000
	σy^2	8.88×10^{-22}	8.27×10^{-24}	8.28×10^{-26}	



8. The phase-noise characteristics of the reference oscillator and the VCO can be expressed with three straight-line segments (I, II, and III); and the PLL output, by two (top). The short-term stability in terms of the Allan variance can then be calculated by keying the required coefficients as determined from the coordinates of these line-segment ends into the calculator (see Table) and plotting the results (bottom).

complete program for an HP-19C calculator—"Allan Variance Calculations." With a, b, ν, and τ established, the only decision remaining is the number of intervals, n, into which the segments must be divided. The more intervals chosen, the more accurate the calculation, but the longer the calculation takes. A good choice for a minimum n value (which must be an even number) is

$$n \geq 10\ [\tau(f_2 - f_1)].$$

The calculation time, then, is 0.056 n + 0.15 min.

To illustrate an application of the Allan variance calculations, the (a and b) program coefficients for the straight-line segments making up the VCO, reference oscillator, and overall output noise were determined from Fig. 8 (top). The coefficients are listed in the "Calculated Short-term Stability" table. Sample times of 1, 10, 100, and 1000 ms and end frequencies of 0.1, 10, and 1000 Hz were employed.

With these inputs, σ_y^2 was determined with the Allan variance program. The frequency stability,

$$\sigma_y(\tau) = \sqrt{\Sigma\sigma_y^2(\tau, f_h)},$$

was calculated, after summing the individual σ_y^2 contributions of each segment. A plot of σ_y vs sampling time for the VCO, reference, and output is shown in Fig. 8 (bottom).□

Acknowledgments

The author wishes to thank Dr. D. Halford and Dr. Fred L. Walls of the National Bureau of Standards, whose constructive discussions contributed to a more insightful understanding of the problems involved in working with PLL noise and short-term frequency stability.

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Remote Control

Application Notes and Technical Articles

4

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MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

AN806A
Application Note

OPERATION OF THE MC14469

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The MC14469 is an addressable asynchronous receiver transmitter that finds applications in control of remote devices, transfer of data to and from remote locations on a shared wire and as an interface from remote sensors to a central processor.

OPERATION OF THE MC14469

The MC14469 is an asynchronous receiver/transmitter fabricated in metal-gate CMOS technology. The asynchronous data format consists of a serial stream of data bits, preceded by a start bit and followed by one or more stop bits. The asynchronous data format is used to eliminate the need to transmit the system clock along with the data bit stream. The fact that the MC14469 is made in CMOS technology means that it offers the high noise immunity and low power consumption characteristic of this technology.

The MC14469 can receive one or two eleven-bit words in a serial data stream. The first received word contains a seven-bit address and if it matches the programmed address of the receiver, the transmitter can be enabled to transmit its two data words. The 7 bits of the received address word must correlate bit by bit with the 7 address pins of the MC14469. A second word may optionally be received for data or control use. This word will contain seven data bits which will be latched onto the command data outputs if it has a valid command format. With 7 address lines, 2^7 or 128 separate units may be interconnected for simplex or full duplex data transmission. The MC14469 is capable of operation at data rates in excess of 30,000 baud controlled by an on chip oscillator. Applications include transmitting data from remote A/D converters, temperature sensors, or remote digital transducers as well as single line control of remote devices such as motors, lights or security devices.

DEVICE OPERATION

As shown in the block diagram of Figure 1, the MC14469 consists of three different sections: the receiver, the transmitter, and the oscillator. The receiver must receive (at least) a valid address on its receive data input (pin 19) in order to set up the necessary internal conditions to allow the transmitter to transmit its two data words. The address word consists of a start bit, seven address bits, the address identifier, an even parity bit and a stop bit. The address will be valid only if: a) the seven address bits match the address that is programmed on input pins A0 through A6, b) if the address identifier is high, and c) if the state of the parity bit causes the total number of ones in the address word, including the address identifier and parity bit, to be even. After reception of a valid address, the MC14469 can optionally receive a command word. Similar to the address word, the command consists of a start bit, seven data bits, a command identifier, an even parity bit and a stop bit. The command will be valid if the command identifier is low and the total number of ones, including the parity bit, is even. The reception of either a valid address or both valid address and a valid command can be used to set up the necessary internal conditions for transmission. The format of address and command words is shown in Figure 2.

Upon receipt of a valid address data stream, the MC14469 generates a valid address pulse (VAP) which in turn sets the internal valid address latch (VAL) and the internal send enable latch (SEL). See Figure 3 for a timing diagram. SEL remains high for eight data bit times or until the send input (pin 30) is taken high. If SEL is allowed to time out and a valid command word is subsequently received, a command strobe (CS) is generated which sets SEL high again. It again remains high for eight data bit times after being set. However, once the valid address latch (VAL) is set high, it will remain high until SEND goes high and resets it.

In order for the MC14469 to transmit its two data words, SEND must receive a rising edge while the valid address latch and send enable latch are both set high. Therefore, a send input must occur within eight bit times after the generation of either a valid address pulse or a command strobe, depending on the system configuration. After eight bit times, SEL will time out and transmission will be inhibited.

Figure 1A. MC14469 Block Diagram

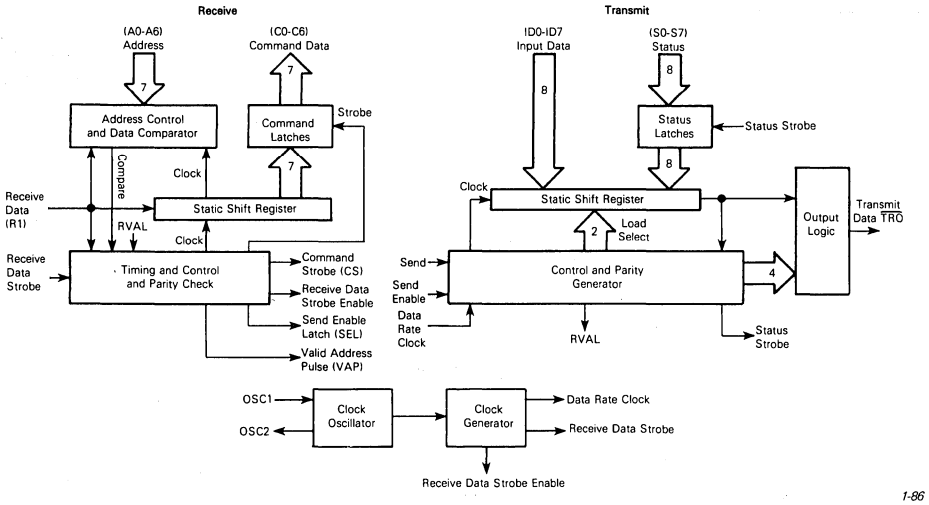

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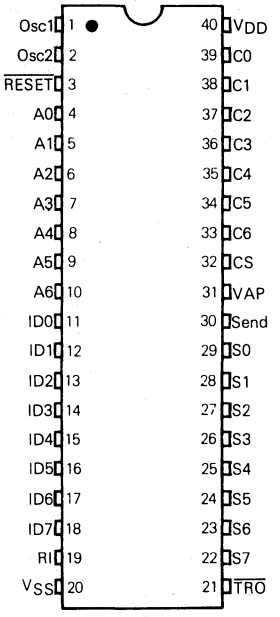
Figure 1B. Pin Assignments



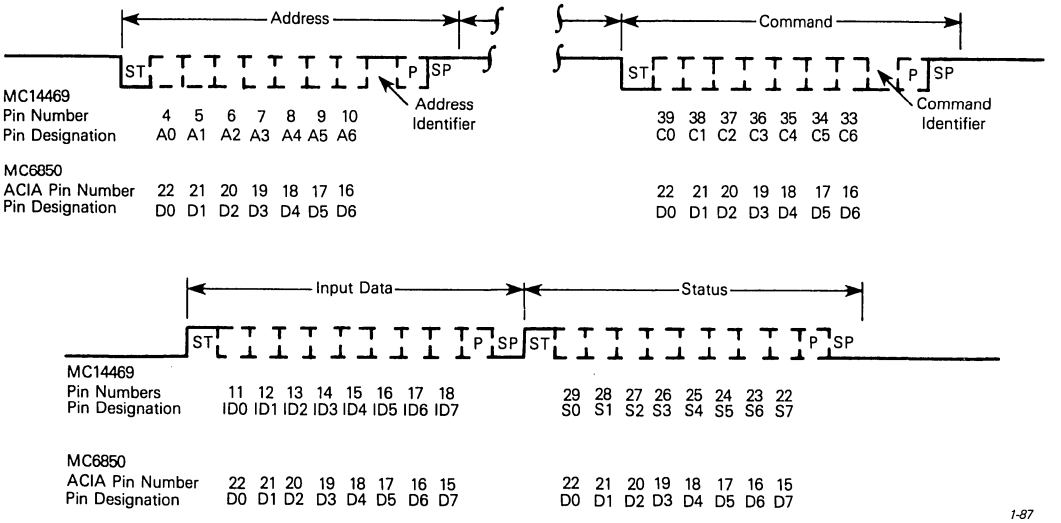
SEND going high resets VAL and SEL, and initiates the transmission of the data defined by input pins 11-18 and the status word defined by input pins 22-29. The transmitted words each contain a start bit, eight data bits, an even parity bit and a stop bit, all in UART compatible format. The transmitted data has the format shown in Figure 3. Note that the transmitted data must be inverted before being presented to the receiving device. This is usually accomplished by the line driver or transistor used to drive the common transmit wire.

OSCILLATOR OPERATION

The oscillator can be controlled by a ceramic resonator, a crystal or by an externally generated clock, and will typically operate at frequencies up to 2 MHz at a V_{DD} of 12 V. The oscillator frequency is divided by 64 to derive the receive data strobe and the data rate clock. Thus, the data bit period is 64 times the oscillator period. To allow for maximum phase jitter, the receive data strobe is centered at the middle of each data bit. The receipt of a start bit initiates the receive data strobe and synchronizes the strobe to the receive data bit stream.

Since data is sent asynchronously, the transmit oscillator and receive oscillator must be the same frequency to ensure that the receive data strobe occurs at the middle of the bit period. The maximum permissible variation in oscillator frequency between a transmitting unit and a receiving unit can be such that over the entire receive data word time the total error is plus or minus one-half data bit period.

Figure 2A. Data Format



1-87

Note: Pin numbers apply to plastic DIP only.

Figure 2B. Example Data Words

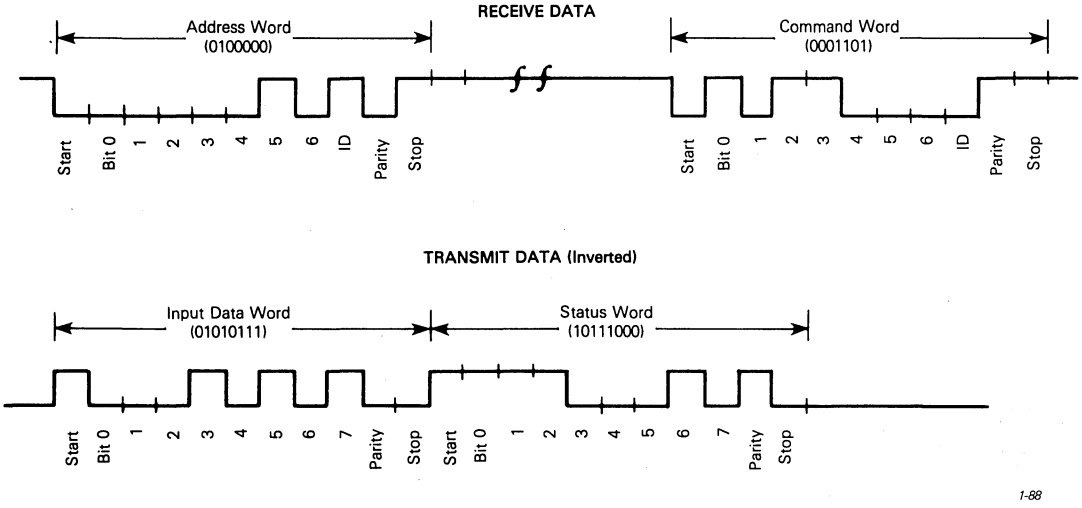


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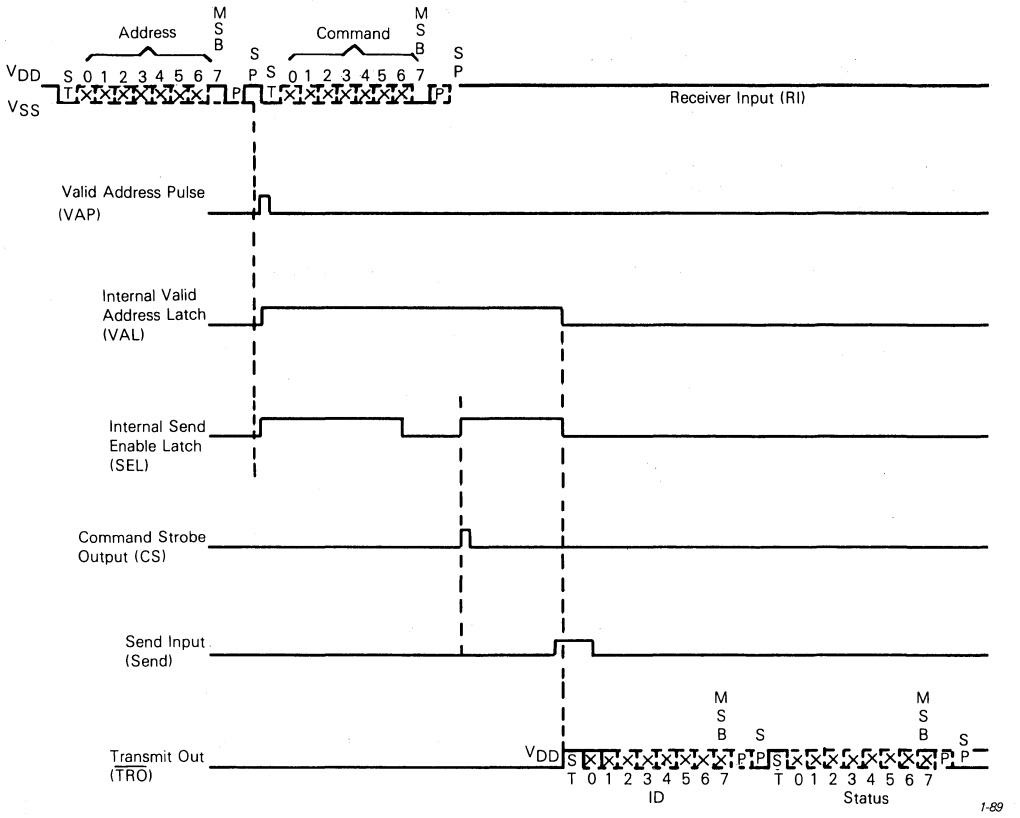
Figure 3. Typical Receive/Send Cycle



Each received data word consists of 11 bits, and thus the variation in oscillators cannot be more than half a bit time divided by 11 bit times or 4.5%.

The internal oscillator active circuitry consists of a normal CMOS inverter. When a high value resistor is used to provide DC feedback, the inverter is biased into its linear region and acts as an AC simplifier. The size of the feedback resistor is unimportant but needs to be small enough to overcome leakages and large enough to not load the oscillator output. Values in the range of 1 MΩ to 22 MΩ are common.

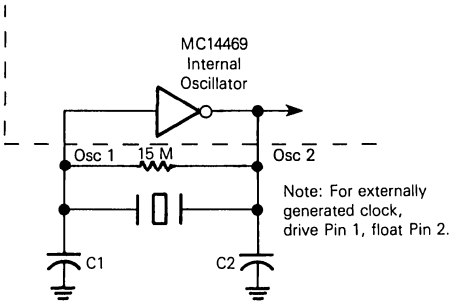
With the inverter biased as an AC amplifier the usual oscillator design is the Pierce type oscillator using a parallel resonant crystal. See Figure 4. Two capacitors, one from input to ground and one from output to ground, present the required capacitive load to the crystal. The series connection of the capacitors through ground avoids feedback of signal through the parallel capacitive path. An inductor or ceramic resonator can be substituted for the crystal to form a Colpitts oscillator ususally at less cost than a crystal but at the expense of frequency stability.

MODES OF OPERATION

The various modes of operation of the MC14469 are discussed below. For most applications, the send input is tied to either VAP or CS for fully automatic operations. If this is not done, the send input must receive a rising edge within eight bit times after VAP or CS in order for a transmission to occur.

It is possible to operate the MC14469 in a receive only mode by tying SEND to V_{SS}. The device can receive valid address words only or both address and command words. Three different modes of operation of the MC14469 are possible depending on the signal used to drive the SEND input. These are RECEIVE ONLY MODE, SEND EQUALS VAP and SEND EQUALS CS.

Figure 4. Oscillator Circuit



Note: Ceramic Resonators
307.2 kHz ±1 kHz for 4800 Baud Rate
C1≈50 pF
C2≈200 pF

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RECEIVE ONLY MODE

If the MC14469 is in the receive only mode (i.e., if SEND is tied to V_{SS}) and if it is receiving valid address words only, it will respond with a valid address pulse after every other valid address. The intervening addresses will cause no output. The reason for this can be seen by examining the flow chart (Figure 5).

Assume the MC14469 has been reset, the receiver is initialized and is ready to be addressed. If the MSB of the first word received is a one (signifying an address), the device checks to see if the valid address and send enable latches are set. If neither is set, and if the word is a valid address, VAL and SEL are set and a valid address pulse is generated. If SEND is not taken high within eight bit times, SEL is reset and the device is re-initialized and ready to receive a command. If the next word received is an address rather than a command, the MC14469 will find that VAL is still set. It will then reset VAL, initialize the receiver, and wait for another address to be sent. As a result, the second consecutive address to be received will not result in the generation of a VAP. This problem does not arise when the device is enabled to transmit every time it is addressed, since VAL is reset during the transmission cycle. Notice that once VAL has been set by the reception of a valid address, the only way it can be reset without rejecting an address is by going through the transmission cycle.

A similar situation arises when the MC14469 is in the receive only mode and valid addresses and valid commands are alternately received. On the reception of the first valid address, VAL and SEL are set and a VAP is generated. After eight bit times, SEL is reset and the receiver is re-initialized. If the next received word is a command, the MSB will be zero, and when the device checks the valid address latch, it will find that it is set. If the command word has a valid format, it will be latched onto the command data outputs (C_0-C_6). A command strobe will be generated and the send enable latch will be set. Once again SEL will be reset after eight bit times and the receiver will be re-initialized. Thus, the reception of the first valid address and command words will result in the generation of a valid address pulse and a command strobe respectively, as expected. However, since data has not been transmitted, the next incoming address word will be rejected because the valid address latch has not been reset. The MC14469 will then reset VAL and re-initialize the receiver. The following word is a command word and because the valid address latch is not set, the command is also rejected and the receiver is re-intialized.

The next address and command words received will result in the generation of a VAP and CS. Thus, in the receive only mode, every other address and command words will be rejected.

SEND EQUALS VAP

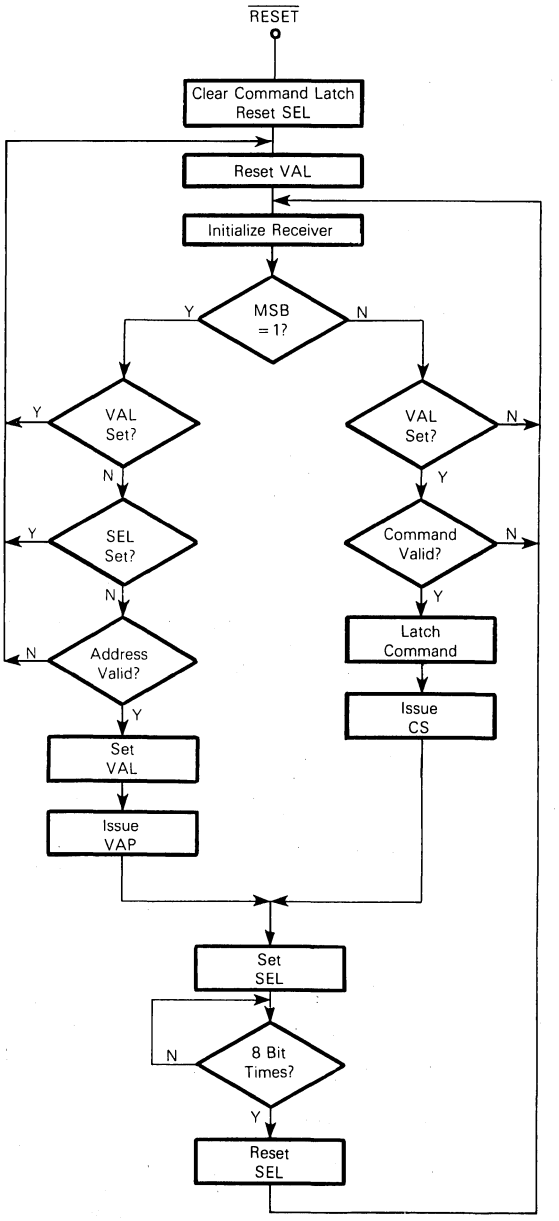
If only addresses are being received and if VAP is tied to SEND, a VAP is generated and data is transmitted when a valid address is received. Normally the transmit cycle is completed before a new address word is received. It is possible, however, for the reception of a new address to overlap the transmission of data. If this occurs, the current transmission is completed before the transmitter is allowed to start another transmission (see Figure 5).

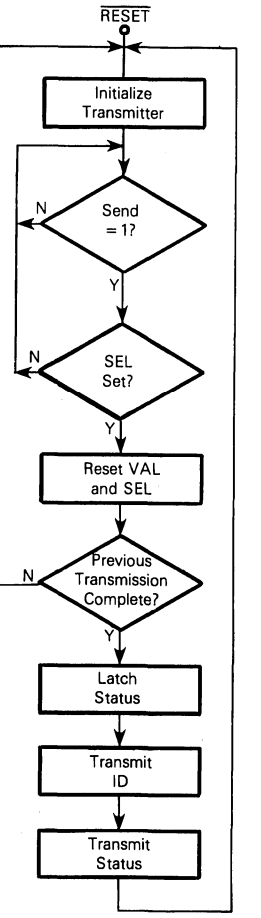
If address and command words are alternately received while SEND is tied to VAP, a VAP is generated every time an address is received. The transmission of data begins as soon as a VAP is generated. This results in VAL and SEL being reset before completion of the received command word and causes the command word to be ignored.

SEND EQUALS CS

If SEND is tied to CS and if address and command words are alternately received, a VAP and CS are generated every time an address and command are received. Data is transmitted every time a CS is generated. Once again, data transmission can overlap the reception of a new address and command word. However, the current transmission will be allowed to finish transmitting (see Figure 5).

Figure 5. Flow Chart of MC14469 Operation





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THE MC14469 AS A MASTER TRANSMITTER

The MC14469 can transmit only after it has received a valid address. For this reason it is usually considered to be a remote or slave device controlled by a UART, MPU or similar control system. However, it is possible to use the MC14469 as a master transmitter by giving it a start pulse on its receive input that has the format of a valid address. The idea is to set the address of the MC14469 that is to be used as a master transmitter in such a way that a valid address will consist of a single pulse which goes low for a certain number of bit times and then goes back high and remains high. This will allow the use of a one-shot or RC network to generate a start pulse which will look like a valid address to the MC14469. On receiving the start pulse, the MC14469 will generate a valid address pulse which can be tied to the SEND input in order to initiate a transmission.

As shown in Figure 2B, if the address of the MC14469 has an even number of ones, the parity bit will be high. The address identifier and stop bit are also high. Therefore, if the address begins with any odd number of zeros and ends with an even number of ones, the address word (start pulse) will need to go low for the start bit, stay low for an odd number of address bits, go high for the rest of the address bits, the address identifier, parity and stop bits. For example, if the address of the MC14469 is set to hex 00, a valid address will consist of a signal which goes low for eight bit times and then goes back high (see Figures 6 and 7). The other addresses for which the scheme will work are hex 60, hex 78 and hex 7E.

Figure 6.

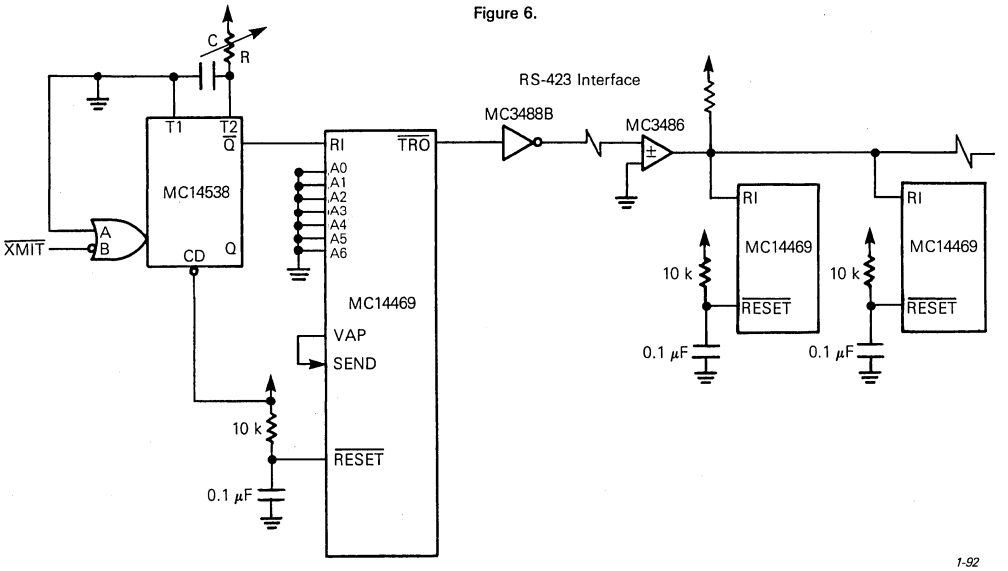
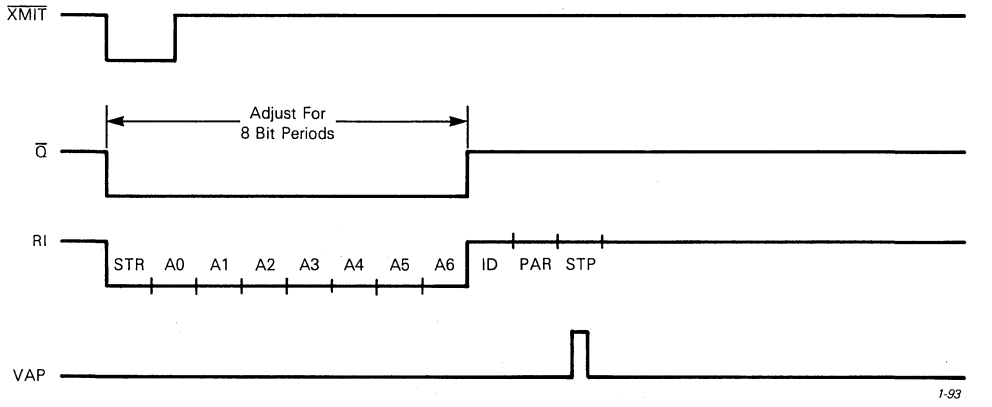


Figure 7. Transmitter Timing Diagram



Infrared Sensing and Data Transmission Fundamentals

Prepared by: Dave Hyder
Field Applications Engineer

Many applications today benefit greatly from electrical isolation of assemblies, require remote control, or need to sense a position or presence. Infrared light is an excellent solution for these situations due to low cost, ease of use, ready availability of components, and freedom from licensing requirements or interference concerns that may be required by RF techniques. Construction of these systems is not difficult, but many designers are not familiar with the principles involved. The purpose of this application note is to present a "primer" on those techniques and thus speed their implementation.

THE GENERAL PROBLEM

Figure 1 represents a generalized IR system. The transmitting portion presents by far the simplest hurdle. All that needs to be accomplished is to drive the light source such that sufficient power is launched at the intended frequency to produce adequate reception. This is quite easy to do, and specific circuits will be presented later.

Figure 1. Simplified IR Sensing/Data Transmission System

The bulk of the challenge lies in the receiving area, with several factors to consider. The ambient light environment is a primary concern. Competing with the feeble IR transmitted signal are light sources of relatively high power, such as local incandescent sources, fluorescent lighting, and sunlight. These contribute to the problem in two ways. First, they produce an ambient level of stimulation to the detector that appears as a dc bias which can cause decreased sensitivity and, worst of all, saturation in some types of detectors. Second, they provide a noise level often 60 dB greater than the desired signal, especially in the form of the 50 or 60 Hz power frequency. Also, recall that the sensitivity of silicon photo detectors extends well into the visible range. This sensitivity, albeit reduced, causes severe interference since the sources in this region are often of significant power, e.g., incandescent lighting and sunlight. In addition to the visible component, both produce large amounts of infrared energy, especially sunlight.

Some IR applications are not exposed to this competition, and for them dc excitation of the source may be adequate. These include some position sensing areas and slow data links over short distances.

But the bulk of IR needs require a distance greater than 30 cm, speeds greater than 300 baud, and exposure to interfering elements. For these needs high-frequency excitation of the source is necessary. This ac drive permits much easier amplification of the detected signal, filtering of lower frequency components, and is not difficult to produce at the driving end. Optical filtering for removal of the visible spectrum is usually required in addition to the electrical, but this too is quite simple.

A WORD ABOUT DETECTORS

Figure 2 shows the three basic detection schemes: a phototransistor, a Darlington phototransistor, and a photodiode. All three produce hole-electron pairs in response to photons striking a junction. This is seen as a current when they are swept across the junction by the bias voltage, but they differ greatly in other respects.

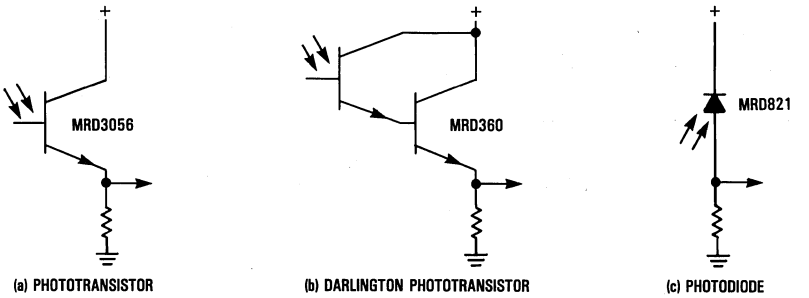


Figure 2. The Basic Detectors for IR Photosensing

The most sensitive is the Darlington. The penalties are temperature drift, very-low tolerance to saturation, and speeds, limited to about 5 kHz (usually much less). Next is the single transistor, having similar penalties (but to a lesser degree), with speeds limited to less than 10 kHz. Typically, they are limited to less than half that number. These two detectors normally find their use in enclosed environments, where ample source intensity is available to provide large voltage outputs without much additional circuitry (their prime advantage). Their detection area is almost never exposed to ambient light.

In virtually all remote-control applications (implying distance), the diode is the detector of choice. This is due primarily to its near-freedom from saturation, even in most sunlit environments. The penalty is sensitivity, often in the nanoamp or low microamp region, but balanced by response speed in the nanosecond range. This permits transmission frequencies in the 50–100 kHz area, providing ample data rates, inexpensive amplification, and easy filtering of noise.

For more information on the internal characteristics of these devices, see the appropriate section of the Motorola Optoelectronics data book (#DL118/D).

SHORT DISTANCES

Many applications in position sensing lend themselves well to the sensitive, if slow, nature of phototransistors. When a go, no-go situation exists, these provide a simple solution provided that ambient light is not present at the detector. The designer must ensure that the system operates even if this portion of the equipment is exposed, as by opening a hatch during servicing or final adjustment during production. This is often achieved via covers, tubes limiting light paths, or that enough directionality exists in the basic device construction to provide the needed isolation. Also available for this application are logic-level output devices, usually of the open-collector type, making processor or logic interfacing convenient.

The light source for these uses is chosen primarily by the distance needed. LEDs work well up to about 5 cm. Above this, incandescents are often used due to their high output and ease of drive with low-voltage ac. Fluorescent sources are seldom adequate due to their "cool" color temperature compared to incandescent. That is, not enough output in the near-infrared or infrared portion of the spectrum.

Data can be transmitted in these short distance situations, provided the speeds required are not great. An example is the electrical isolation of two adjacent PC boards in a rack, with IR elements facing each other across the short space. Here the data can be used to drive the LED directly; modulating a high frequency is not necessary.

Speed and sensitivity are the tradeoff. The resistor used to develop a voltage can be made larger to provide increased sensitivity, but speed suffers and tendency toward saturation increases. Values of 50–200 Ω are common, but can be higher.

MODERATE DISTANCES

For the general case of remote control or sensing at distances greater than 30 cm, the vast majority of applications utilize an LED source switched at a carrier frequency of 20 kHz to 50 kHz and a diode detector coupled to ac band-limited amplifiers. Although certainly more complex than the simpler short-distance sensors, today's product offerings make it an easy task to achieve 10 meters with a data rate of around 5,000 baud at very modest cost.

The transmission end is easily configured. Figure 3 shows a simple IR source capable of 50 kHz transmission. Note that no special techniques are needed to switch the diode at these frequencies. A burst of high frequency is created for each bit time in the data being sent. This mode of gating a carrier on and off is known as CW (continuous wave).

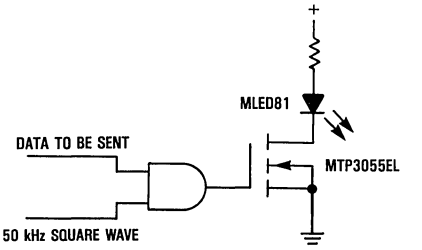


Figure 3. Basic IR Source Drive for CW Operation

The main areas of interest are the switch device and the diode current. Today's IREDs (infrared emitting diodes) are generally capable of around one ampere peak currents, but applications typically limit this to half that value. Most designs that use a 50 percent duty cycle square wave switching waveform have diode currents in the 100–500 mA range. It is important to realize that although IRED output increases linearly with drive current, it drops rapidly with increasing temperature. Therefore, reliability is not the only reason for resisting the temptation to increase range by driving the IRED harder. A diode with a 100 mA continuous rating can be reliably driven with a 200 mA square wave, and so on. It is quite common to use more than one IRED in series for increasing output and range, lowering the current requirements, and increasing reliability of the diodes.

The driver device can be a bipolar transistor or a FET. The bipolar works fine, but requires enough base current for saturation that the driving circuitry often must provide 10–20 mA or more. This may not be available directly from CMOS devices. Darlingtons solve this problem, but are usually much too slow. Another solution is an inexpensive logic-level FET such as the MTP3055EL, its physically smaller cousin, the MTD3055EL, or a MTP4N06L. This provides plenty of speed while being driven directly from any CMOS device, with absolute minimum parts count. A resistor (50–500 Ω) is sometimes used in series with the gate to moderate the very-high switching speed and noise from high frequency oscillations. The resistor is usually not needed if the gate is driven from a medium-speed CMOS gate such as the MC14081B or MC14011UB.

THE RECEIVING PROCESS

At the receiving end, the first item encountered is an IR optical filter as shown in Figure 4. This serves the sole purpose of attenuating the visible portion of the spectrum while leaving the IR intact. It can be a material specifically designed for the purpose, such as the Kodak filter series, but is usually an inexpensive acrylic plastic. This is almost any readily-available red, non-opaque plastic. Suitability is easily proven by inserting a sample between an emitter and detector while observing the

detector output. The IR signal should be minimally altered. This filter may be incorporated into the system as a unique piece of the material in front of the detector, or the entire front panel of the product may be made of this plastic. Sometimes lenses are actually molded from it (discussed in a later section).

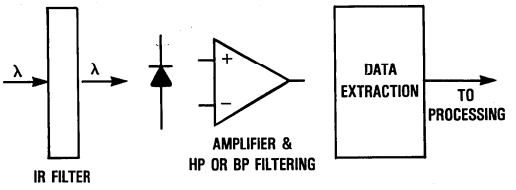


Figure 4. Basic IR Receiver

The detector diode behind the filter is usually constructed as a large-geometry device specifically designed for IR remote control, and presents a large area simply for more IR energy absorption or increased aperture. It is not unusual to find the material used for encapsulation to be red or black, and apparently opaque. The encapsulation serves as an IR filter, as in the case of the MRD821. Even so, an additional one is usually employed as mentioned above, often for the cosmetics of the product.

In addition to visible-light filtering mentioned above, electrical filtering must be applied to greatly attenuate the low-frequency interference present in both the visible spectrum and the IR. This is accomplished by three methods. First, coupling capacitance values are judiciously chosen to begin rolloff just below the transmitted frequency. This is quite effective since the area of interest is usually about a factor of 10^3, or some 9 to 10 octaves above the power-line frequencies. The second method is to use explicit high-pass filter circuitry, but in practice this is seldom needed due to the effectiveness of the other techniques. A third option is to use a bandpass amplifier, usually with an LC tank. More discussion of this later.

After the signal is brought up to a level sufficient for detection, some method must be employed to extract the data. Most common is a simple peak detector. This detects the presence of the high-frequency pulses, charging a capacitor up to a threshold in a few cycles, at which point a comparator signals the new level. In the absence of a signal (the carrier), the capacitor discharges until the comparator's lower threshold is reached, signifying the opposite logic level. Other techniques are also available, such as the phase-locked loop, whose lock-detect output can be used as the recovered logic-level data.

MORE ON RECEIVING CIRCUITS

Two general methods are used to begin the amplification. First the diode light current (a few microamps or less) may be used to develop a voltage across a series resistance, which is then capacitively coupled to the amplifier using the rolloff of low frequencies mentioned above, as shown in Figure 5a. Second, the current may be driven directly into the amplifier, as in Figure 5b, where the photo current is summed with the feedback current at the amplifier input. Note that in these and other figures, the amplifier symbol does not necessarily denote an actual integrated operational amplifier, but may symbolize a discrete amplifier.

Figure 6 shows an amplifier system coupled to a bandpass amplifier centered about 50 kHz. Here the front end is actually an operational amplifier, used in the mode of Figure 5b. Various choices for operational amplifiers exist; perhaps the first hinges

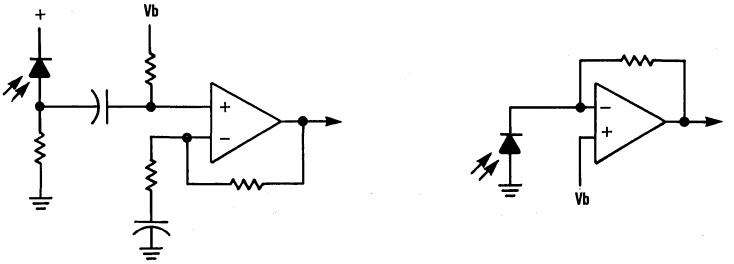
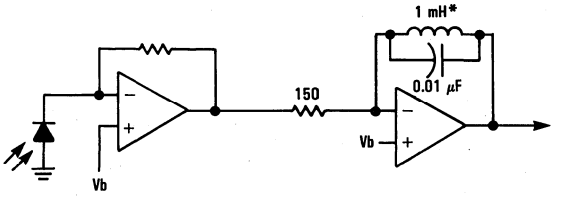


Figure 5. Front-End Amplifier Options



*Toko type 10 PA or equivalent. Available from Digi-Key Corporation, phone (800) 344-4539.

Figure 6. Amplifier Chain Showing 50 kHz Bandpass Filter Second Stage

on the supply voltage. Some recent advances in the technology have greatly increased slew rates and gain-bandwidth products. This has permitted devices that are capable of operation on a single 5 volt supply, yet can be used in the 50 kHz range. An example of this is the MC34072 series, whose input common mode range includes ground, permitting the diode or the other amplifier input to be referenced there. If greater gains are needed, and higher supply rails are available, the MC34082 series provides slew rates of 25 V/μs, or twice that of the MC34083. These operational amplifiers in general do not have the low-noise performance of discrete versions, with the above devices being in the 30 nV/$\sqrt{Hz}$ region. However, the MC33077 provides excellent noise performance of about 4.5 nV/$\sqrt{Hz}$ at a similar slew rate on a 5 volt supply, although its common mode range does not include ground. A simple discrete amplifier example is shown in Figure 7.

Another option that should be considered for data reception is the MC3373 (Figure 8), which integrates many of the functions already described. This device contains the front-end amplifier, a negative-peak detector with comparator, and requires only a few external components. The amplifier may have the diode directly connected to it, or ac coupled for purposes of rolloff. A tuned circuit can be used for the better noise performance of a band-limited system. Some words of caution: supply bypassing close to the device, particularly at the gain-determining impedance (resistance or tuned circuit), is critical. Without proper bypassing, gain and range suffer. Also, a higher supply voltage of around 12 volts or so assists in greater range performance.

The vast majority of IR links in consumer products (VCRs, TVs) use an LC tank. The inductor is a shielded, adjustable slug type in the 1-5 mH range. Shielding in the form of a metal can usually encloses the entire subassembly, and the designer should expect to employ such shielding in most applications requiring moderate or long distance operation.

Note that in Figures 7, 8, and 9 the bias supply to the receiving diode is heavily decoupled from the supply via an RC. Any noise present at this point directly impacts system noise and sensitivity. Bandwidth is also often limited at the upper end as an aid in overall noise performance as seen in Figures 7 and 9. These amplifiers use small capacitors (33 pF, 10 pF, 100 pF) to roll off frequencies above 100 kHz.

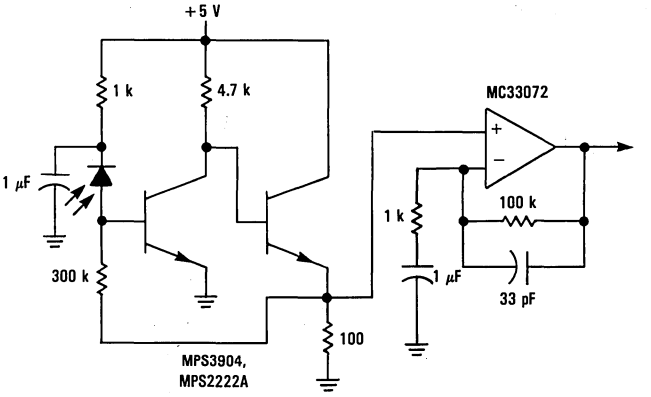


Figure 7. Simple Discrete Front End with Op Amp

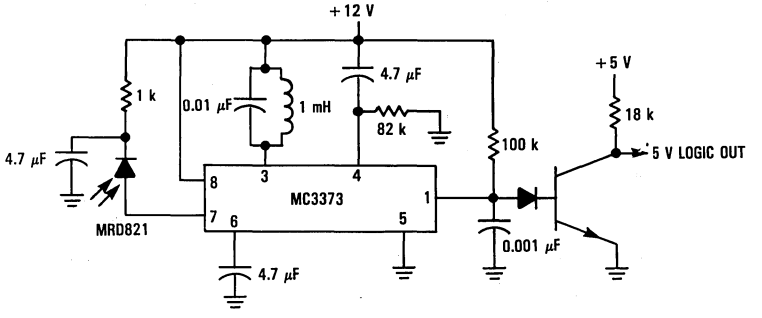


Figure 8. IR Receiver Using the Integrated MC3373

LONG DISTANCES

When the distance to be covered extends beyond 10 meters or so, other methods must be considered. The methods described below have resulted in ranges of 100 meters or more.

At the transmitting end, most of the options available center on increasing the power output. One way is to increase the IRED current, but this is subject to limits as previously discussed. Another solution is to use multiple diodes in series, often three. Note that this does not require additional supply current. Multiple diodes also provide one solution to those applications requiring less directionality, with the IREDs being slightly misaligned from one another.

The diodes can also be driven much harder, and produce proportionally higher instantaneous power, if they are pulsed with a very-short duty cycle. Currents of about an ampere are common, but for only a few microseconds and with a duty cycle of 5 percent or less. This also requires modified receiving techniques.

At the receiving end, most solutions center on increasing the aperture of the system such that simply more energy is gathered. Multiple receiver diodes can be connected in parallel, adding their currents, with the additional possibility of reducing directionality if needed. Another technique is to add a lens, with the diode being placed at the focal point. In higher volume production, this is often molded into a front panel and is usually of the red filtering plastic mentioned earlier. Some systems make use of a flat Fresnel lens, being somewhat more difficult to mount but very effective. They can also be hidden behind a plastic panel.

Front-end amplifiers superior to the simple operational amplifier or discrete versions already mentioned may be found in these highest-performance situations. Such an amplifier is shown in Figure 9, where low-noise transistors are used in a circuit designed specifically for low-noise applications.

When pulsed sources are used, some encoding scheme is normally used to transmit the data. One common technique is to use a single pulse for one edge of a data bit, and two or more closely spaced pulses to signal the opposite edge. These are simply differentiated by some flip-flops and a small amount of timing circuitry. Other schemes use multiple pulses at close intervals to indicate one logic level, and a differing number to denote the other.

CONCLUSION

As can be seen from this discussion, IR links have become quite easy to implement. With the basic principles in mind, the designer should be able to adapt the techniques mentioned here to his specific system needs.

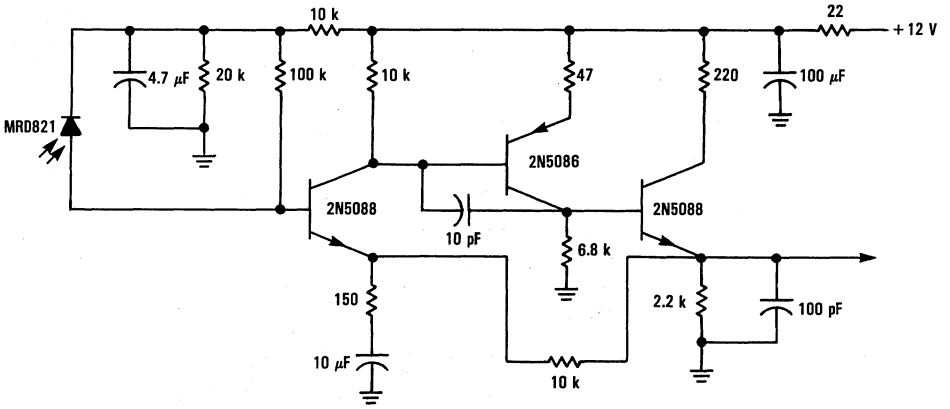


Figure 9. High-Performance Discrete Front-End Amplifier with Special Attention Paid to Noise

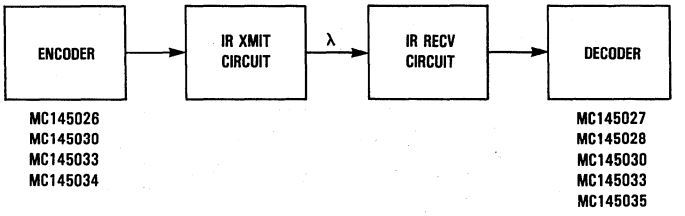


Figure 10. Utilizing Motorola's Encoders and Decoders

AN1126

Evaluation Systems for Remote Control Devices on an Infrared Link

Prepared by: Dave Hyder
Field Applications Engineer

The introduction of many remote control devices and their modest costs now permits the designer a wide choice of inexpensive options in the low-end control area. When this choice is coupled with the ease and economics of infrared communication links, applications for the combination of the two abound. This paper provides information for constructing the basic building blocks for evaluation of both the IR transmitter/receiver and the most popular remote control devices. Schematics and single-sided PC board layouts are presented that should enable the designer to quickly put together a basic control link and evaluate its suitability for his application in terms of data rate, effective distance, error rate, and cost. Sources for speciality parts required are also given.

Motorola offers a wide variety of devices suitable for remote control applications, and these are grouped in three distinct families. The oldest of the three is the MC145026/7/8 series, comprising one encoder sending nine bits of information and two decoders, one considering all transmitted data as an address, the other utilizing less addressing possibilities and using the difference as four bits of data. This series also uses trinary addressing, permitting greatly increased numbers of address codes for a given pin count.

The next series is comprised of one part, the MC145030, which is an encoder and decoder on the same part. Thus, it is suitable for applications requiring bidirectional or half-duplex control. It is capable of nine bits of address, no data.

Derived from the internal architecture of the MC145030 is the MC145033/4/5 series, which comprise a wide variety of choices of address/data combinations, outputs, and a single-chip encoder/decoder. This series can encode up to 17 address bits, or 13 address/4 data. Other features, such as an ability to defeat attempts to break the code, are also included. At present, these devices are available in surface mount packages only.

This paper presents simple board layouts and schematics for encoder/decoder pairs "connected" by IR transmitter/receiver links. For each of the three families of devices, there are two PC layouts and schematics, one encoder/transmitter and one decoder/receiver. These are made sufficiently general that each can be modified and jumpered so as to enable evaluation of any member of that family.

Note that only one IR transmitter and one IR receiver design is used for all of the encoder/decoder options, and so there is only one schematic of each of these two, and it would be mated with the encoder or decoder schematic of choice to form a complete system. The PC layouts all have these sections included, of course.

DESIGN SPECIFICS

The IR transmitter schematic shows two IR LEDs. While most designs will use but one, the other is allowed for on the PC layout for evaluation of other options, such as lower total current, greater range, misalignment for less directionality, etc. The generation of the transmitted frequency (in this case 50 kHz) is not done with minimal components, but allows for flexibility in frequency, and selection of other crystals via some cuts and additional resistors. A production design would likely utilize a common oscillator for the transmitter and encoder sections or even include the ability to startup on request to minimize power. Open pads are provided to enable jumpering of different frequencies with a combination of divider taps and crystals/resonators.

The IR receiver section uses an MC3373P as an amplifier/data detector. This is a high-gain device working with some very low signal levels. Thus, shielding will likely be required, and ground area is provided for its attachment. The component values are "middle-of-the-road" and will work well as presented; the designer will want to evaluate for himself whether to permit higher gains, different low frequency rolloffs, or other sensitivities. The choice of the LC tank values is of particular interest. The values shown are adequate for many applications, but higher Q's may be needed. This comes at the cost of slower rise and fall times on the data envelope, visible at pin three of the MC3373P, and is the primary factor governing the maximum data bit rate of the design. Lower Q's will yield "squarer" data envelopes (higher possible bit rates), broader tuning, and less selectivity. Tuning is accomplished by placing a transmitting source several feet away, and adjusting the inductor for maximum data envelope at pin three. The output of the MC3373P is squared and inverted by a Schmitt-trigger MC74HC14 device. In many designs, a slower and quieter version of this device may be preferred, such as the MC14093 NAND Schmitt. This device will generate less system noise, critical to good operation of the receiver, and also would operate on higher supply voltages, such as 12 V, where the MC3373 receiver also works well.

The output of the receiver section is presented to a red LED to indicate that data is being received (activity on the MC3373 output). This, of course, does not indicate valid data, but only that something is being detected. It may be an indication of noise or power-line pickup and require design changes or shielding. Valid data is indicated via a green LED driven by the output of the decoder device and annunciates

that it has received its correct address (set by the DIP switches).

The transmitting section is attached to one of the three encoder designs, and three PC layouts are presented; the same is true of the receiver and the three possible decoders. The receiver schematic in Figure 1 is joined with the decoders of Figures 3, 5, and 7 and the transmitter schematic of Figure 2 with those encoders in Figures 4, 6, and 8. Each encoder or decoder layout can be used with more than one version in the same family, and appropriate pads and jumpers are provided on the layout. Other situations certainly are possible, such as changing minor portions of the layout to make the data bits on some systems available to a connector, or remote transmit enables, etc., and these layouts may serve as a starting point.

One caution on the choice of R and C values for the encoders and decoders: the tolerance and dielectric type are important, especially for production-volume designs intended to operate over temperature. Refer carefully to the data sheets of the appropriate device for a discussion of these parameters and permitted tolerances.

CONCLUSION

The designs as presented here are intended for a 5 V supply and a transmitter carrier frequency of 50 kHz. Other frequencies should be investigated for ease of generation, minimum components, increased data rates, and different Qs. With a single transmitting LED driven with about 250 mA, the author achieved effective distances of about 10 meters. This distance could be extended by a few meters if two LEDs were utilized. There are applications that do not require this level of sensitivity, and the receiver should be modified accordingly. On the other hand, greater distances or those requiring less directionality may require adding more LEDs, driving them harder, utilizing multiple receiving diodes, and/or adding Fresnel lensing in front of them. For more information on IR techniques, see Application Note AN1016, and the CMOS Application-Specific Standard IC Data Book, DL130 rev. 1.

SPECIFIC COMPONENT SOURCES

Trinary DIP switch, 8 position	AMP #436172-3
Trinary DIP switch, 9 position	AMP #436172-2
Other DIP switches	AMP series 7100 or similar
PB switch, transmitter enable	Digi-Key # P9950
Inductor, variable, shielded, 4.7 mH, type 7PA	Toko # 126LNS–T1028Z Digi-Key # TK3209
Ceramic resonator, 400 kHz	Panasonic # EFO-A400K04B Digi-Key # P9940
Transmitting IR LED	Motorola MLED81
Receiving IR diode	Motorola MRD821
Shielding Material, 0.005" Tin sheet, solders easily	K & S "Easy Solder Tin Sheet" Most hobby shops

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of component suppliers.

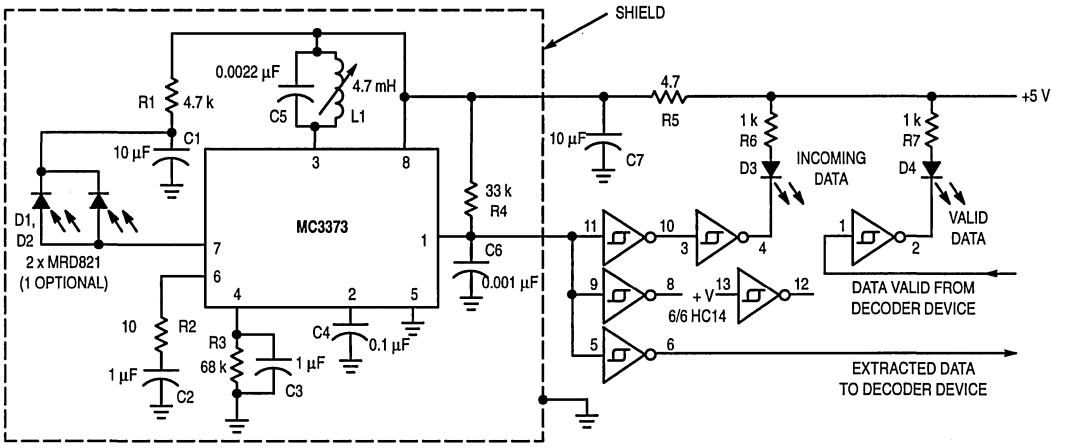


Figure 1. IR Receiver section common to all receiver boards. Values shown are for a 50 kHz carrier frequency and a 5 V supply. Note that the use of two receiving diodes is optional and provided for on the board layout. The shield is required in all but the shortest range applications.

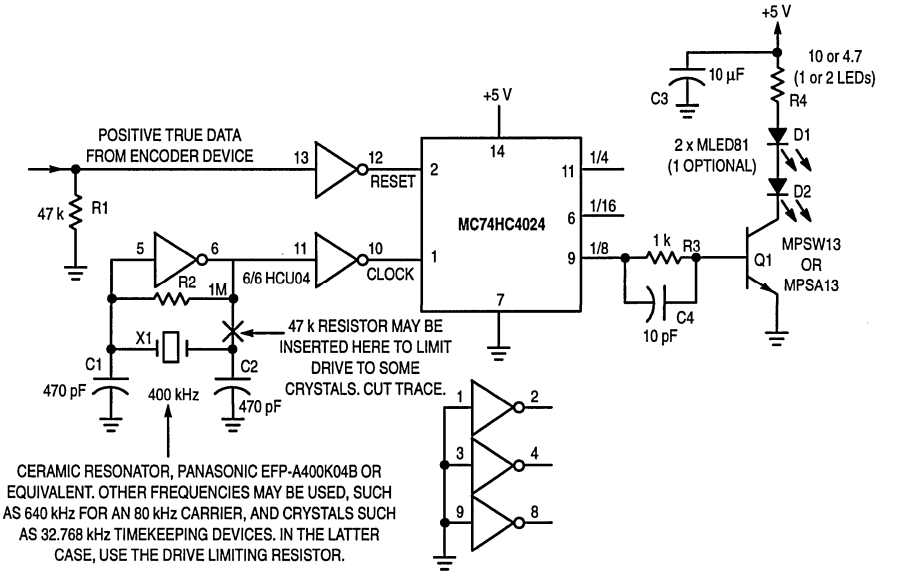


Figure 2. IR transmitter section common to all transmitter boards. Note that the use of two IR LEDs is optional but is provided for on the board layout. Choose R4 for an LED current appropriate to the application. Common values are from 100 to more than 500 mA, with 250 mA being common.

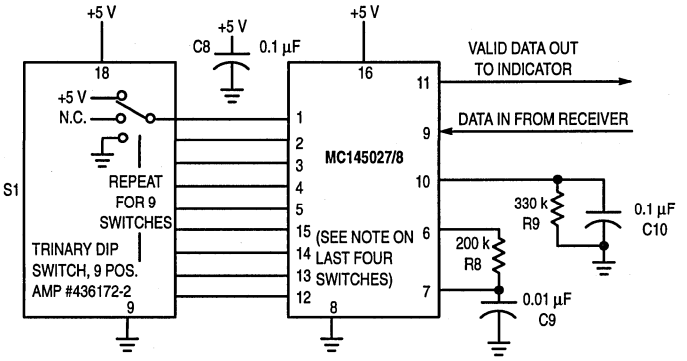


Figure 3. Two decoders, identical except that the MC145027 uses only 5 bits of address, considering the last 4 bits as data. To use this device, leave the last four Dip switch positions open as these pins (12, 13, 14, 15) become outputs.

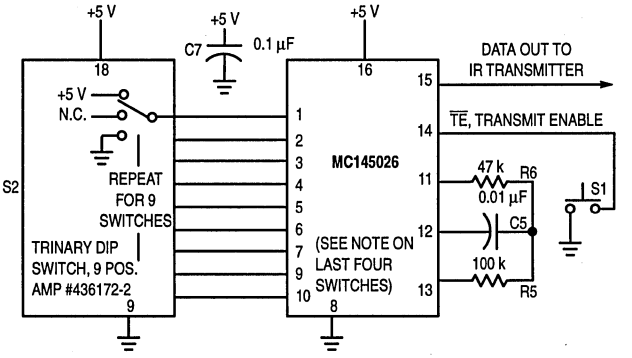


Figure 4. The MC145026 Encoder. Note that when used with the MC145028 decoder in the receiver, all 9 switches are considered addresses, and that with the MC145027 the last four are interpreted as data. In the latter case, a trinary (open) position is decoded as a logical one.

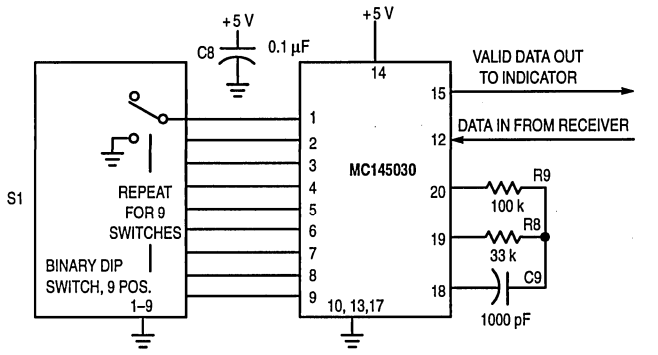


Figure 5. The MC145030 as a decoder. Note that the 9 DIP switches take advantage of the on-chip pullup resistors on the device. Also the decoder out (Pin 15) toggles with each successful data reception, unlike the MC145027/8 devices.

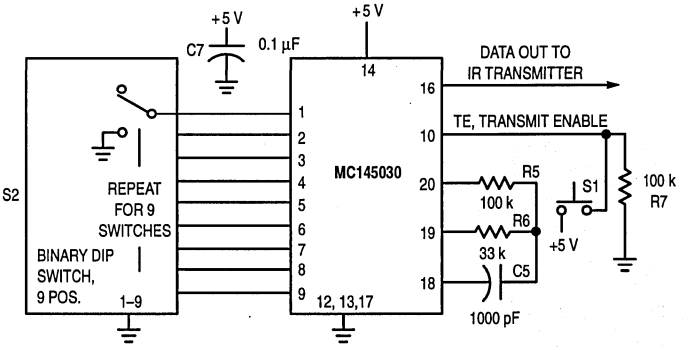


Figure 6. The MC145030 as an encoder. Note that transmit enable occurs on the rising edge of the waveform.

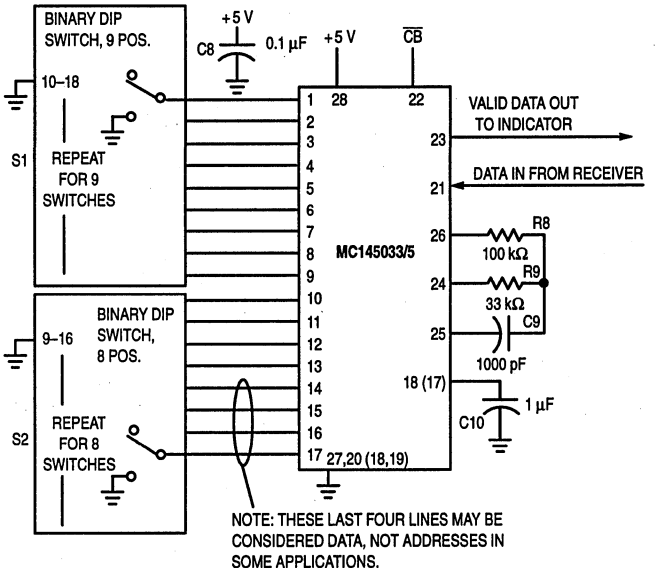


Figure 7. The MC145033/5 as a decoder. Note that there are two DIP switches, one 9 position, one 8. In the event of using the upper addresses as data, leave these pins open (center position). Also the CE pin may be either 18 or 17 depending on the device, and pin 18 is strapped to ground on the MC145033. "Mode," pin 19, is grounded on the MC145035.

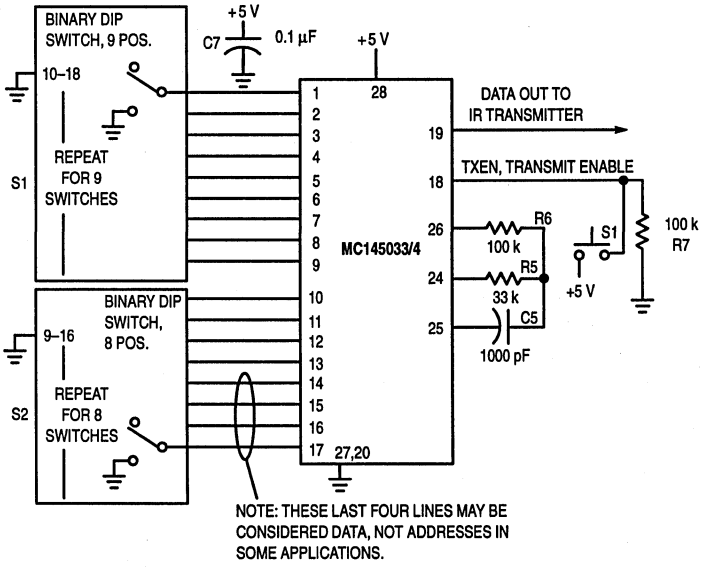
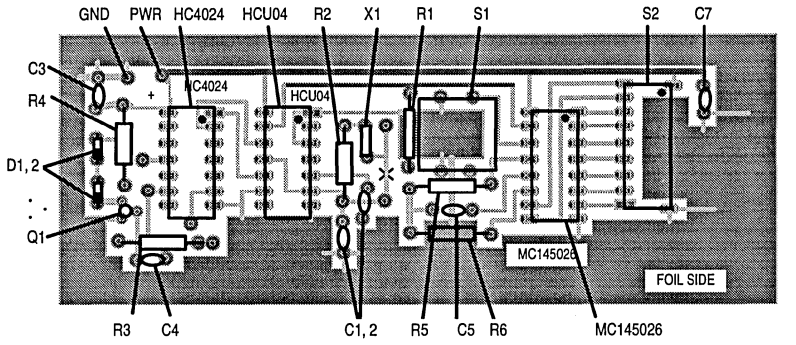
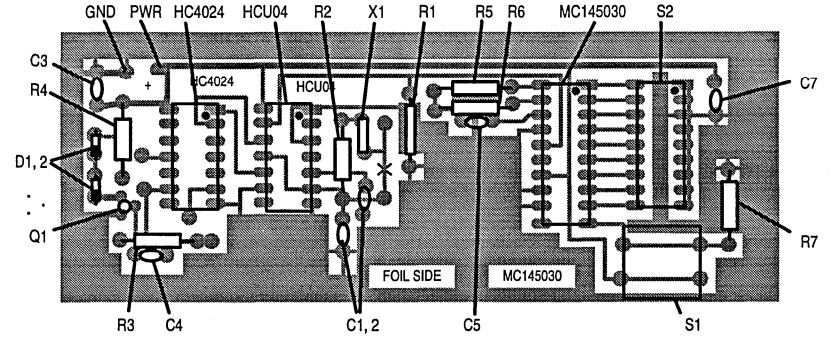


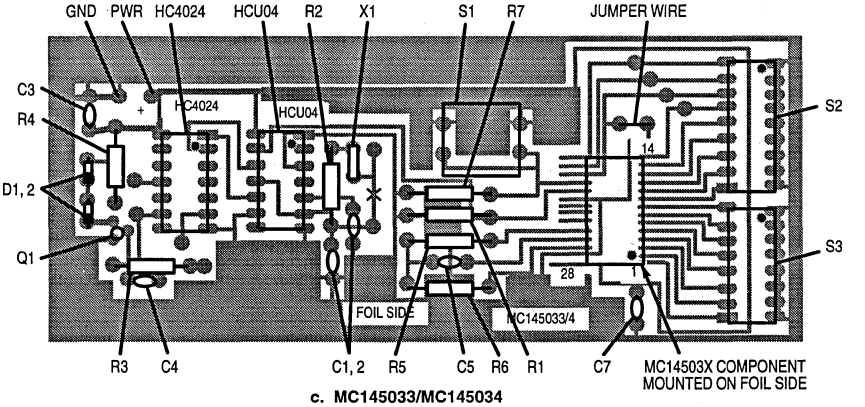
Figure 8. The MC145033/4 as an encoder. Note that transmit enable occurs on the rising edge of the waveform. Pin 20 is grounded on the MC145033.



a. MC145026

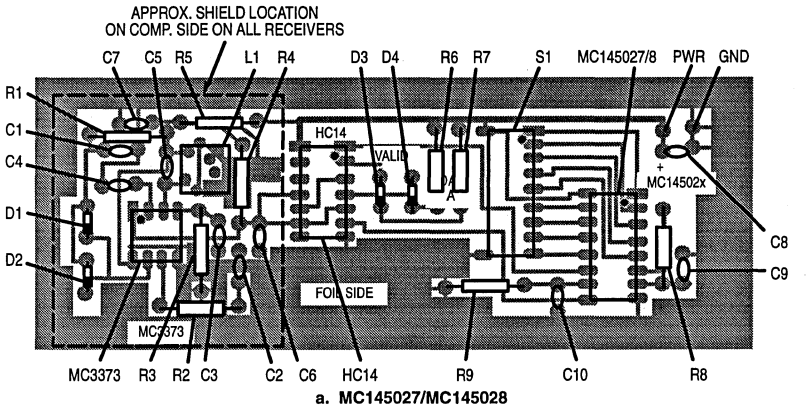


b. MC145030

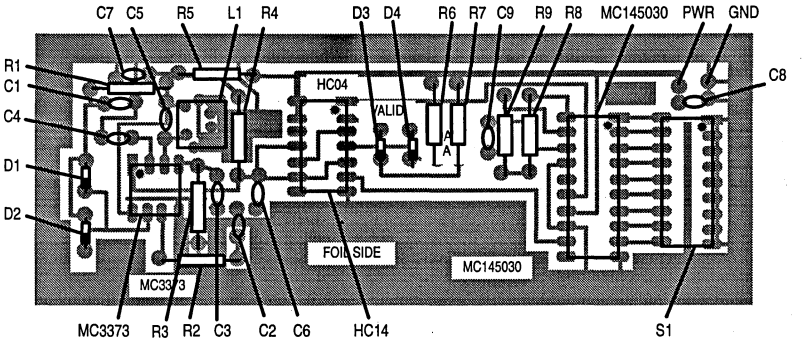


c. MC145033/MC145034

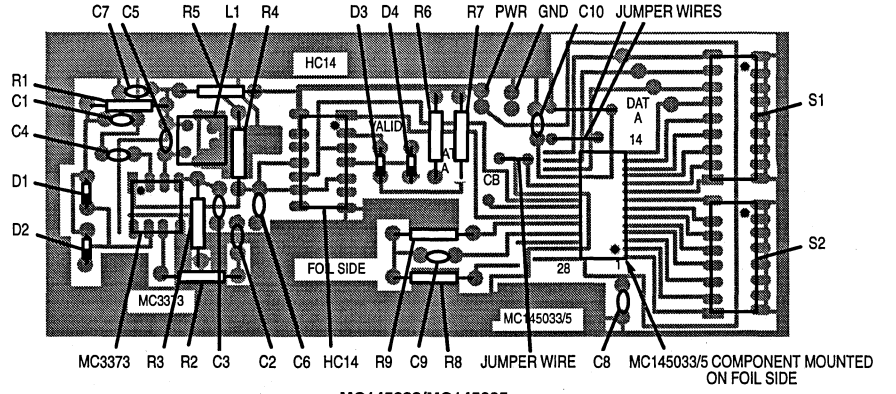
Figure 9. Three Component Layouts for IR Transmitters



a. MC145027/MC145028

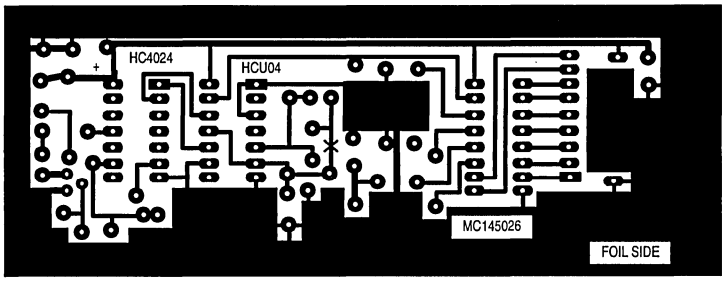


b. MC145030

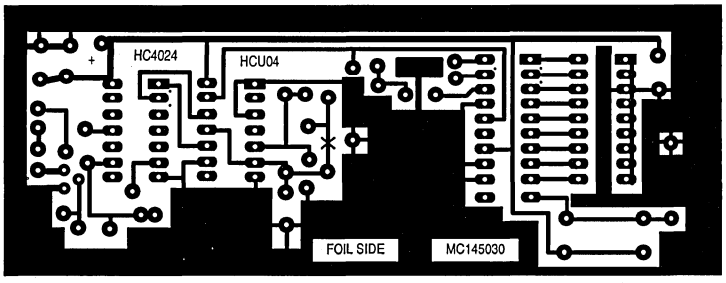


c. MC145033/MC145035

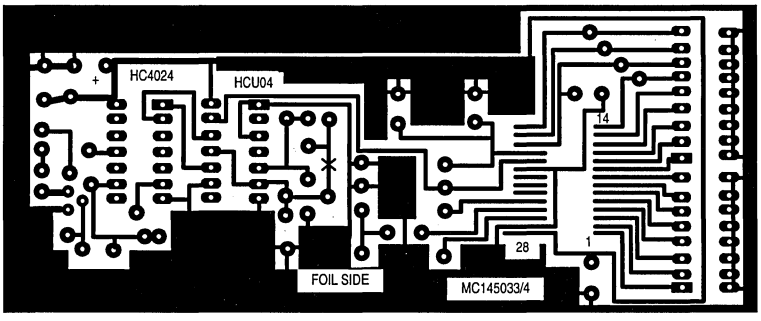
Figure 10. Three Component Layouts for IR Receivers



a. MC145026

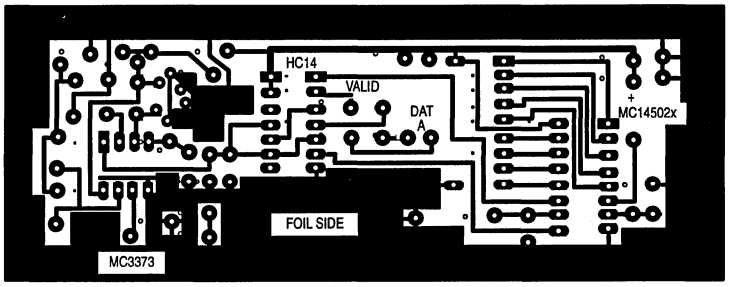


b. MC145030

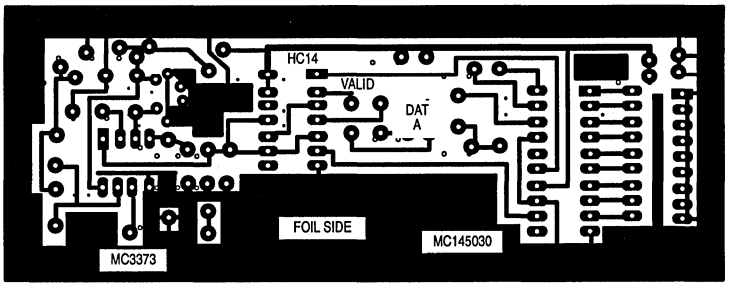


c. MC145033/MC145034

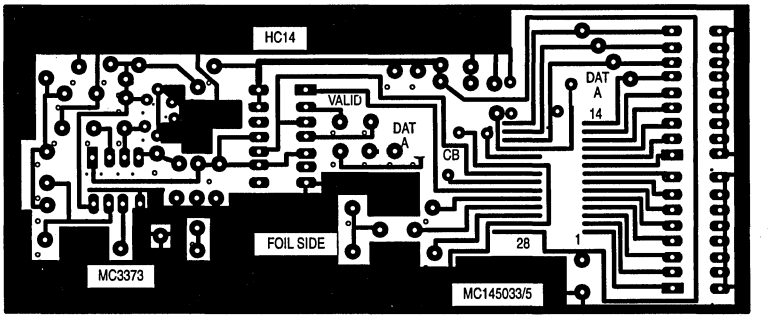
Figure 11. Three PC Layouts for IR Transmitters



a. MC145027/MC145028



b. MC145030



c. MC145033/MC145035

Figure 12. Three PC Layouts for IR Receiver

MOTOROLA
SEMICONDUCTOR
APPLICATION NOTE

A Software Method for Decoding the Output from the MC14497/MC3373 Combination

Prepared by: Steve Reinhardt

The electronics industry has used infrared media as a simple, easy, and effective method of wireless communications over short distances. It is not without its problems since simple on/off modulation is affected by the many infrared sources in our environment today. To provide immunity from the noise created by lamps, lighters, electronics, and even humans, the IR carrier is modulated at a rate that would not occur in nature. The industry has settled on around 40 kHz as the modulation frequency.[1]

The data that is transmitted usually takes the form of AM (or CW – continuous wave); that is the carrier is turned on and off for variable periods of time. Some have used a FM scheme, where the modulation frequency is changed to represent 1 or 0. The output of detectors is generally the same: that is a logic 0 represents a presence of carrier in AM, or one of the frequencies in FM. A logic 1 then represents no carrier in AM, or the second frequency in FM.

The encoding of the data varies widely, from schemes that encode the data as variable pulse widths, constant length coding schemes, or simple ASCII, to the biphase scheme used in the MC14497. Any of these schemes can be decoded by the use of a microcomputer that has a timer, such as the MC68HC05 family or the MC68HC11 family of parts.

THE MC14497

The MC14497 is a complete building block for IR data transmission, lacking only a high current driver to power the IR LED (or LEDs, depending on the range required) such as the MLED81. The chip limits the duty cycle of the LED to about 10%. The use of an inexpensive ceramic resonator generates the 31.25 kHz carrier. A simple SPST matrix keyboard completes the transmitter.

THE MC3373

The MC3373 is a companion chip to the MC14497. It provides all of the front-end signal processing to interface an IR photo detector, such as the MRD821, to a TTL level. It includes the gain stages, with automatic background level control (AGC), a simple frequency discriminator to eliminate interference from other sources, and a wave shaper that generates a TTL or CMOS output level. The MC3373 does not decode the data, it merely reconstructs it in logic level form (the way it was transmitted) to facilitate decoding. It too requires few outside components, such as a tuned circuit and a few capacitors for wave shaping. Care must be taken in circuit layout, as this device operates at very high gain to accommodate the low level input signal from the photodetector. Since there are frequency sensitive components in the circuit, it is best to minimize lead lengths, work on a ground plane, and perhaps even put a shield around the components that make up the receiver.[1]

THE ENCODED BIT STREAM

To understand how to decode the data from the MC14497, it is important to understand what is transmitted. Each word transmitted consists of an AGC burst, a start bit, and 6 data bits. The 6 data bits represent 64 individual channels (0–63). However, channel 63 (111111) is never sent.

The carrier frequency is determined by dividing the oscillator frequency by 16. For a 500 kHz resonator, the carrier is 31.25 kHz. The baud rate (signalling rate) is equal to the carrier divided by 32, or the oscillator divided by 512. Again, for a 500 kHz resonator, the baud rate is approximately 976 bps. Each command word takes approximately 8 ms to send.

Refer to Figure 1. Data is the representation of the channel code (001010, channel 10). Carrier represents the output of the MC14497. Recovered is the signal that is output from the MC3373. Notice that the data is inverted, or normally high. When a key is pressed, the chip sends a signal to setup the AGC in the receiver. In the AM mode, which is most common, each transmitted word is preceded by a 512 μs burst (oscillator divided by 256). One bit time later, the start bit is sent. The bi-phase modulation scheme then uses the position of a carrier within the bit time to represent the data value. Refer to Figure 2. The presence of carrier immediately after the bit time boundary represents a 1. The lack of the carrier represents a 0. The phase then changes so that there is a constant modulation, with clock edges on each bit time boundary. This feature is important in some communications schemes, but is not important here.

If a key is held down, the code is repeated at 90 ms intervals. See Figure 3. This results in a duty cycle of about 10% so that the IR LED can be pulsed at high peak power. At this duty cycle, the MLED81 can tolerate peak currents well in excess of 100 mA. Once a key is released, the MC14497 automatically sends the code for channel 62 (111110), which indicates end of transmission (EOT).

[1]See also AN1016, "Infrared Sensing and Data Transmission Fundamentals".

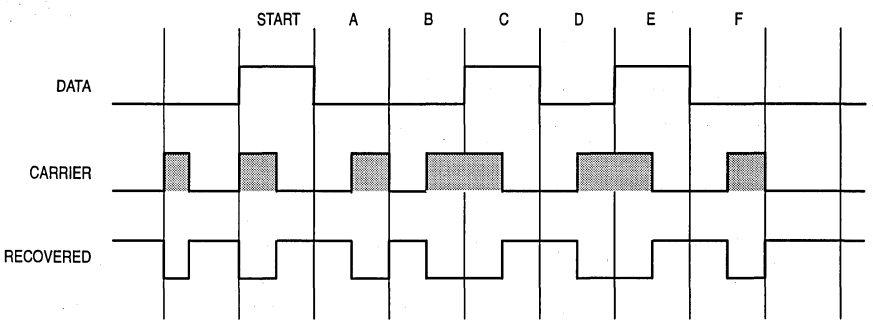


Figure 1

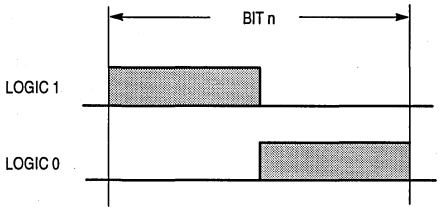


Figure 2

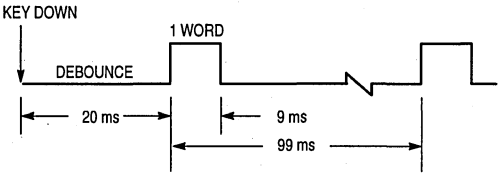


Figure 3

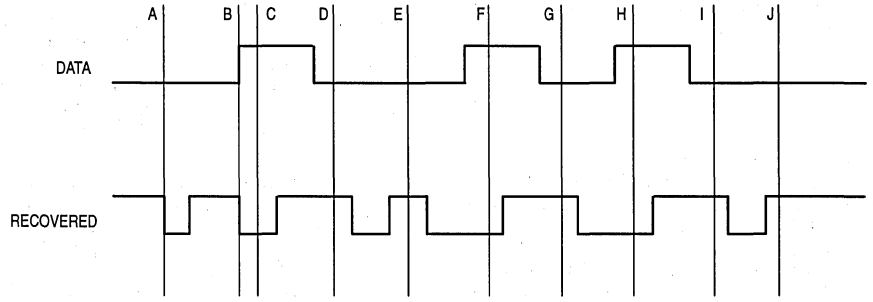


Figure 4

THE DECODING METHOD

Refer to Figure 4. The letters refer to time slices shown on Fig. 4. The pseudocode to decode the data looks like this:

Main:
  Set up an interrupt to look for the start bit transition.

Interrupt:
  Capture the timer value and save it.(a)
  Look for the next transition(b), capture the timer value and subtract the saved value. This is the bit time value. Save it.
  Add one quarter bit time value to the timer, and set an interrupt for when it times out.(c)
  At that interrupt(c-i), look for the value, and set the carry bit accordingly.
  Add the bit time to the timer, and set the interrupt.
  Shift the carry into the data storage location.
  Have we got the six bits plus start? If not, repeat, otherwise we're done with this word.
  Is the word EOT (channel 62)? if not, the key is probably repeating. If it is, the message is complete

THE MC68HC11 PROGRAM

This chip is easy to use because of the 16-bit add (ADDD) and subtract (SUBD) features which can used to service the timer. The MC68HC05 devices lack this, but do provide an add with carry (ADC) to implement 16-bit adds.

Port A pin 3 (PA3) is used as the input from the MC3373. This is an input capture pin (IC1). The output compare feature is required to generate the bit clock, though an output pin is not necessary.

THE MC68HC05 PROGRAM

The code for the MC68HC05 is a little different. First, since the state of the input capture pin cannot be read, the data must be routed to another pin. Therefore, PA7 is used to sample the data. The internal output compare interrupt is utilized to set the baud clock.

MC68HC11 PROGRAM LISTING

```
  start
lds
#$ FF
*load the stack pointer

ldaa
#2
*set prescaler to /4

staa
TMSK2
*by writing to TMSK2 register

ldaa
#1
*enable input capture 3 functions

staa
TMSK1
*TMSK1 enables the interrupt

staa
TFLG1
*TFLG1 clears the flag

ldaa
#2
*look at falling edges

staa
TCTL2
*by writing to TCTL2

ldaa
#6

staa
count
*number of bits to assemble


*end of initialization

.

.

.
  main

*main program

.

.

.
  *Input capture interrupt service routine. The first time through, the
  *value of the timer is saved, the second time through, the difference
  *is calculated, determining the bit interval, and the time slice is
  *shifted by one quarter bit interval for sampling the data.
  *
  timeint
brset
flags,0,next
*input capture 3 interrupt routine

ldd
#$1014
*save the timer value from the first edge(a)

std
saveit
*to time the baud rate

bset
flags,0
*bit 0 in flags indicates first edge

bra
endint
*exit interrupt cleanly
  next
ldd
```

```
#$1014
*get the timer value(b)

subd
saveit
*subtract the first value(b–a)

std
baud
*save that in baud

lsrd
*divide by 2

lsrd
*divide by 4

addd
#$1014
*add 1/4 bit time to the timer

std
OUTC1
*store to output compare 1

ldaa
#$FE
*clear the mask

anda
TMSK1
*without disturbing other bits

staa
TMSK1
*disable further input compare interrupts

bclr
flags,0
*clear first edge flag bitendint
  endint
ldaa
#1
*setup to clear flag for next edge

staa
TFLG2
*and writing to TFLG2

rti
*wait for next edge


  *Output compare interrupt service routine. Each time an in-
terrupt
  *occurs, sample the input line and shift the equivalent value
  *into the data register. Do so for all six data bits, then word
  *is complete.
  *
  bitint
ldaa
PORTA
*get the present value of the data

anda
#4
*mask all but PA3, the input

rora
*shift towards carry

rora
*once more

rora
*now the input bit is in carry

cmc
*data from 3373 is inverted

ldaa
data
*get the saved data byte

rola
*rotate the carry in

staa
data
*save the byte

dec
count
*the number of bits is complete?

bne
next2
*not done yet

bset
flags,1
*we're done

bra
endin
*no more in this word
  next2
ldd
OC1
*get the last timer value

addd
baud
*add the baud interval

std
OC1
*store it for the next interrupt

ldaa
#1
*

staa
TMSK2
*and clear the flag for the next interrupt
  endin
rti
```

MC68HC05 PROGRAM LISTING

```
  start
lda
#$C0
*set up timer control register

sta
TCR
*interrupts enabled, negative edge

lda
#$0
* make sure port a is an input

sta
PADDR
* write to data direction

lda
#6

sta
count
*number of bits to assemble

.

.

.
  main
equ
*
*main program

.

.

.
  *input capture service routine. The first time through, the
value of
  *the timer is saved. The second time through, the difference
is
  *calculated, determining the bit interval. The time slice is
shifted
  *by one quarter time for sampling the data.
  *
  *timeint
brset
flags,0,next

lda
ICH
*grab the high byte

sta
saveit
*store it

lda
ICL
*then the low byte

sta
saveit+1
* and save that.

bset
flags,0
*got first edge flag

bra
endint
  next
lda
ICL
*get the new low byte

sub
saveit+1
*subtract the old low byte

sta
byte+1
*and save the result

lda
ICH
*get the new high byte

sbc
saveit
*subtract the old, with carry

sta
byte
*save the byte interval

lsr
*divide by two

sta
OCH
*to output compare

lda
byte+1
*get low byte

ror
*use ror to get carry in

sta
OCL
to output compare

lda
OCH

lsr

sta
OCH

lda
OCL

ror
```

```
sta
OCL
*finish divide by four

lda
#$7F
*mask off input capture

sta
TSR
*by writing to timer status

bclr
flags,0
*clear first edge flag bit
  endint
rti
  *output compare service routine. For each interrupt that oc-
curs,
  *sample the input line and shift the appropriate data bit into
the
  *data register. Do so for all six bits, then word is complete.
  *
  bitint
lda
PADR
*get the data bit value

lsl
*get the data to carry

lda
data
*get the data byte

rol
*and assemble the byte

sta
data
*to data

dec
count
*check to see if all done

beq
endbit
*exit if done

lda
OCL

add
byte+1
*set up the next interrupt

sta
OCL
*write to OCL resets flag

lda
OCH

adc
byte
*use add with carry to do 16 bit

sta
OCH

rti
  endbit
lda
data
*get the word

coma
*remember the data was inverted

and
#$5F
*and there were only 6 bits

sta
data

bset
flags,1
*word ready flag bit

rti
```

TECH BRIEFS

SIMPLIFIED REMOTE CONTROL CIRCUITS

DAVID BABIN
Application Engineering Manager
Motorola Inc.
Austin, TX

A new chip now provides a simple way to design remotely-controlled on/off devices such as valves and relays. The IC (MC145030) combines serial encoding and decoding functions that form the heart of many remote control circuits.

The 20-pin chip also contains an input amplifier, an output flip-flop, power-on reset, and an oscillator requiring only external *RC* components. No crystals or ceramic resonators are required. The IC is optimized for use in harsh industrial environments, operating from a 2 to 6 V supply over a temperature range of −40 to 85°C. Standby current drain is 100 μA maximum at room temperature while operating current is at most 2.5 mA at the worst-case supply voltage.

A typical remote control application would use the IC in both the controlling and receiving stations. At the master end, the chip would encode the nine-bit parallel address input and send this address onto a serial output line via a three-state encoder-out pin. This output returns to a high-impedance state after encoding is complete.

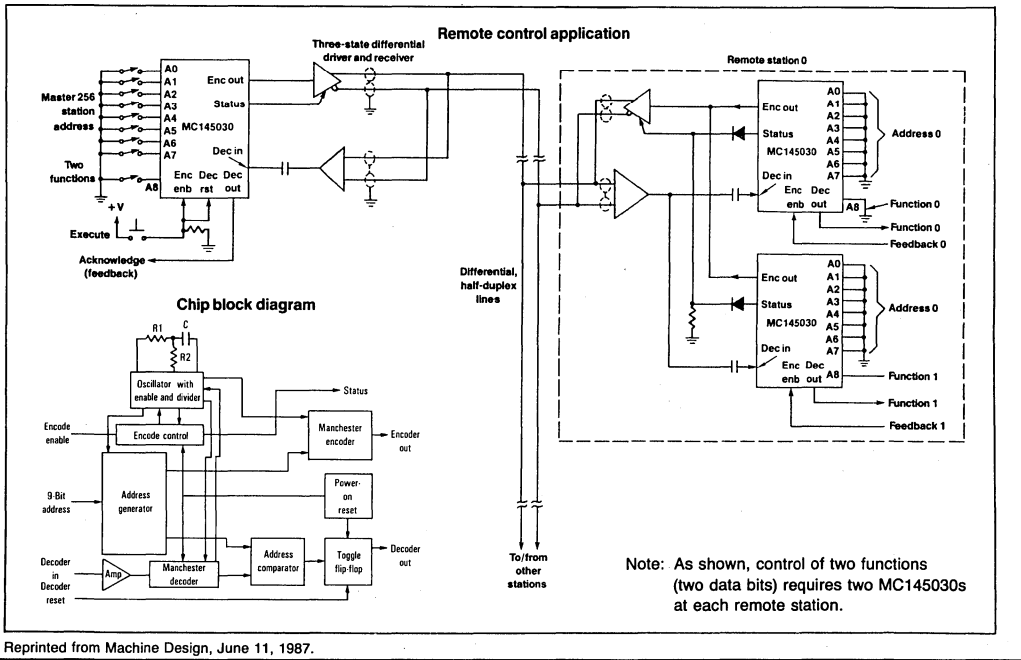
At the receiving end, another MC145030 chip serves as a decoder. The serial stream is received from the master and the address information is decoded. The IC would then compare this decoded address to the address applied to its own address lines. If the two addresses match, the chip would actuate the decoder-out line which would normally be connected to some output device such as a solenoid.

An output device toggles the receiver chip's encoder-enable input as an acknowledgment of either the output signal or of a completed operation. Once the chip senses this acknowledgment, the address is sent back to the master station over the serial line.

The master station treats this address as an acknowledgment that the output operation took place. The chip would compare the information with the address applied on its address lines. If the two addresses matched, decoder-out would toggle.

The master chip can activate any of 512 decoding stations in this manner. Alternatively, the designer can partition the nine address bits into address and data. This allows each remote station to perform several functions as in the remote control application shown.

The serial output of the encoder is in the form of Manchester Code,



Note: As shown, control of two functions (two data bits) requires two MC145030s at each remote station.

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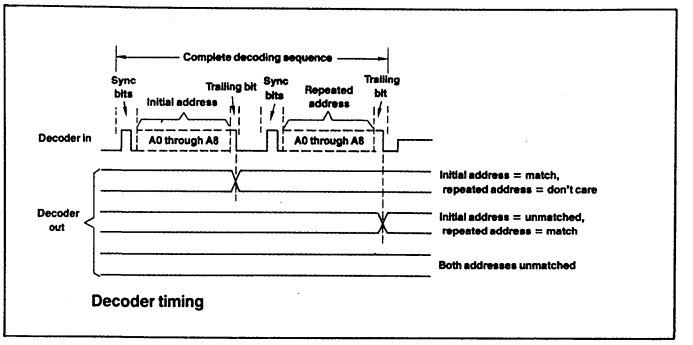
also known as Biϕ-L (biphase-level) code. The encoding technique allows both data and sync information to flow on one signal line instead of two.

The encode-enable input may connect directly to a push-button switch and pull-down resistor without external debounce circuitry. A rising edge on encode-enable aborts any decoding sequence in progress and starts an encoding sequence. Decoding functions are inhibited during this sequence, allowing half-duplex operation.

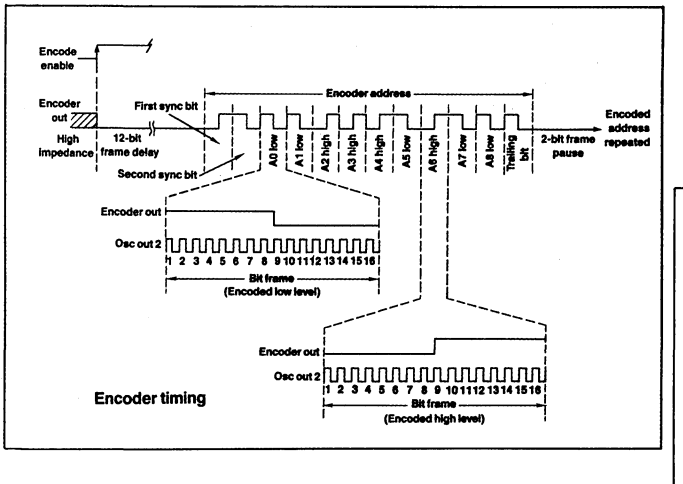
The chip issues an address twice during an encoding sequence to guard against system electrical noise problems. A status pin, when high, indicates that the device is encoding. The device is in standby or decoding when status is low.

Address inputs on the IC have on-chip pull-up devices which are inactive during standby to reduce power consumption. These pull-ups facilitate direct connection of SPST switches or jumpers to V_{ss}.

The decoder in pin is the input to the on-chip amplifier. Signal levels as low as 200 mV_{p-p} may capacitively couple through a 0.1 μF capacitor to this pin. The source impedance driving the series capacitor may be as high as 5 kΩ. Capacitive coupling provides proper amplifier biasing on chip. ■



Decoder timing



Encoder timing

Example RC values

f_{osc} (approx.)	R1	R2	C	Encode enable switch debounce time (approx.) *
452 kHz	30kΩ	5.6kΩ	100pF	1.3 ms
220 kHz	47kΩ	10kΩ	100 pF	2.8 ms
70 kHz	47kΩ	10kΩ	510 pF	8.7 ms
4.1 kHz	330kΩ	47kΩ	2,200pF	148 ms

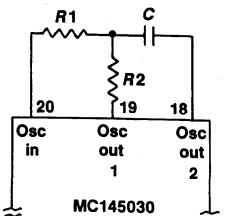
* And max. time for an encoding sequence.

Guidelines: 100 pF≤C≤0.1 μF
10kΩ≤R2≤500kΩ
2 (R2)<R1<10(R2)
R1 ≤ 1MΩ

CHOOSING THE R AND C

For design purposes, the maximum difference in oscillator frequency between encoding and decoding MC145030 chips should be no more than ±11%. Ambient temperature and supply voltage difference between the ICs affect this frequency difference. Tolerances of frequency-determining components $R2$ and C are calculated by a rule of thumb: $\Delta R2 + \Delta C + \Delta f_{IC} + \Delta f_{temp} + \Delta f_{sup} \leqq \pm 11\%$, where $R2$ = tolerance of $R2$, %; C = tolerance of C, %; f_{IC} = IC frequency variation from part to part (expected value = ±4%); f_{temp} = IC frequency variation over temperature (expected value = ±2% at 25°C ±40°); f_{sup} = IC frequency variation with supply (expected value = ±2% at 5 V ±0.5 V).

For example, from the above variances, $\Delta R2 + \Delta C + (\pm 4\%) + (\pm 2\%) + (\pm 2\%) \leqq \pm 11\%$; therefore, $\Delta R2 + \Delta C \leqq \pm 3\%$. Choose $R2$ with a ±1% tolerance and C with a ±2% tolerance. Polystyrene or mylar capacitors are recommended. $R1$ may be ±5%.



Glossary 5

5

Glossary of Terms and Abbreviations

The list contains terms found in this and other Motorola publications concerned with Motorola Semiconductor products for Communications.

A-Law — A European companding/encoding law commonly used in PCM systems.

A/B Signaling — A special case of 8th-bit (LSB) signaling in a μ-law system that allows four logic states to be multiplexed with voice on PCM channels.

A/D (analog-to-digital) converter (ADC) — A converter that uniquely represents all analog input values within a specified total input range by a limited number of digital output codes, each of them exclusively representing a fractional part of the total analog input range.

Aliasing Noise — A distortion component that is created when frequencies present in a sampled signal are greater than one-half the sample rate.

Answer Back — A signal sent by receiving data-processing device in response to a request from a transmitting device, indicating that the receiver is ready to accept or has received data.

Anti-aliasing Filter — A filter (normally low pass) that band limits an input signal *before* sampling to prevent aliasing noise.

Asynchronous — A mode of data transmission in which the time occurrence of the bits within each character or block of characters relates to a fixed time frame, but the start of each character or block of characters is not related to this fixed time frame.

Attenuation — A decrease in magnitude of a communication signal.

Bandwidth — The information-carrying frequencies between the limiting frequencies of a communication line or channel.

Baseband — The frequency band occupied by information-bearing signals before combining with a carrier in the modulation process.

Baud — A unit of signaling speed equal to the number of discrete signal conditions or events per second. This refers to the physical symbols/second used within a transmission channel.

Bit Rate — The speed at which data bits are transmitted over a communication path, usually expressed in bits per second. A 9600 bps terminal is a 2400 baud system with 4 bits/baud.

Blocking — A condition in a switching system in which no paths or circuits are available to establish a connection to the called party even though it is not busy, resulting in a busy tone to the calling party.

BORS(C)HT — Battery, Overvoltage, Ringing, Supervision, (Codec), Hybrid, Test; the functions performed by a subscriber line card in a telephone exchange.

Broadband — A transmission facility whose bandwidth is greater than that available on voice-grade facilities. (Also called wide band.)

C Message — A frequency weighting that evaluates the effects of noise based on its annoyance to the "typical" subscriber of standard telephone service or the effects of noise (background and impulse) on voice-grade data service.

Carrier — An analog signal of fixed amplitude and frequency that combines with an information-bearing signal by modulation to produce an output signal suitable for transmission.

CCITT — Consultative Committee for International Telephone and Telegraph; an international standards group of European International Telecommunications Union.

CCSN — Common Channel Signaling Network.

Central Office (CO) — A main telephone office, usually within a few miles of a subscriber, that houses switching gear; commonly capable of handling about 10,000 subscribers.

Channel Bank — Communication equipment commonly used for multiplexing voice-grade channels into a digital transmission signal (typically 24 channels in the U.S. and 30 channels in Europe).

CIDCW — Calling Identity Delivery on Call Waiting; a subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party while the called party is off-hook.

CLASS — Custom Local Area Signaling Service; a set of services, enhancements, provided to TELCO customers which may include CND, CNAM, Message Waiting, and other features.

CLID — Calling Line IDentification; a subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party.

CNAM — Calling Name Delivery; a subscriber feature which allows for the display of the time, date, number, and name of the caller to the called party.

CND — Calling Number Delivery; a subscriber feature which allows for the display of the time, date, number, and possible other information about the caller to the called party.

CODEC — COder-DECoder; the A/D and D/A function on a subscriber line card in a telephone exchange.

COFIDEC — COder-FIlter-DECoder; the combination of a codec, the associated filtering, and voltage references required to code and decode voice in a subscriber line card.

Common Mode Rejection — The ability of a device having a balanced input to reject a voltage applied simultaneously to both differential-input terminals.

Companding — The process in which dynamic range compression of a signal is followed by expansion in accordance with a given transfer characteristic (companding law) which is usually logarithmic.

Compander — A combination of a compressor at one point in a communication path for reducing the amplitude range of signals, followed by an expander at another point for restoring the original amplitude range, usually to improve the signal-to-noise ratio.

Conference Call — A call between three or more stations, in which each station can carry on a conversation simultaneously.

CPE — Customer Premise Equipment; this could be a POTS phone, answering machine, fax machine, or any number of other devices connected to the PSTN.

Crosspoint — The operating contacts or other low-impedance-path connection over which conversations can be routed.

Crosstalk — The undesired transfer of energy from one signal path to another.

CSN — Circuit Switched Network.

CTS — Clear to send; a control signal between a modem and a controller used to initiate data transmission over a communication line.

CVSD — Continuous Variable Slope Delta (modulation); a simple technique to converting an analog signal (like voice) into a serial bit stream.

D3 — D3 channel bank; a specific generation of AT&T 24-channel PCM terminal that multiplexes 24 voice channels into a 1.544 MHz digital bit stream. The specifications associated with D3 channel banks are the basis for all PCM device specifications.

D/A (digital-to-analog) converter (DAC) — A converter that represents a limited number of different digital input codes by a corresponding number of discrete analog output values.

Data Compression — A technique that provides for the transmission of fewer data bits than originally required without information loss. The receiving location expands the received data bits into the original bit sequence.

dB (decibel) — A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

10 x log (P1/P2) for power measurements, and

20 x log (V1/V2) for voltage measurements.

dBm — An indication of signal power. 1.0 mW across 600 Ω, or 0.775 volts rms, is defined as 0 dBm. Any other voltage level is converted to dBm by:

dBm = 20 x log (Vrms/0.775), or

dBm = [20 x log (Vrms)] + 2.22.

dBmO — Signal power measured at a point in a standard test tone level at the same point.

i.e., dBmO = dBm = dBr

where dBr is the relative transmission level, or level relative to the point in the system defined as the zero transmission level point.

dBmOp — Relative power expressed in dBmp. (See dBmO and dBmp.)

dBmp — Indicates dBm measurement made with a psophometric weighting filter.

dBrn — Relative signal level expressed in decibels above reference noise, where reference noise is 1 pW. Hence, 0 dBrn = 1 pW = – 90 dBm.

dBrnC — Indicates dBrn measurement made with a C-message weighting filter. (These units are most commonly used in the U.S., where psophometric weighting is rarely used.)

dBrnc0 — Noise measured in dBrnc referenced to zero transmission level.

Decoding — A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample.

Delay Distortion — Distortion that occurs on communication lines due to the different propagation speeds of signals at different frequencies, measured in microseconds of delay relative to the delay at 1700 Hz. (This type of distortion does not affect voice communication, but can seriously impair data transmission.)

Delta Modulation — A simple digital coding technique that produces a serial bit stream corresponding to changes in analog input levels; usually utilized in devices employing continuously variable-slope delta (CVSD) modulation.

Demodulator — A functional section of a modem that converts received analog line signals to digital form.

DN — Directory Number.

Digital Telephone — A telephone terminal that digitizes a voice signal for transmission and decodes a received digital signal back to a voice signal. (It will usually multiplex 64 kbps voice and separate data inputs at multiples of 8 kbps.)

Distortion — The failure to reproduce an original signal's amplitude, phase, delay, etc. characteristics accurately.

DPSK — Differential Phase Shift Keying; a modulation technique for transmission where the frequency remains constant but phase changes will occur from 90°, 180°, and 290° to define the digital information.

DTMF — Dual Tone Multi-Frequency. It is the "tone dialing" system based on outputting two non-harmonic related frequencies simultaneously to identify the number dialed. Eight frequencies have been assigned to the four rows and four columns of a typical keypad.

Duplex — A mode of operation permitting the simultaneously two-way independent transmission of telegraph or data signals.

Echo — A signal that has been reflected or returned as a result of impedance mismatches, hybrid unbalance, or time delay. Depending upon the location of impedance irregu-

larities and the propagation characteristics of a facility, echo may interfere with the speaker/listener or both.

Echo Suppressor — A device used to minimize the effect of echo by blocking the echo return currents; typically a voice-operated gate that allows communication one way at a time.

Encoder (PCM) — A device that performs repeated sampling, compression, and A/D conversion to change an analog signal to a serial stream of PCM samples representing the analog signal.

Equalizer — An electrical network in which phase delay or gain varies with frequency to compensate for an undesired amplitude or phase characteristic in a frequency-dependent transmission line.

ET — Exchange Termination (C.O. Switch).

FDM — Frequency-Division Multiplex; a process that permits the transmission of two or more signals over a common path by using a different frequency band for each signal.

Four Wire Circuit — The portion of a telephone, or central office, that operates on two pairs of wires. One pair is for the transmit path (generally from the microphone), and one pair is for the receive path (generally from the receiver).

Frame — A set of consecutive digit time slots in which the position of each digit slot can be identified by reference to a frame alignment. The frame alignment signal does not necessarily occur, in whole or in part, in each frame.

Full Duplex — A mode of operation permitting simultaneous transmission of information between two locations in both directions.

Gain — The change in signal amplitude (increase or decrease) after passing through an amplifier, or other circuit stage. Usually expressed in dB, an increase is a positive number, and a decrease is a negative number.

Gain Tracking Error — The variation of gain from a constant level (determined at 0 dBm input level) when measuring the dependence of gain on signal level by comparing the output signal to the input signal over a range of input signals.

HDLC — High-Level Data Link Control; a CCITT standard data communication line protocol.

Half Duplex — A transmission system that permits communication in one direction at a time. CB ratios, with "push-to-talk" switches, and voice-activated speakerphones, are half duplex.

Handset — A rigid assembly providing both telephone transmitter and receiver in a form convenient for holding simultaneously to mouth and ear.

Hookswitch — A switch that connects the telephone circuit to the subscriber loop. The name derives from old telephones where the switch was activated by lifting the receiver off and onto a hook on the side of the phone.

Idle Channel Noise (ICN) — The total signal energy measured at the output of a device or channel under test when the input of the device or channel is grounded (often a wide-band noise measurement using a C-message weighting filter to band-limit the output noise).

Intermodulation — The modulation of the components of a complex wave by each other (in a nonlinear system).

Intermodulation Distortion — An analog line impairment when two frequencies interact to create an erroneous frequency, in turn distorting the data signal representation.

IRED — Infrared. Used as a wireless link for remote control or to transfer data.

ISDN — Integrated Services Digital Network; a communication network intended to carry digitized voice and data multiplexed onto the public network.

Jitter — A type of analog communication line distortion caused by abrupt, spurious signal variation from a reference timing position, and capable of causing data transmission errors, particularly at high speeds. (The variation can be in amplitude, time, frequency, or phase.)

Key System — A miniature PABX that accepts 4 to 10 lines and can direct them to as many as 30 telsets.

μ-law — A companding law accepted as the North American standard for PCM based systems.

LAN — Local Area Network; a data-only communication network between data terminals using a standard interface to the network.

Line — The portion of a circuit external to an apparatus that consists of the conductors connecting the apparatus to the exchange or connecting two exchanges.

Line Length Compensation — Also referred to as loop length compensation, it involves changing the gain of the transmit and receive paths, within a telephone, to compensate for different signal levels at the end of different line lengths. A short line (close to the CO) will attenuate signals less, and therefore less gain is needed. Compensation circuits generally use the loop current as an indication of the line length.

Longitudinal Balance — The common-mode rejection of a telephone circuit.

Loop — The loop formed by the two subscriber wires (Tip and Ring) connected to the telephone at one end, and the central office (or PBX) at the other end. Generally it is a floating system, not referred to ground, or ac power.

Loopback — Directing signals back toward the source at some point along a communication path.

Loop Current — The dc current that flows through the subscriber loop. It is typically provided by the central office or PBX, and ranges from 20 to 120 mA.

LT — Line Termination (Line Card).

MCU — MicroComputer Unit (also MicroController Unit).

MPU — MicroProcessor Unit.

Mu-Law — A companding/encoding law commonly used in U.S. (same as μ-law).

MUX — Multiplex or multiplexer.

Modem — MOdulator-DEModulator; a unit that modulates and demodulates digital information from a terminal or computer port to an analog carrier signal for passage over an analog line.

Multiplex — To simultaneously transmit two or more messages on a single channel.

NT1 — Network Termination 1 (OSI Layer 1 Only).

NT2 — Network Termination 2 (OSI Layers 2 and 3).

Off-hook — The condition when the telephone is connected to the phone system, permitting loop current to flow. The central office detects the dc current as an indication that the phone is busy.

On-hook — The condition when the telephone's dc path is open, and no dc loop current flows. The central office regards an on-hook phone as available for ringing.

PABX — Private Automatic Branch Exchange; a customer-owned, switchable telephone system providing internal and/or external station-to-station dialing.

Pair — The two associated conductors that form part of a communication channel.

Pass-band Filter — A filter used in communication systems that allows only the frequencies within a communication channel to pass, and rejects all frequencies outside the channel.

PBX — Private Branch Exchange; a class of service in standard Bell System terminology that typically provides the same service as PABX.

PCM — Pulse Code Modulation; a method of transmitting data in which signals are sampled and converted to digital words that are then transmitted serially, typically as 8-bit words.

Phase Jitter — Abrupt, spurious variations in an analog line, generally caused by power and communication equipment along the line that shifts the signal phase relationship back and forth.

PLL — Phase-Locked Loop.

PLL Frequency Synthesizer — Phase-locked loop frequency synthesizer. A frequency synthesizer utilizing a closed loop, as opposed to DDS (direct digital synthesis) which is not a closed loop.

POTS — Plain Old Telephone Service.

Propagation Delay — The time interval between specified reference points on the input and output voltage waveforms.

Psophometric Weighting — A frequency weighting similar to C-Message weighting that is used as the standard for European telephone system testing.

PSN — Packet Switched Network.

PSTN — Public Switched Telephone Network.

Pulse Dialer — A device that generates pulse trains corresponding to digits or characters used in impulse or loop-disconnect dialing.

Quantizing Noise — Signal-correlated noise generally associated with the quantizing error introduced by A/D and D/A conversions in digital transmission systems.

REN — Ringer Equivalence Number; an indication of the impedance, or loading factor, of a telephone bell or ringer circuit. An REN of 1.0 equals about 8 kΩ. The Bell system typically permits a maximum of 5.0 REN (1.6 kΩ) on an individual subscriber line. A minimum REN of 0.2 (40 kΩ) is required by the Bell system.

Repeater — An amplifier and associated equipment used in a telephone circuit to process a signal and retransmit it.

Repertory Dialer — A dialer that stores a repertory of telephone numbers and dials any one of them automatically on request.

Ring — One of the two wires connecting the central office to a telephone. The name derives from the ring portion of the plugs used by operators (in older equipment) to make the connection. Ring is traditionally negative with respect to Tip.

RTS — Request To Send; an EIA-232 control signal between a modem and user's digital equipment that initiates the data transmission sequence on a communication line.

Sampling Rate — The frequency at which the amplitude of an analog signal is gated into a coder circuit. The Nyquist sampling theorem states that if a band-limited signal is sampled at regular intervals and at a rate equal to or greater than twice the highest frequency of interest, the sample contains all the information of the original signal. The frequency band of interest in telephony ranges from 300 to 3400 Hz, so a sampling rate of 8 kHz provides dc to 4000 Hz reproduction.

SCU — Subscriber Channel Unit; the circuitry at a telephone exchange associated with an individual subscriber line or channel.

Sidetone — The sound fed back to the receiver as a result of speaking into the microphone. It is a natural consequence of the 2-to-4 wire conversion system. Sidetone was recognized by Alexander Graham Bell as necessary for a person to be able to speak properly while using a handset.

Signaling — The transmission of control or status information between switching systems in the form of dedicated bits or channels of information inserted on trunks with voice data.

Signal-to-Distortion Ratio (S/D) — The ratio of the input signal level to the level of all components that are present when the input signal (usually a 1.020 kHz sinusoid) is eliminated from the output signal (e.g., by filtering).

SLIC — Subscriber Line Interface Circuit; a circuit that performs the 2-to-4 wire conversion, battery feed, line supervision, and common mode rejection at the central office (or PBX) end of the telephone line.

SOG package — Small-Outline Gull-wing package; formerly SOIC with gull-wing leads. This package has leads which fold out from the body.

SOJ package — Small-Outline J-lead package; formerly SOIC with J leads. This package has leads which are tucked under the body.

Speech Network — A circuit that provides 2-to-4 wire conversion, i.e., connects the microphone and receiver (or the transmit and receive paths) to the Tip and Ring phone lines. Additionally it provides sidetone control, and in many cases, the dc loop current interface.

Subscriber Line — The system consisting of the user's telephone, the interconnecting wires, and the central office equipment dedicated to that subscriber (also referred to as a loop).

Switchhook — A synonym for hookswitch.

Syn (Sync) — (1) A bit character used to synchronize a time frame in a time-division multiplexer. (2) A sequence used by a synchronous modem to perform bit synchronization or by a line controller for character synchronization.

Synchronous Modem — A modem that uses a derived clocking signal to perform bit synchronization with incoming data.

T1 Carrier — A PCM system operating at 1.544 MHz and carrying 24 individual voice-frequency channels.

TA — Terminal Adatper.

Talkdown — Missed signals in the presence of speech. Commonly used to describe the performance of a DTMF receiver when it fails to recognize a valid DTMF tone due to cancellation of that tone by speech.

Talkoff — False detections caused by speech. Commonly used to describe the performance of a DTMF receiver when speech, emulating DTMF, causes the receiver to believe it has detected a valid DTMF tone.

Tandem Trunk — See trunk.

Telephone Exchange — A switching center for interconnecting the lines that service a specific area.

TE1 — Terminal Equipment 1 (ISDN Terminal).

TE2 — Terminal Equipment 2 (Non-ISDN Terminal).

TELETEX — A text communication service between entirely electronic work stations that will gradually replace TELEX with the introduction of the digital network. (Not to be confused with teletext.)

TELETEXT — The name usually used for broadcast text (and graphics) for domestic television reception. (Not to be confused with teletex.)

Time-Division Multiplex — A process that permits the transmission of two or more signals over a common path by using a different time interval for each signal.

Tin Cans and String — A *crude* analog communications system commonly used to introduce voice communications to children.

Tip — One of the two wires connecting the central office to a telephone. The name derives from the tip of the plugs used by operators (in older equipment) to make the connection. Tip is traditionally positive with respect to ring.

Tone Ringer — The modern solid state equivalent of the old electromechanical bell. It provides the sound when the central office alerts the subscriber that someone is calling. Ringing voltage is typically 80–90 volts rms, 20 Hz.

Trunk — A telephone circuit or channel between two central offices or switching entities.

TSAC — Time Slot Assigner Circuit; a circuit that determines when a CODEC will put its 8 bits of data on a PCM bit stream.

TSIC — Time Slot Interchange Circuit; a device that switches digital highways in PCM based switching systems; a "digital" crosspoint switch.

Twist — The amplitude ratio of a pair of DTMF tones. (Because of transmission and equipment variations, a pair of tones that originated equal in amplitude may arrive with a considerable difference in amplitude.)

Two Wire Circuit — Refers to the two wires connecting the central office to the subscriber's telephone. Commonly referred to as Tip and Ring, the two wires carry both transmit and receive signals in a differential manner.

UDLT — Universal Digital Loop Transceiver; a Motorola originated name for a voice/data transceiver circuit.

VCO — Voltage-controlled oscillator. Input is a voltage; output is a sinusoidal waveform.

VCM — Voltage-controlled multivibrator. Input is a voltage; output is a square wave.

Voice Frequency — A frequency within that part of the audio range that is used for the transmission of speech of commercial quality (i.e., 300–3400 Hz).

Weighting Network — A network whose loss varies with frequency in a predetermined manner.

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Handling and Design Guidelines

6

6

Handling and Design Guidelines

HANDLING PRECAUTIONS

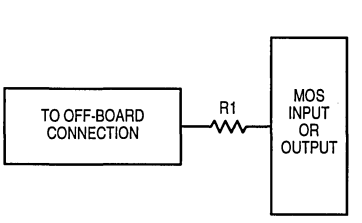
All CMOS devices have an insulated gate that is subject to voltage breakdown. The high-impedance gates on the devices are protected by on-chip networks. However, these on-chip networks do not make the IC immune to electrostatic damage (ESD). Laboratory tests show that devices may fail after one very high voltage discharge. They may also fail due to the cumulative effect of several discharges of lower potential.

Static-damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged are the easiest to detect because the input or output has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS}, or open-circuited. The effect is that the device is no longer functional. Less severe cases are more difficult to detect because they appear as intermittent failures or degraded performance. Static damage can often increase leakage currents.

CMOS devices are not immune to large static voltage discharges that can be generated while handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4–15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed.

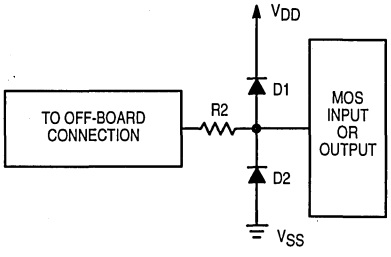
1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low-impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. A circuit board containing CMOS or devices is merely an extension of the device and the same handling precautions apply. Contacting connectors wired directly to devices can cause damage. Plastic wrapping should be avoided. When external connections to a PC board address pins of CMOS integrated circuits, a resistor should be used in series with the inputs or outputs. The limiting factor for the series resistor is the added delay caused by the time constant formed by the series resistor and input capacitance. This resistor will help limit accidental damage if the PC board is removed and brought into contact with static generating materials. For convenience, equations for added propagation delay and rise time effects due to series resistance size are given in Figure 1.
5. All CMOS devices should be stored or transported in materials that are antistatic. Devices must not be inserted into conventional plastic "snow", styrofoam or

Figure 1. Networks for Minimizing ESD and Reducing CMOS Latch Up Susceptibility



Advantage: Requires minimal board area.

Disadvantage: R1 > R2 for the same level of protection, therefore rise and fall times, propagation delays, and output drives are severely affected.



Advantage: R2 < R1 for the same level of protection. Impact on ac and dc characteristics is minimized.

Disadvantage: More board area, higher initial cost.

NOTE: These networks are useful for protecting the following:

A. digital inputs and outputs
B. analog inputs and outputs
C. 3-state outputs
D. bidirectional (I/O) ports

EQUATION 1 – PROPAGATION DELAY VS SERIES RESISTANCE

$$R \approx \frac{t}{C \bullet k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.33 for devices with TTL input levels (switch point ≈ 1.3 V)
k = 0.7 for devices with CMOS input levels (switch point ≈ 50% V_{DD}).

EQUATION 2 – RISE TIME VS SERIES RESISTANCE

$$R \approx \frac{t}{C \bullet k}$$

where:
R = the maximum allowable series resistance in ohms
t = the maximum tolerable propagation delay in seconds
C = the board capacitance plus the driven device's input capacitance in farads
k = 0.7 for devices with TTL input levels (switch point ≈ 1.3 V)
k = 2.3 for devices with CMOS input levels (switch point ≈ 50% V_{DD}).

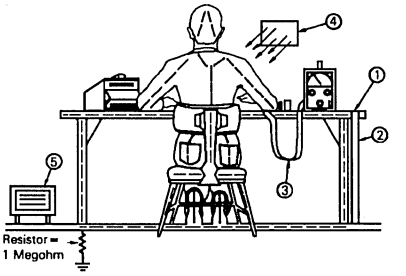
plastic trays, but should be left in their original container until ready for use.

6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 2.
7. Nylon or other static generating materials should not come in contact with CMOS circuits.
8. If automatic handling is being used, high levels of static electricity may be generated by the movement of devices, belts, or boards. Reduce static build-up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, and sides of IC packages must be grounded metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and devices must be contained on or in conductive material.
10. When lead-straightening or hand-soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations.
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.
12. The following steps should be observed during board cleaning operation.
    a. Vapor degreasers and baskets must be grounded to an earth ground. Operators must likewise be grounded.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when module circuits are grounded and a static eliminator is directed at the module.
13. The use of static detection meters for line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check the equipment setup for proper polarity of voltage before conducting parametric or functional testing.

RECOMMENDED READING

"Total Control of the Static in Your Business"
Available by writing to:
3M
Static Control Systems
Building A145-3N-01
P.O. Box 2963
Austin, TX 78769-2963
Or calling:
1-800-328-1368

Figure 2. Typical Manufacturing Work Station



NOTES:
1. 1/16 inch conductive sheet stock covering bench top work area.
2. Ground strap.
3. Wrist strap in contact with skin.
4. Static neutralizer. (Ionized air blower directed at work.) Primarily for use in areas where direct grounding is impractical.
5. Room humidifier. Primarily for use in areas where the relative humidity is less than 45%. Caution: building heating and cooling systems usually dry the air causing the relative humidity inside of buildings to be less than outside humidity.

CMOS LATCH UP

Latch up will not be a problem for most designs, but the designer should be aware of it, what causes it, and how to prevent it.

Figure 3 shows the layout of a typical CMOS inverter and Figure 4 shows the parasitic bipolar devices that are formed. The circuit formed by the parasitic transistors and resistors is the basic configuration of a silicon controlled rectifier, or SCR. In the latch-up condition, transistors Q1 and Q2 are turned on, each providing the base current necessary for the other to remain in saturation, thereby latching the devices on. Unlike a conventional SCR, where the device is turned on by applying a voltage to the base of the NPN transistor, the parasitic SCR is turned on by applying a voltage to the emitter of either transistor. The two emitters that trigger the SCR are the same point, the CMOS output. Therefore, to latch up the CMOS device, the output voltage must be greater than V_{DD} + 0.5 Vdc or less than – 0.5 Vdc and have sufficient current to trigger the SCR. The latch-up mechanism is similar for the inputs.

Once a CMOS device is latched up, if the supply current is not limited, the device will be destroyed. Ways to prevent such occurrences are listed below.

1. Ensure that inputs and outputs are limited to the maximum rated values, as follows:
   – 0.5 ≤ V_{in} ≤ V_{DD} + 0.5 Vdc referenced to V_{SS}
   – 0.5 ≤ V_{out} ≤ V_{DD} + 0.5 Vdc referenced to V_{SS}
   $|I_{in}|$ ≤ 10 mA
   $|I_{out}|$ ≤ 10 mA when transients or dc levels exceed the supply voltages.
2. If voltage transients of sufficient energy to latch up the device are expected on the outputs, external protection diodes can be used to clamp the voltage. Another method of protection is to use a series resistor to limit the expected worst case current to the Maximum Ratings values (see Figure 1).
3. If voltage transients are expected on the inputs, protection diodes may be used to clamp the voltage or a series resistor may be used to limit the current to a level less than the maximum rating of I_{in} = 10 mA (see Figure 1).
4. Sequence power supplies so that the inputs or outputs of CMOS devices are not powered up first (e.g., recessed edge connectors may be used in plug-in board applications and/or series resistors).
5. Power supply lines should be free of excessive noise. Care in board layout and filtering should be used.
6. Limit the available power supply current to the devices that are subject to latch-up conditions. This can be accomplished with the power supply filtering network or with a current-limiting regulator.

Figure 3. CMOS Wafer Cross Section

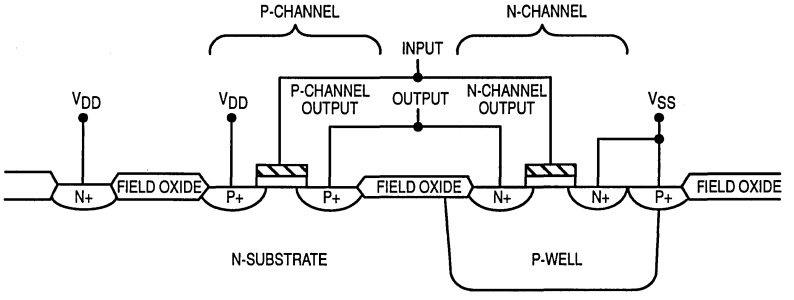
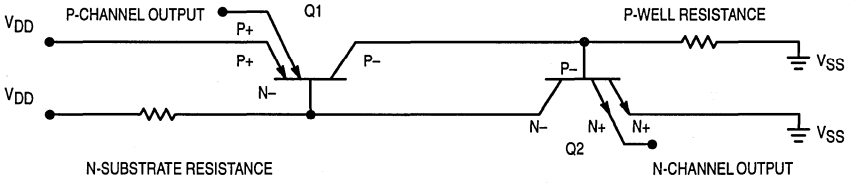


Figure 4. Latch Up Circuit Schematic



Quality and Reliability

7

7

Quality In Manufacturing

QUALITY IN DESIGN

Motorola's quality activity starts at the product design stage. It is Motorola's philosophy to "design in" reliability. At all development points of any new design reliability oriented guidelines are continuously used to ensure that a thoroughly reliable part is ultimately produced. This is demonstrated by the excellent in-house reliability testing results obtained for all Motorola's semiconductor products and, more importantly, by our numerous customers.

MATERIAL INCOMING CONTROLS

Each vendor is supplied with a copy of the Motorola Procurement Specification which must be agreed in detail between both parties before any purchasing agreement is made. This is followed by a vendor appraisal report whereby each vendor's manufacturing facility is visited by Motorola Quality Engineers responsible for ensuring that the vendor has a well organized and adequately controlled manufacturing process capable of supplying the high quality material required to meet the Motorola Incoming Inspection Specification. Large investments have and are continuously being made and Quality Improvement programs developed with our main suppliers concerning:

Masks — Silicon — Piece-parts — Chemical products — Industrial gas, etc.

Each batch of material delivered to Motorola is quarantined at Goods-in until the Incoming Quality Organization has subjected adequate samples to the incoming detailed inspection specification. In the case of masks, this will include mask inspection for:

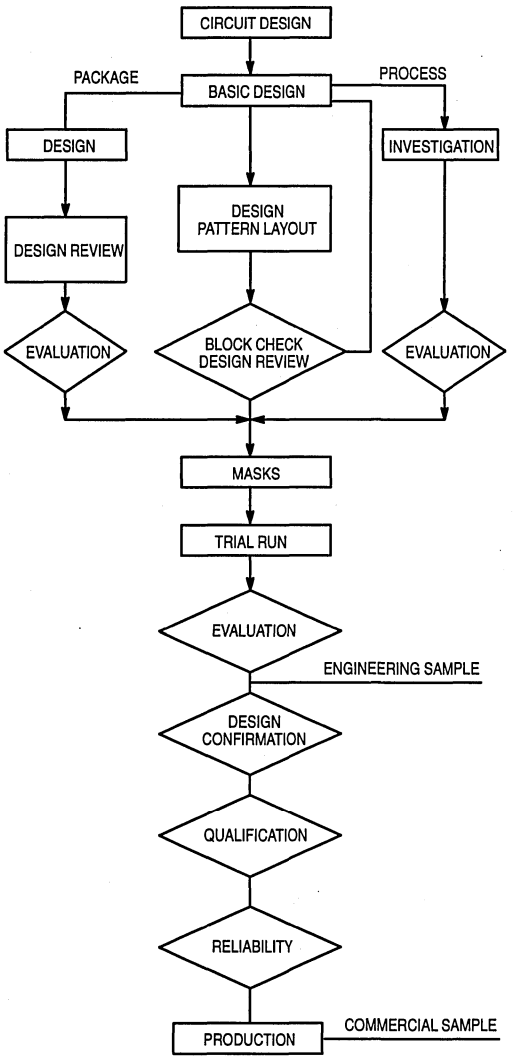
1. Defect Density
2. Intermask Alignment
3. Mask Revision
4. Device to Device Alignment
5. Mask Type

Silicon will undergo the following inspections:

1. Type "N" or "P"
2. Resistivity
3. Resistivity Gradient
4. Defects
5. Physical Dimensions
6. Dislocation Density

Incoming chemicals are also controlled to very rigorous standards. Many are submitted to in-house chemical analysis where the supplier's conformance to specification is meticulously checked. In many cases, line tests are performed before final acceptance. A major issue and responsibility for the Incoming Quality Department is to ensure that the most disciplined safety factors have been employed with regard to chemicals. Chemicals can and are often rejected because safety standards have not been deemed acceptable.

NEW PRODUCT TYPICAL DESIGN FLOW



THIS BASIC DESIGN FLOW-CHART OMITS SOME FEEDBACK LOOPS FOR SIMPLICITY

The Six Sigma Challenge

Motorola's expressed objective is the achievement of "error free performance" in products and services. The high quality level of the product-line outputs, followed by stringent outgoing quality control, readily assures this objective. But error-free output from the product lines themselves is a matter that continues to demand full attention at all levels of production, design and administration. This far more stringent requirement has a two-fold goal:

1. To further improve ultimate product reliability — experience has proved that products **designed** for 100% conformance to specifications are far less subject to field failure than products **selected** to a given level of performance.
2. To reduce waste — thereby making the end-product more cost competitive.

Whether or not one-hundred percent perfection is consistently achievable remains subject to conjecture. Motorola's already low reject rates, however, warrant a high level of confidence that the goal can be met, and milestones toward this objective have been firmly established. They call for a hundred-fold performance improvement in output by 1991, and a Six Sigma Capability by 1992.

Six Sigma Capability — not yet zero defects, but 99.9999998% perfection in both product and in customer services.

Why Six Sigma?

Each process attempts to reproduce its characteristics identically from unit to unit. Inherent in each process, however, there are variations in conditions and in materials that are uncontrollable and unalterable. In all cases, therefore, the unit-to-unit output characteristics vary somewhat from the ideal (design target).

The performance of a product is determined by how much margin exists between the design specifications and the actual value of that specification. For some processes, such as those using real-time feedback to control the output, the variations can be quite small; for others they may be quite large. Many of the parametric data of a given specification tend to follow the normal distribution curve shown in Figure 1.

Variation of the process is measured in Standard Deviations (Sigma) from the Mean. The normal deviation, defined as process width, is ± 3 Sigma about the mean, representing a yield of 99.73%. But is ± 3 Sigma good enough as an overall specification? Statistically, with a ± 3 sigma deviation, approximately 2700 parts per million still fall outside acceptable performance limits. Clearly, for a product to be built virtually defect free it must be designed with a component yield that is significantly better than ± 3 Sigma.

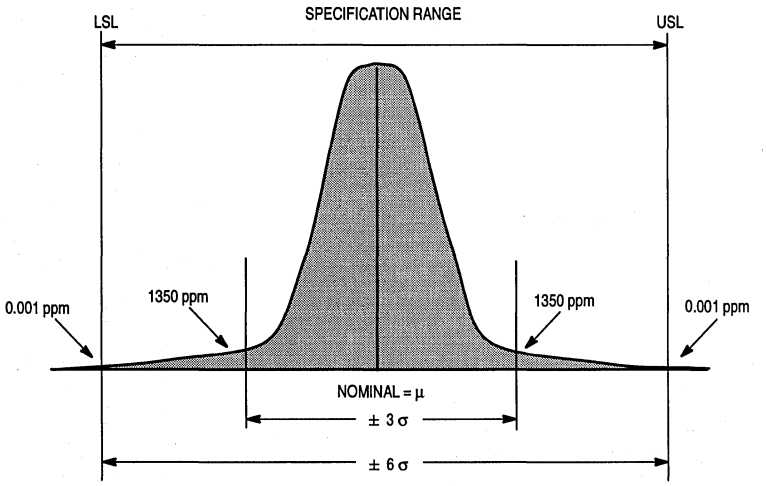
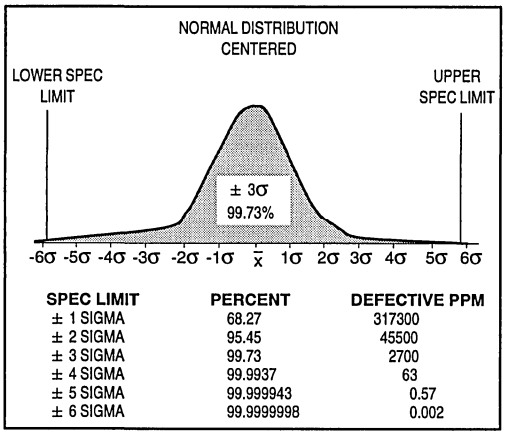
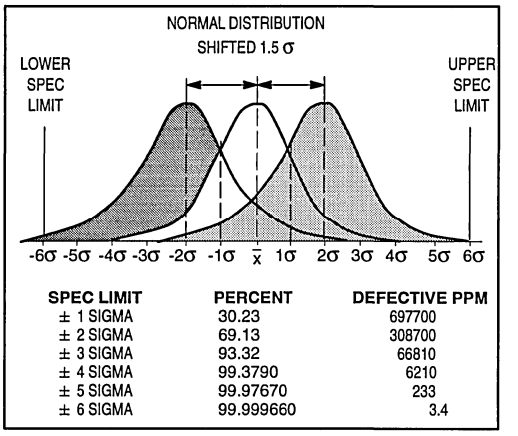


Figure 1. Standard distribution curve illustrates the Three Sigma and Six Sigma Parametric Conformance.



SPEC LIMIT	PERCENT	DEFECTIVE PPM
± 1 SIGMA	68.27	317300
± 2 SIGMA	95.45	45500
± 3 SIGMA	99.73	2700
± 4 SIGMA	99.9937	63
± 5 SIGMA	99.999943	0.57
± 6 SIGMA	99.9999998	0.002

Figure 2. With a Centered Distribution Between Six-Sigma Limits Only Two Devices Per Billion Fail to Meet the Specification Target.



SPEC LIMIT	PERCENT	DEFECTIVE PPM
± 1 SIGMA	30.23	697700
± 2 SIGMA	69.13	308700
± 3 SIGMA	93.32	66810
± 4 SIGMA	99.3790	6210
± 5 SIGMA	99.97670	233
± 6 SIGMA	99.999660	3.4

Figure 3. Effects of a 1.5 Sigma Shift Where Only 3.4 ppm Fail to Meet Specification.

The Six Sigma Latitude

Product yield is a factor of two variables: Process width and design width. If a process is adequately controlled so that its output is ± 3 Sigma, and if the product is so well designed that ± 3 Sigma deviations still place the products well within the specified design limits, then the overall yield is increased.

The table in Figure 2 shows that a design which can accept twice the normal ± 3 Sigma variation of the process (design width = ± 6 Sigma) will have a product yield of 99.9999998%, corresponding to 2.0 defective parts per billion. Even if the process mean were to shift by as much as ± 1.5 Sigma from the center of the distribution, the process would be expected to have no more than 3.4 parts per million defective.

It is Motorola's goal to achieve ± 6 Sigma capability in product design, manufacturing, sales and services by 1992.

The Motorola SPC Program

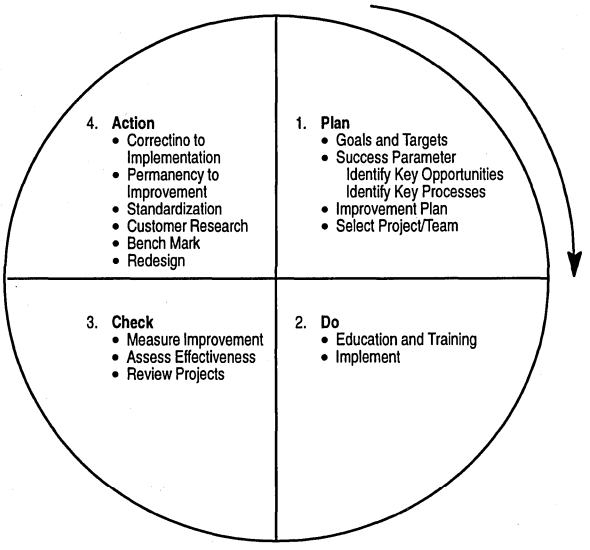
*** Purpose * Objective * Scope**

The Purpose of this program is to establish a standard approach toward continued process improvement through statistical process control.

Its Objective is to maintain all critical processes under tight statistical control in order to enhance quality and reduce scrap through identification of process variation, and through the reduction of these variations by means of real time corrective action. It is expected to establish the cultural environment and the organizational support required to achieve the Six-Sigma goal.

Its Scope encompasses a total quality improvement effort, involving design, manufacturing and management of all Motorola product groups and their suppliers as well as their support departments and vendors. It provides for the establishment of SPC teams and ensures adequate training. It serves as a liaison between teams in order to standardize and unify the approach to continuous quality improvement.

Continuous Improvement



Key Factors for Success

- Management Leadership
  - Top Down
  - Committed
  - Active
- Clear and Agreed-On Goals
- Breakthrough Thinking
- Project/Teamwork
- Training
- Reinforcing Successes

Verification of Statistical Process Control

Statistical process control programs have two specific functions:

1. as a monitor, to verify that a specific process is under control, or to indicate that a process is not in control based on interpretation of control-chart abnormalities or other indications;
2. as a quality improvement tool, for the purpose of improving process capability.

In either case, documentation must be available that permits the utilization, verification and interpretation of process control data, or if necessary, to implement new programs for process improvement.

Evidence of Process Capability

Capability indices must be established for each critical process and there must be evidence that the upper and lower specification limits are realistic and not arbitrary. The present goal is $C_p \geq 2.0$ and $C_{pk} \geq 1.5$.

Evidence of a process capability study must be on file. Depending on the level of sophistication, the study may include a factorial experiment, a nested variance study, summation of the results and recommendation for further action. The selection of critical process points must be justified.

Measurement System Capability

Results of measurement system capability study must be on file. Precision-to-Tolerance (P/T) ratio should be less than 0.10.

Process Control Specifications

Process specifications must include procedures to be followed in the event of a process requiring corrective action.

Operator Training

The operators are normally the first to see the control charts. Incorrect interpretation will cause unnecessary and time consuming investigations or delay needed studies. Consequently, operator training is a vital function and documented operator certification must be on file.

Control Chart Accuracy and Visibility

Control charts must be current and readily available. They shall be maintained by the production operators and upper and lower control limits must be calculated according to historical data.

Control Chart Tracking

Control charts must be tracked continuously. All out-of-control points must be highlighted and the appropriate corrective action described either on the chart or in a companion log. The objective is to view the trend, not simply to obtain a snapshot-in-time.

Supplier/Customer Relationships

Customers have no desire to control a supplier's process. Nor are they interested in the confidential details of a supplier's processes. They only want assurance (data) that a supplier has an ongoing program that supports an overall statistical process control plan. Primarily, Motorola's customers are interested in a supplier's statistical control of the critical processes, and his early warning system which keeps a process from becoming marginal. Most importantly, they are interested in what is being done for continuous improvement.

What We Offer Our Customers

It has been adequately demonstrated that a well monitored and controlled manufacturing process with minimum variations will produce a better, more useful and more reliable product at a reduced cost. In many instances, customer satisfaction now hinges not so much on a product's ability to meet specifications as on a manufacturer's ability to control his processes as evidenced by reduced variability. This is used as an indicator of both product quality and projected costs. Motorola provides detailed data and inferential statistics that allow customers to make decisions about the product they buy. In many instances, we provide a customer access to our computer data banks in order to improve communications and reduce turnaround time for product approval.

What We Expect From Our Suppliers

Improved quality of incoming material is crucial to success in achieving our Six Sigma goals. In order to accomplish this goal, we feel it necessary to reduce the number of suppliers and to work closely with those remaining as partners to resolve quality issues.

It is the responsibility of Motorola Supplier Quality Control to ensure that all suppliers maintain an adequate system of process and material controls which provides for prevention (as opposed to detection) of defects in their manufacturing processes. This includes, but is not limited to, the following:

- General plan for continuous improvement
- Detailed product flow
- Process control plan
- Equipment and process capability studies
- Measurement system capability studies
- Specific action plan for out-of-control conditions
- Evidence of statistical process control

Motorola's Reliability and Quality Monitor Philosophy

In order to guarantee that the high standards of reliability and quality required by the Motorola continue throughout the entire production lifetime of each product family, an ongoing Reliability Monitor/Audit Program is established.

Individual product and package family monitors are developed by identifying the appropriate device(s) for each process family (in most cases the same device used to qualify a process/product/package family). Once identified, the appropriate stress test programs are put in place to monitor the ongoing process average of the specific family. This process average measurement is made by understanding the reliability and quality results of individual samples. The stresses and sampling used vary according to the product technologies used and the unique requirements of the customer base. In all cases the monitors have been defined so as to quantify the progress being made toward sector goals of six sigma quality and significant reduction in infant mortality, and long term failure rates.

Monitor testing is completed on an ongoing cycle with test results made available quarterly. These reports detail all test results received for the previous quarter, outlining the reliability data associated with all process/package family types.

With all of these data, an effective ongoing monitor is established which is capable of identifying reliability trends associated with all process/product/package families.

For a complete description, order document BR518/D.

Reliability Stress Tests

The following summary gives brief descriptions of the various reliability tests included in a reliability monitor program. Not all of the tests listed are performed by each product group and other tests can be performed when appropriate. In addition some form of preconditioning may be used in conjunction with the following tests.

HIGH TEMPERATURE OPERATING LIFE

High temperature operating life (HTOL or HTRB) testing is performed to accelerate failure mechanisms which are thermally activated through the application of extreme temperatures and the use of biased operating conditions. The temperature and voltage conditions used in the stress will vary with the product being stressed. However, the typical stress ambient is 125°C, with the bias applied equal to or greater than the data sheet nominal value. All devices used in the HTOL test are sampled directly after final electrical test with no prior burn-in or other prescreening unless called out in the normal production flow. Testing can either be performed with dynamic signals applied to the device or in static bias configuration for a typical test duration of 1008 hours.

TEMPERATURE CYCLE

Temperature cycle accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed per MIL-STD-883 or MIL-STD-750 with the minimum and maximum temperatures being – 65°C and + 150°C. During temperature cycle testing, devices are inserted into a cycling system and held at the cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minute time period. The system employs a circulating air environment to assure rapid stabilization at the specified temperature. The dwell at each extreme, plus the two transition times of five minutes each (one up to the hot dwell temperature, another down to the cold dwell temperature), constitute one cycle. Test duration for this test will vary with device and packaging system employed. Typical test duration is for 1000 cycles with some tests extended to look for longer term effects.

THERMAL SHOCK

The objective of thermal shock testing is the same as that for temperature cycle testing — to emphasize the differences in expansion coefficients of the packaging system. However, thermal shock provides additional stress in that the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed per MIL-STD-883 or MIL-STD-750 with minimum and maximum temperatures being – 65°C to + 150°C. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes minimum, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five-minute dwells plus two ten-second transitions constitute one cycle. Test duration is for normally 1000 cycles with some tests being extended to look for longer term effects.

TEMPERATURE HUMIDITY BIAS

Temperature humidity bias (THB or H3TRB) is an environmental test performed at a temperature of 85°C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metalization. Most groups are tested to 1008 hours, with some groups extended beyond to look for longer term effects.

AUTOCLAVE

Autoclave is an environmental test that measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test. Typical test durations are 48 and 96 hours. This test may be followed by HTOL or HTRB for 24 to 48 hours to further accelerate the corrosion failure mechanism.

HAST/PTHB (PRESSURE-TEMPERATURE-HUMIDITY-BIAS)

This test is performed to accelerate the effects of moisture penetration with the dominant effect being corrosion. This test detects similar failure mechanisms as THB, but at a greatly accelerated rate. Conditions usually employed during this test are a temperature of 121°C or greater, pressure of 15 psig or greater, humidity of 100% (PTHB) or humidity of 85% (HAST), and a bias level that is the nominal rating of the device.

CYCLED TEMPERATURE HUMIDITY BIAS

This test is used to examine devices ability to withstand the combined effects of temperature cycling, high humidity, and voltage (test can be run without bias). This test differs from a typical humidity test in its use of temperature cycling. A typical test condition used is as follows: humidity = 90 to 98%, temperature cycle of 25°C to 65°C, and bias applied = nominal device rating. This test is usually run for 1008 hours.

POWER TEMPERATURE CYCLING

This test is performed on semiconductor devices to determine the effects of alternate exposures to extremes of high and low temperature with operating voltages periodically applied and removed. A typical test condition used is as follows: temperature cycle range = – 40°C to 125°C, bias applied = nominal device rating, and power cycling rate = 5.0 minutes (ON)/5 minutes (OFF). This test is usually run for 1000 cycles.

POWER CYCLING

This test is performed at a constant ambient temperature with operating voltage(s) periodically applied and removed, producing a ΔTJA, typically between 50°C and 150°C. Ambient temperatures range between 25°C and 150°C. A typical test condition used is as follows: ambient temperature 25°C, ΔTJA = 125°C with nominal bias, power "ON" 5.0 minutes and "OFF" 5.0 minutes. This test is usually run for at least 504 hours.

LOW TEMPERATURE OPERATING LIFE

This test is performed primarily to accelerate HCI (hot carrier injection) effects in semiconductor devices by exposing them to room ambient or colder temperatures with the use of biased operating conditions. Threshold shifts or parametric changes are typically the basis for failure. The length of this test will vary with temperature and bias conditions employed.

WRITE/ERASE CYCLING OF EEPROMs

This test is employed to evaluate the effects of repeated programming and erasing excursions on EEPROM devices without corruption of data. This write/erase cycling will usually be performed at an elevated operating temperature for greater than 10,000 cycles.

HIGH TEMPERATURE STORAGE/DATA RETENTION

High temperature storage is performed to measure the stability of semiconductor devices, including the data retention characteristics of EPROM and EEPROM devices, during storage at elevated temperatures with no electrical stress applied. The devices are typically exposed to an ambient of 150°C. An acceleration of charge loss from the storage cell or threshold changes are the expected results. All groups are typically tested to 1008 hours.

SYSTEM SOFT ERROR

System soft error is designed to detect errors caused by impact ionization of silicon by high energy particles. This stress is performed on a system level basis. The system is operated for millions of device hours to obtain an accurate measure of actual system soft error performance. This test is performed on memory devices only.

MECHANICAL SHOCK

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand a sudden change in mechanical stress typically due to abrupt changes in motion as seen in handling, transportation, or actual use. A typical test condition would be as follows: acceleration = 1500 g, orientation = Y1 plane, t = 0.5 ms, and number of pulse = 5.

VARIABLE FREQUENCY VIBRATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand deterioration due to mechanical resonance. A typical test condition is: peak acceleration = 20 g, frequency range = 20 Hz to 20 kHz, and t = 48 minutes.

CONSTANT ACCELERATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to indicate structural or mechanical weaknesses in a device/packaging system by applying a severe mechanical stress. A typical test condition used is as follows: stress level = 30 kg, orientation = Y1 plane, and t = 1 minute.

SOLDER HEAT

This test is used to examine the device's ability to withstand the temperatures seen in soldering over a more extended period as compared to the typical exposure levels seen in a production process. Electrical testing is the endpoint criterion for this stress.

LEAD INTEGRITY

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the mechanical properties of a device's leads, welds, and seals. Various conditions can be employed and provide for: tensile loading, bending stresses, torque or twist, and peel stress. The failure is determined visually under 3X to 10X magnification.

SALT ATMOSPHERE

This test is performed per MIL-STD-883 or MIL-STD-750 and is used to evaluate the corrosive effects of a seacoast type atmosphere on device and package elements. A failure is determined visually under 10X to 20X magnification.

Mechanical Data

8

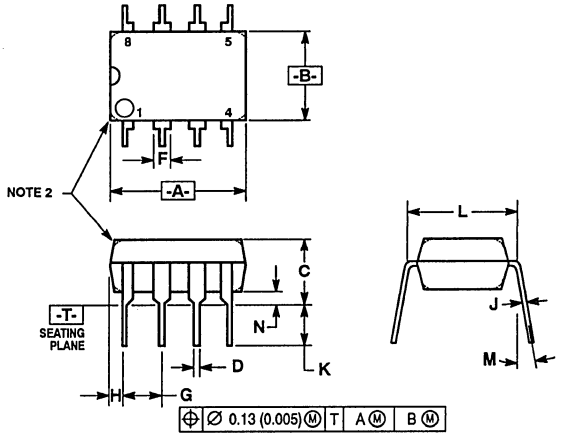
8

Mechanical Data

The package availability for each device is indicated on the front page of the individual data sheets. Dimensions for the packages are given in this chapter.

8-PIN PACKAGES

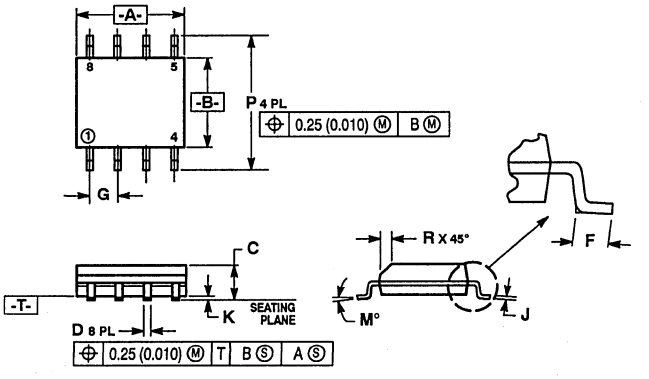
PLASTIC PACKAGE
CASE 626-05



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

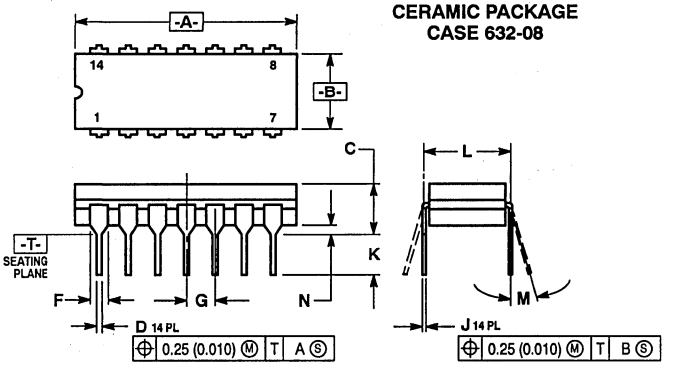
SO PACKAGE
CASE 751-04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIM: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

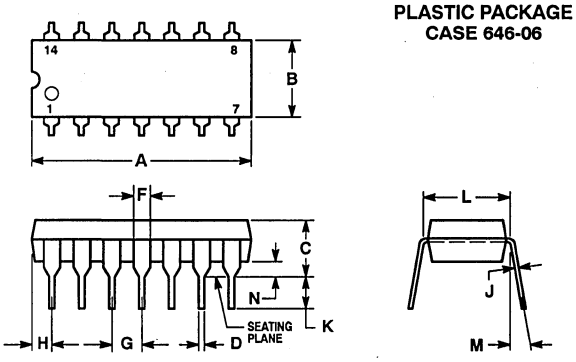
CERAMIC PACKAGE
CASE 632-08



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

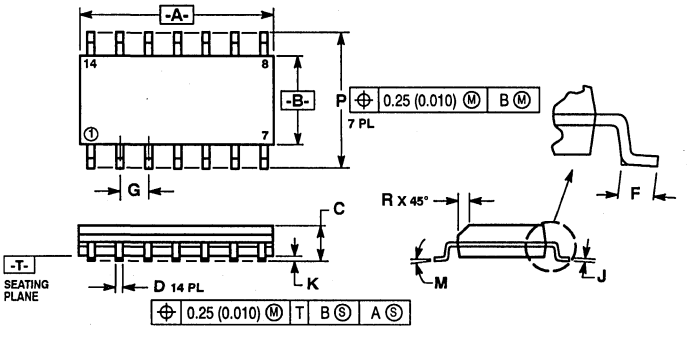
PLASTIC PACKAGE
CASE 646-06



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

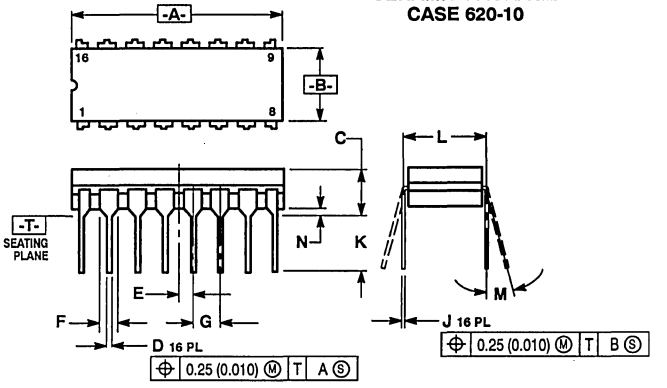
SO PACKAGE
CASE 751A-03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.299	0.244
R	0.25	0.50	0.010	0.019

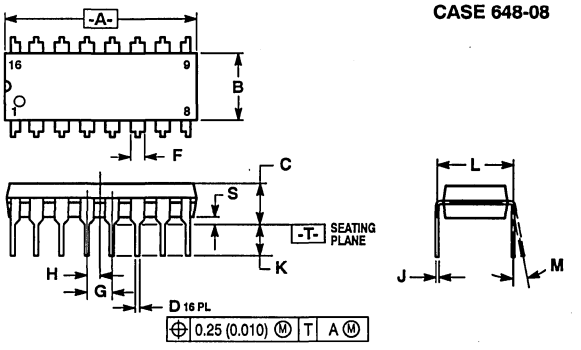
CERAMIC PACKAGE
CASE 620-10



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

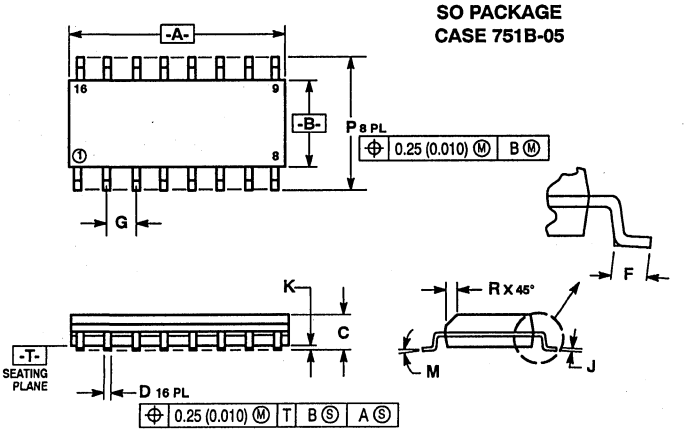
PLASTIC PACKAGE
CASE 648-08



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

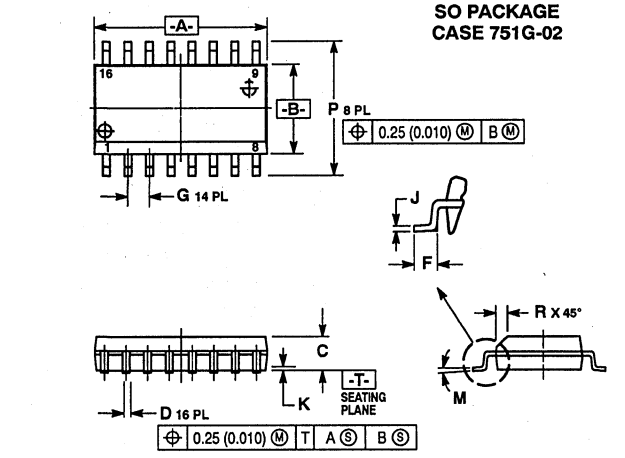
SO PACKAGE
CASE 751B-05



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

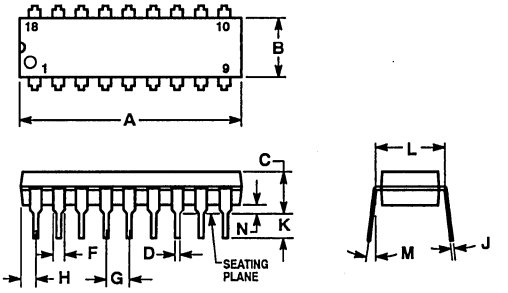
SO PACKAGE
CASE 751G-02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

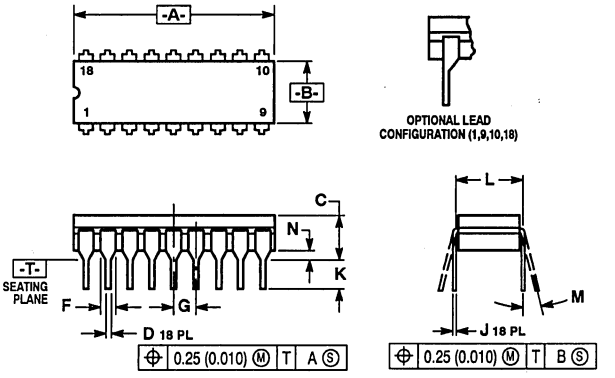
PLASTIC PACKAGE
CASE 707-02



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

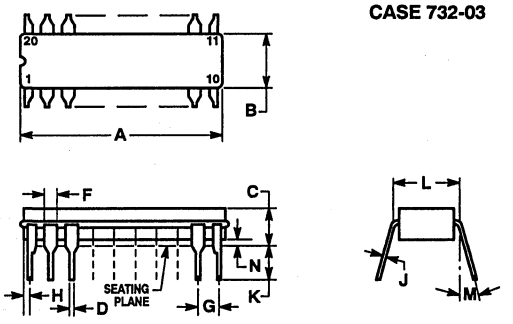
CERAMIC PACKAGE
CASE 726-04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

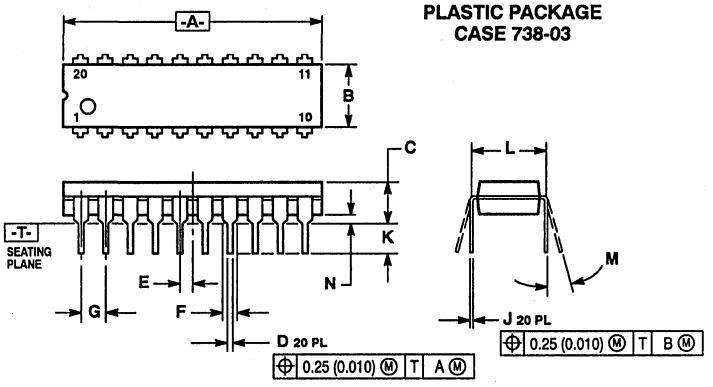
CERAMIC PACKAGE
CASE 732-03



NOTES:
1. LEADS WITHIN 0.25 (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

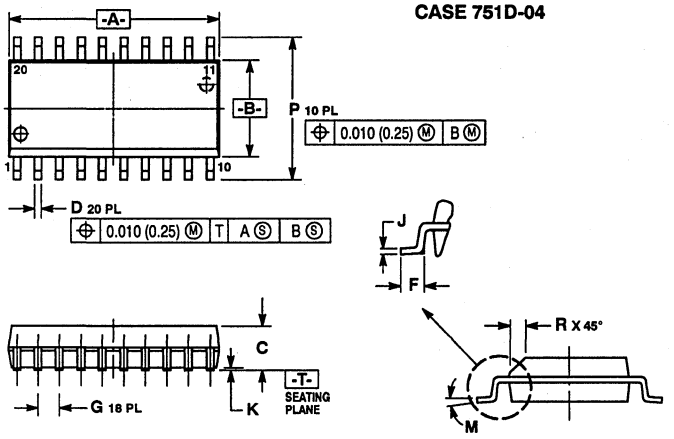
PLASTIC PACKAGE
CASE 738-03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

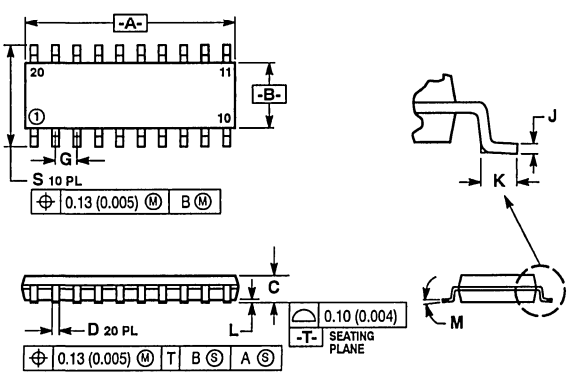
SO PACKAGE
CASE 751D-04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

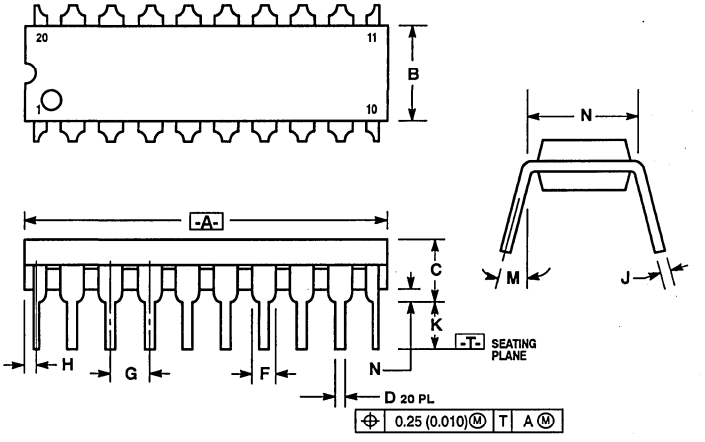
SO PACKAGE
CASE 751J-02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIM: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.55	12.80	0.494	0.504
B	5.10	5.40	0.201	0.213
C	—	2.00	—	0.079
D	0.35	0.45	0.014	0.018
G	1.27 BSC		0.050 BSC	
J	0.18	0.23	0.007	0.009
K	0.55	0.85	0.022	0.033
L	0.05	0.20	0.002	0.008
M	0°	7°	0°	7°
S	7.40	8.20	0.291	0.323

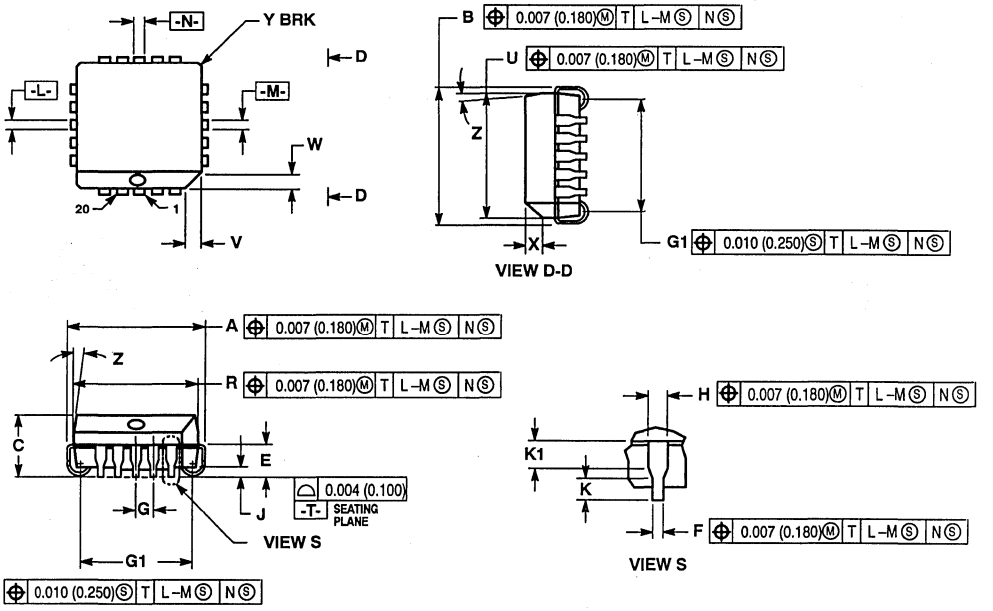
PLASTIC PACKAGE
CASE 804-01



NOTES:
9. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
10. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
11. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
12. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.930	0.970	23.63	24.63
B	0.240	0.260	6.10	6.60
C	0.150	0.170	3.81	4.31
D	0.015	0.022	0.38	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.030 NOM		0.76 NOM	
J	0.009	0.013	0.23	0.33
K	0.115	0.140	2.93	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

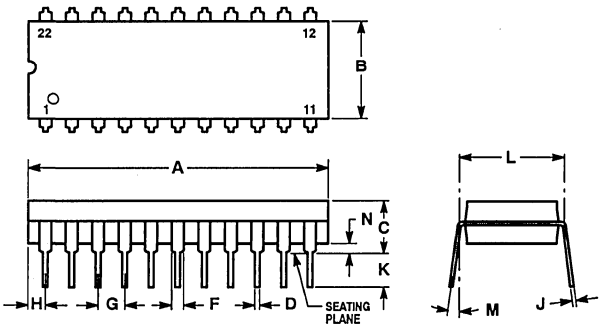
PLCC PACKAGE
CASE 775-02



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

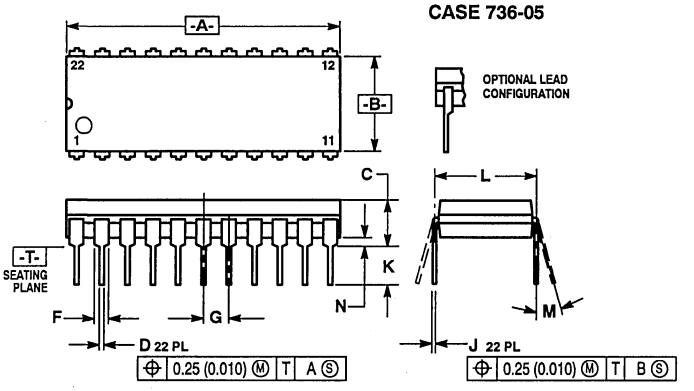
PLASTIC PACKAGE
CASE 708-04



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	27.56	28.32	1.085	1.115
B	8.64	9.14	0.340	0.360
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

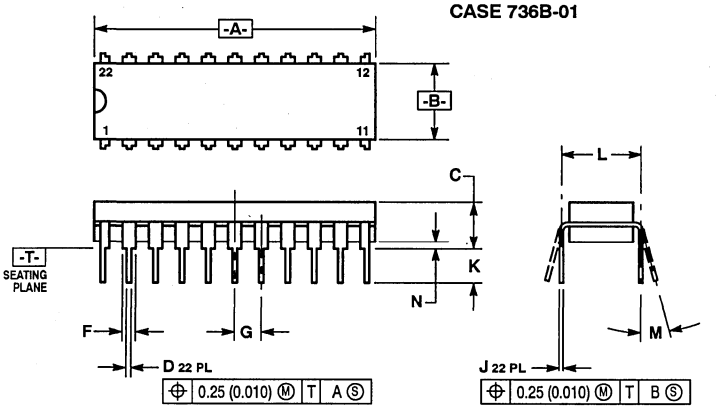
CERAMIC PACKAGE
CASE 736-05



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 11, 12, AND 22.
5. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.060	1.095	26.93	27.81
B	0.360	0.390	9.15	9.90
C	0.150	0.215	3.81	5.46
D	0.015	0.021	0.39	0.53
F	0.050	0.065	1.27	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.20	0.39
K	0.125	0.170	3.18	4.31
L	0.400 BSC		10.16 BSC	
M	0°	15°	0°	15°
N	0.020	0.050	0.51	1.27

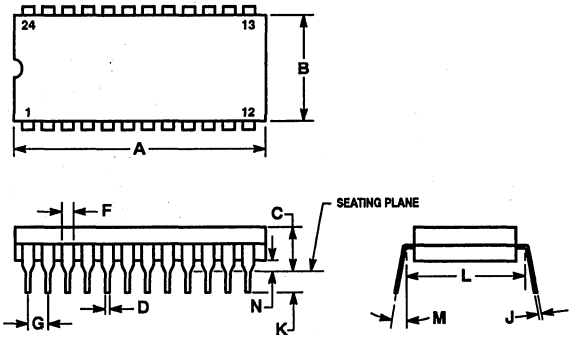
PLASTIC PACKAGE
CASE 736B-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.060	1.070	26.92	27.17
B	0.280	0.300	7.12	7.62
C	0.150	0.180	3.81	4.57
D	0.015	0.021	0.39	0.53
F	0.045	0.055	1.15	1.39
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.125	0.135	3.18	3.42
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

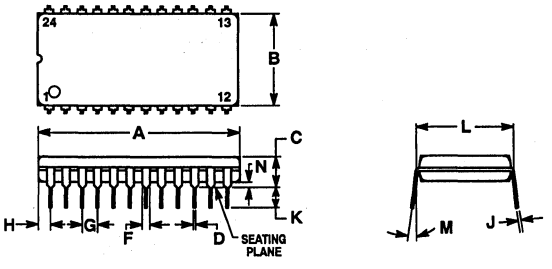
CERAMIC PACKAGE
CASE 623-05



NOTES:
1. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

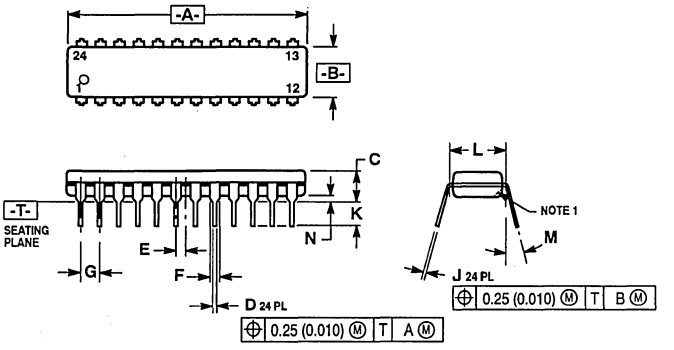
PLASTIC PACKAGE
CASE 709-02



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

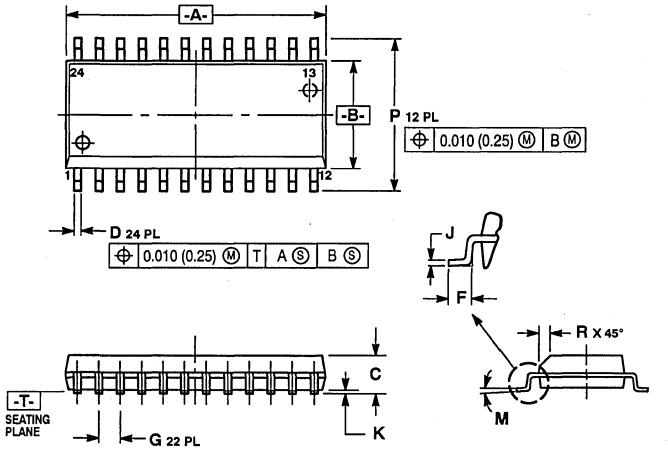
PLASTIC PACKAGE
CASE 724-03



NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

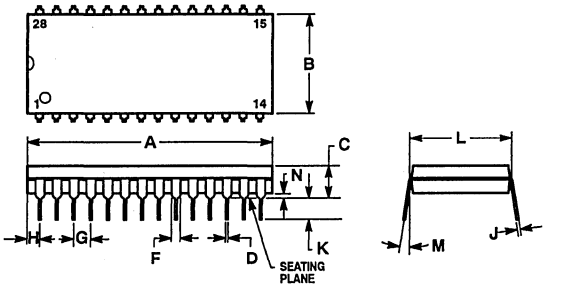
SO PACKAGE
CASE 751E-04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

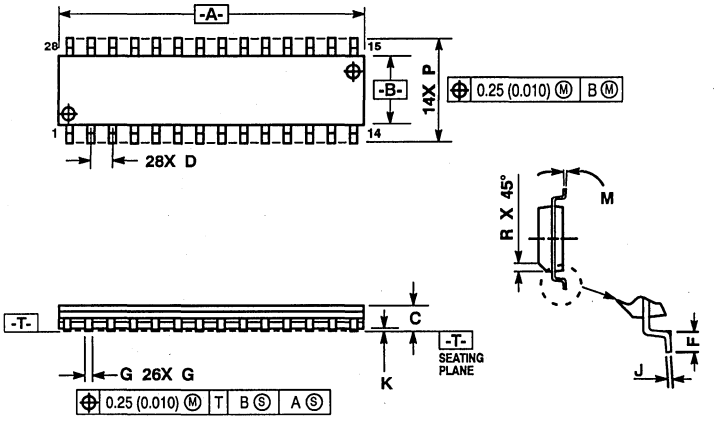
PLASTIC PACKAGE
CASE 710-02



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

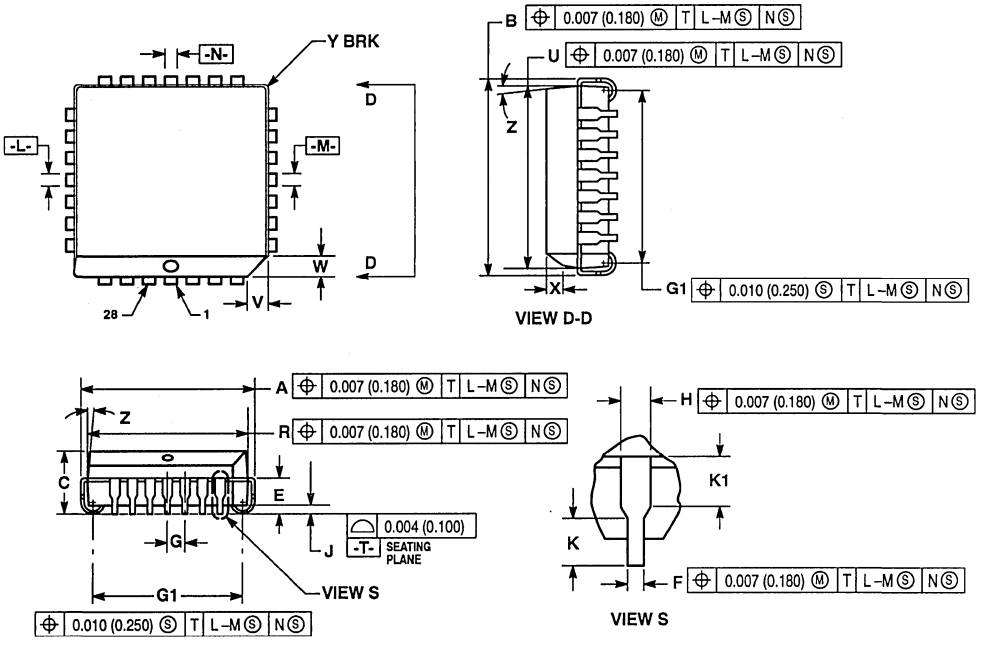
CERAMIC PACKAGE
CASE 751F-04



NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. DIMENSION "D" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF "D" DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

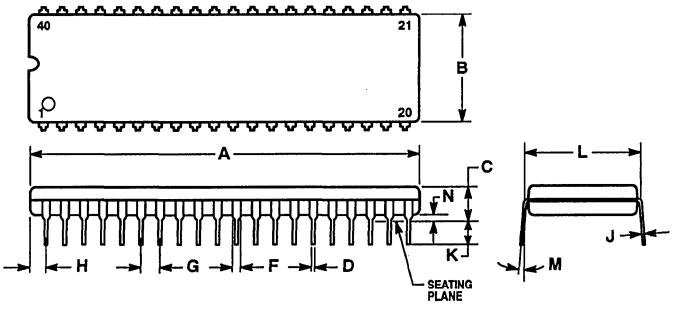
PLCC PACKAGE
CASE 776-02



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

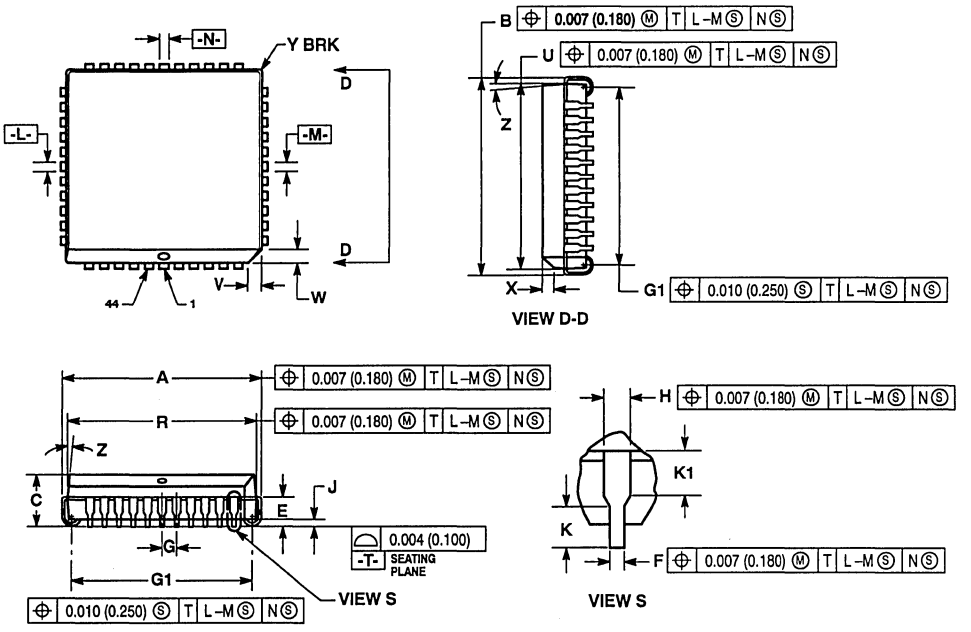
PLASTIC PACKAGE
CASE 711-03



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

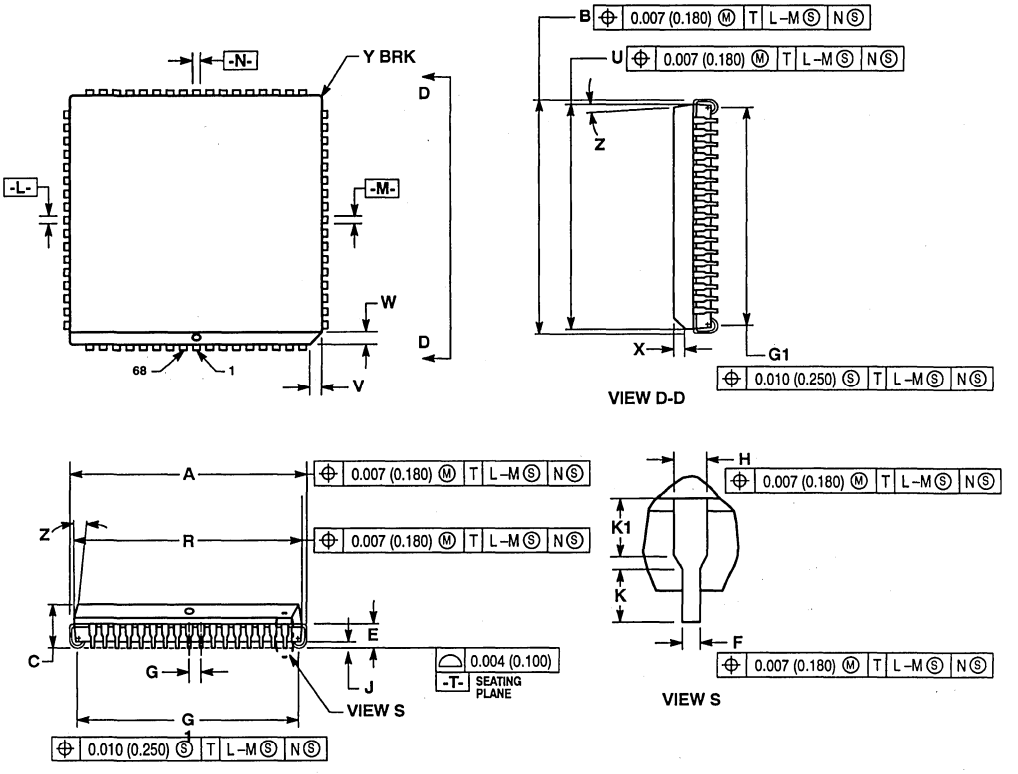
PLCC PACKAGE
CASE 777-02



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS (0.010) 0.25 PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

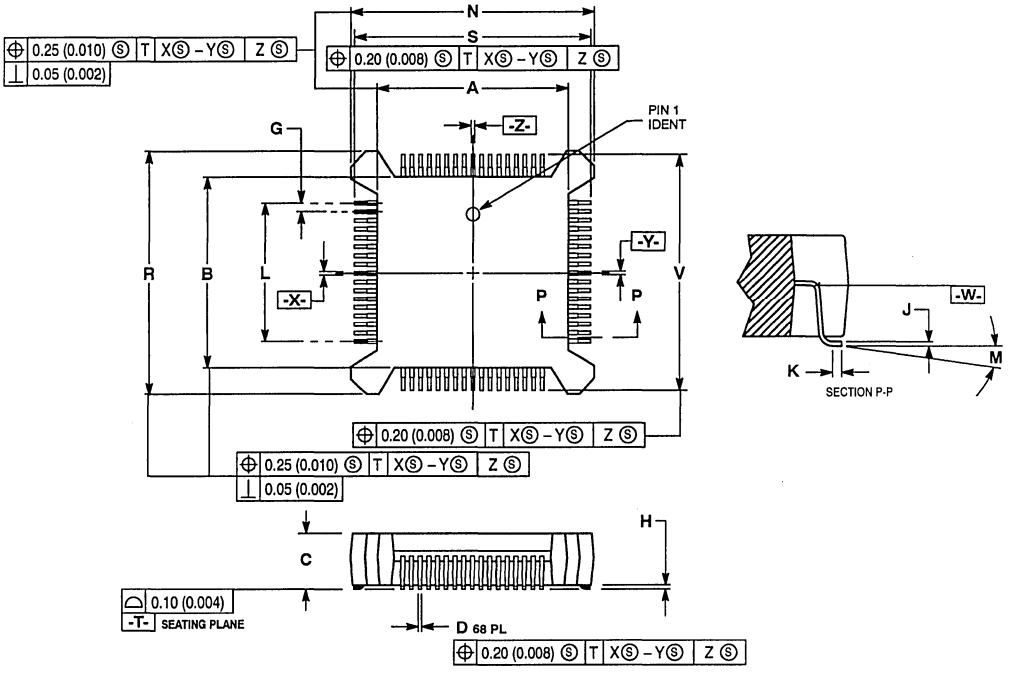
PLCC PACKAGE
CASE 779-01



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.985	0.995	25.02	25.27
B	0.985	0.995	25.02	25.27
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.950	0.956	24.13	24.28
U	0.950	0.956	24.13	24.28
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.910	0.930	23.12	23.62
K1	0.040	—	1.02	—

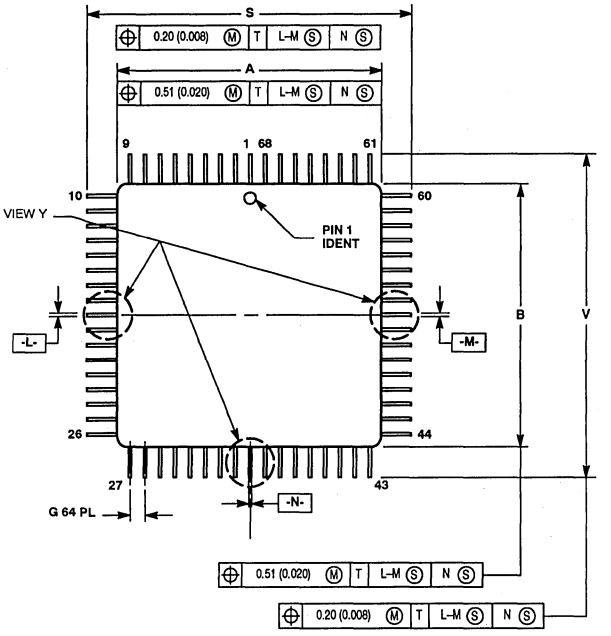
PLASTIC QUAD FLAT PACK (PQFP)
CASE 847-01

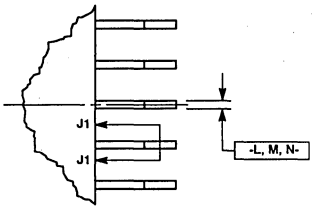


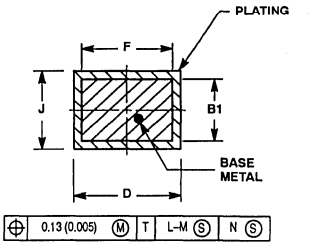
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A, B, N, AND R DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION FOR DIMENSIONS A AND B IS 0.25 (0.010), FOR DIMENSIONS N AND R IS 0.18 (0.007).
4. DATUM PLANE -W- IS LOCATED AT THE UNDERSIDE OF LEADS WHERE LEADS EXIT PACKAGE BODY.
5. DATUMS X-Y AND -Z- TO BE DETERMINED WHERE CENTER LEADS EXIT PACKAGE BODY AT DATUM -W-.
6. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM -T-.
7. DIMENSIONS A, B, N, AND R TO BE DETERMINED AT DATUM PLANE -W-.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.547	0.553	13.90	14.04
B	0.547	0.553	13.90	14.04
C	0.084	0.120	2.14	3.04
D	0.008	0.012	0.21	0.30
G	0.025 BSC		0.64 BSC	
H	0.004	0.019	0.11	0.40
J	0.006	0.008	0.16	0.20
K	0.020	0.030	0.51	0.76
L	0.400 REF		10.16 REF	
M	0°	8°	0°	8°
N	0.697	0.703	17.71	17.85
R	0.697	0.703	17.71	17.85
S	0.675	0.685	17.15	17.39
V	0.675	0.685	17.15	17.39

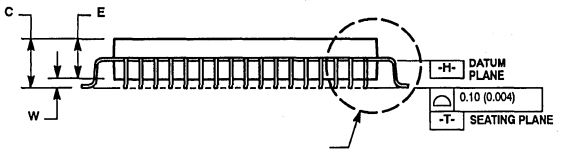
CERAMIC QUAD FLAT PACK (CQFP)
CASE 847B-01

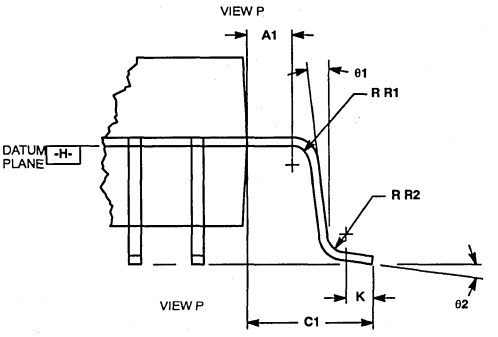






SECTION J1-J1
68 PL





NOTES:
1. ALL DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE CERAMIC BODY.
4. DATUMS L-M AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DEFINE MAXIMUM CERAMIC BODY DIMENSIONS INCLUDING GLASS PROTRUSION AND MISMATCH OF CERAMIC BODY TOP AND BOTTOM.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	21.85	22.86	0.860	0.900
B	21.85	22.86	0.860	0.900
C	3.94	4.31	0.155	0.170
D	0.204	0.292	0.0080	0.011
E	2.95	3.71	0.116	5
F	0.20	0.28	0.008	0.146
G	1.27 BSC		0.050 BSC	
J	0.13	0.20	0.005	0.008
K	0.51	0.76	0.020	0.030
S	27.31	27.55	1.075	1.085
V	27.31	27.55	1.075	1.085
W	0.64	0.88	0.025	0.035
A1	0.64	0.88	0.025	0.035
B1	0.10	0.15	0.004	0.006
C1	2.54 REF		0.100 REF	
R1	0.20 REF		0.008 REF	
R2	0.20 REF		0.008 REF	
θ1	0°	8°	0°	8°
θ2	0°	8°	0°	8°

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